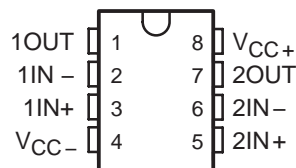


LF412C DUAL JFET-INPUT OPERATIONAL AMPLIFIER

SLOS010B – MARCH 1987 – REVISED AUGUST 1994

- Low Input Bias Current . . . 50 pA Typ
- Low Input Noise Current
0.01 pA/√Hz Typ
- Low Supply Current . . . 4.5 mA Typ
- High Input impedance . . . 10¹² Ω Typ
- Internally Trimmed Offset Voltage
- Wide Gain Bandwidth . . . 3 MHz Typ
- High Slew Rate . . . 13 V/μs Typ

D OR P PACKAGE
(TOP VIEW)



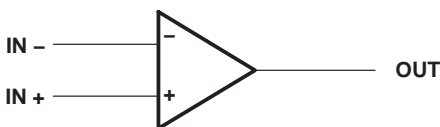
description

This device is a low-cost, high-speed, JFET-input operational amplifier with very low input offset voltage and a specified maximum input offset voltage drift. It requires low supply current yet maintains a large gain bandwidth product and a fast slew rate. In addition, the matched high-voltage JFET input provides very low input bias and offset currents.

The LF412C can be used in applications such as high-speed integrators, digital-to-analog converters, sample-and-hold circuits, and many other circuits.

The LF412C is characterized for operation from 0°C to 70°C.

symbol (each amplifier)



AVAILABLE OPTIONS

T _A	V _{IO} max AT 25°C	PACKAGE	
		SMALL OUTLINE (D)	PLASTIC DIP (P)
0°C to 70°C	3 mV	LF412CD	LF412CP

The D packages are available taped and reeled. Add the suffix R to the device type (ie., LF412CDR).

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V _{CC+}	18 V
Supply voltage, V _{CC-}	–18 V
Differential input voltage, V _{ID}	±30 V
Input voltage, V _I (see Note 1)	±15 V
Duration of output short circuit	unlimited
Continuous total power dissipation	500 mW
Operating temperature range	0°C to 70°C
Storage temperature range	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

NOTE 1: Unless otherwise specified, the absolute maximum negative input voltage is equal to the negative power supply voltage.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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LF412C

DUAL JFET-INPUT OPERATIONAL AMPLIFIER

SLOS010B – MARCH 1987 – REVISED AUGUST 1994

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{CC+}	3.5	18	V
Supply voltage, V_{CC-}	-3.5	-18	V

electrical characteristics over operating free-air temperature range, $V_{CC\pm} = \pm 15$ V (unless otherwise specified)

PARAMETER	TEST CONDITIONS	T_A †	MIN	TYP	MAX	UNIT
V_{IO} Input offset voltage	$V_{IC} = 0$, $R_S = 10$ k Ω	25°C		1	3	mV
α_{VIO} Average temperature coefficient of input offset voltage	$V_{IC} = 0$, $R_S = 10$ k Ω			10	20‡	μ V/°C
I_{IO} Input offset current§	$V_{IC} = 0$	25°C		25	100	pA
		70°C			4	nA
I_{IB} Input bias current§	$V_{IC} = 0$	25°C		50	200	pA
		70°C			8	nA
V_{ICR} Common-mode input voltage range			± 11	-11.5 to 14.5		V
V_{OM} Maximum peak output voltage swing	$R_L = 10$ k Ω		± 12	± 13.5		V
A_{VD} Large-signal differential voltage	$V_O = \pm 10$ V, $R_L = 2$ k Ω	25°C	25	200		V/mV
		Full range	15	200		
r_i Input resistance	$T_A = 25^\circ\text{C}$			10^{12}		Ω
CMRR Common-mode rejection ratio	$R_S \leq 10$ k Ω		70	100		dB
k_{SVR} Supply-voltage rejection ratio	See Note 2		70	100		dB
I_{CC} Supply current				4.5	6.8	mA

† Full range is 0°C to 70°C.

‡ At least 90% of the devices meet this limit for α_{VIO} .

§ Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive. Pulse techniques must be used that will maintain the junction temperatures as close to the ambient temperature as possible.

NOTE 2: Supply-voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously.

operating characteristics, $V_{CC\pm} = \pm 15$ V, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{O1}/V_{O2} Crosstalk attenuation	$f = 1$ kHz		120		dB
SR Slew rate		8	13		V/ μ s
B_1 Unity-gain bandwidth		2.7	3		MHz
V_n Equivalent input noise voltage	$f = 1$ kHz, $R_S = 20$ Ω		18		nV/ $\sqrt{\text{Hz}}$
I_n Equivalent input noise current	$f = 1$ kHz		0.01		pA/ $\sqrt{\text{Hz}}$



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LF412 MWC	ACTIVE	WAFERSALE	YS	0	1	RoHS & Green	Call TI	Level-1-NA-UNLIM	-40 to 85		Samples
LF412CD	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	0 to 70	LF412C	
LF412CDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LF412C	Samples
LF412CDRE4	ACTIVE	SOIC	D	8	2500	TBD	Call TI	Call TI	0 to 70		Samples
LF412CDRG4	ACTIVE	SOIC	D	8	2500	TBD	Call TI	Call TI	0 to 70		Samples
LF412CP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	LF412CP	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LF412CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LF412CDR	SOIC	D	8	2500	356.0	356.0	35.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
LF412CP	P	PDIP	8	50	506	13.97	11230	4.32



D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed $.006$ [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
 EXPOSED METAL SHOWN
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



4040082/E 04/2010

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

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