Design Guide: TIDM-02022

2kW 4-Phase Interleaved Buck Converter Reference Design with Coupled Inductors

Description

The significant growth of data center power consumption led an increase in demand for highly efficient DC/DC brick converters with high power density. Isolated topologies are prevalent but control is difficult. A multiphase synchronous buck topology with coupled inductors have better load transient performance and are easier to control compared to isolated topologies like inductor-inductor-capacitor (LLC). This reference design shows the control (Voltage mode) of power stage using a C2000™ microcontroller.

Resources

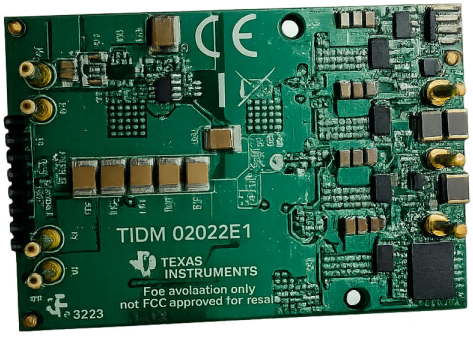
TIDM-02022	Design Folder
TMS320F28P550SJ	Product Folder
LMG3100R017	Product Folder
INA241x-Q1	Datasheet
C2000WARE-DIGITALPOWER-SDK	Product Folder

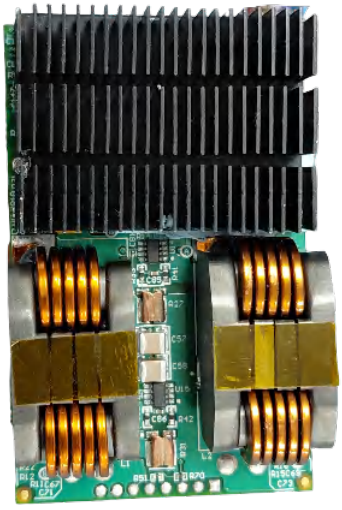
Features

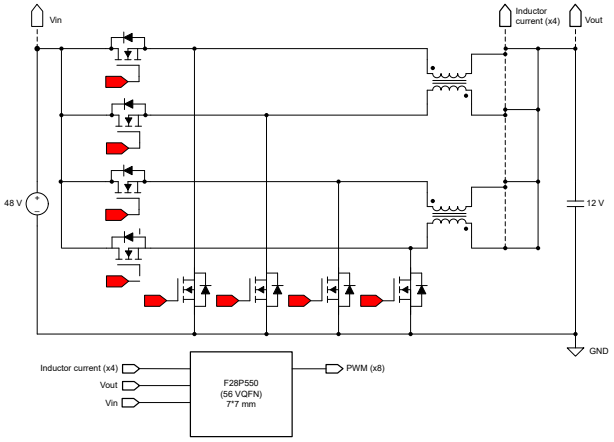
- 48V DC input, 12V DC output nominal, 2kW
- 200kHz pulse width modulation (PWM) frequency switching
- 200kHz interrupt service routine (ISR) frequency
- Greater than 98% peak efficiency
- Software frequency response analyzer (SFRA) and compensation designer for ease of tuning of control loop
- Voltage mode control loop
- Software support for F28P550 using driver library

Applications

- Power distribution board with 48V input
- Telecom DC/DC modules







1 System Description

The 48V to 12V stage in power supply of GPUs in data centers are mainly LLC converters. Control of LLC converters is complex. A non-isolated topology, like multiphase synchronous buck, can operate at the same efficiency with much easier control. Coupled inductors significantly improve the load transient response when negatively coupled. GaN modules and small package of C2000 MCU increase the power density.

A 4-phase interleaved synchronous buck is implemented with coupled inductors. The first two phases share one coupled inductor. The last two phases share one coupled inductor. This design provides an example of how to control a multiphase buck with coupled inductors using the C2000 MCU F28P550 device.

1.1 Key System Specifications

Table 1-1 shows the key power specifications for the 4-phase synchronous buck.

Table 1-1. Key Specifications of TIDM 02022

PARAMETER	SPECIFICATION
Input voltage (Vin)	40V to 60V, 48V DC nominal
Input current (Iin)	50A RMS Max
Output voltage (Vout)	12V DC nominal
Power rating	2kW
Efficiency	The peak is 98% The average is approximately 97%
Effective inductance due to coupling	5.4uH
Combined output capacitance (base board and module)	5.5mF
PWM switching frequency	200kHz
ISR frequency	200kHz

2 System Overview

2.1 Block Diagram

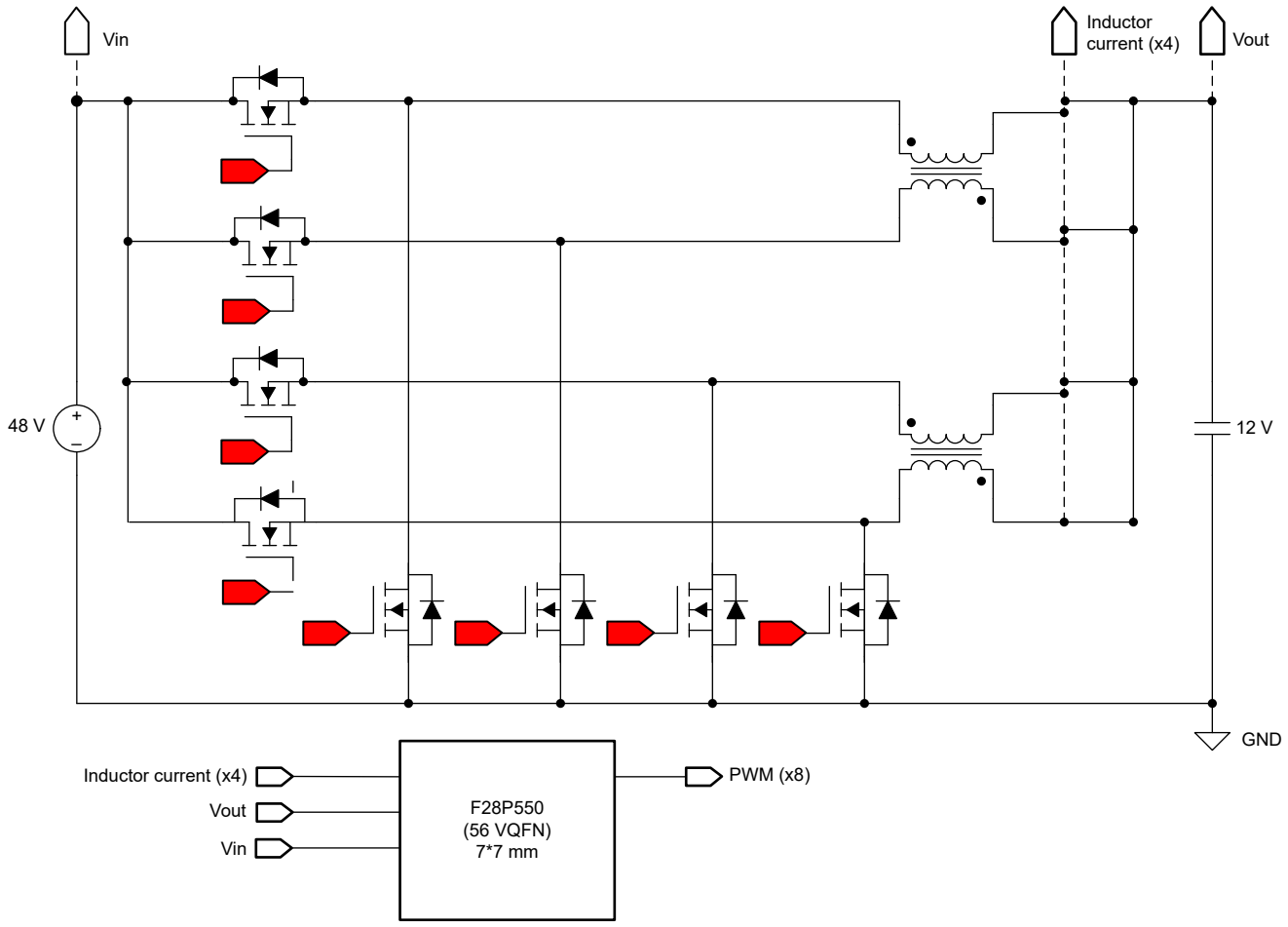


Figure 2-1. TIDM-02022 Block Diagram

2.2 Design Considerations

To realize the 48V–12V conversion in a quarter-brick form factor (36.8mm × 58.4mm), component selection is crucial. This section describes the high level details behind each part selection.

2.2.1 Microcontroller Unit

MCU is crucial for proper operation of the reference design. TMS320F28P550SJ C2000 device enables precise control in a space constrained quarter brick form factor. For achieving fast transient response for a load step, an use the software frequency response analyzer (SFRA) to make an appropriately tuned control loop. The analog comparators in the device enable protection for overcurrent.

2.2.2 GaN Power Stage

TI GaN power stages play a crucial role in this size-competitive module space due to the integrated FET + driver and the capability of higher switching, which reduces passive size. To deliver power up to 2kW and meet > 98.1% efficiency at mid-load, a four-phase interleaved design is considered with 1.7mΩ RDS(on). The LMG3100 provides different RDS(on) variants in the same package, which makes tuning the efficiency at different load and frequency conditions easy.

2.2.3 Inductor

To deliver 2kW total power, each phase inductor must support 42A current. The inductor must also support higher saturation current, depending on the inductor current ripple and derating. Choose a low direct current

resistance (DCR) inductor to reduce conduction losses that affect full load efficiency. The inductor size is another constraint. Four inductors must fit within a 36.8mm dimension to achieve a streamlined power flow across a 58.4mm dimension. The smallest catalog, single inductors with these ratings occupy a large board area. To address this issue, the design uses the ERUC23-2R2K coupled inductor from TDK®. In a coupled inductor, both phases share the same part of the core. Negative magnetic coupling between the two phases occurs, resulting in ripple cancellation. This magnetic coupling provides an added benefit of ripple cancellation at the output due to multiphasing. To achieve higher power and higher saturation rating for peak power delivery, choose a lower inductance value with a smaller DCR. An increase in the switching frequency can be required to reduce the ripple and switching losses in GaN.

The coupled inductor design offers several benefits:

- Reduced current ripple: Magnetic coupling between phases enables significant ripple current cancellation, resulting in lower current ripple throughout the circuit.
- Increased efficiency: Lower ripple currents reduce IRMS losses in GaN FETs, inductors, and PCB traces, helping improve converter efficiency overall.
- Faster transient response: Lower inductance can be used for the same ripple, meaning a coupled inductor design allows for faster response to load changes, often reducing the need for bulky output capacitors.
- Space and size savings: Using a single core for multiple windings requires less board area and potentially smaller magnetics for the same current ratings.

2.2.4 Cooling

One of the major aspects of this design is to dissipate heat efficiently through a heat sink and fan. This design uses heat sink which has approximately 2.2°C/W thermal resistance at 200 linear feet per minute (LFM) air flow. The design also uses a 1mm-thick thermal interface material (TIM) with 6W/m-K thermal conductivity. Using a thinner TIM can improve heat dissipation if there is enough distance between the heat sink and the LMG3100R017 exposed GaN die and capacitors for electrical isolation.

2.3 Highlighted Products

2.3.1 TMS320F28P550SG9

The C2000 MCUs are an optimized MCU family for real-time control applications. The fast and high quality analog-to-digital controller enables accurate measurement of the current and voltage signals, and the integrated comparator subsystem (CMPSS) integrates protection for overcurrent and overvoltage without using any external devices. The optimized CPU core enables fast execution of control loop. Trigonometric operations are accelerated using the on-chip trigonometric math unit (TMU), which imparts additional speedup in control loop execution.

2.3.2 LMG3100R017

The LMG3100 device is a 100V, 97A Gallium Nitride (GaN) FET with integrated driver. The device consists of a 100V GaN FET driven by a high-frequency GaN-FET driver.

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Hardware Requirements

- Base board with:
  - VIN input and VOUT output connector
  - Input and output capacitors
  - PMBus connector
  - Test points for VIN, VOUT measurement
  - 5V, 3.3V bias supply
    - The bias supply flashes the code when VIN is not applied)
- Horizontal mount card:
  - Four-phase buck power stage with auxiliary power and controller
- 100V, 60A programmable DC source
- 12V, 180A programmable DC load
- Two air cooling fans
  - The fans are essential to limit the temperature on board and to prevent efficiency value drop)

3.2 Software

The software of this design is available inside C2000Ware_DigitalPower_SDK

3.2.1 Opening the Project Inside Code Composer Studio

To start:

1. Install CCS
2. Install C2000Ware DigitalPower SDK from C2000WARE-DIGITALPOWER-SDK Software development kit (SDK) | TI.com
3. Open CCS
4. Below **Project > New CCS Project**
5. Click on **Import Wizard**
6. Browse to the C2000 DigitalPower SDK folder
7. Open **Solutions** folder
8. Select **tidm_02022** folder
9. Click **Finish**

3.2.2 Digital Power SDK Architecture

Once the project is imported, the Project Explorer appears inside CCS.

brick_dcdc.c and **brick_dcdc.h** files are in **brick_dcdc** folder. Lab environment setup files are n working directory.

brick_dcdc_main.c file consists of main framework of the project. This file consists of calls to the board files and algorithm specific files that help in creating the system framework, along with the interrupt service routines (ISRs) and slow background tasks.

brick_dcdc_settings.h file contains all the user settings, for selecting lab number, switching frequency, digital compensator coefficients, and so forth.

Brick_dcdc_vmc.syscfg file consists of all peripheral configurations.

3.2.3 Interrupt and lab structure

The project consists of one ISR1, which consists of control loop and PWM updates. The SOC2 of ADCB module triggers the ISR1. The ADC interrupt occurs at the end of the acquisition window of sampling. The ePWM1 module triggers the conversion with the event "Time-base counter equal to CMPB when the timer is incrementing."

The software of this reference design is organized in two labs. The first lab is an open loop operation, and second lab is a closed loop voltage mode control. Both labs are in **brick_dcdc.h** as shown in Figure 3-1.

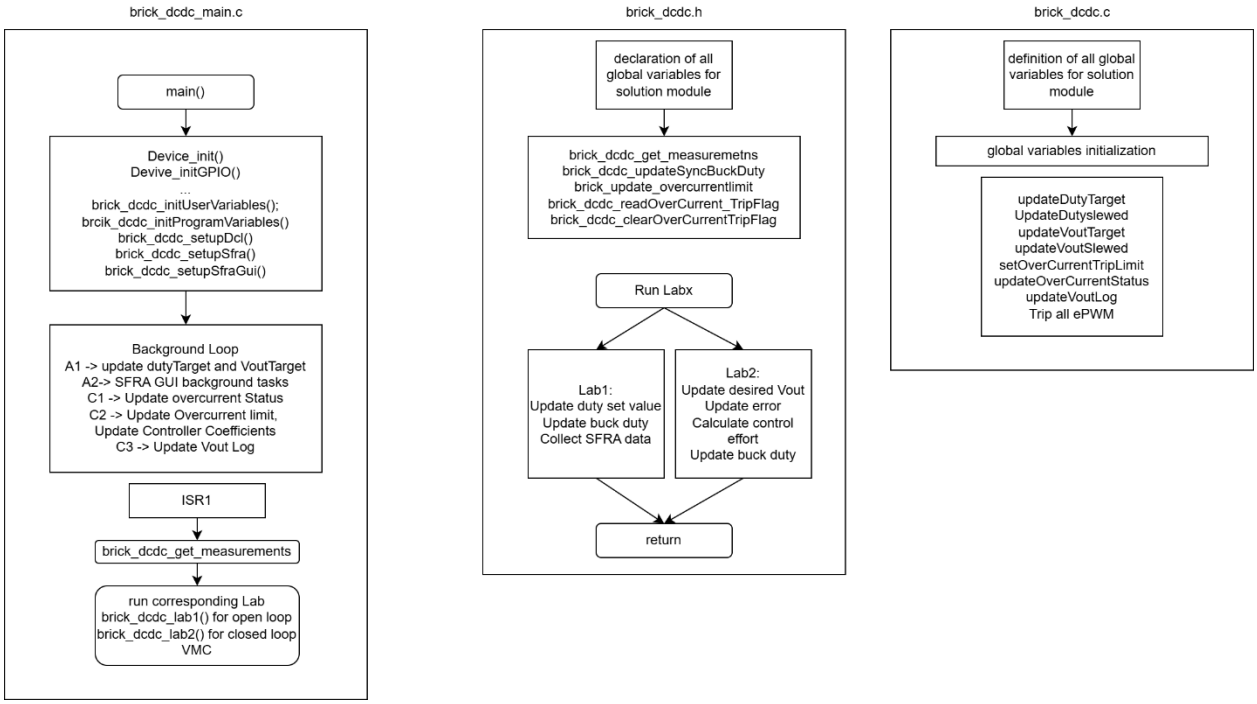


Figure 3-1. Software Flow Diagram

3.2.4 Labs structure and details

Figure Figure 3-2 shows the open loop voltage mode control from Lab 1. Figure 3-3 shows the closed loop voltage mode control from Lab 2

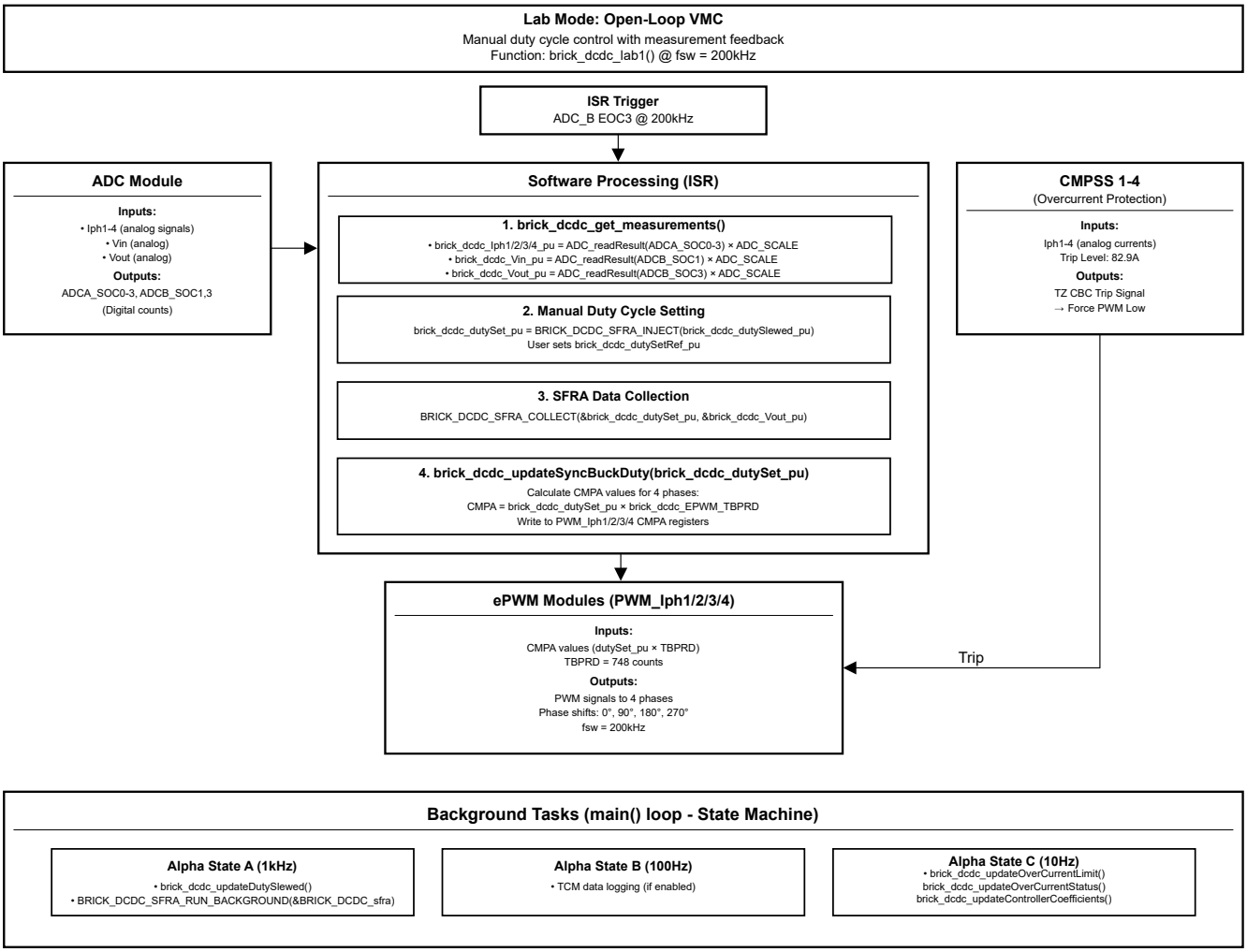


Figure 3-2. Software Diagram for Lab 1 - Open Loop

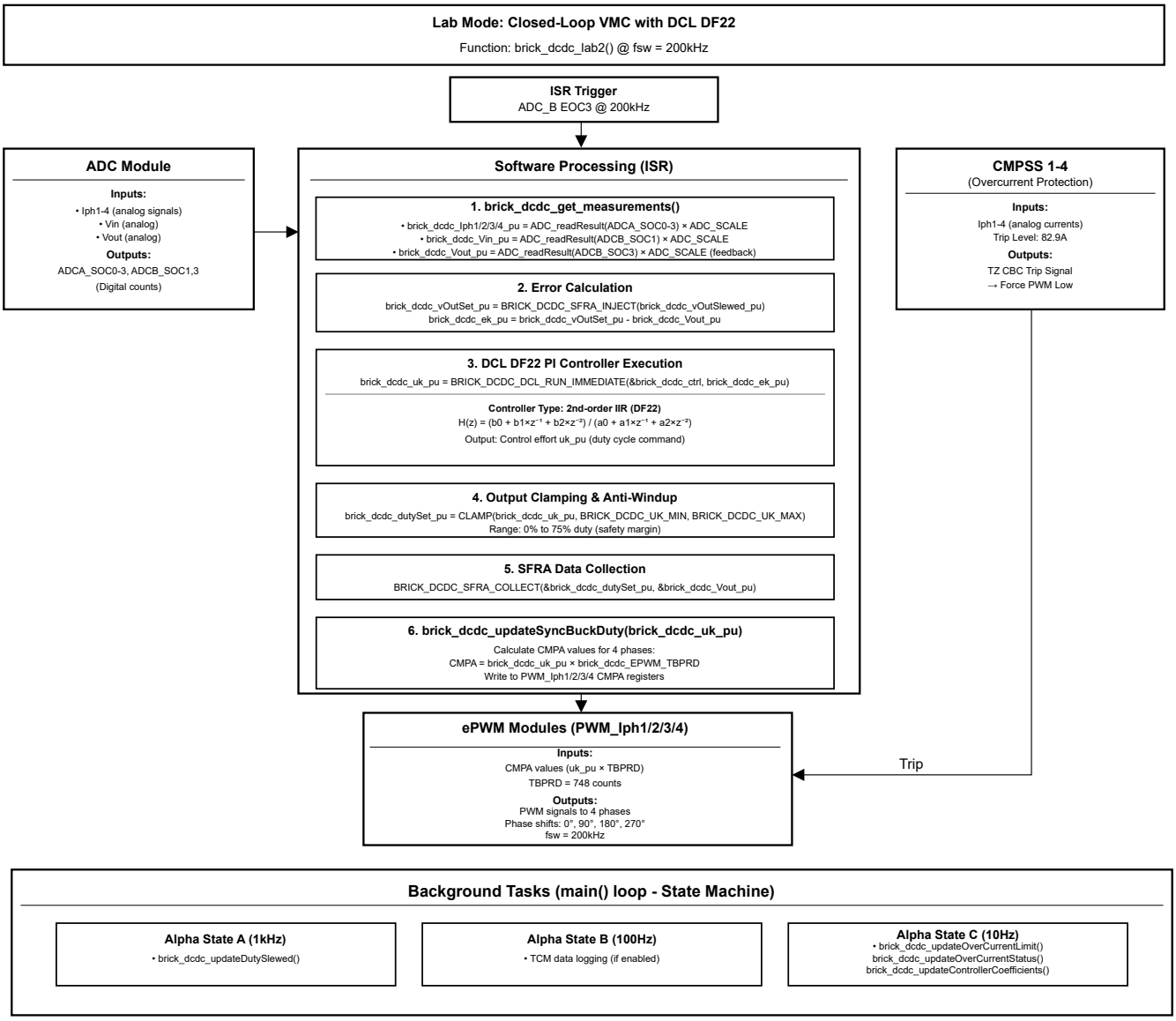


Figure 3-3. Software Diagram for Lab 2 - Closed Loop Voltage Mode Control

3.2.5 ADC Loading

ADC loading is as shown in Table 3-1.

Table 3-1. ADC Loading Architecture

	ADC_A	ADC_B
SOC0	Iph1 – A1	
SOC1	Iph2 – A9	
SOC2	Iph3 – A5	VOUT – B14
SOC3	Iph4 – A7	
SOC4		

3.2.6 Building, Loading and Debugging the Firmware

To build the project:

1. Right click on the project name
2. Click *Rebuild Project*. The project builds successfully.

To load the project:

1. In the Project Explorer, verify that the correct target configuration file is set as Active under targetConfigs (*.ccxml file).
2. Click *Run* → *Debug* to launch a debugging session.

In case of dual-CPU devices, a window can appear for the user to select the CPU on which the debug is to be performed. In this case, select CPU1. The project loads on the device and the CCS debug view becomes active. The code halts at the start of the main routine.

To debug the system, monitor the variables in the expressions window.

To populate this window with the correct variables:

1. Click *View* → *Scripting Console* to open the scripting console dialog box.
2. On the upper right corner of this console, click on *Open*
3. Navigate to the **setupdebugenv_lab1.js** or **setupdebugenv_lab2.js** script file located inside the project folder. These scripts populate the watch window with the appropriate variables needed to debug the system.
4. Enable the *Continuous Refresh* button on the watch window to continuously update the values from the controller

3.2.7 Protection Scheme

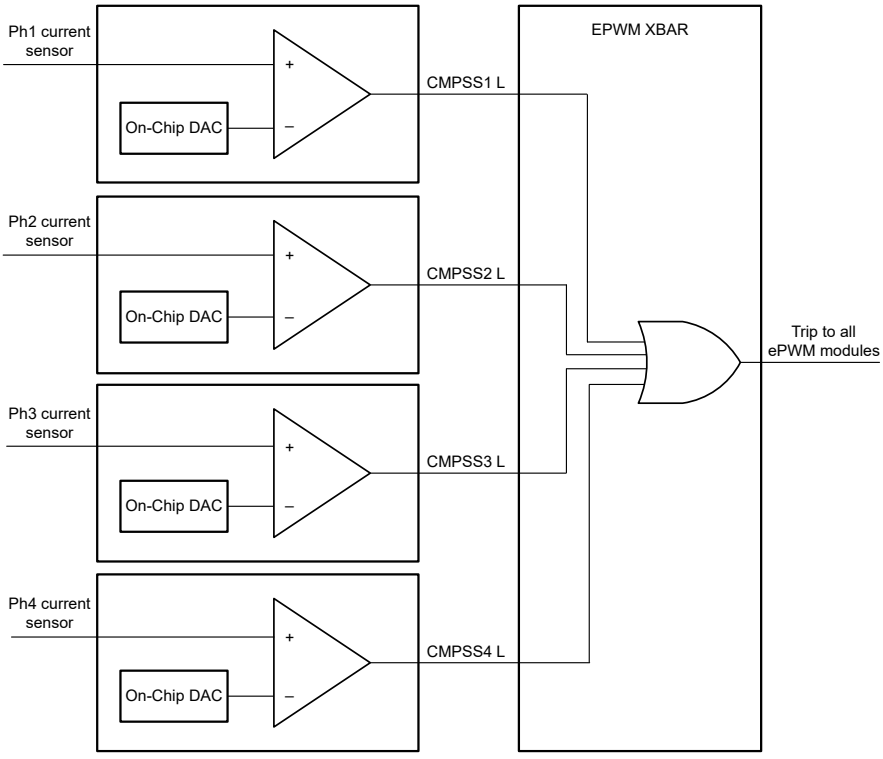


Figure 3-4. Diagram for Protection

The **brick_dcdc_readOverCurrentTripFlag()** and **brick_dcdc_ClearOvercurrentTripFlag()** functions are called periodically in a slow background task to update the trip flags.

3.2.8 PWM Switching Scheme

Figure 3-5 shows the PWM switching scheme. Only the PWM1 time base is shown. The other time bases are identical.

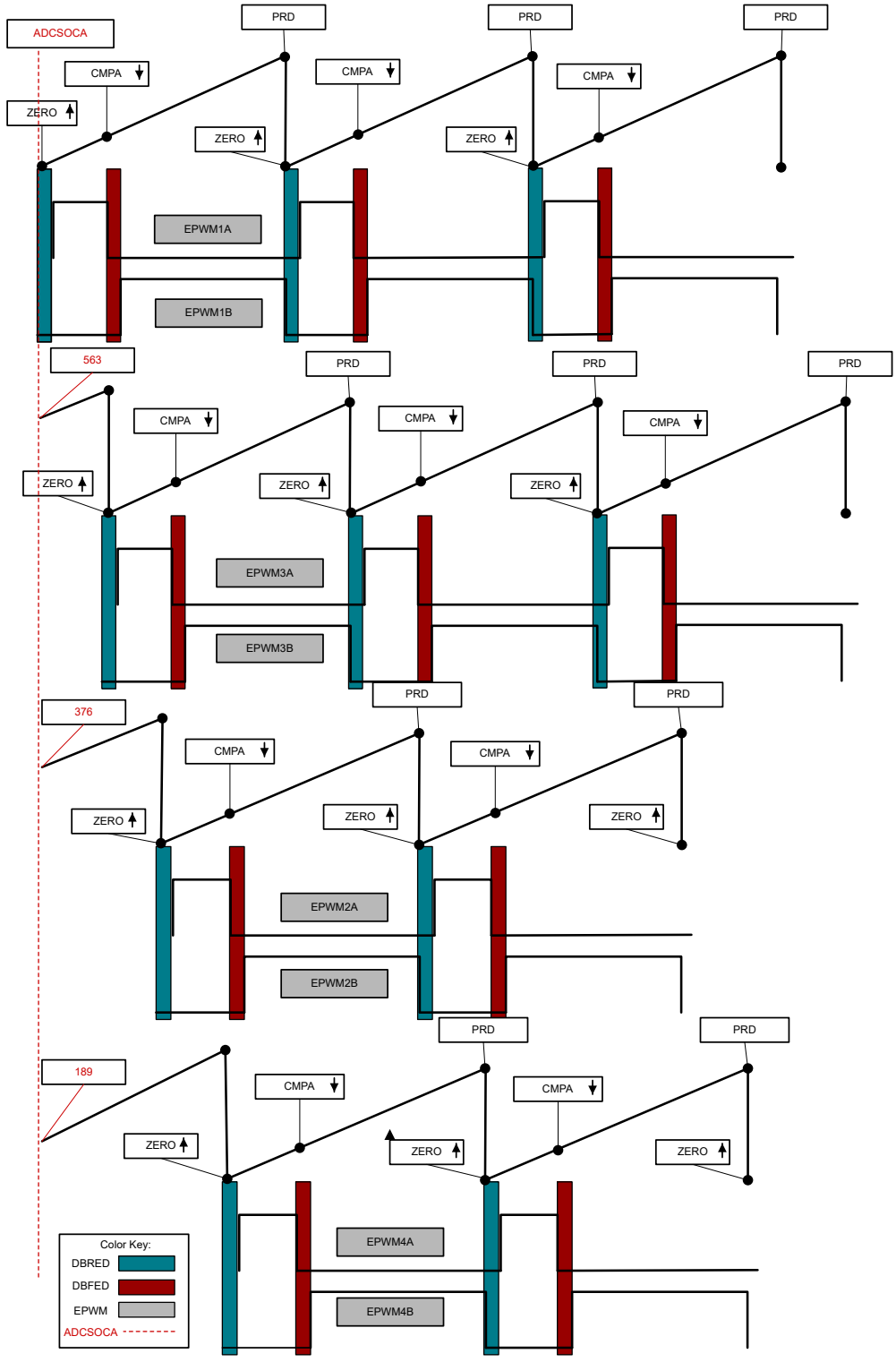


Figure 3-5. PWM Configuration

3.3 Test Setup

Complete the following steps for the test setup:

1. Insert the daughter card module into the base board.
2. Connect the 100V DC voltage source to the base board connector.
3. Set the input voltage ranges from 40V to 60V with current limit as 60A.
4. Place the fans near the heat sink and turn the fans on.
5. Connect the programmable DC load.
6. Upload the firmware to F28P550 device.
7. Turn on the DC source and increase the constant current (CC) load up to 167A.

3.4 Test Results

The following test results show that for a 12V output, peak efficiency is approximately 98.1% at 1000W output power and 48V input voltage. Using two fans keeps the temperature below 100℃.

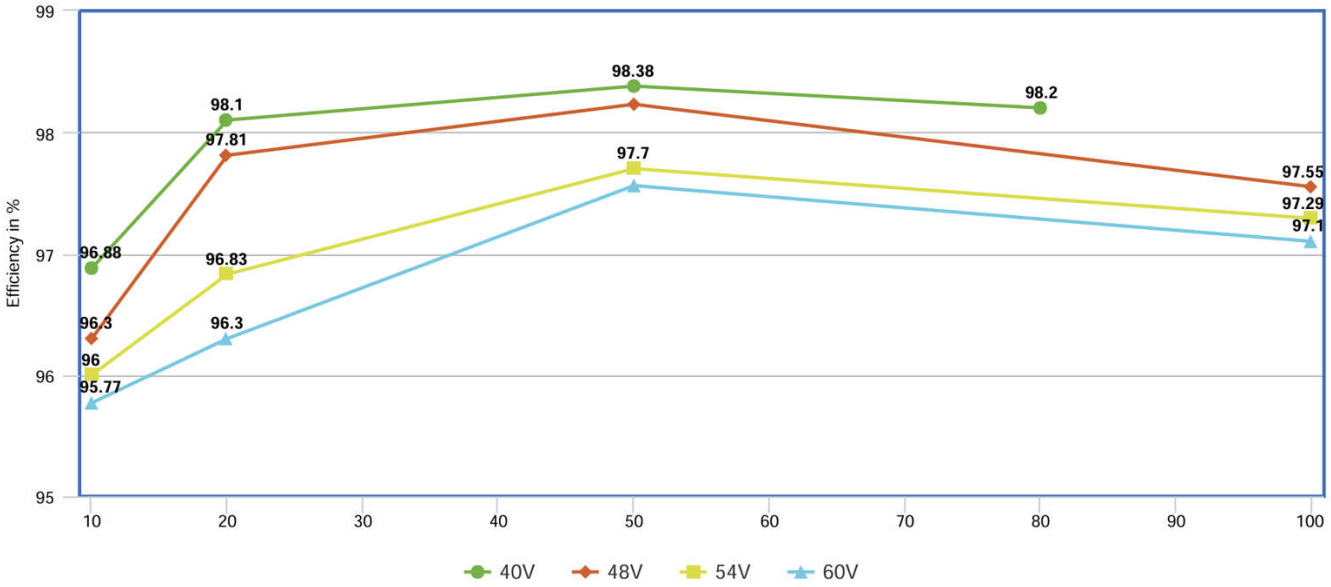


Figure 3-6. Efficiency versus Load (in % of Full Load)

Figure 3-7. Transient Response for 48V Input Voltage with 25% to 75% To 25% Load Changes with 5A/us

Figure 3-8 shows a thermal image capture (48V – 12V, 2kW, 25℃ ambient).

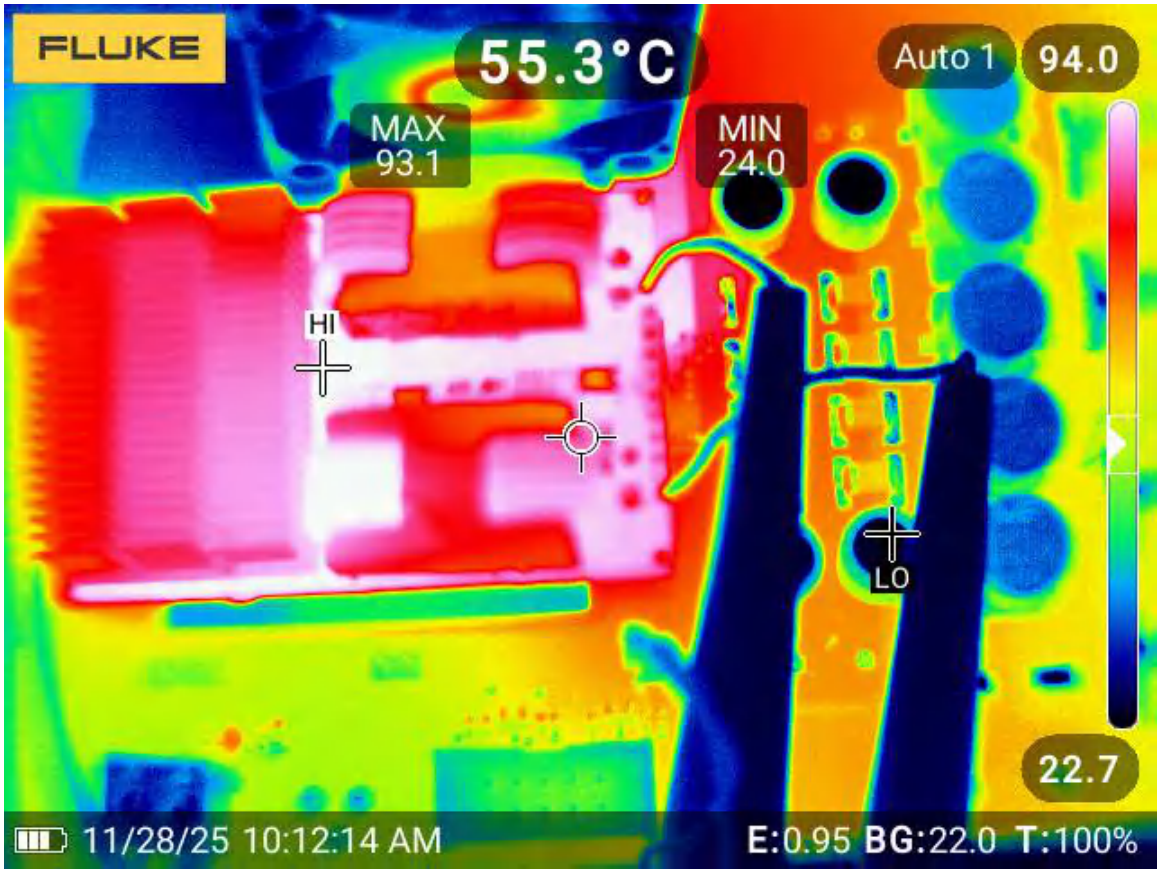


Figure 3-8. Thermal Image Captured at Full Load, 48V Input, 25℃ Ambient

4 Design and Documentation Support

4.1 Design Files

4.1.1 Schematics

Download the schematics from the TIDA-02022 Design Folder.

4.1.2 Bill of materials

Download the bill of materials (BOM) from the TIDA-02022 Design Folder.

4.1.3 PCB Layout Prints

Download the layer plots from the TIDA-02022 Design Folder.

4.1.4 Altium Project

Download the Altium Designer project files from the TIDA-02022 Design Folder.

4.1.5 Gerber Files

Download the Gerber files from the TIDA-02022 Design Folder.

4.2 Documentation Support

1. Texas Instruments, *TMS320F28P55x Real-Time Microcontrollers* datasheet
2. Texas Instruments, *LMG3100R017 100V, 97A GaN FET With Integrated Driver* datasheet
3. Texas Instruments, *Benefits of a multiphase buck converter* analog design journal
4. Texas Instruments, *Multiphase Buck Design From Start to Finish* application report

Trademarks

5 About the Authors

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Last updated 10/2025