Design Guide: TIDA-010970

Low-Noise, Highly Linear Digital Multimeter and Data Acquisition Signal Chain Reference Design

Description

The target application for this design includes digital multimeters (DMMs) that require ultra-high precision to measure dc signals. This design achieves effective dc accuracy using the ADS127L21B, a high-performance, 24-bit analog-to-digital converter (ADC) with effective linearity. An ultra-low drift buried Zener reference, REF81, calibrates the signal chain to eliminate gain and offset errors.

Resources

TIDA-010970	Design Folder
ADS127L21B, REF81	Product Folder
REF54, RES21A, RES11A	Product Folder
THP210, OPA828	Product Folder
MUX36S08, TMUX6104	Product Folder

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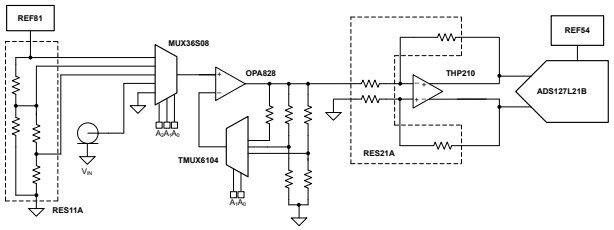
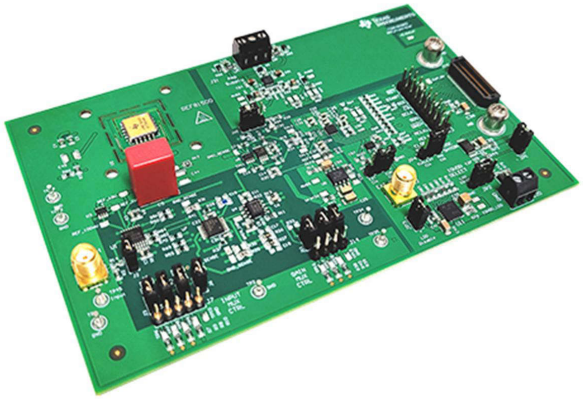


Features

- Ultra-low drift, low-noise reference for calibrating the entire signal chain, enabling high dc accuracy post-calibration
- Three input ranges: ±100mV, ±1V, ±10V
- Linearity: 1.1ppm maximum (±10V range)
- Noise: 335nV$_{RMS}$ at 60SPS (±10V range)

Applications

- Digital multimeter (DMM)
- Precision multifunction input and output DAQ
- Power analyzer
- Source measurement unit (SMU)



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1 System Description

This reference design is a linear, low-noise signal chain for systems that perform precision voltage measurements, including digital multimeters (DMMs), data acquisition (DAQ), source measurement units (SMUs), and other precision test and measurement applications. This document focuses on DMM applications.

DMMs need high linearity and low noise to accurately measure signals. Multiple input ranges are required to match signal levels with consistent resolution. Calibration corrects initial gain and offset errors.

This design features a precision resistor network, RES21A, and a high-performance data converter, ADS127L21B, to achieve effective linearity and noise performance. OPA828 and TMUX6104 create a programmable gain input amplifier, which allows for multiple input ranges. This design also has an onboard calibration source, REF81, to calibrate out gain and offset errors from the entire signal chain.

1.1 Key System Specifications

Table 1-1 presents the key system specifications implemented in this reference design.

Table 1-1. Key System Specifications

RANGE	NOISE	LINEARITY (MAXIMUM)
±10V range	335nV$_{RMS}$ at 60SPS	1.1ppm
±1V range	547nV$_{RMS}$ at 60SPS	0.6ppm
±100mV range	3.23µV$_{RMS}$ at 60SPS	3.0ppm

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2 System Overview

2.1 Block Diagram

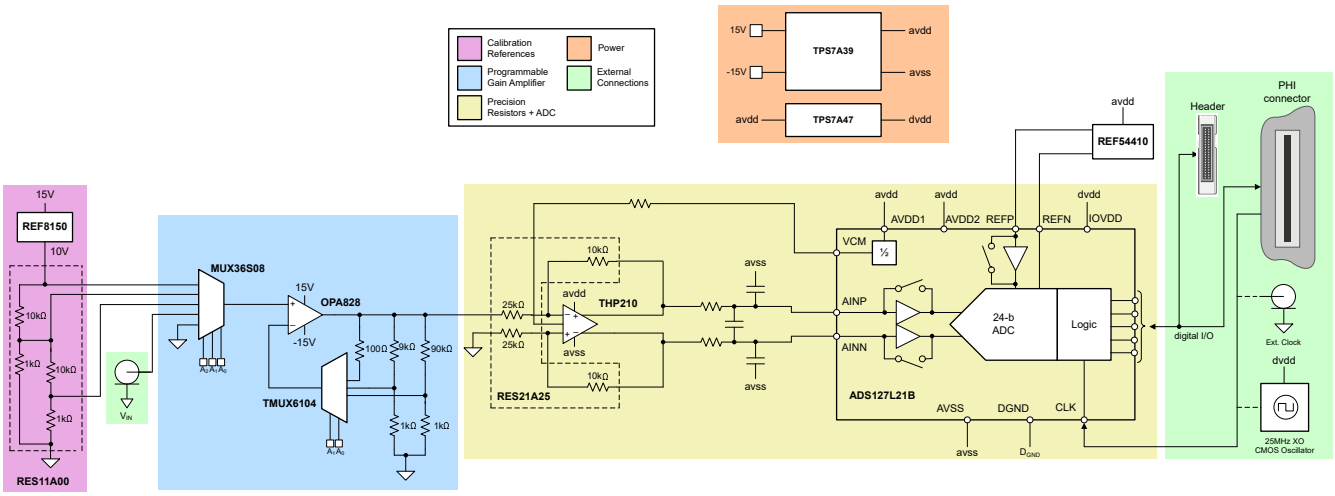

Figure 2-1. TIDA-010970 Block Diagram

2.2 Design Considerations

DMMs are classified by the number of digits the DMM can display on the screen. For example, a 6.5-digit DMM can display 6 whole digits (a digit that ranges from 0 to 9), and a leading digit that can display a 0 or a 1. The leading digit is a half digit since the digit can only display two values. Therefore, a 6.5-digit DMM has a measurement range of ±1999999, or 2,000,000 counts. Each DMM digit adds another order of magnitude of resolution. For example, a 6.5-digit DMM has 10 times more counts than a 5.5-digit DMM, and a 7.5digit DMM has 10 times more counts than a 6.5digit DMM. High-resolution DMMs with 6.5 digits or more are used to measure sensitive dc signals with high resolution.

DMMs have input different ranges to accommodate different signal levels ranging from tens or hundreds of volts to millivolts or microvolts. Multiple ranges allows the DMM to measure smaller signals with the same resolution as larger signals. For example, a 6.5 DMM meter with only one range, 0V to 10V, measures a 10V signal as 10 ±0.00005V. This same DMM measures a 100mV signal as 0.1 ±0.00005V, which translates to 4.5 digits of resolution. A DMM with multiple ranges, such as 10V, 1V, and 100mV, measures a 100mV signal as 100 ±0.00005mV, which is 6.5-digit resolution.

The DMM signal chain must have as little error as possible to accurately measure signals across input ranges. Calibration can remove initial gain and offset errors from the signal chain, and continuous calibration can remove temperature and long-term drift. However, the calibration is only as good as the accuracy of the calibration source.

Errors from noise and nonlinearities are still present even if a DMM signal chain is calibrated for gain and offset errors. Integral non-linearity (INL) is a measure of the deviation of the system output to the linear theoretical output after correcting for offset and gain errors. Noise is any unwanted signal that interferes with the signal chain. Noise cannot be fully eliminated from any signal chain because noise is inherent to any electronic component. Nonlinearities and noise are difficult to calibrate, so choosing low-noise, linear devices is the best way to minimize the noise and nonlinearities in a signal chain.

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2.3 Highlighted Products

This design uses many precision components to achieve the desired performance.

2.3.1 ADS127L21B

The ADS127L21B is a high-precision, 24-bit, delta-sigma (ΔΣ), analog-to-digital converter (ADC) featuring programmable digital filters. This digital filter has data rates up to 512kSPS using the wideband filter and up to 1365kSPS using the low-latency sinc filter. The device offers an excellent combination of ac performance and dc precision with low power consumption.

The low-drift modulator achieves excellent dc precision and an industry-leading INL specification of 0.8ppm (0°C to 70°C) and outstanding ac performance with low wideband noise. The power-scalable architecture features four speed modes to optimize data rate, resolution, and power consumption. Signal and reference input buffers reduce driver loading for increased accuracy.

2.3.2 REF81

The REF81 integrates a precision resistor divider with a 7.6V buried Zener output, providing precision voltage references which can be used with high-performance data converters. The integrated resistor pair is matched to provide best-in-class temperature drift and long-term stability. An internal heater provides integrated temperature control to enable a constant reference voltage despite ambient temperature variations. This integrated heater allows REF81 to achieve an extremely low temperature drift of 0.05ppm/°C. The device integrates temperature control and a precision divider, which eliminates design complexities. This provides fast design cycles, easy bring up and no dependence on high-cost external precision components for temperature control and voltage generation.

The REF81 family is available in a 20-pin LCCC package. The LCCC package is a hermetically-sealed ceramic package that enables ultra-low, long-term stability specification of 1ppm, critical for applications that demand a long time period without calibration. The package also offers excellent immunity against humidity variation.

2.3.3 REF54

The REF54 is a high-precision, low-drift, low current consumption voltage reference device. The REF54 offers low temperature drift coefficient (0.8ppm/°C), low noise (0.11ppm$_{p-p}$), and high accuracy (±0.02%) while consuming 380µA current. The REF54 helps systems meet the strict performance requirements of high-precision applications, with low long-term drift (3ppm LCCC; 25ppm SOIC). The device is designed as a companion device for high-resolution data converters such as ADS127L21B.

2.3.4 RES21A

The RES21A is a matched pair of resistor dividers implemented in thin-film SiCr with Texas Instruments' modern, high-performance, analog CMOS process. The device has a nominal input resistance of 10kΩ for low thermal and current noise, and is available in several nominal ratios to meet a wide array of system needs. Use the RES21A in an inverse gain configuration by simply rotating the device placement by 180°. This feature supports layout reuse and increases flexibility for applications such as discrete instrumentation or difference amplifier implementations. The RES21A series features high ratio-matching precision, within ±500ppm of the nominal and a maximum ratio drift of only ±2ppm/°C.

2.3.5 THP210

The THP210 is an ultra-low-offset, low-noise, high-voltage, precision, fully differential amplifier that easily filters and drives fully differential signal chains. The THP210 is also used to convert single-ended sources to differential outputs as required by high-resolution ADCs. Designed for exceptional offset, low noise, and Total Harmonic Distortion (THD), the bipolar super-beta inputs yield a very-low noise figure at very-low quiescent current and input bias current. This device is designed for signal conditioning circuits that require low power consumption and excellent signal-to-noise ratio (SNR). The THP210 features high-voltage supply capability up to ±18V. This capability allows high-voltage differential signal chains to benefit from dynamic range without adding separate amplifiers for each polarity of the differential signal. Very-low voltage and current noise enables the THP210 to be used in high gain configurations with minimal impact to the signal fidelity.

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2.3.6 OPA828

The OPA828 and OPA2828 (OPAx828) Junction Field Effect Transistor (JFET) input operational amplifiers combine high speed with high dc precision and ac performance. These op amps supply low offset voltage, low drift overtemperature, low bias current, and low noise with only 60nV$_{RMS}$, 0.1Hz to 10Hz noise. The OPAx828 operates over a wide supply-voltage range of ±4V to ±18V and a supply current of 5.5mA/channel, typical.

AC characteristics, including a 45MHz gain bandwidth product (GBW), a slew rate of 150V/µs, make the OPAx828 family an excellent choice for a variety of systems. These include high-speed and high-resolution data acquisition systems, transimpedance (I/V-conversion) amplifiers, filters, precision ±10V front ends, and high-impedance sensor-interface applications.

3 System Design Theory

This highly-linear, low-noise signal chain reference design achieves three primary goals:

- Support multiple input ranges
- Provide onboard system-level calibration
- Demonstrate low-noise and highly linear performance

3.1 Range Selection

This design features a voltage measurement signal chain with three measurement ranges: ±100mV, ±1V, and ±10V. As Figure 3-1 shows, OPA828 is the input amplifier and is in a non-inverting configuration for high-input impedance. A low-leakage multiplexer (TMUX6104) switches between three different gain settings.

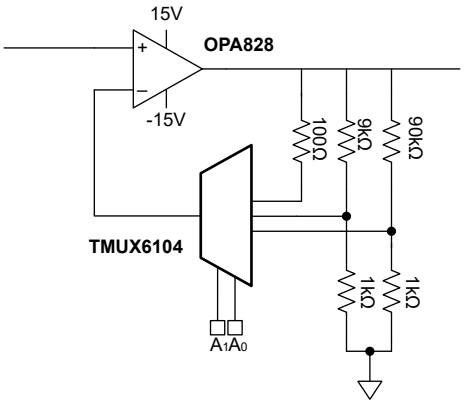

Figure 3-1. TIDA-010970 Programmable Gain Amplifier Block Diagram

OPA828 is a JFET amplifier, offering a higher input impedance compared to bipolar input amplifiers, while having a lower 1/f noise than CMOS input amplifiers. Low 1/f noise is more important in dc measurements than broadband noise. The higher input impedance of the JFET amplifier is a practical trade-off even though bipolar amplifiers have lower 1/f noise than JFET. The high-input impedance prevents the measurement signal chain from disrupting the measured signal. The DMM connects to the load in parallel for voltage measurements. The load can experience a voltage drop if too much current from the circuit under test flows through the meter, resulting in an inaccurate measurement.

The gain on the input amplifier is programmable so the signal chain can accommodate three input ranges, 1V/V, 10V/V, and 99.8V/V, to scale the input signal to a 10V range. Each gain setting has a different bandwidth such that the minimum bandwidth is 15kHz at the largest gain. The different bandwidths across gains are not a concern since this design is intended to measure dc signals. Install capacitors C17, C18, and C19 to adjust the bandwidth as needed.

Each range must scale the input signal to a 5.5V signal or less because the ADS127L21B has a maximum recommended supply of 5.5V. This design scales the input signal to 4V because the ADC reference is 4.096V. The ADS127L21B power supply is ±2.75V. This power supply range is shared with THP210 and provides margin for the THP210 input common-mode limit.

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3.2 Linearity and Low-Noise Signal Chain

This design features a highly linear, low-noise signal chain intended to measure dc voltages. Offset and gain errors are easily corrected with a simple two- or three-point calibration, but noise and linearity cannot be easily calibrated. Choosing low-noise and highly linear components is crucial. The 1/f noise, or flicker noise, is a much greater concern than broadband noise because this signal chain is intended to measure low-frequency signals.

The THP210 device, a fully differential amplifier shown in Figure 3-2, converts the single-ended input signals to differential signals for measurement with ADS127L21B.

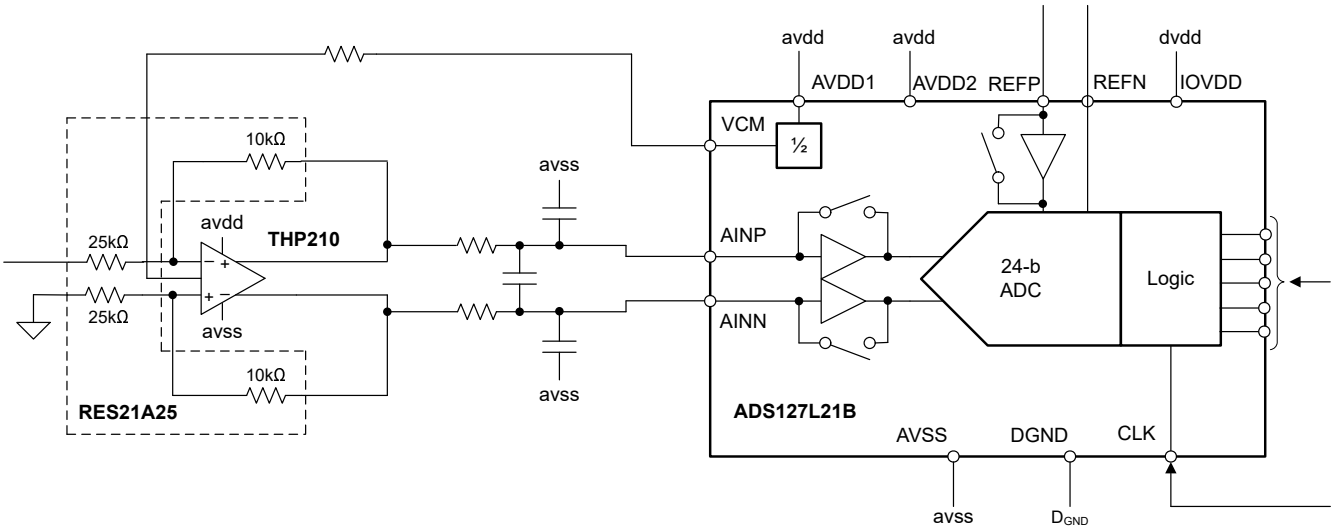

Figure 3-2. TIDA-010970 ADC Block Diagram

A single-ended input measurement allows the DMM to measure the load relative to a common ground. Converting the signal to a differential signal provides better signal integrity and noise immunity for the remaining signal chain. The THP210 uses external precision thin-film resistors, RES21A, with a 1:2.5 ratio to achieve a gain of 0.4V/V. This stage attenuates the OPA828 output from a 10V range to a 4V range. The ADC reference is 4.096V, so the maximum ADC input signal uses 98% of the ADC full-scale range. This maximizes the ADC resolution.

The RES21A resistor divider is 10kΩ-based. RES21A has low nonlinearity because the large resistances reduce self-heating. These larger resistances add broadband noise to this system; however, the linearity improvement from RES21A outweighs the additional noise since most DMM measurements are taken at slower speeds.

3.3 Calibration

This design uses REF81, a highly stable buried-Zener reference for calibrating the signal chain. A precision resistor divider network (RES11A) generates additional calibration source signals for the 1V and 100mV input ranges, as shown in Figure 3-3. An input multiplexer (MUX36) selects between the input signal, the calibration source signals for each input range, and ground.

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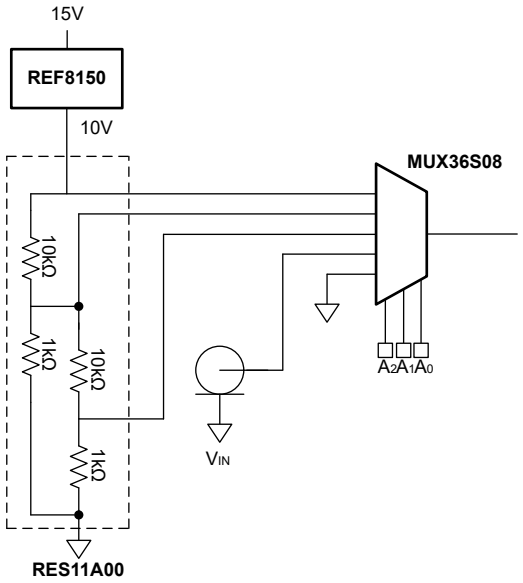

Figure 3-3. TIDA-010970 Calibration References Block Diagram

The 10V range calibration source originates directly from REF81, making this range the most accurate calibration range available. The calibration sources for the 1V and 100mV ranges are slightly less accurate since those sources are derived from the 10V signal. Any error from the precision resistor divider used to generate the 1V and 100mV sources is present. This reference design uses a near full-scale signal to maximize the calibrated error across the entire input range.

The calibration source calibrates the entire signal chain. Repeated calibration between measurements continuously removes initial gain and offset error from every measurement. This continuous calibration removes offset and gain error drift as well. Therefore, the only remaining errors in the system are the noise and linearity of the signal chain, as well as the drift of the calibration source. The calibration source must be stable over time and temperature to reduce errors from long-term and temperature drift because the overall signal chain accuracy depends on the calibration source. Nonlinearity and noise become the dominant sources of error with a stable calibration source. Reduce these error sources with careful component selection, as discussed in Section 3.2.

Use the following procedure to implement a continuous calibration routine. Software can implement this routine automatically, and one full cycle of the calibration routine is required to produce an accurate measurement. Figure 3-4 shows this process.

1. Set the input to ground to measure the offset of the system. Calculate the offset error.
2. Switch the multiplexer back to the input. Measure the input, subtracting the offset and multiplying by the gain. For the first measurement in the first iteration of this routine, there is no gain coefficient.
3. Switch the multiplexer to the calibration source. Measure the calibration source and calculate the gain error. There are calibration sources for each range, choose the appropriate source given the desired range.
4. Switch the multiplexer back to the input. Measure the input, subtracting the offset and multiplying by the gain to get the final calibrated result.
5. Repeat steps 1–4.

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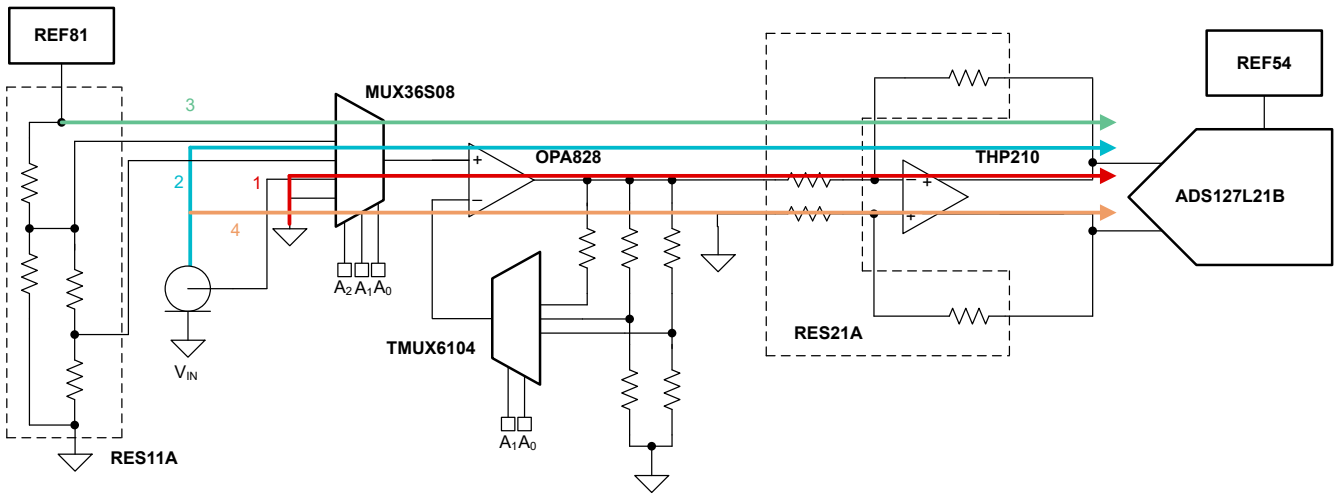

Figure 3-4. TIDA-010970 Calibration Procedure

Apply the gain and offset values to the ADS127L21B GAIN and OFFSET registers so ADS127L21B automatically applies gain and offset corrections to the conversion data. The value in the OFFSET registers is first subtracted from the conversion result. Next, the value in the GAIN registers is multiplied by the conversion result divided by 400000h. See the *Calibration* section of the *ADS127L21B 512kSPS, High-Precision, 24-Bit, Wideband Delta-Sigma ADC* datasheet for more details.

This calibration routine measures the input twice during one cycle. Measuring the input twice allows the DMM to measure the input at half the sampling rate, rather than one-third the sampling rate since the DMM measures the input at every other measurement. For example, a DMM executing the calibration routine at 60SPS has an effective measurement rate of 30SPS. Alternatively, operate the DMM at 120SPS to take a 60SPS measurement. Additionally, a continuous routine calibration requires a multiplexer with fast settling time to take accurate measurements.

3.4 Additional System Design Considerations

The TPS7A39 is a dual-output LDO which generates the positive and negative power rails for THP210 and ADS127L21B. The TPS7A39 outputs are set to ±2.75V to keep the THP210 input common-mode in range.

This design consumes 335mA at start-up and approximately 75mA during normal operation. In power-sensitive applications, several strategies can minimize the power consumption. REF81 provides 80% of the power consumption. The REF81 heater draws approximately 60mA during normal operation. This design uses the +15V rail to power the REF81 heater; however, increasing the heater power supply between the HEATP and HEATM pins reduces the REF81 current consumption. See the *REF81 Temperature Controlled Precision Voltage Reference with 0.05ppm/°C Temperature Drift and < 1ppm Stability* datasheet for more details. Additionally, the PCB includes mounting holes around the REF81 for an external enclosure. Adding an enclosure allows for better heater regulation and less overall output voltage drift.

Any small resistance on the ground plane causes an unpredictable voltage drop in the measurement path because the REF81 current draw is so high. To avoid errors from this current drop, all components in the signal measurement path are referenced to a star-ground plane (GND_SENSE). The components referenced to this star-ground plane have lower current. A resistance on the star-ground plane causes a lower voltage drop than an equivalent resistance on the REF81 ground plane, resulting in minimized errors. The star-ground and REF81 ground planes are connected at one point, R12. See *Schematic and PCB With the GND_SENSE Plane*.

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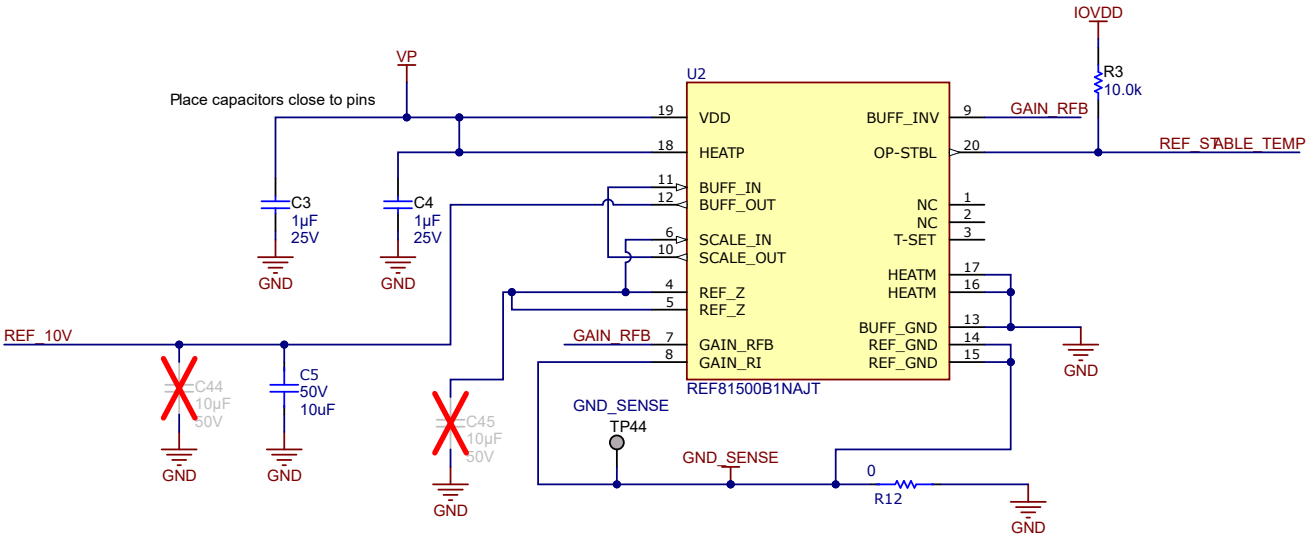

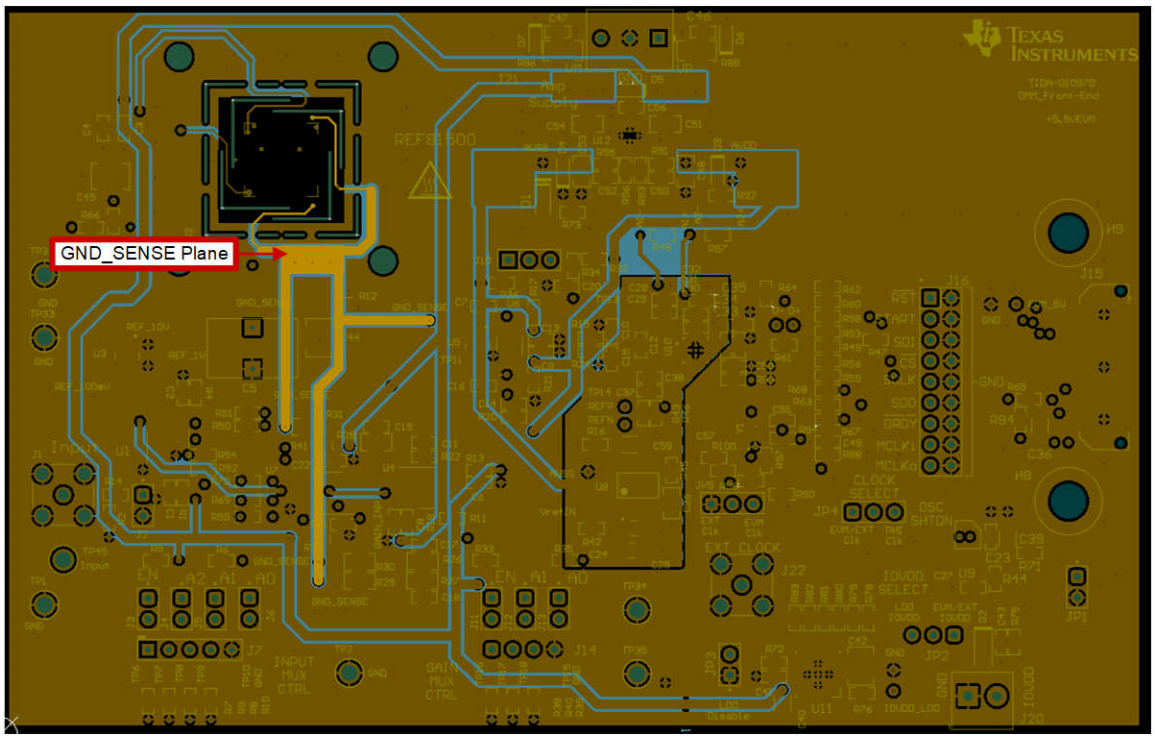

Figure 3-5. Schematic and PCB With the GND_SENSE Plane

REF54 is chosen as the ADC reference due to the low 1/f noise and low temperature drift. There is no need for additional reference circuitry to provide an accurate and stable ADC reference because REF54 has a buffered output. Using a REF81 as the ADC reference is possible; however, REF54 is smaller and consumes less current than REF81. Additionally, REF54 can be placed closer to the ADC without heating concerns.

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4 Hardware, Software, Testing Requirements, and Test Results

4.1 Hardware Description

Figure 4-1 shows the PCB design. REF81 and RES11 (U2 and U3) in the upper left provide the calibration reference voltages. TMUX6104 and OPA828 (U7 and U4) in the bottom right create the programmable gain amplifier. THP210 and ADS127L21B (U6 and U10) in the center of the board provide a linear, low-noise signal path. There are several layout choices intended to improve performance. A star-ground plane as discussed in Section 3.4 reduces errors from the large current consumption of REF81. Additionally, the traces in the differential signal path are as symmetrical as possible to reduce any errors from mismatch between the differential signals.

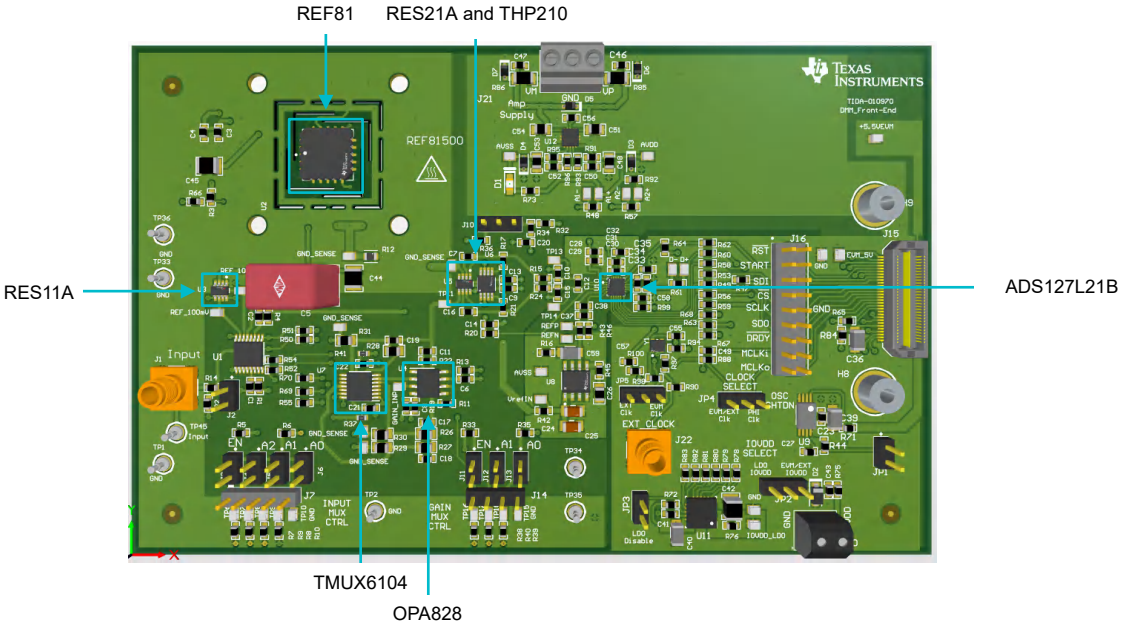

Figure 4-1. TIDA-010970 PCB

4.1.1 PCB Interface

Figure 4-2 shows the PCB connectors. Access the digital interface through J15, which connects to the PHI controller, or through J16, a pin header. J16 has a row of connections to ground, to enable easy connection for an oscilloscope or logic analyzer. The reference design requires an external power supply to operate, which is supplied at J21. Pin headers are used to select the input and set the gain of the programmable gain amplifier.

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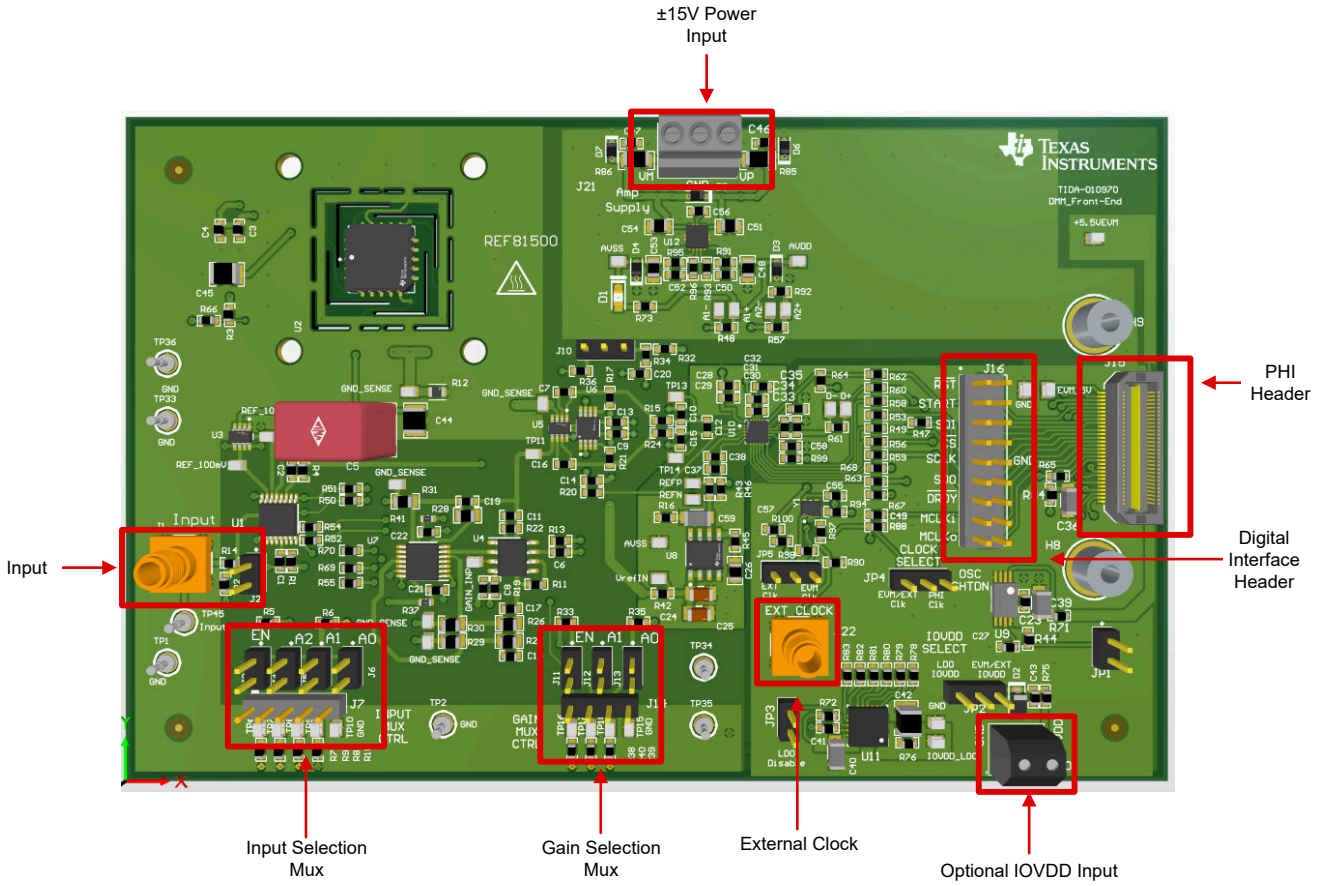

Figure 4-2. PCB Connectors

Table 4-1. TIDA-010970 External Connections

CONNECTOR	DESCRIPTION
J1	SMA connector for input signal
J2	Header connector for input signal
J3, J4, J5, J6, J7	Enable and input selection headers for the input multiplexer (U7). See Table 4-2 for more details
J10	Header for THP210 shutdown
J11, J12, J13, J14	Enable and input selection headers for the gain multiplexer. See Table 4-3 for more details
J15	QSH connector to connect to PHI, best practice is to power the PCB before connection
J16	SPI signals header, use for debugging and probing, or to connect to another board (if no QSH)
JP1	EEPROM enable
JP2	1–2: External IOVDD signal 2–3: IOVDD signal generated by TPS7A47
JP3	LDO enable
JP4	1–2: Selects onboard clock for ADC CLK pin 2–3: Selects PHI clock for ADC CLK pin
JP5	1–2: Selects external clock as onboard clock 2–3: Selects local oscillator (Y1) as onboard clock

This reference design is intended to operate with a Precision Host Interface (PHI) board, allowing for easy connection with the ADS127L21 Graphical User Interface (GUI). Additionally, the PCB includes a header to allow access to the digital signals from the ADC with an external controller. See also Figure 4-2 for all the PCB connections.

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4.1.2 Input Multiplexer

The reference design has three input ranges, ±100mV, ±1V, and ±10V that can calibrated. Select between the input signal and the calibration sources using the 8-channel input multiplexer (U1). Jumpers J3, J4, J5, and J6 enable the input multiplexer and select the desired input channel. See Table 4-2 for details.

Table 4-2. Jumper Settings for Input Multiplexer

J3 (EN)	J4 (A2)	J5 (A1)	J6 (A0)	INPUT CHANNEL
0	X(1)	X(1)	X(1)	None, U1 disabled
1	0	0	0	Input signal
1	0	0	1	10V range calibration signal
1	0	1	0	1V range calibration signal
1	0	1	1	100mV range calibration signal
1	1	X(1)	X(1)	Ground

(1) 'X' denotes a 'Don't Care'.

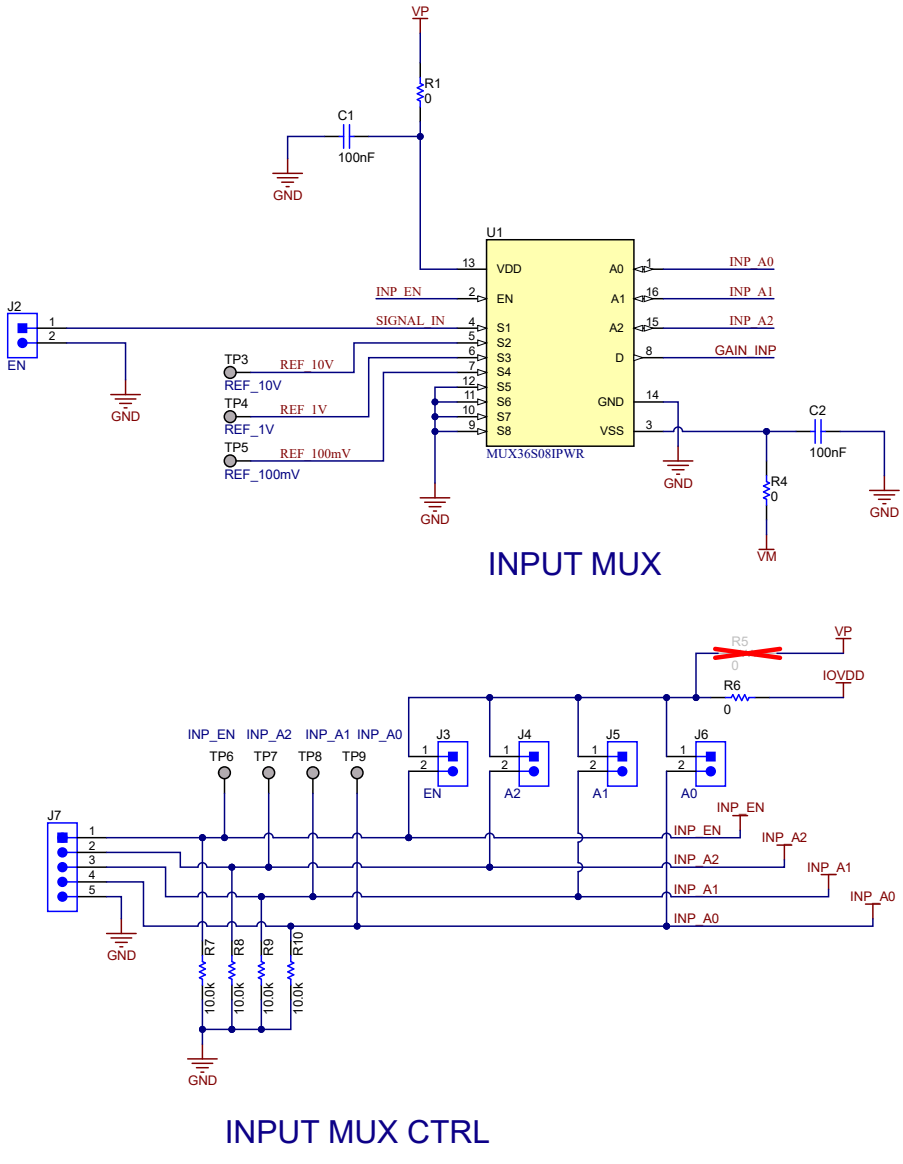

Figure 4-3. Input Multiplexer Schematic

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4.1.3 Gain Multiplexer

Select the desired input range using the 4-channel gain multiplexer (U7). The gain multiplexer changes the input amplifier (U4) gain. The input signal needs to be scaled to the ADS127L21B full-scale range to maximize measurement resolution. The input amplifier scales the input signal to a 10V scale. Jumpers J11, J12, and J13 enable the gain multiplexer and select the desired input channel. See Table 4-3 for more details.

Table 4-3. Jumper Settings for Gain Multiplexer

J11 (En)	J12 (A1)	J13 (A0)	INPUT CHANNEL	VOLTAGE RANGE
0	X(1)	X(1)	U7 Disabled	–
1	0	X(1)	Gain = 1.00V/V	±10V
1	1	0	Gain = 10.0V/V	±1V
1	1	1	Gain = 99.8V/V	±100mV

(1) 'X' denotes a 'Don't Care'.

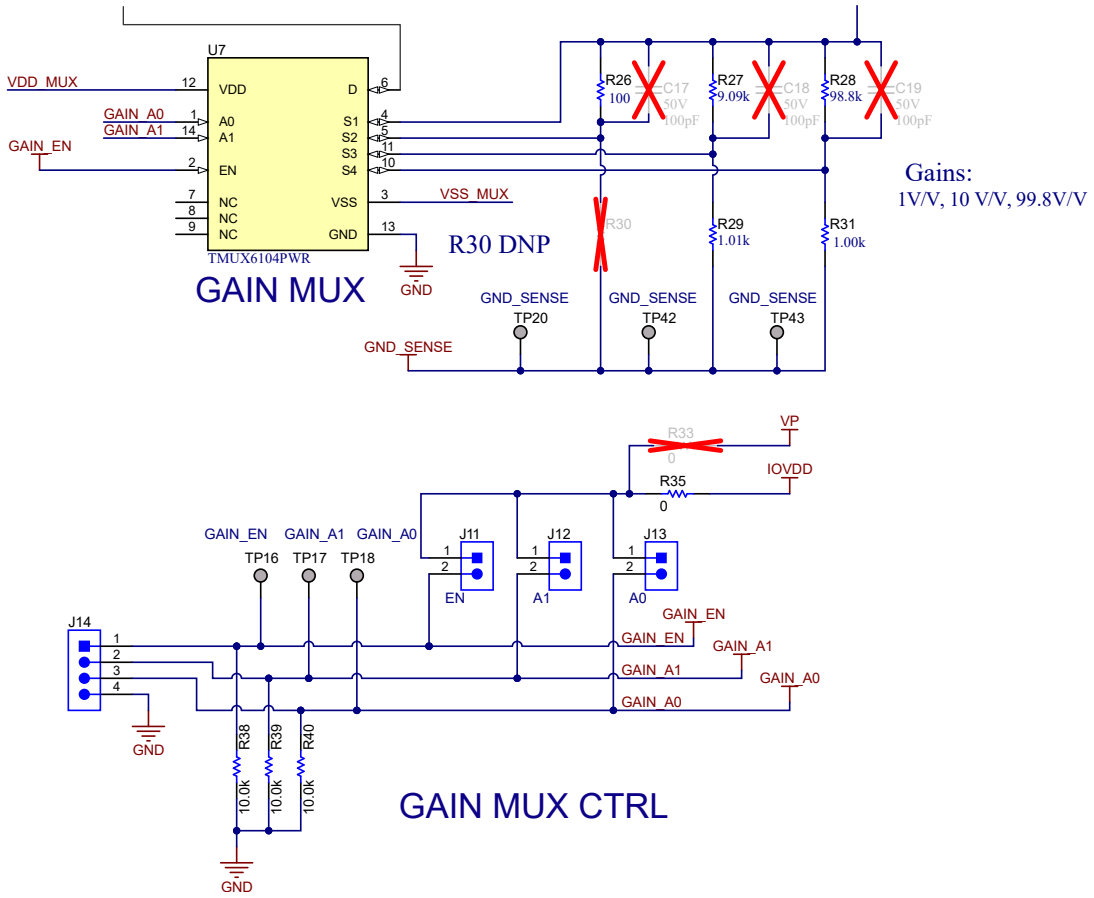

Figure 4-4. Gain Multiplexer Schematic

4.1.4 Power Supplies

External ±15V power supplies power the PCB. Figure 4-5 shows the power tree. The ±15V power supplies directly power REF81, OPA828, TPS7A39, TPS7A47, MUX36S08, and TMUX6104. The reference design is fitted with 36V diodes D5, D6, and D7. These diodes allow for ±16.5V bipolar power supplies, which is the maximum recommended operating voltage for TMUX6104.

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TPS7A39 generates ±2.75V (AVDD and AVSS) power rails to supply THP210, ADS127L21B, and REF54. TPS7A47 generates a 2.5V power rail that supplies IOVDD to ADS127L21B. Install JP2 in the 1–2 position and use J20 to supply an external IOVDD rail.

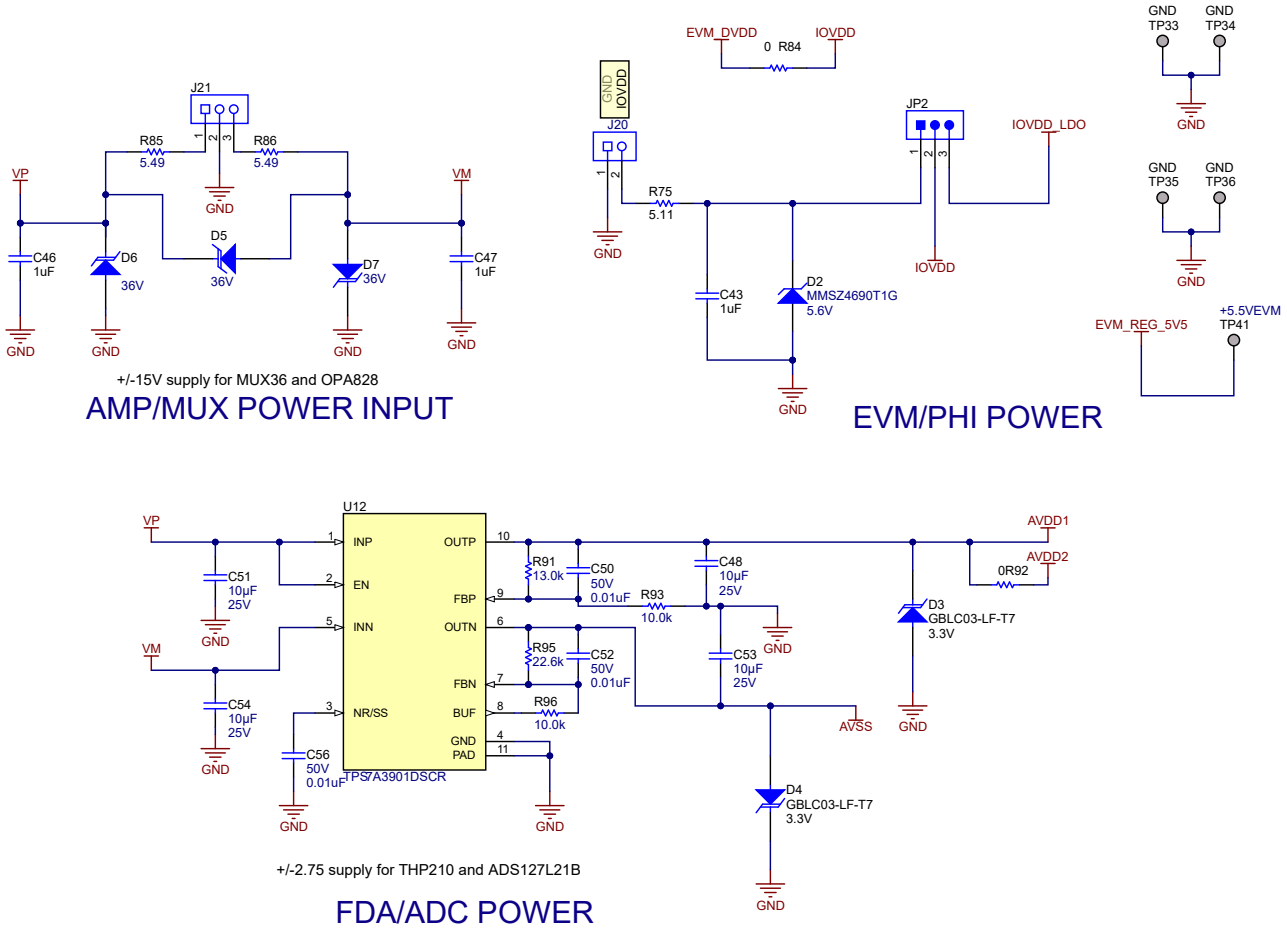

Figure 4-5. Power Tree Schematic

4.1.5 Clock Tree

This reference design supports three different clock options:

1. PHI clock (no external connections)
2. Local clock (no external connections)
3. External clock

The default position for jumper JP4 is 2–3, which routes the PHI digital controller board clock to the CLK pin on the ADS127L21 (U10). Move the jumper to position 1–2 to directly route the local clock to ADS127L21 if the PCB is used without the PHI controller. Position 2–3 on jumper JP5 enables the local 32.768MHz oscillator (Y1) on the PCB, which is the default position required to work with the ADS127L21EVM-PDK-GUI software (see the *ADS127L21EVM-PDK* tool page). Supply an external clock with jumper J5 in position 1–2. Use a CMOS square-wave signal with an amplitude equal to IOVDD (2.5V when using the PHI board) and a frequency within the specified ADS127L21B range.

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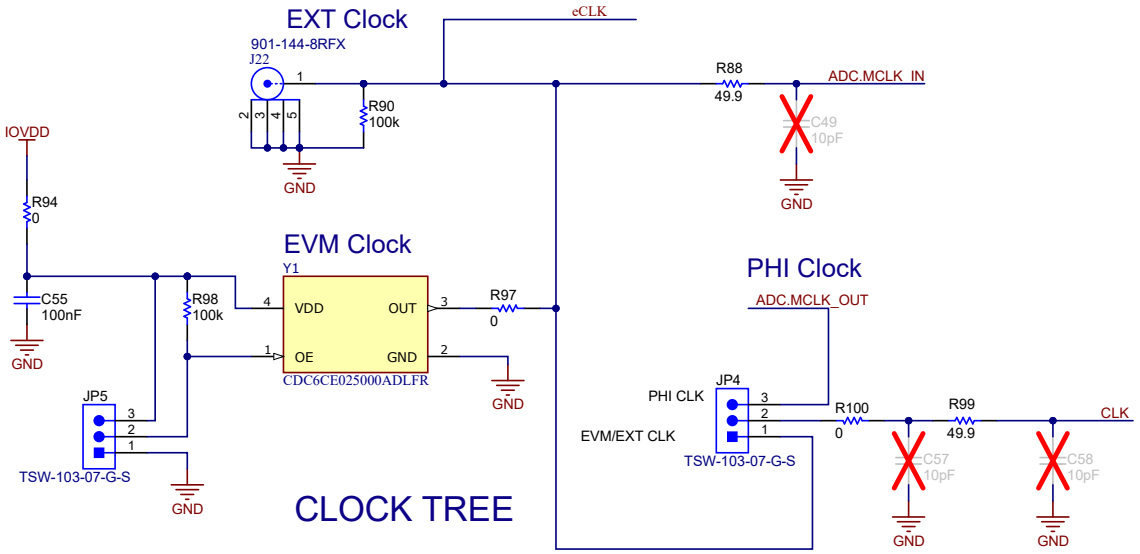

Figure 4-6. Clock Tree Schematic

4.2 Software Requirements

This reference design is intended to be used with the dedicated ADS127L21EVM-PDK-GUI software shown in Figure 4-7. The ADS127L21GUI supports both the ADS127L21 and ADS127L21B. See also the *ADS127L21EVM-PDK Evaluation Module* user's guide for more information.

Use the GUI to configure ADS127L21B and select the ADC sample rate. Adjust the clock frequencies to change the data rate.

The GUI also collects time domain data and automatically calculates the RMS noise. Data collected by the GUI can be downloaded for additional post-processing.

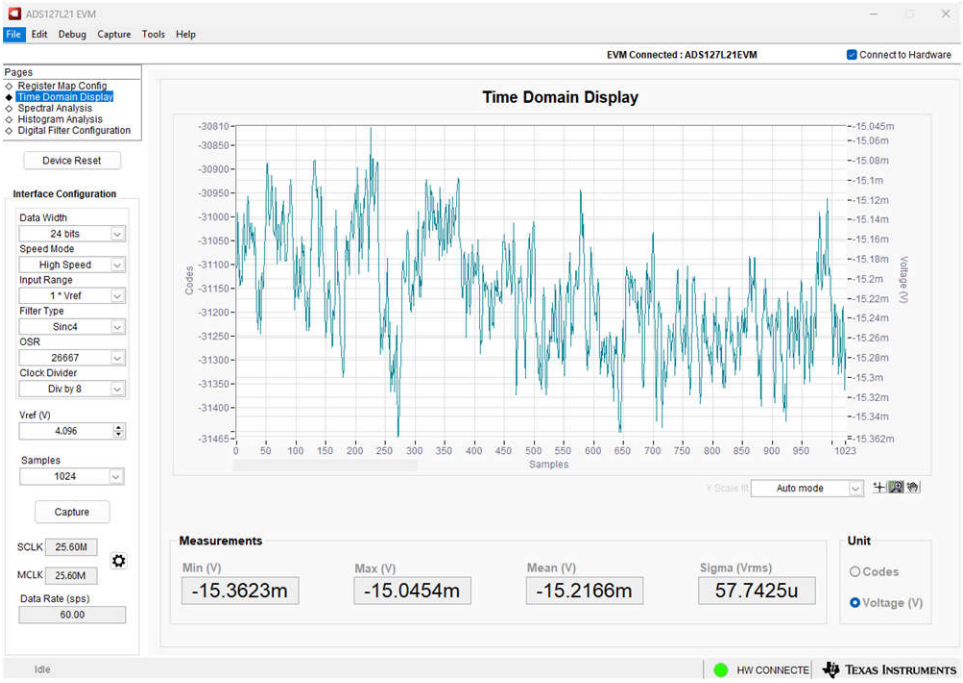

Figure 4-7. ADS127L21 EVM GUI

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4.3 Test Setup

The PCB is evaluated through the PHI board connected to a computer running the ADS127L21EVM-PDK-GUI software.

The following components are required for noise and linearity tests:

- Reference design PCB
- PHI controller card
- PC running ADS127L21B software
- ±15V power supplies
- Low-noise dc source
- 8.5-digit DMM

Follow the steps shown in Figure 4-8 to measure dc voltages.

1. Connect the PHI controller to the PCB
2. Connect ±15V power supplies to the PCB using J21
3. Connect an 8.5-digit DMM between the input at J2 and GND_SENSE (TP19)
4. Use J4, J5, and J6 to select the input signal
5. Use J12 and J13 to select the gain of the programmable gain amplifier
6. Connect a precision DC source to the SMA input connector, J1

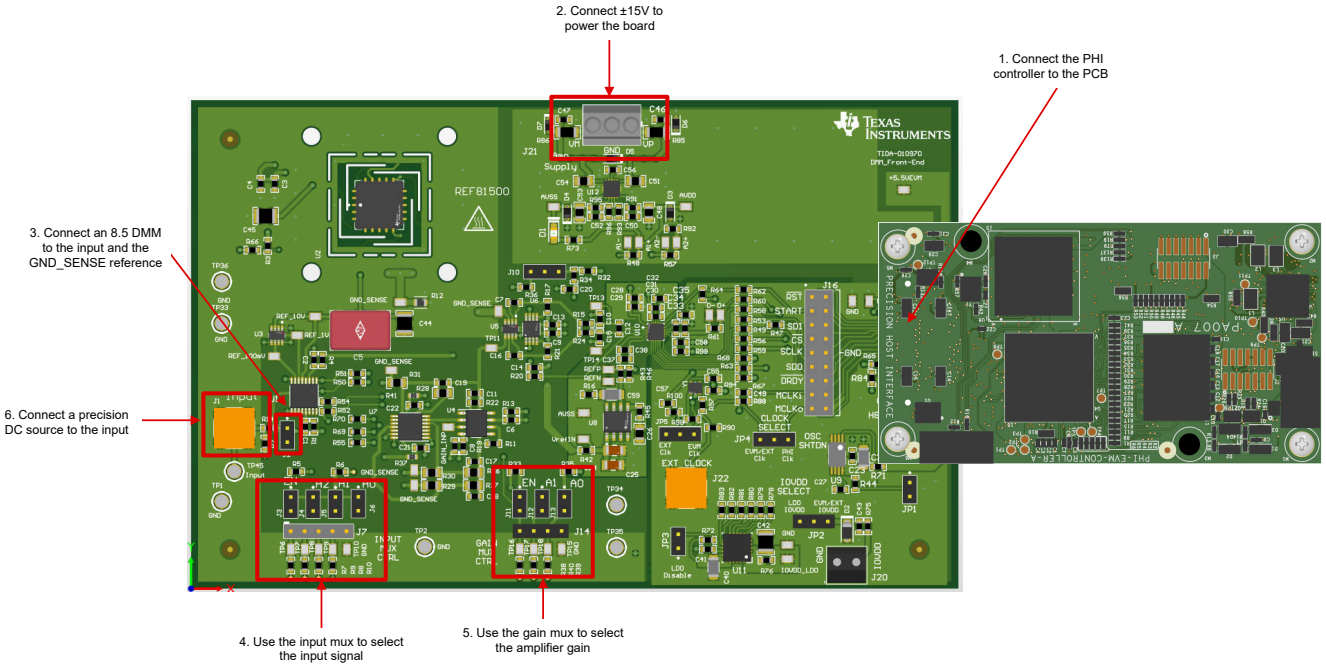

Figure 4-8. Test Setup for Measuring dc Voltages With TIDA-010970

Use the SMA connector to connect the precision dc source to the signal chain input with the shortest connections possible. SMA connectors reduce the noise coupled into the signal chain compared to pin headers, allowing for higher-accuracy measurements. Use an 8.5-digit DMM because the reference design is intended to measure with 7.5-digit accuracy. Using a meter with higher resolution than the target resolution of the signal chain is important. Assessing whether the signal chain has met the target resolution is not possible if the meter has the same resolution because the meter has error.

Calibrating and taking measurements with respect to a GND_SENSE test point (TP19, TP20, TP42, TP43, or TP44) is important. REF81 is referenced to the GND plane. Small resistances on the GND plane can cause measurable voltage drops because REF81 draws significant current, which impacts measurement accuracy.

All the measured test results are taken with respect to a GND_SENSE test point.

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4.4 Test Results

The following ADC settings are used for the noise and linearity tests:

Table 4-4. GUI Settings

SETTING	SELECTION	GUI LOCATION
REF_RNG	High-reference range	Register Map Config - CONFIG1
CLK_SEL	Internal clock operation	Register Map Config - CONFIG3
VREF	4.096V	Interface Configuration
Speed Mode	High speed	Interface Configuration
Filter Type	Sinc4+Sinc1	Interface Configuration
OSR	26667	Interface Configuration
CLK Divider	Divide by 8	Interface Configuration
CLK Source	External	Clock Settings
CLK Frequency	25.6MHz	Clock Settings
SCLK Source	Internal (PHI)	Clock Settings
SCLK Frequency	25.6MHz	Clock Settings
Samples	1024	Interface Configuration

Locate the clock settings by pressing the gear icon next to the SCLK and MCLK frequencies, as shown in Figure 4-7. Any settings not shown in Table 4-4 are left at the GUI default settings. The calculated *data rate* is set to 60SPS with these changes. Use an external clock source to test other data rates, such as 10PLC (power line cycles) or 0.1PLC. Use connector J22 and move JP5 to the 1–2 position to connect an external clock source. See Section 4.1.5 for more details.

4.4.1 Integral Nonlinearity Measurements

INL testing requires a very low-noise source to avoid introducing errors into the measurement. An 8.5-digit DMM is required to accurately measure the INL because this is a highly linear signal chain. The DMM measures the signal chain input, and the GUI measures the ADC output. The output and scaled input are compared. Measurements are taken along the full input range.

The INL can be less than the noise floor because the measurement signal chain is designed to have low nonlinearity. Averaging N samples reduces the thermal noise by a factor of $\sqrt{N}$. With sufficient averaging, the INL can be detected and measured. Each measured point is an average of 1024 measurements.

Figure 4-9 shows that the measured INL for the reference design is approximately 1.1ppm for the 10V range. TIDA-010970 is not a full DMM design, so a full DMM design includes other components in the signal chain that add nonlinearities, such as input protection. However, TIDA-010970 includes the most critical components of the signal measurement path.

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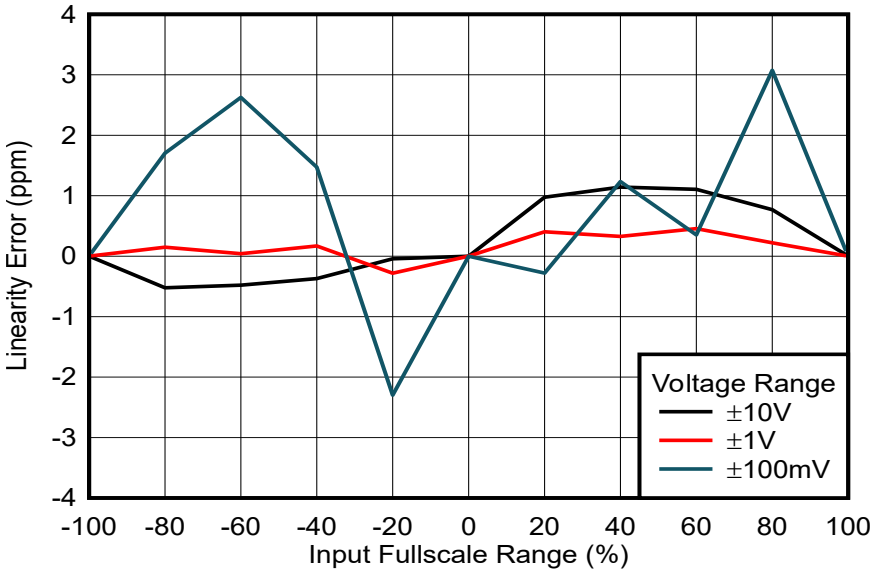

Figure 4-9. TIDA-010970 Linearity Error vs Input Full-Scale Range

Calculate INL using a three-endpoint calibration. This method requires three measurements: zero, positive full-scale, and negative full-scale. Calculate two sets of coefficients from these three measurements: one set provides a linear correction for the negative range; the second provides a linear correction for the positive range. These linear corrections create a piece-wise linear fit. Then, the INL is calculated by comparing the actual measured output with the expected calibrated piece-wise linear output. In theory, more than three points can be measured to create a piece-wise function with more than two sets of coefficients. However, this system has been designed for low linearity such that two sets of coefficients are sufficient.

4.4.2 Noise Simulation

Figure 4-10 shows the TINA-TI schematic used to simulate the complete signal chain noise. Figure 4-11 shows the simulation results. DMM noise is often specified in numbers of power line cycles (PLC), which represents one cycle of the power line frequency. A higher PLC indicates a longer measurement integration time. For example, 5 PLC indicates the DMM measured for 5 power line cycles. A higher PLC results in a more accurate measurement at the cost of increased measurement time. At 60Hz, or 1 PLC, the simulated noise is less than $1\mu V_{RMS}$.

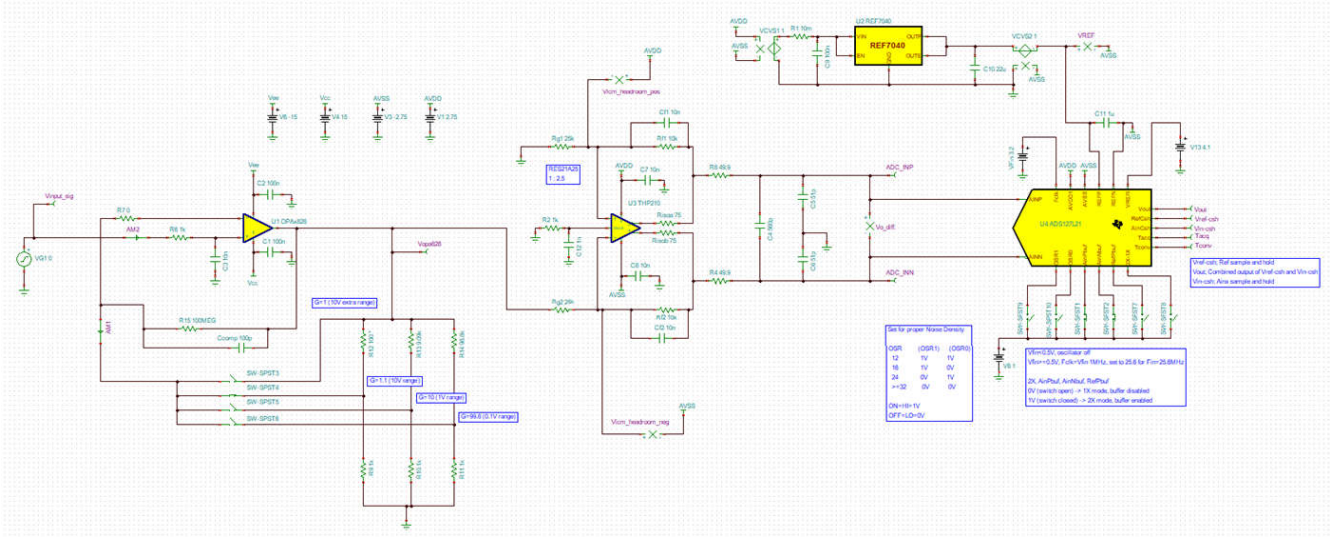

Figure 4-10. TIDA-010970 TINA-TI Simulation Schematic

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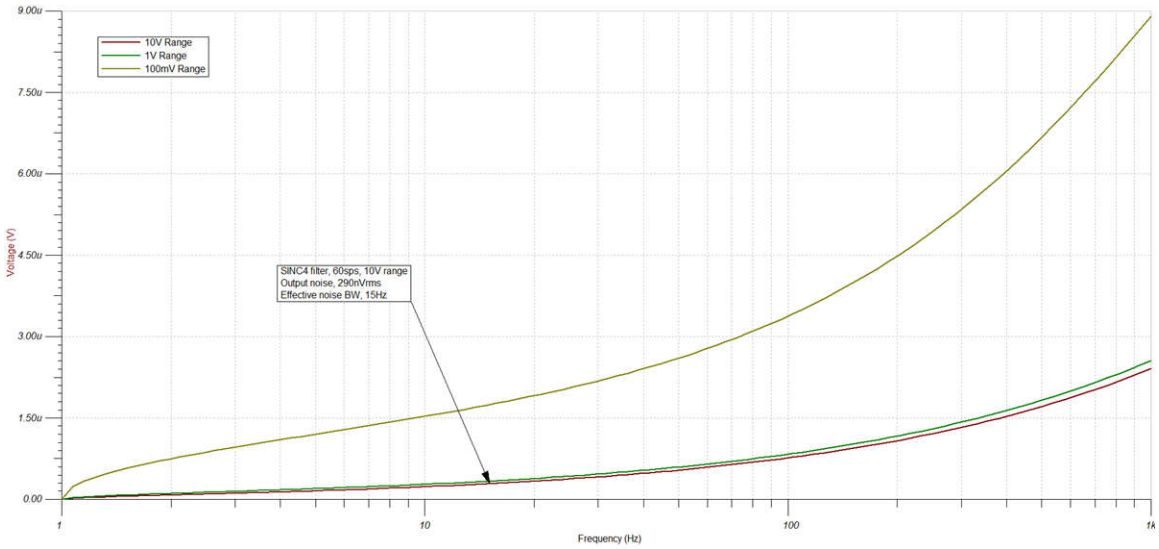

Figure 4-11. Total Noise for TIDA-010970 for All Input Ranges

4.4.3 Noise Measurements

The noise can also be calculated from the sampled data. The RMS noise for 1 PLC can be calculated by taking the standard deviation of all the samples since the data is collected at 60SPS. Figure 4-12 shows the measured results for the ±10V range.

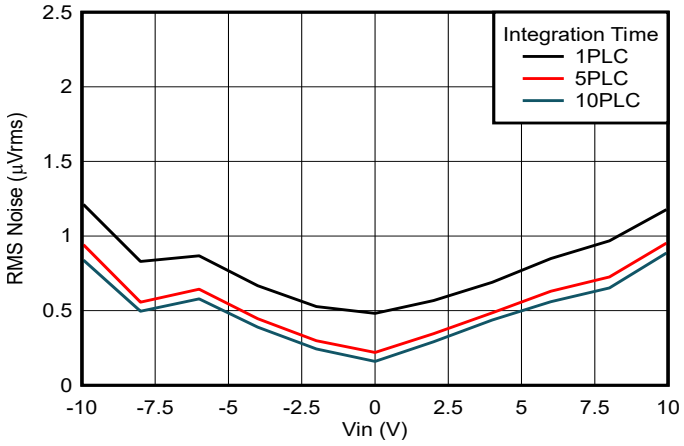

Figure 4-12. RMS Noise at 1, 5, and 10 PLC for the ±10V Range

Take a moving average to get noise measurements for higher data rates, such as 5 PLC or 10 PLC (with 5 points and 10 points, respectively). The moving average effectively applies a Sinc1 filter to the data. See also Figure 4-12 for the ±1V and ±100mV results.

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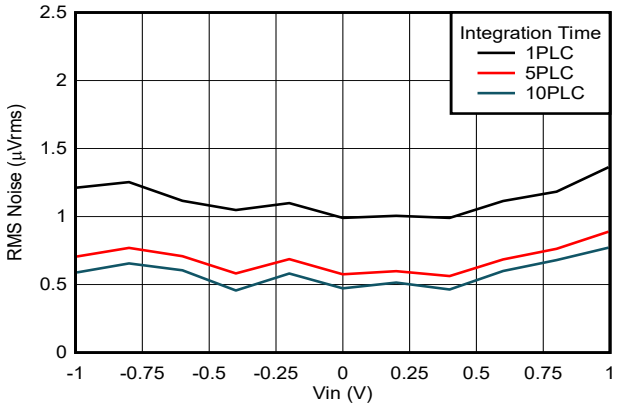

Figure 4-13. RMS Noise at 1, 5, and 10 PLC for the ±1V Range

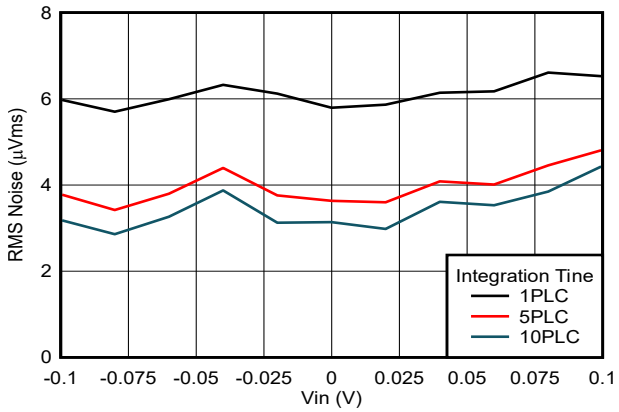

Figure 4-14. RMS Noise at 1, 5, and 10 PLC for the ±100mV Range

Table 4-5. TIDA-010970 Measured Noise vs Simulation

NOISE AT 1 PLC	±10V RANGE	±1V RANGE	±100mV RANGE
Measured Noise (Shorted Input)	335nV$_{RMS}$	547nV$_{RMS}$	3.23µV$_{RMS}$
TINA-TI Simulation	290nV$_{RMS}$	337nV$_{RMS}$	1.74µV$_{RMS}$

4.4.4 Conclusion

This reference design had three design goals:

1. Support multiple input ranges
2. Provide onboard system-level calibration
3. Demonstrate low-noise and highly linear performance

The design features a programmable gain amplifier, which allows the user to select between ±10V, ±1V, and ±100mV ranges. The reference design also features an on-board calibration source, REF81, which provides a stable reference voltage to calibrate the entire signal chain. The design is also low noise and low INL, measuring 335nV$_{RMS}$ noise and 1.1ppm INL for the ±10V range. These low noise and INL measurements, along with the stable calibration source and multiple input ranges, make this reference design an excellent design choice for a DMM voltage measurement path.

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5 Design and Documentation Support

5.1 Design Files

5.1.1 Schematics

To download the schematics, see the design files at TIDA-010970.

5.1.2 BOM

To download the bill of materials (BOM), see the design files at TIDA-010970.

5.2 Tools

ADS127L21 EVM Software User Interface	This reference design is intended to be used with the dedicated GUI for the ADS127L21 EVM.

5.3 Documentation Support

1. Texas Instruments, *REF81 Temperature Controlled Precision Voltage Reference with 0.05ppm/°C Temperature Drift and < 1ppm Stability Datasheet*
2. Texas Instruments, *ADS127L21B 512kSPS, High-Precision, 24-Bit, Wideband Delta-Sigma ADC Datasheet*
3. Texas Instruments, *RES11A Matched, Thin-Film Resistor Dividers With 1kΩ Inputs Datasheet*
4. Texas Instruments, *RES21A Matched, Thin-Film Resistor Dividers With 10kΩ Inputs Datasheet*
5. Texas Instruments, *ADS127L21EVM-PDK Evaluation Module User's Guide*

5.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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6 About the Author

MAGGIE LEE is a systems engineer at Texas Instruments, where she is responsible for developing reference designs for *Test and Measurement* applications. Maggie earned a bachelor's degree (B.S.) in electrical engineering from the California Institute of Technology. The author thanks KEITH NICHOLAS, LUIS CHIOYE, CARRIE STOLL, and CARL SCHARRER for supporting this reference design.

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (November 2025) to Revision A (February 2026)	Page
• Updated title of the document to better cover reference design capabilities	1

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