TI High-Speed Designs

Verified Design Pipeline ADC Code Error Rate Analysis and Measurement

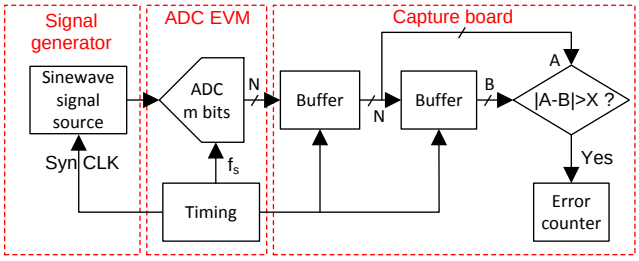
TI High-Speed Designs

TI High-Speed Designs are analog solutions created by TI's analog experts. Verified designs offer the theory, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of useful circuits. The Design also discusses circuit modifications which help to meet alternative design goals.

Design Resources

ADS54J54	Product Folder
ADS54J54EVM	Product Folder
TSW14J56EVM	Product Folder

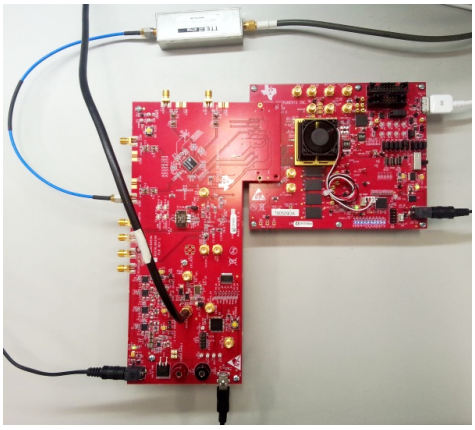
TI E2E™ Community — Ask The Analog Experts WEBENCH® Design Center



Circuit Description

Code errors from an analog-to-digital converter (ADC) could pose a critical issue for applications concerned with the time-domain performance. For example, when using an oscilloscope the user would like to see an actual signal waveform instead of the spikes caused by the ADC code errors.

This TI Design explains the architecture and operation of pipeline ADC, followed by an analysis of why code errors occur, and how digital correction works. The Design includes a block diagram of the code error rate (CER) test, and explains the measurement procedures. The Design shows and analyzes a CER test example of a high-speed ADC ADS54J54.



1 Introduction

Different from other ADC metrics such as a signal-to-noise ratio (SNR) or an effective number of bits (ENOB), bit error rate (BER) is an important specification used to evaluate how stable the output codes of an ADC can be over an extended time interval. Large bit errors occur less frequently, and Figure 1 shows the waveform of the ADC output with error codes.

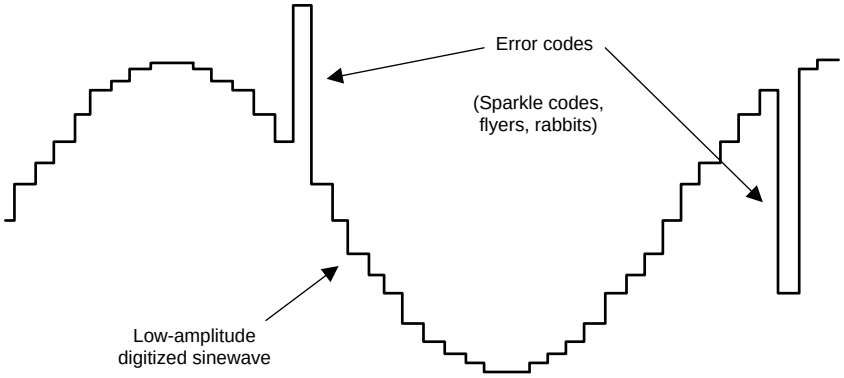


Figure 1. Output of ADC With Error Codes

BER is a major concern in digital communication systems, and possibly instrumentation applications such as digital oscilloscopes, especially when operating in *single shot* mode, or trying to capture infrequent transient pulses. An error code can be misinterpreted as a transient pulse, therefore giving a false result. In sensitive application environments, like the military or aerospace, CER of an ADC is an important specification to consider.

2 How ADC Output Code Error Occurs

The pipelined ADC has become the most popular ADC architecture for sampling rates, from a few mega samples per second (MSPS) up to over 100 MSPS. Resolutions range from 8 bits at the faster sample rates up to 16 bits at the lower sample rates. These resolutions and sampling rates cover a wide range of applications including CCD imaging, ultrasonic-medical imaging, digital receivers, base stations, digital video (HDTV for example), xDSL, cable modems, and fast Ethernet.

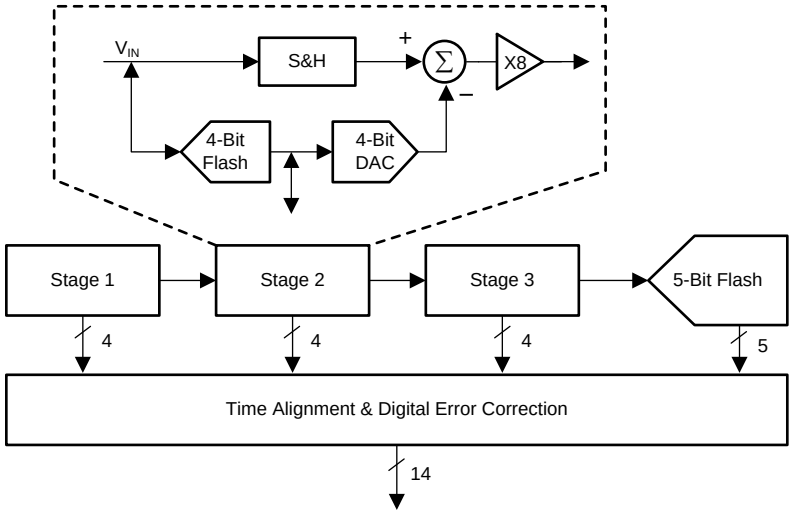


Figure 2. ADS54J54 Pipelined ADC Architecture

The ADS54J54 is a 14-bit, 500-MSPS quad-channel pipeline ADC. Figure 2 shows the basic diagram of the ADS54J54. The ADC has four stages. The first three stages resolve 4-bits per stage, and the last stage is a 5-bit flash. During each stage, the input signal is first converted by a simple 4-bit flash ADC. The digital value is converted back to analog format by a 4-bit DAC, and subtracted from the input, which gives a residue. Next, the residue is multiplied to get the full range, and then converted by the subsequent stage. In a pipelined ADC, built-in redundancy is normally used between every two stages for the digital correction. The details are further discussed in the following section.

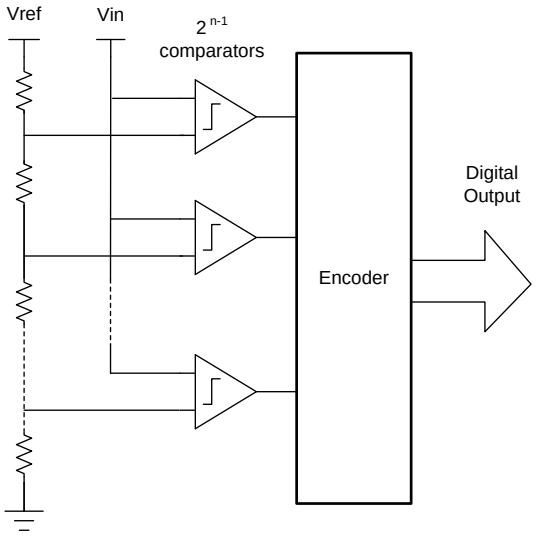


Figure 3. N-Bit Flash ADC Architecture

Figure 3 shows the architecture of an N-bit flash ADC.

- Each comparator has its own threshold voltage, spaced by 1 LSB.
- The input is fed to all the comparators in parallel.
- The output of the comparators is in “thermometer” format.
- An encoder is used to convert the output into binary format.

Inside a high-speed flash ADC, the comparators are typically required to provide fast amplification in a short time period. As shown in Figure 4, the clock CK is applied at t = 0, and the outputs VX and VY regeneratively depart from the initial difference of VXY0. For an excessively small VXY0, the outputs fail to reach valid logical levels within the allotted time TCMOP, possibly causing metastability errors in the subsequent stages. Therefore, a code error occurs. For example, in Figure 2, a comparison error which occurs in stage 2 causes an error of $2^{3+5} = 2^8$ LSBs.

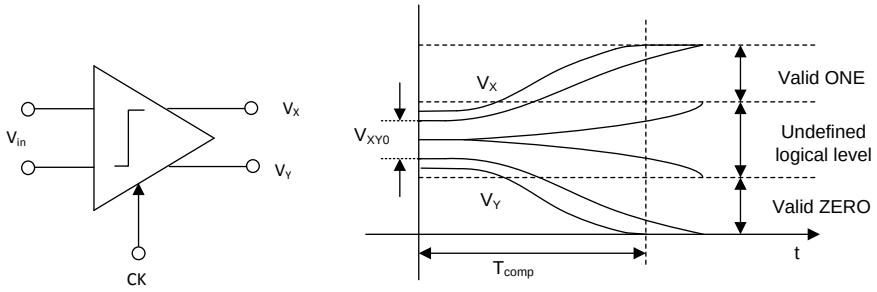


Figure 4. Outputs of a Typical Clocked Comparator

3 Built-In Redundancy for Digital Error Correction

Most modern pipelined ADCs employ a technique called *digital error correction* to greatly reduce the accuracy requirement of the flash ADCs (and thus the individual comparators). In Figure 2, notice that the 4-bit residue at the summation-node output has a dynamic range 1/16 that of the original stage 1 input (VIN), yet the subsequent gain is only eight. Therefore, the input in stage 2 occupies only half the range of the 3-bit ADC in stage 2 (when there is no error in the first 3-bit conversion in stage 1).

If one of the comparators in the first 4-bit flash ADC has a significant offset, when an analog input close to the trip point of this comparator is applied, an incorrect 4-bit code and 4-bit DAC output would result, producing a different residue. As long as this gained-up residue does not over range the subsequent 4-bit ADC, there's some proof that the LSB code generated by the remaining pipeline (when added to the incorrect 4-bit MSB code) will give the correct ADC output code. The digital error correction will not correct for errors made in the final 5-bit flash conversion. Any errors made at that conversion are suppressed by the large (83) cumulative gain preceding the 4-bit flash.

Although each stage generates 4 raw bits in the Figure 2 example, because the interstage gain is only eight, each stage (stages 1-3) effectively resolves only 3 bits. The extra bit is simply to reduce the size of the residue by one half, allowing extra range in the next 4-bit ADC for digital error correction, as mentioned above. The extra bit process is called *1-bit overlap* between adjacent stages. The effective number of bits of the entire ADC is therefore 3 + 3 + 3 + 5 = 14 bits.

In some cases, a high-speed CMOS pipelined ADC tends to favor a lower number of bits per stage (as low as just 1-bit per stage, so that the interstage gain is only two), because it is difficult to realize wideband amplifiers of very high gain in CMOS. That is using the popular 1.5-bit-per-stage architecture, where each stage resolves 1-bit with 0.5-bit overlap. Each 1.5-bit stage has a 1.5-bit flash ADC (only two comparators), versus a full 2-bit flash ADC. Figure 5 shows the transfer characteristics of VRESIDUE versus VIN of 1.5-bit pipelined stage.

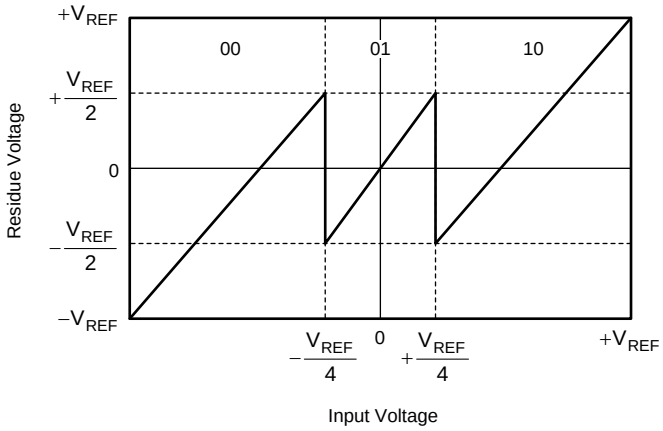


Figure 5. VRESIDUE Versus VIN Transfer Characteristics

Generally, the redundancy mechanism between every two stages can significantly correct one comparator error in each stage. However, when more than two comparator errors occur, the residue fed to the subsequent stage still overflows and a code error occurs. Though the probability of two comparator errors is much smaller than the probability of one comparator error, the redundancy mechanism is still very useful. As the sampling frequency of the converter increases, the convention time for the comparator decreases, and the CER rises. Section 4 explains how to test the CER of a converter and shows a test example.

4 ADC CER Measurement

The test system in Figure 6 shows the procedures used to test the BER of an ADC. The analog input for the ADC is provided by a high-stability low-noise sinewave generator. The analog input level is set slightly smaller than the full scale. When testing the CER, an attempt to cover almost all the dynamic range of the ADC means going through almost all the words coming out of the ADC. Therefore, coherent sampling is required, and the input signal should be set to –1 dBFS of the full scale of the converter.

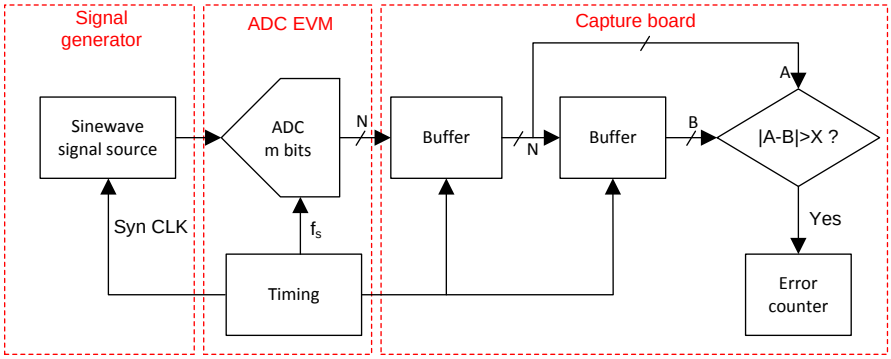


Figure 6. Block Diagram for ADC CER Test

The test set uses two series buffer registers to acquire successive codes A and B. A logic calculation determines the absolute difference between A and B. The difference is then compared to the error limit, chosen to allow for the expected random Gaussian noise spikes, due to the normal ADC noise. Errors which cause the difference to be larger than the error limit will increment the counters. The number of errors, E, are counted over a period of time, T. The error rate is then calculated as BER = E/2Tfs. The factor of 2 in the denominator is required because the hardware records a second error when the output returns to the correct code after making the initial error. The error counter is therefore incremented twice for each error.

4.1 Coherent Sampling

- Fs = sampling rate of the ADC
- Fin = input signal frequency
- N = number of bits of the ADC resolution
- M = number of samples in one buffer (power of 2)

To ensure that the samples in the previous buffer, and the corresponding samples in the following buffer, are sampled at exactly the same time point of a sinewave, a coherent sampling is necessary. The signal generator must be synchronized with the ADC sampling clock. In the test, a 10-MHz CLK reference signal output from the ADC evaluation board is used to synchronize the sinewave generator with the ADC. The oscillator of the signal generator is configured to an external reference. An example of how to calculate the coherent input frequency in a CER test follows.

4.1.1 Example

A designer wishes to evaluate the performance of a 14-bit ADC at:

- Fs = 500 MSPS
- Fin = 15.5 MHz
- N = 14

4.1.2 Problem Solving

1. Set buffer size to M = 2^{15}. M should be at least 2^{14} to cover all the codes of a 14-bit ADC. M is also limited by the RAM size of the capture board.
2. Calculate the number of cycles. N_{cycle} = M / (Fs/Fin) = 2^{15} × 15.5 / 500 = 1015.808. The nearest prime number is 1013, so set N_{cycle} = 1013. A prime number is chosen to ensure all the samples in the buffer are unique to each other.
3. Recalculate the coherent frequency. Fin = N_{cycle} × Fs/M = 15.45715332 MHz.

Designers can also use the automatic calculation tool in HSDC Pro software to calculate the coherent frequency, shown in Figure 7.

4.2 Threshold and Running Time Determination

Thermal noise and other disruptions from clock jitter, aperture jitter, or the driving circuit, are all added to the conversion results coming out of an ADC. The threshold should be set larger than the peak value of the noise to get correct results.

Table 1. SNR Performance Of The Tested ADC

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SNR	Signal-to-noise ratio	f_{in} = 10 MHz	—	68.3	—	dBFS
		f_{in} = 100 MHz	—	68.2	—	
		f_{in} = 170 MHz	—	67.2	—	
		f_{in} = 310 MHz	—	67.6	—	
		f_{in} = 450 MHz	—	66.8	—	

For example, Table 1 shows the SNR performance of the ADS54J54 at the sample rate of 500 MSPS. The noise floor of the ADC conversion can be calculated as shown in Equation 1.

$$V_{noise} = \frac{\frac{2^{14}}{2\sqrt{2}}}{10^{\frac{SNR}{20}}} = \frac{\frac{16384}{2\sqrt{2}}}{10^{\frac{68.3}{20}}} = 2.228\ LSB_{RMS} \quad (1)$$

Figure 7 shows the plot of noise in time domain. The VPP of the noise is approximately 25 LSB, therefore the minimum threshold can be set at 32 LSB.

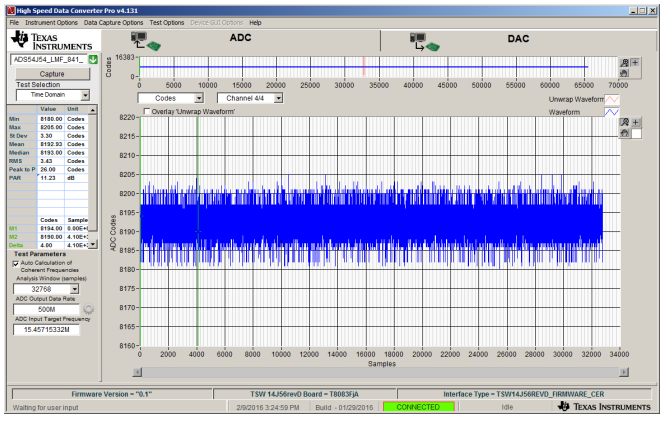


Figure 7. Noise Plot in Time Domain in HSDC Pro

Figure 8 shows a CER test window. There are five thresholds and corresponding counters. The cycle count records how many cycles have been tested, therefore the total number of samples, and the running time can be calculated from the cycle count.

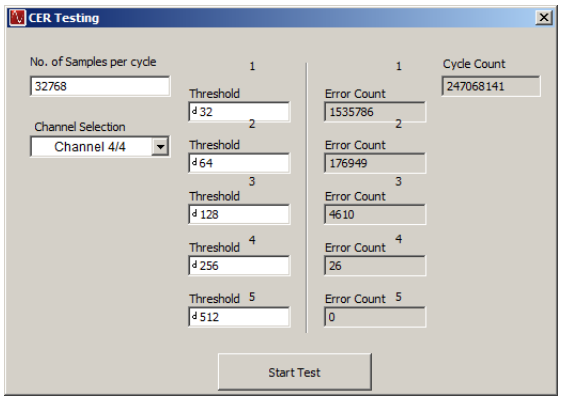


Figure 8. CER Test Window

Based on the Figure 8 settings, the test results of CER measurements under the sampling rate of 500 MSPS for the ADS54J54EVM are listed in Table 2.

Table 2. Measured Code Errors for ADS54J54 at Fs = 500 MSPS

Sampling Rate	500,000,000	Threshold	Error Count	Error Rate
Buffer length	32768	>32	3,353,112	4.86E-08
Cycle count	1052540728	>64	387,170	5.61E-09
Total codes	3.45E+13	>128	17,407	2.52E-10
Running time(H)	19.16	>256	146	2.12E-12
	—	>512	0	0

A 95% confidence level (CL) means that if the BER measurements are repeated multiple times, 95% of the results are either equal to or better than the result presented here. So at a confidence level of 0.95, no bit errors are observed above 2^{10} LSBs (or error magnitude greater than 512). See Equation 2.

$$P = \frac{-\mathrm{Ln}(1-CL)}{n} = \frac{-\mathrm{Ln}(1-0.95)}{8.1\times10^{12}} = 8.683\times10^{-14} \quad (2)$$

Consequently, if these measurements are repeated 100 times for the ADS54J54, 95 out of 100 times, the results give a BER value that is either equal to or less than 8.683×10^{-14} for bits greater than or equal to 2^{10} LSBs.

Code Error Rate Versus Sampling Frequency

Figure 9 shows the CER performances of the ADS54J54 at different sampling rates. The CER displays a strong correlation with the sampling frequency. CER significantly improves at lower sampling rates. At the sampling rate of 375 MSPS, almost no large code error occurs, because the error rate curve is very close to the expected Gaussian noise.

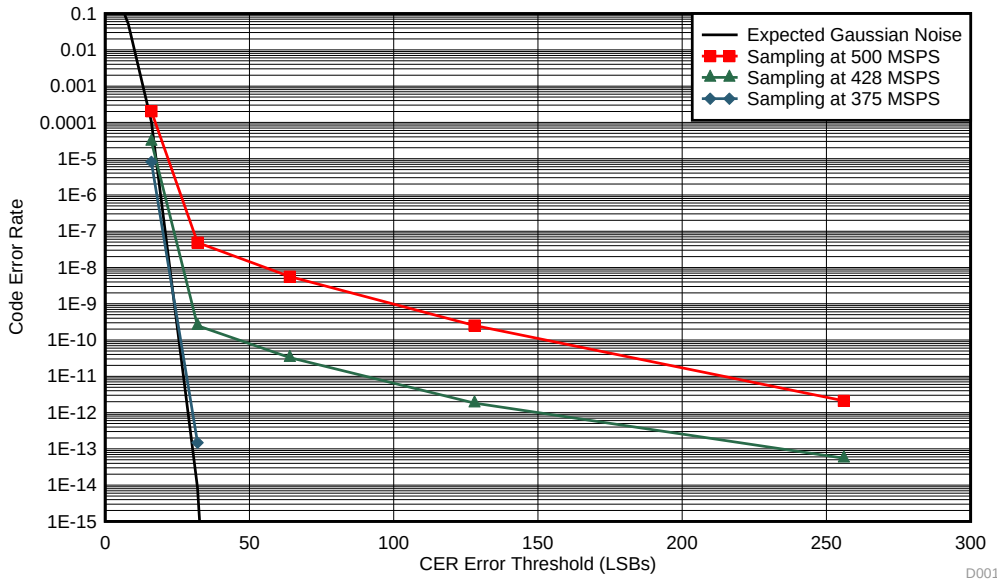


Figure 9. Measured Code Errors for the ADS54J54 at Fs = 500 MSPS

5 Conclusion

This TI Design discusses the mechanism which causes a code error, and a method to measure the CER of an ADC. Pipelined ADCs exhibit metastability that may corrupt the residue or the digital output generated. Based on the analysis and the test results returned, the CER shows strong correlation with the ADC sampling frequency. For many applications, due to the need to be observed over a large sample size, the CER is an uncommonly used metric. However, in applications where the customer is concerned with the time domain, like in an oscilloscope or a defense application, those CER measurement results could be an important metric to quantify the performance of the ADC.

6 Design Files

6.1 Schematics

To download the schematics, see the design files at TIDA-01080.

7 Software Files

To download the software files, see the design files at TIDA-01080.

8 References

1. Measuring Bit Errors in the Output Word of an A/D Converter, SLAA582 Verified TI design, Texas Instruments.
2. Find Those Elusive ADC Sparkle Codes and Metastable States, MT-011 Tutorial, Analog Devices.
3. Sedigheh Hashemi, Behzad Razavi, Analysis of Metastability in Pipelined ADCs, IEEE Journal of Solid-State Circuits, Vol. 49, No. 5, May 2014.
4. Understanding Pipelined ADCs, Tutorial 1023, Maxim Integrated.

9 About the Author

BELL YE is an analog field applications engineer at Texas Instruments based in Shanghai, China. After earning his MSEE from Southeast University in 2015, he went through TI Applications' Rotational Program, under High Speed Products. He provides customer support through TI online forums, application notes, and reference designs.

KEN CHAN is an applications engineer with TI in the high-speed data converter product line based in Dallas, TX. He supports data converter devices, systems, and solutions in high-speed signal chains covering communications and industrial applications.

IMPORTANT NOTICE FOR TI REFERENCE DESIGNS

Texas Instruments Incorporated ('TI") reference designs are solely intended to assist designers ("Designer(s)") who are developing systems that incorporate TI products. TI has not conducted any testing other than that specifically described in the published documentation for a particular reference design.

TI's provision of reference designs and any other technical, applications or design advice, quality characterization, reliability data or other information or services does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such reference designs or other items.

TI reserves the right to make corrections, enhancements, improvements and other changes to its reference designs and other items.

Designer understands and agrees that Designer remains responsible for using its independent analysis, evaluation and judgment in designing Designer's systems and products, and has full and exclusive responsibility to assure the safety of its products and compliance of its products (and of all TI products used in or for such Designer's products) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to its applications, it has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any systems that include TI products, Designer will thoroughly test such systems and the functionality of such TI products as used in such systems. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

Designers are authorized to use, copy and modify any individual TI reference design only in connection with the development of end products that include the TI product(s) identified in that reference design. HOWEVER, NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of the reference design or other items described above may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI REFERENCE DESIGNS AND OTHER ITEMS DESCRIBED ABOVE ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING THE REFERENCE DESIGNS OR USE OF THE REFERENCE DESIGNS, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNERS AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS AS DESCRIBED IN A TI REFERENCE DESIGN OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF THE REFERENCE DESIGNS OR USE OF THE REFERENCE DESIGNS, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

TI's standard terms of sale for semiconductor products (http://www.ti.com/sc/docs/stdterms.htm) apply to the sale of packaged integrated circuit products. Additional terms may apply to the use or sale of other types of TI products and services.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265