User's Guide

AM263x Control Card Hardware User's Guide

ABSTRACT

The AM263x Control Card Evaluation Module (EVM) is an evaluation and development board for the Texas Instruments Sitara™ AM263x series of microcontrollers (MCUs). This EVM provides an easy way to start developing on the AM263x MCUs with on-board emulation for programming and debugging as well as buttons and LED for a simple user interface. The control card also enables header pin access to key signals through the use of a high speed edge connector (HSEC) baseboard docking station for rapid prototyping.

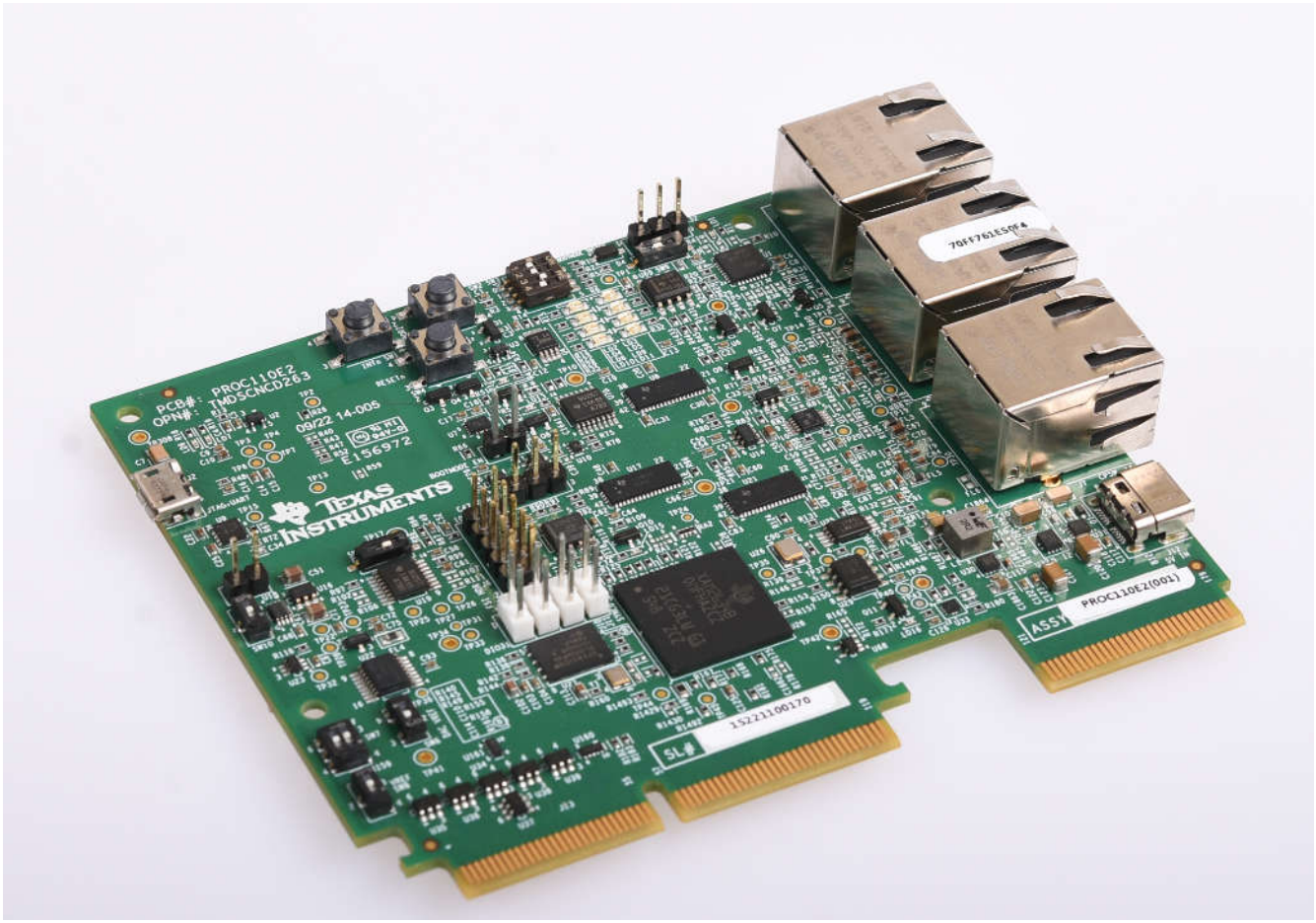

Table of Contents

1 Preface: Read This First 4
1.1 Sitara MCU+ Academy 4
1.2 If You Need Assistance 4
1.3 Important Usage Notes 4
2 Control Card Overview 5
2.1 Kit Contents 5
2.2 Key Features 6
2.3 Component Identification 7
2.4 HSEC 180-pin Control Card Docking Station 8
2.5 Compliance 8
3 Board Setup 8
3.1 Power Requirements 8
3.2 Push Buttons 13
3.3 Boot Mode Selection 14
3.4 JTAG Path Selection 15
4 Hardware Description 16
4.1 Functional Block Diagram 16
4.2 GPIO Mapping 17
4.3 Reset 18
4.4 Clock 20
4.5 Memory Interface 21
4.6 Ethernet Interface 22
4.7 I2C 28
4.8 Industrial Application LEDs 29
4.9 SPI 30
4.10 UART 30
4.11 MCAN 31
4.12 FSI 32
4.13 JTAG 32
4.14 Test Automation Header 34
4.15 LIN 35
4.16 MMC 36
4.17 ADC and DAC 37
4.18 HSEC Pinout and Pinmux Mapping 40
5 References 49
5.1 References 49
5.2 Other TI Components Used in This Design 49
Revision History 49
A E2 Design Changes 50
B E1 HSEC Pinout Table 55

List of Figures

Figure 2-1. System Architecture 5
Figure 2-2. Component Identification 7
Figure 3-1. USB Type-C Power Delivery Classification 9
Figure 3-2. Type-C CC Configuration 10
Figure 3-3. Power Status LEDs 11
Figure 3-4. E1 Power Tree Diagram of AM263x Control Card 12
Figure 3-5. Power Sequence Diagram 13
Figure 3-6. Push Buttons 13
Figure 3-7. SW3 Switch Positions 14
Figure 3-8. JTAG Path Switch Position 15
Figure 4-1. AM263x Control Card Block Diagram 16
Figure 4-2. Reset Architecture 18
Figure 4-3. PORz Reset Signal Tree 18
Figure 4-4. WARMRESETn Reset Signal Tree 19
Figure 4-5. Oscillator Clock Tree 20
Figure 4-6. Crystal Clock Tree 20
Figure 4-7. QSPI Interface 21
Figure 4-8. Board ID EEPROM 22

Figure 4-9. RGMII1 Gigabit Ethernet PHY....22
Figure 4-10. RGMII1 Gigabit Ethernet PHY Strapping Resistors....23
Figure 4-11. ICSSM Overview....24
Figure 4-12. PRU0 ICSS Gigabit Ethernet PHY Strapping Resistors....25
Figure 4-13. PRU1 ICSS Industrial Ethernet PHY Strapping Resistors....26
Figure 4-14. I2C Instances Tree....28
Figure 4-15. Industrial Application LED Driver....29
Figure 4-16. SPI....30
Figure 4-17. UART-USB Bridge for Emulation....30
Figure 4-18. UART 1:2 MUX to HSEC....31
Figure 4-19. MCAN Transceiver....31
Figure 4-20. FSI Header....32
Figure 4-21. JTAG....32
Figure 4-22. JTAG Path Switch....33
Figure 4-23. Test Automation Header....34
Figure 4-24. LIN PHY....35
Figure 4-25. Micro-SD Connector Interface....36
Figure 4-26. ADC HSEC Connections....37
Figure 4-27. ADC Switch Routing....38
Figure A-1. LIN PHY....50

List of Tables

Table 3-1. Current Sourcing Capability and State of USB Type-C Cable....10
Table 3-2. Power Status LEDs....10
Table 3-3. Control Card Push Buttons....14
Table 3-4. Supported Boot Modes....14
Table 3-5. Boot-Mode Selection Table....15
Table 4-1. GPIO Mapping Table....17
Table 4-2. Clock Source....20
Table 4-3. EEPROM Mux Table....22
Table 4-4. RGMII1 Gigabit Ethernet PHY Strapping Resistors....23
Table 4-5. Gigabit Ethernet PHY MDIO/MDC MUX....25
Table 4-6. PRU0 ICSS Gigabit Ethernet PHY Strapping Resistors....26
Table 4-7. PRU1 ICSS Industrial Ethernet PHY Strapping Resistors....27
Table 4-8. ICSS HSEC MUX....27
Table 4-9. CPSW RGMII1 RJ45 Connector LED indication....27
Table 4-10. ICSSM PRU0 RJ45 Connector LED indication....28
Table 4-11. ICSSM PRU1 RJ45 Connector LED indication....28
Table 4-12. I2C Addressing....29
Table 4-13. UART Mux Select Logic....31
Table 4-14. Test Automation Header GPIO Mapping....35
Table 4-15. LIN MUX Select Logic....35
Table 4-16. LIN Switch Logic....36
Table 4-17. LIN Node Application Switch....36
Table 4-18. ADC MUX Select Logic....38
Table 4-19. VREF Switch....38
Table 4-20. DAC VREF Switch....38
Table 4-21. ADC VREF Switch....39
Table 4-22. HSEC Pinout....40
Table 4-23. Pinmux Mapping Table....43
Table A-1. I2C2 Signal Routing....50
Table A-2. LIN MUX Selection Table....50
Table A-3. E2 Termination Resistor Location Table....51
Table A-4. E2 Buck Converter Table....51
Table A-5. E2 HSEC Connector Mapping....51
Table A-6. E1 ADC Channel Signals....52
Table A-7. E2 ADC Channel Signals....52
Table A-8. E2 HSEC MUX Table....53
Table A-9. E2 ESD Connection Mapping....53
Table B-1. E1 HSEC Pinout....55

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1 Preface: Read This First

1.1 Sitara MCU+ Academy

Texas Instruments™ offers the *MCU+ Academy* as a resource for designing with the MCU+ software and tools on supported devices. The MCU+ Academy features easy-to-use training modules that range from the basics of getting started to advanced development topics.

1.2 If You Need Assistance

If you have any feedback or questions, support for the Sitara MCUs and the AM263x Control Card development kit is provided by the TI Product Information Center (PIC) and the TI E2E™ Forum. Contact information for the PIC can be found on the TI website. Additional device-specific information can be found in the Reference Documents.

1.3 Important Usage Notes

Note

The E1 Control Cards have a known issue that will cause JTAG connection issues when using the on-board XDS110 at speeds higher than 1 MHz. A small number of E1 sample devices have a slower isolator (U53) installed that is limited to 1 MHz. If you are experiencing JTAG connections issues with Code Composer Studio™ (CCS) IDE then ensure that the target configuration being used has a JTAG TCLK Frequency of 1.0 MHz. To check the JTAG TCLK frequency of the target configuration:

1. Open the target configuration or create a new target configuration.
2. Click on the **advanced** tab to access advanced setup settings.
3. Click on **Texas Instruments XDS110 USB Debug Probe_0** connection
4. Change the default setting for **The JTAG TCLK Frequency (MHz)** from "Fixed default 5.5-MHz frequency" to "Fixed with user specified value"
5. Change the fixed user specified value from "5.5 MHz" to "1.0 MHz"
6. Click the **Save** button
7. Click **Test Connection** and confirm that there are no errors connecting to JTAG

Note

The AM263x Control Card requires a 5 V, 3A power supply in order to function. While a USB type-C cable is included, A 5 V, 3A power supply is not included in the kit and must be ordered separately The *Belkin USB-C Wall Charger* is known to work with the Control Card and supplied type-C cable. For more information on power requirements refer to Power Requirements. If there is an insufficient power input then the red LED (LD16) will glow. For more information on power status LEDs refer to Power Status LEDs.

Note

External Power Supply or Power Accessory Requirements:

- Nominal output voltage: 5-VDC
- Max output current: 3000 mA
- Efficiency Level V

Note

TI recommends using an external power supply or accessory which complies with applicable regional safety standards such as (by example) UL, CSA, VDE,CCC,PSE, etc.

Note

For a list of design changes for E2 of the AM263x Control Card, refer to E2 Design Changes

2 Control Card Overview

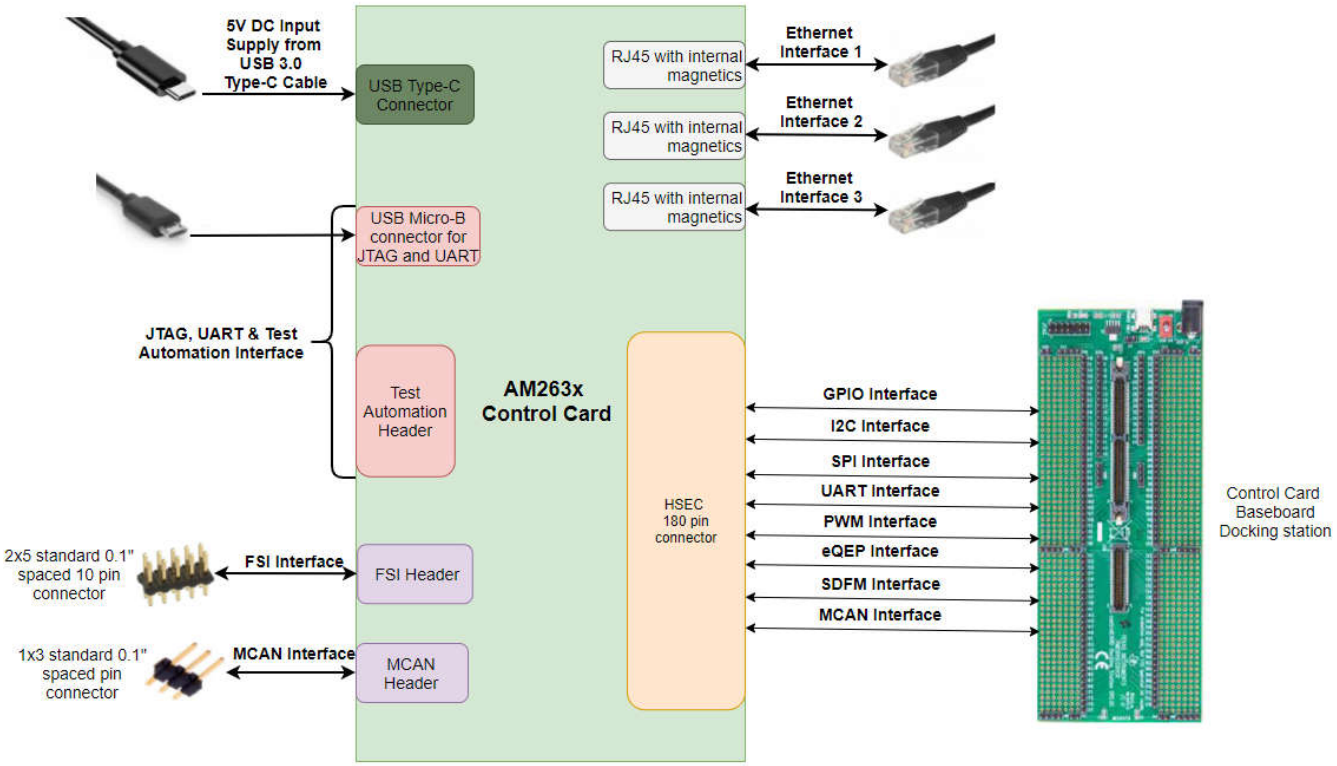

Figure 2-1. System Architecture

2.1 Kit Contents

The Sitara AM263x Control card development kit contains the following items:

- AM263x Sitara series control card development board
- Type-A to Micro-B USB cable (1 meter length)
- MicroSD Card (16Gbyte capacity)

Note

The maximum length of the IO cables shall not exceed 3 meters.

Not included:

- HSEC 180-pin Baseboard Docking Station
- Standoffs
- USB Type-C 5-V/3-A AC/DC supply and cable

2.2 Key Features

The AM263x Control Card has the following features:

- PCB dimensions: 105.76 mm width by 82.81 mm length + 6.17 mm length of HSEC interface
- Powered through 5V, 3A USB type-C input
- Three RJ45 ethernet ports capable of 1 Gb or 100Mb speeds
- On-board XDS110 debug probe
- Three push buttons:
  - PORz
  - User interrupt
  - RESETz
- LEDs for:
  - Power status
  - User testing
  - Ethernet connection
  - I2C driven array
- CAN connectivity with on-board CAN transceiver
- Dedicated FSI connector
- TI Test Automation Header
- MMC interface to micro SD card connector
- 180 pin HSEC interface for rapid prototyping
- On-board memory
  - 128 MB QSPI Flash
  - 1 MB I2C EEPROM

2.3 Component Identification

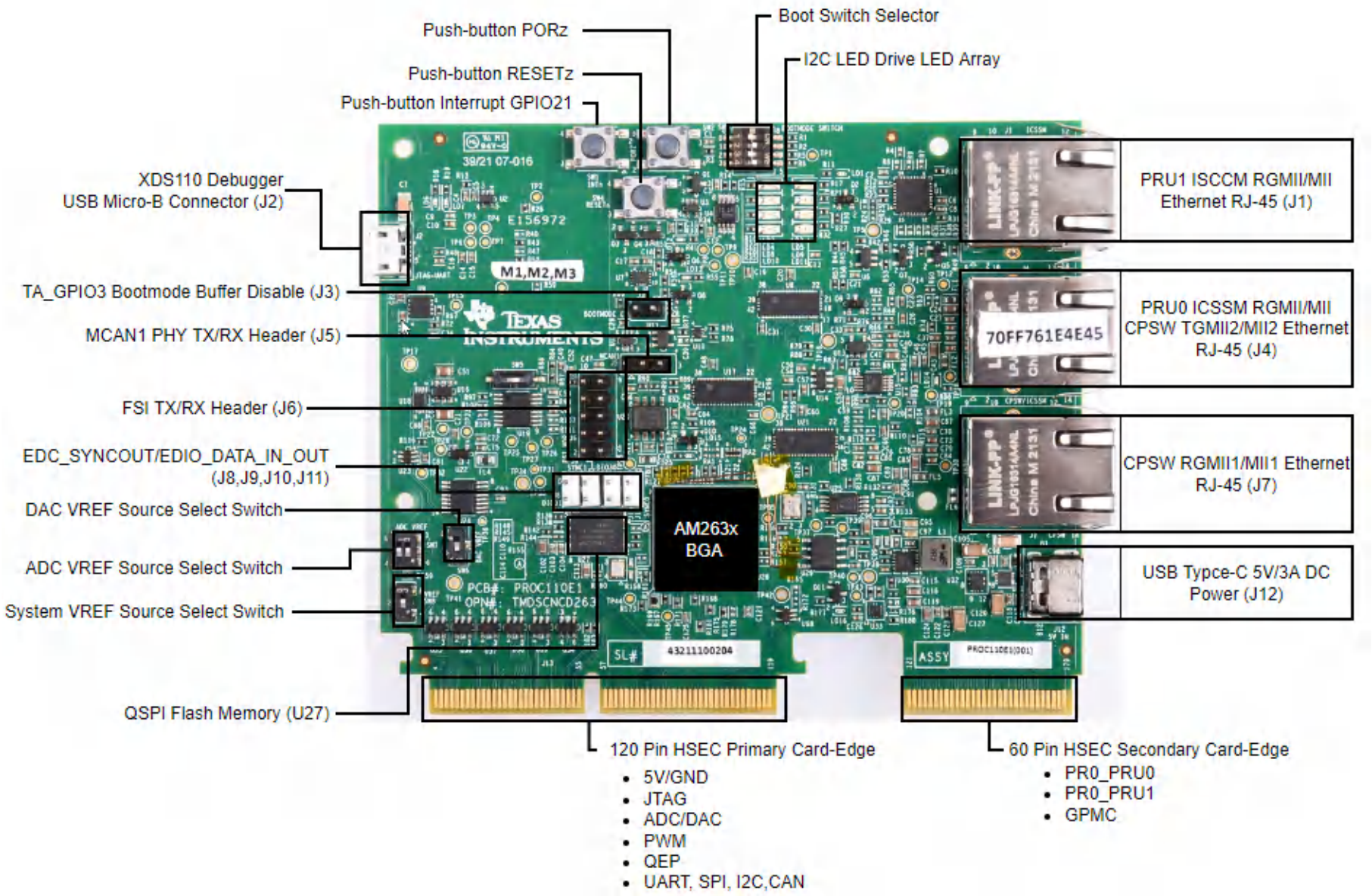

Figure 2-2. Component Identification

2.4 HSEC 180-pin Control Card Docking Station

The *TMDSHSECDOCK 180-pin docking station* is available for purchase through Texas Instruments. The docking station is a baseboard that enables rapid prototyping. There is a power switch on the docking station that determines whether power to the control card will be supplied by the 5V connector or USB connector.

Note

The docking station power switch must to be toggled to the EXT-ON side to meet the power requirements of the AM263x Control Card. EXT-ON indicates that the power is being sourced from the Barrell connector of the Control Card Dock. The mini-USB (USB-ON) connector does not meet the power requirements of the AM263x Control Card.

The AM263x Control Card has a power mux (TPS2121RUXT) that will supply power from the type-C connection as long as the voltage supplied by the type-C connection is equal to or greater than the voltage supplied by the HSEC docking station. Therefore, if both a type-C connection is present and the control card is connected to a powered HSEC docking station, then the power mux will rout the type-C supplied voltage to VMAIN of the control card. If there is no type-C connection and voltage is being supplied through the HSEC docking station then the power mux will route that voltage to VMAIN of the control card.

For more information on the docking station, refer to the *Informational Guide*

2.5 Compliance

RoHS Compliance: All components selected meet *RoHS compliance*.

Electrostatic Discharge Compliance: Components installed on the product are sensitive to Electrostatic Discharge (ESD). It is recommended this product be used in an ESD controlled environment. This may include a temperature and/or humidity controlled environment to limit the buildup of ESD. It is also recommended to use ESD protection such as wrist straps and ESD mats when interfacing with the product.

Note

The product is used in the basic electromagnetic environment as in laboratory condition and the applied standard will be as per EN IEC 61326-1:2021

3 Board Setup

3.1 Power Requirements

The AM263x Control Card is powered from a 5 V, 3 A USB type-C input or from a 5 V, 3 A HSEC connection supplied by the docking station. The following sections describe the power distribution network topology that supply the AM263x Control Card, supporting components and the reference voltages.

Power supplies that are compatible with the AM263x Control Card:

- When using the USB type-C input:
  - 5 V, 3 A power adapter with USB-C receptacle
  - 5 V, 3 A power adapter with captive USB-C cable
  - PC USB type-C port that has Power Delivery classification
    - Thunderbolt
    - Battery behind USB logo

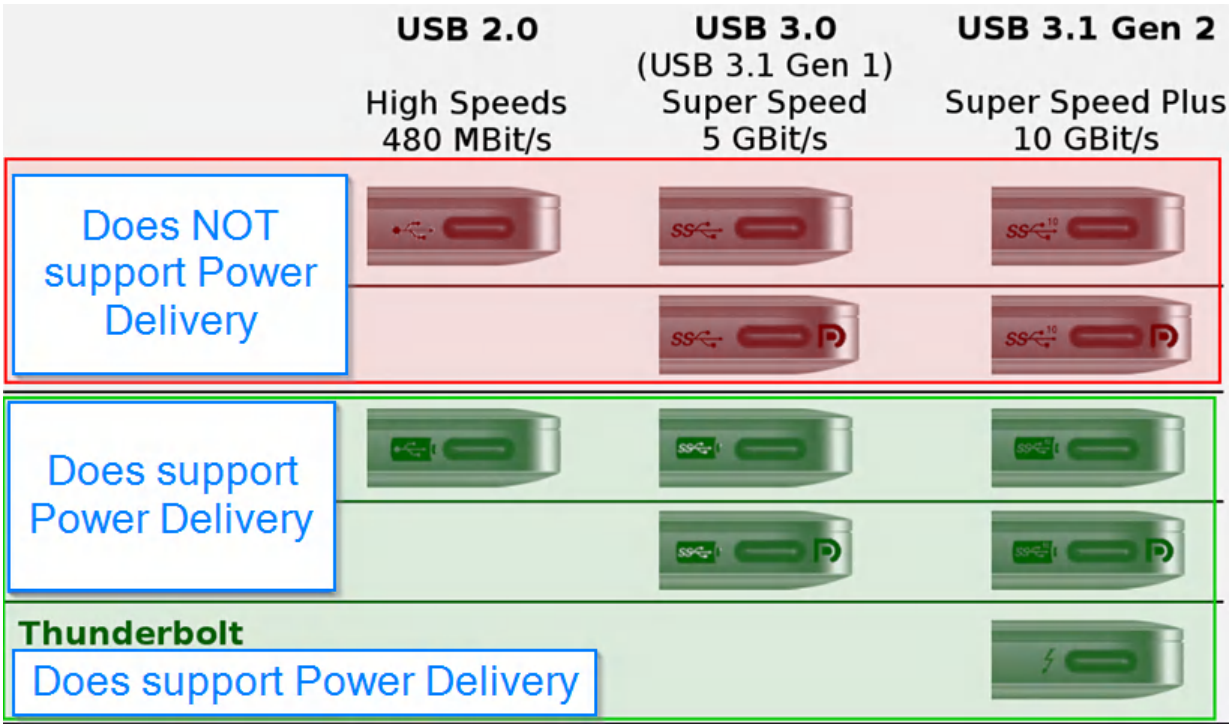

Figure 3-1. USB Type-C Power Delivery Classification

- When using the HSEC DC barrel jack power input:
  - A power adapter that is at least 15 W

Power supplies that are **NOT** compatible with the AM263x Control Card:

- When using USB type-C input:
  - Any USB adapter cables such as:
    - Type-A to type-C
    - micro-B to type-C
    - DC barrel jack to type-C
  - 5 V, 1.5 A power adapter with USB-C captive cable or receptacle
  - PC USB type-C port not capable of 3 A

3.1.1 Power Input Using USB Type-C Connector

The AM263x Control Card can be powered through a USB type-C connection. The USB Type-C source should be capable of providing 3A at 5 V and should advertise the current sourcing capability through the CC1 and CC2 signals. On this EVM, the CC1 and CC2 from the USB type-C connector are interfaced to the port controller IC (TUSB320LAIRWBR). This device uses the CC pins to determine port attach/detach, cable orientation, role detection, and port control for Type-C current mode. The CC logic detects the Type-C current mode as default, medium, or high depending on the role detected.

The Port pin is pulled down to ground with a resistor to configure the IC in upward facing port (UFP) mode. VBUS detection is implemented to determine a successful attach in UFP mode. The OUT1 and OUT2 pins are connected to a NOR gate. Active low on both the OUT1 and OUT2 pins advertises high current (3A) in the attached state which enables the load switch (TPS22965DSGT) to provide the VBUS_MAIN supply which powers other regulators that create the power rails for the device.

In UFP mode, the port controller IC constantly presents pull-down resistors on both CC pins. The port controller IC also monitors the CC pins for the voltage level corresponding to the Type-C mode current advertisement by the connected DFP. The port controller IC de-bounces the CC pins and waits for VBUS detection before successfully attaching. As a UFP, the port controller device detects and communicates the advertised current level of the DFP to the system through the OUT1 and OUT2 GPIOs.

The AM263x Control Card's power requirement is 5 V at 3A and if the source is not capable of providing the required power, the output at the NOR gate becomes low that disables the VBUS_MAIN power switch. Therefore, if the power requirement is not met, all power supplies except VSYS_TA_3V3 will remain in the off state. The board gets powered on completely only when the source can provide 5 V at 3A.

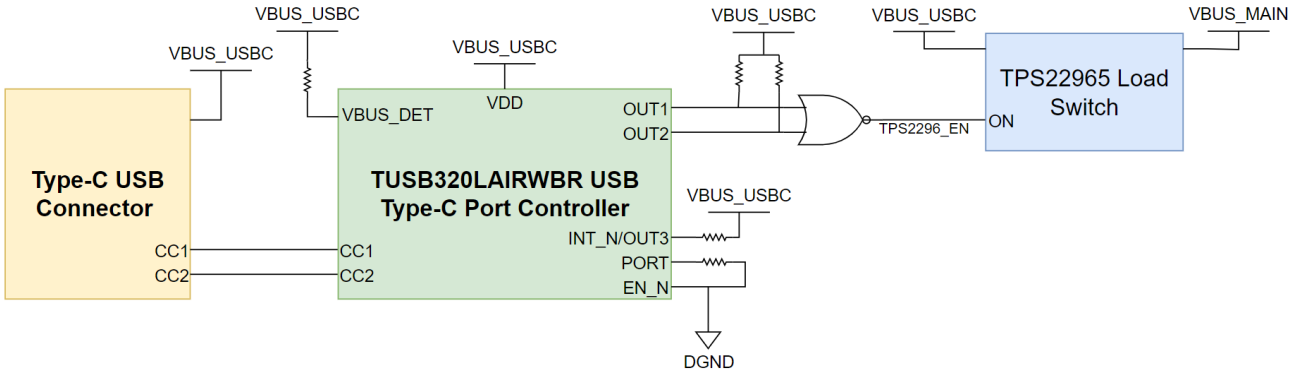

Figure 3-2. Type-C CC Configuration

Table 3-1. Current Sourcing Capability and State of USB Type-C Cable

OUT1	OUT2	Advertisement
H	H	Default current in unattached state
H	L	Default current in attached state
L	H	Medium current (1.5A) in attached state
L	L	High current (3.0A) in attached state

The AM263x Control Card includes a power solution based on discrete regulators for each of the power rails. During the initial stage of the power supply, 5V supplied by the type-C USB connector is used to generate all of the necessary voltages required by the Control Card.

Discrete DC-DC buck regulators are used to generate the supplies required for the AM263x system on a chip (SoC) and other peripherals

One DC-DC buck regulator (TPS54334) is used to generate the 3.3 V supply from the main 5V supply. The 3.3V supply is then used as Vin for two different DC-DC buck regulators: 1.2V supply (TPS62826), and 1.7V VPP supply (TPS75801). The test automation header's 3.3V supply is generated by one DC-DC buck regulator (TPS62177) from the main 5V supply.

3.1.2 Power Status LEDs

Multiple power-indication LEDs are provided on-board to indicate to users the output status of major supplies. The LEDs indicate power across various domains as shown in the table below.

Table 3-2. Power Status LEDs

Name	Default Status	Operation	Function
LD16	OFF	SAFETY_ERROR	Power error indication for voltage - VUSB_5V0
LD15	ON	VSYS_3V3	Power indicator for voltage - VSYS_3V3
LD14	ON	VSYS_TA_3V3	Power indicator for voltage -VSYS_TA_3V3
LD1	ON	VSYS_1V2	Power indicator for voltage - VSYS_1V2
LD6	OFF	XDS110_PROG_STAZ2	LED glows after XDS configuration
LD7	OFF	XDS110_PROG_STAZ1	

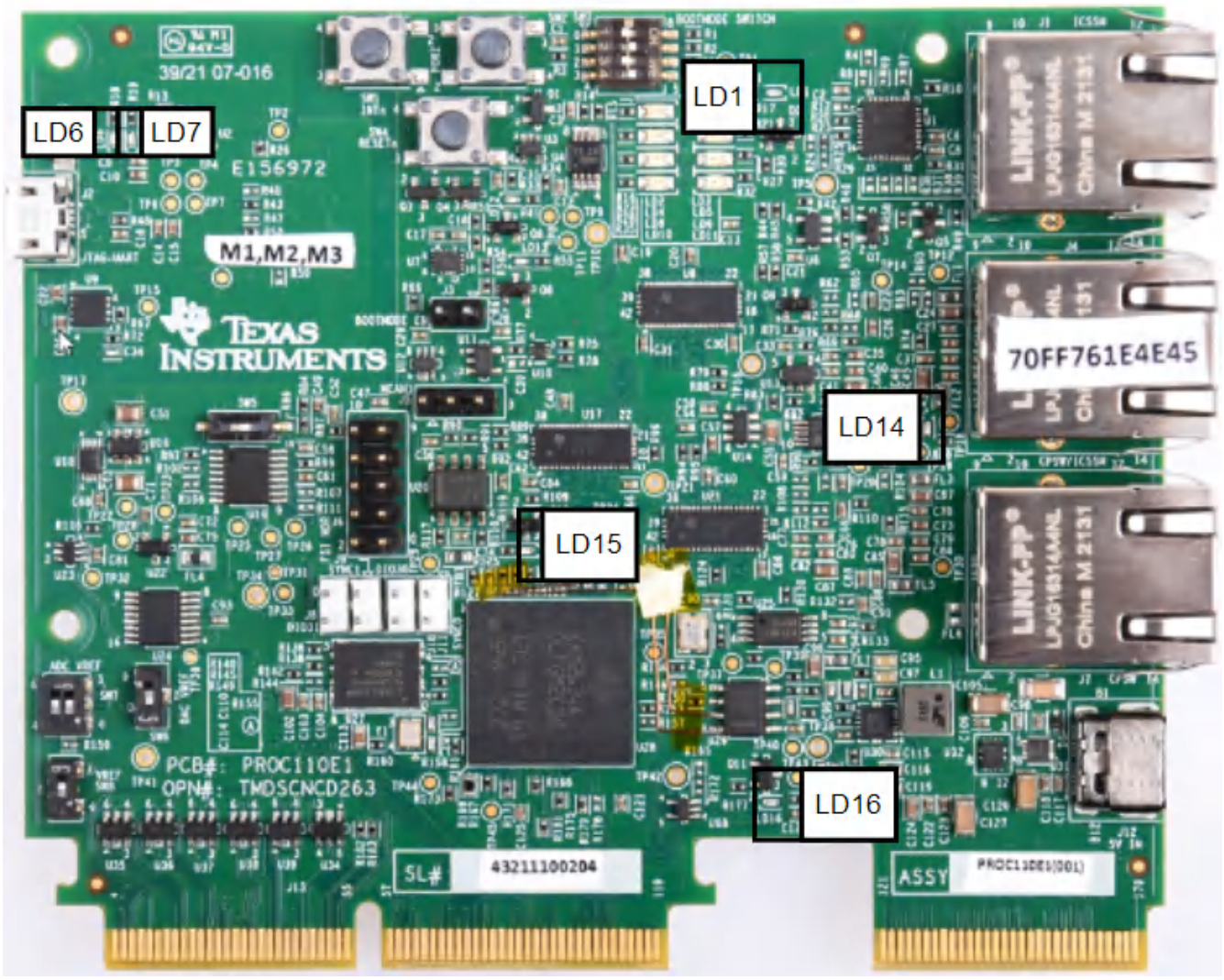

Figure 3-3. Power Status LEDs

3.1.3 Power Tree

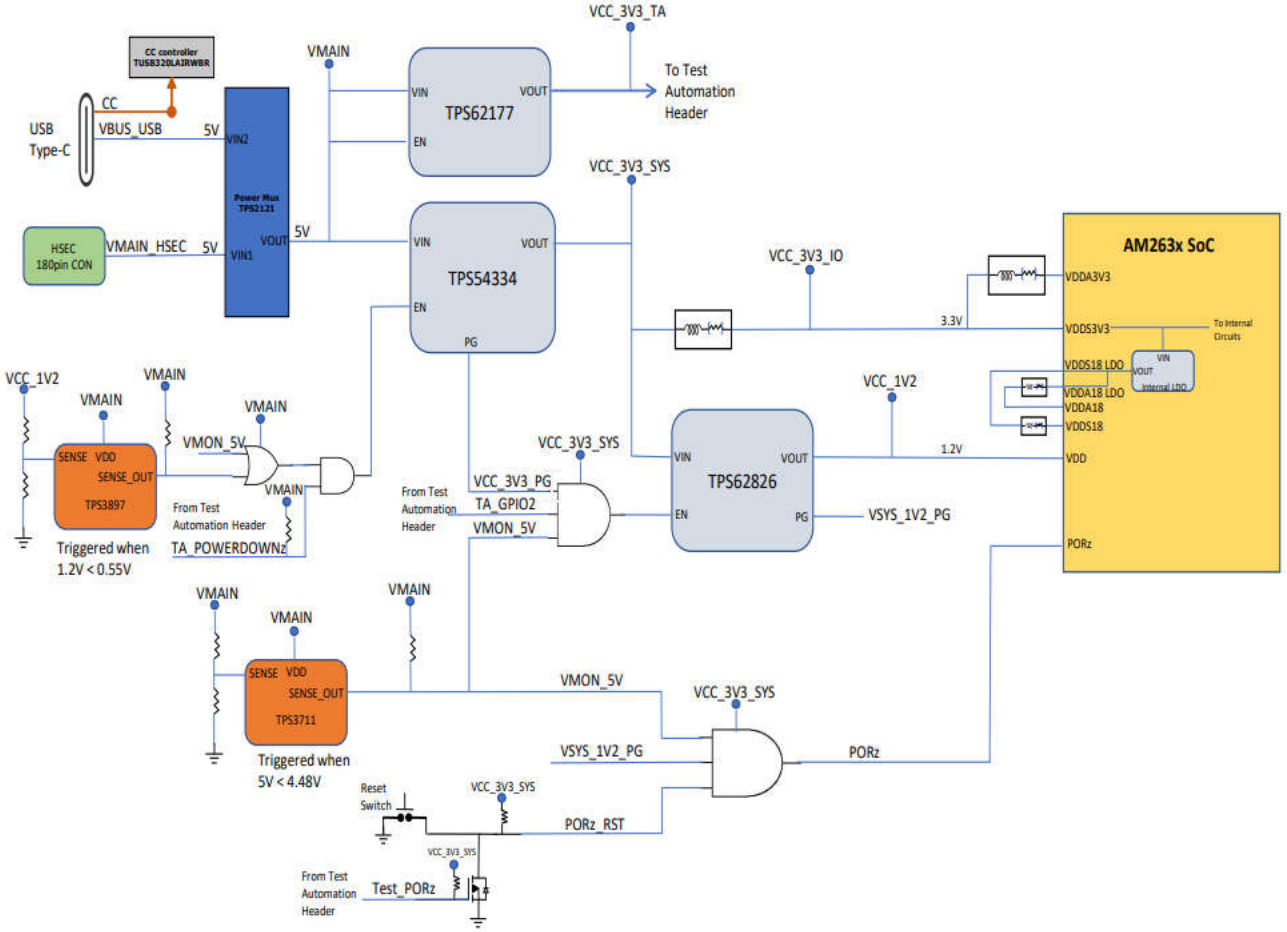

Figure 3-4. E1 Power Tree Diagram of AM263x Control Card

A. In E2 of the Control Card, the TPS62826 and TPS54334 are both changed to be TPS62913.

3.1.4 Power Sequence

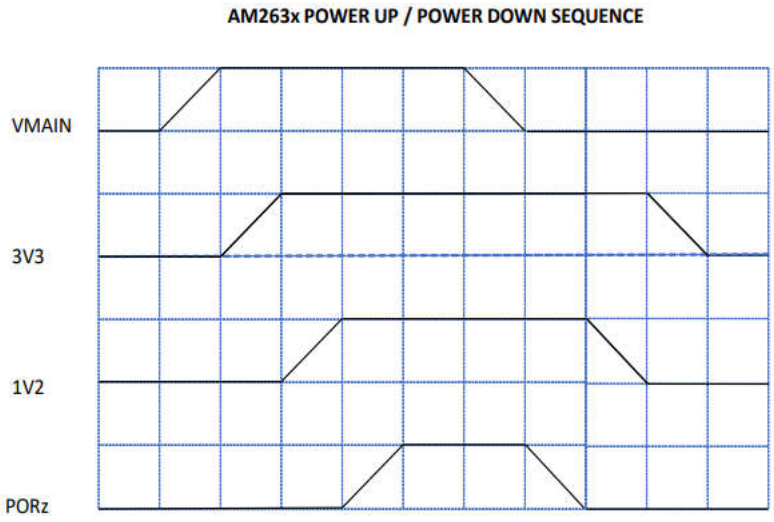

Figure 3-5. Power Sequence Diagram

3.2 Push Buttons

The control card supports multiple user push buttons that provide reset inputs and user interrupts to the processor.

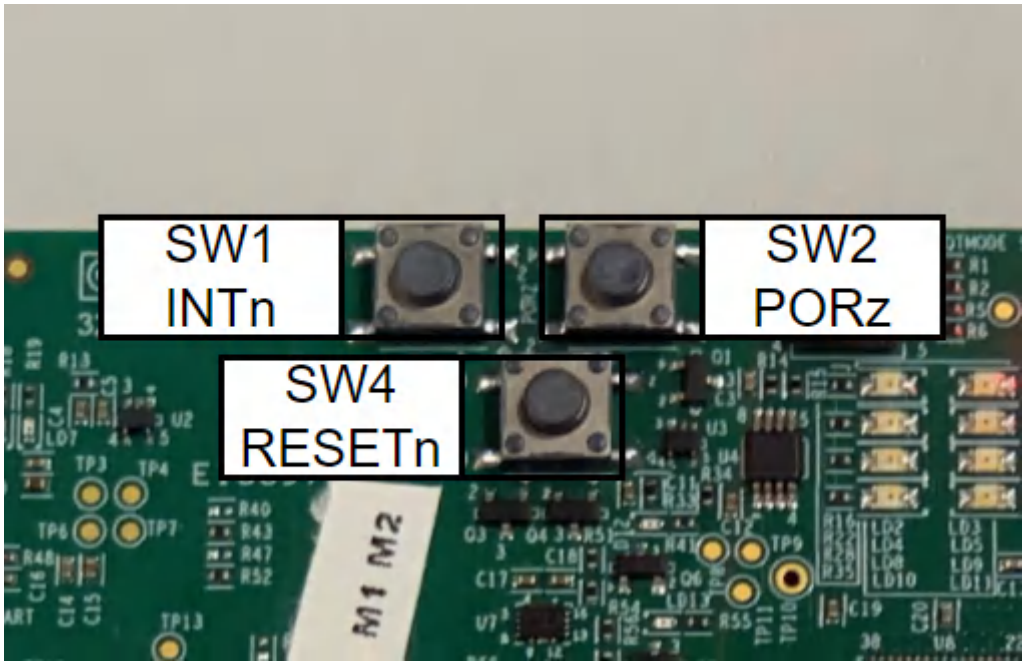

Figure 3-6. Push Buttons

Table 3-3 lists the push buttons that are placed on the top side of the AM263x control card board.

Table 3-3. Control Card Push Buttons

Push Button	Signal	Function
SW1	INTn	User Interrupt signal
SW2	PORz	SoC PORz reset input
SW4	RESETn	SoC warm reset input

3.3 Boot Mode Selection

The bootmode for the AM263x is selected by a DIP switch (SW3) or the test automation header. The test automation header uses an I2C IO expansion buffer to drive the bootmode when PORz is toggled. The supported boot modes are as shown in Table 3-4.

Table 3-4. Supported Boot Modes

Boot Mode/Peripheral	Boot Media/Host	Notes
QSPI (4S) - Quad Read Mode	QSPI Flash	Download and boot SBL from QSPI flash in quad read mode. Attempt Primary SBL, followed by Secondary SBL if primary loading fails.
UART	External Host	Download and boot SBL from UART. Device is expected to get SBL from UART. Device supports the XMODEM protocol for download over UART.
QSPI (1S) - Single Read Mode	QSPI Flash	Download and boot SBL from QSPI flash in single read mode. Attempt Primary SBL,followed by Secondary SBL if primary loading fails.
QSPI (4S) - Quad Read UART Fallback Mode	QSPI Flash / External Host	Download and boot SBL from QSPI flash in quad read mode. Attempt Primary SBL, followed by Secondary SBL if primary loading fails. If Secondary SBL also fails then boot from external host via UART interface.
QSPI (1S) - Single Read UART Fallback Mode	QSPI Flash / External Host	Download and boot SBL from QSPI flash in single read mode. Attempt Primary SBL, followed by Secondary SBL if primary loading fails. If Secondary SBL also fails then boot from external host via UART interface.
DevBoot	N/A	No SBL. Used for development purposes only.

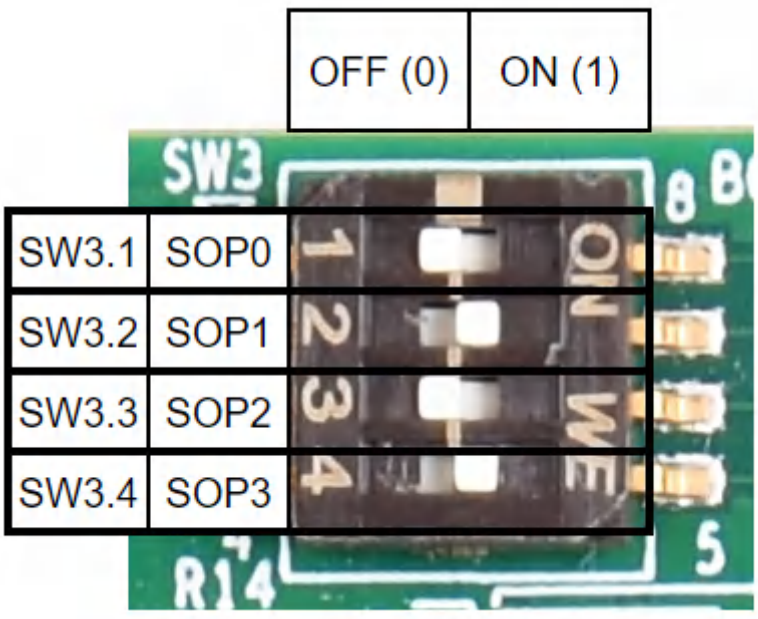

Figure 3-7. SW3 Switch Positions

Table 3-5. Boot-Mode Selection Table

Boot Mode	SPI0_D0_pad (SOP3)	SPI0_CLK_pad (SOP2)	QSPI_D1 (SOP1)	QSPI_D0 (SOP0)
QSPI (4S) - Quad Read Mode	0	0	0	0
UART	0	0	0	1
QSPI (1S) - Single Read Mode	0	0	1	0
QSPI (4S) - Quad Read UART Fallback Mode	0	1	0	0
QSPI (1S) - Single Read UART Fallback Mode	0	1	0	1
DevBoot	1	0	1	1
Unsupported Boot Mode	All other combinations not defined above			

3.4 JTAG Path Selection

The AM263x Control Card allows for JTAG connections to the SoC through the on-board XDS110 or an external emulator via the HSEC docking station. A switch (SW5) is used to drive the select line of a mux (U19) to determine the JTAG path for the SoC. The following image shows proper switch position for SW5 for the two JTAG paths.

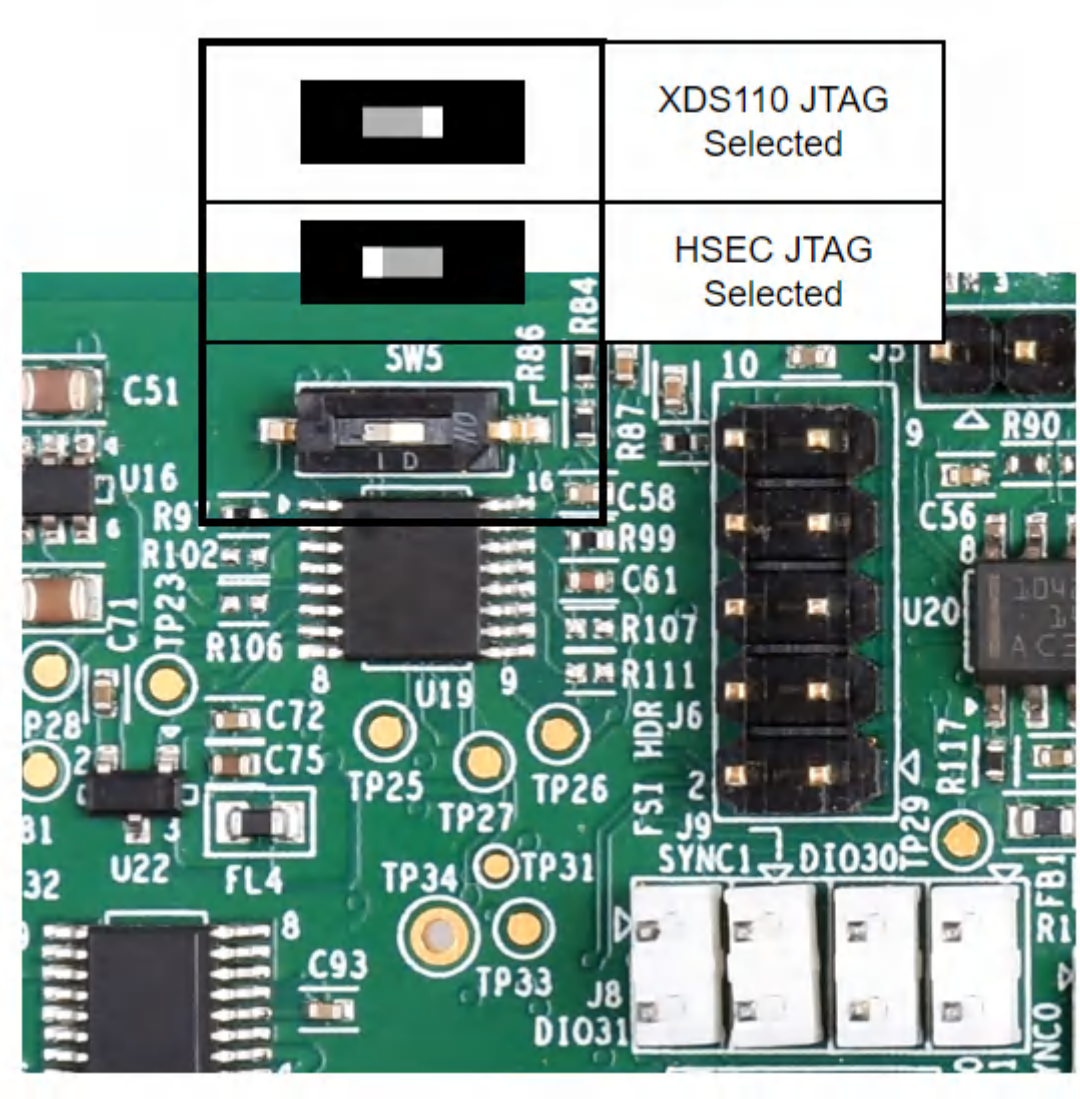

Figure 3-8. JTAG Path Switch Position

4 Hardware Description

4.1 Functional Block Diagram

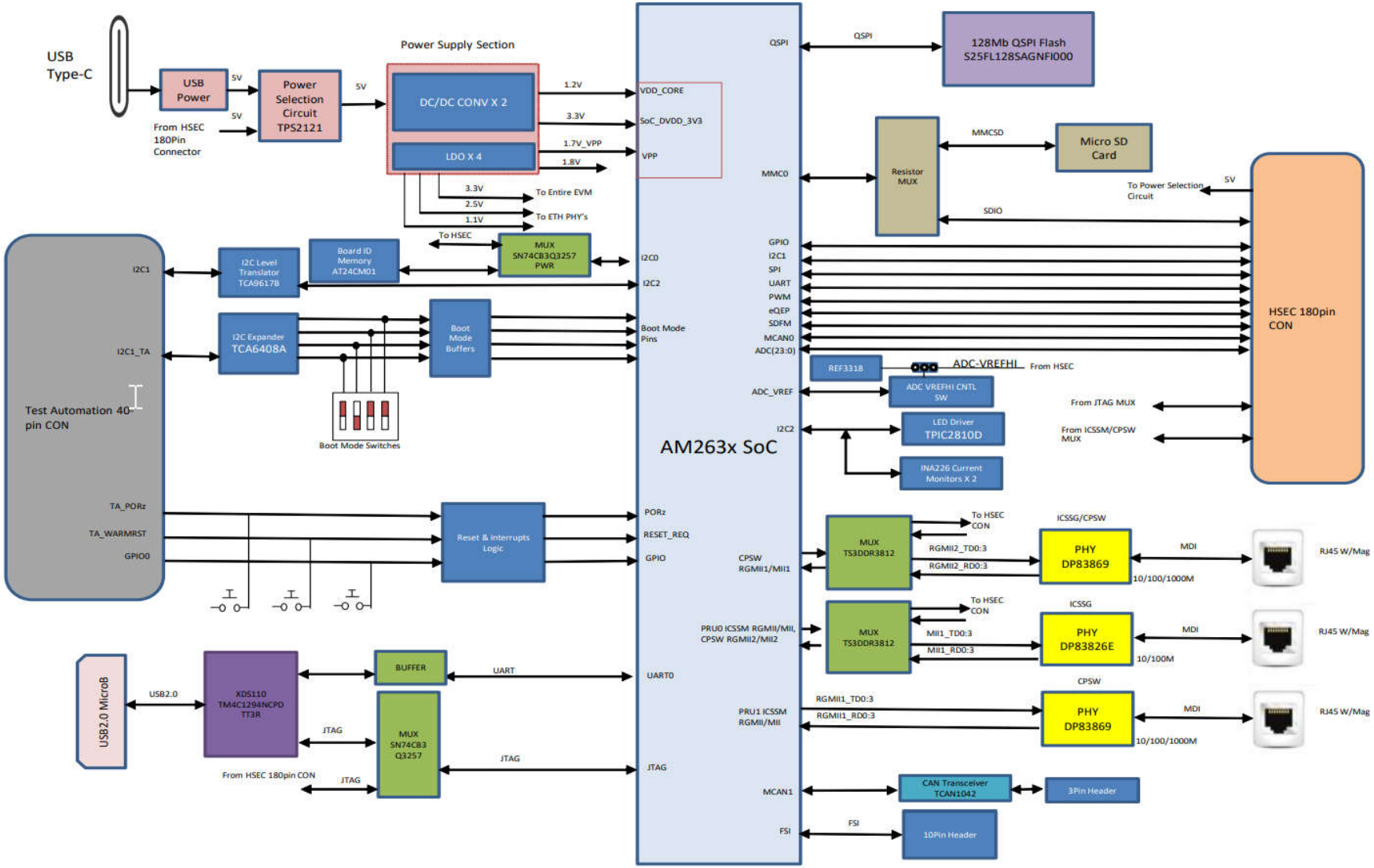

Figure 4-1. AM263x Control Card Block Diagram

4.2 GPIO Mapping

Table 4-1. GPIO Mapping Table

Sl No.	GPIO Description	GPIO	Pin Name	Functionality	Net Name	Active Status
1	Interupt To SoC	GPIO21	LIN2_RXD	Interrupt	SOC_INTn	LOW
2	Interupt To DP83826E	GPIO66	EPWM12_A	Interrupt	ICSSM2_PWDN/INTn	LOW
3	Interupt To DP83869_01	GPIO67	EPWM11_B	Interrupt	RGMII1_INT	LOW
4	Interupt To DP83869_02	GPIO68	EPWM12_B	Interrupt	ICSSM1_INT	LOW
5	User Defined LED	GPIO20	LIN2_TXD	GPIO	USER_LED0	PREFERABLE
6	User Defined LED	GPIO1	QSPI0_CSn1	GPIO	USER_LED1	PREFERABLE
IO Expander 01						
7	Standby input to CAN tranciever		P00	GPIO	MCAN1_STB	High
8	Enable control to clock buffer		P01	Enable	CLK_BUF_EN	High
9	Select line for ICSSM Mux 1		P02	Mux Selection	ICSSM1_MUX_SEL	PREFERABLE
10	Select line for ICSSM Mux 2		P03	Mux Selection	ICSSM2_MUX_SEL	PREFERABLE
11	Reset input to DP83869_01		P04	Reset	GPIO_RGMII1_RST	LOW
12	Reset input to DP83869_02		P05	Reset	GPIO_ICSSM1_RST	LOW
13	Reset input to DP83826E		P06	Reset	GPIO_ICSSM2_RST	LOW
14	Enable control to SD load switch		P07	Load SW Enable	GPIO_uSD_PWR_EN	High
15	Select line for RGMII1 MUX		P10	Mux Selection	RGMII_MUX_SEL	PREFERABLE
16	Reset Control to QSPI		P11	Reset	QSPI0_RESET	LOW
17	Select line for I2C0 MUX		P12	Mux Selection	I2C0_MUX_SEL	PREFERABLE
18	GPIO output from TA header to SoC		P13	1.2V REG EN	TA_GPIO2	PREFERABLE
19	Enable control to 1.7V LDO		P14	LDO Enable	VPP_LDO_EN	High

4.3 Reset

Figure 4-2 shows the reset architecture of the AM263x Control Card.

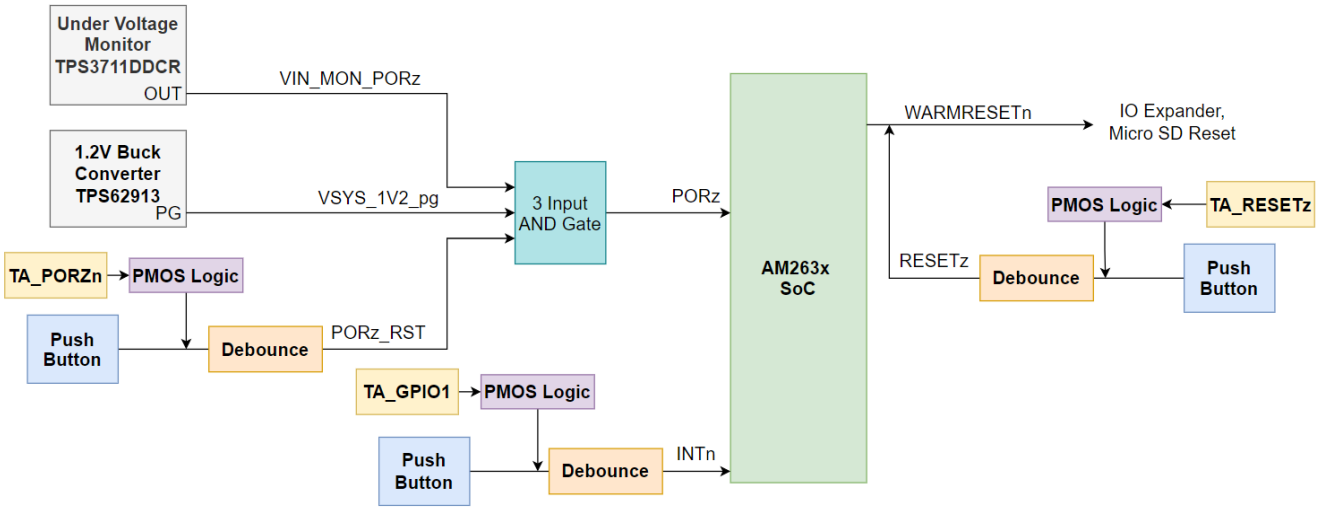

Figure 4-2. Reset Architecture

The AM263x SoC has the following resets:

- PORz is the Power-On-Reset for the MAIN Domain.
- WARMRESETn is the Warm Reset to MAIN Domain.

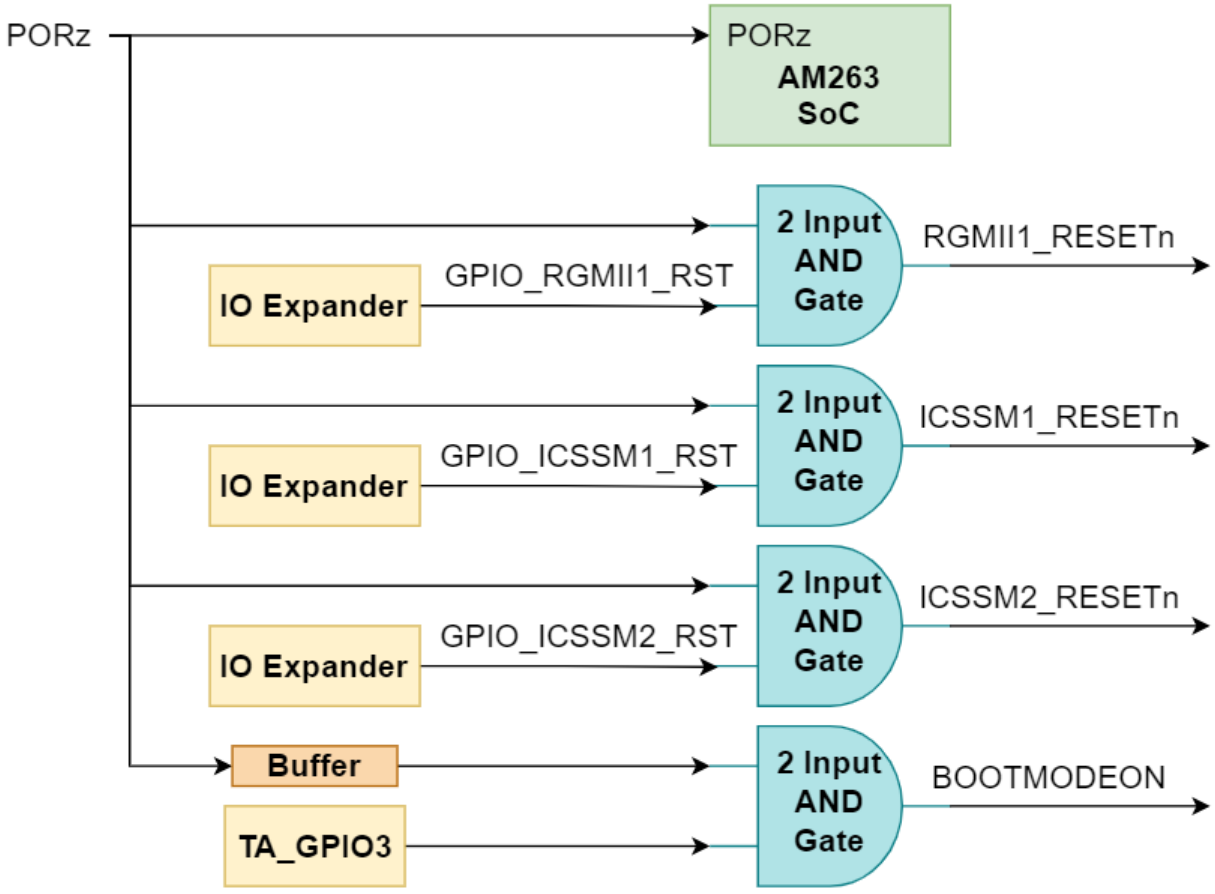

Figure 4-3. PORz Reset Signal Tree

The PORz signal is driven by a 3-input AND gate that generates a power on reset for the MAIN domain when:

- The under voltage monitor (TPS3711DDCR) has an input voltage, VMAIN, that is below 4.48 V.
- The 1.2-V buck converter (TPS62913RPUR) power good output is driven low by having an output voltage that is below the power-good threshold.
- The user push button (SW2) is pressed.
- The Test Automation Header outputs a logic LOW signal (TA_PORZn) to a P-Channel MOSFET gate which causes V_GS of the PMOS to be less than zero and so the PORz signal connects to the PMOS drain which is tied directly to ground.

The PORz signal is tied to:

- AM263x SoC PORz input
- RGMII1 Ethernet PHY reset
- ICSSM1 Gigabit Ethernet PHY reset
- ICSSM2 Industrial Ethernet PHY reset
- BOOTMODE buffer output enable

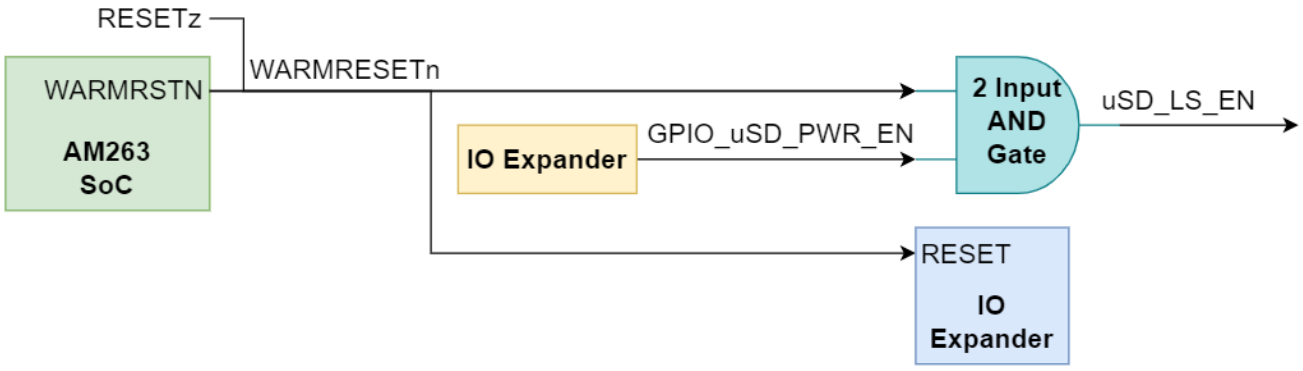

Figure 4-4. WARMRESETn Reset Signal Tree

The WARMRESETn signal creates a warm reset to the MAIN domain when:

- The user push button (SW4) is pressed.
- The Test Automation Header outputs a logic LOW signal (TA_RESETz) to a P-Channel MOSFET gate which causes V_GS of the PMOS to be less than zero and so the RESETz signal connects to the PMOS drain which is tied directly to ground.

The WARMRESETn signal is tied to:

- AM263x SoC WARMRESETN output
- RESETz signal created from push button + PMOS logic
- IO Expander reset
- Micro SD reset

The AM263x Control Card also has an external interrupt to the SoC, INTn, that occurs when:

- The user push button (SW1) is pressed.
- The Test Automation Header outputs a logic LOW signal (TA_GPIO1) to a P-Channel MOSFET gate which causes V_GS of the PMOS to be less than zero and so the INTn signal connects to the PMOS drain which is tied directly to ground.

4.4 Clock

The AM263x SoC requires a 25-MHz clock input for XTAL_XI. All reference clocks required for the SoC and the three Ethernet PHY's are generated from a single four output clock buffer (LMK1C1104PWR), which is sourced from a single 25-MHz LVCMOS Oscillator by default. A clock buffer is used for level translation from 3.3 V to 1.8 V.

The Control Card also requires a 16-MHz clock source for the TM4C129 microcontroller for UART-USB JTAG support.

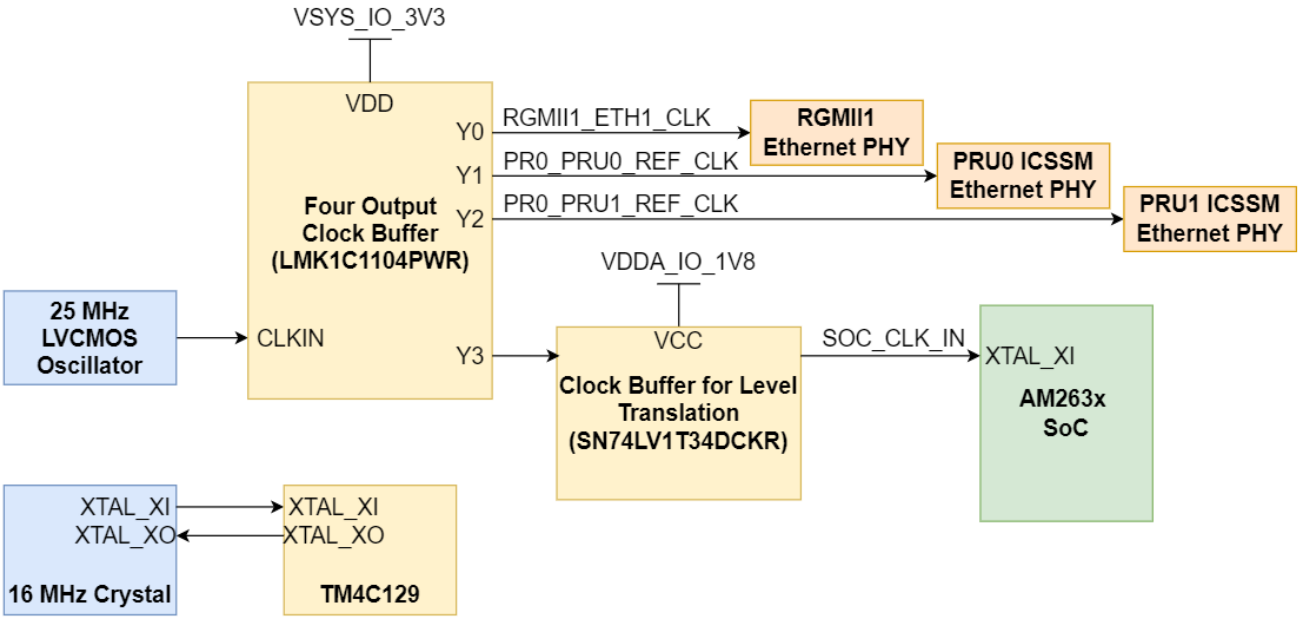

Figure 4-5. Oscillator Clock Tree

Alternatively, the SoC clock input can be sourced from a single 25-MHz crystal. To use the crystal there must be resistors mounted and unmounted. When the Crystal is used as a clock source then the AM263x CLKOUT0 signal is used to source the four output clock buffer for the Ethernet PHY reference clock signals.

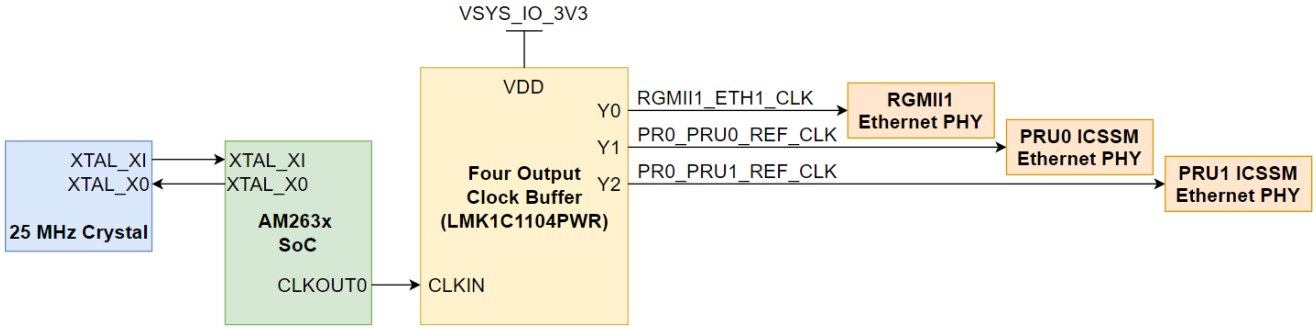

Figure 4-6. Crystal Clock Tree

The following table describes the proper resistors to be mounted and DNI'd in order for each clock source configuration.

Table 4-2. Clock Source

Clock Source	Mounted	DNI
25-MHz LVCMOS Oscillator (default)	R161, R135	R158, R155, R134
25-MHz Crystal	R158, R155, R134	R161, R135

4.5 Memory Interface

4.5.1 QSPI

The AM263x Control Card has a 128Mbit QSPI memory device (S25FL128SAGNFI000), which is connected to the QSPI0 interface of the AM263x SoC. The QSPI interface supports single data rates with memory speeds up to 104 MHz. The QSPI flash is powered by the 3.3-V IO supply.

Note

There is typically a reset pin for Flash memory. The Reset pin is not present in the WSON package that is used in the Control Card.

The QSPI0_D0/D1 signals are also used for BOOTMODE control logic. There are 10-kΩ resistors used to isolate the BOOTMODE control logic after the value is latched.

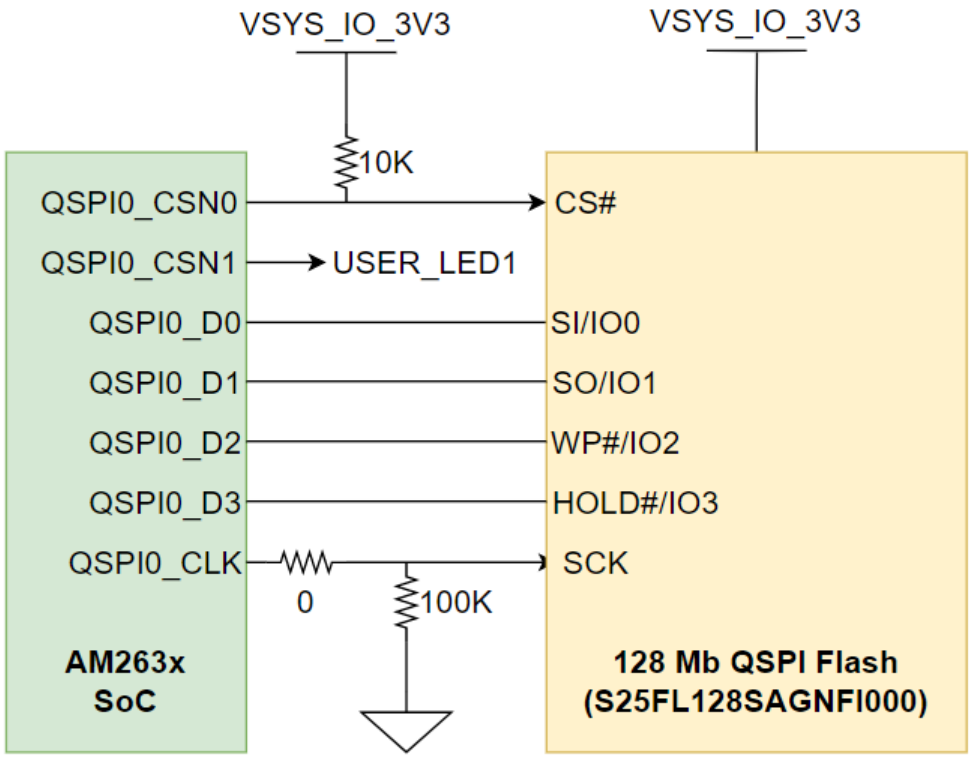

Figure 4-7. QSPI Interface

4.5.2 Board ID EEPROM

The AM263x Control Card has a I2C based 1Mbit EEPROM (CAT23M01WI-GT3) to store board configuration details. The Board ID EEPROM is connected to the I2C0 interface of the AM263x via a 1:2 Mux (SN74CB3Q3257PWR). The default I2C address of the EEPROM is set to 0x50 by pulling down the address pins A1 and A2 to ground. The Write Protect pin for the EEPROM is by default pulled down to ground and therefore Write Protect is disabled. There is also the option to enable write protect by removing the 10KΩ pull down resistor (R273) and mounting a pull up resistor (R268) to the 3.3 V IO voltage supply.

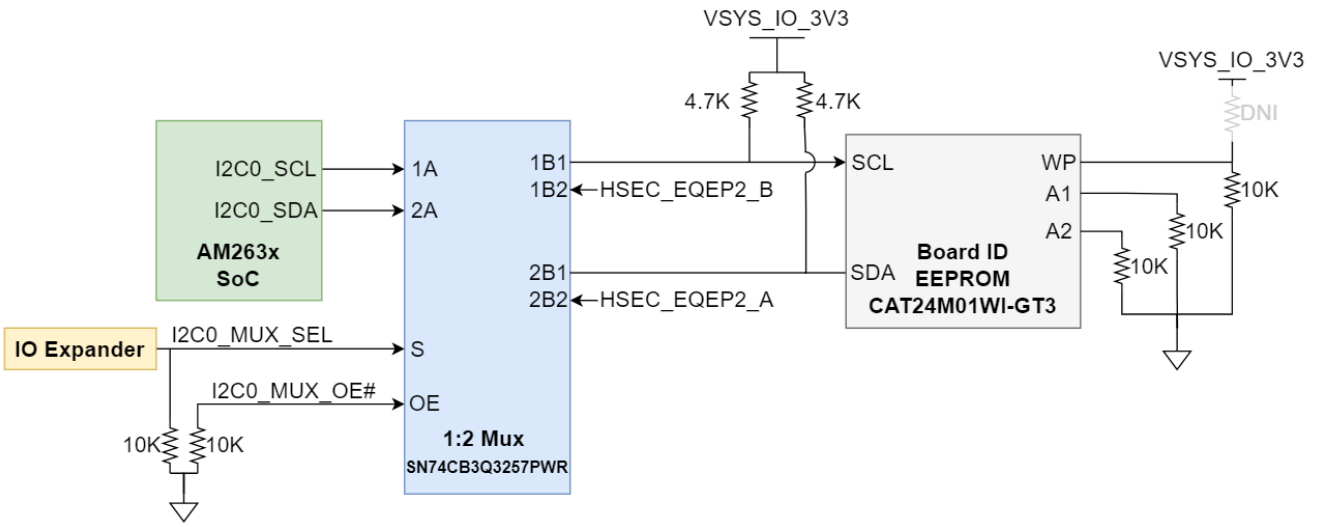

Figure 4-8. Board ID EEPROM

The GPIO Expander is used to control the select signal (I2C0_MUX_SEL) of the 1:2 Mux.

Table 4-3. EEPROM Mux Table

Select	Condition	Mux Function
HIGH	HSEC EQEP Selected	A→B2 port
LOW	I2C0 Selected	A→B1 port

4.6 Ethernet Interface

4.6.1 RGMII

The AM263x Control Card uses one port of RGMII signals to be connected to a 48-pin ethernet PHY (DP83869HMRGZT). The PHY is configured to advertise 1-Gb operation. The ethernet data signals of the PHY are terminated to an RJ45 connector. The RJ45 connector is used on the board for Ethernet 10/100/1000 Mbps connectivity with integrated magnetic and LEDs for link and activity indication.

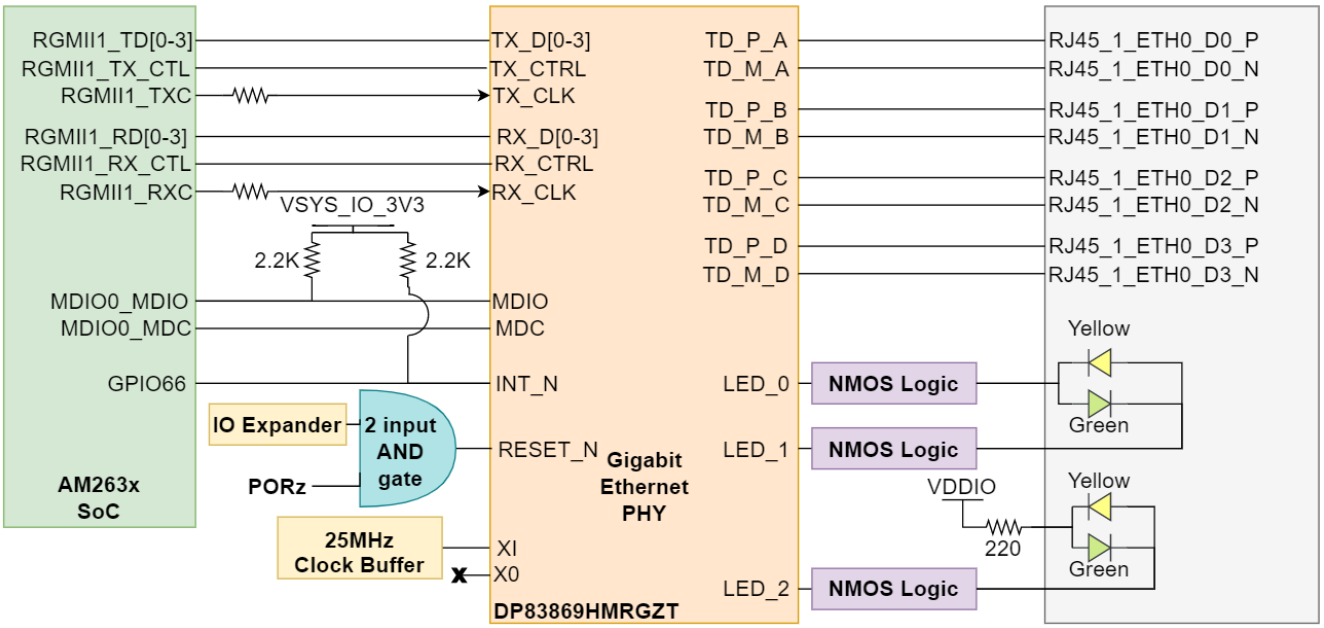

Figure 4-9. RGMII1 Gigabit Ethernet PHY

The Ethernet PHY requires three separate power sources. VDDIO is the 3.3V, system generated supply. There are dedicated LDO's for the 1.1 V and 2.5 V supplies for the Ethernet PHY.

There are series termination resistors on the transmit and receive clock signals located near the AM263x SoC.

The MDIO and Interrupt signals from the SoC to the PHY require 2.2KΩ pull up resistors to the I/O supply voltage for proper operation. The interrupt signal is driven by a GPIO signal that is mapped from the AM263x SoC.

The reset signal for the Ethernet PHY is driven by a 2-input AND gate. The AND gate's inputs are a GPIO signal that is generated by the IO Expander and PORz.

The Ethernet PHY uses many functional pins as strap option to place the device into specific modes of operation.

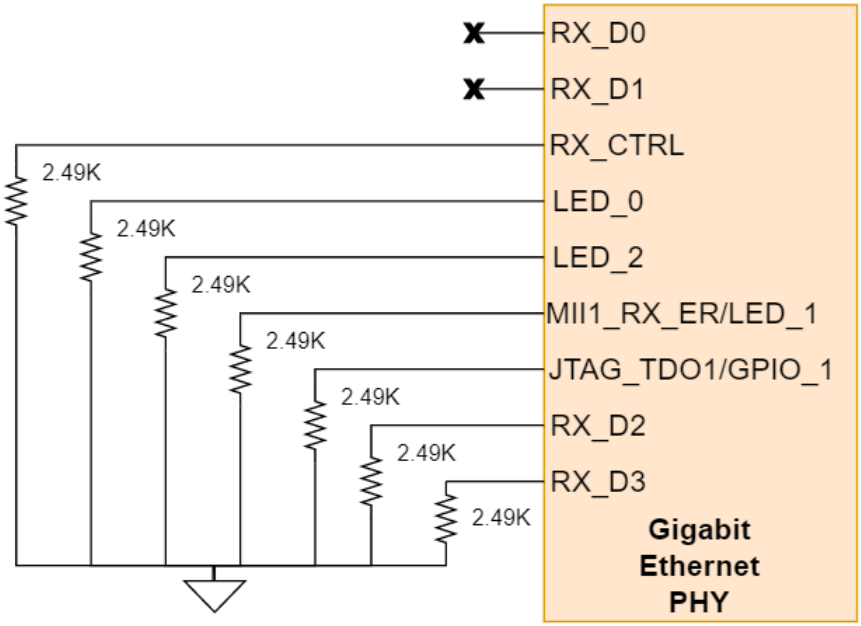

Figure 4-10. RGMII1 Gigabit Ethernet PHY Strapping Resistors

Note

RX_D0 and RX_D1 are open rather than pulled down with 2.49KΩ resistors because they are on a 4-level strap resistor mode scheme. All other signals are 2-level strap resistor modes.

Note

Each strapping has an internal pull down resistance of 9KΩ.

Table 4-4. RGMII1 Gigabit Ethernet PHY Strapping Resistors

Functional Pin	Default Mode	Mode in CC	Function
RX_D0	0	0	PHY address: 0000
RX_D1	0	0	
JTAG_TDO/GPIO_1	0	0	RGMII to Copper
RX_D3	0	0	
RX_D2	0	0	
LED_0	0	0	Auto-negotiation, 1000/100/10 advertised, auto MDI-X
RX_ER	0	0	
LED_2	0	0	
RX_DV	0	0	Port Mirroring Disabled

4.6.2 PRU-ICSS

Note

The PRU internal pinmux mapping provided in the TRM is part of the original hardware definition of the PRU. However, due to the flexibility provided by the IP and associated firmware configurations, this is not necessarily a hard requirement. The first PRU implementation for AM65x had the MII TX pins swapped during initial SoC integration and this convention was maintained for subsequent PRU revisions to enable firmware reuse. To make use of the SDK firmware, use the SYSCONFIG generated PRU pin mapping.

The AM263x Control Card makes use of two on-die programmable real-time unit and industrial communication subsystem's (PRU-ICSS) of the AM263x SoC to interface with two Ethernet PHY transceivers. There is a Gigabit Ethernet PHY transceiver (DP83869HMRGZT) connected to PRU0 of the SoC and an industrial Ethernet PHY transceiver (DP83826ERHBT) connected to PRU1. The ethernet data signals of each PHY are terminated to an RJ45 connector. The RJ45 connectors are used on the board for Ethernet 10/100/1000 (DP83869HMRGZT) and 10/100 (DP83826ERHBT) Mbps connectivity with integrated magnetic and LEDs for link and activity indication.

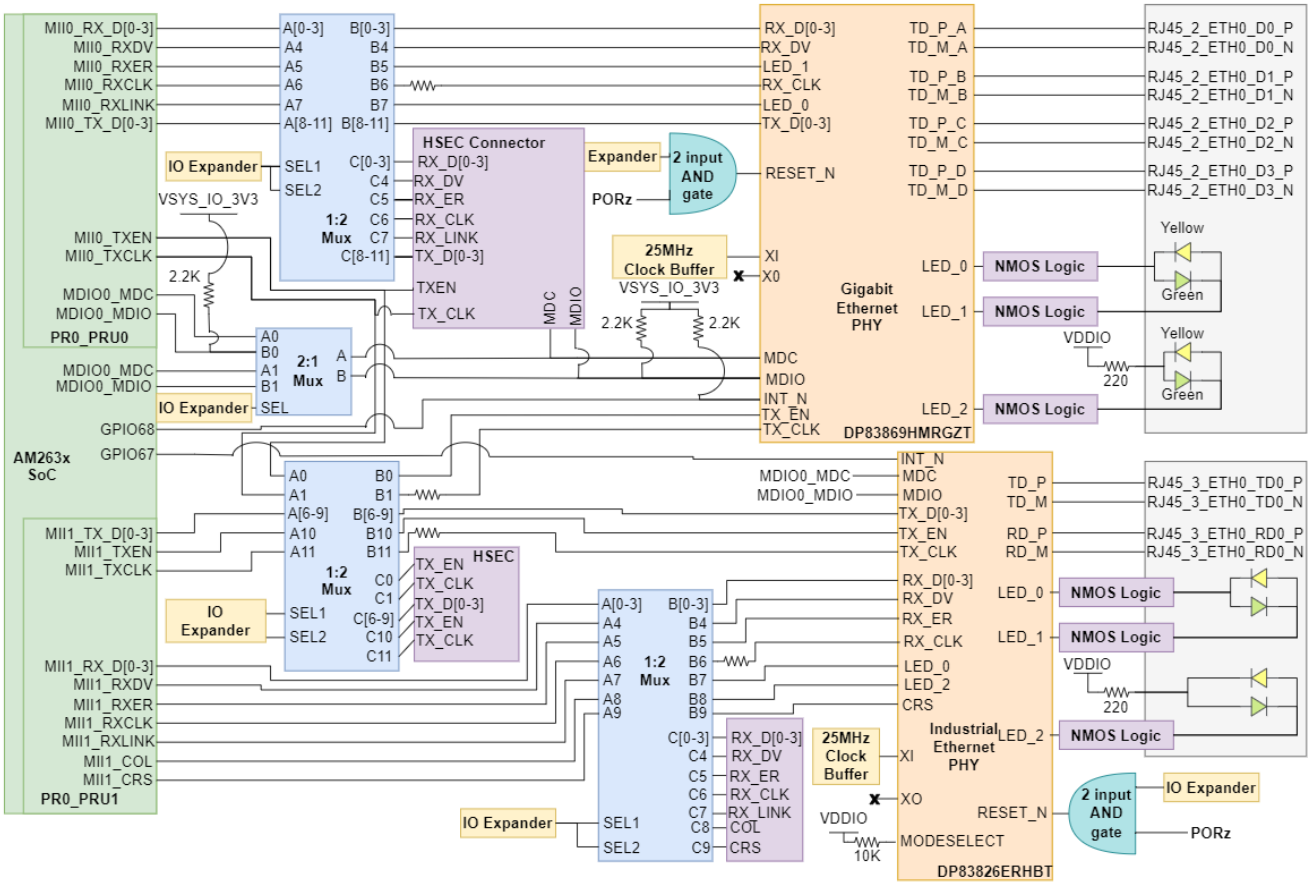

Figure 4-11. ICSSM Overview

For the Gigabit Ethernet PHY:

- The Ethernet PHY requires three separate power sources. VDDIO is the 3.3 V, system generated analog supply. There are dedicated LDO's for the 1.1 V and 2.5 V supplies for the Ethernet PHY.
- The Ethernet PHY uses many functional pins as strap options to place the device into a specific mode of operation. Each functional pin has a default mode that is driven by an internal pull resistor.
- There is a 2:1 mux (TMUX154EDGSR) that controls the mapping of MDIO and MDC signals for the ethernet PHY's.

Table 4-5. Gigabit Ethernet PHY MDIO/MDC MUX

SEL	Condition	Function
HIGH	AM263x SoC MDIO0 MDIO/MDC signals selected	A1/B1→A/B port
LOW	PRU MDIO/MDC signals selected	A0/B0→ A/B port

- The Ethernet PHY uses many functional pins as strap options to place the device into a specific mode of operation. Each functional pin has a default mode that is driven by an internal pull resistor.

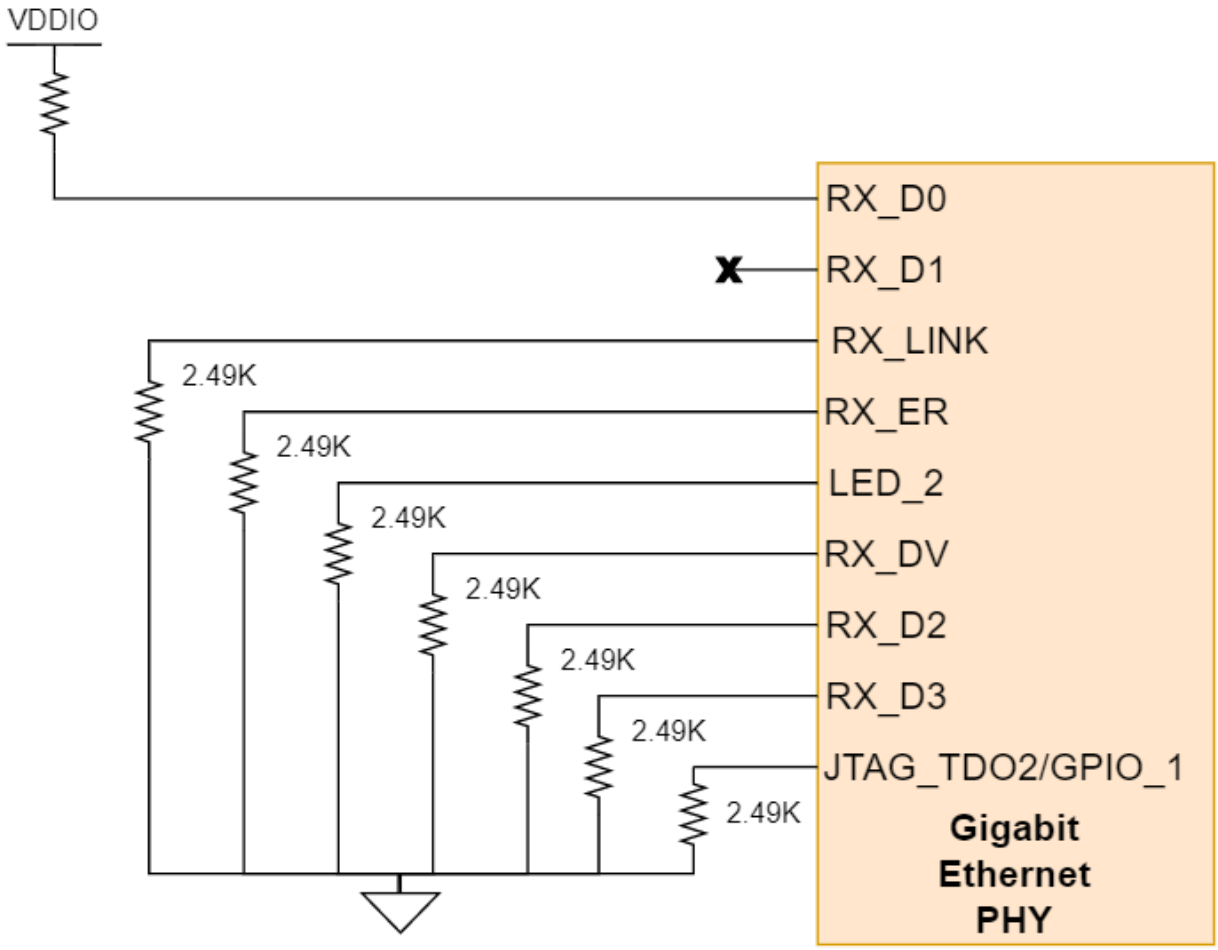

Figure 4-12. PRU0 ICSS Gigabit Ethernet PHY Strapping Resistors

Table 4-6. PRU0 ICSS Gigabit Ethernet PHY Strapping Resistors

Functional Pin	Default Mode	Mode in CC	Function
RX_D0	0	3	PHY address: 0011
RX_D1	0	0	
JTAG_TDO/GGPIO_1	0	0	RGMII to Copper
RX_D3	0	0	
RX_D2	0	0	
RX_LINK	0	0	Auto-negotiation, 1000/100/10 advertised, auto MDI-X
RX_ER	0	0	
LED_2	0	0	
RX_DV	0	0	Port Mirroring Disabled

For the Industrial Ethernet PHY transceiver:

- The Ethernet PHY requires two separate power sources. VDDIO is the 3.3 V, system generated analog supply. VSYS_IO_3V3 is the 3.3 V I/O supply.
- The Ethernet PHY is set to ENHANCED mode by pulling the MODESELECT pin up to VDDIO.
  - ENHANCED mode allows the DP83826E to support real-time Ethernet applications in addition to standard Ethernet applications.
- The Ethernet PHY uses many functional pins as strap options to place the device into a specific mode of operation. Each functional pin has a default mode that is driven by an internal pull resistor.

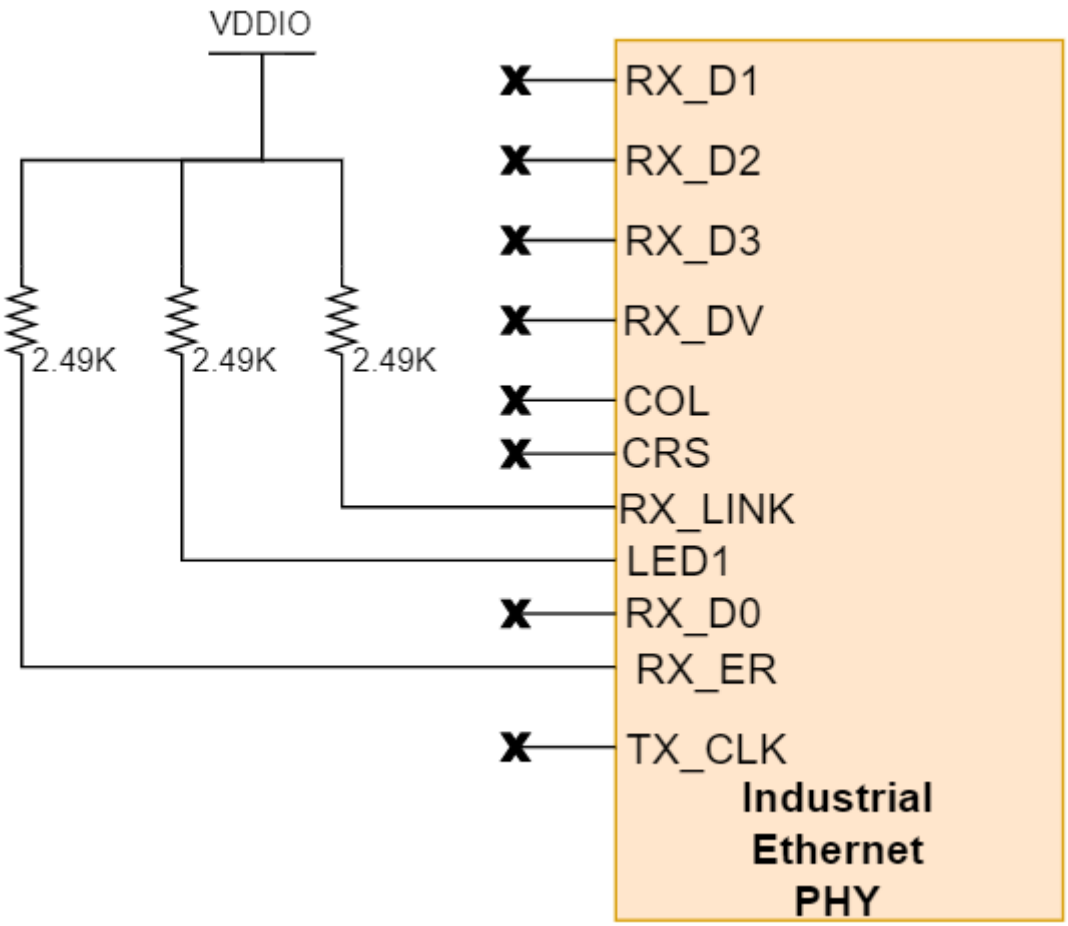

Figure 4-13. PRU1 ICSS Industrial Ethernet PHY Strapping Resistors

Table 4-7. PRU1 ICSS Industrial Ethernet PHY Strapping Resistors

Functional Pin	Default Mode	Mode in CC	Function
RX_D0	1	1	Auto-negotiation enable
LED1	1	1	Odd nibble detection enable
RX_LINK	0	1	PHY address: 001
CRS	0	0	
COL	0	0	
TX_CLK	0	0	RMII Controller Mode
RX_ER	0	1	LED1 on pin 31
RX_D3	0	0	Fast link-drop disable
RX_D2	0	0	MII MAC mode
RX_D1	0	0	Auto MDIX enable
RX_DV	0	0	MDIX (applicable only when auto-MIDX is disabled)

For both Ethernet PHY's:

- There are series termination resistors on the transmit and receive clock signals located near the AM263x SoC.
- The MDIO and Interrupt signals from the SoC to the PHY require 2.2KΩ pull up resistors to the I/O supply voltage for proper operation. The interrupt signal is driven by a GPIO signal that is mapped from the AM263x SoC.
- The reset signal for the Ethernet PHY is driven by a 2-input AND gate. The AND gate's inputs are a GPIO signal that is generated by the IO Expander and PORz.
- A 25 MHz clock is sourced from a four output clock buffer that has a 25 MHz oscillator as an input.
- There are three 1:2 muxes (TS3DDR3812RUAR) that control the mapping of ethernet signals from the SoC to either the Ethernet PHY's or the HSEC connector. The select logic for the three muxes is driven by two GPIO signals that are generated by the IO expander.

Table 4-8. ICSS HSEC MUX

Select Signal	Logic Level	Condition	Function
ICSSM1_MUX_SEL	LOW	PRU0 signals mapped to Ethernet PHY	A[n] → B[n]
	HIGH	PRU0 signals mapped to HSEC	A[n] → C[n]
ICSSM2_MUX_SEL	LOW	PRU1 signals mapped to Ethernet PHY	A[n] → B[n]
	HIGH	PRU1 signals mapped to HSEC	A[n] → C[n]

4.6.3 LED Indication in RJ45 Connector

The AM263x Control Card has three RJ45 network ports for the RGMII and two ICSSM ports of the AM263x SoC. Each RJ45 connector contains two bi-color LEDs that are used to indicate link and activity.

- RJ45 Connector LED indication for the CPSW RGMII1 port:

Table 4-9. CPSW RGMII1 RJ45 Connector LED indication

LED	Color	Indication
Right LED	Green	Ethernet PHY power established
	Yellow	Transmit or Receive activity
Left LED	Green	Link OK
	Yellow	1000BT link is up

- RJ45 Connector LED indication for the ICSSM PRU0 port:

Table 4-10. ICSSM PRU0 RJ45 Connector LED indication

LED	Color	Indication
Right LED	Green	Ethernet PHY power established
	Yellow	Transmit or Receive activity
Left LED	Green	Link OK
	Yellow	1000BT link is up

- RJ45 Connector LED indication for the ICSSM PRU1 port:

Table 4-11. ICSSM PRU1 RJ45 Connector LED indication

LED	Color	Indication
Right LED	Green	Ethernet PHY power established
	Yellow	10BT speed link is up
Left LED	Green	Link OK
	Yellow	1000BT speed link is up

4.7 I2C

The AM263x Control Card uses three AM263x SoC inter-integrated circuit (I2C) ports to operate as a controller for various targets. It is important that all I2C data and clock lines are pulled up to the 3.3 V IO voltage supply to enable communication.

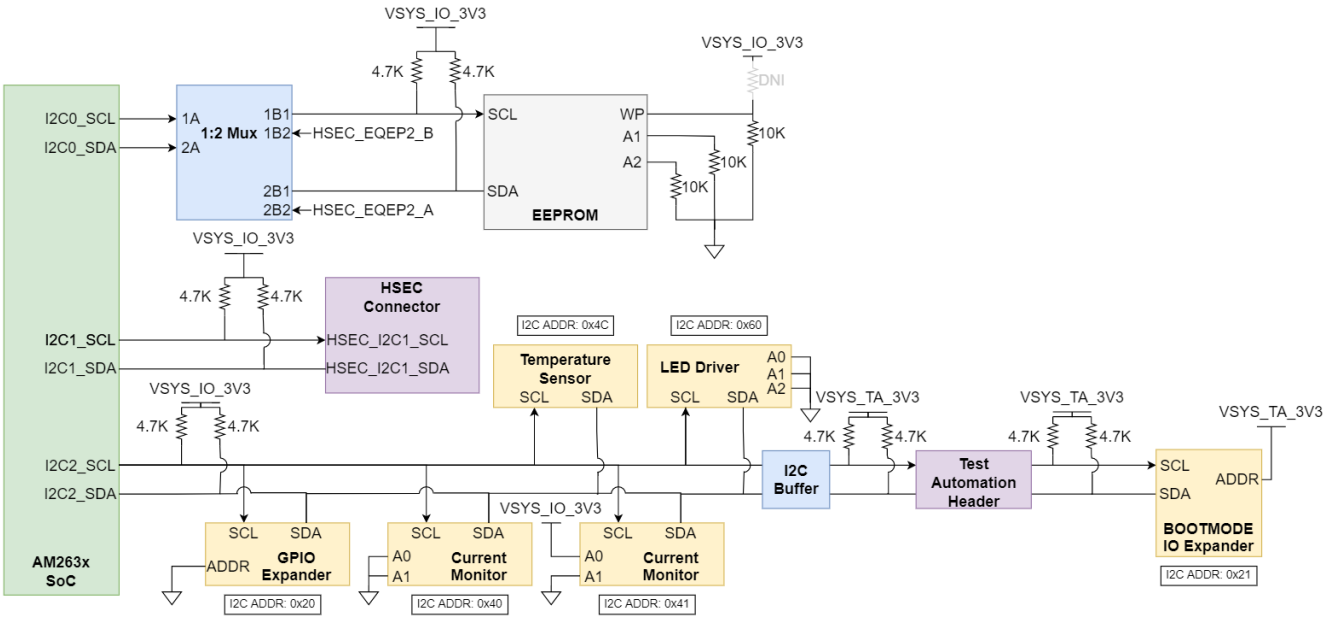

Figure 4-14. I2C Instances Tree

Table 4-12. I2C Addressing

Target	I2C Instance	I2C Address Bit Description	Device Configuration	CC Config.	I2C Address
Board ID EEPROM	I2C0	The first 4 bits of the device address are set to 1010, the next two are set by the A2 and A1 pins, the seventh bit, a16, is the most significant internal address bit	0b10110[A2][A1][a16] A1/A2 are connected to ground	0b1010000	0x50
GPIO Expander	I2C2	The first 6 bits of the target address are set to 010000, the next bit is determined by the addr pin of the IO expander	0b010000[ADDR] ADDR pin connected to ground	0b0100000	0x20
BOOTMODE IO Expander	I2C2/ I2C1_TA	The first 6 bits of the target address are set to 010000, the next bit is determined by the addr pin of the IO expander	0b010000[ADDR] ADDR pin connected to 3.3V IO supply	0b0100001	0x21
Current Monitor	I2C2	The first three bits of the target address are 100, the following four bits are determined by what is hooked up to A1 and A0	Refer to Address pin table from *Device-Specific Datasheet*.	0b1000000	0x40
Current Monitor	I2C2	The first three bits of the target address are 100, the following four bits are determined by what is hooked up to A1 and A0	Refer to Address pin table from *Device-Specific Datasheet*.	0b1000001	0x41
Temperature Sensor	I2C2	Fixed value of 1001100 for part number TMP411Ax	N/A	0b1001100	0x4C
LED Driver	I2C2	The first four bits of the target address are 1100, the following three are determined by A2, A1, and A0	0b1100[A2][A1][A0] A2/A1/A0 all connected to ground	0b1100000	0x60

Note

Underlined address bits are fixed based on the device addressing and cannot be configured.

4.8 Industrial Application LEDs

The AM263x Control Card has an LED driver (TPIC2810D) that is used for Industrial Communication LEDs. The driver is connected to eight green LEDs and it has an I2C address of 0x60.

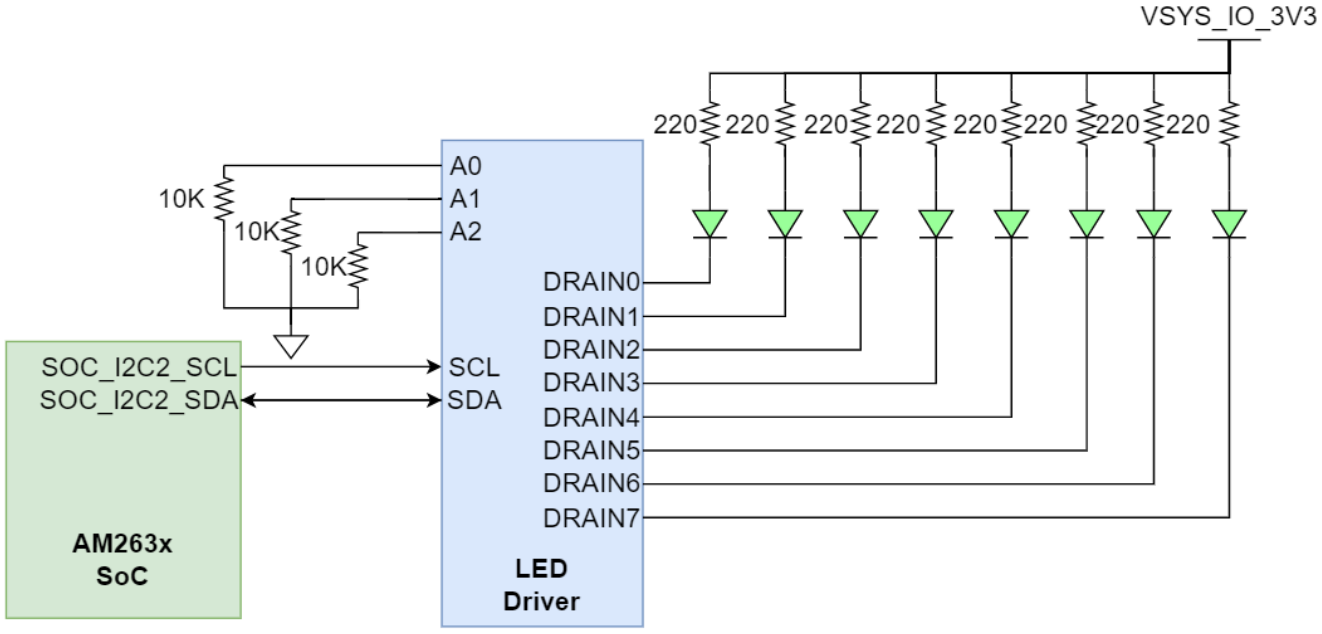

Figure 4-15. Industrial Application LED Driver

4.9 SPI

The AM263x Control Card maps two SPI instances (SPI0,SPI1) from the AM263x SoC to the HSEC 180 pin connector. Series termination resistors are placed near the SoC for each SPI clock signal.

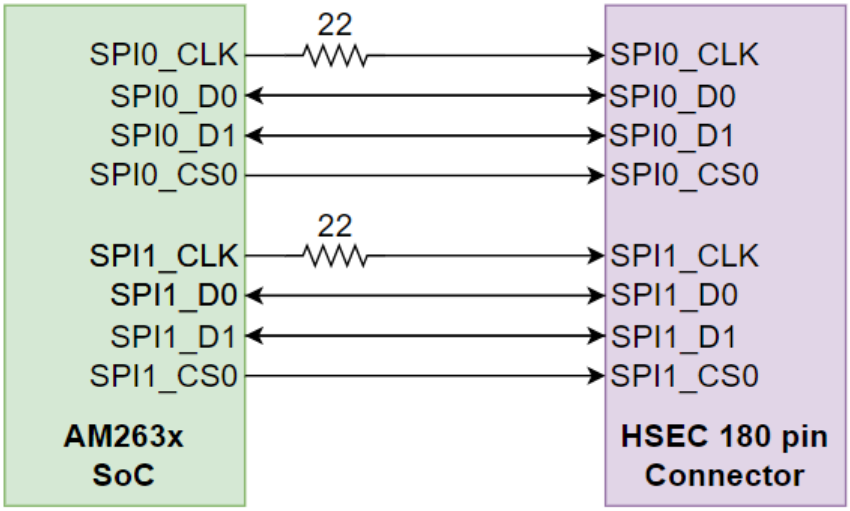

Figure 4-16. SPI

4.10 UART

The AM263x Control Card uses the XDS110 as a USB2.0 to UART bridge for terminal access. UART0 transmit and receive signals of the AM263x SoC are mapped to the XDS110 with a dual channel isolation buffer (ISO7221CDR) for translating from the 3.3 V IO voltage supply to the 3.3 V XDS supply. The XDS110 is connected to a micro-B USB connector for the USB 2.0 signals. ESD protection is provided to the USB 2.0 signals by a transient voltage suppression device (TPD4E004DRYR). The micro-B USB connector's VBUS 5 V power is mapped to a low dropout regulator (TPS79601DRBR) to generate the 3.3 V XDS supply. A separate 3.3V supply for the XDS110 allows for the emulator to maintain a connection when power to the Control Card is removed.

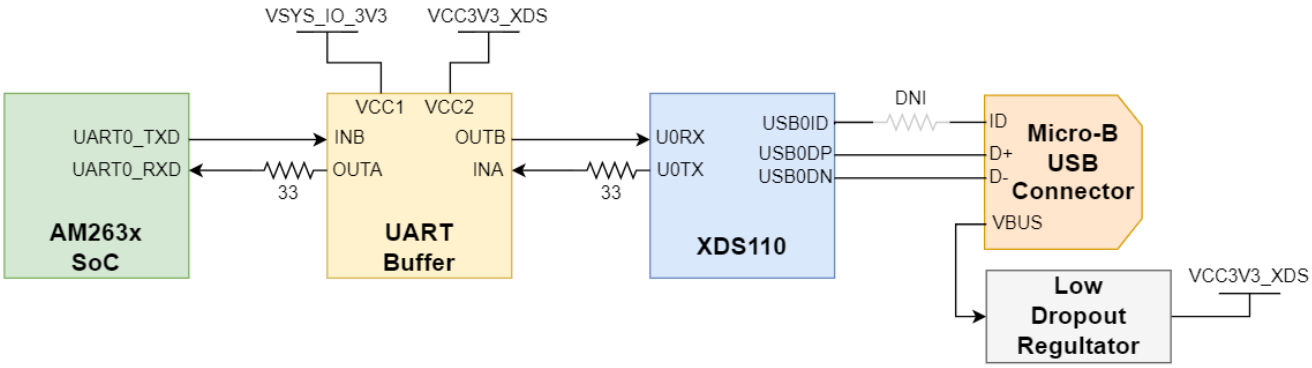

Figure 4-17. UART-USB Bridge for Emulation

The Control Card supports an additional UART1 instance that has the transmit and receive signals mapped from the AM263x SoC to the HSEC connector. To make use of UART1, the select line of a 1:2 mux must be high. The select line is driven by a GPIO signal (LIN_MUX_SEL) that is sourced from the IO expander.

Table 4-13. UART Mux Select Logic

Select	Condition	Function
LOW	LIN Selected	A→B1
HIGH	HSEC UART Selected	A→B2

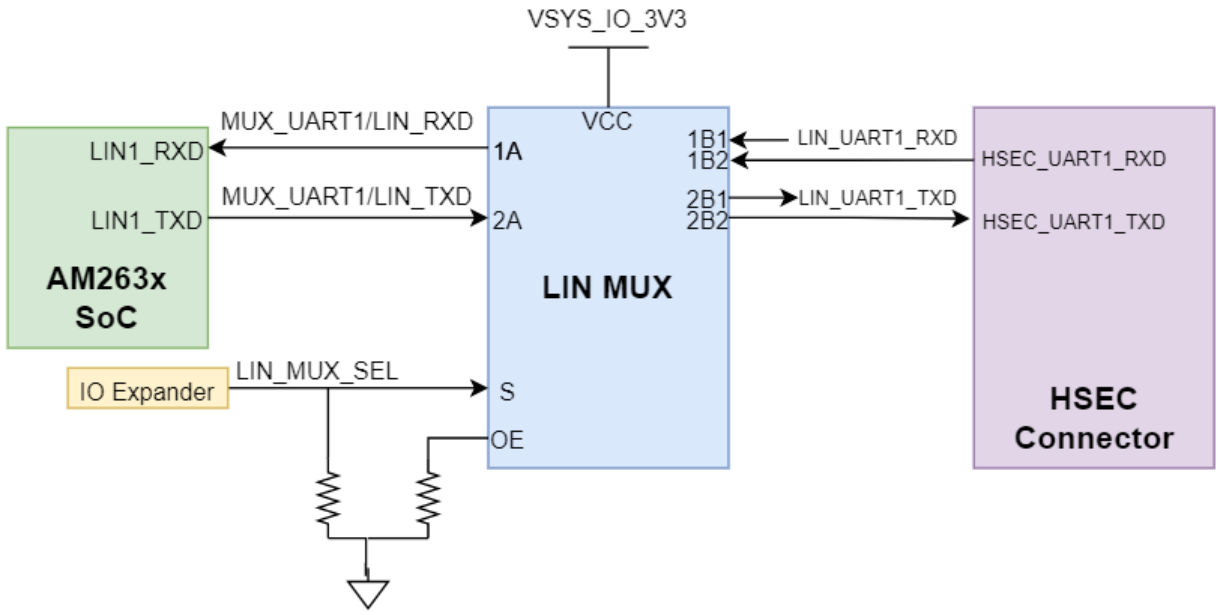

Figure 4-18. UART 1:2 MUX to HSEC

4.11 MCAN

The Control Card is equipped with a single MCAN transceiver (TCAN1024H-Q1) that is connected to the MCAN1 interface of the AM263x SoC. The MCAN0 interface of the AM263x SoC is mapped directly to the HSEC connector.

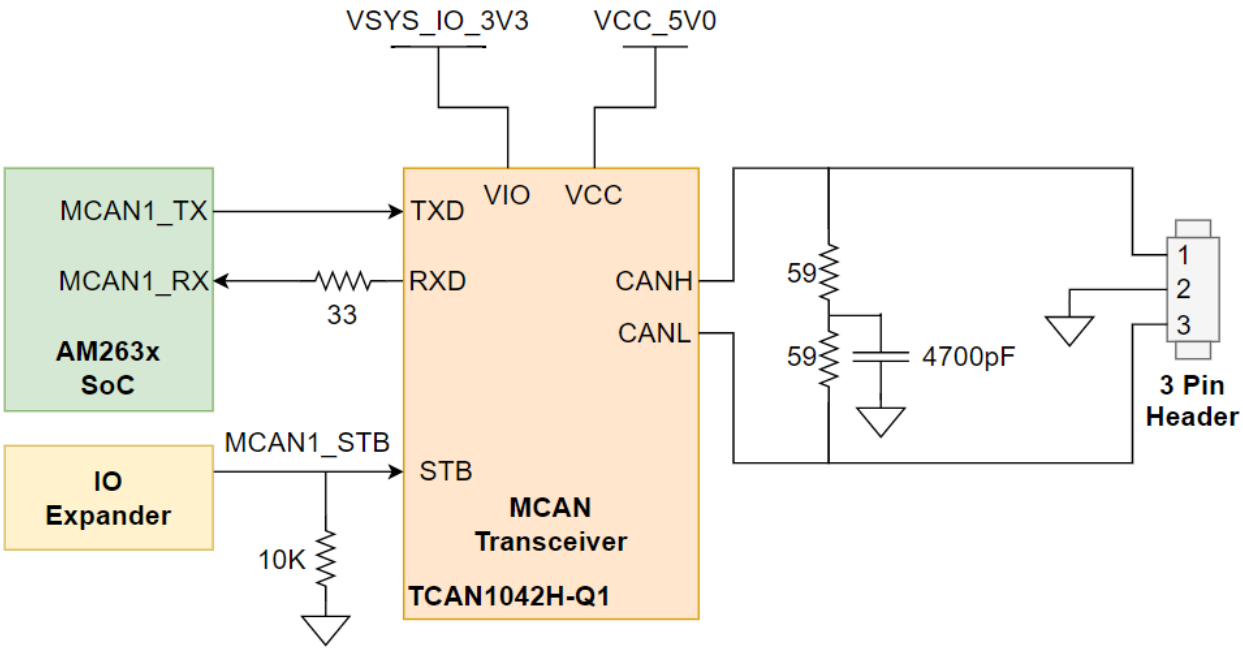

Figure 4-19. MCAN Transceiver

The MCAN transceiver has two power inputs, VIO is the transceiver I/O level shifting supply voltage and VCC is the transceiver 5 V supply voltage. The SoC CAN data transmit data input is mapped to TXD of the transceiver and the CAN receive data output of the transceiver is mapped to the MCAN RX signal of the SoC with a series termination resistor close to the transceiver.

The standby control signal is a GPIO signal sourced from the IO expander. The STB control input is active high and a pulldown resistor is used to have the transceiver operate in normal mode as opposed to the standby mode that is default due to a weak internal pull up.

The system has a 120 Ω split termination on the CANH and CANL signals to improve EMI performance. Split termination improves the electromagnetic emissions behavior of the network by eliminating fluctuations in the bus common-mode voltages at the start and end of message transmissions.

The low- and high-level CAN bus input output lines are terminated to a three pin header.

4.12 FSI

The AM263x Control Card supports a fast serial interface by terminating the SoC signals to a 10 pin header. The interface has two lines of data and a clock line for both the receive and transmit signals. The header is connected to the 3.3 V IO voltage supply.

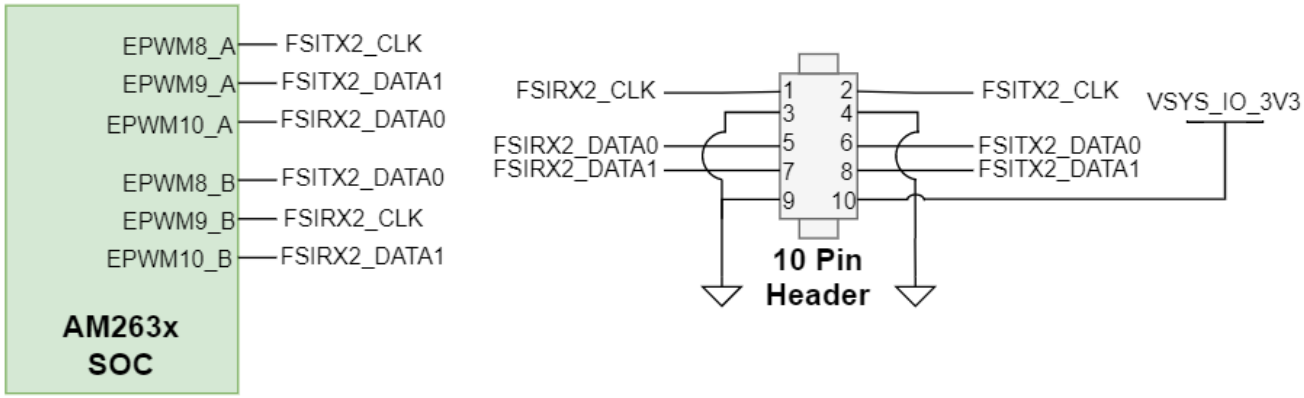

Figure 4-20. FSI Header

4.13 JTAG

The AM263x Control Card includes an XDS110 class on-board emulator. The control card also has the option to map the JTAG signals from the AM263x SoC to the HSEC connector.

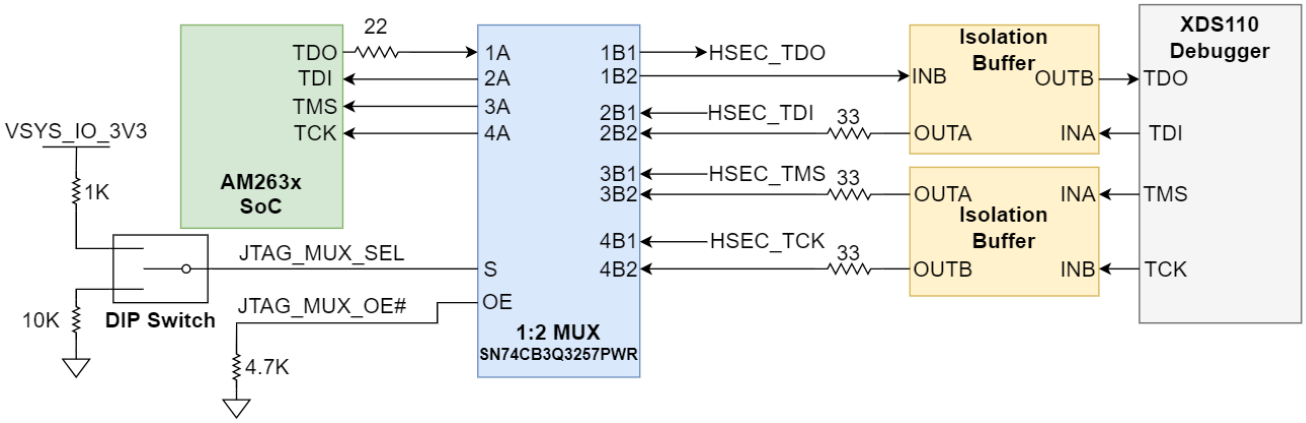

Figure 4-21. JTAG

A DIP switch is used to drive the select line of a 1:2 mux (SN74CB3Q3257PWR) that determines the pathing of the AM263x SoC JTAG signals.

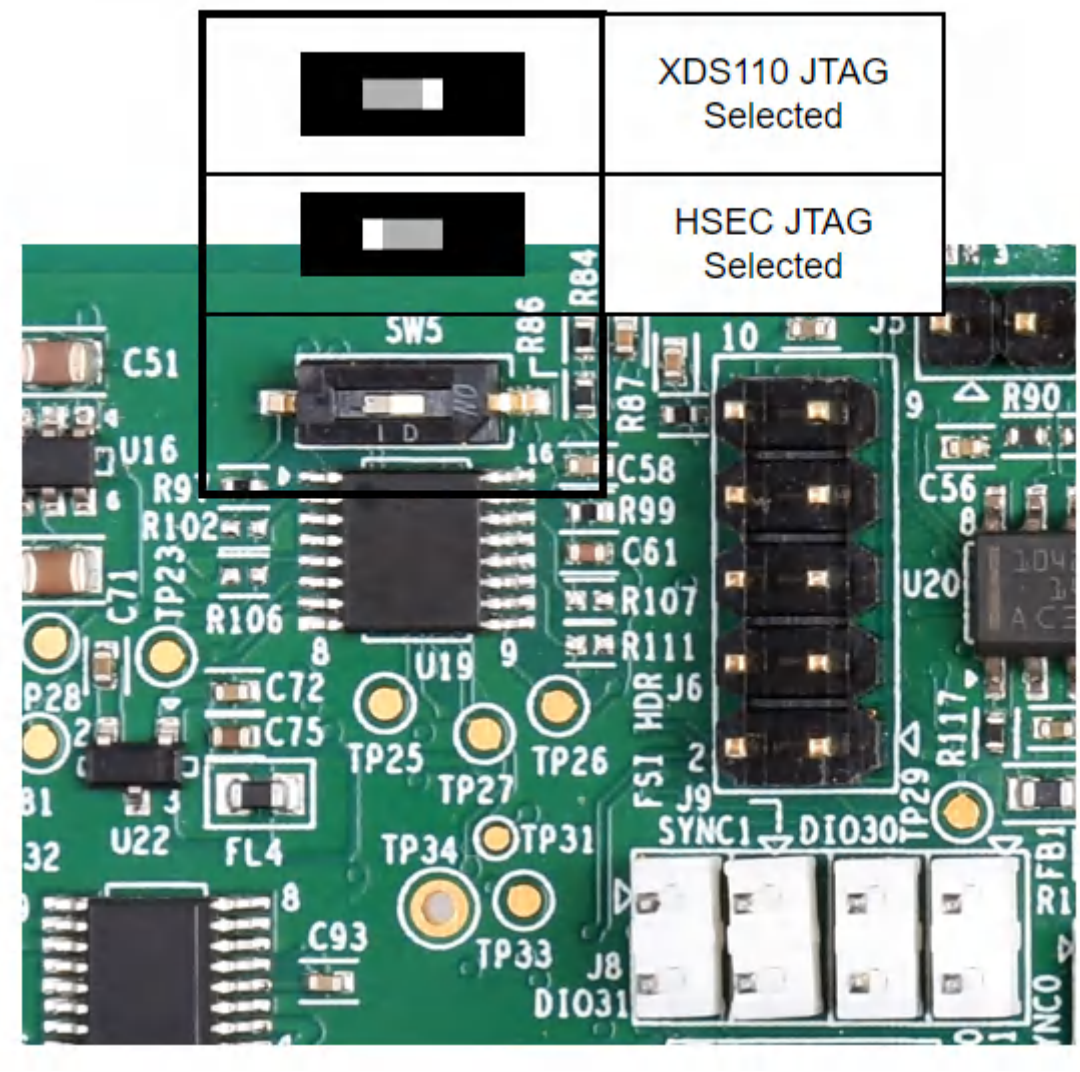

Figure 4-22. JTAG Path Switch

The Control Card includes all circuitry needed for XDS110 emulation. The emulator uses a USB 2.0 micro-B connector to interface the USB 2.0 signals that are created from the UART-USB bridge. The VBUS power from the connector is used to power the emulation circuit so that the connection to the emulator is not lost when power to the Control Card is removed.

The XDS110 controls two power status LED's. For more information refer to Power Status LED's.

4.14 Test Automation Header

The AM263x Control Card supports a 40 pin test automation header that allows an external controller to manipulate basic operations such as power down, PORz, warm reset, and bootmode control.

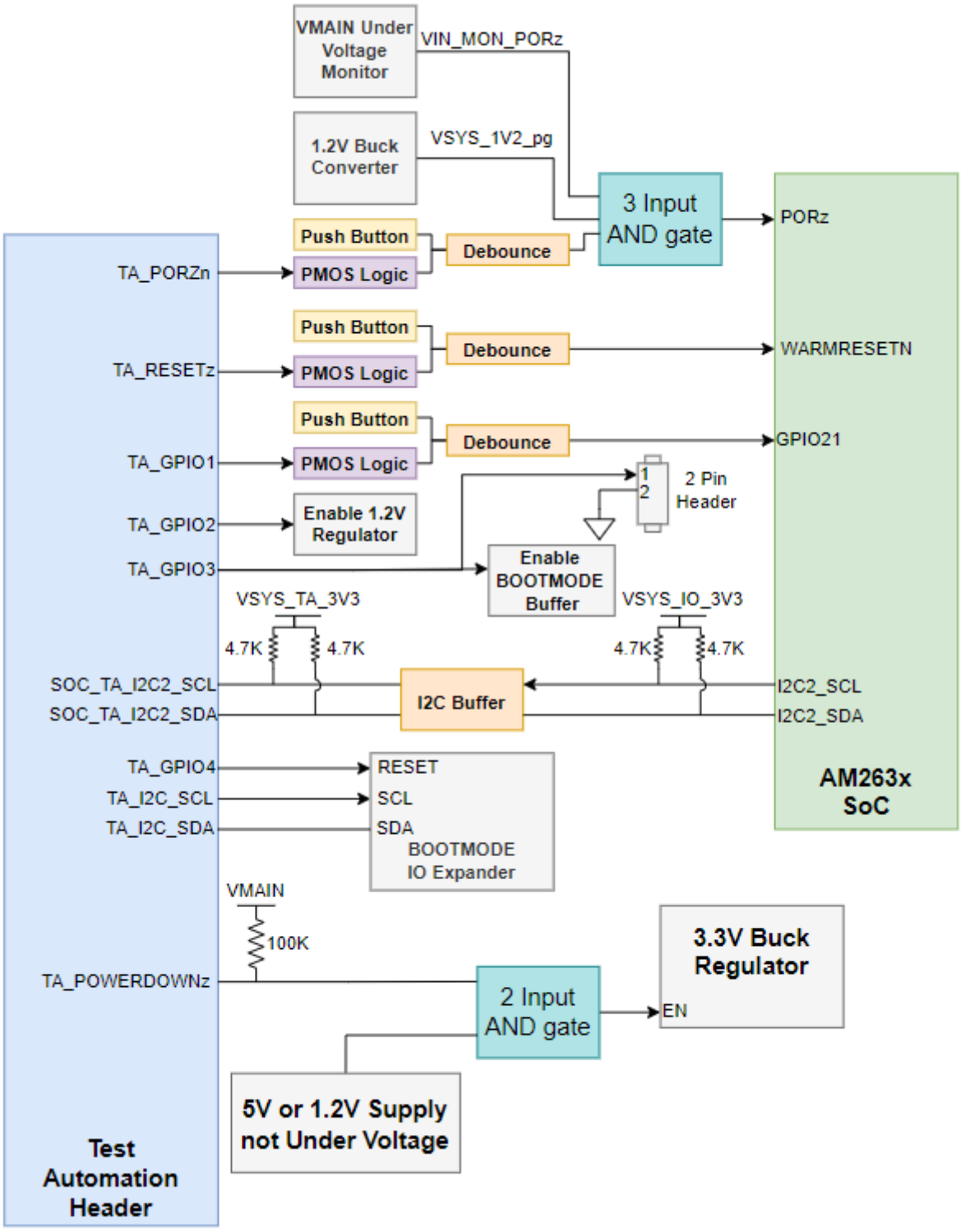

Figure 4-23. Test Automation Header

The Test Automation Circuit is powered by a dedicated 3.3 V power supply (VSYS_TA_3V3) that is generated by a 5 V to 3.3 V buck regulator (TPS62177DQCR).

The AM263x SoC I2C2 instance is connected to both the Test Automation Header and the bootmode IO expander (TCA6408ARGTR).

Table 4-14 details the Test Automation GPIO mapping:

Table 4-14. Test Automation Header GPIO Mapping

Signal Name	Description	Direction
TA_POWERDOWN	When logic low, disables the 3.3 V buck regulator (TPS62913RPUR) that is used in the first stage of DC/DC conversion	Output
TA_PORZn	When logic low, connects the PORz signal to ground due to the PMOS V_GS being less than zero creating a power on reset to the MAIN domain	Output
TA_RESETz	When logic low, connects the WARMRESETn signal to ground due to the PMOS V_GS being less than zero creating a warm reset to the MAIN domain	Output
TA_GPIO1	When logic low, connects the INTn signal to ground due to the PMOS V_GS being less than zero creating an interrupt to the SoC	Output
TA_GPIO2	When logic low, disables the 1.2 V buck regulator (TPS62913RPUR)	Output
TA_GPIO3	When logic low, disables the bootmode buffer output enable	Output
TA_GPIO4	Reset signal for Bootmode IO Expander (TCA6408ARGTR)	Output

4.15 LIN

The AM263x Control Card supports Local Interconnect Network communication through the use of a LIN transceiver (TLIN2029-Q1) that outputs the LIN Bus to the second pin of a 3 pin header.

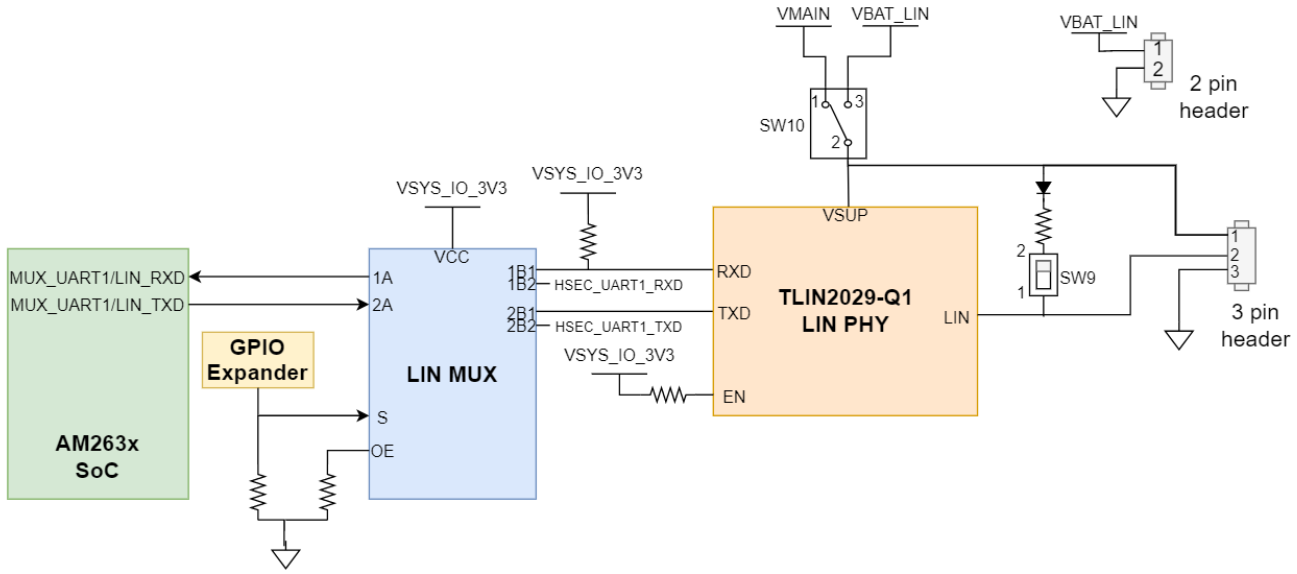

Figure 4-24. LIN PHY

The LIN transmit and receive signals are internally muxed on the AM263x with the UART1 transmit and receive signals. Because of the internal muxing, there is an external 1:2 mux (SN74CB3Q3257PWR) which has a select line that is driven by the GPIO Expander.

Table 4-15. LIN MUX Select Logic

Select Logic	Condition	Function
LOW	LIN Selected	A→B1
HIGH	HSEC UART Selected	A→B2

The AM263x SoC does not have an integrated pull up for the LIN RX signal, therefore, an external pull up resistor is needed to the processor I/O supply voltage is required.

The AM263x Control Card includes a double pole single throw switch (SW10) to control the voltage supply for the LIN Transceiver.

Table 4-16. LIN Switch Logic

LIN Voltage Switch Position	Voltage Supply Selected
Pin 1-2	VMAIN, 5 V supply output from either the USB-C connection or HSEC power connection.
Pin 2-3	VBAT_LIN, external voltage supply from pin 1 of 2 pin header

There is also a single pole throw switch (SW9) that drives the LIN Node application.

Table 4-17. LIN Node Application Switch

LIN Node Application Switch Position	LIN Node Application
Pin 1	Device node application
Pin 2	Controller node application

The Control Card pulls up the enable pin of the LIN transceiver for the transceiver to be in normal operational mode when the I/O Voltage supply is brought up.

4.16 MMC

The AM263x Control Card provides a micro SD card interface that is mapped to the MMC0 instance of the AM263x SoC.

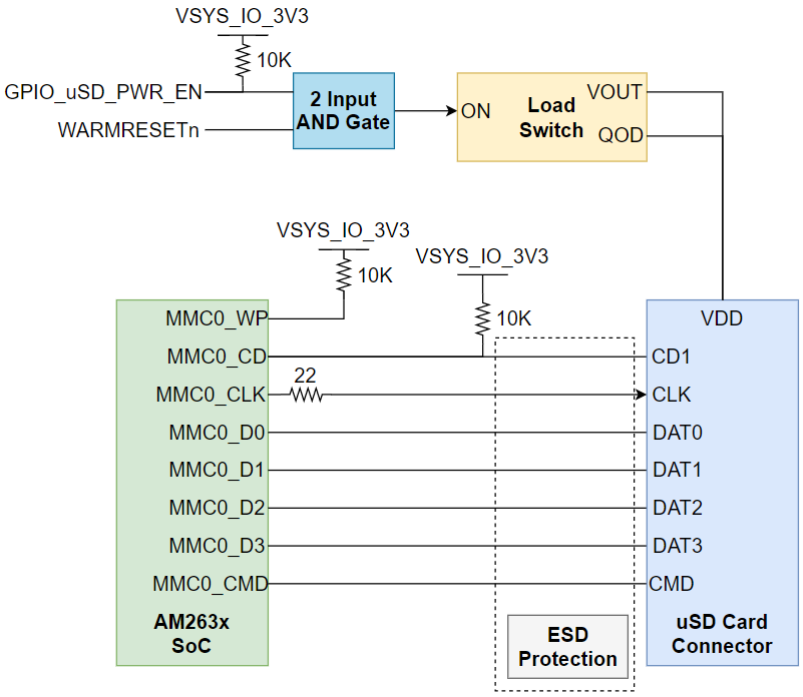

Figure 4-25. Micro-SD Connector Interface

A load switch (TPS22918DBVR) is used to power the micro SD card connector. The load switch is driven by the output of a 2-input AND gate between WARMRESETn and GPIO_uSD_PWR_EN to power cycle the card upon reset. The load switch uses quick output discharge (QOD) to ensure that the supply voltage reaches <10% of nominal value during reset.

Inline ESD protection is provided for the MMC signals in the form of a six channel transient voltage suppressor device (TPD6E001RSER).

The Write Protect (WP) and Card Detect (CD) signals of the SD card connector are pulled up to the 3.3 V IO voltage supply.

A series termination resistor is provided for the MMC clock signal.

4.17 ADC and DAC

The AM263x Control Card supports 24 ADC signal channels that are mapped for the AM263x SoC and terminated to the HSEC connector. All ADC signals are ESD protected (TPD4E001DBVR).

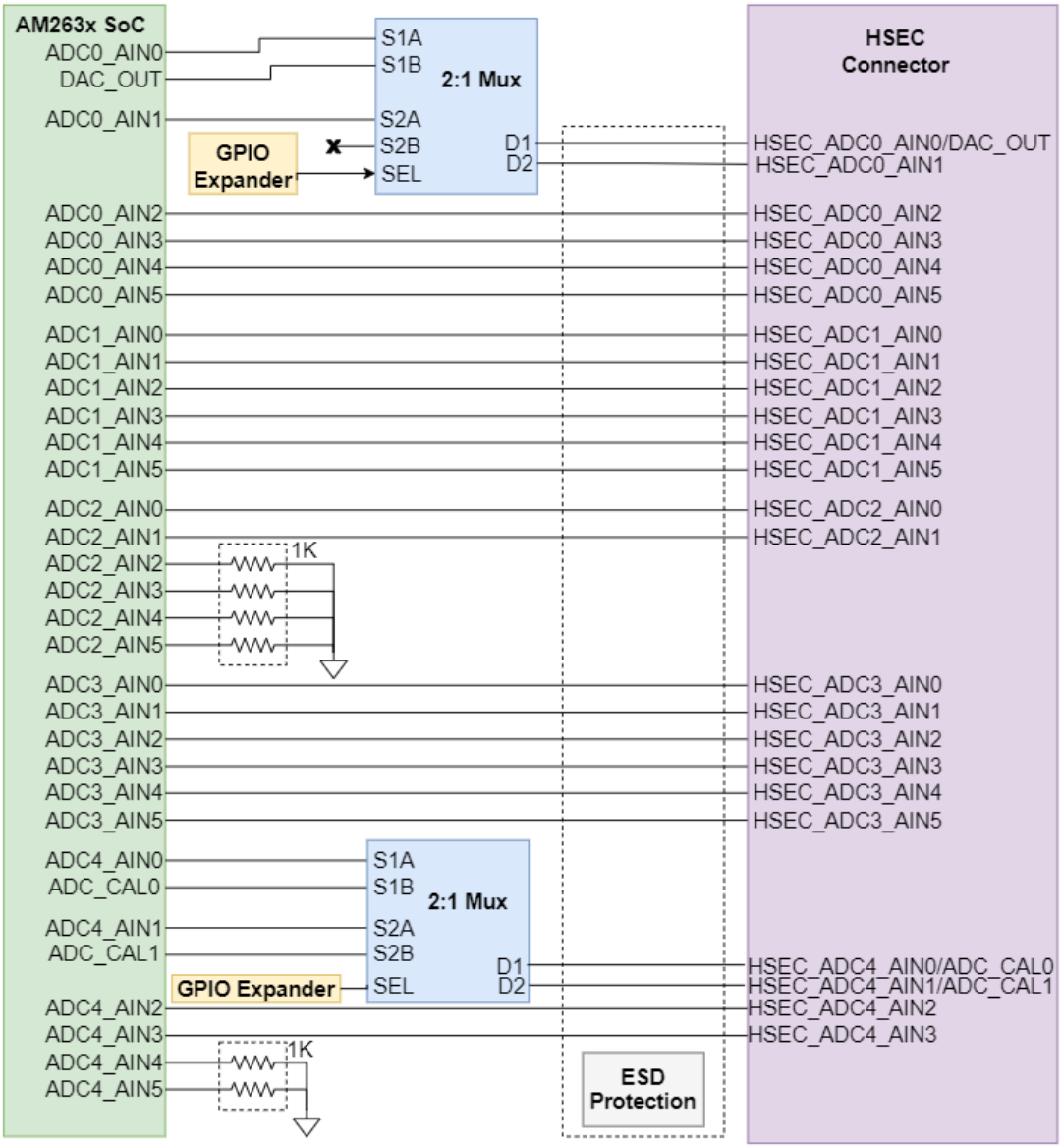

Figure 4-26. ADC HSEC Connections

There are two muxes (TMUX1136DQAR) that determine the pathing of ADC signals to and from the HSEC Connector.

Table 4-18. ADC MUX Select Logic

MUX Select Signal	Condition	Function	Description
ADC1_MUX_SEL	SEL Signal HIGH	S1A → D1	HSEC_ADC0_AIN0 selected
		S2A → D2	HSEC_ADC0_AIN1 selected
	SEL Signal LOW	S1B → D1	HSEC_DAC_OUT selected
		S2B → D2	HSEC_DAC_OUT selected
ADC2_MUX_SEL	SEL Signal HIGH	S1A → D1	HSEC_ADC4_AIN0 selected
		S2A → D2	HSEC_ADC4_AIN1 selected
	SEL Signal LOW	S1B → D1	ADC_CAL0 selected
		S2B → D2	ADC_CAL1 selected

There are three switches that are used to configure the reference voltages for the ADC and DAC.

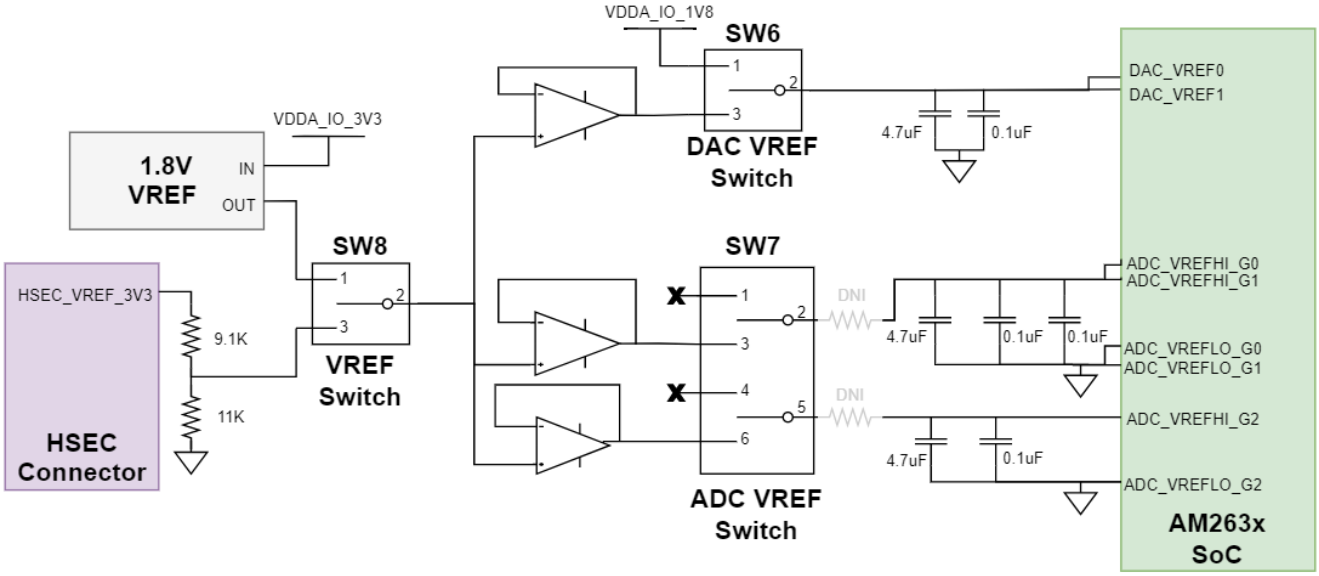

Figure 4-27. ADC Switch Routing

- The VREF Switch (SW8) is a single pole double throw switch that controls which 1.8 V reference will be used for ADC and DAC.

Table 4-19. VREF Switch

VREF Switch Position	Reference Selection
Pin 1-2	On board 1.8 V Reference (REF3318AIDBZT)
Pin 2-3	HSEC VREF

- The DAC VREF Switch (SW6) is a single pole double throw switch that controls the input for the DAC VREF inputs of the AM263x SoC.

Table 4-20. DAC VREF Switch

DAC VREF Switch Position	Reference Selection
Pin 1-2	AM263x on-die LDO
Pin 2-3	Output of VREF Switch

- The ADC VREF Switch (SW7) contains two single pole double throw switches that control the input for the ADC VREF inputs of the AM263x SoC.

Table 4-21. ADC VREF Switch

ADC VREF Switch Position	Reference Selection
Pin 1-2	OPEN - Allow for reference to be AM263x on-die LDO reference
Pin 2-3	Output of VREF Switch
Pin 4-5	OPEN - Allow for reference to be AM263x on-die LDO reference
Pin 5-6	Output of VREF Switch

4.18 HSEC Pinout and Pinmux Mapping

Note

Table 4-22 displays the pinout of the AM263x Control Card HSEC and all PinMux options for **E2 and beyond**. If you are using an E1 Control Card, see Appendix B.

Table 4-22. HSEC Pinout

Pin#	Package Signal Name	Muxed Signal Options		Muxed Signal Options	Signal Package Name	Pin#
1	NC	NC		NC	NC	2
3	HSEC_TMS	TMS		NC	NC	4
5	HSEC_TCK	TCK		TDO	HSEC_TDO	6
7	GND	GND		TDI	HSEC_TDI	8
9	HSEC_ADC0_AIN4/DAC_OUT	HSEC_ADC0_AIN0/DAC_OUT		GND	GND	10
11	HSEC_ADC0_AIN5/DAC_OUT	HSEC_ADC0_AIN1/DAC_OUT		ADC1_AIN0	ADC1_AIN0	12
13	GND	GND		ADC1_AIN1	ADC1_AIN1	14
15	ADC0_AIN2	ADC0_AIN2		GND	GND	16
17	ADC0_AIN3	ADC0_AIN3		ADC1_AIN2	ADC1_AIN2	18
19	GND	GND		ADC1_AIN3	ADC1_AIN3	20
21	ADC0_AIN4	ADC0_AIN4		GND	GND	22
23	ADC0_AIN5	ADC0_AIN5		ADC1_AIN4	ADC1_AIN4	24
25	ADC4_AIN0/ADC_CAL0	ADC4_AIN0/ADC_CAL0		ADC1_AIN5	ADC1_AIN5	26
27	ADC4_AIN1/ADC_CAL1	ADC4_AIN1/ADC_CAL1		ADC3_AIN0	ADC3_AIN0	28
29	GND	GND		ADC3_AIN1	ADC3_AIN1	30
31	ADC2_AIN0	ADC2_AIN0		GND	GND	32
33	ADC2_AIN1	ADC2_AIN1		ADC3_AIN2	ADC3_AIN2	34
35	GND	GND		ADC3_AIN3	ADC3_AIN3	36
37	ADC2_AIN2	ADC2_AIN2		GND	GND	38
39	ADC2_AIN3	ADC2_AIN3		ADC3_AIN4	ADC3_AIN4	40
41	NC	NC		ADC3_AIN5	ADC3_AIN5	42
43	NC	NC		NC	NC	44
45	HSEC_ADC-VREFHI	HSEC_ADC-VREFHI		GND	GND	46
47	GND	GND		HSEC_5V0	HSEC_5V0	48
49	EPWM0_A	EPWM0_A/GPIO43		EPWM2_A/GPIO47	EPWM2_A	50
51	EPWM0_B	EPWM0_B/GPIO44		EPWM2_B/GPIO48	EPWM2_B	52
53	EPWM1_A	EPWM1_A/GPIO45		EPWM3_A/GPIO49	EPWM3_A	54
55	EPWM1_B	EPWM1_B/GPIO46		EPWM3_B/GPIO50	EPWM3_B	56
57	EPWM4_A	EPWM4_A/GPIO51		EPWM6_A/FSIRX1_CLK/GPIO55	EPWM6_A	58
59	EPWM4_B	EPWM4_B/FSITX1_CLK/GPIO52		EPWM6_B/FSIRX1_DATA0/GPIO56	EPWM6_B	60
61	EPWM5_A	EPWM5_A/FSITX1_DATA0/GPIO53		EPWM7_A/FSIRX1_DATA1/GPIO57	EPWM7_A	62
63	EPWM5_B	EPWM5_B/FSITX1_DATA1/GPIO54		EPWM7_B/GPIO58	EPWM7_B	64
65	GND	GND		NC	NC	66
67	SPI0_D0	SPI0_D0/FSITX0_DATA0/GPIO13/SOP3		PR0_PRU1_GPO19/UART3_RXD/ PR0_IEP0_EDC_SYNC_OUT0/TRC_CLK/ XBAROUT13/GPIO119/EQEP1_A	EQEP1_A	68

Table 4-22. HSEC Pinout (continued)

Pin#	Package Signal Name	Muxed Signal Options		Muxed Signal Options	Signal Package Name	Pin#
69	SPI0_D1	SPI0_D1/FSITX0_DATA1/GPIO14		PR0_PRU1_GPO18/UART3_TXD/ PR0_IEP0_EDIO_DATA_IN_OUT31/ TRC_CTL/XBAROUT14/GPMC0_WAIT1/ GPIO120/EQEP1_B	EQEP1_B	70
71	SPI0_CLK	SPI0_CLK/UART3_TXD/LIN3_TXD/ FSITX0_CLK/GPIO12/SOP2		SDFM0_CLK0/CLKOUT1/GPIO122/ EQEP1_STROBE	EQEP1_STROBE	72
73	SPI0_CS0	SPI0_CS0/UART3_RXD/LIN3_RXD/GPIO11		EXT_REFCLK0/XBAROUT15/GPIO121/ EQEP1_INDEX	EQEP1_INDEX	74
75	SPI1_D0	SPI1_D0/UART5_TXD/XBAROUT3/ FSIRX0_DATA0/GPIO17		LIN1_RXD/UART1_RXD/SPI2_CS0/ XBAROUT5/GPIO19	UART1_RXD	76
77	SPI1_D1	SPI1_D1/UART5_RXD/XBAROUT4/ FSIRX0_DATA1/GPIO18		LIN1_TXD/UART1_TXD/SPI2_CLK/ XBAROUT6/GPIO20	UART1_TXD	78
79	SPI1_CLK	SPI1_CLK/UART4_RXD/LIN4_RXD/ XBAROUT2/FSIRX0_CLK/GPIO16		MCAN0_RX/SPI4_CS0/GPIO7	MCAN0_RX	80
81	SPI1_CS0	SPI1_CS0/UART4_TXD/LIN4_TXD/ XBAROUT1/GPIO15		MCAN0_TX/SPI4_CLK/GPIO8	MCAN0_TX	82
83	GND	GND		HSEC_5V0	HSEC_5V0	84
85	I2C1_SDA	I2C1_SDA/SPI3_CLK/XBAROUT8/GPIO24		EPWM11_A/UART2_CTSn/GPMC0_CLKLB/ GPIO65	GPMC0_CLKB	86
87	I2C1_SCL	I2C1_SCL/SPI3_CS0/XBAROUT7/GPIO23		NC	NC	88
89	EPWM21_A	PR0_MDIO0_MDIO/EPWM21_A/ GPMC0_CSn2/GPIO85		PR0_MDIO0_MDC/EPWM21_B/ GPMC0_CSn3/GPIO86	EPWM21_B	90
91	SDFM0_D0	SDFM0_D0/PR0_ECAP0_APWM_OUT/ GPIO123		I2C0_SDA/GPIO134/EQEP2_A/ SDFM1_CLK2	EQEP2_A	92
93	EQEP2_B	I2C0_SCL/GPIO135/EQEP2_B/ SDFM1_CLK3		MCAN2_RX/UART2_RTSn/GPIO137/ EQEP2_INDEX/SDFM1_D3	EQEP2_INDEX	94
95	EQEP2_STROBE	MCAN2_TX/UART1_RTSn/GPIO136/ EQEP2_STROBE/SDFM1_D2		NC	NC	96
97	GND	GND		HSEC_5V0	HSEC_5V0	98
99	SDFM0_D1	SDFM0_D1/PR0_PRU1_GPIO17/ UART5_CTSn/ PR0_IEP0_EDIO_DATA_IN_OUT30/GPIO125		EQEP0_A/UART4_RTSn/SPI4_CLK/ GPIO130/SDFM1_CLK0	EQEP0_B	100
101	SDFM0_CLK1	SDFM0_CLK1/PR0_PRU1_GPIO7/ CPTS0_TS_SYNC/UART5_RTSn/ PR0_IEP0_EDC_SYNC_OUT1/I2C3_SDA/ GPIO124		EQEP0_B/UART4_CTSn/SPI4_CS0/ GPIO131/SDFM1_D0	EQEP0_A	102
103	SDFM0_D2	SDFM0_D2/UART5_RXD/GPIO127		EQEP0_STROBE/UART4_TXD/LIN4_TXD/ SPI4_D0/GPIO132/SDFM1_CLK1	EQEP0_STROBE	104
105	SDFM0_CLK2	SDFM0_CLK2/UART5_TXD/I2C3_SCL/ GPMC0_ADVn_ALE/GPIO126/SDFM0_CLK2		EQEP0_INDEX/UART4_RXD/LIN4_RXD/ SPI4_D1/GPIO133/SDFM1_D1	EQEP0_INDEX	106
107	SDFM0_D3	SDFM0_D3/MCAN3_RX/GPIO129		PR0_PRU0_GPO5/RMII2_RX_ER/ MII2_RX_ER/EPWM22_A/GPMC0_DIR/ GPIO87	MII0_RXER	108
109	SDFM0_CLK3	SDFM0_CLK3/MCAN3_TX/UART5_RXD/ GPIO128		PR0_PRU0_GPO9/PR0_UART0_CTSn/ MII2_COL/EPWM22_B/GPMC0_CLK/GPIO88	MII0_CO	110
111	GND	GND		HSEC_5V0	HSEC_5V0	112
113	NC	NC		NC	NC	114
115	NC	NC		NC	NC	116
117	NC	NC		HSEC_5V0	HSEC_5V0	118
119	NC	NC		PORz	PORz	120

Table 4-22. HSEC Pinout (continued)

Pin#	Package Signal Name	Muxed Signal Options		Muxed Signal Options	Signal Package Name	Pin#
121	ICSS_MII0_CRS	PR0_PRU0_GPO10/RMII2_CRS_DV/ PR0_UART0_RTSn/MII2_CRS/EPWM23_A/ GPMC0_WAIT0/GPIO89		PR0_PRU0_GPO8/EPWM23_B/ GPMC0_WPn/GPIO90	ICSS_MII0_RXLINK	122
123	ICSS_MII0_RXCLK	PR0_PRU0_GPO6/RMII2_REF_CLK/ RGMII2_RXC/MII2_RXCLK/EPWM24_A/ GPMC0_CSn1/GPIO91		PR0_PRU0_GPO4/RGMII2_RX_CTL/ MII2_RXDV/EPWM24_B/GPMC0_A0/GPIO92	ICSS_MII0_RXDV	124
125	ICSS_MII0_RXD0	PR0_PRU0_GPO0/RMII2_RXD0/ RGMII2_RD0/MII2_RXD0/EPWM25_A/ GPMC0_A1/GPIO93		PR0_PRU0_GPO1/RMII2_RXD1/ RGMII2_RD1/MII2_RXD1/EPWM25_B/ GPMC0_A2/GPIO94	ICSS_MII0_RXD1	126
127	ICSS_MII0_RXD2	PR0_PRU0_GPO2/RGMII2_RD2/MII2_RXD2/ EPWM26_A/GPMC0_A3/GPIO95		PR0_PRU0_GPO3/RGMII2_RD3/MII2_RXD3/ EPWM26_B/GPMC0_A4/GPIO96	ICSS_MII0_RXD3	128
129	ICSS_MII0_TXCLK	PR0_PRU0_GPO16/RGMII2_TXC/ MII2_TXCLK/EPWM27_A/GPMC0_A5/ GPIO97		PR0_PRU0_GPO15/RMII2_TX_EN/ RGMII2_TX_CTL/MII2_TX_EN/EPWM27_B/ GPMC0_A6/GPIO98	ICSS_MII0_TXEN	130
131	ICSS_MII0_TXD0	PR0_PRU0_GPO11/RMII2_TXD0/ RGMII2_TD0/MII2_TXD0/EPWM28_A/ GPMC0_A7/GPIO99		PR0_PRU0_GPO12/RMII2_TXD1/ RGMII2_TD1/MII2_TXD1/EPWM28_B/ GPMC0_A8/GPIO100	ICSS_MII0_TXD1	132
133	ICSS_MII0_TXD2	PR0_PRU0_GPO14/RGMII2_TD3/ MII2_TXD3/EPWM29_B/GPMC0_A10/ GPIO102		PR0_PRU0_GPO14/RGMII2_TD3/ MII2_TXD3/EPWM29_B/GPMC0_A10/ GPIO102	ICSS_MII0_TXD3	134
135	GND	GND		NC	NC	136
137	ICSS_MII1_RXER	PR0_PRU1_GPO5/TRC_DATA0/EPWM30_A/ GPMC0_OEn_REn/GPIO103		PR0_PRU1_GPO9/PR0_UART0_RXD/ TRC_DATA1/EPWM30_B/ GPMC0_BE0n_CLE/GPIO104	ICSS_MII1_COL	138
139	ICSS_MII1_CRS	PR0_PRU1_GPO10/PR0_UART0_TXD/ TRC_DATA2/EPWM31_A/GPMC0_BE1n/ GPIO105		PR0_PRU1_GPO8/TRC_DATA3/EPWM31_B/ GPMC0_WEn/GPIO106	ICSS_MII1_RXLINK	140
141	ICSS_MII1_RXCLK	PR0_PRU1_GPO6/FSITX2_CLK/ TRC_DATA4/GPMC0_A11/GPIO107		PR0_PRU1_GPO4/FSITX2_DATA0/ TRC_DATA5/GPMC0_A12/GPIO108	ICSS_MII1_RXDV	142
143	ICSS_MII1_RXD0	PR0_PRU1_GPO0/FSITX2_DATA1/ TRC_DATA6/GPMC0_A13/GPIO109		PR0_PRU1_GPO1/FSIRX2_CLK/ TRC_DATA7/GPMC0_A14/GPIO110	ICSS_MII1_RXD1	144
145	ICSS_MII1_RXD2	PR0_PRU1_GPO2/FSIRX2_DATA0/ TRC_DATA8/GPMC0_A15/GPIO111		PR0_PRU1_GPO3/FSIRX2_DATA1/ TRC_DATA9/GPMC0_A16/GPIO112	ICSS_MII1_RXD3	146
147	ICSS_MII1_TXCLK	PR0_PRU1_GPO16/FSITX3_CLK/ TRC_DATA10/GPMC0_A17/GPIO113		PR0_PRU1_GPO15/FSITX3_DATA0/ TRC_DATA11/GPMC0_A18/GPIO114	ICSS_MII1_TXEN	148
149	ICSS_MII1_TXD0	PR0_PRU1_GPO11/FSITX3_DATA1/ TRC_DATA12/GPMC0_A19/GPIO115		PR0_PRU1_GPO12/FSIRX3_CLK/ TRC_DATA13/GPMC0_A20/GPIO116	ICSS_MII1_TXD1	150
151	ICSS_MII1_TXD2	PR0_PRU1_GPO13/FSIRX3_DATA0/ TRC_DATA14/XBAROUT11/GPMC0_A21/ GPIO117		PR0_PRU1_GPO14/FSIRX3_DATA1/ TRC_DATA15/XBAROUT12/GPMC0_CSn0/ GPIO118	ICSS_MII1_TXD3	152
153	GPMC0_AD0	EPWM13_A/UART1_RIn/GPMC0_AD0/ GPIO69		EPWM13_B/UART1_DTRn/GPMC0_AD1/ GPIO70	GPMC0_AD1	154
155	GPMC0_AD2	EPWM14_A/UART1_DSRn/GPMC0_AD2/ GPIO71		EPWM14_B/MII1_RX_ER/GPMC0_AD3/ GPIO72	GPMC0_AD3	156
157	GND	GND		HSEC_5V0	HSEC_5V0	158
159	GPMC0_AD4	EPWM15_A/UART5_TXD/MII1_COL/ GPMC0_AD4/GPIO73		EPWM15_B/UART5_RXD/MII1_CRS/ GPMC0_AD5/GPIO74	GPMC0_AD5	160
161	GPMC0_AD6	UART1_RXD/LIN1_RXD/EPWM16_A/ GPMC0_AD6/GPIO75		UART1_TXD/LIN1_TXD/EPWM16_B/ GPMC0_AD7/GPIO76	GPMC0_AD7	162
163	GPMC0_AD8	MMC0_CLK/UART0_RXD/LIN0_RXD/ EPWM17_A/GPMC0_AD8/GPIO77/ SDFM1_CLK0		MMC0_CMD/UART0_TXD/LIN0_TXD/ EPWM17_B/GPMC0_AD9/GPIO78/ SDFM1_D0	GPMC0_AD9	164

Table 4-22. HSEC Pinout (continued)

Pin#	Package Signal Name	Muxed Signal Options		Muxed Signal Options	Signal Package Name	Pin#
165	GPMC0_AD10	MMC0_D0/UART2_RXD/I2C1_SCL/ EPWM18_A/GPMC0_AD10/GPIO79/ SDFM1_CLK1		MMC0_D1/EPWM18_B/GPMC0_AD11/ GPIO80/SDFM1_D1	GPMC0_AD11	166
167	GPMC0_AD12	MMC0_D2/UART2_TXD/I2C1_SDA/ EPWM19_A/GPMC0_AD12/GPIO81/ SDFM1_CLK2		MMC0_D3/UART3_RTSn/EPWM19_B/ GPMC0_AD13/GPIO82/SDFM1_D2	GPMC0_AD13	168
169	GPMC0_AD14	MMC0_WP/UART0_RTSn/I2C2_SCL/ EPWM20_A/GPMC0_AD14/GPIO83/ SDFM1_CLK3		MMC0_CD/UART0_CTSn/I2C2_SDA/ EPWM20_B/GPMC0_AD15/GPIO84/ SDFM1_D3	GPMC0_AD15	170
171	NC	NC		NC	NC	172
173	NC	NC		NC	NC	174
175	NC	NC		NC	NC	176
177	NC	NC		NC	NC	178
179	GND	GND		HSEC_5V0	HSEC_5V0	180

Table 4-23. Pinmux Mapping Table

Pin#	Pinlist	Mode0	Mode1	Mode2	Mode3	Mode4	Mode5	Mode6	Mode7	Mode8	Mode9
U16	**ADC_CAL0**	ADC_CAL0									
T15	**ADC_CAL1**	ADC_CAL1									
V14	**ADC_VREFHI_G0**	ADC_VREFHI_G0									
V10	**ADC_VREFHI_G1**	ADC_VREFHI_G1									
V6	**ADC_VREFHI_G2**	ADC_VREFHI_G2									
V13	**ADC_VREFLO_G0**	ADC_ VREFLOSRC0									
V11	**ADC_VREFLO_G1**	ADC_ VREFLO1									
V7	**ADC_VREFLO_G2**	ADC_ VREFLOSRC1									
V15	**ADC0_AIN0**	ADC0_AIN0									
U15	**ADC0_AIN1**	ADC0_AIN1									
T14	**ADC0_AIN2**	ADC0_AIN2									
U14	**ADC0_AIN3**	ADC0_AIN3									
U13	**ADC0_AIN4**	ADC0_AIN4									
R14	**ADC0_AIN5**	ADC0_AIN5									
T11	**ADC1_AIN0**	ADC1_AIN0									
U11	**ADC1_AIN1**	ADC1_AIN1									
T12	**ADC1_AIN2**	ADC1_AIN2									
V12	**ADC1_AIN3**	ADC1_AIN3									
U12	**ADC1_AIN4**	ADC1_AIN4									
R12	**ADC1_AIN5**	ADC1_AIN5									
R10	**ADC2_AIN0**	ADC2_AIN0									
T10	**ADC2_AIN1**	ADC2_AIN1									
U10	**ADC2_AIN2**	ADC2_AIN2									
T9	**ADC2_AIN3**	ADC2_AIN3									
V9	**ADC2_AIN4**	ADC2_AIN4									

Table 4-23. Pinmux Mapping Table (continued)

Pin#	Pinlist	Mode0	Mode1	Mode2	Mode3	Mode4	Mode5	Mode6	Mode7	Mode8	Mode9
T8	**ADC2_AIN5**	ADC2_AIN5									
U7	**ADC3_AIN0**	ADC3_AIN0									
U8	**ADC3_AIN1**	ADC3_AIN1									
T7	**ADC3_AIN2**	ADC3_AIN2									
R7	**ADC3_AIN3**	ADC3_AIN3									
V8	**ADC3_AIN4**	ADC3_AIN4									
U9	**ADC3_AIN5**	ADC3_AIN5									
U6	**ADC4_AIN0**	ADC4_AIN0									
V5	**ADC4_AIN1**	ADC4_AIN1									
V4	**ADC4_AIN2**	ADC4_AIN2									
U5	**ADC4_AIN3**	ADC4_AIN3									
V3	**ADC4_AIN4**	ADC4_AIN4									
U4	**ADC4_AIN5**	ADC4_AIN5									
U3	**ATESTV0**	ATESTV0									
V2	**ATESTV1**	ATESTV1									
M2	**CLKOUT0**	CLKOUT0							GPIO138		
T5	**DAC_OUT**	DAC_OUT									
T13	**DAC_VREF0**	DAC_VREF0									
T6	**DAC_VREF1**	DAC_VREF1									
B2	**EPWM0_A**	EPWM0_A							GPIO43		
B1	**EPWM0_B**	EPWM0_B							GPIO44		
D3	**EPWM1_A**	EPWM1_A							GPIO45		
D2	**EPWM1_B**	EPWM1_B							GPIO46		
G4	**EPWM10_A**	EPWM10_A	UART1_CTSn					FSIRX2_DATA0	GPIO63		
J3	**EPWM10_B**	EPWM10_B	UART2_RTSn					FSIRX2_DATA1	GPIO64		
H1	**EPWM11_A**	EPWM11_A	UART2_CTSn					GPMC0_CLKLB	GPIO65		
J1	**EPWM11_B**	EPWM11_B	UART3_RTSn					GPMC0_OEn_REn	GPIO66		
K2	**EPWM12_A**	EPWM12_A	UART3_CTSn	SPI4_CS1				GPMC0_WEn	GPIO67		
J4	**EPWM12_B**	EPWM12_B	UART1_DCDn					GPMC0_CSn0	GPIO68		
K4	**EPWM13_A**	EPWM13_A	UART1_RIn					GPMC0_AD0	GPIO69		
K3	**EPWM13_B**	EPWM13_B	UART1_DTRn					GPMC0_AD1	GPIO70		
V17	**EPWM14_A**	EPWM14_A	UART1_DSRn					GPMC0_AD2	GPIO71		
T16	**EPWM14_B**	EPWM14_B		MII1_RX_ER				GPMC0_AD3	GPIO72		
P15	**EPWM15_A**	EPWM15_A	UART5_TXD	MII1_COL				GPMC0_AD4	GPIO73		
R16	**EPWM15_B**	EPWM15_B	UART5_RXD	MII1_CRS				GPMC0_AD5	GPIO74		
C2	**EPWM2_A**	EPWM2_A							GPIO47		
C1	**EPWM2_B**	EPWM2_B							GPIO48		
E2	**EPWM3_A**	EPWM3_A							GPIO49		
E3	**EPWM3_B**	EPWM3_B							GPIO50		
D1	**EPWM4_A**	EPWM4_A							GPIO51		
E4	**EPWM4_B**	EPWM4_B						FSITX1_CLK	GPIO52		

Table 4-23. Pinmux Mapping Table (continued)

Pin#	Pinlist	Mode0	Mode1	Mode2	Mode3	Mode4	Mode5	Mode6	Mode7	Mode8	Mode9
F2	**EPWM5_A**	EPWM5_A						FSITX1_DATA0	GPIO53		
G2	**EPWM5_B**	EPWM5_B						FSITX1_DATA1	GPIO54		
E1	**EPWM6_A**	EPWM6_A						FSIRX1_CLK	GPIO55		
F3	**EPWM6_B**	EPWM6_B						FSIRX1_DATA0	GPIO56		
F4	**EPWM7_A**	EPWM7_A						FSIRX1_DATA1	GPIO57		
F1	**EPWM7_B**	EPWM7_B							GPIO58		
G3	**EPWM8_A**	EPWM8_A	UART4_TXD	I2C3_SDA				FSITX2_CLK	GPIO59		
H2	**EPWM8_B**	EPWM8_B	UART4_RXD	I2C3_SCL				FSITX2_DATA0	GPIO60		
G1	**EPWM9_A**	EPWM9_A						FSITX2_DATA1	GPIO61		
J2	**EPWM9_B**	EPWM9_B	UART1_RTSn					FSIRX2_CLK	GPIO62		
B14	**EQEP0_A**	UART4_RTSn			SPI4_CLK				GPIO130	EQEP0_A	SDFM1_CLK0
A14	**EQEP0_B**	UART4_CTSn			SPI4_CS0				GPIO131	EQEP0_B	SDFM1_D0
D11	**EQEP0_INDEX**	UART4_RXD	LIN4_RXD		SPI4_D1				GPIO133	EQEP0_INDEX	SDFM1_D1
C12	**EQEP0_STROBE**	UART4_TXD	LIN4_TXD		SPI4_D0				GPIO132	EQEP0_STROBE	SDFM1_CLK1
P2	**EXT_REFCLK0**	EXT_REFCLK0					XBAROUT15		GPIO121		EQEP1_INDEX
A13	**I2C0_SCL**	I2C0_SCL							GPIO135	EQEP2_B	SDFM1_CLK3
B13	**I2C0_SDA**	I2C0_SDA							GPIO134	EQEP2_A	SDFM1_CLK2
D7	**I2C1_SCL**	I2C1_SCL		SPI3_CS0			XBAROUT7		GPIO23		
C8	**I2C1_SDA**	I2C1_SDA		SPI3_CLK			XBAROUT8		GPIO24		
A9	**LIN1_RXD**	LIN1_RXD	UART1_RXD	SPI2_CS0			XBAROUT5		GPIO19		
B9	**LIN1_TXD**	LIN1_TXD	UART1_TXD	SPI2_CLK			XBAROUT6		GPIO20		
B8	**LIN2_RXD**	LIN2_RXD	UART2_RXD	SPI2_D0					GPIO21		
A8	**LIN2_TXD**	LIN2_TXD	UART2_TXD	SPI2_D1					GPIO22		
M1	**MCAN0_RX**	MCAN0_RX	SPI4_CS0						GPIO7		
L1	**MCAN0_TX**	MCAN0_TX	SPI4_CLK						GPIO8		
L2	**MCAN1_RX**	MCAN1_RX	SPI4_D0						GPIO9		
K1	**MCAN1_TX**	MCAN1_TX	SPI4_D1						GPIO10		
A12	**MCAN2_RX**	MCAN2_RX	UART2_RTSn						GPIO137	EQEP2_INDEX	SDFM1_D3
B12	**MCAN2_TX**	MCAN2_TX	UART1_RTSn						GPIO136	EQEP2_STROBE	SDFM1_D2
M17	**MDIO0_MDC**	MDIO0_MDC							GPIO42		
N16	**MDIO0_MDIO**	MDIO0_MDIO							GPIO41		
A5	**MMC0_CD**	MMC0_CD	UART0_CTSn	I2C2_SDA			EPWM20_B	GPMC0_AD15	GPIO84	SDFM1_D3	
B6	**MMC0_CLK**	MMC0_CLK	UART0_RXD	LIN0_RXD			EPWM17_A	GPMC0_AD8	GPIO77	SDFM1_CLK0	
A4	**MMC0_CMD**	MMC0_CMD	UART0_TXD	LIN0_TXD			EPWM17_B	GPMC0_AD9	GPIO78	SDFM1_D0	
B5	**MMC0_D0**	MMC0_D0	UART2_RXD	I2C1_SCL			EPWM18_A	GPMC0_AD10	GPIO79	SDFM1_CLK1	
B4	**MMC0_D1**	MMC0_D1					EPWM18_B	GPMC0_AD11	GPIO80	SDFM1_D1	
A3	**MMC0_D2**	MMC0_D2	UART2_TXD	I2C1_SDA			EPWM19_A	GPMC0_AD12	GPIO81	SDFM1_CLK2	
A2	**MMC0_D3**	MMC0_D3	UART3_RTSn				EPWM19_B	GPMC0_AD13	GPIO82	SDFM1_D2	
C6	**MMC0_WP**	MMC0_WP	UART0_RTSn	I2C2_SCL			EPWM20_A	GPMC0_AD14	GPIO83	SDFM1_CLK3	
R2	**PORZ**	PORZ									
L18	**PR0_MDIO0_MDC**	PR0_MDIO0_MDC					EPWM21_B	GPMC0_CSn3	GPIO86		

Table 4-23. Pinmux Mapping Table (continued)

Pin#	Pinlist	Mode0	Mode1	Mode2	Mode3	Mode4	Mode5	Mode6	Mode7	Mode8	Mode9
L17	**PR0_MDIO0_ MDIO**	PR0_MDIO0_ MDIO					EPWM21_A	GPMC0_CSn2	GPIO85		
K17	**PR0_PRU0_GPO0**	PR0_PRU0_ GPIO0		RMII2_RXD0	RGMII2_RD0	MII2_RXD0	EPWM25_A	GPMC0_A1	GPIO93		
K18	**PR0_PRU0_GPO1**	PR0_PRU0_ GPIO1		RMII2_RXD1	RGMII2_RD1	MII2_RXD1	EPWM25_B	GPMC0_A2	GPIO94		
G18	**PR0_PRU0_ GPO10**	PR0_PRU0_ GPIO10		RMII2_CRS_DV	PR0_UART0_RTSn	MII2_CRS	EPWM23_A	GPMC0_WAIT0	GPIO89		
M16	**PR0_PRU0_GPO11**	PR0_PRU0_ GPIO11		RMII2_TXD0	RGMII2_TD0	MII2_TXD0	EPWM28_A	GPMC0_A7	GPIO99		
M15	**PR0_PRU0_ GPO12**	PR0_PRU0_ GPIO12		RMII2_TXD1	RGMII2_TD1	MII2_TXD1	EPWM28_B	GPMC0_A8	GPIO100		
H17	**PR0_PRU0_ GPO13**	PR0_PRU0_ GPIO13			RGMII2_TD2	MII2_TXD2	EPWM29_A	GPMC0_A9	GPIO101		
H16	**PR0_PRU0_ GPO14**	PR0_PRU0_ GPIO14			RGMII2_TD3	MII2_TXD3	EPWM29_B	GPMC0_A10	GPIO102		
L16	**PR0_PRU0_ GPO15**	PR0_PRU0_ GPIO15		RMII2_TX_EN	RGMII2_TX_CTL	MII2_TX_EN	EPWM27_B	GPMC0_A6	GPIO98		
H18	**PR0_PRU0_ GPO16**	PR0_PRU0_ GPIO16			RGMII2_TXC	MII2_TXCLK	EPWM27_A	GPMC0_A5	GPIO97		
J18	**PR0_PRU0_GPO2**	PR0_PRU0_ GPIO2			RGMII2_RD2	MII2_RXD2	EPWM26_A	GPMC0_A3	GPIO95		
J17	**PR0_PRU0_GPO3**	PR0_PRU0_ GPIO3			RGMII2_RD3	MII2_RXD3	EPWM26_B	GPMC0_A4	GPIO96		
K16	**PR0_PRU0_GPO4**	PR0_PRU0_ GPIO4			RGMII2_RX_CTL	MII2_RXDV	EPWM24_B	GPMC0_A0	GPIO92		
G17	**PR0_PRU0_GPO5**	PR0_PRU0_ GPIO5		RMII2_RX_ER		MII2_RX_ER	EPWM22_A	GPMC0_DIR	GPIO87		
K15	**PR0_PRU0_GPO6**	PR0_PRU0_ GPIO6		RMII2_REF_CLK	RGMII2_RXC	MII2_RXCLK	EPWM24_A	GPMC0_CSn1	GPIO91		
G15	**PR0_PRU0_GPO8**	PR0_PRU0_ GPIO8					EPWM23_B	GPMC0_WPn	GPIO90		
F17	**PR0_PRU0_GPO9**	PR0_PRU0_ GPIO9			PR0_UART0_CTSn	MII2_COL	EPWM22_B	GPMC0_CLK	GPIO88		
F18	**PR0_PRU1_GPO0**	PR0_PRU1_ GPIO0			FSITX2_DATA1	TRC_DATA6		GPMC0_A13	GPIO109		
G16	**PR0_PRU1_GPO1**	PR0_PRU1_ GPIO1			FSIRX2_CLK	TRC_DATA7		GPMC0_A14	GPIO110		
D17	**PR0_PRU1_ GPO10**	PR0_PRU1_ GPIO10			PR0_UART0_TXD	TRC_DATA2	EPWM31_A	GPMC0_BE1n	GPIO105		
B18	**PR0_PRU1_ GPO11**	PR0_PRU1_ GPIO11			FSITX3_DATA1	TRC_DATA12		GPMC0_A19	GPIO115		
B17	**PR0_PRU1_ GPO12**	PR0_PRU1_ GPIO12			FSIRX3_CLK	TRC_DATA13		GPMC0_A20	GPIO116		
D16	**PR0_PRU1_ GPO13**	PR0_PRU1_ GPIO13			FSIRX3_DATA0	TRC_DATA14	XBAROUT11	GPMC0_A21	GPIO117		
C17	**PR0_PRU1_ GPO14**	PR0_PRU1_ GPIO14			FSIRX3_DATA1	TRC_DATA15	XBAROUT12	GPMC0_CSn0	GPIO118		
A17	**PR0_PRU1_ GPO15**	PR0_PRU1_ GPIO15			FSITX3_DATA0	TRC_DATA11		GPMC0_A18	GPIO114		

Table 4-23. Pinmux Mapping Table (continued)

Pin#	Pinlist	Mode0	Mode1	Mode2	Mode3	Mode4	Mode5	Mode6	Mode7	Mode8	Mode9
C16	**PR0_PRU1_GPO16**	PR0_PRU1_GPIO16			FSITX3_CLK	TRC_DATA10		GPMC0_A17	GPIO113		
C15	**PR0_PRU1_GPO18**	PR0_PRU1_GPIO18		UART3_TXD	PR0_IEP0_EDIO_DATA_IN_OUT31	TRC_CTL	XBAROUT14	GPMC0_WAIT1	GPIO120		EQEP1_B
D15	**PR0_PRU1_GPO19**	PR0_PRU1_GPIO19		UART3_RXD	PR0_IEP0_EDC_SYNC_OUT0	TRC_CLK	XBAROUT13		GPIO119		EQEP1_A
E17	**PR0_PRU1_GPO2**	PR0_PRU1_GPIO2			FSIRX2_DATA0	TRC_DATA8		GPMC0_A15	GPIO111		
E18	**PR0_PRU1_GPO3**	PR0_PRU1_GPIO3			FSIRX2_DATA1	TRC_DATA9		GPMC0_A16	GPIO112		
F16	**PR0_PRU1_GPO4**	PR0_PRU1_GPIO4			FSITX2_DATA0	TRC_DATA5		GPMC0_A12	GPIO108		
F15	**PR0_PRU1_GPO5**	PR0_PRU1_GPIO5				TRC_DATA0	EPWM30_A	GPMC0_OEn_REn	GPIO103		
E16	**PR0_PRU1_GPO6**	PR0_PRU1_GPIO6			FSITX2_CLK	TRC_DATA4		GPMC0_A11	GPIO107		
D18	**PR0_PRU1_GPO8**	PR0_PRU1_GPIO8				TRC_DATA3	EPWM31_B	GPMC0_WEn	GPIO106		
C18	**PR0_PRU1_GPO9**	PR0_PRU1_GPIO9			PR0_UART0_RXD	TRC_DATA1	EPWM30_B	GPMC0_BE0n_CLE	GPIO104		
N2	**QSPI0_CLK**	QSPI0_CLK							GPIO2		
P1	**QSPI0_CSN0**	QSPI0_CSn0							GPIO0		
R3	**QSPI0_CSN1**	QSPI0_CSn1					XBAROUT0		GPIO1		
N1	**QSPI0_D0**	QSPI0_D0							GPIO3		
N4	**QSPI0_D1**	QSPI0_D1							GPIO4		
M4	**QSPI0_D2**	QSPI0_D2							GPIO5		
P3	**QSPI0_D3**	QSPI0_D3							GPIO6		
U17	**RGMII1_RD0**	RGMII1_RD0	RMII1_RXD0	MII1_RXD0				FSITX0_DATA1	GPIO31	EQEP2_STROBE	
T17	**RGMII1_RD1**	RGMII1_RD1	RMII1_RXD1	MII1_RXD1				FSIRX0_CLK	GPIO32	EQEP2_INDEX	
U18	**RGMII1_RD2**	RGMII1_RD2		MII1_RXD2				FSIRX0_DATA0	GPIO33	EQEP0_A	
T18	**RGMII1_RD3**	RGMII1_RD3		MII1_RXD3				FSIRX0_DATA1	GPIO34	EQEP0_B	
R18	**RGMII1_RX_CTL**	RGMII1_RX_CTL	RMII1_RX_ER	MII1_RXDV				FSITX0_DATA0	GPIO30	EQEP2_B	
R17	**RGMII1_RXC**	RGMII1_RXC	RMII1_REF_CLK	MII1_RXCLK				FSITX0_CLK	GPIO29	EQEP2_A	
P16	**RGMII1_TD0**	RGMII1_TD0	RMII1_TXD0	MII1_TXD0				FSITX1_DATA1	GPIO37	EQEP1_A	
P17	**RGMII1_TD1**	RGMII1_TD1	RMII1_TXD1	MII1_TXD1				FSIRX1_CLK	GPIO38	EQEP1_B	
P18	**RGMII1_TD2**	RGMII1_TD2	RMII1_CRS_DV	MII1_TXD2				FSIRX1_DATA0	GPIO39	EQEP1_STROBE	
N17	**RGMII1_TD3**	RGMII1_TD3		MII1_TXD3				FSIRX1_DATA1	GPIO40	EQEP1_INDEX	
M18	**RGMII1_TX_CTL**	RGMII1_TX_CTL	RMII1_TX_EN	MII1_TX_EN				FSITX1_DATA0	GPIO36	EQEP0_STROBE	
N18	**RGMII1_TXC**	RGMII1_TXC		MII1_TXCLK				FSITX1_CLK	GPIO35	EQEP0_INDEX	
D4	**SAFETY_ERRORN**	SAFETY_ERRORn									
B16	**SDFM0_CLK0**	CLKOUT1							GPIO122	SDFM0_CLK0	EQEP1_STROBE
A16	**SDFM0_CLK1**	PR0_PRU1_GPIO7	CPTS0_TS_SYNC	UART5_RTSn	PR0_IEP0_EDC_SYNC_OUT1		I2C3_SDA		GPIO124	SDFM0_CLK1	
B15	**SDFM0_CLK2**	UART5_TXD					I2C3_SCL	GPMC0_ADVn_ALE	GPIO126	SDFM0_CLK2	
A15	**SDFM0_CLK3**	MCAN3_TX	UART5_RXD						GPIO128	SDFM0_CLK3	

Table 4-23. Pinmux Mapping Table (continued)

Pin#	Pinlist	Mode0	Mode1	Mode2	Mode3	Mode4	Mode5	Mode6	Mode7	Mode8	Mode9
D14	**SDFM0_D0**	PR0_ECAP0_ APWM_OUT							GPIO123	SDFM0_D0	
D13	**SDFM0_D1**	PR0_PRU1_ GPIO17		UART5_CTSn	PR0_IEP0_EDIO_D ATA_IN_OUT30				GPIO125	SDFM0_D1	
C13	**SDFM0_D2**	UART5_RXD							GPIO127	SDFM0_D2	
C14	**SDFM0_D3**	MCAN3_RX							GPIO129	SDFM0_D3	
A11	**SPI0_CLK**	SPI0_CLK	UART3_TXD	LIN3_TXD				FSITX0_CLK	GPIO12		
C11	**SPI0_CS0**	SPI0_CS0	UART3_RXD	LIN3_RXD					GPIO11		
C10	**SPI0_D0**	SPI0_D0						FSITX0_DATA0	GPIO13		
B11	**SPI0_D1**	SPI0_D1						FSITX0_DATA1	GPIO14		
A10	**SPI1_CLK**	SPI1_CLK	UART4_RXD	LIN4_RXD			XBAROUT2	FSIRX0_CLK	GPIO16		
C9	**SPI1_CS0**	SPI1_CS0	UART4_TXD	LIN4_TXD			XBAROUT1		GPIO15		
B10	**SPI1_D0**	SPI1_D0	UART5_TXD				XBAROUT3	FSIRX0_DATA0	GPIO17		
D9	**SPI1_D1**	SPI1_D1	UART5_RXD				XBAROUT4	FSIRX0_DATA1	GPIO18		
B3	**TCK**	TCK									
C5	**TDI**	TDI									
C4	**TDO**	TDO									
U1	**TEMPCAL**	TEMPCAL									
D5	**TMS**	TMS									
B7	**UART0_CTSN**	UART0_CTSn	I2C2_SDA	SPI3_D1	MCAN3_RX	SPI0_CS1	XBAROUT10		GPIO26		
C7	**UART0_RTSN**	UART0_RTSn	I2C2_SCL	SPI3_D0	MCAN3_TX		XBAROUT9		GPIO25		
A7	**UART0_RXD**	UART0_RXD	LIN0_RXD						GPIO27		
A6	**UART0_TXD**	UART0_TXD	LIN0_TXD						GPIO28		
L3	**UART1_RXD**	UART1_RXD	LIN1_RXD				EPWM16_A	GPMC0_AD6	GPIO75		
M3	**UART1_TXD**	UART1_TXD	LIN1_TXD				EPWM16_B	GPMC0_AD7	GPIO76		
U2	**VSYS_MON**	VSYS_MON									
C3	**WARMRSTN**	WARMRSTn									
T1	**XTAL_XI**	XTAL_XI									
R1	**XTAL_XO**	XTAL_XO									

5 References

5.1 References

In addition to this document, the following references are available for download at www.ti.com.

- *AM2634 Sitara™ Microcontrollers*
- *AM263x Sitara™ Microcontrollers Data Sheet*
- *AM263x Sitara™ Microcontrollers Technical Reference Manual*
- *AM263x Sitara™ Microcontrollers Silicon Errata*
- *Texas Instruments Code Composer Studio*
- *Updating XDS110 Firmware*
  - To find the serial number, only follow steps 1 and 2 of updating XDS110 firmware

5.2 Other TI Components Used in This Design

This Control Card uses various other TI components for its functions. A consolidated list of these components with links to their TI product pages is shown below.

- *TPS22918 Load Switch*
- *TMP411 Temperature Sensor*
- *TCAN1042-Q1 CAN Transceiver*
- *XDS110 JTAG Debug Probe*
- *DP83869HM 10/100/1000 Ethernet Physical Layer Transceiver*
- *DP83826 10/100 Industrial Ethernet PHY*
- *TPS3711 Voltage Detector*
- *LMK1C110x LVCMOS Clock Buffer*
- *INA228 Current Monitor with I2C Interface*
- *TLIN2029-Q1 LIN Transceiver*
- *TCA6408 8-Bit I2C I/O Expander*
- *TPIC2810 8-Bit LED Driver with I2C Interface*
- *TCA6416 16-BIT I2C I/O Expander*
- *TUSB320LAI USB Type-C Configuration Channel Logic and Port Control*
- *TPS212x Power MUX*
- *TPS6291x Buck Converter*
- *TPS6217x Step-Down Converter*
- *TPS22918 Load Switch*
- *TPS62097 Step-Down Converter*
- *TPS389x Adjustable Voltage Monitor*

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (February 2023) to Revision D (September 2023)	Page
• (HSEC 180-pin Control Card Docking Station): Added Context to EXT-ON Note	8
• (Power Requirements): Fixed wording of power supplies	8
• (HSEC Pinout): Moved E1 HSEC Pinout to Appendix B	40
• Added Appendix B	55

A E2 Design Changes

The AM263x Control Card had various design changes for the E2 revision of the board. The changes are listed below:

1. **Removal of pull up resistors for QSPI flash D2 and D3 signals.**
   a. The pull up resistors on the data lines D2 and D3 are redundant with the on-die resistors of the QSPI flash itself.
2. **Fixed netlist error and rerouted I2C2_SDA and I2C2_SCL for proper operation.**
   a. The E1 revision of the Control Card had the I2C2_SCL signal tied to ball B7 and I2C2_SDA tied to C7. The correct routing of the signals is implemented in the E2 Control Card with I2C2_SDA connected to B7 and I2C2_SCL connected to C7.

Table A-1. I2C2 Signal Routing

Signal	E1 Pin Routing	E2 Pin Routing
I2C2_SDA	C7	B7
I2C2_SCL	B7	C7

3. **Ethernet PHY default mode changed to enhanced mode from basic mode.**
   a. The Ethernet PHY (DP83826ERHBT) in E1 had a default mode of basic due to a pull down resistor on the MODESELECT pin of the PHY. E2 replaced the pull down with a pull up resistor so that the default mode would be enhanced mode. Enhanced mode allows for the PHY to support real time Ethernet applications.
4. **Add on-board LIN PHY (TLIN2029-Q1).**
   a. In order to support the LIN PHY, a 1:2 mux (U70) was added so that the LIN1_RXD and LIN1_TXD would be able to interface with the PHY without losing the signal pathing for UART1_RXD and UART1_TXD.
   b. Two additional header were added to support the LIN PHY's voltage (J33) and output (J32)

Table A-2. LIN MUX Selection Table

Select Line	Condition	Function
LOW	LIN Selected	A->B1 port
HIGH	HSEC UART Selected	A->B2 port

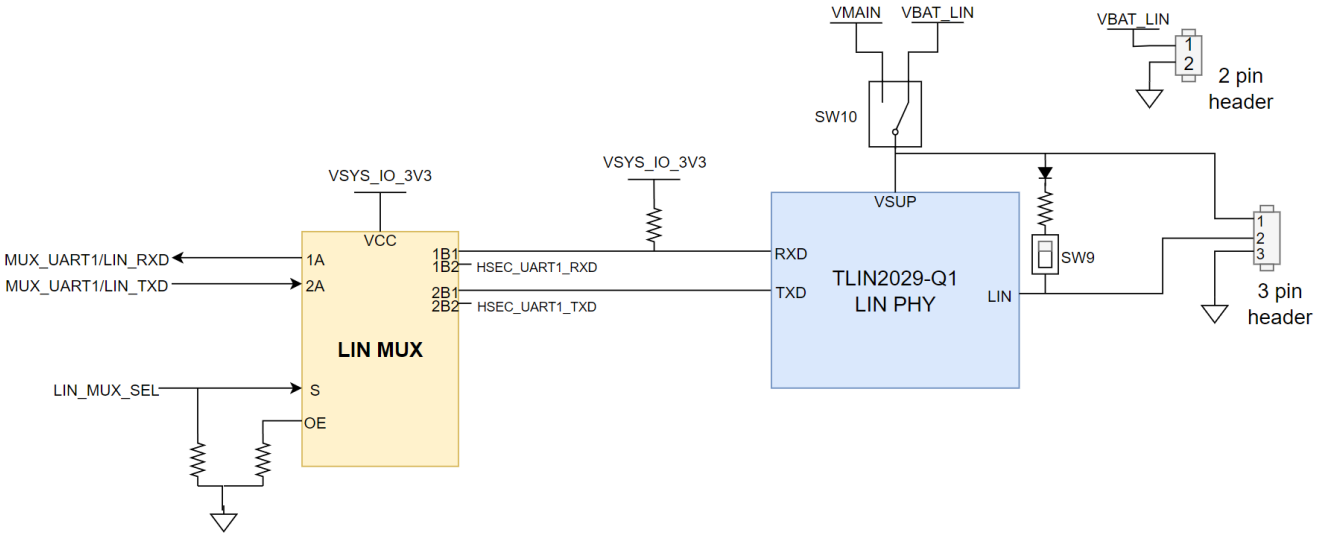

Figure A-1. LIN PHY

5. **Added additional series termination resistors.**
   a. 33Ω resistors were placed for the XDS110 TMS and TCK signals at the output of an isolation buffer (U49). One 33Ω resistor was placed for the XDS110 TDI signal on the OUTA of an isolation buffer (U53).
   b. Series terminations resistors were places on outputs of three isolation buffers to better control edge overshoot/undershoot.

Table A-3. E2 Termination Resistor Location Table

Isolation Buffer Output Pin	Signal Name	Series Termination Resistor Value
U45.2	UART0_RXD	33Ω
U49.6	XDS110_TCK_ISO	33Ω
U49.7	XDS110_TMS_ISO	33Ω
U53.2	XDS110_TDI_ISO	33Ω

6. **DC-DC converter solution components updated.**
   a. The DC-DC buck converters responsible for generating the 3.3V rail and 1.2V rail were both replaced with the TSP62913RPUR buck converter.

Table A-4. E2 Buck Converter Table

DC-DC Conversion	E1 Buck Converter	E2 Buck Converter
5V->3.3V	TPS54334DRCT	TPS62913RPUR
3.3V->1.2V	TPS62826DMQR	TPS62913RPUR

7. **Updated passive components.**
   a. C136 and C1861 were replaced with 0805 from 1210
   b. L3 and L4 were replaced with IHLP2020BZER1R0M01 from 744316100
8. **Changed HSEC ADC Connections.**

Table A-5. E2 HSEC Connector Mapping

HSEC Pin	E1 Signal	E2 Signal
1	NC	NC
2	NC	NC
3	TMS	TMS
4	NC	NC
5	TCK	TCK
6	TDO	TDO
7	GND	GND
8	TDI	TDI
9	DAC_OUT	ADC0_AIN0/DAC_OUT
10	GND	GND
11	ADC0_AIN0_P	ADC0_AIN1/DAC_OUT
12	ADC0_AIN0_n	ADC1_AIN0
13	GND	GND
14	ADC0_AIN1_p	ADC1_AIN1
15	ADC0_AIN1_n	ADC0_AIN2
16	GND	GND
17	ADC0_AIN2_p	ADC0_AIN3
18	ADC0_AIN2_n	ADC1_AIN2
19	GND	GND
20	ADC1_AIN0_p	ADC1_AIN3

Table A-5. E2 HSEC Connector Mapping (continued)

HSEC Pin	E1 Signal	E2 Signal
21	ADC1_AIN0_n	ADC0_AIN4
22	GND	GND
23	ADC1_AIN1_p	ADC0_AIN5
24	ADC1_AIN1_n	ADC1_AIN4
25	ADC1_AIN2_p	ADC4_AIN0/ADC_CAL0
26	ADC1_AIN2_n	ADC1_AIN5
27	ADC2_AIN0_p	ADC4_AIN1/ADC_CAL1
28	ADC2_AIN0_n	ADC3_AIN0
29	GND	GND
30	ADC2_AIN1_p	ADC3_AIN1
31	ADC2_AIN1_n	ADC2_AIN0
32	NC	GND
33	ADC2_AIN2_p	ADC2_AIN1
34	ADC2_AIN2_n	ADC3_AIN2
35	GND	GND
36	ADC3_AIN0_p	ADC3_AIN3
37	ADC3_AIN0_n	ADC2_AIN2
38	GND	GND
39	ADC3_AIN1_p	ADC2_AIN3
40	ADC3_AIN1_n	ADC3_AIN4
41	NC	NC
42	ADC3_AIN2_p	ADC3_AIN5
43	ADC_VREFLO	GND
44	NC	NC
45	ADC_VREFhi	ADC_VREFH

Table A-6. E1 ADC Channel Signals

ADC0	AIN0p	AIN0n	AIN1p	AIN1n	AIN2p	AIN2n
ADC1	AIN0p	AIN0n	AIN1p	AIN1n	AIN2p	AIN2n
ADC2	AIN0p	AIN0n	AIN1p	AIN1n	AIN2p	AIN2n
ADC3	AIN0p	AIN0n	AIN1p	AIN1n	AIN2p	GND
ADC4	GND	GND	GND	GND	GND	GND

Table A-7. E2 ADC Channel Signals

ADC0	AIN0	AIN1	AIN2	AIN3	AIN4	AIN5
ADC1	AIN0	AIN1	AIN2	AIN3	AIN4	AIN5
ADC2	AIN0	AIN1	AIN2	AIN3	GND	GND
ADC3	AIN0	AIN1	AIN2	AIN3	AIN4	AIN5
ADC4	AIN0	AIN1	GND	GND	GND	GND

9. **Added two 2:1 MUX's to support new HSEC ADC Connections.**

Table A-8. E2 HSEC MUX Table

MUX_SEL Signal	Condition	Function	Description
ADC1_MUX_SEL	SEL Signal HIGH	S1A->D1	route HSEC_ADC0_AIN0 to AM263
		S2A->D2	route HSEC_ADC0_AIN1 to AM263
	SEL Signal LOW	S1B->D1	route HSEC_DAC_OUT to AM263
		S2B->D2	route HSEC_DAC_OUT to AM263
ADC2_MUX_SEL	SEL Signal HIGH	S1A->D1	route HSEC_ADC4_AIN0 to AM263
		S2A->D2	route HSEC_ADC4_AIN1 to AM263
	SEL Signal LOW	S1B->D1	route ADC_CAL0 to AM263
		S2B->D2	route ADC_CAL0 to AM263

10. **Updated ADC ESD Connections.**

Table A-9. E2 ESD Connection Mapping

E1 ESD Pin	E1 Signal	E2 ESD Pin	E2 Signal
U26.1	HSEC_ADC0_AIN0_P	U35.1	HSEC_ADC0_AIN0/DAC_OUT
U26.2	GND	U35.2	GND
U26.3	HSEC_ADC0_AIN0_N	U35.3	HSEC_ADC0_AIN1/DAC_OUT
U26.4	HSEC_ADC0_AIN1_N	U35.4	HSEC_ADC4_AIN0/ADC_CAL0
U26.5	VDDA_IO_1V8	U35.5	VDDA_IO_3V3
U26.6	HSEC_ADC0_AIN1_P	U35.6	HSEC_ADC4_AIN1/ADC_CAL1
U27.1	HSEC_ADC0_AIN2_P	U36.1	HSEC_ADC1_AIN0
U27.2	GND	U36.2	GND
U27.3	HSEC_ADC0_AIN2_N	U36.3	HSEC_ADC1_AIN1
U27.4	HSEC_ADC1_AIN0_N	U36.4	HSEC_ADC0_AIN3
U27.5	VDDA_IO_1V8	U36.5	VDDA_IO_3V3
U27.6	HSEC_ADC1_AIN0_P	U36.6	HSEC_ADC0_AIN2
U28.1	HSEC_ADC1_AIN1_P	U37.1	HSEC_ADC2_AIN0
U28.2	GND	U37.2	GND
U28.3	HSEC_ADC1_AIN1_N	U37.3	HSEC_ADC2_AIN1
U28.4	HSEC_ADC1_AIN2_N	U37.4	HSEC_ADC0_AIN5
U28.5	VDDA_IO_1V8	U37.5	VDDA_IO_3V3
U28.6	HSEC_ADC1_AIN2_P	U37.6	HSEC_ADC0_AIN4
U29.1	HSEC_ADC2_AIN0_P	U38.1	HSEC_ADC3_AIN0
U29.2	GND	U38.2	GND
U29.3	HSEC_ADC2_AIN0_N	U38.3	HSEC_ADC3_AIN1
U29.4	HSEC_ADC2_AIN1_N	U38.4	HSEC_ADC3_AIN3
U29.5	VDDA_IO_1V8	U38.5	VDDA_IO_3V3
U29.6	HSEC_ADC2_AIN1_P	U38.6	HSEC_ADC3_AIN2
U30.1	HSEC_ADC2_AIN2_P	U39.1	HSEC_ADC3_AIN4
U30.2	GND	U39.2	GND
U30.3	HSEC_ADC2_AIN2_N	U39.3	HSEC_ADC3_AIN5
U30.4	HSEC_ADC3_AIN0_N	U39.4	HSEC_ADC2_AIN3

Table A-9. E2 ESD Connection Mapping (continued)

E1 ESD Pin	E1 Signal	E2 ESD Pin	E2 Signal
U30.5	VDDA_IO_1V8	U39.5	VDDA_IO_3V3
U30.6	HSEC_ADC3_AIN0_P	U39.6	HSEC_ADC2_AIN2
U31.1	HSEC_ADC3_AIN1_P	U40.1	HSEC_ADC1_AIN2
U31.2	GND	U40.2	GND
U31.3	HSEC_ADC3_AIN1_N	U40.3	HSEC_ADC1_AIN3
U31.4	HSEC_ADC3_AIN2_P	U40.4	HSEC_ADC1_AIN4
U31.5	VDDA_IO_1V8	U40.5	VDDA_IO_3V3
U31.6	NC	U40.6	HSEC_ADC1_AIN5

B E1 HSEC Pinout Table

Note

The table in this section applies only to the **E1** version of the AM263x Control Card. For a table of the HSEC pinout for E2 and beyond, refer to HSEC Pinout and Pinmux Mapping.

Table B-1. E1 HSEC Pinout

Pin #	Package Signal Name	Muxed Signal Options		Muxed Signal Options	Package Signal Name	Pin #
1	NC	NC		NC	NC	2
3	HSEC_TMS	TMS		NC	NC	4
5	HSEC_TCK	TCK		TDO	HSEC_TDO	6
7	GND	GND		TDI	HSEC_TDI	8
9	HSEC_DAC_OUT	DAC_OUT		GND	GND	10
11	NC	NC		ADC0_AIN0	ADC0_AIN0	12
13	GND	GND		ADC0_AIN1	ADC0_AIN1	14
15	ADC0_AIN2	ADC0_AIN2		GND	GND	16
17	ADC0_AIN3	ADC0_AIN3		ADC1_AIN0	ADC1_AIN0	18
19	GND	GND		ADC1_AIN1	ADC1_AIN1	20
21	ADC1_AIN2	ADC1_AIN2		GND	GND	22
23	ADC1_AIN3	ADC1_AIN3		ADC2_AIN0	ADC2_AIN0	24
25	ADC_CAL0	ADC_CAL0		ADC2_AIN1	ADC2_AIN1	26
27	ADC_CAL1	ADC_CAL1		ADC2_AIN2	ADC2_AIN2	28
29	GND	GND		ADC2_AIN3	ADC2_AIN3	30
31	ADC3_AIN0	ADC3_AIN0		GND	GND	32
33	ADC3_AIN1	ADC3_AIN1		ADC3_AIN2	ADC3_AIN2	34
35	GND	GND		ADC3_AIN3	ADC3_AIN3	36
37	ADC4_AIN0	ADC4_AIN0		GND	GND	38
39	ADC4_AIN1	ADC4_AIN1		ADC4_AIN2	ADC4_AIN2	40
41	NC	NC		ADC4_AIN3	ADC4_AIN3	42
43	NC	NC		NC	NC	44
45	HSEC_ADC-VREFHI	HSEC_ADC-VREFHI		GND	GND	46
47	GND	GND		HSEC_5V0	HSEC_5V0	48
49	EPWM0_A	EPWM0_A/GPIO43		EPWM2_A/GPIO47	EPWM2_A	50
51	EPWM0_B	EPWM0_B/GPIO44		EPWM2_B/GPIO48	EPWM2_B	52
53	EPWM1_A	EPWM1_A/GPIO45		EPWM3_A/GPIO49	EPWM3_A	54
55	EPWM1_B	EPWM1_B/GPIO46		EPWM3_B/GPIO50	EPWM3_B	56
57	EPWM4_A	EPWM4_A/GPIO51		EPWM6_A/FSIRX1_CLK/GPIO55	EPWM6_A	58
59	EPWM4_B	EPWM4_B/FSITX1_CLK/GPIO52		EPWM6_B/FSIRX1_DATA0/GPIO56	EPWM6_B	60
61	EPWM5_A	EPWM5_A/FSITX1_DATA0/GPIO53		EPWM7_A/FSIRX1_DATA1/GPIO57	EPWM7_A	62
63	EPWM5_B	EPWM5_B/FSITX1_DATA1/GPIO54		EPWM7_B/GPIO58	EPWM7_B	64
65	GND	GND		NC	NC	66

Table B-1. E1 HSEC Pinout (continued)

Pin #	Package Signal Name	Muxed Signal Options		Muxed Signal Options	Package Signal Name	Pin #
67	SPI0_D0	SPI0_D0/FSITX0_DATA0/GPIO13/SOP3		PR0_PRU1_GPO19/UART3_RXD/PR0_IEP0_EDC_SYNC_OUT0/TRC_CLK/ XBAROUT13/GPIO119/EQEP1_A	EQEP1_A	68
69	SPI0_D1	SPI0_D1/FSITX0_DATA1/GPIO14		PR0_PRU1_GPO18/UART3_TXD/PR0_IEP0_EDIO_DATA_IN_OUT31/TRC_CTL/ XBAROUT14/GPMC0_WAIT1/GPIO120/EQEP1_B	EQEP1_B	70
71	SPI0_CLK	SPI0_CLK/UART3_TXD/LIN3_TXD/FSITX0_CLK/GPIO12/SOP2		SDFM0_CLK0/CLKOUT1/GPIO122/EQEP1_STROBE	EQEP1_STROBE	72
73	SPI0_CS0	SPI0_CS0/UART3_RXD/LIN3_RXD/GPIO11		EXT_REFCLK0/XBAROUT15/GPIO121/EQEP1_INDEX	EQEP1_INDEX	74
75	SPI1_D0	SPI1_D0/UART5_TXD/XBAROUT3/FSIRX0_DATA0/GPIO17		LIN1_RXD/UART1_RXD/SPI2_CS0/XBAROUT5/GPIO19	UART1_RXD	76
77	SPI1_D1	SPI1_D1/UART5_RXD/XBAROUT4/FSIRX0_DATA1/GPIO18		LIN1_TXD/UART1_TXD/SPI2_CLK/XBAROUT6/GPIO20	UART1_TXD	78
79	SPI1_CLK	SPI1_CLK/UART4_RXD/LIN4_RXD/XBAROUT2/FSIRX0_CLK/GPIO16		MCAN0_RX/SPI4_CS0/GPIO7	MCAN0_RX	80
81	SPI1_CS0	SPI1_CS0/UART4_TXD/LIN4_TXD/XBAROUT1/GPIO15		MCAN0_TX/SPI4_CLK/GPIO8	MCAN0_TX	82
83	GND	GND		HSEC_5V0	HSEC_5V0	84
85	I2C1_SDA	I2C1_SDA/SPI3_CLK/XBAROUT8/GPIO24		EPWM11_A/UART2_CTSn/GPMC0_CLKLB/GPIO65	GPMC0_CLKB	86
87	I2C1_SCL	I2C1_SCL/SPI3_CS0/XBAROUT7/GPIO23		NC	NC	88
89	EPWM21_A	PR0_MDIO0_MDIO/EPWM21_A/GPMC0_CSn2/GPIO85		PR0_MDIO0_MDC/EPWM21_B/GPMC0_CSn3/GPIO86	EPWM21_B	90
91	SDFM0_D0	SDFM0_D0/PR0_ECAP0_APWM_OUT/GPIO123		I2C0_SDA/GPIO134/EQEP2_A/SDFM1_CLK2	EQEP2_A	92
93	EQEP2_B	I2C0_SCL/GPIO135/EQEP2_B/SDFM1_CLK3		MCAN2_RX/UART2_RTSn/GPIO137/EQEP2_INDEX/SDFM1_D3	EQEP2_INDEX	94
95	EQEP2_STROBE	MCAN2_TX/UART1_RTSn/GPIO136/EQEP2_STROBE/SDFM1_D2		NC	NC	96
97	GND	GND		HSEC_5V0	HSEC_5V0	98
99	SDFM0_D1	SDFM0_D1/PR0_PRU1_GPIO17/UART5_CTSn/ PR0_IEP0_EDIO_DATA_IN_OUT30/GPIO125		EQEP0_B/UART4_CTSn/SPI4_CS0/GPIO131/SDFM1_D0	EQEP0_B	100
101	SDFM0_CLK1	SDFM0_CLK1/PR0_PRU1_GPIO7/CPTS0_TS_SYNC/UART5_RTSn/ PR0_IEP0_EDC_SYNC_OUT1/I2C3_SDA/GPIO124		EQEP0_A/UART4_RTSn/SPI4_CLK/GPIO130/SDFM1_CLK0	EQEP0_A	102
103	SDFM0_D2	SDFM0_D2/UART5_RXD/GPIO127		EQEP0_STROBE/UART4_TXD/LIN4_TXD/SPI4_D0/GPIO132/SDFM1_CLK1	EQEP0_STROBE	104
105	SDFM0_CLK2	SDFM0_CLK2/UART5_TXD/I2C3_SCL/GPMC0_ADVn_ALE/GPIO126/ SDFM0_CLK2		EQEP0_INDEX/UART4_RXD/LIN4_RXD/SPI4_D1/GPIO133/SDFM1_D1	EQEP0_INDEX	106
107	SDFM0_D3	SDFM0_D3/MCAN3_RX/GPIO129		PR0_PRU0_GPO5/RMII2_RX_ER/MII2_RX_ER/EPWM22_A/GPMC0_DIR/ GPIO87	MII0_RXER	108
109	SDFM0_CLK3	SDFM0_CLK3/MCAN3_TX/UART5_RXD/GPIO128		PR0_PRU0_GPO9/PR0_UART0_CTSn/MII2_COL/EPWM22_B/GPMC0_CLK/ GPIO88	MII0_CO	110
111	GND	GND		HSEC_5V0	HSEC_5V0	112
113	NC	NC		NC	NC	114
115	NC	NC		NC	NC	116
117	NC	NC		HSEC_5V0	HSEC_5V0	118
119	NC	NC		PORz	PORz	120
121	ICSS_MII0_CRS	PR0_PRU0_GPO10/RMII2_CRS_DV/PR0_UART0_RTSn/MII2_CRS/EPWM23_A/ GPMC0_WAIT0/GPIO89		PR0_PRU0_GPO8/EPWM23_B/GPMC0_WPn/GPIO90	ICSS_MII0_RXLINK	122
123	ICSS_MII0_RXCLK	PR0_PRU0_GPO6/RMII2_REF_CLK/RGMII2_RXC/MII2_RXCLK/EPWM24_A/ GPMC0_CSn1/GPIO91		PR0_PRU0_GPO4/RGMII2_RX_CTL/MII2_RXDV/EPWM24_B/GPMC0_A0/ GPIO92	ICSS_MII0_RXDV	124
125	ICSS_MII0_RXD0	PR0_PRU0_GPO0/RMII2_RXD0/RGMII2_RD0/MII2_RXD0/EPWM25_A/ GPMC0_A1/GPIO93		PR0_PRU0_GPO1/RMII2_RXD1/RGMII2_RD1/MII2_RXD1/EPWM25_B/ GPMC0_A2/GPIO94	ICSS_MII0_RXD1	126
127	ICSS_MII0_RXD2	PR0_PRU0_GPO2/RGMII2_RD2/MII2_RXD2/EPWM26_A/GPMC0_A3/GPIO95		PR0_PRU0_GPO3/RGMII2_RD3/MII2_RXD3/EPWM26_B/GPMC0_A4/GPIO96	ICSS_MII0_RXD3	128
129	ICSS_MII0_TXCLK	PR0_PRU0_GPO16/RGMII2_TXC/MII2_TXCLK/EPWM27_A/GPMC0_A5/GPIO97		PR0_PRU0_GPO15/RMII2_TX_EN/RGMII2_TX_CTL/MII2_TX_EN/EPWM27_B/ GPMC0_A6/GPIO98	ICSS_MII0_TXEN	130
131	ICSS_MII0_TXD0	PR0_PRU0_GPO11/RMII2_TXD0/RGMII2_TD0/MII2_TXD0/EPWM28_A/ GPMC0_A7/GPIO99		PR0_PRU0_GPO12/RMII2_TXD1/RGMII2_TD1/MII2_TXD1/EPWM28_B/ GPMC0_A8/GPIO100	ICSS_MII0_TXD1	132

Table B-1. E1 HSEC Pinout (continued)

Pin #	Package Signal Name	Muxed Signal Options		Muxed Signal Options	Package Signal Name	Pin #
133	ICSS_MII0_TXD2	PR0_PRU0_GPO14/RGMII2_TD3/MII2_TXD3/EPWM29_B/GPMC0_A10/ GPIO102		PR0_PRU0_GPO14/RGMII2_TD3/MII2_TXD3/EPWM29_B/GPMC0_A10/ GPIO102	ICSS_MII0_TXD3	134
135	GND	GND		NC	NC	136
137	ICSS_MII1_RXER	PR0_PRU1_GPO5/TRC_DATA0/EPWM30_A/GPMC0_OEn_REn/GPIO103		PR0_PRU1_GPO9/PR0_UART0_RXD/TRC_DATA1/EPWM30_B/ GPMC0_BE0n_CLE/GPIO104	ICSS_MII1_COL	138
139	ICSS_MII1_CRS	PR0_PRU1_GPO10/PR0_UART0_TXD/TRC_DATA2/EPWM31_A/GPMC0_BE1n/ GPIO105		PR0_PRU1_GPO8/TRC_DATA3/EPWM31_B/GPMC0_WEn/GPIO106	ICSS_MII1_RXLINK	140
141	ICSS_MII1_RXCLK	PR0_PRU1_GPO6/FSITX2_CLK/TRC_DATA4/GPMC0_A11/GPIO107		PR0_PRU1_GPO4/FSITX2_DATA0/TRC_DATA5/GPMC0_A12/GPIO108	ICSS_MII1_RXDV	142
143	ICSS_MII1_RXD0	PR0_PRU1_GPO0/FSITX2_DATA1/TRC_DATA6/GPMC0_A13/GPIO109		PR0_PRU1_GPO1/FSIRX2_CLK/TRC_DATA7/GPMC0_A14/GPIO110	ICSS_MII1_RXD1	144
145	ICSS_MII1_RXD2	PR0_PRU1_GPO2/FSIRX2_DATA0/TRC_DATA8/GPMC0_A15/GPIO111		PR0_PRU1_GPO3/FSIRX2_DATA1/TRC_DATA9/GPMC0_A16/GPIO112	ICSS_MII1_RXD3	146
147	ICSS_MII1_TXCLK	PR0_PRU1_GPO16/FSITX3_CLK/TRC_DATA10/GPMC0_A17/GPIO113		PR0_PRU1_GPO15/FSITX3_DATA0/TRC_DATA11/GPMC0_A18/GPIO114	ICSS_MII1_TXEN	148
149	ICSS_MII1_TXD0	PR0_PRU1_GPO11/FSITX3_DATA1/TRC_DATA12/GPMC0_A19/GPIO115		PR0_PRU1_GPO12/FSIRX3_CLK/TRC_DATA13/GPMC0_A20/GPIO116	ICSS_MII1_TXD1	150
151	ICSS_MII1_TXD2	PR0_PRU1_GPO13/FSIRX3_DATA0/TRC_DATA14/XBAROUT11/GPMC0_A21/ GPIO117		PR0_PRU1_GPO14/FSIRX3_DATA1/TRC_DATA15/XBAROUT12/GPMC0_CSn0/ GPIO118	ICSS_MII1_TXD3	152
153	GPMC0_AD0	EPWM13_A/UART1_RIn/GPMC0_AD0/GPIO69		EPWM13_B/UART1_DTRn/GPMC0_AD1/GPIO70	GPMC0_AD1	154
155	GPMC0_AD2	EPWM14_A/UART1_DSRn/GPMC0_AD2/GPIO71		EPWM14_B/MII1_RX_ER/GPMC0_AD3/GPIO72	GPMC0_AD3	156
157	GND	GND		HSEC_5V0	HSEC_5V0	158
159	GPMC0_AD4	EPWM15_A/UART5_TXD/MII1_COL/GPMC0_AD4/GPIO73		EPWM15_B/UART5_RXD/MII1_CRS/GPMC0_AD5/GPIO74	GPMC0_AD5	160
161	GPMC0_AD6	UART1_RXD/LIN1_RXD/EPWM16_A/GPMC0_AD6/GPIO75		UART1_TXD/LIN1_TXD/EPWM16_B/GPMC0_AD7/GPIO76	GPMC0_AD7	162
163	GPMC0_AD8	MMC0_CLK/UART0_RXD/LIN0_RXD/EPWM17_A/GPMC0_AD8/GPIO77/ SDFM1_CLK0		MMC0_CMD/UART0_TXD/LIN0_TXD/EPWM17_B/GPMC0_AD9/GPIO78/ SDFM1_D0	GPMC0_AD9	164
165	GPMC0_AD10	MMC0_D0/UART2_RXD/I2C1_SCL/EPWM18_A/GPMC0_AD10/GPIO79/ SDFM1_CLK1		MMC0_D1/EPWM18_B/GPMC0_AD11/GPIO80/SDFM1_D1	GPMC0_AD11	166
167	GPMC0_AD12	MMC0_D2/UART2_TXD/I2C1_SDA/EPWM19_A/GPMC0_AD12/GPIO81/ SDFM1_CLK2		MMC0_D3/UART3_RTSn/EPWM19_B/GPMC0_AD13/GPIO82/SDFM1_D2	GPMC0_AD13	168
169	GPMC0_AD14	MMC0_WP/UART0_RTSn/I2C2_SCL/EPWM20_A/GPMC0_AD14/GPIO83/ SDFM1_CLK3		MMC0_CD/UART0_CTSn/I2C2_SDA/EPWM20_B/GPMC0_AD15/GPIO84/ SDFM1_D3	GPMC0_AD15	170
171	NC	NC		NC	NC	172
173	NC	NC		NC	NC	174
175	NC	NC		NC	NC	176
177	NC	NC		NC	NC	178
179	GND	GND		HSEC_5V0	HSEC_5V0	180

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2 *Limited Warranty and Related Remedies/Disclaimers*:

   2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.

   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

WARNING

Evaluation Kits are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.

User shall operate the Evaluation Kit within TI’s recommended guidelines and any applicable legal or environmental requirements as well as reasonable and customary safeguards. Failure to set up and/or operate the Evaluation Kit within TI’s recommended guidelines may result in personal injury or death or property damage. Proper set up entails following TI’s instructions for electrical ratings of interface circuits such as input, output and electrical loads.

NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGREDATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 *Regulatory Notices:*

3.1 *United States*

3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

【無線電波を送信する製品の開発キットをお使いになる際の注意事項】 開発キットの中には技術基準適合証明を受けていないものがあります。 技術適合証明を受けていないもののご使用に際しては、電波法遵守のため、以下のいずれかの措置を取っていただく必要がありますのでご注意ください。

1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

なお、本製品は、上記の「ご使用にあたっての注意」を譲渡先、移転先に通知しない限り、譲渡、移転できないものとします。

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東京都新宿区西新宿 6 丁目 2 4 番 1 号

西新宿三井ビル

3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

電力線搬送波通信についての開発キットをお使いになる際の注意事項については、次のところをご覧ください。https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-for-power-line-communication.html

3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

6. *Disclaimers:*

6.1 EXCEPT AS SET FORTH ABOVE, EVMS AND ANY MATERIALS PROVIDED WITH THE EVM (INCLUDING, BUT NOT LIMITED TO, REFERENCE DESIGNS AND THE DESIGN OF THE EVM ITSELF) ARE PROVIDED "AS IS" AND "WITH ALL FAULTS." TI DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, REGARDING SUCH ITEMS, INCLUDING BUT NOT LIMITED TO ANY EPIDEMIC FAILURE WARRANTY OR IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF ANY THIRD PARTY PATENTS, COPYRIGHTS, TRADE SECRETS OR OTHER INTELLECTUAL PROPERTY RIGHTS.

6.2 EXCEPT FOR THE LIMITED RIGHT TO USE THE EVM SET FORTH HEREIN, NOTHING IN THESE TERMS SHALL BE CONSTRUED AS GRANTING OR CONFERRING ANY RIGHTS BY LICENSE, PATENT, OR ANY OTHER INDUSTRIAL OR INTELLECTUAL PROPERTY RIGHT OF TI, ITS SUPPLIERS/LICENSORS OR ANY OTHER THIRD PARTY, TO USE THE EVM IN ANY FINISHED END-USER OR READY-TO-USE FINAL PRODUCT, OR FOR ANY INVENTION, DISCOVERY OR IMPROVEMENT, REGARDLESS OF WHEN MADE, CONCEIVED OR ACQUIRED.

7. *USER'S INDEMNITY OBLIGATIONS AND REPRESENTATIONS.* USER WILL DEFEND, INDEMNIFY AND HOLD TI, ITS LICENSORS AND THEIR REPRESENTATIVES HARMLESS FROM AND AGAINST ANY AND ALL CLAIMS, DAMAGES, LOSSES, EXPENSES, COSTS AND LIABILITIES (COLLECTIVELY, "CLAIMS") ARISING OUT OF OR IN CONNECTION WITH ANY HANDLING OR USE OF THE EVM THAT IS NOT IN ACCORDANCE WITH THESE TERMS. THIS OBLIGATION SHALL APPLY WHETHER CLAIMS ARISE UNDER STATUTE, REGULATION, OR THE LAW OF TORT, CONTRACT OR ANY OTHER LEGAL THEORY, AND EVEN IF THE EVM FAILS TO PERFORM AS DESCRIBED OR EXPECTED.

8. *Limitations on Damages and Liability:*

   8.1 *General Limitations*. IN NO EVENT SHALL TI BE LIABLE FOR ANY SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL, OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF THESE TERMS OR THE USE OF THE EVMS , REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. EXCLUDED DAMAGES INCLUDE, BUT ARE NOT LIMITED TO, COST OF REMOVAL OR REINSTALLATION, ANCILLARY COSTS TO THE PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES, RETESTING, OUTSIDE COMPUTER TIME, LABOR COSTS, LOSS OF GOODWILL, LOSS OF PROFITS, LOSS OF SAVINGS, LOSS OF USE, LOSS OF DATA, OR BUSINESS INTERRUPTION. NO CLAIM, SUIT OR ACTION SHALL BE BROUGHT AGAINST TI MORE THAN TWELVE (12) MONTHS AFTER THE EVENT THAT GAVE RISE TO THE CAUSE OF ACTION HAS OCCURRED.

   8.2 *Specific Limitations.* IN NO EVENT SHALL TI'S AGGREGATE LIABILITY FROM ANY USE OF AN EVM PROVIDED HEREUNDER, INCLUDING FROM ANY WARRANTY, INDEMITY OR OTHER OBLIGATION ARISING OUT OF OR IN CONNECTION WITH THESE TERMS, , EXCEED THE TOTAL AMOUNT PAID TO TI BY USER FOR THE PARTICULAR EVM(S) AT ISSUE DURING THE PRIOR TWELVE (12) MONTHS WITH RESPECT TO WHICH LOSSES OR DAMAGES ARE CLAIMED. THE EXISTENCE OF MORE THAN ONE CLAIM SHALL NOT ENLARGE OR EXTEND THIS LIMIT.

9. *Return Policy.* Except as otherwise provided, TI does not offer any refunds, returns, or exchanges. Furthermore, no return of EVM(s) will be accepted if the package has been opened and no return of the EVM(s) will be accepted if they are damaged or otherwise not in a resalable condition. If User feels it has been incorrectly charged for the EVM(s) it ordered or that delivery violates the applicable order, User should contact TI. All refunds will be made in full within thirty (30) working days from the return of the components(s), excluding any postage or packaging costs.

10. *Governing Law:* These terms and conditions shall be governed by and interpreted in accordance with the laws of the State of Texas, without reference to conflict-of-laws principles. User agrees that non-exclusive jurisdiction for any dispute arising out of or relating to these terms and conditions lies within courts located in the State of Texas and consents to venue in Dallas County, Texas. Notwithstanding the foregoing, any judgment may be enforced in any United States or foreign court, and TI may seek injunctive relief in any United States or foreign court.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

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