Programmer's Guide

LMK3H0102 Configuration Guide

ABSTRACT

This document provides information on the configurations available for the LMK3H0102 device. For the default configuration of the LMK3H0102V18 and LMK3H0102V33 devices, refer to the LMK3H0102 data sheet.

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Trademarks

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1 Introduction

This programming guide helps designers understand the differences between each configuration offered for the LMK3H0102 devices. Each LMK3H0102Axxx part number is a different configuration, with potentially different frequencies and output formats. Use this guide to determine if one of the released configurations meets application requirements. Critical Configuration Settings Overview details the high level settings for each configuration. OTP Page Configuration Overview describes each key configuration parameter that can change between configurations, and details the settings for each OTP Page. LMK3H0102Axxx Configuration Registers provides each register setting for each of the configurations that are available.

2 Critical Configuration Settings Overview

This section provides an overview of the critical device settings of the LMK3H0102Axxx configurations.

2.1 LMK3H0102Axxx Critical Device Settings

LMK3H0102Axxx Critical Device Settings displays the critical device settings upon startup in I^2C Mode. Some configurations appear the same in this table, but have differences in the full configuration table. For full device settings for each part number, refer to OTP Page Configuration Overview. LMK3H0102 Configuration Orderable Part Numbers lists the orderable part numbers for the different configurations.

Table 2-1. LMK3H0102Axxx Critical Device Settings

Part Number	OUT0 Frequency (MHz)	OUT0 Format	OUT1 Frequency (MHz)	OUT1 Format	REFCLK Configuration
LMK3H0102A001	100	100Ω LP-HCSL	100	100Ω LP-HCSL	High-Z
LMK3H0102A006	24	CMOS In-Phase	25	CMOS In-Phase	50MHz
LMK3H0102A014	100	100Ω LP-HCSL	100	100Ω LP-HCSL	CLK_READY
LMK3H0102A015	100	85Ω LP-HCSL	100	85Ω LP-HCSL	50MHz
LMK3H0102A016	50	CMOS In-Phase	50	CMOS In-Phase	High-Z

Table 2-2. LMK3H0102 Configuration Orderable Part Numbers

Orderable Part Numbers	Package Type
LMK3H0102A001RERR	Large Tape & Reel
LMK3H0102A001RERT	Small Tape & Reel
LMK3H0102A006RERR	Large Tape & Reel
LMK3H0102A006RERT	Small Tape & Reel
LMK3H0102A014RERR	Large Tape & Reel
LMK3H0102A014RERT	Small Tape & Reel
LMK3H0102A015RERR	Large Tape & Reel
LMK3H0102A015RERT	Small Tape & Reel
LMK3H0102A016RERR	Large Tape & Reel
LMK3H0102A016RERT	Small Tape & Reel

3 OTP Page Configuration Overview

This section provides an overview of all selectable device settings of the LMK3H0102Axx configurations for each OTP page. Use the following tables to determine if the settings for a configuration match the application requirements. If there is not a configuration that matches the application requirements, contact TI to request creation of a new configuration.

3.1 LMK3H0102Axxx OTP Page Configurations

Any table entries below that are merged between OTP Pages are not able to be changed between OTP Pages.

Table 3-1. LMK3H0102A001 OTP Configuration

Parameter	OTP Page 0	OTP Page 1	OTP Page 2	OTP Page 3
VDD Voltage	1.8V			
OUT0 FOD Source	FOD0			
OUT0 Frequency	100MHz			
OUT0 Output Format	100Ω LP-HCSL	LVCMOS, Differential	LVCMOS, Differential	LVCMOS, Differential
OUT0 Enable	Disabled	Enabled	Enabled	Enabled
OUT0 Differential Slew Rate	1.4V/ns to 2.7V/ns			
OUT0 LP-HCSL Amplitude	755mV			
OUT0 Disable Behavior	GND			
OUT1 FOD Source	FOD0			
OUT1 Frequency	100MHz			
OUT1 Output Format	100Ω LP-HCSL	100Ω LP-HCSL	100Ω LP-HCSL	100Ω LP-HCSL
OUT1 Enable	Disabled	Enabled	Enabled	Enabled
OUT1 Differential Slew Rate	1.4V/ns to 2.7V/ns			
OUT1 LP-HCSL Amplitude	690mV			
OUT1 Disable Behavior	GND			
REF_CTRL Frequency	N/A			
REF_CTRL Behavior	High-Z			
FOD0 Frequency	200MHz			
FOD1 Frequency	200MHz			
SSC Enable	Disabled	Enabled	Enabled	Disabled
SSC Modulation Type	No SSC	Preconfigured -0.5% Down-spread	Preconfigured -0.3% Down-spread	No SSC
Pin 2 Function	I^2C Address LSB Selection			

Table 3-2. LMK3H0102A006 OTP Configuration

Parameter	OTP Page 0	OTP Page 1	OTP Page 2	OTP Page 3
VDD Voltage	3.3V			
OUT0 FOD Source	FOD0			
OUT0 Frequency	24MHz			
OUT0 Output Format	LVCMOS, In-Phase	LVCMOS, In-Phase	LVCMOS, In-Phase	LVCMOS, In-Phase
OUT0 Enable	Enabled	Enabled	Enabled	Enabled
OUT0 Differential Slew Rate	2.3V/ns to 3.5V/ns			
OUT0 LP-HCSL Amplitude	755mV			
OUT0 Disable Behavior	GND			
OUT1 FOD Source	FOD1			
OUT1 Frequency	25MHz			
OUT1 Output Format	LVCMOS, In-Phase	LVCMOS, In-Phase	LVCMOS, In-Phase	LVCMOS, In-Phase
OUT1 Enable	Enabled	Enabled	Enabled	Enabled
OUT1 Differential Slew Rate	2.3V/ns to 3.5V/ns			
OUT1 LP-HCSL Amplitude	755mV			
OUT1 Disable Behavior	GND			
REF_CTRL Frequency	50MHz			
REF_CTRL Behavior	REF_CLK			
FOD0 Frequency	144MHz			
FOD1 Frequency	200MHz			
SSC Enable	Disabled	Disabled	Disabled	Disabled
SSC Modulation Type	No SSC	No SSC	No SSC	No SSC
Pin 2 Function	I^2C Address LSB Selection			

Table 3-3. LMK3H0102A014 OTP Configuration

Parameter	OTP Page 0	OTP Page 1	OTP Page 2	OTP Page 3
VDD Voltage	3.3V			
OUT0 FOD Source	FOD0			
OUT0 Frequency	100MHz			
OUT0 Output Format	100Ω LP-HCSL	100Ω LP-HCSL	100Ω LP-HCSL	100Ω LP-HCSL
OUT0 Enable	Enabled	Disabled	Enabled	Enabled
OUT0 Differential Slew Rate	2.3V/ns to 3.5V/ns			
OUT0 LP-HCSL Amplitude	755mV			
OUT0 Disable Behavior	GND			
OUT1 FOD Source	FOD0			
OUT1 Frequency	100MHz			
OUT1 Output Format	100Ω LP-HCSL	100Ω LP-HCSL	100Ω LP-HCSL	100Ω LP-HCSL
OUT1 Enable	Disabled	Enabled	Enabled	Enabled
OUT1 Differential Slew Rate	2.3V/ns to 3.5V/ns			
OUT1 LP-HCSL Amplitude	755mV			
OUT1 Disable Behavior	GND			
REF_CTRL Frequency	N/A			
REF_CTRL Behavior	CLK_READY			
FOD0 Frequency	200MHz			
FOD1 Frequency	200MHz			
SSC Enable	Enabled	Enabled	Disabled	Enabled
SSC Modulation Type	Preconfigured -0.5% Down-spread	Preconfigured -0.5% Down-spread	Preconfigured -0.5% Down-spread	Preconfigured -0.5% Down-spread
Pin 2 Function	I^2C Address LSB Selection			

Table 3-4. LMK3H0102A015 OTP Configuration

Parameter	OTP Page 0	OTP Page 1	OTP Page 2	OTP Page 3
VDD Voltage	3.3V			
OUT0 FOD Source	FOD0			
OUT0 Frequency	100MHz			
OUT0 Output Format	85Ω LP-HCSL	85Ω LP-HCSL	85Ω LP-HCSL	85Ω LP-HCSL
OUT0 Enable	Enabled	Enabled	Enabled	Enabled
OUT0 Differential Slew Rate	2.3V/ns to 3.5V/ns			
OUT0 LP-HCSL Amplitude	755mV			
OUT0 Disable Behavior	GND			
OUT1 FOD Source	FOD0			
OUT1 Frequency	100MHz			
OUT1 Output Format	85Ω LP-HCSL	85Ω LP-HCSL	85Ω LP-HCSL	85Ω LP-HCSL
OUT1 Enable	Enabled	Enabled	Enabled	Enabled
OUT1 Differential Slew Rate	2.3V/ns to 3.5V/ns			
OUT1 LP-HCSL Amplitude	755mV			
OUT1 Disable Behavior	GND			
REF_CTRL Frequency	50MHz			
REF_CTRL Behavior	GND			
FOD0 Frequency	200MHz			
FOD1 Frequency	200MHz			
SSC Enable	Disabled	Enabled	Enabled	Enabled
SSC Modulation Type	No SSC	Preconfigured -0.1% Down-spread	Preconfigured -0.3% Down-spread	Preconfigured -0.5% Down-spread
Pin 2 Function	I^2C Address LSB Selection			

Table 3-5. LMK3H0102A016 OTP Configuration

Parameter	OTP Page 0	OTP Page 1	OTP Page 2	OTP Page 3
VDD Voltage	3.3V			
OUT0 FOD Source	FOD0			
OUT0 Frequency	50MHz			
OUT0 Output Format	LVCMOS, In-Phase	LVCMOS, P Only	LVCMOS, P Only	LVCMOS, P Only
OUT0 Enable	Disabled	Enabled	Enabled	Enabled
OUT0 Differential Slew Rate	2.3V/ns to 3.5V/ns			
OUT0 LP-HCSL Amplitude	755mV			
OUT0 Disable Behavior	GND			
OUT1 FOD Source	FOD0			
OUT1 Frequency	50MHz			
OUT1 Output Format	LVCMOS, In-Phase	LVCMOS, P Only	LVCMOS, N Only	LVCMOS, In-Phase
OUT1 Enable	Disabled	Enabled	Enabled	Enabled
OUT1 Differential Slew Rate	2.3V/ns to 3.5V/ns			
OUT1 LP-HCSL Amplitude	755mV			
OUT1 Disable Behavior	GND			
REF_CTRL Frequency	N/A			
REF_CTRL Behavior	High-Z			
FOD0 Frequency	100MHz			
FOD1 Frequency	100MHz			
SSC Enable	Disabled	Disabled	Disabled	Disabled
SSC Modulation Type	No SSC	No SSC	No SSC	No SSC
Pin 2 Function	I^2C Address LSB Selection			

4 LMK3H0102Axxx Configuration Registers

This section provides an overview of the register settings of the LMK3H0102Axx configurations. These register settings reflect the settings on OTP Page 0 only. Registers R146, R17, and R148 are for FOD calibration, and are described in the LMK3H0102 data sheet. Register R238 is for the offset code for the BAW frequency, and is described in the LMK3H0102 data sheet. FOD divider values assume that R238 is 0x0000. Any other registers in the data sheet not referred to in this document do not impact core configuration, and can be neglected.

4.1 LMK3H0102A001 Registers

4.1.1 LMK3H0102A001 R0 Register (Address = 0x0) [reset = 0x0863]

Table 4-1. R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	DIG_CLK_N_DIV	R/W	0x02	Digital State Machine clock rate. Derived from the FOD frequency sourced by the CH0_FOD_SEL multiplexer. The target for the frequency is 50MHz maximum. The actual divide value is the DIG_CLK_N_DIV value plus 2. This field is stored in the EFUSE.
9:3	FOD0_N_DIV	R/W	0x0C	Integer Ratio of BAW frequency to FOD0 frequency. This field is stored in the EFUSE.
2:1	Reserved	R	N/A	Reserved, do not write to this field.
0	OTP_BURNT	R/WL	0x1	Indicates if the EFUSE has been programmed. If this field is '1', the EFUSE is programmed.

4.1.2 LMK3H0102A001 R1 Register (Address = 0x1) [reset = 0x5599]

Table 4-2. R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	FOD0_NUM[23:16]	R/W	0x55	High byte of the FOD0 fractional divide value. The value of this field changes from device to device. This field is stored in the EFUSE.
7:0	ADC_CLK_N_DIV	R/W	0x99	ADC clock frequency in MHz, derived directly from BAW. Default is ceil(2467 / 16) - 2 = 0x99. TI does not recommend modifying the value of this field. This field is stored in the EFUSE.

4.1.3 LMK3H0102A001 R2 Register (Address = 0x2) [reset = 0xC28F]

Table 4-3. R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	FOD0_NUM[15:0]	R/W	0xC28F	Lower two bytes of the FOD0 fractional divide value. The value of this field changes from device to device. This field is stored in the EFUSE.

4.1.4 LMK3H1002A001 R3 Register (Address = 0x3) [reset = 0x1801]

Table 4-4. R3 Register Field Descriptions

Bit	Firld	Type	Reset	Description
15:9	FOD1_N_DIV	R/W	0x0C	Integer Ratio of BAW frequency to FOD1 frequency. This field is stored in the EFUSE.
8	CH1_FOD_SEL	R/W	0x0	Selects the FOD to use as the input source for Channel Divider 1. This field is stored in the EFUSE. 0h: FOD0. 1h: FOD1.

Table 4-4. R3 Register Field Descriptions (continued)

Bit	Firld	Type	Reset	Description
7	CH1_EDGE_COMB_EN	R/W	0x0	Selects between using Channel Divider 1 or using the Edge Combiner as the input source for Output Driver 1. This field is stored in the EFUSE. 0h: Channel Divider 1 input 1h: Edge Combiner input
6	OUT1_DISABLE_STATE	R/W	0x0	When OUT1 is disabled, this bit selects whether the OUT1_P and OUT1_N pins are forced to GND or tri-stated. This field is stored in the EFUSE. 0h: Forced to GND on disable. Tri-state on disable.
5	OUT0_DISABLE_STATE	R/W	0x0	When OUT0 is disabled, this bit selects whether the OUT0_P and OUT0_N pins are forced to GND or tri-stated. This field is stored in the EFUSE. 0h: Forced to GND on disable. Tri-state on disable.
4	CH0_FOD_SEL	R/W	0x0	Selects the FOD to use as the input source for Channel Divider 0. This field is stored in the EFUSE. 0h: FOD0. 1h: FOD1.
3	CH0_EDGE_COMB_EN	R/W	0x0	Selects between using Channel Divider 0 or using the Edge Combiner as the input source for Output Driver 0. This field is stored in the EFUSE. 0h: Channel Divider 0 input 1h: Edge Combiner input
2:0	CH0_DIV	R/W	0x1	Divider value for Channel Divider 0. This field is stored in the EFUSE. 0h: Channel Divider disabled. 1h: FOD / 2 2h: FOD / 4 3h: FOD / 6 4h: FOD / 8 5h: FOD / 10 6h: FOD / 20 7h: FOD / 40

4.1.5 LMK3H0102A001 R4 Register (Address = 0x4) [reset = 0x0000]

Table 4-5. R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Reserved	R	0x0	Reserved
14:2	SSC_STEPS	R/W	0x0000	Number of steps in each segment of the triangular profile for SSC. See the data sheet for instructions on how to calculate this value. This field is stored in the EFUSE.
1	SSC_MOD_TYPE	R/W	0x0	Selects between down-spread or center-spread modulation for custom SSC configurations. This field is stored in the EFUSE. 0h: Down-spread modulation. 1h: Center-spread modulation.
0	SSC_EN	R/W	0x0	Enable SSC. This field is stored in the EFUSE. 0h: SSC Disabled. 1h: SSC Enabled.

4.1.6 LMK3H0102A001 R5 Register (Address = 0x5) [reset = 0x0000]

Table 4-6. R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	SSC_STEP_SIZE	R/W	0x0000	Numerator increment value per step for SSC. This field is stored in the EFUSE.

4.1.7 LMK3H0102A001 R6 Register (Address = 0x6) [reset = 0x0AB8]

Table 4-7. R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	CH1_DIV	R/W	0x0	Divider value for Channel Divider 1. This field is stored in the EFUSE. 0h: Channel Divider disabled. Set CH1_DIV to '0' when using the edge combiner for OUT1. 1h: FOD / 2 2h: FOD / 4 3h: FOD / 6 4h: FOD / 8 5h: FOD / 10 6h: FOD / 20 7h: FOD / 40
12:5	FOD1_NUM[23:16]	R/W	0x55	High byte of the FOD1 fractional divide value. The value of this field changes from device to device. This field is stored in the EFUSE.
4:3	OUT0_SLEW_RATE	R/W	0x3	Slew rate control for OUT0. This field is stored in the EFUSE. Only applies to differential output formats. 0h: Between 2.3V/ns and 3.5V/ns. 1h: Between 2.0V/ns and 3.2V/ns. 2h: Between 1.7V/ns and 2.8V/ns. 3h: Between 1.4V/ns and 2.7V/ns.
2:0	OUT0_FMT	R/W	0x0	Selects the output format for OUT0. This field is stored in the EFUSE. 0h: LP-HCSL 100Ω Termination. 1h: LP-HCSL 85Ω Termination. 2h: AC-coupled LVDS. 3h: DC-coupled LVDS. 4h: LVCMOS, OUTx_P enabled, OUTx_N disabled. 5h: LVCMOS, OUTx_P disabled, OUTx_N enabled. 6h: LVCMOS, OUTx_P enabled, OUTx_N enabled, 180 degrees out of phase. 7h: LVCMOS, OUTx_P enabled, OUTx_N enabled, OUTx_P and OUTx_N in phase.

4.1.8 LMK3H0102A001 R7 Register (Address = 0x7) [reset = 0x2461]

Table 4-8. R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Reserved	R	0x0	Reserved
14:13	REF_CTRL_PIN_FUNC	R/W	0x1	Sets the function of the REF_CTRL pin. This field is stored in the EFUSE. 0h: REF_CTRL pin disabled, pulled to GND. 1h: REF_CTRL pin disabled, tri-state. 2h: REF_CTRL pin functions as an additional LVCMOS REF_CLK output. 3h: REF_CTRL pin functions as "clock ready" signal.
12:11	REF_CLK_DIV	R/W	0x0	REF_CLK output divisor value when REF_CTRL is used as REF_CLK. This field is stored in the EFUSE. 0h: REF_CLK disabled. 1h: FOD / 2. 2h: FOD / 4. 3h: FOD / 8.
10	Reserved	R/W	0x1	Reserved. Do not write any value other than '1' to this field.
9	REF_CLK_FOD_SEL	R/W	0x0	Select the FOD used to generate the REF_CLK output. This field is stored in the EFUSE. 0h: FOD0. 1h: FOD1.

Table 4-8. R7 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	OUT1_EN	R/W	0x0	Output Enable bit for OUT1. This field is stored in the EFUSE. 0h: OUT1 is disabled. 1h: OUT1 is enabled.
7	OUT1_CH_SEL	R/W	0x0	Selects the source for OUT1. This field is stored in the EFUSE. 0h: OUT1 is sourced from Channel Divider 0 if CH0_EDGE_COMB_EN is a '0', or the Edge Combiner if CH0_EDGE_COMB_EN is a '1'. 1h: OUT1 is sourced from Channel Divider 1 if CH1_EDGE_COMB_EN is a '0', or the Edge Combiner if CH1_EDGE_COMB_EN is a '1'.
6:5	OUT1_SLEW_RATE	R/W	0x3	Slew rate control for OUT1. This field is stored in the EFUSE. Only applies to differential output formats. 0h: Between 2.3V/ns and 3.5V/ns. 1h: Between 2.0V/ns and 3.2V/ns. 2h: Between 1.7V/ns and 2.8V/ns. 3h: Between 1.4V/ns and 2.7V/ns.
4:2	OUT1_FMT	R/W	0x0	Selects the output format for OUT1. This field is stored in the EFUSE. 0h: LP-HCSL 100Ω Termination. 1h: LP-HCSL 85Ω Termination. 2h: AC-coupled LVDS. 3h: DC-coupled LVDS. 4h: LVCMOS, OUTx_P enabled, OUTx_N disabled. 5h: LVCMOS, OUTx_P disabled, OUTx_N enabled. 6h: LVCMOS, OUTx_P enabled, OUTx_N enabled, 180 degrees out of phase. 7h: LVCMOS, OUTx_P enabled, OUTx_N enabled, OUTx_P and OUTx_N in phase.
1	OUT0_EN	R/W	0x0	Output Enable bit for OUT0. This field is stored in the EFUSE. 0h: OUT0 is disabled. 1h: OUT0 is enabled.
0	OE_PIN_POLARITY	R/W	0x1	OE pin polarity selection. This bit does not affect the polarity of the OUTx_EN bits, only the OE pin. This field is stored in the EFUSE. 0h: OE is active high (OE tied to VDD enables outputs). 1h: OE is active low (OE tied to GND enables outputs).

4.1.9 LMK3H0102A001 R8 Register (Address = 0x8) [reset = 0xC28F]

Table 4-9. R8 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	FOD1_NUM[15:0]	R/W	0xC28F	Lower two bytes of the FOD1 fractional divide value. The value of this field changes from device to device. This field is stored in the EFUSE.

4.1.10 LMK3H0102A001 R9 Register (Address = 0x9) [reset = 0x4036]

Table 4-10. R9 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	OTP_ID	R/W	0x4	Configurable field for identifying the OTP configuration. Can be used in I2C mode as a 4-bit spare field. This field is stored in the EFUSE.

Table 4-10. R9 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:9	SSC_CONFIG_SEL	R/W	0x0	SSC modulation configuration. If center-spread modulation is desired, then custom SSC configuration is required. Four preconfigured down-spread modulation depths are also available. Any other modulation depths require custom SSC configuration. This field is stored in the EFUSE. 0h: Custom SSC Configuration 1h: –0.10% preconfigured down-spread. 2h: –0.25% preconfigured down-spread. 3h: –0.30% preconfigured down-spread. 4h: –0.50% preconfigured down-spread. All other values: Reserved
8	OUT_FMT_SRC_SEL	R/W	0x0	Forces the FMT_ADDR pin to override the output format register settings in OTP Mode. When in I2C mode, the FMT_ADDR pin is never used for this purpose. This field is stored in the EFUSE. 0h: FMT_ADDR pin is ignored in OTP mode for output format selection. 1h: FMT_ADDR pin overrides the register settings. The output format is LP-HCSL, and the termination resistor values are based on the FMT_ADDR pin state on start-up.
7:4	OUT1_LPHSCL_AMP_SEL	R/W	0x3	OUT1 output swing level when using LP-HCSL output format. This field is stored in the EFUSE. 0h: 625mV. 1h: 647mV. 2h: 668mV. 3h: 690mV. 4h: 712mV. 5h: 733mV. 6h: 755mV. 7h: 777mV. 8h: 798mV. 9h: 820mV. Ah: 842mV. Bh: 863mV. Ch: 885mV. Dh: 907mV. Eh: 928mV. Fh: 950mV.

Table 4-10. R9 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	OUT0_LPHSCL_AMP_SEL	R/W	0x6	OUT0 output swing level when using LP-HCSL output format. This field is stored in the EFUSE. 0h: 625mV. 1h: 647mV. 2h: 668mV. 3h: 690mV. 4h: 712mV. 5h: 733mV. 6h: 755mV. 7h: 777mV. 8h: 798mV. 9h: 820mV. Ah: 842mV. Bh: 863mV. Ch: 885mV. Dh: 907mV. Eh: 928mV. Fh: 950mV.

4.1.11 LMK3H0102A001 R10 Register (Address = 0xA) [reset = 0x0010]

Table 4-11. R10 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Reserved	R/W	0x0	Reserved. Only write '0' to this bit.
14:11	PROD_REVID	R	0x0	Product revision identifier.
10	CLK_READY	R	0x0	CLK_READY status. The REF_CTRL pin mirrors this status signal when the pin functions as a "clock ready" signal.
9	Reserved	R	0x0	Reserved. Do not write to this field.
8	RB_PIN_15	R	0x0	Readback of the REF_CTRL pin.
7	RB_PIN_4	R	0x0	Readback of the OTP_SEL1/SDA pin.
6	RB_PIN_3	R	0x0	Readback of the OTP_SEL0/SCL pin.
5	RB_PIN_2	R	0x0	Readback of the FMT_ADDR pin.
4	DEV_IDLE_STATE_SEL	R/W	0x1	This bit controls the behavior of the device when both outputs are disabled. Placing the device into a low-power state is not recommended for PCIe applications, as the time to re-enable the clocks is extended. This field is stored in the EFUSE. 0h: When both outputs are disabled, the outputs are muted, and the device is placed into a low-power state. 1h: When both outputs are disabled, the outputs are muted. The device does not enter a low-power state.
3	PIN_RESAMPLE_DIS	R/W	0x0	This bit controls the resampling of the device pins when exiting the low power mode. Write this bit while in the low power mode. TI recommends keeping this bit as a '1' unless the functionality is explicitly desired. After PDN, pins 2, 3, 4, and 15 are resampled. Device functionality can change based on new logic level of the pins. 0h: Pin resampling is enabled. When exiting the low power mode, the FMT_ADDR, OTP_SEL0/SCL, OTP_SEL1/SDA, and FMT_ADDR pins are resampled. If FMT_ADDR is high, the device enters OTP Mode. 1h: Pin resampling is disabled. When exiting the low power mode, the FMT_ADDR, OTP_SEL0/SCL, OTP_SEL1/SDA, and FMT_ADDR pins are not resampled. The device remains in I2C Mode.

Table 4-11. R10 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	OTP_AUTOLOAD_DIS	R/W	0x0	This bit controls the behavior of the device when exiting the low power mode. Write this bit while in the low power mode. TI recommends keeping this bit as a '1' unless the functionality is explicitly desired. 0h: OTP autoload is enabled. When exiting the low power mode, the contents of OTP Page 0 are written to the device registers. 1h: OTP autoload is disabled. When exiting the low power mode, the contents of OTP Page 0 are not written to the device registers.
1	PDN	R/W	0x0	Writing a '1' to this bit puts the device into a low power state.
0	Reserved	R/W	0x0	Reserved, do not write to this field.

4.1.12 LMK3H0102A001 R11 Register (Address = 0xB) [reset = 0x0000]

Table 4-12. R11 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Reserved	R/W	0x0	Reserved, only write '0' to this field.
14	SEPARATE_OE_EN	R/W	0x0	This bit enables the separate output enable functionality of the device. If this bit is a '1', then OUT_FMT_SRC_SEL and I2C_ADDR_LSB_SEL must be set to '0'. This field is stored in the EFUSE. 0h: Pin 1 is the output enable for OUT0 and OUT1. 1h: Pin 1 is the output enable for OUT0, Pin 2 is the output enable for OUT1.
13:0	Reserved	R/W	0x0000	Reserved, only write '0' to this field.

4.1.13 LMK3H0102A001 R12 Register (Address = 0xC) [reset = 0xE800]

Table 4-13. R12 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	I2C_ADDR_LSB_SEL	R/WL	0x1	I2C peripheral address source. If this bit is a '1', SEPARATE_OE_EN must be '0'. This field is stored in the EFUSE. 0h: I2C peripheral address comes entirely from the I2C_ADDR field. 1h: The two lowest bits of the I2C peripheral address come from the FMT_ADDR pin, all other bits come from R12[14:10].
14:8	I2C_ADDR	R/WL	0x68	I2C peripheral address. After writing to this field, the device responds to the new I2C address. This field is stored in the EFUSE.
7:0	UNLOCK_PROTECTED_REG	R/W	0x00	This field locks all registers from R13 onward, in addition to R12[15:8]. Registers R13 onward are largely device calibration registers, and must not have contents modified. These registers can be read from normally regardless of the unlock status. 5Bh: Unlocks register writes for R12[15:8] and above. Any other value: R12[15:8] and above ignore all writes.

4.2 LMK3H0102A006 Registers

4.2.1 LMK3H0102A006 R0 Register (Address = 0x0) [reset = 0x0489]

Table 4-14. R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	DIG_CLK_N_DIV	R/W	0x01	Digital State Machine clock rate. Derived from the FOD frequency sourced by the CH0_FOD_SEL multiplexer. The target for the frequency is 50MHz maximum. The actual divide value is the DIG_CLK_N_DIV value plus 2. This field is stored in the EFUSE.
9:3	FOD0_N_DIV	R/W	0x11	Integer Ratio of BAW frequency to FOD0 frequency. This field is stored in the EFUSE.
2:1	Reserved	R	N/A	Reserved, do not write to this field.
0	OTP_BURNT	R/WL	0x1	Indicates if the EFUSE has been programmed. If this field is '1', the EFUSE is programmed.

4.2.2 LMK3H0102A006 R1 Register (Address = 0x1) [reset = 0x2199]

Table 4-15. R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	FOD0_NUM[23:16]	R/W	0x21	High byte of the FOD0 fractional divide value. The value of this field changes from device to device. This field is stored in the EFUSE.
7:0	ADC_CLK_N_DIV	R/W	0x99	ADC clock frequency in MHz, derived directly from BAW. Default is ceil(2467 / 16) - 2 = 0x99. TI does not recommend modifying the value of this field. This field is stored in the EFUSE.

4.2.3 LMK3H0102A006 R2 Register (Address = 0x2) [reset = 0xC71C]

Table 4-16. R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	FOD0_NUM[15:0]	R/W	0xC71C	Lower two bytes of the FOD0 fractional divide value. The value of this field changes from device to device. This field is stored in the EFUSE.

4.2.4 LMK3H1002A006 R3 Register (Address = 0x3) [reset = 0x1903]

Table 4-17. R3 Register Field Descriptions

Bit	Firld	Type	Reset	Description
15:9	FOD1_N_DIV	R/W	0x0C	Integer Ratio of BAW frequency to FOD1 frequency. This field is stored in the EFUSE.
8	CH1_FOD_SEL	R/W	0x1	Selects the FOD to use as the input source for Channel Divider 1. This field is stored in the EFUSE. 0h: FOD0. 1h: FOD1.
7	CH1_EDGE_COMB_EN	R/W	0x0	Selects between using Channel Divider 1 or using the Edge Combiner as the input source for Output Driver 1. This field is stored in the EFUSE. 0h: Channel Divider 1 input 1h: Edge Combiner input
6	OUT1_DISABLE_STATE	R/W	0x0	When OUT1 is disabled, this bit selects whether the OUT1_P and OUT1_N pins are forced to GND or tri-stated. This field is stored in the EFUSE. 0h: Forced to GND on disable. 1h: Tri-state on disable.

Table 4-17. R3 Register Field Descriptions (continued)

Bit	Firld	Type	Reset	Description
5	OUT0_DISABLE_STATE	R/W	0x0	When OUT0 is disabled, this bit selects whether the OUT0_P and OUT0_N pins are forced to GND or tri-stated. This field is stored in the EFUSE. 0h: Forced to GND on disable. 1h: Tri-state on disable.
4	CH0_FOD_SEL	R/W	0x0	Selects the FOD to use as the input source for Channel Divider 0. This field is stored in the EFUSE. 0h: FOD0. 1h: FOD1.
3	CH0_EDGE_COMB_EN	R/W	0x0	Selects between using Channel Divider 0 or using the Edge Combiner as the input source for Output Driver 0. This field is stored in the EFUSE. 0h: Channel Divider 0 input 1h: Edge Combiner input
2:0	CH0_DIV	R/W	0x3	Divider value for Channel Divider 0. This field is stored in the EFUSE. 0h: Channel Divider disabled. 1h: FOD / 2 2h: FOD / 4 3h: FOD / 6 4h: FOD / 8 5h: FOD / 10 6h: FOD / 20 7h: FOD / 40

4.2.5 LMK3H0102A006 R4 Register (Address = 0x4) [reset = 0x0000]

Table 4-18. R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Reserved	R	0x0	Reserved
14:2	SSC_STEPS	R/W	0x0000	Number of steps in each segment of the triangular profile for SSC. See the data sheet for instructions on how to calculate this value. This field is stored in the EFUSE.
1	SSC_MOD_TYPE	R/W	0x0	Selects between down-spread or center-spread modulation for custom SSC configurations. This field is stored in the EFUSE. 0h: Down-spread modulation. 1h: Center-spread modulation.
0	SSC_EN	R/W	0x0	Enable SSC. This field is stored in the EFUSE. 0h: SSC Disabled. 1h: SSC Enabled.

4.2.6 LMK3H0102A014 R5 Register (Address = 0x5) [reset = 0x0000]

Table 4-19. R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	SSC_STEP_SIZE	R/W	0x0000	Numerator increment value per step for SSC. This field is stored in the EFUSE.

4.2.7 LMK3H0102A006 R6 Register (Address = 0x6) [reset = 0x8AA7]

Table 4-20. R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	CH1_DIV	R/W	0x4	Divider value for Channel Divider 1. This field is stored in the EFUSE. 0h: Channel Divider disabled. Set CH1_DIV to '0' when using the edge combiner for OUT1. 1h: FOD / 2 2h: FOD / 4 3h: FOD / 6 4h: FOD / 8 5h: FOD / 10 6h: FOD / 20 7h: FOD / 40
12:5	FOD1_NUM[23:16]	R/W	0x55	High byte of the FOD1 fractional divide value. The value of this field changes from device to device. This field is stored in the EFUSE.
4:3	OUT0_SLEW_RATE	R/W	0x0	Slew rate control for OUT0. This field is stored in the EFUSE. Only applies to differential output formats. 0h: Between 2.3V/ns and 3.5V/ns. 1h: Between 2.0V/ns and 3.2V/ns. 2h: Between 1.7V/ns and 2.8V/ns. 3h: Between 1.4V/ns and 2.7V/ns.
2:0	OUT0_FMT	R/W	0x7	Selects the output format for OUT0. This field is stored in the EFUSE. 0h: LP-HCSL 100Ω Termination. 1h: LP-HCSL 85Ω Termination. 2h: AC-coupled LVDS. 3h: DC-coupled LVDS. 4h: LVCMOS, OUTx_P enabled, OUTx_N disabled. 5h: LVCMOS, OUTx_P disabled, OUTx_N enabled. 6h: LVCMOS, OUTx_P enabled, OUTx_N enabled, 180 degrees out of phase. 7h: LVCMOS, OUTx_P enabled, OUTx_N enabled, OUTx_P and OUTx_N in phase.

4.2.8 LMK3H0102A006 R7 Register (Address = 0x7) [reset = 0x579F]

Table 4-21. R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Reserved	R	0x0	Reserved
14:13	REF_CTRL_PIN_FUNC	R/W	0x2	Sets the function of the REF_CTRL pin. This field is stored in the EFUSE. 0h: REF_CTRL pin disabled, pulled to GND. 1h: REF_CTRL pin disabled, tri-state. 2h: REF_CTRL pin functions as an additional LVCMOS REF_CLK output. 3h: REF_CTRL pin functions as "clock ready" signal.
12:11	REF_CLK_DIV	R/W	0x2	REF_CLK output divisor value when REF_CTRL is used as REF_CLK. This field is stored in the EFUSE. 0h: REF_CLK disabled. 1h: FOD / 2. 2h: FOD / 4. 3h: FOD / 8.
10	Reserved	R/W	0x1	Reserved. Do not write any value other than '1' to this field.
9	REF_CLK_FOD_SEL	R/W	0x1	Select the FOD used to generate the REF_CLK output. This field is stored in the EFUSE. 0h: FOD0. 1h: FOD1.

Table 4-21. R7 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	OUT1_EN	R/W	0x1	Output Enable bit for OUT1. This field is stored in the EFUSE. 0h: OUT1 is disabled. 1h: OUT1 is enabled.
7	OUT1_CH_SEL	R/W	0x1	Selects the source for OUT1. This field is stored in the EFUSE. 0h: OUT1 is sourced from Channel Divider 0 if CH0_EDGE_COMB_EN is a '0', or the Edge Combiner if CH0_EDGE_COMB_EN is a '1'. 1h: OUT1 is sourced from Channel Divider 1 if CH1_EDGE_COMB_EN is a '0', or the Edge Combiner if CH1_EDGE_COMB_EN is a '1'.
6:5	OUT1_SLEW_RATE	R/W	0x0	Slew rate control for OUT1. This field is stored in the EFUSE. Only applies to differential output formats. 0h: Between 2.3V/ns and 3.5V/ns. 1h: Between 2.0V/ns and 3.2V/ns. 2h: Between 1.7V/ns and 2.8V/ns. 3h: Between 1.4V/ns and 2.7V/ns.
4:2	OUT1_FMT	R/W	0x7	Selects the output format for OUT1. This field is stored in the EFUSE. 0h: LP-HCSL 100Ω Termination. 1h: LP-HCSL 85Ω Termination. 2h: AC-coupled LVDS. 3h: DC-coupled LVDS. 4h: LVCMOS, OUTx_P enabled, OUTx_N disabled. 5h: LVCMOS, OUTx_P disabled, OUTx_N enabled. 6h: LVCMOS, OUTx_P enabled, OUTx_N enabled, 180 degrees out of phase. 7h: LVCMOS, OUTx_P enabled, OUTx_N enabled, OUTx_P and OUTx_N in phase.
1	OUT0_EN	R/W	0x1	Output Enable bit for OUT0. This field is stored in the EFUSE. 0h: OUT0 is disabled. 1h: OUT0 is enabled.
0	OE_PIN_POLARITY	R/W	0x1	OE pin polarity selection. This bit does not affect the polarity of the OUTx_EN bits, only the OE pin. This field is stored in the EFUSE. 0h: OE is active high (OE tied to VDD enables outputs). 1h: OE is active low (OE tied to GND enables outputs).

4.2.9 LMK3H0102A006 R8 Register (Address = 0x8) [reset = 0xC28F]

Table 4-22. R8 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	FOD1_NUM[15:0]	R/W	0xC28F	Lower two bytes of the FOD1 fractional divide value. The value of this field changes from device to device. This field is stored in the EFUSE.

4.2.10 LMK3H0102A006 R9 Register (Address = 0x9) [reset = 0xD066]

Table 4-23. R9 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	OTP_ID	R/W	0xD	Configurable field for identifying the OTP configuration. Can be used in I2C mode as a 4-bit spare field. This field is stored in the EFUSE.

Table 4-23. R9 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:9	SSC_CONFIG_SEL	R/W	0x0	SSC modulation configuration. If center-spread modulation is desired, then custom SSC configuration is required. Four preconfigured down-spread modulation depths are also available. Any other modulation depths require custom SSC configuration. This field is stored in the EFUSE. 0h: Custom SSC Configuration 1h: –0.10% preconfigured down-spread. 2h: –0.25% preconfigured down-spread. 3h: –0.30% preconfigured down-spread. 4h: –0.50% preconfigured down-spread. All other values: Reserved
8	OUT_FMT_SRC_SEL	R/W	0x0	Forces the FMT_ADDR pin to override the output format register settings in OTP Mode. When in I2C mode, the FMT_ADDR pin is never used for this purpose. This field is stored in the EFUSE. 0h: FMT_ADDR pin is ignored in OTP mode for output format selection. 1h: FMT_ADDR pin overrides the register settings. The output format is LP-HCSL, and the termination resistor values are based on the FMT_ADDR pin state on start-up.
7:4	OUT1_LPHSCL_AMP_SEL	R/W	0x6	OUT1 output swing level when using LP-HCSL output format. This field is stored in the EFUSE. 0h: 625mV. 1h: 647mV. 2h: 668mV. 3h: 690mV. 4h: 712mV. 5h: 733mV. 6h: 755mV. 7h: 777mV. 8h: 798mV. 9h: 820mV. Ah: 842mV. Bh: 863mV. Ch: 885mV. Dh: 907mV. Eh: 928mV. Fh: 950mV.

Table 4-23. R9 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	OUT0_LPHSCL_AMP_SEL	R/W	0x6	OUT0 output swing level when using LP-HCSL output format. This field is stored in the EFUSE. 0h: 625mV. 1h: 647mV. 2h: 668mV. 3h: 690mV. 4h: 712mV. 5h: 733mV. 6h: 755mV. 7h: 777mV. 8h: 798mV. 9h: 820mV. Ah: 842mV. Bh: 863mV. Ch: 885mV. Dh: 907mV. Eh: 928mV. Fh: 950mV.

4.2.11 LMK3H0102A006 R10 Register (Address = 0xA) [reset = 0x0010]

Table 4-24. R10 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Reserved	R/W	0x0	Reserved. Only write '0' to this bit.
14:11	PROD_REVID	R	0x0	Product revision identifier.
10	CLK_READY	R	0x0	CLK_READY status. The REF_CTRL pin mirrors this status signal when the pin functions as a "clock ready" signal.
9	Reserved	R	0x0	Reserved. Do not write to this field.
8	RB_PIN_15	R	0x0	Readback of the REF_CTRL pin.
7	RB_PIN_4	R	0x0	Readback of the OTP_SEL1/SDA pin.
6	RB_PIN_3	R	0x0	Readback of the OTP_SEL0/SCL pin.
5	RB_PIN_2	R	0x0	Readback of the FMT_ADDR pin.
4	DEV_IDLE_STATE_SEL	R/W	0x1	This bit controls the behavior of the device when both outputs are disabled. Placing the device into a low-power state is not recommended for PCIe applications, as the time to re-enable the clocks is extended. This field is stored in the EFUSE. 0h: When both outputs are disabled, the outputs are muted, and the device is placed into a low-power state. 1h: When both outputs are disabled, the outputs are muted. The device does not enter a low-power state.
3	PIN_RESAMPLE_DIS	R/W	0x0	This bit controls the resampling of the device pins when exiting the low power mode. Write this bit while in the low power mode. TI recommends keeping this bit as a '1' unless the functionality is explicitly desired. After PDN, pins 2, 3, 4, and 15 are resampled. Device functionality can change based on new logic level of the pins. 0h: Pin resampling is enabled. When exiting the low power mode, the FMT_ADDR, OTP_SEL0/SCL, OTP_SEL1/SDA, and FMT_ADDR pins are resampled. If FMT_ADDR is high, the device enters OTP Mode. 1h: Pin resampling is disabled. When exiting the low power mode, the FMT_ADDR, OTP_SEL0/SCL, OTP_SEL1/SDA, and FMT_ADDR pins are not resampled. The device remains in I2C Mode.

Table 4-24. R10 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	OTP_AUTOLOAD_DIS	R/W	0x0	This bit controls the behavior of the device when exiting the low power mode. Write this bit while in the low power mode. TI recommends keeping this bit as a '1' unless the functionality is explicitly desired. 0h: OTP autoload is enabled. When exiting the low power mode, the contents of OTP Page 0 are written to the device registers. 1h: OTP autoload is disabled. When exiting the low power mode, the contents of OTP Page 0 are not written to the device registers.
1	PDN	R/W	0x0	Writing a '1' to this bit puts the device into a low power state.
0	Reserved	R/W	0x0	Reserved, do not write to this field.

4.2.12 LMK3H0102A006 R11 Register (Address = 0xB) [reset = 0x0000]

Table 4-25. R11 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Reserved	R/W	0x0	Reserved, only write '0' to this field.
14	SEPARATE_OE_EN	R/W	0x0	This bit enables the separate output enable functionality of the device. If this bit is a '1', then OUT_FMT_SRC_SEL and I2C_ADDR_LSB_SEL must be set to '0'. This field is stored in the EFUSE. 0h: Pin 1 is the output enable for OUT0 and OUT1. 1h: Pin 1 is the output enable for OUT0, Pin 2 is the output enable for OUT1.
13:0	Reserved	R/W	0x0000	Reserved, only write '0' to this field.

4.2.13 LMK3H0102A006 R12 Register (Address = 0xC) [reset = 0xE800]

Table 4-26. R12 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	I2C_ADDR_LSB_SEL	R/WL	0x1	I2C peripheral address source. If this bit is a '1', SEPARATE_OE_EN must be '0'. This field is stored in the EFUSE. 0h: I2C peripheral address comes entirely from the I2C_ADDR field. 1h: The two lowest bits of the I2C peripheral address come from the FMT_ADDR pin, all other bits come from R12[14:10].
14:8	I2C_ADDR	R/WL	0x68	I2C peripheral address. After writing to this field, the device responds to the new I2C address. This field is stored in the EFUSE.
7:0	UNLOCK_PROTECTED_REG	R/W	0x00	This field locks all registers from R13 onward, in addition to R12[15:8]. Registers R13 onward are largely device calibration registers, and must not have contents modified. These registers can be read from normally regardless of the unlock status. 5Bh: Unlocks register writes for R12[15:8] and above. Any other value: R12[15:8] and above ignore all writes.

4.3 LMK3H0102A014 Registers

4.3.1 LMK3H0102A014 R0 Register (Address = 0x0) [reset = 0x0861]

Table 4-27. R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	DIG_CLK_N_DIV	R/W	0x02	Digital State Machine clock rate. Derived from the FOD frequency sourced by the CH0_FOD_SEL multiplexer. The target for the frequency is 50MHz maximum. The actual divide value is the DIG_CLK_N_DIV value plus 2. This field is stored in the EFUSE.
9:3	FOD0_N_DIV	R/W	0x0C	Integer Ratio of BAW frequency to FOD0 frequency. This field is stored in the EFUSE.
2:1	Reserved	R	N/A	Reserved, do not write to this field.
0	OTP_BURNT	R/WL	0x1	Indicates if the EFUSE has been programmed. If this field is '1', the EFUSE is programmed.

4.3.2 LMK3H0102A014 R1 Register (Address = 0x1) [reset = 0x5599]

Table 4-28. R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	FOD0_NUM[23:16]	R/W	0x55	High byte of the FOD0 fractional divide value. The value of this field changes from device to device. This field is stored in the EFUSE.
7:0	ADC_CLK_N_DIV	R/W	0x99	ADC clock frequency in MHz, derived directly from BAW. Default is ceil(2467 / 16) - 2 = 0x99. TI does not recommend modifying the value of this field. This field is stored in the EFUSE.

4.3.3 LMK3H0102A014 R2 Register (Address = 0x2) [reset = 0xC28F]

Table 4-29. R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	FOD0_NUM[15:0]	R/W	0xC28F	Lower two bytes of the FOD0 fractional divide value. The value of this field changes from device to device. This field is stored in the EFUSE.

4.3.4 LMK3H1002A014 R3 Register (Address = 0x3) [reset = 0x1801]

Table 4-30. R3 Register Field Descriptions

Bit	Firld	Type	Reset	Description
15:9	FOD1_N_DIV	R/W	0x0C	Integer Ratio of BAW frequency to FOD1 frequency. This field is stored in the EFUSE.
8	CH1_FOD_SEL	R/W	0x0	Selects the FOD to use as the input source for Channel Divider 1. This field is stored in the EFUSE. 0h: FOD0. 1h: FOD1.
7	CH1_EDGE_COMB_EN	R/W	0x0	Selects between using Channel Divider 1 or using the Edge Combiner as the input source for Output Driver 1. This field is stored in the EFUSE. 0h: Channel Divider 1 input 1h: Edge Combiner input
6	OUT1_DISABLE_STATE	R/W	0x0	When OUT1 is disabled, this bit selects whether the OUT1_P and OUT1_N pins are forced to GND or tri-stated. This field is stored in the EFUSE. 0h: Forced to GND on disable. Tri-state on disable.

Table 4-30. R3 Register Field Descriptions (continued)

Bit	Firld	Type	Reset	Description
5	OUT0_DISABLE_STATE	R/W	0x0	When OUT0 is disabled, this bit selects whether the OUT0_P and OUT0_N pins are forced to GND or tri-stated. This field is stored in the EFUSE. 0h: Forced to GND on disable. Tri-state on disable.
4	CH0_FOD_SEL	R/W	0x0	Selects the FOD to use as the input source for Channel Divider 0. This field is stored in the EFUSE. 0h: FOD0. 1h: FOD1.
3	CH0_EDGE_COMB_EN	R/W	0x0	Selects between using Channel Divider 0 or using the Edge Combiner as the input source for Output Driver 0. This field is stored in the EFUSE. 0h: Channel Divider 0 input 1h: Edge Combiner input
2:0	CH0_DIV	R/W	0x1	Divider value for Channel Divider 0. This field is stored in the EFUSE. 0h: Channel Divider disabled. 1h: FOD / 2 2h: FOD / 4 3h: FOD / 6 4h: FOD / 8 5h: FOD / 10 6h: FOD / 20 7h: FOD / 40

4.3.5 LMK3H0102A014 R4 Register (Address = 0x4) [reset = 0x0001]

Table 4-31. R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Reserved	R	0x0	Reserved
14:2	SSC_STEPS	R/W	0x0000	Number of steps in each segment of the triangular profile for SSC. See the data sheet for instructions on how to calculate this value. This field is stored in the EFUSE.
1	SSC_MOD_TYPE	R/W	0x0	Selects between down-spread or center-spread modulation for custom SSC configurations. This field is stored in the EFUSE. 0h: Down-spread modulation. 1h: Center-spread modulation.
0	SSC_EN	R/W	0x1	Enable SSC. This field is stored in the EFUSE. 0h: SSC Disabled. 1h: SSC Enabled.

4.3.6 LMK3H0102A014 R5 Register (Address = 0x5) [reset = 0x0000]

Table 4-32. R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	SSC_STEP_SIZE	R/W	0x0000	Numerator increment value per step for SSC. This field is stored in the EFUSE.

4.3.7 LMK3H0102A014 R6 Register (Address = 0x6) [reset = 0x0AA0]

Table 4-33. R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	CH1_DIV	R/W	0x0	Divider value for Channel Divider 1. This field is stored in the EFUSE. 0h: Channel Divider disabled. Set CH1_DIV to '0' when using the edge combiner for OUT1. 1h: FOD / 2 2h: FOD / 4 3h: FOD / 6 4h: FOD / 8 5h: FOD / 10 6h: FOD / 20 7h: FOD / 40
12:5	FOD1_NUM[23:16]	R/W	0x55	High byte of the FOD1 fractional divide value. The value of this field changes from device to device. This field is stored in the EFUSE.
4:3	OUT0_SLEW_RATE	R/W	0x0	Slew rate control for OUT0. This field is stored in the EFUSE. Only applies to differential output formats. 0h: Between 2.3V/ns and 3.5V/ns. 1h: Between 2.0V/ns and 3.2V/ns. 2h: Between 1.7V/ns and 2.8V/ns. 3h: Between 1.4V/ns and 2.7V/ns.
2:0	OUT0_FMT	R/W	0x0	Selects the output format for OUT0. This field is stored in the EFUSE. 0h: LP-HCSL 100Ω Termination. 1h: LP-HCSL 85Ω Termination. 2h: AC-coupled LVDS. 3h: DC-coupled LVDS. 4h: LVCMOS, OUTx_P enabled, OUTx_N disabled. 5h: LVCMOS, OUTx_P disabled, OUTx_N enabled. 6h: LVCMOS, OUTx_P enabled, OUTx_N enabled, 180 degrees out of phase. 7h: LVCMOS, OUTx_P enabled, OUTx_N enabled, OUTx_P and OUTx_N in phase.

4.3.8 LMK3H0102A014 R7 Register (Address = 0x7) [reset = 0x6403]

Table 4-34. R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Reserved	R	0x0	Reserved
14:13	REF_CTRL_PIN_FUNC	R/W	0x3	Sets the function of the REF_CTRL pin. This field is stored in the EFUSE. 0h: REF_CTRL pin disabled, pulled to GND. 1h: REF_CTRL pin disabled, tri-state. 2h: REF_CTRL pin functions as an additional LVCMOS REF_CLK output. 3h: REF_CTRL pin functions as "clock ready" signal.
12:11	REF_CLK_DIV	R/W	0x0	REF_CLK output divisor value when REF_CTRL is used as REF_CLK. This field is stored in the EFUSE. 0h: REF_CLK disabled. 1h: FOD / 2. 2h: FOD / 4. 3h: FOD / 8.
10	Reserved	R/W	0x1	Reserved. Do not write any value other than '1' to this field.
9	REF_CLK_FOD_SEL	R/W	0x0	Select the FOD used to generate the REF_CLK output. This field is stored in the EFUSE. 0h: FOD0. 1h: FOD1.

Table 4-34. R7 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	OUT1_EN	R/W	0x0	Output Enable bit for OUT1. This field is stored in the EFUSE. 0h: OUT1 is disabled. 1h: OUT1 is enabled.
7	OUT1_CH_SEL	R/W	0x0	Selects the source for OUT1. This field is stored in the EFUSE. 0h: OUT1 is sourced from Channel Divider 0 if CH0_EDGE_COMB_EN is a '0', or the Edge Combiner if CH0_EDGE_COMB_EN is a '1'. 1h: OUT1 is sourced from Channel Divider 1 if CH1_EDGE_COMB_EN is a '0', or the Edge Combiner if CH1_EDGE_COMB_EN is a '1'.
6:5	OUT1_SLEW_RATE	R/W	0x0	Slew rate control for OUT1. This field is stored in the EFUSE. Only applies to differential output formats. 0h: Between 2.3V/ns and 3.5V/ns. 1h: Between 2.0V/ns and 3.2V/ns. 2h: Between 1.7V/ns and 2.8V/ns. 3h: Between 1.4V/ns and 2.7V/ns.
4:2	OUT1_FMT	R/W	0x0	Selects the output format for OUT1. This field is stored in the EFUSE. 0h: LP-HCSL 100Ω Termination. 1h: LP-HCSL 85Ω Termination. 2h: AC-coupled LVDS. 3h: DC-coupled LVDS. 4h: LVCMOS, OUTx_P enabled, OUTx_N disabled. 5h: LVCMOS, OUTx_P disabled, OUTx_N enabled. 6h: LVCMOS, OUTx_P enabled, OUTx_N enabled, 180 degrees out of phase. 7h: LVCMOS, OUTx_P enabled, OUTx_N enabled, OUTx_P and OUTx_N in phase.
1	OUT0_EN	R/W	0x1	Output Enable bit for OUT0. This field is stored in the EFUSE. 0h: OUT0 is disabled. 1h: OUT0 is enabled.
0	OE_PIN_POLARITY	R/W	0x1	OE pin polarity selection. This bit does not affect the polarity of the OUTx_EN bits, only the OE pin. This field is stored in the EFUSE. 0h: OE is active high (OE tied to VDD enables outputs). 1h: OE is active low (OE tied to GND enables outputs).

4.3.9 LMK3H0102A014 R8 Register (Address = 0x8) [reset = 0xC28F]

Table 4-35. R8 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	FOD1_NUM[15:0]	R/W	0xC28F	Lower two bytes of the FOD1 fractional divide value. The value of this field changes from device to device. This field is stored in the EFUSE.

4.3.10 LMK3H0102A014 R9 Register (Address = 0x9) [reset = 0x4866]

Table 4-36. R9 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	OTP_ID	R/W	0x4	Configurable field for identifying the OTP configuration. Can be used in I2C mode as a 4-bit spare field. This field is stored in the EFUSE.

Table 4-36. R9 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:9	SSC_CONFIG_SEL	R/W	0x4	SSC modulation configuration. If center-spread modulation is desired, then custom SSC configuration is required. Four preconfigured down-spread modulation depths are also available. Any other modulation depths require custom SSC configuration. This field is stored in the EFUSE. 0h: Custom SSC Configuration 1h: –0.10% preconfigured down-spread. 2h: –0.25% preconfigured down-spread. 3h: –0.30% preconfigured down-spread. 4h: –0.50% preconfigured down-spread. All other values: Reserved
8	OUT_FMT_SRC_SEL	R/W	0x0	Forces the FMT_ADDR pin to override the output format register settings in OTP Mode. When in I2C mode, the FMT_ADDR pin is never used for this purpose. This field is stored in the EFUSE. 0h: FMT_ADDR pin is ignored in OTP mode for output format selection. 1h: FMT_ADDR pin overrides the register settings. The output format is LP-HCSL, and the termination resistor values are based on the FMT_ADDR pin state on start-up.
7:4	OUT1_LPHSCL_AMP_SEL	R/W	0x6	OUT1 output swing level when using LP-HCSL output format. This field is stored in the EFUSE. 0h: 625mV. 1h: 647mV. 2h: 668mV. 3h: 690mV. 4h: 712mV. 5h: 733mV. 6h: 755mV. 7h: 777mV. 8h: 798mV. 9h: 820mV. Ah: 842mV. Bh: 863mV. Ch: 885mV. Dh: 907mV. Eh: 928mV. Fh: 950mV.

Table 4-36. R9 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	OUT0_LPHSCL_AMP_SEL	R/W	0x6	OUT0 output swing level when using LP-HCSL output format. This field is stored in the EFUSE. 0h: 625mV. 1h: 647mV. 2h: 668mV. 3h: 690mV. 4h: 712mV. 5h: 733mV. 6h: 755mV. 7h: 777mV. 8h: 798mV. 9h: 820mV. Ah: 842mV. Bh: 863mV. Ch: 885mV. Dh: 907mV. Eh: 928mV. Fh: 950mV.

4.3.11 LMK3H0102A014 R10 Register (Address = 0xA) [reset = 0x0010]

Table 4-37. R10 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Reserved	R/W	0x0	Reserved. Only write '0' to this bit.
14:11	PROD_REVID	R	0x0	Product revision identifier.
10	CLK_READY	R	0x0	CLK_READY status. The REF_CTRL pin mirrors this status signal when the pin functions as a "clock ready" signal.
9	Reserved	R	0x0	Reserved. Do not write to this field.
8	RB_PIN_15	R	0x0	Readback of the REF_CTRL pin.
7	RB_PIN_4	R	0x0	Readback of the OTP_SEL1/SDA pin.
6	RB_PIN_3	R	0x0	Readback of the OTP_SEL0/SCL pin.
5	RB_PIN_2	R	0x0	Readback of the FMT_ADDR pin.
4	DEV_IDLE_STATE_SEL	R/W	0x1	This bit controls the behavior of the device when both outputs are disabled. Placing the device into a low-power state is not recommended for PCIe applications, as the time to re-enable the clocks is extended. This field is stored in the EFUSE. 0h: When both outputs are disabled, the outputs are muted, and the device is placed into a low-power state. 1h: When both outputs are disabled, the outputs are muted. The device does not enter a low-power state.
3	PIN_RESAMPLE_DIS	R/W	0x0	This bit controls the resampling of the device pins when exiting the low power mode. Write this bit while in the low power mode. TI recommends keeping this bit as a '1' unless the functionality is explicitly desired. After PDN, pins 2, 3, 4, and 15 are resampled. Device functionality can change based on new logic level of the pins. 0h: Pin resampling is enabled. When exiting the low power mode, the FMT_ADDR, OTP_SEL0/SCL, OTP_SEL1/SDA, and FMT_ADDR pins are resampled. If FMT_ADDR is high, the device enters OTP Mode. 1h: Pin resampling is disabled. When exiting the low power mode, the FMT_ADDR, OTP_SEL0/SCL, OTP_SEL1/SDA, and FMT_ADDR pins are not resampled. The device remains in I2C Mode.

Table 4-37. R10 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	OTP_AUTOLOAD_DIS	R/W	0x0	This bit controls the behavior of the device when exiting the low power mode. Write this bit while in the low power mode. TI recommends keeping this bit as a '1' unless the functionality is explicitly desired. 0h: OTP autoload is enabled. When exiting the low power mode, the contents of OTP Page 0 are written to the device registers. 1h: OTP autoload is disabled. When exiting the low power mode, the contents of OTP Page 0 are not written to the device registers.
1	PDN	R/W	0x0	Writing a '1' to this bit puts the device into a low power state.
0	Reserved	R/W	0x0	Reserved, do not write to this field.

4.3.12 LMK3H0102A014 R11 Register (Address = 0xB) [reset = 0x0000]

Table 4-38. R11 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Reserved	R/W	0x0	Reserved, only write '0' to this field.
14	SEPARATE_OE_EN	R/W	0x0	This bit enables the separate output enable functionality of the device. If this bit is a '1', then OUT_FMT_SRC_SEL and I2C_ADDR_LSB_SEL must be set to '0'. This field is stored in the EFUSE. 0h: Pin 1 is the output enable for OUT0 and OUT1. 1h: Pin 1 is the output enable for OUT0, Pin 2 is the output enable for OUT1.
13:0	Reserved	R/W	0x0000	Reserved, only write '0' to this field.

4.3.13 LMK3H0102A014 R12 Register (Address = 0xC) [reset = 0xE800]

Table 4-39. R12 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	I2C_ADDR_LSB_SEL	R/WL	0x1	I2C peripheral address source. If this bit is a '1', SEPARATE_OE_EN must be '0'. This field is stored in the EFUSE. 0h: I2C peripheral address comes entirely from the I2C_ADDR field. 1h: The two lowest bits of the I2C peripheral address come from the FMT_ADDR pin, all other bits come from R12[14:10].
14:8	I2C_ADDR	R/WL	0x68	I2C peripheral address. After writing to this field, the device responds to the new I2C address. This field is stored in the EFUSE.
7:0	UNLOCK_PROTECTED_REG	R/W	0x00	This field locks all registers from R13 onward, in addition to R12[15:8]. Registers R13 onward are largely device calibration registers, and must not have contents modified. These registers can be read from normally regardless of the unlock status. 5Bh: Unlocks register writes for R12[15:8] and above. Any other value: R12[15:8] and above ignore all writes.

4.4 LMK3H0102A015 Registers

4.4.1 LMK3H0102A015 R0 Register (Address = 0x0) [reset = 0x0861]

Table 4-40. R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	DIG_CLK_N_DIV	R/W	0x02	Digital State Machine clock rate. Derived from the FOD frequency sourced by the CH0_FOD_SEL multiplexer. The target for the frequency is 50MHz maximum. The actual divide value is the DIG_CLK_N_DIV value plus 2. This field is stored in the EFUSE.
9:3	FOD0_N_DIV	R/W	0x0C	Integer Ratio of BAW frequency to FOD0 frequency. This field is stored in the EFUSE.
2:1	Reserved	R	N/A	Reserved, do not write to this field.
0	OTP_BURNT	R/WL	0x1	Indicates if the EFUSE has been programmed. If this field is '1', the EFUSE is programmed.

4.4.2 LMK3H0102A015 R1 Register (Address = 0x1) [reset = 0x5599]

Table 4-41. R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	FOD0_NUM[23:16]	R/W	0x55	High byte of the FOD0 fractional divide value. The value of this field changes from device to device. This field is stored in the EFUSE.
7:0	ADC_CLK_N_DIV	R/W	0x99	ADC clock frequency in MHz, derived directly from BAW. Default is ceil(2467 / 16) - 2 = 0x99. TI does not recommend modifying the value of this field. This field is stored in the EFUSE.

4.4.3 LMK3H0102A015 R2 Register (Address = 0x2) [reset = 0xC28F]

Table 4-42. R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	FOD0_NUM[15:0]	R/W	0xC28F	Lower two bytes of the FOD0 fractional divide value. The value of this field changes from device to device. This field is stored in the EFUSE.

4.4.4 LMK3H1002A015 R3 Register (Address = 0x3) [reset = 0x1801]

Table 4-43. R3 Register Field Descriptions

Bit	Firld	Type	Reset	Description
15:9	FOD1_N_DIV	R/W	0x0C	Integer Ratio of BAW frequency to FOD1 frequency. This field is stored in the EFUSE.
8	CH1_FOD_SEL	R/W	0x0	Selects the FOD to use as the input source for Channel Divider 1. This field is stored in the EFUSE. 0h: FOD0. 1h: FOD1.
7	CH1_EDGE_COMB_EN	R/W	0x0	Selects between using Channel Divider 1 or using the Edge Combiner as the input source for Output Driver 1. This field is stored in the EFUSE. 0h: Channel Divider 1 input 1h: Edge Combiner input
6	OUT1_DISABLE_STATE	R/W	0x0	When OUT1 is disabled, this bit selects whether the OUT1_P and OUT1_N pins are forced to GND or tri-stated. This field is stored in the EFUSE. 0h: Forced to GND on disable. Tri-state on disable.

Table 4-43. R3 Register Field Descriptions (continued)

Bit	Firld	Type	Reset	Description
5	OUT0_DISABLE_STATE	R/W	0x0	When OUT0 is disabled, this bit selects whether the OUT0_P and OUT0_N pins are forced to GND or tri-stated. This field is stored in the EFUSE. 0h: Forced to GND on disable. Tri-state on disable.
4	CH0_FOD_SEL	R/W	0x0	Selects the FOD to use as the input source for Channel Divider 0. This field is stored in the EFUSE. 0h: FOD0. 1h: FOD1.
3	CH0_EDGE_COMB_EN	R/W	0x0	Selects between using Channel Divider 0 or using the Edge Combiner as the input source for Output Driver 0. This field is stored in the EFUSE. 0h: Channel Divider 0 input 1h: Edge Combiner input
2:0	CH0_DIV	R/W	0x1	Divider value for Channel Divider 0. This field is stored in the EFUSE. 0h: Channel Divider disabled. 1h: FOD / 2 2h: FOD / 4 3h: FOD / 6 4h: FOD / 8 5h: FOD / 10 6h: FOD / 20 7h: FOD / 40

4.4.5 LMK3H0102A015 R4 Register (Address = 0x4) [reset = 0x0000]

Table 4-44. R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Reserved	R	0x0	Reserved
14:2	SSC_STEPS	R/W	0x0000	Number of steps in each segment of the triangular profile for SSC. See the data sheet for instructions on how to calculate this value. This field is stored in the EFUSE.
1	SSC_MOD_TYPE	R/W	0x0	Selects between down-spread or center-spread modulation for custom SSC configurations. This field is stored in the EFUSE. 0h: Down-spread modulation. 1h: Center-spread modulation.
0	SSC_EN	R/W	0x0	Enable SSC. This field is stored in the EFUSE. 0h: SSC Disabled. 1h: SSC Enabled.

4.4.6 LMK3H0102A015 R5 Register (Address = 0x5) [reset = 0x0000]

Table 4-45. R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	SSC_STEP_SIZE	R/W	0x0000	Numerator increment value per step for SSC. This field is stored in the EFUSE.

4.4.7 LMK3H0102A015 R6 Register (Address = 0x6) [reset = 0x0AA1]

Table 4-46. R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	CH1_DIV	R/W	0x0	Divider value for Channel Divider 1. This field is stored in the EFUSE. 0h: Channel Divider disabled. Set CH1_DIV to '0' when using the edge combiner for OUT1. 1h: FOD / 2 2h: FOD / 4 3h: FOD / 6 4h: FOD / 8 5h: FOD / 10 6h: FOD / 20 7h: FOD / 40
12:5	FOD1_NUM[23:16]	R/W	0x55	High byte of the FOD1 fractional divide value. The value of this field changes from device to device. This field is stored in the EFUSE.
4:3	OUT0_SLEW_RATE	R/W	0x0	Slew rate control for OUT0. This field is stored in the EFUSE. Only applies to differential output formats. 0h: Between 2.3V/ns and 3.5V/ns. 1h: Between 2.0V/ns and 3.2V/ns. 2h: Between 1.7V/ns and 2.8V/ns. 3h: Between 1.4V/ns and 2.7V/ns.
2:0	OUT0_FMT	R/W	0x1	Selects the output format for OUT0. This field is stored in the EFUSE. 0h: LP-HCSL 100Ω Termination. 1h: LP-HCSL 85Ω Termination. 2h: AC-coupled LVDS. 3h: DC-coupled LVDS. 4h: LVCMOS, OUTx_P enabled, OUTx_N disabled. 5h: LVCMOS, OUTx_P disabled, OUTx_N enabled. 6h: LVCMOS, OUTx_P enabled, OUTx_N enabled, 180 degrees out of phase. 7h: LVCMOS, OUTx_P enabled, OUTx_N enabled, OUTx_P and OUTx_N in phase.

4.4.8 LMK3H0102A015 R7 Register (Address = 0x7) [reset = 0x1507]

Table 4-47. R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Reserved	R	0x0	Reserved
14:13	REF_CTRL_PIN_FUNC	R/W	0x0	Sets the function of the REF_CTRL pin. This field is stored in the EFUSE. 0h: REF_CTRL pin disabled, pulled to GND. 1h: REF_CTRL pin disabled, tri-state. 2h: REF_CTRL pin functions as an additional LVCMOS REF_CLK output. 3h: REF_CTRL pin functions as "clock ready" signal.
12:11	REF_CLK_DIV	R/W	0x2	REF_CLK output divisor value when REF_CTRL is used as REF_CLK. This field is stored in the EFUSE. 0h: REF_CLK disabled. 1h: FOD / 2. 2h: FOD / 4. 3h: FOD / 8.
10	Reserved	R/W	0x1	Reserved. Do not write any value other than '1' to this field.
9	REF_CLK_FOD_SEL	R/W	0x0	Select the FOD used to generate the REF_CLK output. This field is stored in the EFUSE. 0h: FOD0. 1h: FOD1.

Table 4-47. R7 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	OUT1_EN	R/W	0x1	Output Enable bit for OUT1. This field is stored in the EFUSE. 0h: OUT1 is disabled. 1h: OUT1 is enabled.
7	OUT1_CH_SEL	R/W	0x0	Selects the source for OUT1. This field is stored in the EFUSE. 0h: OUT1 is sourced from Channel Divider 0 if CH0_EDGE_COMB_EN is a '0', or the Edge Combiner if CH0_EDGE_COMB_EN is a '1'. 1h: OUT1 is sourced from Channel Divider 1 if CH1_EDGE_COMB_EN is a '0', or the Edge Combiner if CH1_EDGE_COMB_EN is a '1'.
6:5	OUT1_SLEW_RATE	R/W	0x0	Slew rate control for OUT1. This field is stored in the EFUSE. Only applies to differential output formats. 0h: Between 2.3V/ns and 3.5V/ns. 1h: Between 2.0V/ns and 3.2V/ns. 2h: Between 1.7V/ns and 2.8V/ns. 3h: Between 1.4V/ns and 2.7V/ns.
4:2	OUT1_FMT	R/W	0x1	Selects the output format for OUT1. This field is stored in the EFUSE. 0h: LP-HCSL 100Ω Termination. 1h: LP-HCSL 85Ω Termination. 2h: AC-coupled LVDS. 3h: DC-coupled LVDS. 4h: LVCMOS, OUTx_P enabled, OUTx_N disabled. 5h: LVCMOS, OUTx_P disabled, OUTx_N enabled. 6h: LVCMOS, OUTx_P enabled, OUTx_N enabled, 180 degrees out of phase. 7h: LVCMOS, OUTx_P enabled, OUTx_N enabled, OUTx_P and OUTx_N in phase.
1	OUT0_EN	R/W	0x1	Output Enable bit for OUT0. This field is stored in the EFUSE. 0h: OUT0 is disabled. 1h: OUT0 is enabled.
0	OE_PIN_POLARITY	R/W	0x1	OE pin polarity selection. This bit does not affect the polarity of the OUTx_EN bits, only the OE pin. This field is stored in the EFUSE. 0h: OE is active high (OE tied to VDD enables outputs). 1h: OE is active low (OE tied to GND enables outputs).

4.4.9 LMK3H0102A015 R8 Register (Address = 0x8) [reset = 0xC28F]

Table 4-48. R8 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	FOD1_NUM[15:0]	R/W	0xC28F	Lower two bytes of the FOD1 fractional divide value. The value of this field changes from device to device. This field is stored in the EFUSE.

4.4.10 LMK3H0102A015 R9 Register (Address = 0x9) [reset = 0x5066]

Table 4-49. R9 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	OTP_ID	R/W	0x5	Configurable field for identifying the OTP configuration. Can be used in I2C mode as a 4-bit spare field. This field is stored in the EFUSE.

Table 4-49. R9 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:9	SSC_CONFIG_SEL	R/W	0x0	SSC modulation configuration. If center-spread modulation is desired, then custom SSC configuration is required. Four preconfigured down-spread modulation depths are also available. Any other modulation depths require custom SSC configuration. This field is stored in the EFUSE. 0h: Custom SSC Configuration 1h: –0.10% preconfigured down-spread. 2h: –0.25% preconfigured down-spread. 3h: –0.30% preconfigured down-spread. 4h: –0.50% preconfigured down-spread. All other values: Reserved
8	OUT_FMT_SRC_SEL	R/W	0x0	Forces the FMT_ADDR pin to override the output format register settings in OTP Mode. When in I2C mode, the FMT_ADDR pin is never used for this purpose. This field is stored in the EFUSE. 0h: FMT_ADDR pin is ignored in OTP mode for output format selection. 1h: FMT_ADDR pin overrides the register settings. The output format is LP-HCSL, and the termination resistor values are based on the FMT_ADDR pin state on start-up.
7:4	OUT1_LPHSCL_AMP_SEL	R/W	0x6	OUT1 output swing level when using LP-HCSL output format. This field is stored in the EFUSE. 0h: 625mV. 1h: 647mV. 2h: 668mV. 3h: 690mV. 4h: 712mV. 5h: 733mV. 6h: 755mV. 7h: 777mV. 8h: 798mV. 9h: 820mV. Ah: 842mV. Bh: 863mV. Ch: 885mV. Dh: 907mV. Eh: 928mV. Fh: 950mV.

Table 4-49. R9 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	OUT0_LPHSCL_AMP_SEL	R/W	0x6	OUT0 output swing level when using LP-HCSL output format. This field is stored in the EFUSE. 0h: 625mV. 1h: 647mV. 2h: 668mV. 3h: 690mV. 4h: 712mV. 5h: 733mV. 6h: 755mV. 7h: 777mV. 8h: 798mV. 9h: 820mV. Ah: 842mV. Bh: 863mV. Ch: 885mV. Dh: 907mV. Eh: 928mV. Fh: 950mV.

4.4.11 LMK3H0102A015 R10 Register (Address = 0xA) [reset = 0x0010]

Table 4-50. R10 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Reserved	R/W	0x0	Reserved. Only write '0' to this bit.
14:11	PROD_REVID	R	0x0	Product revision identifier.
10	CLK_READY	R	0x0	CLK_READY status. The REF_CTRL pin mirrors this status signal when the pin functions as a "clock ready" signal.
9	Reserved	R	0x0	Reserved. Do not write to this field.
8	RB_PIN_15	R	0x0	Readback of the REF_CTRL pin.
7	RB_PIN_4	R	0x0	Readback of the OTP_SEL1/SDA pin.
6	RB_PIN_3	R	0x0	Readback of the OTP_SEL0/SCL pin.
5	RB_PIN_2	R	0x0	Readback of the FMT_ADDR pin.
4	DEV_IDLE_STATE_SEL	R/W	0x1	This bit controls the behavior of the device when both outputs are disabled. Placing the device into a low-power state is not recommended for PCIe applications, as the time to re-enable the clocks is extended. This field is stored in the EFUSE. 0h: When both outputs are disabled, the outputs are muted, and the device is placed into a low-power state. 1h: When both outputs are disabled, the outputs are muted. The device does not enter a low-power state.
3	PIN_RESAMPLE_DIS	R/W	0x0	This bit controls the resampling of the device pins when exiting the low power mode. Write this bit while in the low power mode. TI recommends keeping this bit as a '1' unless the functionality is explicitly desired. After PDN, pins 2, 3, 4, and 15 are resampled. Device functionality can change based on new logic level of the pins. 0h: Pin resampling is enabled. When exiting the low power mode, the FMT_ADDR, OTP_SEL0/SCL, OTP_SEL1/SDA, and FMT_ADDR pins are resampled. If FMT_ADDR is high, the device enters OTP Mode. 1h: Pin resampling is disabled. When exiting the low power mode, the FMT_ADDR, OTP_SEL0/SCL, OTP_SEL1/SDA, and FMT_ADDR pins are not resampled. The device remains in I2C Mode.

Table 4-50. R10 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	OTP_AUTOLOAD_DIS	R/W	0x0	This bit controls the behavior of the device when exiting the low power mode. Write this bit while in the low power mode. TI recommends keeping this bit as a '1' unless the functionality is explicitly desired. 0h: OTP autoload is enabled. When exiting the low power mode, the contents of OTP Page 0 are written to the device registers. 1h: OTP autoload is disabled. When exiting the low power mode, the contents of OTP Page 0 are not written to the device registers.
1	PDN	R/W	0x0	Writing a '1' to this bit puts the device into a low power state.
0	Reserved	R/W	0x0	Reserved, do not write to this field.

4.4.12 LMK3H0102A015 R11 Register (Address = 0xB) [reset = 0x0000]

Table 4-51. R11 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Reserved	R/W	0x0	Reserved, only write '0' to this field.
14	SEPARATE_OE_EN	R/W	0x0	This bit enables the separate output enable functionality of the device. If this bit is a '1', then OUT_FMT_SRC_SEL and I2C_ADDR_LSB_SEL must be set to '0'. This field is stored in the EFUSE. 0h: Pin 1 is the output enable for OUT0 and OUT1. 1h: Pin 1 is the output enable for OUT0, Pin 2 is the output enable for OUT1.
13:0	Reserved	R/W	0x0000	Reserved, only write '0' to this field.

4.4.13 LMK3H0102A015 R12 Register (Address = 0xC) [reset = 0xE800]

Table 4-52. R12 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	I2C_ADDR_LSB_SEL	R/WL	0x1	I2C peripheral address source. If this bit is a '1', SEPARATE_OE_EN must be '0'. This field is stored in the EFUSE. 0h: I2C peripheral address comes entirely from the I2C_ADDR field. 1h: The two lowest bits of the I2C peripheral address come from the FMT_ADDR pin, all other bits come from R12[14:10].
14:8	I2C_ADDR	R/WL	0x68	I2C peripheral address. After writing to this field, the device responds to the new I2C address. This field is stored in the EFUSE.
7:0	UNLOCK_PROTECTED_REG	R/W	0x00	This field locks all registers from R13 onward, in addition to R12[15:8]. Registers R13 onward are largely device calibration registers, and must not have contents modified. These registers can be read from normally regardless of the unlock status. 5Bh: Unlocks register writes for R12[15:8] and above. Any other value: R12[15:8] and above ignore all writes.

4.5 LMK3H0102A016 Registers

4.5.1 LMK3H0102A016 R0 Register (Address = 0x0) [reset = 0x00C1]

Table 4-53. R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	DIG_CLK_N_DIV	R/W	0x00	Digital State Machine clock rate. Derived from the FOD frequency sourced by the CH0_FOD_SEL multiplexer. The target for the frequency is 50MHz maximum. The actual divide value is the DIG_CLK_N_DIV value plus 2. This field is stored in the EFUSE.
9:3	FOD0_N_DIV	R/W	0x10	Integer Ratio of BAW frequency to FOD0 frequency. This field is stored in the EFUSE.
2:1	Reserved	R	N/A	Reserved, do not write to this field.
0	OTP_BURNT	R/WL	0x1	Indicates if the EFUSE has been programmed. If this field is '1', the EFUSE is programmed.

4.5.2 LMK3H0102A016 R1 Register (Address = 0x1) [reset = 0xAB99]

Table 4-54. R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	FOD0_NUM[23:16]	R/W	0xAB	High byte of the FOD0 fractional divide value. The value of this field changes from device to device. This field is stored in the EFUSE.
7:0	ADC_CLK_N_DIV	R/W	0x99	ADC clock frequency in MHz, derived directly from BAW. Default is ceil(2467 / 16) - 2 = 0x99. TI does not recommend modifying the value of this field. This field is stored in the EFUSE.

4.5.3 LMK3H0102A016 R2 Register (Address = 0x2) [reset = 0x84EA]

Table 4-55. R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	FOD0_NUM[15:0]	R/W	0x84EA	Lower two bytes of the FOD0 fractional divide value. The value of this field changes from device to device. This field is stored in the EFUSE.

4.5.4 LMK3H1002A016 R3 Register (Address = 0x3) [reset = 0x3001]

Table 4-56. R3 Register Field Descriptions

Bit	Firld	Type	Reset	Description
15:9	FOD1_N_DIV	R/W	0x18	Integer Ratio of BAW frequency to FOD1 frequency. This field is stored in the EFUSE.
8	CH1_FOD_SEL	R/W	0x0	Selects the FOD to use as the input source for Channel Divider 1. This field is stored in the EFUSE. 0h: FOD0. 1h: FOD1.
7	CH1_EDGE_COMB_EN	R/W	0x0	Selects between using Channel Divider 1 or using the Edge Combiner as the input source for Output Driver 1. This field is stored in the EFUSE. 0h: Channel Divider 1 input 1h: Edge Combiner input
6	OUT1_DISABLE_STATE	R/W	0x0	When OUT1 is disabled, this bit selects whether the OUT1_P and OUT1_N pins are forced to GND or tri-stated. This field is stored in the EFUSE. 0h: Forced to GND on disable. Tri-state on disable.

Table 4-56. R3 Register Field Descriptions (continued)

Bit	Firld	Type	Reset	Description
5	OUT0_DISABLE_STATE	R/W	0x0	When OUT0 is disabled, this bit selects whether the OUT0_P and OUT0_N pins are forced to GND or tri-stated. This field is stored in the EFUSE. 0h: Forced to GND on disable. Tri-state on disable.
4	CH0_FOD_SEL	R/W	0x0	Selects the FOD to use as the input source for Channel Divider 0. This field is stored in the EFUSE. 0h: FOD0. 1h: FOD1.
3	CH0_EDGE_COMB_EN	R/W	0x0	Selects between using Channel Divider 0 or using the Edge Combiner as the input source for Output Driver 0. This field is stored in the EFUSE. 0h: Channel Divider 0 input 1h: Edge Combiner input
2:0	CH0_DIV	R/W	0x1	Divider value for Channel Divider 0. This field is stored in the EFUSE. 0h: Channel Divider disabled. 1h: FOD / 2 2h: FOD / 4 3h: FOD / 6 4h: FOD / 8 5h: FOD / 10 6h: FOD / 20 7h: FOD / 40

4.5.5 LMK3H0102A016 R4 Register (Address = 0x4) [reset = 0x0000]

Table 4-57. R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Reserved	R	0x0	Reserved
14:2	SSC_STEPS	R/W	0x0000	Number of steps in each segment of the triangular profile for SSC. See the data sheet for instructions on how to calculate this value. This field is stored in the EFUSE.
1	SSC_MOD_TYPE	R/W	0x0	Selects between down-spread or center-spread modulation for custom SSC configurations. This field is stored in the EFUSE. 0h: Down-spread modulation. 1h: Center-spread modulation.
0	SSC_EN	R/W	0x0	Enable SSC. This field is stored in the EFUSE. 0h: SSC Disabled. 1h: SSC Enabled.

4.5.6 LMK3H0102A016 R5 Register (Address = 0x5) [reset = 0x0000]

Table 4-58. R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	SSC_STEP_SIZE	R/W	0x0000	Numerator increment value per step for SSC. This field is stored in the EFUSE.

4.5.7 LMK3H0102A016 R6 Register (Address = 0x6) [reset = 0x1566]

Table 4-59. R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	CH1_DIV	R/W	0x0	Divider value for Channel Divider 1. This field is stored in the EFUSE. 0h: Channel Divider disabled. Set CH1_DIV to '0' when using the edge combiner for OUT1. 1h: FOD / 2 2h: FOD / 4 3h: FOD / 6 4h: FOD / 8 5h: FOD / 10 6h: FOD / 20 7h: FOD / 40
12:5	FOD1_NUM[23:16]	R/W	0xAB	High byte of the FOD1 fractional divide value. The value of this field changes from device to device. This field is stored in the EFUSE.
4:3	OUT0_SLEW_RATE	R/W	0x0	Slew rate control for OUT0. This field is stored in the EFUSE. Only applies to differential output formats. 0h: Between 2.3V/ns and 3.5V/ns. 1h: Between 2.0V/ns and 3.2V/ns. 2h: Between 1.7V/ns and 2.8V/ns. 3h: Between 1.4V/ns and 2.7V/ns.
2:0	OUT0_FMT	R/W	0x6	Selects the output format for OUT0. This field is stored in the EFUSE. 0h: LP-HCSL 100Ω Termination. 1h: LP-HCSL 85Ω Termination. 2h: AC-coupled LVDS. 3h: DC-coupled LVDS. 4h: LVCMOS, OUTx_P enabled, OUTx_N disabled. 5h: LVCMOS, OUTx_P disabled, OUTx_N enabled. 6h: LVCMOS, OUTx_P enabled, OUTx_N enabled, 180 degrees out of phase. 7h: LVCMOS, OUTx_P enabled, OUTx_N enabled, OUTx_P and OUTx_N in phase.

4.5.8 LMK3H0102A016 R7 Register (Address = 0x7) [reset = 0x241D]

Table 4-60. R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Reserved	R	0x0	Reserved
14:13	REF_CTRL_PIN_FUNC	R/W	0x1	Sets the function of the REF_CTRL pin. This field is stored in the EFUSE. 0h: REF_CTRL pin disabled, pulled to GND. 1h: REF_CTRL pin disabled, tri-state. 2h: REF_CTRL pin functions as an additional LVCMOS REF_CLK output. 3h: REF_CTRL pin functions as "clock ready" signal.
12:11	REF_CLK_DIV	R/W	0x0	REF_CLK output divisor value when REF_CTRL is used as REF_CLK. This field is stored in the EFUSE. 0h: REF_CLK disabled. 1h: FOD / 2. 2h: FOD / 4. 3h: FOD / 8.
10	Reserved	R/W	0x1	Reserved. Do not write any value other than '1' to this field.
9	REF_CLK_FOD_SEL	R/W	0x0	Select the FOD used to generate the REF_CLK output. This field is stored in the EFUSE. 0h: FOD0. 1h: FOD1.

Table 4-60. R7 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	OUT1_EN	R/W	0x0	Output Enable bit for OUT1. This field is stored in the EFUSE. 0h: OUT1 is disabled. 1h: OUT1 is enabled.
7	OUT1_CH_SEL	R/W	0x0	Selects the source for OUT1. This field is stored in the EFUSE. 0h: OUT1 is sourced from Channel Divider 0 if CH0_EDGE_COMB_EN is a '0', or the Edge Combiner if CH0_EDGE_COMB_EN is a '1'. 1h: OUT1 is sourced from Channel Divider 1 if CH1_EDGE_COMB_EN is a '0', or the Edge Combiner if CH1_EDGE_COMB_EN is a '1'.
6:5	OUT1_SLEW_RATE	R/W	0x0	Slew rate control for OUT1. This field is stored in the EFUSE. Only applies to differential output formats. 0h: Between 2.3V/ns and 3.5V/ns. 1h: Between 2.0V/ns and 3.2V/ns. 2h: Between 1.7V/ns and 2.8V/ns. 3h: Between 1.4V/ns and 2.7V/ns.
4:2	OUT1_FMT	R/W	0x7	Selects the output format for OUT1. This field is stored in the EFUSE. 0h: LP-HCSL 100Ω Termination. 1h: LP-HCSL 85Ω Termination. 2h: AC-coupled LVDS. 3h: DC-coupled LVDS. 4h: LVCMOS, OUTx_P enabled, OUTx_N disabled. 5h: LVCMOS, OUTx_P disabled, OUTx_N enabled. 6h: LVCMOS, OUTx_P enabled, OUTx_N enabled, 180 degrees out of phase. 7h: LVCMOS, OUTx_P enabled, OUTx_N enabled, OUTx_P and OUTx_N in phase.
1	OUT0_EN	R/W	0x0	Output Enable bit for OUT0. This field is stored in the EFUSE. 0h: OUT0 is disabled. 1h: OUT0 is enabled.
0	OE_PIN_POLARITY	R/W	0x1	OE pin polarity selection. This bit does not affect the polarity of the OUTx_EN bits, only the OE pin. This field is stored in the EFUSE. 0h: OE is active high (OE tied to VDD enables outputs). 1h: OE is active low (OE tied to GND enables outputs).

4.5.9 LMK3H0102A016 R8 Register (Address = 0x8) [reset = 0x84EA]

Table 4-61. R8 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	FOD1_NUM[15:0]	R/W	0x84EA	Lower two bytes of the FOD1 fractional divide value. The value of this field changes from device to device. This field is stored in the EFUSE.

4.5.10 LMK3H0102A016 R9 Register (Address = 0x9) [reset = 0x6066]

Table 4-62. R9 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	OTP_ID	R/W	0x6	Configurable field for identifying the OTP configuration. Can be used in I2C mode as a 4-bit spare field. This field is stored in the EFUSE.

Table 4-62. R9 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:9	SSC_CONFIG_SEL	R/W	0x0	SSC modulation configuration. If center-spread modulation is desired, then custom SSC configuration is required. Four preconfigured down-spread modulation depths are also available. Any other modulation depths require custom SSC configuration. This field is stored in the EFUSE. 0h: Custom SSC Configuration 1h: –0.10% preconfigured down-spread. 2h: –0.25% preconfigured down-spread. 3h: –0.30% preconfigured down-spread. 4h: –0.50% preconfigured down-spread. All other values: Reserved
8	OUT_FMT_SRC_SEL	R/W	0x0	Forces the FMT_ADDR pin to override the output format register settings in OTP Mode. When in I2C mode, the FMT_ADDR pin is never used for this purpose. This field is stored in the EFUSE. 0h: FMT_ADDR pin is ignored in OTP mode for output format selection. 1h: FMT_ADDR pin overrides the register settings. The output format is LP-HCSL, and the termination resistor values are based on the FMT_ADDR pin state on start-up.
7:4	OUT1_LPHSCL_AMP_SEL	R/W	0x6	OUT1 output swing level when using LP-HCSL output format. This field is stored in the EFUSE. 0h: 625mV. 1h: 647mV. 2h: 668mV. 3h: 690mV. 4h: 712mV. 5h: 733mV. 6h: 755mV. 7h: 777mV. 8h: 798mV. 9h: 820mV. Ah: 842mV. Bh: 863mV. Ch: 885mV. Dh: 907mV. Eh: 928mV. Fh: 950mV.

Table 4-62. R9 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	OUT0_LPHSCL_AMP_SEL	R/W	0x6	OUT0 output swing level when using LP-HCSL output format. This field is stored in the EFUSE. 0h: 625mV. 1h: 647mV. 2h: 668mV. 3h: 690mV. 4h: 712mV. 5h: 733mV. 6h: 755mV. 7h: 777mV. 8h: 798mV. 9h: 820mV. Ah: 842mV. Bh: 863mV. Ch: 885mV. Dh: 907mV. Eh: 928mV. Fh: 950mV.

4.5.11 LMK3H0102A016 R10 Register (Address = 0xA) [reset = 0x0810]

Table 4-63. R10 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Reserved	R/W	0x0	Reserved. Only write '0' to this bit.
14:11	PROD_REVID	R	0x1	Product revision identifier.
10	CLK_READY	R	0x0	CLK_READY status. The REF_CTRL pin mirrors this status signal when the pin functions as a "clock ready" signal.
9	Reserved	R	0x0	Reserved. Do not write to this field.
8	RB_PIN_15	R	0x0	Readback of the REF_CTRL pin.
7	RB_PIN_4	R	0x0	Readback of the OTP_SEL1/SDA pin.
6	RB_PIN_3	R	0x0	Readback of the OTP_SEL0/SCL pin.
5	RB_PIN_2	R	0x0	Readback of the FMT_ADDR pin.
4	DEV_IDLE_STATE_SEL	R/W	0x1	This bit controls the behavior of the device when both outputs are disabled. Placing the device into a low-power state is not recommended for PCIe applications, as the time to re-enable the clocks is extended. This field is stored in the EFUSE. 0h: When both outputs are disabled, the outputs are muted, and the device is placed into a low-power state. 1h: When both outputs are disabled, the outputs are muted. The device does not enter a low-power state.
3	PIN_RESAMPLE_DIS	R/W	0x0	This bit controls the resampling of the device pins when exiting the low power mode. Write this bit while in the low power mode. TI recommends keeping this bit as a '1' unless the functionality is explicitly desired. After PDN, pins 2, 3, 4, and 15 are resampled. Device functionality can change based on new logic level of the pins. 0h: Pin resampling is enabled. When exiting the low power mode, the FMT_ADDR, OTP_SEL0/SCL, OTP_SEL1/SDA, and FMT_ADDR pins are resampled. If FMT_ADDR is high, the device enters OTP Mode. 1h: Pin resampling is disabled. When exiting the low power mode, the FMT_ADDR, OTP_SEL0/SCL, OTP_SEL1/SDA, and FMT_ADDR pins are not resampled. The device remains in I2C Mode.

Table 4-63. R10 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	OTP_AUTOLOAD_DIS	R/W	0x0	This bit controls the behavior of the device when exiting the low power mode. Write this bit while in the low power mode. TI recommends keeping this bit as a '1' unless the functionality is explicitly desired. 0h: OTP autoload is enabled. When exiting the low power mode, the contents of OTP Page 0 are written to the device registers. 1h: OTP autoload is disabled. When exiting the low power mode, the contents of OTP Page 0 are not written to the device registers.
1	PDN	R/W	0x0	Writing a '1' to this bit puts the device into a low power state.
0	Reserved	R/W	0x0	Reserved, do not write to this field.

4.5.12 LMK3H0102A016 R11 Register (Address = 0xB) [reset = 0x0000]

Table 4-64. R11 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Reserved	R/W	0x0	Reserved, only write '0' to this field.
14	SEPARATE_OE_EN	R/W	0x0	This bit enables the separate output enable functionality of the device. If this bit is a '1', then OUT_FMT_SRC_SEL and I2C_ADDR_LSB_SEL must be set to '0'. This field is stored in the EFUSE. 0h: Pin 1 is the output enable for OUT0 and OUT1. 1h: Pin 1 is the output enable for OUT0, Pin 2 is the output enable for OUT1.
13:0	Reserved	R/W	0x0000	Reserved, only write '0' to this field.

4.5.13 LMK3H0102A016 R12 Register (Address = 0xC) [reset = 0xE800]

Table 4-65. R12 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	I2C_ADDR_LSB_SEL	R/WL	0x1	I2C peripheral address source. If this bit is a '1', SEPARATE_OE_EN must be '0'. This field is stored in the EFUSE. 0h: I2C peripheral address comes entirely from the I2C_ADDR field. 1h: The two lowest bits of the I2C peripheral address come from the FMT_ADDR pin, all other bits come from R12[14:10].
14:8	I2C_ADDR	R/WL	0x68	I2C peripheral address. After writing to this field, the device responds to the new I2C address. This field is stored in the EFUSE.
7:0	UNLOCK_PROTECTED_REG	R/W	0x00	This field locks all registers from R13 onward, in addition to R12[15:8]. Registers R13 onward are largely device calibration registers, and must not have contents modified. These registers can be read from normally regardless of the unlock status. 5Bh: Unlocks register writes for R12[15:8] and above. Any other value: R12[15:8] and above ignore all writes.

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