LMK05028 Registers

1 LMK05028 Register Map Generation Using TICS Pro

The TICS Pro software tool for EVM programming has a step-by-step design flow to enter the user's clock design parameters, calculate the frequency plan, and generate the device register settings for the desired configuration. The register settings can be exported (in hex format) to enable host programming of the LMK05028 on start-up. The TICS Pro setup file can also be provided to TI for device configuration review, optimization, and to enable factory pre-programmed sample devices.

See the *LMK05028 Datasheet* for the General Register Programming Sequence and EEPROM Programming Flow.

2 LMK05028 Registers

Table 1 lists the memory-mapped registers for the LMK05028. All register offset addresses not listed in Table 1 should be considered as reserved locations and the register contents should not be modified.

Table 1. LMK05028 Registers

Address	Acronym	Register Name	Section
0h	R0	VNDRID_BY1	Go
1h	R1	VNDRID_BY0	Go
2h	R2	PRODID	Go
3h	R3	REVID	Go
4h	R4	PARTID_BY3	Go
5h	R5	PARTID_BY2	Go
6h	R6	PARTID_BY1	Go
7h	R7	PARTID_BY0	Go
8h	R8	PINMODE_SW	Go
9h	R9	PINMODE_HW	Go
Ah	R10	SLAVEADR	Go
Bh	R11	EEREV	Go
Ch	R12	DEV_CTL	Go
Dh	R13	INT_LIVE0	Go
Eh	R14	INT_LIVE1	Go
Fh	R15	INT_LIVE2	Go
10h	R16	INT_MASK0	Go
11h	R17	INT_MASK1	Go
12h	R18	INT_MASK2	Go
13h	R19	INT_FLAG_POL0	Go
14h	R20	INT_FLAG_POL1	Go
15h	R21	INT_FLAG_POL2	Go
16h	R22	INT_FLAG0	Go
17h	R23	INT_FLAG1	Go
18h	R24	INT_FLAG2	Go
19h	R25	INTCTL	Go

Table 1. LMK05028 Registers (continued)

Address	Acronym	Register Name	Section
1Ah	R26	RESERVED	Go
1Bh	R27	MUTELVL1	Go
1Ch	R28	MUTELVL2	Go
1Dh	R29	OUT_MUTE	Go
1Eh	R30	CH_SLEW_RATE1	Go
1Fh	R31	CH_SLEW_RATE2	Go
20h	R32	RESERVED	Go
21h	R33	RESERVED	Go
22h	R34	XO_DIFF_DETAMP	Go
23h	R35	RESERVED	Go
24h	R36	XO_CLKCTL1	Go
25h	R37	RESERVED	Go
26h	R38	XO_CLKCTL3	Go
27h	R39	RESERVED	Go
28h	R40	RESERVED	Go
29h	R41	RESERVED	Go
2Ah	R42	RESERVED	Go
2Bh	R43	REF_CLKCTL1	Go
2Ch	R44	REF_CLKCTL2	Go
2Dh	R45	REF_CLKCTL3	Go
2Eh	R46	STAT0_SEL	Go
2Fh	R47	STAT1_SEL	Go
30h	R48	GPIO5_STAT_SEL	Go
31h	R49	GPIO6_STAT_SEL	Go
32h	R50	GPIO_FDEV_EN	Go
33h	R51	PWDN	Go
34h	R52	OUTCTL_0	Go
35h	R53	OUTDIV_0_CLK_MUX	Go
36h	R54	OUTDIV_0_BY3	Go
37h	R55	OUTDIV_0_BY2	Go
38h	R56	OUTDIV_0_BY1	Go
39h	R57	OUTDIV_0_BY0	Go
3Ah	R58	OUTCTL_1	Go
3Bh	R59	OUTDIV_1_BY2	Go
3Ch	R60	OUTDIV_1_BY1	Go
3Dh	R61	OUTDIV_1_BY0	Go
3Eh	R62	OUTCTL_2	Go
3Fh	R63	OUTCTL_3	Go
40h	R64	OUTDIV_2_3_BY2	Go
41h	R65	OUTDIV_2_3_BY1	Go
42h	R66	OUTDIV_2_3_BY0	Go
43h	R67	OUTCTL_4	Go
44h	R68	OUTCTL_5	Go
45h	R69	OUTDIV_4_5_BY2	Go
46h	R70	OUTDIV_4_5_BY1	Go
47h	R71	OUTDIV_4_5_BY0	Go
48h	R72	OUTCTL_6	Go

Table 1. LMK05028 Registers (continued)

Address	Acronym	Register Name	Section
49h	R73	OUTDIV_6_BY2	Go
4Ah	R74	OUTDIV_6_BY1	Go
4Bh	R75	OUTDIV_6_BY0	Go
4Ch	R76	OUTCTL_7	Go
4Dh	R77	OUTDIV_7_CLK_MUX	Go
4Eh	R78	OUTDIV_7_BY3	Go
4Fh	R79	OUTDIV_7_BY2	Go
50h	R80	OUTDIV_7_BY1	Go
51h	R81	OUTDIV_7_BY0	Go
52h	R82	OUTSYNCCTL	Go
53h	R83	OUTSYNCEN	Go
54h	R84	OUT0DLYEN	Go
55h	R85	OUTCH_VLD_TMR_CTRL1	Go
56h	R86	OUTCH_VLD_TMR_CTRL2	Go
57h	R87	OUTCH_VLD_TMR_CTRL3	Go
58h	R88	OUTACT	Go
59h	R89	REF_BYPASS_SEL	Go
5Ah	R90	PLL1_CTRL0	Go
5Bh	R91	PLL1_CTRL1	Go
5Ch	R92	PLL1_CTRL2	Go
5Dh	R93	RESERVED	Go
5Eh	R94	PLL1_CTRL4	Go
5Fh	R95	PLL1_CALCTRL0	Go
60h	R96	PLL2_CTRL0	Go
61h	R97	PLL2_CTRL1	Go
62h	R98	PLL2_CTRL2	Go
63h	R99	RESERVED	Go
64h	R100	PLL2_CTRL4	Go
65h	R101	PLL2_CALCTRL0	Go
66h	R102	PLL1_NDIV_BY1	Go
67h	R103	PLL1_NDIV_BY0	Go
68h	R104	PLL1_NUM_BY4	Go
69h	R105	PLL1_NUM_BY3	Go
6Ah	R106	PLL1_NUM_BY2	Go
6Bh	R107	PLL1_NUM_BY1	Go
6Ch	R108	PLL1_NUM_BY0	Go
6Dh	R109	PLL1_MASHCTRL	Go
6Eh	R110	RESERVED	Go
6Fh	R111	PLL1_MODE	Go
70h	R112	RESERVED	Go
71h	R113	RESERVED	Go
72h	R114	RESERVED	Go
73h	R115	RESERVED	Go
74h	R116	RESERVED	Go
75h	R117	RESERVED	Go
76h	R118	PLL1_NUM_STAT_BY4	Go
77h	R119	PLL1_NUM_STAT_BY3	Go

Table 1. LMK05028 Registers (continued)

Address	Acronym	Register Name	Section
78h	R120	PLL1_NUM_STAT_BY2	Go
79h	R121	PLL1_NUM_STAT_BY1	Go
7Ah	R122	PLL1_NUM_STAT_BY0	Go
7Bh	R123	PLL1_MASH_STAT	Go
7Ch	R124	PLL1_LF_R2	Go
7Dh	R125	RESERVED	Go
7Eh	R126	PLL1_LF_R3	Go
7Fh	R127	PLL1_LF_R4	Go
80h	R128	PLL1_LF_C3C4	Go
81h	R129	PLL2_NDIV_BY1	Go
82h	R130	PLL2_NDIV_BY0	Go
83h	R131	PLL2_NUM_BY4	Go
84h	R132	PLL2_NUM_BY3	Go
85h	R133	PLL2_NUM_BY2	Go
86h	R134	PLL2_NUM_BY1	Go
87h	R135	PLL2_NUM_BY0	Go
88h	R136	PLL2_MASHCTRL	Go
89h	R137	RESERVED	Go
8Ah	R138	PLL2_MODE	Go
8Bh	R139	RESERVED	Go
8Ch	R140	RESERVED	Go
8Dh	R141	RESERVED	Go
8Eh	R142	RESERVED	Go
8Fh	R143	RESERVED	Go
90h	R144	RESERVED	Go
91h	R145	PLL2_NUM_STAT_BY4	Go
92h	R146	PLL2_NUM_STAT_BY3	Go
93h	R147	PLL2_NUM_STAT_BY2	Go
94h	R148	PLL2_NUM_STAT_BY1	Go
95h	R149	PLL2_NUM_STAT_BY0	Go
96h	R150	PLL2_MASH_STAT	Go
97h	R151	PLL2_LF_R2	Go
98h	R152	RESERVED	Go
99h	R153	PLL2_LF_R3	Go
9Ah	R154	PLL2_LF_R4	Go
9Bh	R155	PLL2_LF_C3C4	Go
9Ch	R156	RESERVED	Go
9Dh	R157	RESERVED	Go
9Eh	R158	RESERVED	Go
9Fh	R159	RESERVED	Go
A0h	R160	RESERVED	Go
A1h	R161	RESERVED	Go
A2h	R162	RESERVED	Go
A3h	R163	RESERVED	Go
A4h	R164	RESERVED	Go
A5h	R165	NVMSCRC	Go
A6h	R166	NVMCNT	Go

Table 1. LMK05028 Registers (continued)

Address	Acronym	Register Name	Section
A7h	R167	NVMCTL	Go
A8h	R168	NVMLCRC	Go
A9h	R169	MEMADR_BY1	Go
AAh	R170	MEMADR_BY0	Go
ABh	R171	NVMDAT	Go
ACh	R172	RAMDAT	Go
ADh	R173	RESERVED	Go
AEh	R174	NVMUNLK	Go
AFh	R175	REGCOMMIT_PAGE	Go
B0h	R176	DPLL_REF_PATH_SEL1	Go
B1h	R177	RESERVED	Go
B2h	R178	RESERVED	Go
B3h	R179	RESERVED	Go
B4h	R180	RESERVED	Go
B5h	R181	RESERVED	Go
B6h	R182	SPARE_NVM2	Go
B7h	R183	SPARE_NVM1	Go
B8h	R184	SPARE_NVM0	Go
B9h	R185	DPLL_TCXO_MDIV	Go
BAh	R186	TCXO_CLKCTL1	Go
BBh	R187	REF01_DETAMP	Go
BCh	R188	REF23_DETAMP	Go
BDh	R189	REF0_DETEN	Go
BEh	R190	REF1_DETEN	Go
BFh	R191	REF2_DETEN	Go
C0h	R192	REF3_DETEN	Go
C1h	R193	RESERVED	Go
C2h	R194	RESERVED	Go
C3h	R195	RESERVED	Go
C4h	R196	RESERVED	Go
C5h	R197	RESERVED	Go
C6h	R198	RESERVED	Go
C7h	R199	RESERVED	Go
C8h	R200	RESERVED	Go
C9h	R201	RESERVED	Go
CAh	R202	RESERVED	Go
CBh	R203	RESERVED	Go
CCh	R204	RESERVED	Go
CDh	R205	REF_MISSCLK_CTL	Go
CEh	R206	RESERVED	Go
CFh	R207	RESERVED	Go
D0h	R208	RESERVED	Go
D1h	R209	RESERVED	Go
D2h	R210	RESERVED	Go
D3h	R211	RESERVED	Go
D4h	R212	RESERVED	Go
D5h	R213	RESERVED	Go

Table 1. LMK05028 Registers (continued)

Address	Acronym	Register Name	Section
D6h	R214	RESERVED	Go
D7h	R215	RESERVED	Go
D8h	R216	RESERVED	Go
D9h	R217	RESERVED	Go
DAh	R218	REF_PPMCTL	Go
DBh	R219	RESERVED	Go
DCh	R220	RESERVED	Go
DDh	R221	RESERVED	Go
DEh	R222	RESERVED	Go
DFh	R223	RESERVED	Go
E0h	R224	RESERVED	Go
E1h	R225	RESERVED	Go
E2h	R226	RESERVED	Go
E3h	R227	RESERVED	Go
E4h	R228	RESERVED	Go
E5h	R229	RESERVED	Go
E6h	R230	RESERVED	Go
E7h	R231	RESERVED	Go
E8h	R232	RESERVED	Go
E9h	R233	RESERVED	Go
EAh	R234	RESERVED	Go
EBh	R235	RESERVED	Go
ECh	R236	RESERVED	Go
EDh	R237	RESERVED	Go
EEh	R238	RESERVED	Go
EFh	R239	RESERVED	Go
F0h	R240	RESERVED	Go
F1h	R241	RESERVED	Go
F2h	R242	RESERVED	Go
F3h	R243	RESERVED	Go
F4h	R244	RESERVED	Go
F5h	R245	RESERVED	Go
F6h	R246	RESERVED	Go
F7h	R247	RESERVED	Go
F8h	R248	RESERVED	Go
F9h	R249	RESERVED	Go
FAh	R250	RESERVED	Go
FBh	R251	RESERVED	Go
FCh	R252	RESERVED	Go
FDh	R253	RESERVED	Go
FEh	R254	RESERVED	Go
FFh	R255	RESERVED	Go
100h	R256	RESERVED	Go
101h	R257	RESERVED	Go
102h	R258	RESERVED	Go
103h	R259	RESERVED	Go
104h	R260	RESERVED	Go

Table 1. LMK05028 Registers (continued)

Address	Acronym	Register Name	Section
105h	R261	RESERVED	Go
106h	R262	RESERVED	Go
107h	R263	RESERVED	Go
108h	R264	RESERVED	Go
109h	R265	RESERVED	Go
10Ah	R266	RESERVED	Go
10Bh	R267	RESERVED	Go
10Ch	R268	RESERVED	Go
10Dh	R269	RESERVED	Go
10Eh	R270	RESERVED	Go
10Fh	R271	RESERVED	Go
110h	R272	RESERVED	Go
111h	R273	RESERVED	Go
112h	R274	RESERVED	Go
113h	R275	RESERVED	Go
114h	R276	RESERVED	Go
115h	R277	RESERVED	Go
116h	R278	RESERVED	Go
117h	R279	RESERVED	Go
118h	R280	RESERVED	Go
119h	R281	RESERVED	Go
11Ah	R282	RESERVED	Go
11Bh	R283	RESERVED	Go
11Ch	R284	RESERVED	Go
11Dh	R285	RESERVED	Go
11Eh	R286	RESERVED	Go
11Fh	R287	RESERVED	Go
120h	R288	RESERVED	Go
121h	R289	RESERVED	Go
122h	R290	RESERVED	Go
123h	R291	RESERVED	Go
124h	R292	DPLL1_REF01_PRTY	Go
125h	R293	DPLL1_REF23_PRTY	Go
126h	R294	DPLL1_REF45_PRTY	Go
127h	R295	DPLL1_REF_LOOPBACK	Go
128h	R296	DPLL1_REF_SWMODE	Go
129h	R297	DPLL2_REF01_PRTY	Go
12Ah	R298	DPLL2_REF23_PRTY	Go
12Bh	R299	DPLL2_REF45_PRTY	Go
12Ch	R300	DPLL2_REF_LOOPBACK	Go
12Dh	R301	DPLL2_REF_SWMODE	Go
12Eh	R302	DPLL1_GEN_CTL	Go
12Fh	R303	DPLL1_SWITCHOVER_TMR_EXP	Go
130h	R304	DPLL1_SWITCHOVER_TMR_MANT_BY1	Go
131h	R305	DPLL1_SWITCHOVER_TMR_MANT_BY0	Go
132h	R306	DPLL1_REF0_RDIV_BY1	Go
133h	R307	DPLL1_REF0_RDIV_BY0	Go

Table 1. LMK05028 Registers (continued)

Address	Acronym	Register Name	Section
134h	R308	DPLL1_REF1_RDIV_BY1	Go
135h	R309	DPLL1_REF1_RDIV_BY0	Go
136h	R310	DPLL1_REF2_RDIV_BY1	Go
137h	R311	DPLL1_REF2_RDIV_BY0	Go
138h	R312	DPLL1_REF3_RDIV_BY1	Go
139h	R313	DPLL1_REF3_RDIV_BY0	Go
13Ah	R314	RESERVED	Go
13Bh	R315	RESERVED	Go
13Ch	R316	DPLL1_REF5_RDIV_BY1	Go
13Dh	R317	DPLL1_REF5_RDIV_BY0	Go
13Eh	R318	DPLL1_REF_TDC_CTL	Go
13Fh	R319	RESERVED	Go
140h	R320	RESERVED	Go
141h	R321	RESERVED	Go
142h	R322	RESERVED	Go
143h	R323	RESERVED	Go
144h	R324	RESERVED	Go
145h	R325	RESERVED	Go
146h	R326	RESERVED	Go
147h	R327	RESERVED	Go
148h	R328	RESERVED	Go
149h	R329	RESERVED	Go
14Ah	R330	RESERVED	Go
14Bh	R331	RESERVED	Go
14Ch	R332	RESERVED	Go
14Dh	R333	RESERVED	Go
14Eh	R334	RESERVED	Go
14Fh	R335	RESERVED	Go
150h	R336	RESERVED	Go
151h	R337	RESERVED	Go
152h	R338	RESERVED	Go
153h	R339	RESERVED	Go
154h	R340	RESERVED	Go
155h	R341	RESERVED	Go
156h	R342	RESERVED	Go
157h	R343	RESERVED	Go
158h	R344	RESERVED	Go
159h	R345	RESERVED	Go
15Ah	R346	RESERVED	Go
15Bh	R347	RESERVED	Go
15Ch	R348	RESERVED	Go
15Dh	R349	RESERVED	Go
15Eh	R350	RESERVED	Go
15Fh	R351	RESERVED	Go
160h	R352	RESERVED	Go
161h	R353	RESERVED	Go
162h	R354	RESERVED	Go

Table 1. LMK05028 Registers (continued)

Address	Acronym	Register Name	Section
163h	R355	RESERVED	Go
164h	R356	RESERVED	Go
165h	R357	RESERVED	Go
166h	R358	RESERVED	Go
167h	R359	RESERVED	Go
168h	R360	RESERVED	Go
169h	R361	DPLL1_CLK_FB_DIV	Go
16Ah	R362	DPLL1_REF_FB_PREDIV	Go
16Bh	R363	DPLL1_REF_FB_DIV_BY3	Go
16Ch	R364	DPLL1_REF_FB_DIV_BY2	Go
16Dh	R365	DPLL1_REF_FB_DIV_BY1	Go
16Eh	R366	DPLL1_REF_FB_DIV_BY0	Go
16Fh	R367	DPLL1_REF_NUM_BY4	Go
170h	R368	DPLL1_REF_NUM_BY3	Go
171h	R369	DPLL1_REF_NUM_BY2	Go
172h	R370	DPLL1_REF_NUM_BY1	Go
173h	R371	DPLL1_REF_NUM_BY0	Go
174h	R372	DPLL1_REF_DEN_BY4	Go
175h	R373	DPLL1_REF_DEN_BY3	Go
176h	R374	DPLL1_REF_DEN_BY2	Go
177h	R375	DPLL1_REF_DEN_BY1	Go
178h	R376	DPLL1_REF_DEN_BY0	Go
179h	R377	DPLL1_REF_MASHCTL	Go
17Ah	R378	RESERVED	Go
17Bh	R379	RESERVED	Go
17Ch	R380	RESERVED	Go
17Dh	R381	RESERVED	Go
17Eh	R382	RESERVED	Go
17Fh	R383	RESERVED	Go
180h	R384	RESERVED	Go
181h	R385	RESERVED	Go
182h	R386	RESERVED	Go
183h	R387	RESERVED	Go
184h	R388	RESERVED	Go
185h	R389	RESERVED	Go
186h	R390	RESERVED	Go
187h	R391	RESERVED	Go
188h	R392	RESERVED	Go
189h	R393	RESERVED	Go
18Ah	R394	RESERVED	Go
18Bh	R395	RESERVED	Go
18Ch	R396	RESERVED	Go
18Dh	R397	RESERVED	Go
18Eh	R398	DPLL1_REF_SYNC_PH_OFFSET_BY5	Go
18Fh	R399	DPLL1_REF_SYNC_PH_OFFSET_BY4	Go
190h	R400	DPLL1_REF_SYNC_PH_OFFSET_BY3	Go
191h	R401	DPLL1_REF_SYNC_PH_OFFSET_BY2	Go

Table 1. LMK05028 Registers (continued)

Address	Acronym	Register Name	Section
192h	R402	DPLL1_REF_SYNC_PH_OFFSET_BY1	Go
193h	R403	DPLL1_REF_SYNC_PH_OFFSET_BY0	Go
194h	R404	RESERVED	Go
195h	R405	RESERVED	Go
196h	R406	RESERVED	Go
197h	R407	RESERVED	Go
198h	R408	RESERVED	Go
199h	R409	RESERVED	Go
19Ah	R410	RESERVED	Go
19Bh	R411	RESERVED	Go
19Ch	R412	RESERVED	Go
19Dh	R413	RESERVED	Go
19Eh	R414	RESERVED	Go
19Fh	R415	RESERVED	Go
1A0h	R416	RESERVED	Go
1A1h	R417	RESERVED	Go
1A2h	R418	RESERVED	Go
1A3h	R419	RESERVED	Go
1A4h	R420	RESERVED	Go
1A5h	R421	RESERVED	Go
1A6h	R422	RESERVED	Go
1A7h	R423	RESERVED	Go
1A8h	R424	RESERVED	Go
1A9h	R425	RESERVED	Go
1AAh	R426	RESERVED	Go
1ABh	R427	RESERVED	Go
1ACh	R428	RESERVED	Go
1ADh	R429	RESERVED	Go
1AEh	R430	DPLL1_TCXO_FB_PREDIV	Go
1AFh	R431	DPLL1_TCXO_FB_DIV_BY3	Go
1B0h	R432	DPLL1_TCXO_FB_DIV_BY2	Go
1B1h	R433	DPLL1_TCXO_FB_DIV_BY1	Go
1B2h	R434	DPLL1_TCXO_FB_DIV_BY0	Go
1B3h	R435	DPLL1_TCXO_NUM_BY4	Go
1B4h	R436	DPLL1_TCXO_NUM_BY3	Go
1B5h	R437	DPLL1_TCXO_NUM_BY2	Go
1B6h	R438	DPLL1_TCXO_NUM_BY1	Go
1B7h	R439	DPLL1_TCXO_NUM_BY0	Go
1B8h	R440	DPLL1_TCXO_MASHCTL	Go
1B9h	R441	DPLL2_GEN_CTL	Go
1BAh	R442	DPLL2_SWITCHOVER_TMR_EXP	Go
1BBh	R443	DPLL2_SWITCHOVER_TMR_MANT_BY1	Go
1BCh	R444	DPLL2_SWITCHOVER_TMR_MANT_BY0	Go
1BDh	R445	DPLL2_REF0_RDIV_BY1	Go
1BEh	R446	DPLL2_REF0_RDIV_BY0	Go
1BFh	R447	DPLL2_REF1_RDIV_BY1	Go
1C0h	R448	DPLL2_REF1_RDIV_BY0	Go

Table 1. LMK05028 Registers (continued)

Address	Acronym	Register Name	Section
1C1h	R449	DPLL2_REF2_RDIV_BY1	Go
1C2h	R450	DPLL2_REF2_RDIV_BY0	Go
1C3h	R451	DPLL2_REF3_RDIV_BY1	Go
1C4h	R452	DPLL2_REF3_RDIV_BY0	Go
1C5h	R453	RESERVED	Go
1C6h	R454	RESERVED	Go
1C7h	R455	DPLL2_REF5_RDIV_BY1	Go
1C8h	R456	DPLL2_REF5_RDIV_BY0	Go
1C9h	R457	DPLL2_REF_TDC_CTL	Go
1CAh	R458	DPLL2_REF_DLY_GEN	Go
1CBh	R459	RESERVED	Go
1CCh	R460	RESERVED	Go
1CDh	R461	RESERVED	Go
1CEh	R462	RESERVED	Go
1CFh	R463	RESERVED	Go
1D0h	R464	RESERVED	Go
1D1h	R465	RESERVED	Go
1D2h	R466	RESERVED	Go
1D3h	R467	RESERVED	Go
1D4h	R468	RESERVED	Go
1D5h	R469	RESERVED	Go
1D6h	R470	RESERVED	Go
1D7h	R471	RESERVED	Go
1D8h	R472	RESERVED	Go
1D9h	R473	RESERVED	Go
1DAh	R474	RESERVED	Go
1DBh	R475	RESERVED	Go
1DCh	R476	RESERVED	Go
1DDh	R477	RESERVED	Go
1DEh	R478	RESERVED	Go
1DFh	R479	RESERVED	Go
1E0h	R480	RESERVED	Go
1E1h	R481	RESERVED	Go
1E2h	R482	RESERVED	Go
1E3h	R483	RESERVED	Go
1E4h	R484	RESERVED	Go
1E5h	R485	RESERVED	Go
1E6h	R486	RESERVED	Go
1E7h	R487	RESERVED	Go
1E8h	R488	RESERVED	Go
1E9h	R489	RESERVED	Go
1EAh	R490	RESERVED	Go
1EBh	R491	RESERVED	Go
1ECh	R492	RESERVED	Go
1EDh	R493	RESERVED	Go
1EEh	R494	RESERVED	Go
1EFh	R495	RESERVED	Go

Table 1. LMK05028 Registers (continued)

Address	Acronym	Register Name	Section
1F0h	R496	RESERVED	Go
1F1h	R497	RESERVED	Go
1F2h	R498	RESERVED	Go
1F3h	R499	RESERVED	Go
1F4h	R500	DPLL2_CLK_FB_DIV	Go
1F5h	R501	DPLL2_REF_FB_PREDIV	Go
1F6h	R502	DPLL2_REF_FB_DIV_BY3	Go
1F7h	R503	DPLL2_REF_FB_DIV_BY2	Go
1F8h	R504	DPLL2_REF_FB_DIV_BY1	Go
1F9h	R505	DPLL2_REF_FB_DIV_BY0	Go
1FAh	R506	DPLL2_REF_NUM_BY4	Go
1FBh	R507	DPLL2_REF_NUM_BY3	Go
1FCh	R508	DPLL2_REF_NUM_BY2	Go
1FDh	R509	DPLL2_REF_NUM_BY1	Go
1FEh	R510	DPLL2_REF_NUM_BY0	Go
1FFh	R511	DPLL2_REF_DEN_BY4	Go
200h	R512	DPLL2_REF_DEN_BY3	Go
201h	R513	DPLL2_REF_DEN_BY2	Go
202h	R514	DPLL2_REF_DEN_BY1	Go
203h	R515	DPLL2_REF_DEN_BY0	Go
204h	R516	DPLL2_REF_MASHCTL	Go
205h	R517	RESERVED	Go
206h	R518	RESERVED	Go
207h	R519	RESERVED	Go
208h	R520	RESERVED	Go
209h	R521	RESERVED	Go
20Ah	R522	RESERVED	Go
20Bh	R523	RESERVED	Go
20Ch	R524	RESERVED	Go
20Dh	R525	RESERVED	Go
20Eh	R526	RESERVED	Go
20Fh	R527	RESERVED	Go
210h	R528	RESERVED	Go
211h	R529	RESERVED	Go
212h	R530	RESERVED	Go
213h	R531	RESERVED	Go
214h	R532	RESERVED	Go
215h	R533	RESERVED	Go
216h	R534	RESERVED	Go
217h	R535	RESERVED	Go
218h	R536	RESERVED	Go
219h	R537	DPLL2_REF_SYNC_PH_OFFSET_BY5	Go
21Ah	R538	DPLL2_REF_SYNC_PH_OFFSET_BY4	Go
21Bh	R539	DPLL2_REF_SYNC_PH_OFFSET_BY3	Go
21Ch	R540	DPLL2_REF_SYNC_PH_OFFSET_BY2	Go
21Dh	R541	DPLL2_REF_SYNC_PH_OFFSET_BY1	Go
21Eh	R542	DPLL2_REF_SYNC_PH_OFFSET_BY0	Go

Table 1. LMK05028 Registers (continued)

Address	Acronym	Register Name	Section
21Fh	R543	RESERVED	Go
220h	R544	RESERVED	Go
221h	R545	RESERVED	Go
222h	R546	RESERVED	Go
223h	R547	DPLL2_TCXO_DLY_GEN	Go
224h	R548	RESERVED	Go
225h	R549	RESERVED	Go
226h	R550	RESERVED	Go
227h	R551	RESERVED	Go
228h	R552	RESERVED	Go
229h	R553	RESERVED	Go
22Ah	R554	RESERVED	Go
22Bh	R555	RESERVED	Go
22Ch	R556	RESERVED	Go
22Dh	R557	RESERVED	Go
22Eh	R558	RESERVED	Go
22Fh	R559	RESERVED	Go
230h	R560	RESERVED	Go
231h	R561	RESERVED	Go
232h	R562	RESERVED	Go
233h	R563	RESERVED	Go
234h	R564	RESERVED	Go
235h	R565	RESERVED	Go
236h	R566	RESERVED	Go
237h	R567	RESERVED	Go
238h	R568	RESERVED	Go
239h	R569	DPLL2_TCXO_FB_PREDIV	Go
23Ah	R570	DPLL2_TCXO_FB_DIV_BY3	Go
23Bh	R571	DPLL2_TCXO_FB_DIV_BY2	Go
23Ch	R572	DPLL2_TCXO_FB_DIV_BY1	Go
23Dh	R573	DPLL2_TCXO_FB_DIV_BY0	Go
23Eh	R574	DPLL2_TCXO_NUM_BY4	Go
23Fh	R575	DPLL2_TCXO_NUM_BY3	Go
240h	R576	DPLL2_TCXO_NUM_BY2	Go
241h	R577	DPLL2_TCXO_NUM_BY1	Go
242h	R578	DPLL2_TCXO_NUM_BY0	Go
243h	R579	DPLL2_TCXO_MASHCTL	Go
244h	R580	DPLL1_FDEV_CTL	Go
245h	R581	DPLL2_FDEV_CTL	Go
246h	R582	DPLL1_FDEV_BY4	Go
247h	R583	DPLL1_FDEV_BY3	Go
248h	R584	DPLL1_FDEV_BY2	Go
249h	R585	DPLL1_FDEV_BY1	Go
24Ah	R586	DPLL1_FDEV_BY0	Go
24Bh	R587	DPLL1_FDEV_REG_CTL	Go
24Ch	R588	DPLL2_FDEV_BY4	Go
24Dh	R589	DPLL2_FDEV_BY3	Go

Table 1. LMK05028 Registers (continued)

Address	Acronym	Register Name	Section
24Eh	R590	DPLL2_FDEV_BY2	Go
24Fh	R591	DPLL2_FDEV_BY1	Go
250h	R592	DPLL2_FDEV_BY0	Go
251h	R593	DPLL2_FDEV_REG_CTL	Go
252h	R594	DPLL1_ZDM_CTRL0	Go
253h	R595	RESERVED	Go
254h	R596	RESERVED	Go
255h	R597	RESERVED	Go
256h	R598	RESERVED	Go
257h	R599	RESERVED	Go
258h	R600	RESERVED	Go
259h	R601	RESERVED	Go
25Ah	R602	RESERVED	Go
25Bh	R603	RESERVED	Go
25Ch	R604	RESERVED	Go
25Dh	R605	RESERVED	Go
25Eh	R606	RESERVED	Go
25Fh	R607	RESERVED	Go
260h	R608	RESERVED	Go
261h	R609	RESERVED	Go
262h	R610	RESERVED	Go
263h	R611	RESERVED	Go
264h	R612	RESERVED	Go
265h	R613	RESERVED	Go
266h	R614	RESERVED	Go
267h	R615	RESERVED	Go
268h	R616	RESERVED	Go
269h	R617	RESERVED	Go
26Ah	R618	RESERVED	Go
26Bh	R619	RESERVED	Go
26Ch	R620	RESERVED	Go
26Dh	R621	RESERVED	Go
26Eh	R622	RESERVED	Go
26Fh	R623	RESERVED	Go
270h	R624	RESERVED	Go
271h	R625	RESERVED	Go
272h	R626	DPLL1_TUNING_FREE_RUN_BY4	Go
273h	R627	DPLL1_TUNING_FREE_RUN_BY3	Go
274h	R628	DPLL1_TUNING_FREE_RUN_BY2	Go
275h	R629	DPLL1_TUNING_FREE_RUN_BY1	Go
276h	R630	DPLL1_TUNING_FREE_RUN_BY0	Go
277h	R631	DPLL1_REF_HISTCTL	Go
278h	R632	DPLL1_REF_HISTCNT	Go
279h	R633	DPLL1_REF_HISTDLY_BY3	Go
27Ah	R634	DPLL1_REF_HISTDLY_BY2	Go
27Bh	R635	DPLL1_REF_HISTDLY_BY1	Go
27Ch	R636	DPLL1_REF_HISTDLY_BY0	Go

Table 1. LMK05028 Registers (continued)

Address	Acronym	Register Name	Section
27Dh	R637	DPLL2_TUNING_FREE_RUN_BY4	Go
27Eh	R638	DPLL2_TUNING_FREE_RUN_BY3	Go
27Fh	R639	DPLL2_TUNING_FREE_RUN_BY2	Go
280h	R640	DPLL2_TUNING_FREE_RUN_BY1	Go
281h	R641	DPLL2_TUNING_FREE_RUN_BY0	Go
282h	R642	DPLL2_REF_HISTCTL	Go
283h	R643	DPLL2_REF_HISTCNT	Go
284h	R644	DPLL2_REF_HISTDLY_BY3	Go
285h	R645	DPLL2_REF_HISTDLY_BY2	Go
286h	R646	DPLL2_REF_HISTDLY_BY1	Go
287h	R647	DPLL2_REF_HISTDLY_BY0	Go
2A4h	R676	SWRST1	Go
2A5h	R677	SWRST2	Go
2A6h	R678	RESERVED	Go
2A9h	R681	RESERVED	Go
2AAh	R682	RESERVED	Go
2ABh	R683	RESERVED	Go
2ACh	R684	RESERVED	Go
2ADh	R685	RESERVED	Go
2AEh	R686	RESERVED	Go
2AFh	R687	RESERVED	Go
2B0h	R688	RESERVED	Go
2B3h	R691	RESERVED	Go
2CBh	R715	RESERVED	Go
2CCh	R716	RESERVED	Go
2CDh	R717	RESERVED	Go
2CEh	R718	RESERVED	Go
2CFh	R719	RESERVED	Go
2E0h	R736	XOTSTCTRL	Go
2E5h	R741	RESERVED	Go
2E6h	R742	REFVALSTAT	Go
2FCh	R764	RESERVED	Go
2FEh	R766	RESERVED	Go
2FFh	R767	DPLL1_REFSEL_STAT	Go
302h	R770	RESERVED	Go
303h	R771	DPLL2_REFSEL_STAT	Go
307h	R775	RESERVED	Go
308h	R776	RESERVED	Go
310h	R784	RESERVED	Go
311h	R785	RESERVED	Go

Complex bit access types are encoded to fit into small table cells. Table 2 shows the codes that are used for access types in this section.

Table 2. LMK05028 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
W0C	0C W	0 to clear Write
W1C	1C W	1 to clear Write
Reset or Default Value		
-n		Value after reset or the default value

2.1 R0 Register (Address = 0h) [reset = 10h]

R0 is shown in Figure 1 and described in Table 3.

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Figure 1. R0 Register

7	6	5	4	3	2	1	0
VNDRID[15:8]							
R-10h							

Table 3. R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	VNDRID[15:8]	R	10h	Bits 15:8 of VNDRID

2.2 R1 Register (Address = 1h) [reset = Bh]

R1 is shown in Figure 2 and described in Table 4.

Return to Summary Table.

Figure 2. R1 Register

7	6	5	4	3	2	1	0
VNDRID							
R-Bh							

Table 4. R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	VNDRID	R	Bh	Vendor Identification Number Unique 16-bit number assigned to chip vendors. TI's vendor ID is 0x100B.

2.3 R2 Register (Address = 2h) [reset = 35h]

R2 is shown in Figure 3 and described in Table 5.

Return to Summary Table.

Figure 3. R2 Register

7	6	5	4	3	2	1	0
PRODID							
R-35h							

Table 5. R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PRODID	R	35h	Product Identification Number Unique 8-bit number used to identify the LMK05028.

2.4 R3 Register (Address = 3h) [reset = 0h]

R3 is shown in Figure 4 and described in Table 6.

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Figure 4. R3 Register

7	6	5	4	3	2	1	0
REVID							
R-0h							

Table 6. R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	REVID	R	0h	Device Revision Number Used to identify the mask-set revision.

2.5 R4 Register (Address = 4h) [reset = X]

R4 is shown in Figure 5 and described in Table 7.

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Figure 5. R4 Register

7	6	5	4	3	2	1	0
PRTID[31:24]							
R-X							

Table 7. R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PRTID[31:24]	R	X	Bits 31:24 of PRTID

2.6 R5 Register (Address = 5h) [reset = X]

R5 is shown in Figure 6 and described in Table 8.

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Figure 6. R5 Register

7	6	5	4	3	2	1	0
PRTID[23:16]							
R-X							

Table 8. R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PRTID[23:16]	R	X	Bits 23:16 of PRTID

2.7 R6 Register (Address = 6h) [reset = X]

R6 is shown in Figure 7 and described in Table 9.

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Figure 7. R6 Register

7	6	5	4	3	2	1	0
PRTID[15:8]							
R-X							

Table 9. R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PRTID[15:8]	R	X	Bits 15:8 of PRTID

2.8 R7 Register (Address = 7h) [reset = X]

R7 is shown in Figure 8 and described in Table 10.

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Figure 8. R7 Register

7	6	5	4	3	2	1	0
PRTID							
R-X							

Table 10. R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PRTID	R	X	Part Identification Number Unique 32-bit number used to serialize individual LMK05028 devices. Factory programmed. Cannot be modified by the user.

2.9 R8 Register (Address = 8h) [reset = 0h]

R8 is shown in Figure 9 and described in Table 11.

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Figure 9. R8 Register

7	6	5	4	3	2	1	0
RESERVED	HW_SW_CTRL_MODE	GPIO2_SW_MODE		HW_DFLT_MODE	OP_MODE		
R-0h	R-0h	R-0h		R-0h	R-0h		

Table 11. R8 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	HW_SW_CTRL_MODE	R	0h	HW_SW_CTRL Pin Configuration Reflects the values sampled on the HW_SW_CTRL pin during device power-on reset (POR). 0h = EEPROM/Soft Pin Mode 1h = ROM/Hard Pin Mode
5-4	GPIO2_SW_MODE	R	0h	GPIO2 Soft Pin Configuration Mode Reflects the value sampled on the GPIO2 pin when HW_SW_CTRL is 0 during POR. When HW_SW_CTRL is 1 this field reads back 0x0. 0h = Low 1h = High 2h = Mid / Float
3	HW_DFLT_MODE	R	0h	Hardware Default Mode Indicates if device is configured from the register hardware default values (when GPIO2=F and HW_SW_CTRL=0 during POR). 0h = EEPROM/ROM Mode 1h = Hardware Default Mode
2-0	OP_MODE	R	0h	Operating Mode The OP_MODE fields reflects the device operating mode as determined by the input levels on the HW_SW_CTRL, STATUS0, and STATUS1 pins respectively during POR. 0h = [F, F, F]: EEPROM + SPI Mode 1h = [F, 0/1, 0/1]: Reserved (Test Mode) 2h = [0, X, X]: EEPROM + I2C Mode 3h = [1, X, X]: ROM + I2C Mode where: F = Float or Mid (0.8 V) and X = Don't Care.

2.10 R9 Register (Address = 9h) [reset = 0h]

R9 is shown in Figure 10 and described in Table 12.

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Figure 10. R9 Register

7	6	5	4	3	2	1	0
RESERVED				GPIO_HW_MODE			
R-0h				R-0h			

Table 12. R9 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	
4-0	GPIO_HW_MODE	R	0h	GPIO[3:0] Hard Pin Configuration Mode Reflects the value sampled on the GPIO[3:0] pins when HW_SW_CTRL = 1 during POR. This corresponds to the ROM page.

2.11 R10 Register (Address = Ah) [reset = X]

R10 is shown in Figure 11 and described in Table 13.

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Figure 11. R10 Register

7	6	5	4	3	2	1	0
SLAVEADR_GPIO1_SW							RESERVED
R-X							R-X

Table 13. R10 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	SLAVEADR_GPIO1_SW	R	X	7-bit I2C Slave Address. The five MSBs (base address bits) are programmable in EEPROM, which is 11000b for generic factory devices. The two LSBs are determined by control input pin levels sampled during device POR. When the HW_SW_CTRL pin is 1, the two LSBs are fixed to 00b. When the HW_SW_CTRL pin is 0, the 2 LSBs are determined by input levels sampled on the GPIO2 and GPIO1 pins respectively.
0	RESERVED	R	X	

2.12 R11 Register (Address = Bh) [reset = X]

R11 is shown in Figure 12 and described in Table 14.

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Figure 12. R11 Register

7	6	5	4	3	2	1	0
EEREV							
R-X							

Table 14. R11 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	EEREV	R	X	EEPROM Image Revision ID EEPROM Image Revision automatically retrieved from EEPROM and reflected in the EEREV register after a reset or after a NVM commit operation.

2.13 R12 Register (Address = Ch) [reset = X]

R12 is shown in Figure 13 and described in Table 15.

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Figure 13. R12 Register

7	6	5	4	3	2	1	0
RESET_SW	SYNC_SW	RESERVED	SYNC_AUTO_APLL	SYNC_MUTE	RESERVED	PLLSTRTMODE	AUTOSTRT
R/W-0h	R/W-0h	R/W-X	R/W-X	R/W-X	R-X	R/W-X	R/W-X

Table 15. R12 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESET_SW	R/W	0h	Software Reset ALL functions Writing a 1 will cause the device to return to its power-up state apart from the registers and the configuration controller. The configuration controller is excluded to prevent a re-transfer of EEPROM data to on-chip registers.
6	SYNC_SW	R/W	0h	Output Synchronization (SYNC) Assert bit 0h = De-assert SYNC 1h = Assert SYNC
5	RESERVED	R/W	X	Reserved
4	SYNC_AUTO_APLL	R/W	X	Enable Automatic Output SYNC after PLL lock 0h = Disable Auto SYNC 1h = Enable Auto SYNC
3	SYNC_MUTE	R/W	X	Determines if the output drivers are muted during a SYNC event 0h = Do not mute any outputs during SYNC 1h = Mute all outputs during SYNC
2	RESERVED	R	X	
1	PLLSTRTMODE	R/W	X	PLL Startup Mode 0h = PLL2 will only be calibrated after PLL1 has achieved lock or PLL1 is powered down. 1h = Calibration sequence for both PLL's is run independently. At startup this means PLL1 and PLL2 will be calibrated in parallel. Additionally if PLL2 is subject to a Software Reset or Power down cycle then PLL2 re-calibration will restart regardless of the state of PLL1.
0	AUTOSTRT	R/W	X	Autostart If AUTOSTRT is set to 1, the device will automatically initiate the PLL and output start-up sequence after a device reset. A device reset can be triggered by the power-on-reset, PDN pin, or by writing to the RESET_SW bit. If AUTOSTRT is 0, the device will halt after the configuration phase; a subsequent write to set the AUTOSTRT bit will initiate the start-up sequence.

2.14 R13 Register (Address = Dh) [reset = 0h]

R13 is shown in Figure 14 and described in Table 16.

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Figure 14. R13 Register

7	6	5	4	3	2	1	0
RESERVED		LOS_FDET_TCXO	LOS_FDET_XO	LOL_PLL		LOS_TCXO	LOS_XO
R-0h		R-0h	R-0h	R-0h		R-0h	R-0h

Table 16. R13 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	
5	LOS_FDET_TCXO	R	0h	Loss of source freq detection TCXO
4	LOS_FDET_XO	R	0h	Loss of source freq detection XO
3-2	LOL_PLL	R	0h	Loss of Lock APLL[2:1]
1	LOS_TCXO	R	0h	Loss of source TCXO
0	LOS_XO	R	0h	Loss of source XO

2.15 R14 Register (Address = Eh) [reset = 0h]

R14 is shown in Figure 15 and described in Table 17.

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Figure 15. R14 Register

7	6	5	4	3	2	1	0
LOPL_DPLL1	LOFL_DPLL1	HIST1	HLDOVR1	REFSWITCH1	LOR_MISSCLK1	LOR_FREQ1	LOR_AMP1
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 17. R14 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LOPL_DPLL1	R	0h	Loss of phase lock DPLL1
6	LOFL_DPLL1	R	0h	Loss of freq lock DPLL1
5	HIST1	R	0h	Tuning word history update DPLL1
4	HLDOVR1	R	0h	Holdover event DPLL1
3	REFSWITCH1	R	0h	Reference switchover DPLL1
2	LOR_MISSCLK1	R	0h	Loss of active reference missing clk DPLL1
1	LOR_FREQ1	R	0h	Loss of active reference freq DPLL1
0	LOR_AMP1	R	0h	Loss of active reference amplitude DPLL1

2.16 R15 Register (Address = Fh) [reset = 0h]

R15 is shown in Figure 16 and described in Table 18.

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Figure 16. R15 Register

7	6	5	4	3	2	1	0
LOPL_DPLL2	LOFL_DPLL2	HIST2	HLDOVR2	REFSWITCH2	LOR_MISSCLK2	LOR_FREQ2	LOR_AMP2
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 18. R15 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LOPL_DPLL2	R	0h	Loss of phase lock DPLL2
6	LOFL_DPLL2	R	0h	Loss of freq lock DPLL2
5	HIST2	R	0h	Tuning word history update DPLL2
4	HLDOVR2	R	0h	Holdover event DPLL2

Table 18. R15 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	REFSWITCH2	R	0h	Reference switchover DPLL2
2	LOR_MISSCLK2	R	0h	Loss of active reference missing clk DPLL2
1	LOR_FREQ2	R	0h	Loss of active reference freq DPLL2
0	LOR_AMP2	R	0h	Loss of active reference amplitude DPLL2

2.17 R16 Register (Address = 10h) [reset = X]

R16 is shown in Figure 17 and described in Table 19.

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Figure 17. R16 Register

7	6	5	4	3	2	1	0
RESERVED		LOS_FDET_TCXO_MASK	LOS_FDET_XO_MASK	LOL_PLL2_MASK	LOL_PLL1_MASK	LOS_TCXO_MASK	LOS_XO_MASK
R-X		R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X

Table 19. R16 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	
5	LOS_FDET_TCXO_MASK	R/W	X	Mask Loss of Source Freq Det TCXO 1h = Interrupt source is masked and will not cause the interrupt signal to be activated.
4	LOS_FDET_XO_MASK	R/W	X	Mask Loss of Source Freq Det XO 1h = The LOS_FDET_XO interrupt source is masked and will not cause the interrupt signal to be activated.
3	LOL_PLL2_MASK	R/W	X	Mask Loss of Lock APLL2 1h = The LOL_PLL2 interrupt source is masked and will not cause the interrupt signal to be activated.
2	LOL_PLL1_MASK	R/W	X	Mask Loss of Lock APLL1 1h = The LOL_PLL1 interrupt source is masked and will not cause the interrupt signal to be activated.
1	LOS_TCXO_MASK	R/W	X	Mask Loss of source TCXO 1h = The LOS_TCXO interrupt source is masked and will not cause the interrupt signal to be activated.
0	LOS_XO_MASK	R/W	X	Mask Loss of source XO 1h = The LOS_XO interrupt source is masked and will not cause the interrupt signal to be activated.

2.18 R17 Register (Address = 11h) [reset = X]

R17 is shown in Figure 18 and described in Table 20.

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Figure 18. R17 Register

7	6	5	4	3	2	1	0
LOPL_DPLL1_MASK	LOFL_DPLL1_MASK	HIST1_MASK	HLDOVR1_MASK	REFSWITCH1_MASK	LOR_MISSCLK1_MASK	LOR_FREQ1_MASK	LOR_AMP1_MASK
R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X

Table 20. R17 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LOPL_DPLL1_MASK	R/W	X	Mask Loss of Phase Lock DPLL1 1h = The LOPL_DPLL1 interrupt source is masked and will not cause the interrupt signal to be activated.
6	LOFL_DPLL1_MASK	R/W	X	Mask Loss of Freq Lock DPLL1 1h = The LOFL_DPLL1 interrupt source is masked and will not cause the interrupt signal to be activated.
5	HIST1_MASK	R/W	X	Mask Tuning word history update DPLL1 1h = The HIST1 interrupt source is masked and will not cause the interrupt signal to be activated.
4	HLDOVR1_MASK	R/W	X	Mask Holdover event DPLL1 1h = The HLDOVR1 interrupt source is masked and will not cause the interrupt signal to be activated.
3	REFSWITCH1_MASK	R/W	X	Mask Reference switchover DPLL1 1h = The REFSWITCH1 interrupt source is masked and will not cause the interrupt signal to be activated.
2	LOR_MISSCLK1_MASK	R/W	X	Loss of active reference missing clk DPLL1 1h = The LOR_MISSCLK1 interrupt source is masked and will not cause the interrupt signal to be activated.
1	LOR_FREQ1_MASK	R/W	X	Loss of active reference freq DPLL1 1h = The LOR_FREQ1 interrupt source is masked and will not cause the interrupt signal to be activated.
0	LOR_AMP1_MASK	R/W	X	Mask Loss of active reference amplitude DPLL1 1h = The LOR_AMP1 interrupt source is masked and will not cause the interrupt signal to be activated.

2.19 R18 Register (Address = 12h) [reset = X]

R18 is shown in Figure 19 and described in Table 21.

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Figure 19. R18 Register

7	6	5	4	3	2	1	0
LOPL_DPLL2_MASK	LOFL_DPLL2_MASK	HIST2_MASK	HLDOVR2_MASK	REFSWITCH2_MASK	LOR_MISSCLK2_MASK	LOR_FREQ2_MASK	LOR_AMP2_MASK
R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X

Table 21. R18 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LOPL_DPLL2_MASK	R/W	X	Mask Loss of Phase Lock DPLL2 1h = The LOPL_DPLL2 interrupt source is masked and will not cause the interrupt signal to be activated.
6	LOFL_DPLL2_MASK	R/W	X	Mask Loss of Freq Lock DPLL1 1h = The LOFL_DPLL2 interrupt source is masked and will not cause the interrupt signal to be activated.
5	HIST2_MASK	R/W	X	Mask Tuning word history update DPLL2 1h = The HIST2 interrupt source is masked and will not cause the interrupt signal to be activated.
4	HLDOVR2_MASK	R/W	X	Mask Holdover event DPLL2 1h = The HLDOVR2 interrupt source is masked and will not cause the interrupt signal to be activated.

Table 21. R18 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	REFSWITCH2_MASK	R/W	X	Mask Reference switchover DPLL2 1h = The REFSWITCH2 interrupt source is masked and will not cause the interrupt signal to be activated.
2	LOR_MISSCLK2_MASK	R/W	X	Loss of active reference missing clk DPLL2 1h = The LOR_MISSCLK2 interrupt source is masked and will not cause the interrupt signal to be activated.
1	LOR_FREQ2_MASK	R/W	X	Loss of active reference freq DPLL2 1h = The LOR_FREQ2 interrupt source is masked and will not cause the interrupt signal to be activated.
0	LOR_AMP2_MASK	R/W	X	Mask Loss of active reference amplitude DPLL2 1h = The LOR_AMP2 interrupt source is masked and will not cause the interrupt signal to be activated.

2.20 R19 Register (Address = 13h) [reset = X]

R19 is shown in Figure 20 and described in Table 22.

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Figure 20. R19 Register

7	6	5	4	3	2	1	0
RESERVED		LOS_FDET_TCXO_POL	LOS_FDET_XO_POL	LOL_PLL2_POL	LOL_PLL1_POL	LOS_TCXO_POL	LOS_XO_POL
R-X		R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X

Table 22. R19 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	
5	LOS_FDET_TCXO_POL	R/W	X	LOS_FDET_TCXO Flag Polarity 0h = A falling edge on LOS_FDET_TCXO will set the LOS_FDET_TCXO_INTR bit. 1h = A rising edge on LOS_FDET_TCXO will set the LOS_FDET_TCXO_INTR bit of the INT_FLAG0 register.
4	LOS_FDET_XO_POL	R/W	X	LOS_FDET_XO Flag Polarity 0h = A falling edge on LOS_FDET_XO will set the LOS_FDET_XO_INTR bit. 1h = A rising edge on LOS_FDET_XO will set the LOS_FDET_XO_INTR bit of the INT_FLAG0 register.
3	LOL_PLL2_POL	R/W	X	LOL_PLL2 Flag Polarity 0h = A falling edge on LOL_PLL2 will set the LOL_PLL2_INTR bit. 1h = A rising edge on LOS2 will set the LOL_PLL2_INTR bit of the INT_FLAG0 register.
2	LOL_PLL1_POL	R/W	X	LOL_PLL1 Flag Polarity 0h = A falling edge on LOL_PLL1 will set the LOL_PLL1_INTR bit. 1h = A rising edge on LOL_PLL1 will set the LOL_PLL1_INTR bit of the INT_FLAG0 register.
1	LOS_TCXO_POL	R/W	X	LOS_TCXO Flag Polarity 0h = A falling edge on LOS_TCXO will set the LOS_TCXO_INTR bit. 1h = A rising edge on LOS_TCXO will set the LOS_TCXO_INTR bit of the INT_FLAG0 register.

Table 22. R19 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	LOS_XO_POL	R/W	X	LOS_XO Flag Polarity 0h = A falling edge on LOS_XO will set the LOS_XO_INTR bit. 1h = A rising edge on LOS_XO will set the LOS_XO_INTR bit of the INT_FLAG0 register.

2.21 R20 Register (Address = 14h) [reset = X]

R20 is shown in Figure 21 and described in Table 23.

Return to Summary Table.

Figure 21. R20 Register

7	6	5	4	3	2	1	0
LOPL_DPLL1_POL	LOFL_DPLL1_POL	HIST1_POL	HLDOVR1_POL	REFSWITCH1_POL	LOR_MISSCLK1_POL	LOR_FREQ1_POL	LOR_AMP1_POL
R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X

Table 23. R20 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LOPL_DPLL1_POL	R/W	X	LOPL_DPLL1 Flag Polarity 0h = A falling edge on LOPL_DPLL1 will set the LOPL_DPLL1_INTR bit. 1h = A rising edge on LOPL_DPLL1 will set the LOPL_DPLL1_INTR bit of the INT_FLAG1 register.
6	LOFL_DPLL1_POL	R/W	X	LOFL_DPLL1 Flag Polarity 0h = A falling edge on LOFL_DPLL1 will set the LOFL_DPLL1_INTR bit. 1h = A rising edge on LOFL_DPLL1 will set the LOFL_DPLL1_INTR bit of the INT_FLAG1 register.
5	HIST1_POL	R/W	X	HIST1 Flag Polarity 0h = A falling edge on HIST1 will set the HIST1_INTR bit. 1h = A rising edge on HIST1 will set the HIST1_INTR bit of the INT_FLAG1 register.
4	HLDOVR1_POL	R/W	X	HLDOVR1 Flag Polarity 0h = A falling edge on HLDOVR1 will set the HLDOVR1_INTR bit. 1h = A rising edge on HLDOVR1 will set the HLDOVR1_INTR bit of the INT_FLAG1 register.
3	REFSWITCH1_POL	R/W	X	REFSWITCH1 Flag Polarity 0h = A falling edge on REFSWITCH1 will set the REFSWITCH1_INTR bit. 1h = A rising edge on REFSWITCH1 will set the REFSWITCH1_INTR bit of the INT_FLAG1 register.
2	LOR_MISSCLK1_POL	R/W	X	LOR_MISSCLK1 Flag Polarity 0h = A falling edge on LOR_MISSCLK1 will set the LOR_MISSCLK1_INTR bit. 1h = A rising edge on LOR_MISSCLK1 will set the LOR_MISSCLK1_INTR bit of the INT_FLAG1 register.
1	LOR_FREQ1_POL	R/W	X	LOR_FREQ1 Flag Polarity 0h = A falling edge on LOR_FREQ1 will set the LOR_FREQ1_INTR bit. 1h = A rising edge on LOR_FREQ1 will set the LOR_FREQ1_INTR bit of the INT_FLAG1 register.

Table 23. R20 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	LOR_AMP1_POL	R/W	X	LOR_AMP1 Flag Polarity 0h = A falling edge on LOR_AMP1 will set the LOR_AMP1_INTR bit. 1h = A rising edge on LOR_AMP1 will set the LOR_AMP1_INTR bit of the INT_FLAG1 register.

2.22 R21 Register (Address = 15h) [reset = X]

R21 is shown in Figure 22 and described in Table 24.

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Figure 22. R21 Register

7	6	5	4	3	2	1	0
LOPL_DPLL2_POL	LOFL_DPLL2_POL	HIST2_POL	HLDOVR2_POL	REFSWITCH2_POL	LOR_MISSCLK2_POL	LOR_FREQ2_POL	LOR_AMP2_POL
R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X

Table 24. R21 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LOPL_DPLL2_POL	R/W	X	LOPL_DPLL2 Flag Polarity 0h = A falling edge on LOPL_DPLL2 will set the LOPL_DPLL2_INTR bit. 1h = A rising edge on LOPL_DPLL2 will set the LOPL_DPLL2_INTR bit of the INT_FLAG2 register.
6	LOFL_DPLL2_POL	R/W	X	LOFL_DPLL2 Flag Polarity 0h = A falling edge on LOFL_DPLL2 will set the LOFL_DPLL2_INTR bit. 1h = A rising edge on LOFL_DPLL2 will set the LOFL_DPLL2_INTR bit of the INT_FLAG2 register.
5	HIST2_POL	R/W	X	HIST2 Flag Polarity 0h = A falling edge on HIST2 will set the HIST2_INTR bit. 1h = A rising edge on HIST2 will set the HIST2_INTR bit of the INT_FLAG2 register.
4	HLDOVR2_POL	R/W	X	HLDOVR2 Flag Polarity 0h = A falling edge on HLDOVR2 will set the HLDOVR2_INTR bit. 1h = A rising edge on HLDOVR2 will set the HLDOVR2_INTR bit of the INT_FLAG2 register.
3	REFSWITCH2_POL	R/W	X	REFSWITCH2 Flag Polarity 0h = A falling edge on REFSWITCH2 will set the REFSWITCH2_INTR bit. 1h = A rising edge on REFSWITCH2 will set the REFSWITCH2_INTR bit of the INT_FLAG2 register.
2	LOR_MISSCLK2_POL	R/W	X	LOR_MISSCLK2 Flag Polarity 0h = A falling edge on LOR_MISSCLK2 will set the LOR_MISSCLK2_INTR bit. 1h = A rising edge on LOR_MISSCLK2 will set the LOR_MISSCLK2_INTR bit of the INT_FLAG2 register.
1	LOR_FREQ2_POL	R/W	X	LOR_FREQ2 Flag Polarity 0h = A falling edge on LOR_FREQ2 will set the LOR_FREQ2_INTR bit. 1h = A rising edge on LOR_FREQ2 will set the LOR_FREQ2_INTR bit of the INT_FLAG2 register.

Table 24. R21 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	LOR_AMP2_POL	R/W	X	LOR_AMP2 Flag Polarity 0h = A falling edge on LOR_AMP2 will set the LOR_AMP2_INTR bit. 1h = A rising edge on LOR_AMP2 will set the LOR_AMP2_INTR bit of the INT_FLAG2 register.

2.23 R22 Register (Address = 16h) [reset = 0h]

R22 is shown in Figure 23 and described in Table 25.

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Figure 23. R22 Register

7	6	5	4	3	2	1	0
RESERVED		LOS_FDET_TCXO_INTR	LOS_FDET_XO_INTR	LOL_PLL2_INTR	LOL_PLL1_INTR	LOS_TCXO_INTR	LOS_XO_INTR
R-0h		R/W0C-0h	R/W0C-0h	R/W0C-0h	R/W0C-0h	R/W0C-0h	R/W0C-0h

Table 25. R22 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	
5	LOS_FDET_TCXO_INTR	R/W0C	0h	LOL_FDET_TCXO Interrupt Bit is set when an edge of the correct polarity is detected on the interrupt source. The bt is cleared by writing a 0.
4	LOS_FDET_XO_INTR	R/W0C	0h	LOL_FDET_XO Interrupt Bit is set when an edge of the correct polarity is detected on the LOL_FDET_XO interrupt source. The bit is cleared by writing a 0.
3	LOL_PLL2_INTR	R/W0C	0h	LOL_PLL2 Interrupt Bit is set when an edge of the correct polarity is detected on the LOL_PLL2 interrupt source. The bit is cleared by writing a 0.
2	LOL_PLL1_INTR	R/W0C	0h	LOL_PLL1 Interrupt Bit is set when an edge of the correct polarity is detected on the LOL_PLL1 interrupt source.The bit is cleared by writing a 0.
1	LOS_TCXO_INTR	R/W0C	0h	LOS_TCXO Interrupt Bit is set when an edge of the correct polarity is detected on the LOS_TCXO interrupt source. The bit is cleared by writing a 0.
0	LOS_XO_INTR	R/W0C	0h	LOS_XO Interrupt Bit is set when an edge of the correct polarity is detected on the LOS_XO interrupt source. The bit is cleared by writing a 0.

2.24 R23 Register (Address = 17h) [reset = 0h]

R23 is shown in Figure 24 and described in Table 26.

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Figure 24. R23 Register

7	6	5	4	3	2	1	0
LOPL_DPLL1_INTR	LOFL_DPLL1_INTR	HIST1_INTR	HLDOVR1_INTR	REFSWITCH1_INTR	LOR_MISSCLK1_INTR	LOR_FREQ1_INTR	LOR_AMP1_INTR
R/W0C-0h	R/W0C-0h	R/W0C-0h	R/W0C-0h	R/W0C-0h	R/W0C-0h	R/W0C-0h	R/W0C-0h

Table 26. R23 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LOPL_DPLL1_INTR	R/W0C	0h	LOPL_DPLL1 Interrupt Bt is set when an edge of the correct polarity is detected on the LOPL_DPLL1 interrupt source. The bit is cleared by writing a 0.
6	LOFL_DPLL1_INTR	R/W0C	0h	LOFL_DPLL1 Interrupt Bit is set when an edge of the correct polarity is detected on the LOFL_DPLL1 interrupt source. The bit is cleared by writing a 0.
5	HIST1_INTR	R/W0C	0h	HIST1 Interrupt Bit is set when an edge of the correct polarity is detected on the HIST1 interrupt source. The bit is cleared by writing a 0.
4	HLDOVR1_INTR	R/W0C	0h	HLDOVR1 Interrupt Bit is set when an edge of the correct polarity is detected on the HLDOVR1 interrupt source. The bit is cleared by writing a 0.
3	REFSWITCH1_INTR	R/W0C	0h	REFSWITCH1 Interrupt Bit is set when an edge of the correct polarity is detected on the REFSWITCH1 interrupt source. The bit is cleared by writing a 0.
2	LOR_MISSCLK1_INTR	R/W0C	0h	LOR_MISSCLK1 Interrupt Bit is set when an edge of the correct polarity is detected on the LOR_MISSCLK1 interrupt source. The bit is cleared by writing a 0.
1	LOR_FREQ1_INTR	R/W0C	0h	LOR_FREQ1 Interrupt Bit is set when an edge of the correct polarity is detected on the LOR_FREQ1 interrupt source. The bit is cleared by writing a 0.
0	LOR_AMP1_INTR	R/W0C	0h	LOR_AMP1 Interrupt Bit is set when an edge of the correct polarity is detected on the LOR_AMP1 interrupt source. The bit is cleared by writing a 0.

2.25 R24 Register (Address = 18h) [reset = 0h]

R24 is shown in Figure 25 and described in Table 27.

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Figure 25. R24 Register

7	6	5	4	3	2	1	0
LOPL_DPLL2_INTR	LOFL_DPLL2_INTR	HIST2_INTR	HLDOVR2_INTR	REFSWITCH2_INTR	LOR_MISSCLK2_INTR	LOR_FREQ2_INTR	LOR_AMP2_INTR
R/W0C-0h	R/W0C-0h	R/W0C-0h	R/W0C-0h	R/W0C-0h	R/W0C-0h	R/W0C-0h	R/W0C-0h

Table 27. R24 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LOPL_DPLL2_INTR	R/W0C	0h	LOPL_DPLL2 Interrupt Bit is set when an edge of the correct polarity is detected on the LOPL_DPLL2 interrupt source. The bit is cleared by writing a 0.
6	LOFL_DPLL2_INTR	R/W0C	0h	LOFL_DPLL2 Interrupt Bit is set when an edge of the correct polarity is detected on the LOFL_DPLL2 interrupt source. The bit is cleared by writing a 0.
5	HIST2_INTR	R/W0C	0h	HIST2 Interrupt Bit is set when an edge of the correct polarity is detected on the HIST2 interrupt source. The bit is cleared by writing a 0.
4	HLDOVR2_INTR	R/W0C	0h	HLDOVR2 Interrupt Bit is set when an edge of the correct polarity is detected on the HLDOVR2 interrupt source. The bit is cleared by writing a 0.

Table 27. R24 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	REFSWITCH2_INTR	R/W0C	0h	REFSWITCH2 Interrupt Bit is set when an edge of the correct polarity is detected on the REFSWITCH2 interrupt source. The bit is cleared by writing a 0.
2	LOR_MISSCLK2_INTR	R/W0C	0h	LOR_MISSCLK2 Interrupt Bit is set when an edge of the correct polarity is detected on the LOR_MISSCLK2 interrupt source. The bit is cleared by writing a 0.
1	LOR_FREQ2_INTR	R/W0C	0h	LOR_FREQ2 Interrupt Bit is set when an edge of the correct polarity is detected on the LOR_FREQ2 interrupt source. The bit is cleared by writing a 0.
0	LOR_AMP2_INTR	R/W0C	0h	LOR_AMP2 Interrupt Bit is set when an edge of the correct polarity is detected on the LOR_AMP2 interrupt source. The bit is cleared by writing a 0.

2.26 R25 Register (Address = 19h) [reset = X]

R25 is shown in Figure 26 and described in Table 28.

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Figure 26. R25 Register

7	6	5	4	3	2	1	0
RESERVED						INT_AND_OR	INT_EN
R-X						R/W-X	R/W-X

Table 28. R25 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	X	
1	INT_AND_OR	R/W	X	Interrupt Logical AND or OR Combination 0h = OR: Any un-masked interrupt flags can generate an interrupt 1h = AND: All un-masked interrupt flags must be active in order to generate an interrupt.
0	INT_EN	R/W	X	Interrupt Enable 0h = Interrupt circuit disabled. Interrupts cannot be signaled on STATUS pins and INT_FLAG registers will not be updated. INT_LIVE registers will still reflect current state of internal interrupt signals. 1h = Interrupt circuit enabled

2.27 R26 Register (Address = 1Ah) [reset = X]

R26 is shown in Figure 27 and described in Table 29.

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Figure 27. R26 Register

7	6	5	4	3	2	1	0
RESERVED				RESERVED			
R-X				R/W-X			

Table 29. R26 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	X	
3-0	RESERVED	R/W	X	Reserved

2.28 R27 Register (Address = 1Bh) [reset = X]

R27 is shown in Figure 28 and described in Table 30.

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Figure 28. R27 Register

7	6	5	4	3	2	1	0
CH3_MUTE_LVL		CH2_MUTE_LVL		CH1_MUTE_LVL		CH0_MUTE_LVL	
R/W-X		R/W-X		R/W-X		R/W-X	

Table 30. R27 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	CH3_MUTE_LVL	R/W	X	Output X Mute Level. See CH0_MUTE_LVL for description and bit settings.
5-4	CH2_MUTE_LVL	R/W	X	Output X Mute Level. See CH0_MUTE_LVL for description and bit settings.
3-2	CH1_MUTE_LVL	R/W	X	Output X Mute Level. See CH0_MUTE_LVL for description and bit settings.
1-0	CH0_MUTE_LVL	R/W	X	Output X Mute Level Determines the configuration of the Output Driver during mute. 0h = Bypass Mute 1h = DIFF/HCSL: Mute to Diff. Vocm. LVCMOS: P=Bypass Mute, N=Mute Low 2h = DIFF/HCSL: Mute to Diff. High. LVCMOS: P=Mute Low, N=Bypass Mute 3h = DIFF/HCSL: Mute to Diff. Low. LVCMOS: P=Mute Low, N=Mute Low

2.29 R28 Register (Address = 1Ch) [reset = X]

R28 is shown in Figure 29 and described in Table 31.

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Figure 29. R28 Register

7	6	5	4	3	2	1	0
CH7_MUTE_LVL		CH6_MUTE_LVL		CH5_MUTE_LVL		CH4_MUTE_LVL	
R/W-X		R/W-X		R/W-X		R/W-X	

Table 31. R28 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	CH7_MUTE_LVL	R/W	X	Output X Mute Level. See CH0_MUTE_LVL for description and bit settings.
5-4	CH6_MUTE_LVL	R/W	X	Output X Mute Level. See CH0_MUTE_LVL for description and bit settings.
3-2	CH5_MUTE_LVL	R/W	X	Output X Mute Level. See CH0_MUTE_LVL for description and bit settings.

Table 31. R28 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1-0	CH4_MUTE_LVL	R/W	X	Output X Mute Level. See CH0_MUTE_LVL for description and bit settings.

2.30 R29 Register (Address = 1Dh) [reset = X]

R29 is shown in Figure 30 and described in Table 32.

Return to Summary Table.

Figure 30. R29 Register

7	6	5	4	3	2	1	0
CH_7_MUTE	CH_6_MUTE	CH_5_MUTE	CH_4_MUTE	CH_3_MUTE	CH_2_MUTE	CH_1_MUTE	CH_0_MUTE
R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X

Table 32. R29 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CH_7_MUTE	R/W	X	Output X Mute Control. See CH_0_MUTE for bit settings.
6	CH_6_MUTE	R/W	X	Output X Mute Control. See CH_0_MUTE for bit settings.
5	CH_5_MUTE	R/W	X	Output X Mute Control. See CH_0_MUTE for bit settings.
4	CH_4_MUTE	R/W	X	Output X Mute Control. See CH_0_MUTE for bit settings.
3	CH_3_MUTE	R/W	X	Output X Mute Control. See CH_0_MUTE for bit settings.
2	CH_2_MUTE	R/W	X	Output X Mute Control. See CH_0_MUTE for bit settings.
1	CH_1_MUTE	R/W	X	Output X Mute Control. See CH_0_MUTE for bit settings.
0	CH_0_MUTE	R/W	X	Output X Mute Control 0h = Output will operate regardless of the state of the selected clock source. 1h = Output will be auto-muted when the selected clock source is invalid (e.g. LOL or LOS)

2.31 R30 Register (Address = 1Eh) [reset = X]

R30 is shown in Figure 31 and described in Table 33.

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Figure 31. R30 Register

7	6	5	4	3	2	1	0
CH3_SLEW_RATE		CH2_SLEW_RATE		CH1_SLEW_RATE		CH0_SLEW_RATE	
R/W-X		R/W-X		R/W-X		R/W-X	

Table 33. R30 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	CH3_SLEW_RATE	R/W	X	Output X Driver Slew Rate 0h = Fast 1h = Nominal
5-4	CH2_SLEW_RATE	R/W	X	Output X Driver Slew Rate 0h = Fast 1h = Nominal

Table 33. R30 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-2	CH1_SLEW_RATE	R/W	X	Output X Driver Slew Rate 0h = Fast 1h = Nominal
1-0	CH0_SLEW_RATE	R/W	X	Output X Driver Slew Rate 0h = Fast 1h = Nominal

2.32 R31 Register (Address = 1Fh) [reset = X]

R31 is shown in Figure 32 and described in Table 34.

Return to Summary Table.

Figure 32. R31 Register

7	6	5	4	3	2	1	0
CH7_SLEW_RATE		CH6_SLEW_RATE		CH5_SLEW_RATE		CH4_SLEW_RATE	
R/W-X		R/W-X		R/W-X		R/W-X	

Table 34. R31 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	CH7_SLEW_RATE	R/W	X	Output X Driver Slew Rate 0h = Fast 1h = Nominal
5-4	CH6_SLEW_RATE	R/W	X	Output X Driver Slew Rate 0h = Fast 1h = Nominal
3-2	CH5_SLEW_RATE	R/W	X	Output X Driver Slew Rate 0h = Fast 1h = Nominal
1-0	CH4_SLEW_RATE	R/W	X	Output X Driver Slew Rate 0h = Fast 1h = Nominal

2.33 R32 Register (Address = 20h) [reset = X]

R32 is shown in Figure 33 and described in Table 35.

Return to Summary Table.

Figure 33. R32 Register

7	6	5	4	3	2	1	0
RESERVED						RESERVED	
R-X						R/W-X	

Table 35. R32 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	X	
1-0	RESERVED	R/W	X	Reserved

2.34 R33 Register (Address = 21h) [reset = X]

R33 is shown in Figure 34 and described in Table 36.

Return to Summary Table.

Figure 34. R33 Register

7	6	5	4	3	2	1	0
RESERVED				RESERVED		RESERVED	
R-X				R/W-X		R/W-X	

Table 36. R33 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	X	
3-2	RESERVED	R/W	X	Reserved
1-0	RESERVED	R/W	X	Reserved

2.35 R34 Register (Address = 22h) [reset = X]

R34 is shown in Figure 35 and described in Table 37.

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Figure 35. R34 Register

7	6	5	4	3	2	1	0
RESERVED				RESERVED		LVL_SEL_XO_DIFF	
R-X				R/W-X		R/W-X	

Table 37. R34 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	X	
3-2	RESERVED	R/W	X	Reserved
1-0	LVL_SEL_XO_DIFF	R/W	X	XO Input Amplitude Detector Specifies the minimum differential input peak-to-peak swing to be qualified.

2.36 R35 Register (Address = 23h) [reset = X]

R35 is shown in Figure 36 and described in Table 38.

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Figure 36. R35 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 38. R35 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.37 R36 Register (Address = 24h) [reset = X]

R36 is shown in Figure 37 and described in Table 39.

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Figure 37. R36 Register

7	6	5	4	3	2	1	0
RESERVED				XO_FDET_BYP	XO_DETECT_BYP	XO_BUFSEL	
R-X				R/W-X	R/W-X	R/W-X	

Table 39. R36 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	X	
3	XO_FDET_BYP	R/W	X	XO Frequency Detector Bypass If bypassed, the XO detector status is ignored and the XO input is considered valid by the PLL control state machines 0h = Detector Enabled 1h = Detector Bypassed (Ignored)
2	XO_DETECT_BYP	R/W	X	XO Amplitude Detector Bypass If bypassed, the XO input is considered to be valid by the PLL control state machines. XO_DETECT_BYP bit has no effect on the Interrupt register or status outputs. 0h = Detector Enabled 1h = Detector Bypassed (Ignored)
1-0	XO_BUFSEL	R/W	X	XO Input Buffer Enable 0h = Disable 3h = Enable

2.38 R37 Register (Address = 25h) [reset = X]

R37 is shown in Figure 38 and described in Table 40.

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Figure 38. R37 Register

7	6	5	4	3	2	1	0
RESERVED				RESERVED			
R-X				R/W-X			

Table 40. R37 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	X	
3-0	RESERVED	R/W	X	Reserved

2.39 R38 Register (Address = 26h) [reset = X]

R38 is shown in Figure 39 and described in Table 41.

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Figure 39. R38 Register

7	6	5	4	3	2	1	0
RESERVED		RESERVED	RESERVED	RESERVED	RESERVED		
R-X			R/W-X	R/W-X			

Table 41. R38 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	
4	RESERVED	R/W	X	Reserved
3	RESERVED	R/W	X	Reserved
3-0	XO_DIFF_TYPE	R/W	X	XO Input Type 0h = 2.5-V LVCMOS or DC-DIFF (Internal termination and biasing off) 1h = AC-DIFF (Internal termination off and biasing on) 2h = AC-DIFF (Internal 100-Ω differential and biasing on) 4h = HCSL (Internal 50-Ω to GND and biasing off)

2.40 R39 Register (Address = 27h) [reset = X]

R39 is shown in Figure 40 and described in Table 42.

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Figure 40. R39 Register

7	6	5	4	3	2	1	0
RESERVED						RESERVED	
R-X						R/W-X	

Table 42. R39 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	X	
1-0	RESERVED	R/W	X	Reserved

2.41 R40 Register (Address = 28h) [reset = X]

R40 is shown in Figure 41 and described in Table 43.

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Figure 41. R40 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 43. R40 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.42 R41 Register (Address = 29h) [reset = X]

R41 is shown in Figure 42 and described in Table 44.

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Figure 42. R41 Register

7	6	5	4	3	2	1	0
RESERVED						RESERVED	
R-X						R/W-X	

Table 44. R41 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	X	
1-0	RESERVED	R/W	X	Reserved

2.43 R42 Register (Address = 2Ah) [reset = X]

R42 is shown in Figure 43 and described in Table 45.

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Figure 43. R42 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 45. R42 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.44 R43 Register (Address = 2Bh) [reset = X]

R43 is shown in Figure 44 and described in Table 46.

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Figure 44. R43 Register

7	6	5	4	3	2	1	0
RESERVED				REF3BUFGAIN	REF2BUFGAIN	REF1BUFGAIN	REF0BUFGAIN
R-X				R/W-X	R/W-X	R/W-X	R/W-X

Table 46. R43 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	X	
3	REF3BUFGAIN	R/W	X	REFx Amplitude Detector Enable for LVCMOS input mode. 1h = Slew rate detector enabled
2	REF2BUFGAIN	R/W	X	REFx Amplitude Detector Enable for LVCMOS input mode 1h = Slew rate detector enabled
1	REF1BUFGAIN	R/W	X	REFx Amplitude Detector Enable for LVCMOS input mode 1h = Slew rate detector enabled
0	REF0BUFGAIN	R/W	X	REFx Amplitude Detector Enable for LVCMOS input mode 1h = Slew rate detector enabled

2.45 R44 Register (Address = 2Ch) [reset = X]

R44 is shown in Figure 45 and described in Table 47.

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Figure 45. R44 Register

7	6	5	4	3	2	1	0
REF1_TYPE				REF0_TYPE			
R/W-X				R/W-X			

Table 47. R44 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	REF1_TYPE	R/W	X	REFx Input Type 0h = DC-DIFF (Internal termination and biasing off) 1h = AC-DIFF (Internal termination off, biasing on) 3h = AC-DIFF (Internal 100-Ω differential, biasing on) 4h = HCSL (Internal 50-Ω to GND, biasing off) 8h = LVCMOS (Internal termination and biasing off)
3-0	REF0_TYPE	R/W	X	REFx Input Type 0h = DC-DIFF (Internal termination and biasing off) 1h = AC-DIFF (Internal termination off, biasing on) 3h = AC-DIFF (Internal 100-Ω differential, biasing on) 4h = HCSL (Internal 50-Ω to GND, biasing off) 8h = LVCMOS (Internal termination and biasing off)

2.46 R45 Register (Address = 2Dh) [reset = X]

R45 is shown in Figure 46 and described in Table 48.

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Figure 46. R45 Register

7	6	5	4	3	2	1	0
REF3_TYPE				REF2_TYPE			
R/W-X				R/W-X			

Table 48. R45 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	REF3_TYPE	R/W	X	REFx Input Type 0h = DC-DIFF (Internal termination and biasing off) 1h = AC-DIFF (Internal termination off, biasing on) 3h = AC-DIFF (Internal 100-Ω differential, biasing on) 4h = HCSL (Internal 50-Ω to GND, biasing off) 8h = LVCMOS (Internal termination and biasing off)
3-0	REF2_TYPE	R/W	X	REFx Input Type 0h = DC-DIFF (Internal termination and biasing off) 1h = AC-DIFF (Internal termination off, biasing on) 3h = AC-DIFF (Internal 100-Ω differential, biasing on) 4h = HCSL (Internal 50-Ω to GND, biasing off) 8h = LVCMOS (Internal termination and biasing off)

2.47 R46 Register (Address = 2Eh) [reset = X]

R46 is shown in Figure 47 and described in Table 49.

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Figure 47. R46 Register

7	6	5	4	3	2	1	0
RESERVED	STAT0_SEL						
R-X	R/W-X						

Table 49. R46 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	X	

Table 49. R46 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-0	STAT0_SEL	R/W	X	STATUS0 Indicator Signal Select The output pin state of 1 indicates the status condition is true. 00h = XO Input Loss of Signal (LOS) 01h = TCXO Input Loss of Signal (LOS) 03h = PLL1 Lock Detected (LOLb) 04h = PLL1 VCO Calibration Active 05h = PLL1 N Divider, div-by-2 06h = PLL2 Lock Detected (LOLb) 07h = PLL2 VCO Calibration Active 08h = PLL2 N Divider, div-by-2 09h = EEPROM Active 0Ah = Interrupt (INTR) 0Bh = Reserved 0Ch = Reserved 0Dh = REF0 monitor divider output, div-by-2 0Eh = REF1 monitor divider output, div-by-2 0Fh = REF2 monitor divider output, div-by-2 10h = REF3 monitor divider output, div-by-2 11h = REF0 amplitude monitor fault 12h = REF1 amplitude monitor fault 13h = REF2 amplitude monitor fault 14h = REF3 amplitude monitor fault 15h = REF0 frequency monitor fault 16h = REF1 frequency monitor fault 17h = REF2 frequency monitor fault 18h = REF3 frequency monitor fault 19h = REF0 missing clock monitor fault 1Ah = REF1 missing clock monitor fault 1Bh = REF2 missing clock monitor fault 1Ch = REF3 missing clock monitor fault 1Dh = Reserved 1Eh = Reserved 1Fh = Reserved 20h = Reserved 21h = REF0 validation timer active 22h = REF1 validation timer active 23h = REF2 validation timer active 24h = REF3 validation timer active 25h = REF0 phase validation monitor fault 26h = REF1 phase validation monitor fault 27h = REF2 phase validation monitor fault 28h = REF3 phase validation monitor fault 40h = DPLL1 PathA R Divider, div-by-2 41h = DPLL1 REF N Divider, div-by-2 42h = DPLL TCXO M Divider, div-by-2 43h = DPLL1 TCXO N Divider, div-by-2 44h = Reserved 45h = Reserved 46h = DPLL1 REF0 selected 47h = DPLL1 REF1 selected 48h = DPLL1 REF2 selected 49h = DPLL1 REF3 selected 4Ah = DPLL1 Holdover active 4Bh = DPLL1 Reference switchover event 4Ch = Reserved 4Dh = DPLL1 Tuning history update

Table 49. R46 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				4Eh = Reserved 4Fh = Reserved 50h = DPLL1 Loss of Lock 51h = Reserved 52h = Reserved 53h = Reserved 54h = Reserved 60h = DPLL2 PathB R Divider, div-by-2 61h = DPLL2 REF N Divider, div-by-2 63h = DPLL2 TCXO N Divider, div-by-2 64h = Reserved 65h = Reserved 66h = DPLL2 REF0 selected 67h = DPLL2 REF1 selected 68h = DPLL2 REF2 selected 69h = DPLL2 REF3 selected 6Ah = DPLL2 Holdover active 6Bh = DPLL2 Reference switchover event 6Ch = Reserved 6Dh = DPLL2 Tuning history update 6Eh = DPLL2 Fast lock active 6Fh = DPLL2 Fast lock done 70h = DPLL2 Loss of Lock 71h = Reserved 72h = Reserved 73h = Reserved 74h = Reserved

2.48 R47 Register (Address = 2Fh) [reset = X]

R47 is shown in Figure 48 and described in Table 50.

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Figure 48. R47 Register

7	6	5	4	3	2	1	0
RESERVED	STAT1_SEL						
R-X	R/W-X						

Table 50. R47 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	X	
6-0	STAT1_SEL	R/W	X	STATUS1 Indicator Signal Select See STAT0_SEL for status signal and bit settings.

2.49 R48 Register (Address = 30h) [reset = X]

R48 is shown in Figure 49 and described in Table 51.

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Figure 49. R48 Register

7	6	5	4	3	2	1	0
RESERVED	GPIO5_STAT_SEL						
R-X	R/W-X						

Table 51. R48 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	X	
6-0	GPIO5_STAT_SEL	R/W	X	GPIO5 Status Signal Select See STAT0_SEL for status signal and bit settings.

2.50 R49 Register (Address = 31h) [reset = X]

R49 is shown in Figure 50 and described in Table 52.

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Figure 50. R49 Register

7	6	5	4	3	2	1	0
RESERVED	GPIO6_STAT_SEL						
R-X	R/W-X						

Table 52. R49 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	X	
6-0	GPIO6_STAT_SEL	R/W	X	GPIO6 Status Signal Select See STAT0_SEL for status signal and bit settings.

2.51 R50 Register (Address = 32h) [reset = X]

R50 is shown in Figure 51 and described in Table 53.

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Figure 51. R50 Register

7	6	5	4	3	2	1	0
RESERVED				GPIO6_FDEV_EN	GPIO5_FDEV_EN	GPIO4_FDEV_EN	GPIO3_FDEV_EN
R-X				R/W-X	R/W-X	R/W-X	R/W-X

Table 53. R50 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	X	
3	GPIO6_FDEV_EN	R/W	X	Enable DCO frequency decrement control on GPIO6 pin for PLL2 domain When enabled, a rising edge on this GPIO pin will update the DCO frequency accordingly.

Table 53. R50 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	GPIO5_FDEV_EN	R/W	X	Enable DCO frequency increment control on GPIO5 pin for PLL2 domain When enabled, a rising edge on this GPIO pin will update the DCO frequency accordingly.
1	GPIO4_FDEV_EN	R/W	X	Enable DCO frequency decrement control on GPIO4 pin for PLL1 domain When enabled, a rising edge on this GPIO pin will update the DCO frequency accordingly.
0	GPIO3_FDEV_EN	R/W	X	Enable DCO frequency increment control on GPIO3 pin for PLL1 domain When enabled, a rising edge on this GPIO pin will update the DCO frequency accordingly.

2.52 R51 Register (Address = 33h) [reset = X]

R51 is shown in Figure 52 and described in Table 54.

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Figure 52. R51 Register

7	6	5	4	3	2	1	0
RESERVED		CH7PWDN	CH6PWDN	CH45PWDN	CH23PWDN	CH1PWDN	CH0PWDN
R-X		R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X

Table 54. R51 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	
5	CH7PWDN	R/W	X	Output Channel Divider Power-down Set to 0 for normal operation
4	CH6PWDN	R/W	X	Output Channel Divider Power-down Set to 0 for normal operation
3	CH45PWDN	R/W	X	Output Channel Divider Power-down Set to 0 for normal operation
2	CH23PWDN	R/W	X	Output Channel Divider Power-down Set to 0 for normal operation
1	CH1PWDN	R/W	X	Output Channel Divider Power-down Set to 0 for normal operation
0	CH0PWDN	R/W	X	Output Channel Divider Power-down Set to 0 for normal operation

2.53 R52 Register (Address = 34h) [reset = X]

R52 is shown in Figure 53 and described in Table 55.

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Figure 53. R52 Register

7	6	5	4	3	2	1	0
RESERVED		OUT_0_TYPE					
R-X		R/W-X					

Table 55. R52 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	
5-0	OUT_0_TYPE	R/W	X	Output 0 Driver Type. 00h = Disabled 10h = AC-LVDS 14h = AC-CML 18h = AC-LVPECL 2Ch = HCSL (Internal Term. off) 2Dh = HCSL (Internal 50-Ω to GND) 30h = LVCMOS(HiZ/HiZ) 32h = LVCMOS(HiZ/-) 33h = LVCMOS(HiZ/+) 35h = LVCMOS(low/low) 38h = LVCMOS(-/HiZ) 3Ah = LVCMOS(-/-) 3Bh = LVCMOS(-/+) 3Ch = LVCMOS(+/HiZ) 3Eh = LVCMOS(+/-) 3Fh = LVCMOS(+/+)

2.54 R53 Register (Address = 35h) [reset = X]

R53 is shown in Figure 54 and described in Table 56.

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Figure 54. R53 Register

7	6	5	4	3	2	1	0
RESERVED					CH_0_MUX		
R-X					R/W-X		

Table 56. R53 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	X	
2-0	CH_0_MUX	R/W	X	Channel 0 Output Mux A channel reset or PWDN cycle is required to exit from XO Bypass, or Reference Bypass Mux mode. The XO/TCXO/DPLL Ref Bypass are tapped prior to any input frequency divide and/or doubler blocks. 0h = PLL1 P1 1h = PLL1 P2 2h = PLL2 P1 3h = PLL2 P2 4h = TCXO/Ref Bypass Mux 5h = XO Bypass

2.55 R54 Register (Address = 36h) [reset = X]

R54 is shown in Figure 55 and described in Table 57.

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Figure 55. R54 Register

7	6	5	4	3	2	1	0
RESERVED	OUT_0_DIV_MSB[10:4]						
R-X	R/W-X						

Table 57. R54 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	X	
6-0	OUT_0_DIV_MSB[10:4]	R/W	X	Bits 10:4 of OUT_0_DIV_MSB

2.56 R55 Register (Address = 37h) [reset = X]

R55 is shown in Figure 56 and described in Table 58.

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Figure 56. R55 Register

7	6	5	4	3	2	1	0
OUT_0_DIV_MSB				OUT_0_DIV[19:16]			
R/W-X				R/W-X			

Table 58. R55 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	OUT_0_DIV_MSB	R/W	X	Channel 0 Output MSB Divider. The output of this 11-bit MSB divider is fed to the LSB divider. Output MSB divide value = Register value + 1. The effective output divide value is the product of the effective MSB and LSB divide values (OUT div = MSB Div × LSB Div). 1 PPS or 1 Hz output is supported by these cascaded dividers. Note: A channel reset or PWDN cycle is required to exit from Disabled, min divide, and max divide settings. 000h = Div by 1 (MSB bypassed) 001h = Div by 2 7FEh = Div by 2^{11} - 1 7FFh = Div by 2^{11}
3-0	OUT_0_DIV[19:16]	R/W	X	Bits 19:16 of OUT_0_DIV

2.57 R56 Register (Address = 38h) [reset = X]

R56 is shown in Figure 57 and described in Table 59.

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Figure 57. R56 Register

7	6	5	4	3	2	1	0
OUT_0_DIV[15:8]							
R/W-X							

Table 59. R56 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	OUT_0_DIV[15:8]	R/W	X	Bits 15:8 of OUT_0_DIV

2.58 R57 Register (Address = 39h) [reset = X]

R57 is shown in Figure 58 and described in Table 60.

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Figure 58. R57 Register

7	6	5	4	3	2	1	0
OUT_0_DIV							
R/W-X							

Table 60. R57 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	OUT_0_DIV	R/W	X	Channel 0 Output LSB Divider. The output of this 20-bit LSB divider is fed to the output driver. Output LSB divide value equals the Register value. The effective output divide value is the product of the effective MSB and LSB divide values (OUT div = MSB Div × LSB Div). 1 PPS or 1 Hz output is supported by these cascaded dividers. Note: A channel reset or PWDN cycle is required to exit from Disabled, min divide, and max divide settings. 00000000h = Disabled 00000001h = Div by 1 (LSB bypassed) 00000002h = Div by 2 000FFFFEh = Div by 2^{20} - 2 000FFFFFh = Div by 2^{20} - 1

2.59 R58 Register (Address = 3Ah) [reset = X]

R58 is shown in Figure 59 and described in Table 61.

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Figure 59. R58 Register

7	6	5	4	3	2	1	0
RESERVED		OUT_1_TYPE					
R-X		R/W-X					

Table 61. R58 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	
5-0	OUT_1_TYPE	R/W	X	Output 1 Driver Type See OUT_0_TYPE for bit settings.

2.60 R59 Register (Address = 3Bh) [reset = X]

R59 is shown in Figure 60 and described in Table 62.

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Figure 60. R59 Register

7	6	5	4	3	2	1	0
RESERVED	CH_1_MUX			OUT_1_DIV[19:16]			
R-X	R/W-X			R/W-X			

Table 62. R59 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	X	
6-4	CH_1_MUX	R/W	X	Channel 1 Output Mux A channel reset or PWDN cycle is required to exit from XO Bypass, or Reference Bypass Mux mode. The XO/TCXO/DPLL Ref Bypass are tapped prior to any input frequency divide and/or doubler blocks. 0h = PLL1 P1 1h = PLL1 P2 2h = PLL2 P1 3h = PLL2 P2 4h = TCXO/Ref Bypass Mux 5h = XO Bypass
3-0	OUT_1_DIV[19:16]	R/W	X	Bits 19:16 of OUT_1_DIV

2.61 R60 Register (Address = 3Ch) [reset = X]

R60 is shown in Figure 61 and described in Table 63.

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Figure 61. R60 Register

7	6	5	4	3	2	1	0
OUT_1_DIV[15:8]							
R/W-X							

Table 63. R60 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	OUT_1_DIV[15:8]	R/W	X	Bits 15:8 of OUT_1_DIV

2.62 R61 Register (Address = 3Dh) [reset = X]

R61 is shown in Figure 62 and described in Table 64.

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Figure 62. R61 Register

7	6	5	4	3	2	1	0
OUT_1_DIV							
R/W-X							

Table 64. R61 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	OUT_1_DIV	R/W	X	Channel 1 Output Divider The output of this 20-bit divider is fed to the output driver. Output divide value equals the Register value. Note: A channel reset or PWDN cycle is required to exit from Disabled, min divide, and max divide settings. 00000000h = Disabled 00000001h = Div by 1 (LSB bypassed) 00000002h = Div by 2 000FFFFEh = Div by 2^{20} - 2 000FFFFFh = Div by 2^{20} - 1

2.63 R62 Register (Address = 3Eh) [reset = X]

R62 is shown in Figure 63 and described in Table 65.

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Figure 63. R62 Register

7	6	5	4	3	2	1	0
RESERVED				OUT_2_TYPE			
R-X				R/W-X			

Table 65. R62 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	
5-0	OUT_2_TYPE	R/W	X	Output 2 Driver Type See OUT_0_TYPE for bit settings.

2.64 R63 Register (Address = 3Fh) [reset = X]

R63 is shown in Figure 64 and described in Table 66.

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Figure 64. R63 Register

7	6	5	4	3	2	1	0
RESERVED				OUT_3_TYPE			
R-X				R/W-X			

Table 66. R63 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	
5-0	OUT_3_TYPE	R/W	X	Output 3 Driver Type See OUT_0_TYPE for bit settings.

2.65 R64 Register (Address = 40h) [reset = X]

R64 is shown in Figure 65 and described in Table 67.

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Figure 65. R64 Register

7	6	5	4	3	2	1	0
RESERVED	CH_2_3_MUX			OUT_2_3_DIV[19:16]			
R-X	R/W-X			R/W-X			

Table 67. R64 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	X	
6-4	CH_2_3_MUX	R/W	X	Channel 2 and 3 Output Mux 0h = PLL1 P1 1h = PLL1 P2 2h = PLL2 P1 3h = PLL2 P2

Table 67. R64 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	OUT_2_3_DIV[19:16]	R/W	X	Bits 19:16 of OUT_2_3_DIV

2.66 R65 Register (Address = 41h) [reset = X]

R65 is shown in Figure 66 and described in Table 68.

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Figure 66. R65 Register

7	6	5	4	3	2	1	0
OUT_2_3_DIV[15:8]							
R/W-X							

Table 68. R65 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	OUT_2_3_DIV[15:8]	R/W	X	Bits 15:8 of OUT_2_3_DIV

2.67 R66 Register (Address = 42h) [reset = X]

R66 is shown in Figure 67 and described in Table 69.

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Figure 67. R66 Register

7	6	5	4	3	2	1	0
OUT_2_3_DIV							
R/W-X							

Table 69. R66 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	OUT_2_3_DIV	R/W	X	Channel 2 and 3 Output Divider Same description and bit settings as OUT_1_DIV.

2.68 R67 Register (Address = 43h) [reset = X]

R67 is shown in Figure 68 and described in Table 70.

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Figure 68. R67 Register

7	6	5	4	3	2	1	0
RESERVED		OUT_4_TYPE					
R-X		R/W-X					

Table 70. R67 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	
5-0	OUT_4_TYPE	R/W	X	Output 4 Driver Type See OUT_0_TYPE for bit settings.

2.69 R68 Register (Address = 44h) [reset = X]

R68 is shown in Figure 69 and described in Table 71.

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Figure 69. R68 Register

7	6	5	4	3	2	1	0
RESERVED		OUT_5_TYPE					
R-X		R/W-X					

Table 71. R68 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	
5-0	OUT_5_TYPE	R/W	X	Output 5 Driver Type See OUT_0_TYPE for bit settings.

2.70 R69 Register (Address = 45h) [reset = X]

R69 is shown in Figure 70 and described in Table 72.

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Figure 70. R69 Register

7	6	5	4	3	2	1	0
RESERVED	CH_4_5_MUX			OUT_4_5_DIV[19:16]			
R-X	R/W-X			R/W-X			

Table 72. R69 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	X	
6-4	CH_4_5_MUX	R/W	X	Channel 4 and 5 Output Mux 0h = PLL1 P1 1h = PLL1 P2 2h = PLL2 P1 3h = PLL2 P2
3-0	OUT_4_5_DIV[19:16]	R/W	X	Bits 19:16 of OUT_4_5_DIV

2.71 R70 Register (Address = 46h) [reset = X]

R70 is shown in Figure 71 and described in Table 73.

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Figure 71. R70 Register

7	6	5	4	3	2	1	0
OUT_4_5_DIV[15:8]							
R/W-X							

Table 73. R70 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	OUT_4_5_DIV[15:8]	R/W	X	Bits 15:8 of OUT_4_5_DIV

2.72 R71 Register (Address = 47h) [reset = X]

R71 is shown in Figure 72 and described in Table 74.

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Figure 72. R71 Register

7	6	5	4	3	2	1	0
OUT_4_5_DIV							
R/W-X							

Table 74. R71 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	OUT_4_5_DIV	R/W	X	Channel 4 and 5 Output Divider Same description and bit settings as OUT_1_DIV.

2.73 R72 Register (Address = 48h) [reset = X]

R72 is shown in Figure 73 and described in Table 75.

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Figure 73. R72 Register

7	6	5	4	3	2	1	0
RESERVED		OUT_6_TYPE					
R-X		R/W-X					

Table 75. R72 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	
5-0	OUT_6_TYPE	R/W	X	Output 6 Driver Type See OUT_0_TYPE for bit settings.

2.74 R73 Register (Address = 49h) [reset = X]

R73 is shown in Figure 74 and described in Table 76.

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Figure 74. R73 Register

7	6	5	4	3	2	1	0
RESERVED	CH_6_MUX			OUT_6_DIV[19:16]			
R-X	R/W-X			R/W-X			

Table 76. R73 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	X	
6-4	CH_6_MUX	R/W	X	Channel 6 Output Mux 0h = PLL1 P1 1h = PLL1 P2 2h = PLL2 P1 3h = PLL2 P2
3-0	OUT_6_DIV[19:16]	R/W	X	Bits 19:16 of OUT_6_DIV

2.75 R74 Register (Address = 4Ah) [reset = X]

R74 is shown in Figure 75 and described in Table 77.

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Figure 75. R74 Register

7	6	5	4	3	2	1	0
OUT_6_DIV[15:8]							
R/W-X							

Table 77. R74 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	OUT_6_DIV[15:8]	R/W	X	Bits 15:8 of OUT_6_DIV

2.76 R75 Register (Address = 4Bh) [reset = X]

R75 is shown in Figure 76 and described in Table 78.

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Figure 76. R75 Register

7	6	5	4	3	2	1	0
OUT_6_DIV							
R/W-X							

Table 78. R75 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	OUT_6_DIV	R/W	X	Channel 6 Output Divider Same description and bit settings as OUT_1_DIV.

2.77 R76 Register (Address = 4Ch) [reset = X]

R76 is shown in Figure 77 and described in Table 79.

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Figure 77. R76 Register

7	6	5	4	3	2	1	0
RESERVED		OUT_7_TYPE					
R-X		R/W-X					

Table 79. R76 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	
5-0	OUT_7_TYPE	R/W	X	Output 7 Driver Type See OUT_0_TYPE for bit settings.

2.78 R77 Register (Address = 4Dh) [reset = X]

R77 is shown in Figure 78 and described in Table 80.

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Figure 78. R77 Register

7	6	5	4	3	2	1	0
RESERVED					CH_7_MUX		
R-X					R/W-X		

Table 80. R77 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	X	
2-0	CH_7_MUX	R/W	X	Channel 7 Output Mux 00h = PLL1 P1 01h = PLL1 P2 02h = PLL2 P1 03h = PLL2 P2

2.79 R78 Register (Address = 4Eh) [reset = X]

R78 is shown in Figure 79 and described in Table 81.

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Figure 79. R78 Register

7	6	5	4	3	2	1	0
RESERVED	OUT_7_DIV_MSB[10:4]						
R-X	R/W-X						

Table 81. R78 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	X	
6-0	OUT_7_DIV_MSB[10:4]	R/W	X	Bits 10:4 of OUT_7_DIV_MSB

2.80 R79 Register (Address = 4Fh) [reset = X]

R79 is shown in Figure 80 and described in Table 82.

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Figure 80. R79 Register

7	6	5	4	3	2	1	0
OUT_7_DIV_MSB				OUT_7_DIV[19:16]			
R/W-X				R/W-X			

Table 82. R79 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	OUT_7_DIV_MSB	R/W	X	Channel 7 Output MSB Divider The output of this 11-bit MSB divider is fed to the LSB divider. Output MSB divide value = Register value + 1. The effective output divide value is the product of the effective MSB and LSB divide values (OUT div = MSB Div × LSB Div). 1 PPS or 1 Hz output is supported by these cascaded dividers. Note: A channel reset or PWDN cycle is required to exit from Disabled, min divide, and max divide settings. 000h = Div by 1 (MSB bypassed) 001h = Div by 2 7FEh = Div by 2^{11} - 1 7FFh = Div by 2^{11}
3-0	OUT_7_DIV[19:16]	R/W	X	Bits 19:16 of OUT_7_DIV

2.81 R80 Register (Address = 50h) [reset = X]

R80 is shown in Figure 81 and described in Table 83.

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Figure 81. R80 Register

7	6	5	4	3	2	1	0
OUT_7_DIV[15:8]							
R/W-X							

Table 83. R80 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	OUT_7_DIV[15:8]	R/W	X	Bits 15:8 of OUT_7_DIV

2.82 R81 Register (Address = 51h) [reset = X]

R81 is shown in Figure 82 and described in Table 84.

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Figure 82. R81 Register

7	6	5	4	3	2	1	0
OUT_7_DIV							
R/W-X							

Table 84. R81 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	OUT_7_DIV	R/W	X	Channel 7 Output LSB Divider The output of this 20-bit LSB divider is fed to the output driver. Output LSB divide value equals the Register value. The effective output divide value is the product of the effective MSB and LSB divide values (OUT div = MSB Div × LSB Div). 1 PPS or 1 Hz output is supported by these cascaded dividers. Note: A channel reset or PWDN cycle is required to exit from Disabled, min divide, and max divide settings. 00000000h = Disabled 00000001h = Div by 1 (LSB bypassed) 00000002h = Div by 2 000FFFFEh = Div by 2^{20} - 2 000FFFFFh = Div by 2^{20} - 1

2.83 R82 Register (Address = 52h) [reset = X]

R82 is shown in Figure 83 and described in Table 85.

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Figure 83. R82 Register

7	6	5	4	3	2	1	0
PLL2_SEC_CH47_SYNC_BNK	PLL2_SEC_CH03_SYNC_BNK	PLL2_PRI_CH47_SYNC_BNK	PLL2_PRI_CH03_SYNC_BNK	PLL1_SEC_CH47_SYNC_BNK	PLL1_SEC_CH03_SYNC_BNK	PLL1_PRI_CH47_SYNC_BNK	PLL1_PRI_CH03_SYNC_BNK
R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X

Table 85. R82 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PLL2_SEC_CH47_SYNC_BNK	R/W	X	PLL1 Secondary CH47 Sync Bank Enable
6	PLL2_SEC_CH03_SYNC_BNK	R/W	X	PLL1 Secondary CH03 Sync Bank Enable
5	PLL2_PRI_CH47_SYNC_BNK	R/W	X	PLL1 Primary CH47 Sync Bank Enable
4	PLL2_PRI_CH03_SYNC_BNK	R/W	X	PLL1 Primary CH03 Sync Bank Enable
3	PLL1_SEC_CH47_SYNC_BNK	R/W	X	PLL1 Secondary CH47 Sync Bank Enable
2	PLL1_SEC_CH03_SYNC_BNK	R/W	X	PLL1 Secondary CH03 Sync Bank Enable
1	PLL1_PRI_CH47_SYNC_BNK	R/W	X	PLL1 Primary CH47 Sync Bank Enable
0	PLL1_PRI_CH03_SYNC_BNK	R/W	X	PLL1 Primary CH03 Sync Bank Enable

2.84 R83 Register (Address = 53h) [reset = X]

R83 is shown in Figure 84 and described in Table 86.

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Figure 84. R83 Register

7	6	5	4	3	2	1	0
RESERVED		CH7_SYNCEN	CH6_SYNCEN	CH45_SYNCEN	CH23_SYNCEN	CH1_SYNCEN	CH0_SYNCEN
R-X		R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X

Table 86. R83 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	
5	CH7_SYNCEN	R/W	X	Channel 7 Output Sync Enable
4	CH6_SYNCEN	R/W	X	Channel 6 Output Sync Enable
3	CH45_SYNCEN	R/W	X	Channel 45 Output Sync Enable
2	CH23_SYNCEN	R/W	X	Channel 23 Output Sync Enable
1	CH1_SYNCEN	R/W	X	Channel 1 Output Sync Enable
0	CH0_SYNCEN	R/W	X	Channel 0 Output Sync Enable

2.85 R84 Register (Address = 54h) [reset = X]

R84 is shown in Figure 85 and described in Table 87.

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Figure 85. R84 Register

7	6	5	4	3	2	1	0
RESERVED		O_CH4_7_ZERODLY_EN			O_CH0_3_ZERODLY_EN		
R-X		R/W-X			R/W-X		

Table 87. R84 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	
5-3	O_CH4_7_ZERODLY_EN	R/W	X	Channel 7 to 4 Zero delay mode enable selection 0h = DPLL1 ZDM off 1h = DPLL1 ZDM to OUT7 2h = DPLL1 ZDM to OUT6 4h = DPLL1 ZDM to OUT4/5
2-0	O_CH0_3_ZERODLY_EN	R/W	X	Channel 3 to 0 Zero delay mode enable selection 0h = DPLL1 ZDM off 1h = DPLL1 ZDM to OUT0 2h = DPLL1 ZDM to OUT1 4h = DPLL1 ZDM to OUT2/3

2.86 R85 Register (Address = 55h) [reset = X]

R85 is shown in Figure 86 and described in Table 88.

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Figure 86. R85 Register

7	6	5	4	3	2	1	0
RESERVED		CH1_VLD_TMR			CH0_VLD_TMR		
R-X		R/W-X			R/W-X		

Table 88. R85 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	
5-3	CH1_VLD_TMR	R/W	X	Channel 1 Valid Timer control See CH0_VLD_TMR bit settings.
2-0	CH0_VLD_TMR	R/W	X	Channel 0 Valid Timer control Output start-up delay from when VDDO_x reaches its valid threshold to when the output clock is released. 0h = 0 ms 1h = 0.5 ms 2h = 1 ms 3h = 2 ms 4h = 4 ms 5h = 8 ms 6h = 16 ms 7h = 64 ms

2.87 R86 Register (Address = 56h) [reset = X]

R86 is shown in Figure 87 and described in Table 89.

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Figure 87. R86 Register

7	6	5	4	3	2	1	0
RESERVED		CH45_VLD_TMR			CH23_VLD_TMR		
R-X		R/W-X			R/W-X		

Table 89. R86 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	
5-3	CH45_VLD_TMR	R/W	X	Channel 45 Valid Timer control Same description and bit settings as CH0_VLD_TMR.
2-0	CH23_VLD_TMR	R/W	X	Channel 23 Valid Timer control Same description and bit settings as CH0_VLD_TMR.

2.88 R87 Register (Address = 57h) [reset = X]

R87 is shown in Figure 88 and described in Table 90.

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Figure 88. R87 Register

7	6	5	4	3	2	1	0
RESERVED		CH7_VLD_TMR			CH6_VLD_TMR		
R-X		R/W-X			R/W-X		

Table 90. R87 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	
5-3	CH7_VLD_TMR	R/W	X	Channel 7 Valid Timer control Same description and bit settings as CH0_VLD_TMR.
2-0	CH6_VLD_TMR	R/W	X	Channel 6 Valid Timer control Same description and bit settings as CH0_VLD_TMR.

2.89 R88 Register (Address = 58h) [reset = 0h]

R88 is shown in Figure 89 and described in Table 91.

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Figure 89. R88 Register

7	6	5	4	3	2	1	0
RESERVED		CH7_ACT	CH6_ACT	CH45_ACT	CH23_ACT	CH1_ACT	CH0_ACT
R-0h		R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 91. R88 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	
5	CH7_ACT	R	0h	Channel 7 Output Active flag Reads 1 when output channel is powered-up and active.
4	CH6_ACT	R	0h	Channel 6 Output Active flag Reads 1 when output channel is powered-up and active.
3	CH45_ACT	R	0h	Channel 45 Output Active flag Reads 1 when output channel is powered-up and active.
2	CH23_ACT	R	0h	Channel 23 Output Active flag Reads 1 when output channel is powered-up and active.
1	CH1_ACT	R	0h	Channel 1 Output Active flag Reads 1 when output channel is powered-up and active.
0	CH0_ACT	R	0h	Channel 0 Output Active flag Reads 1 when output channel is powered-up and active.

2.90 R89 Register (Address = 59h) [reset = X]

R89 is shown in Figure 90 and described in Table 92.

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Figure 90. R89 Register

7	6	5	4	3	2	1	0
RESERVED						REF_BYPASS_MUX	
R-X						R/W-X	

Table 92. R89 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	X	
1-0	REF_BYPASS_MUX	R/W	X	TCXO/Ref Input Bypass Mux When CH_0_MUX or CH_1_MUX is 4h, this bit field selects the TCXO or DPLL Ref Input signal bypassed to the corresponding output channel. 0Xb = TCXO Input 10b = Selected DPLL2 Ref Input 11b = Selected DPLL1 Ref Input

2.91 R90 Register (Address = 5Ah) [reset = X]

R90 is shown in Figure 91 and described in Table 93.

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Figure 91. R90 Register

7	6	5	4	3	2	1	0
RESERVED						PLL1_XO_DBLR	PLL1_PDN
R-X						R/W-X	R/W-X

Table 93. R90 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	X	
1	PLL1_XO_DBLR	R/W	X	PLL1 XO Doubler Enable
0	PLL1_PDN	R/W	X	PLL1 Power down The PLL1_PDN bit determines whether PLL1 is automatically enabled and calibrated after a hardware reset. 0h = PLL1 Enabled 1h = PLL1 Disabled

2.92 R91 Register (Address = 5Bh) [reset = X]

R91 is shown in Figure 92 and described in Table 94.

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Figure 92. R91 Register

7	6	5	4	3	2	1	0
RESERVED					RESERVED	PLL1_CP	
R-X					R/W-X	R/W-X	

Table 94. R91 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	X	
2	RESERVED	R/W	X	Reserved
1-0	PLL1_CP	R/W	X	PLL1 Charge Pump Gain 0h = 1.6 mA 1h = 3.2 mA 2h = 4.8 mA 3h = 6.4 mA

2.93 R92 Register (Address = 5Ch) [reset = X]

R92 is shown in Figure 93 and described in Table 95.

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Figure 93. R92 Register

7	6	5	4	3	2	1	0
PLL1_P2				PLL1_P1			
R/W-X				R/W-X			

Table 95. R92 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	PLL1_P2	R/W	X	PLL1 Post-Divider2 Note: A RESET is required after changing Divider values. See PLL1_P1 for bit settings.
3-0	PLL1_P1	R/W	X	PLL1 Post-Divider1 Note: A RESET is required after changing Divider values. 3h = 4 4h = 5 5h = 6 6h = 7 7h = 8 8h = 9 Ah = 11 Ch = 13

2.94 R93 Register (Address = 5Dh) [reset = X]

R93 is shown in Figure 94 and described in Table 96.

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Figure 94. R93 Register

7	6	5	4	3	2	1	0
RESERVED				RESERVED			
R-X				R/W-X			

Table 96. R93 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	X	
3-0	RESERVED	R/W	X	Reserved

2.95 R94 Register (Address = 5Eh) [reset = X]

R94 is shown in Figure 95 and described in Table 97.

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Figure 95. R94 Register

7	6	5	4	3	2	1	0
RESERVED				PLL1_RBLEED_CP			
R-X				R/W-X			

Table 97. R94 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	
5-0	PLL1_RBLEED_CP	R/W	X	PLL1 Bleed resistor selection 00h = Off 01h = 23.7 kΩ 02h = 11.9 kΩ 03h = 7.92 kΩ 04h = 5.94 kΩ 05h = 4.75 kΩ 06h = 3.96 kΩ 07h = 2.97 kΩ 08h = 2.97 kΩ 09h = 2.64 kΩ 0Ah = 2.38 kΩ 0Bh = 2.16 kΩ 0Ch = 1.98 kΩ 0Dh = 1.83 kΩ 0Eh = 1.70 kΩ 0Fh = 1.58 kΩ 10h = 1.49 kΩ 11h = 1.40 kΩ 12h = 1.32 kΩ 13h = 1.25 kΩ 14h = 1.19 kΩ 15h = 1.13 kΩ 16h = 1.08 kΩ 17h = 1.03 kΩ 18h = 0.99 kΩ 19h = 0.95 kΩ 1Ah = 0.92 kΩ 1Bh = 0.88 kΩ 1Ch = 0.85 kΩ 1Dh = 0.82 kΩ 1Eh = 0.79 kΩ 1Fh = 0.77 kΩ

2.96 R95 Register (Address = 5Fh) [reset = X]

R95 is shown in Figure 96 and described in Table 98.

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Figure 96. R95 Register

7	6	5	4	3	2	1	0
RESERVED				PLL1_CLSDWAIT		PLL1_VCOWAIT	
R-X				R/W-X		R/W-X	

Table 98. R95 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	X	
3-2	PLL1_CLSDWAIT	R/W	X	Closed Loop Wait Period VCO calibration time per step (up to 7 steps). 0h = 0.3 ms 1h = 3 ms 2h = 30 ms 3h = 300 ms
1-0	PLL1_VCOWAIT	R/W	X	VCO Wait Period Timeout counter before starting VCO calibration. 0h = 0.02 ms 1h = 0.4 ms 2h = 8 ms 3h = 200 ms

2.97 R96 Register (Address = 60h) [reset = X]

R96 is shown in Figure 97 and described in Table 99.

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Figure 97. R96 Register

7	6	5	4	3	2	1	0
RESERVED						PLL2_XO_DBLR	PLL2_PDN
R-X						R/W-X	R/W-X

Table 99. R96 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	X	
1	PLL2_XO_DBLR	R/W	X	PLL2 XO Doubler Enable
0	PLL2_PDN	R/W	X	PLL2 Power down The PLL2_PDN bit determines whether PLL2 is automatically enabled and calibrated after a hardware reset. If the PLL2_PDN bit is set to 1 during normal operation then PLL2 is disabled and the calibration circuit is reset. When PLL2_PDN is then cleared to 0, PLL2 is re-enabled and the calibration sequence is automatically restarted. 0h = PLL2 Enabled 1h = PLL2 Disabled

2.98 R97 Register (Address = 61h) [reset = X]

R97 is shown in Figure 98 and described in Table 100.

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Figure 98. R97 Register

7	6	5	4	3	2	1	0
RESERVED					RESERVED	PLL2_CP	
R-X					R/W-X	R/W-X	

Table 100. R97 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	X	
2	RESERVED	R/W	X	Reserved
1-0	PLL2_CP	R/W	X	PLL2 Charge Pump Gain 0h = 1.6 mA 1h = 3.2 mA 2h = 4.8 mA 3h = 6.4 mA

2.99 R98 Register (Address = 62h) [reset = X]

R98 is shown in Figure 99 and described in Table 101.

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Figure 99. R98 Register

7	6	5	4	3	2	1	0
PLL2_P2				PLL2_P1			
R/W-X				R/W-X			

Table 101. R98 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	PLL2_P2	R/W	X	PLL2 Post-Divider2 Note: A RESET is required after changing Divider values. See PLL2_P1 for bit settings.
3-0	PLL2_P1	R/W	X	PLL2 Post-Divider1 Note: A RESET is required after changing Divider values. 3h = 4 4h = 5 5h = 6 6h = 7 7h = 8 8h = 9 Ah = 11 Ch = 13

2.100 R99 Register (Address = 63h) [reset = X]

R99 is shown in Figure 100 and described in Table 102.

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Figure 100. R99 Register

7	6	5	4	3	2	1	0
RESERVED				RESERVED			
R-X				R/W-X			

Table 102. R99 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	X	
3-0	RESERVED	R/W	X	Reserved

2.101 R100 Register (Address = 64h) [reset = X]

R100 is shown in Figure 101 and described in Table 103.

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Figure 101. R100 Register

7	6	5	4	3	2	1	0
RESERVED				PLL2_RBLEED_CP			
R-X				R/W-X			

Table 103. R100 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	
5-0	PLL2_RBLEED_CP	R/W	X	PLL2 Bleed resistor selection. See PLL1_RBLEED_CP for bit settings.

2.102 R101 Register (Address = 65h) [reset = X]

R101 is shown in Figure 102 and described in Table 104.

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Figure 102. R101 Register

7	6	5	4	3	2	1	0
RESERVED				PLL2_CLSDWAIT		PLL2_VCOWAIT	
R-X				R/W-X		R/W-X	

Table 104. R101 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	X	
3-2	PLL2_CLSDWAIT	R/W	X	Closed Loop Wait Period VCO calibration time per step (up to 7 steps). 0h = 0.3 ms 1h = 3 ms 2h = 30 ms 3h = 300 ms
1-0	PLL2_VCOWAIT	R/W	X	VCO Wait Period Timeout counter before starting VCO calibration. 0h = 0.02 ms 1h = 0.4 ms 2h = 8 ms 3h = 200 ms

2.103 R102 Register (Address = 66h) [reset = X]

R102 is shown in Figure 103 and described in Table 105.

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Figure 103. R102 Register

7	6	5	4	3	2	1	0
RESERVED							PLL1_NDIV[8:8]
R-X							R/W-X

Table 105. R102 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	X	
0	PLL1_NDIV[8:8]	R/W	X	Bit 8 of PLL1_NDIV

2.104 R103 Register (Address = 67h) [reset = X]

R103 is shown in Figure 104 and described in Table 106.

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Figure 104. R103 Register

7	6	5	4	3	2	1	0
PLL1_NDIV							
R/W-X							

Table 106. R103 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PLL1_NDIV	R/W	X	PLL1 N Divider

2.105 R104 Register (Address = 68h) [reset = X]

R104 is shown in Figure 105 and described in Table 107.

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Figure 105. R104 Register

7	6	5	4	3	2	1	0
PLL1_NUM[39:32]							
R/W-X							

Table 107. R104 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PLL1_NUM[39:32]	R/W	X	Bits 39:32 of PLL1_NUM

2.106 R105 Register (Address = 69h) [reset = X]

R105 is shown in Figure 106 and described in Table 108.

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Figure 106. R105 Register

7	6	5	4	3	2	1	0
PLL1_NUM[31:24]							
R/W-X							

Table 108. R105 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PLL1_NUM[31:24]	R/W	X	Bits 31:24 of PLL1_NUM

2.107 R106 Register (Address = 6Ah) [reset = X]

R106 is shown in Figure 107 and described in Table 109.

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Figure 107. R106 Register

7	6	5	4	3	2	1	0
PLL1_NUM[23:16]							
R/W-X							

Table 109. R106 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PLL1_NUM[23:16]	R/W	X	Bits 23:16 of PLL1_NUM

2.108 R107 Register (Address = 6Bh) [reset = X]

R107 is shown in Figure 108 and described in Table 110.

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Figure 108. R107 Register

7	6	5	4	3	2	1	0
PLL1_NUM[15:8]							
R/W-X							

Table 110. R107 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PLL1_NUM[15:8]	R/W	X	Bits 15:8 of PLL1_NUM

2.109 R108 Register (Address = 6Ch) [reset = X]

R108 is shown in Figure 109 and described in Table 111.

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Figure 109. R108 Register

7	6	5	4	3	2	1	0
PLL1_NUM							
R/W-X							

Table 111. R108 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PLL1_NUM	R/W	X	PLL1 Fractional Divider Numerator

2.110 R109 Register (Address = 6Dh) [reset = X]

R109 is shown in Figure 110 and described in Table 112.

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Figure 110. R109 Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED		PLL1_DTHRMODE		PLL1_ORDER		
R-X	R/W-X		R/W-X		R/W-X		

Table 112. R109 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	X	
6-5	RESERVED	R/W	X	Reserved
4-3	PLL1_DTHRMODE	R/W	X	APLL1 SDM Dither Mode 0h = Weak 1h = Medium 2h = Strong 3h = Disabled
2-0	PLL1_ORDER	R/W	X	APLL1 SDM Order 0h = Integer Mode 1h = 1st 2h = 2nd 3h = 3rd 4h = 4th

2.111 R110 Register (Address = 6Eh) [reset = X]

R110 is shown in Figure 111 and described in Table 113.

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Figure 111. R110 Register

7	6	5	4	3	2	1	0
RESERVED							RESERVED
R-X							R/W-X

Table 113. R110 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	X	
0	RESERVED	R/W	X	Reserved

2.112 R111 Register (Address = 6Fh) [reset = X]

R111 is shown in Figure 112 and described in Table 114.

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Figure 112. R111 Register

7	6	5	4	3	2	1	0
RESERVED					RESERVED	RESERVED	PLL1_MODE
R-X					R/W-X	R/W-X	R/W-X

Table 114. R111 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	X	
2	RESERVED	R/W	X	Reserved
1	RESERVED	R/W	X	Reserved
0	PLL1_MODE	R/W	X	PLL1 operational mode 0h = Free-run mode (APLL only) 1h = DPLL mode

2.113 R112 Register (Address = 70h) [reset = X]

R112 is shown in Figure 113 and described in Table 115.

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Figure 113. R112 Register

7	6	5	4	3	2	1	0
RESERVED		RESERVED					
R-X		R/W-X					

Table 115. R112 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	
5-0	RESERVED	R/W	X	Reserved

2.114 R113 Register (Address = 71h) [reset = X]

R113 is shown in Figure 114 and described in Table 116.

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Figure 114. R113 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 116. R113 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.115 R114 Register (Address = 72h) [reset = X]

R114 is shown in Figure 115 and described in Table 117.

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Figure 115. R114 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 117. R114 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.116 R115 Register (Address = 73h) [reset = X]

R115 is shown in Figure 116 and described in Table 118.

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Figure 116. R115 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 118. R115 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.117 R116 Register (Address = 74h) [reset = X]

R116 is shown in Figure 117 and described in Table 119.

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Figure 117. R116 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 119. R116 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.118 R117 Register (Address = 75h) [reset = 0h]

R117 is shown in Figure 118 and described in Table 120.

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Figure 118. R117 Register

7	6	5	4	3	2	1	0
RESERVED							RESERVED
R-0h							R/W-0h

Table 120. R117 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0h	
0	RESERVED	R/W	0h	Reserved

2.119 R118 Register (Address = 76h) [reset = 0h]

R118 is shown in Figure 119 and described in Table 121.

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Figure 119. R118 Register

7	6	5	4	3	2	1	0
PLL1_NUM_STAT[39:32]							
R-0h							

Table 121. R118 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PLL1_NUM_STAT[39:32]	R	0h	Bits 39:32 of PLL1_NUM_STAT

2.120 R119 Register (Address = 77h) [reset = 0h]

R119 is shown in Figure 120 and described in Table 122.

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Figure 120. R119 Register

7	6	5	4	3	2	1	0
PLL1_NUM_STAT[31:24]							
R-0h							

Table 122. R119 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PLL1_NUM_STAT[31:24]	R	0h	Bits 31:24 of PLL1_NUM_STAT

2.121 R120 Register (Address = 78h) [reset = 0h]

R120 is shown in Figure 121 and described in Table 123.

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Figure 121. R120 Register

7	6	5	4	3	2	1	0
PLL1_NUM_STAT[23:16]							
R-0h							

Table 123. R120 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PLL1_NUM_STAT[23:16]	R	0h	Bits 23:16 of PLL1_NUM_STAT

2.122 R121 Register (Address = 79h) [reset = 0h]

R121 is shown in Figure 122 and described in Table 124.

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Figure 122. R121 Register

7	6	5	4	3	2	1	0
PLL1_NUM_STAT[15:8]							
R-0h							

Table 124. R121 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PLL1_NUM_STAT[15:8]	R	0h	Bits 15:8 of PLL1_NUM_STAT

2.123 R122 Register (Address = 7Ah) [reset = 0h]

R122 is shown in Figure 123 and described in Table 125.

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Figure 123. R122 Register

7	6	5	4	3	2	1	0
PLL1_NUM_STAT							
R-0h							

Table 125. R122 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PLL1_NUM_STAT	R	0h	APLL1 Numerator Status Byte

2.124 R123 Register (Address = 7Bh) [reset = 0h]

R123 is shown in Figure 124 and described in Table 126.

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Figure 124. R123 Register

7	6	5	4	3	2	1	0
RESERVED						PLL1_NUM_SAT_HI	PLL1_NUM_SAT_LO
R-0h						R-0h	R-0h

Table 126. R123 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0h	
1	PLL1_NUM_SAT_HI	R	0h	PLL1 Numerator saturation Hi status
0	PLL1_NUM_SAT_LO	R	0h	PLL1 Numerator saturation Lo status

2.125 R124 Register (Address = 7Ch) [reset = X]

R124 is shown in Figure 125 and described in Table 127.

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Figure 125. R124 Register

7	6	5	4	3	2	1	0
RESERVED		PLL1_LF_R2					
R-X		R/W-X					

Table 127. R124 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	
5-0	PLL1_LF_R2	R/W	X	PLL1 Loop Filter R2 00h = 0.02 kΩ 02h = 0.33 kΩ 03h = 0.15 kΩ 04h = 0.61 kΩ 05h = 0.18 kΩ 06h = 0.23 kΩ 07h = 0.13 kΩ 08h = 1.1 kΩ 0Ah = 0.27 kΩ 0Bh = 0.14 kΩ 0Ch = 0.41 kΩ 0Dh = 0.16 kΩ 0Eh = 0.2 kΩ 10h = 0.83 kΩ 14h = 1.39 kΩ 18h = 1.88 kΩ 1Ch = 1.19 kΩ 1Dh = 0.95 kΩ 1Eh = 0.98 kΩ 1Fh = 0.91 kΩ 20h = 1.63 kΩ 24h = 2.19 kΩ 28h = 2.68 kΩ 2Ch = 1.99 kΩ 2Eh = 1.78 kΩ 2Fh = 1.71 kΩ 30h = 2.42 kΩ 34h = 2.98 kΩ 38h = 3.46 kΩ 3Ch = 2.78 kΩ 3Eh = 2.57 kΩ 3Fh = 2.49 kΩ

2.126 R125 Register (Address = 7Dh) [reset = X]

R125 is shown in Figure 126 and described in Table 128.

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Figure 126. R125 Register

7	6	5	4	3	2	1	0
RESERVED					RESERVED		
R-X					R/W-X		

Table 128. R125 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	X	
2-0	RESERVED	R/W	X	Reserved

2.127 R126 Register (Address = 7Eh) [reset = X]

R126 is shown in Figure 127 and described in Table 129.

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Figure 127. R126 Register

7	6	5	4	3	2	1	0
RESERVED		PLL1_LF_R3					
R-X		R/W-X					

Table 129. R126 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	
5-0	PLL1_LF_R3	R/W	X	PLL1 Loop Filter R3 00h = 0.02 kΩ 01h = 0.22 kΩ 02h = 0.6 kΩ 04h = 0.72 kΩ 05h = 0.17 kΩ 06h = 0.33 kΩ 07h = 0.14 kΩ 08h = 0.85 kΩ 0Ah = 1.41 kΩ 0Bh = 0.98 kΩ 12h = 2.21 kΩ 13h = 1.78 kΩ 14h = 2.33 kΩ 18h = 2.43 kΩ 1Ah = 3 kΩ 1Bh = 2.56 kΩ 1Ch = 3.12 kΩ 1Eh = 2.73 kΩ 1Fh = 2.54 kΩ 20h = 3.25 kΩ 22h = 3.81 kΩ 24h = 3.93 kΩ 26h = 3.55 kΩ 27h = 3.35 kΩ 28h = 4.03 kΩ 2Ah = 4.6 kΩ 2Bh = 4.16 kΩ 2Ch = 4.72 kΩ 2Eh = 4.33 kΩ 2Fh = 4.14 kΩ 30h = 4.83 kΩ 32h = 5.4 kΩ 33h = 4.96 kΩ 34h = 5.52 kΩ 36h = 5.13 kΩ 37h = 4.94 kΩ 38h = 5.62 kΩ 3Ah = 6.18 kΩ 3Ch = 6.3 kΩ 3Dh = 5.76 kΩ 3Eh = 5.92 kΩ 3Fh = 5.72 kΩ

2.128 R127 Register (Address = 7Fh) [reset = X]

R127 is shown in Figure 128 and described in Table 130.

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Figure 128. R127 Register

7	6	5	4	3	2	1	0
RESERVED		PLL1_LF_R4					
R-X		R/W-X					

Table 130. R127 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	
5-0	PLL1_LF_R4	R/W	X	PLL1 Loop Filter R4 See PLL1_LF_R3 for bit settings.

2.129 R128 Register (Address = 80h) [reset = X]

R128 is shown in Figure 129 and described in Table 131.

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Figure 129. R128 Register

7	6	5	4	3	2	1	0
RESERVED	PLL1_LF_C4			RESERVED	PLL1_LF_C3		
R-X	R/W-X			R-X	R/W-X		

Table 131. R128 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	X	
6-4	PLL1_LF_C4	R/W	X	PLL1 Loop Filter C4 See PLL1_LF_C3 for bit settings.
3	RESERVED	R	X	
2-0	PLL1_LF_C3	R/W	X	PLL1 Loop Filter C3 0h = 0 pF 1h = 10 pF 2h = 20 pF 3h = 30 pF 4h = 40 pF 5h = 50 pF 6h = 60 pF 7h = 70 pF

2.130 R129 Register (Address = 81h) [reset = X]

R129 is shown in Figure 130 and described in Table 132.

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Figure 130. R129 Register

7	6	5	4	3	2	1	0
RESERVED							PLL2_NDIV[8:8]
R-X							R/W-X

Table 132. R129 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	X	
0	PLL2_NDIV[8:8]	R/W	X	Bit 8 of PLL2_NDIV

2.131 R130 Register (Address = 82h) [reset = X]

R130 is shown in Figure 131 and described in Table 133.

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Figure 131. R130 Register

7	6	5	4	3	2	1	0
PLL2_NDIV							
R/W-X							

Table 133. R130 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PLL2_NDIV	R/W	X	PLL2 N Divider

2.132 R131 Register (Address = 83h) [reset = X]

R131 is shown in Figure 132 and described in Table 134.

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Figure 132. R131 Register

7	6	5	4	3	2	1	0
PLL2_NUM[39:32]							
R/W-X							

Table 134. R131 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PLL2_NUM[39:32]	R/W	X	Bits 39:32 of PLL2_NUM

2.133 R132 Register (Address = 84h) [reset = X]

R132 is shown in Figure 133 and described in Table 135.

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Figure 133. R132 Register

7	6	5	4	3	2	1	0
PLL2_NUM[31:24]							
R/W-X							

Table 135. R132 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PLL2_NUM[31:24]	R/W	X	Bits 31:24 of PLL2_NUM

2.134 R133 Register (Address = 85h) [reset = X]

R133 is shown in Figure 134 and described in Table 136.

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Figure 134. R133 Register

7	6	5	4	3	2	1	0
PLL2_NUM[23:16]							
R/W-X							

Table 136. R133 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PLL2_NUM[23:16]	R/W	X	Bits 23:16 of PLL2_NUM

2.135 R134 Register (Address = 86h) [reset = X]

R134 is shown in Figure 135 and described in Table 137.

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Figure 135. R134 Register

7	6	5	4	3	2	1	0
PLL2_NUM[15:8]							
R/W-X							

Table 137. R134 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PLL2_NUM[15:8]	R/W	X	Bits 15:8 of PLL2_NUM

2.136 R135 Register (Address = 87h) [reset = X]

R135 is shown in Figure 136 and described in Table 138.

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Figure 136. R135 Register

7	6	5	4	3	2	1	0
PLL2_NUM							
R/W-X							

Table 138. R135 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PLL2_NUM	R/W	X	PLL2 Fractional Divider Numerator

2.137 R136 Register (Address = 88h) [reset = X]

R136 is shown in Figure 137 and described in Table 139.

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Figure 137. R136 Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED		PLL2_DTHRMODE		PLL2_ORDER		
R-X	R/W-X		R/W-X		R/W-X		

Table 139. R136 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	X	
6-5	RESERVED	R/W	X	Reserved
4-3	PLL2_DTHRMODE	R/W	X	SDM Dither Mode 0h = Weak 1h = Medium 2h = Strong 3h = Disabled
2-0	PLL2_ORDER	R/W	X	APLL2 SDM Order 0h = Integer Mode 1h = 1st 2h = 2nd 3h = 3rd 4h = 4th

2.138 R137 Register (Address = 89h) [reset = X]

R137 is shown in Figure 138 and described in Table 140.

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Figure 138. R137 Register

7	6	5	4	3	2	1	0
RESERVED							RESERVED
R-X							R/W-X

Table 140. R137 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	X	
0	RESERVED	R/W	X	Reserved

2.139 R138 Register (Address = 8Ah) [reset = X]

R138 is shown in Figure 139 and described in Table 141.

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Figure 139. R138 Register

7	6	5	4	3	2	1	0
RESERVED					RESERVED	RESERVED	PLL2_MODE
R-X					R/W-X	R/W-X	R/W-X

Table 141. R138 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	X	
2	RESERVED	R/W	X	Reserved
1	RESERVED	R/W	X	Reserved
0	PLL2_MODE	R/W	X	PLL2 operational mode 0h = Free-run mode (APLL only) 1h = DPLL mode

2.140 R139 Register (Address = 8Bh) [reset = X]

R139 is shown in Figure 140 and described in Table 142.

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Figure 140. R139 Register

7	6	5	4	3	2	1	0
RESERVED		RESERVED					
R-X		R/W-X					

Table 142. R139 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	
5-0	RESERVED	R/W	X	Reserved

2.141 R140 Register (Address = 8Ch) [reset = X]

R140 is shown in Figure 141 and described in Table 143.

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Figure 141. R140 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 143. R140 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.142 R141 Register (Address = 8Dh) [reset = X]

R141 is shown in Figure 142 and described in Table 144.

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Figure 142. R141 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 144. R141 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.143 R142 Register (Address = 8Eh) [reset = X]

R142 is shown in Figure 143 and described in Table 145.

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Figure 143. R142 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 145. R142 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.144 R143 Register (Address = 8Fh) [reset = X]

R143 is shown in Figure 144 and described in Table 146.

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Figure 144. R143 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 146. R143 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.145 R144 Register (Address = 90h) [reset = 0h]

R144 is shown in Figure 145 and described in Table 147.

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Figure 145. R144 Register

7	6	5	4	3	2	1	0
RESERVED							RESERVED
R-0h							R/W-0h

Table 147. R144 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0h	
0	RESERVED	R/W	0h	Reserved

2.146 R145 Register (Address = 91h) [reset = 0h]

R145 is shown in Figure 146 and described in Table 148.

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Figure 146. R145 Register

7	6	5	4	3	2	1	0
PLL2_NUM_STAT[39:32]							
R-0h							

Table 148. R145 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PLL2_NUM_STAT[39:32]	R	0h	Bits 39:32 of PLL2_NUM_STAT

2.147 R146 Register (Address = 92h) [reset = 0h]

R146 is shown in Figure 147 and described in Table 149.

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Figure 147. R146 Register

7	6	5	4	3	2	1	0
PLL2_NUM_STAT[31:24]							
R-0h							

Table 149. R146 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PLL2_NUM_STAT[31:24]	R	0h	Bits 31:24 of PLL2_NUM_STAT

2.148 R147 Register (Address = 93h) [reset = 0h]

R147 is shown in Figure 148 and described in Table 150.

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Figure 148. R147 Register

7	6	5	4	3	2	1	0
PLL2_NUM_STAT[23:16]							
R-0h							

Table 150. R147 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PLL2_NUM_STAT[23:16]	R	0h	Bits 23:16 of PLL2_NUM_STAT

2.149 R148 Register (Address = 94h) [reset = 0h]

R148 is shown in Figure 149 and described in Table 151.

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Figure 149. R148 Register

7	6	5	4	3	2	1	0
PLL2_NUM_STAT[15:8]							
R-0h							

Table 151. R148 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PLL2_NUM_STAT[15:8]	R	0h	Bits 15:8 of PLL2_NUM_STAT

2.150 R149 Register (Address = 95h) [reset = 0h]

R149 is shown in Figure 150 and described in Table 152.

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Figure 150. R149 Register

7	6	5	4	3	2	1	0
PLL2_NUM_STAT							
R-0h							

Table 152. R149 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PLL2_NUM_STAT	R	0h	APLL2 Numerator Status

2.151 R150 Register (Address = 96h) [reset = 0h]

R150 is shown in Figure 151 and described in Table 153.

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Figure 151. R150 Register

7	6	5	4	3	2	1	0
RESERVED						PLL2_NUM_SAT_HI	PLL2_NUM_SAT_LO
R-0h						R-0h	R-0h

Table 153. R150 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0h	
1	PLL2_NUM_SAT_HI	R	0h	PLL2 Numerator saturation Hi status
0	PLL2_NUM_SAT_LO	R	0h	PLL2 Numerator saturation Lo status

2.152 R151 Register (Address = 97h) [reset = X]

R151 is shown in Figure 152 and described in Table 154.

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Figure 152. R151 Register

7	6	5	4	3	2	1	0
RESERVED				PLL2_LF_R2			
R-X				R/W-X			

Table 154. R151 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	
5-0	PLL2_LF_R2	R/W	X	PLL2 Loop Filter R2 See PLL1_LF_R2 for bit settings.

2.153 R152 Register (Address = 98h) [reset = X]

R152 is shown in Figure 153 and described in Table 155.

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Figure 153. R152 Register

7	6	5	4	3	2	1	0
RESERVED					RESERVED		
R-X					R/W-X		

Table 155. R152 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	X	
2-0	RESERVED	R/W	X	Reserved

2.154 R153 Register (Address = 99h) [reset = X]

R153 is shown in Figure 154 and described in Table 156.

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Figure 154. R153 Register

7	6	5	4	3	2	1	0
RESERVED				PLL2_LF_R3			
R-X				R/W-X			

Table 156. R153 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	
5-0	PLL2_LF_R3	R/W	X	PLL2 Loop Filter R3 See PLL1_LF_R3 for bit settings.

2.155 R154 Register (Address = 9Ah) [reset = X]

R154 is shown in Figure 155 and described in Table 157.

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Figure 155. R154 Register

7	6	5	4	3	2	1	0
RESERVED				PLL2_LF_R4			
R-X				R/W-X			

Table 157. R154 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	
5-0	PLL2_LF_R4	R/W	X	PLL2 Loop Filter R4 See PLL1_LF_R3 for bit settings.

2.156 R155 Register (Address = 9Bh) [reset = X]

R155 is shown in Figure 156 and described in Table 158.

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Figure 156. R155 Register

7	6	5	4	3	2	1	0
RESERVED	PLL2_LF_C4			RESERVED	PLL2_LF_C3		
R-X	R/W-X			R-X	R/W-X		

Table 158. R155 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	X	
6-4	PLL2_LF_C4	R/W	X	PLL2 Loop Filter C4 See PLL1_LF_C3 for bit settings.
3	RESERVED	R	X	
2-0	PLL2_LF_C3	R/W	X	PLL2 Loop Filter C3 See PLL1_LF_C3 for bit settings.

2.157 R156 Register (Address = 9Ch) [reset = X]

R156 is shown in Figure 157 and described in Table 159.

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Figure 157. R156 Register

7	6	5	4	3	2	1	0
RESERVED						RESERVED	
R-X						R/W-X	

Table 159. R156 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	X	
1-0	RESERVED	R/W	X	Reserved

2.158 R157 Register (Address = 9Dh) [reset = X]

R157 is shown in Figure 158 and described in Table 160.

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Figure 158. R157 Register

7	6	5	4	3	2	1	0
RESERVED			RESERVED		RESERVED		
R-X			R/W-X		R/W-X		

Table 160. R157 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	X	
4-3	RESERVED	R/W	X	Reserved
2-0	RESERVED	R/W	X	Reserved

2.159 R158 Register (Address = 9Eh) [reset = X]

R158 is shown in Figure 159 and described in Table 161.

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Figure 159. R158 Register

7	6	5	4	3	2	1	0
RESERVED						RESERVED	
R-X						R/W-X	

Table 161. R158 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	X	
1-0	RESERVED	R/W	X	Reserved

2.160 R159 Register (Address = 9Fh) [reset = X]

R159 is shown in Figure 160 and described in Table 162.

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Figure 160. R159 Register

7	6	5	4	3	2	1	0
RESERVED				RESERVED			
R-X				R/W-X			

Table 162. R159 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	X	
3-0	RESERVED	R/W	X	Reserved

2.161 R160 Register (Address = A0h) [reset = X]

R160 is shown in Figure 161 and described in Table 163.

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Figure 161. R160 Register

7	6	5	4	3	2	1	0
RESERVED				RESERVED			
R/W-X				R/W-X			

Table 163. R160 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	X	Reserved
3-0	RESERVED	R/W	X	Reserved

2.162 R161 Register (Address = A1h) [reset = X]

R161 is shown in Figure 162 and described in Table 164.

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Figure 162. R161 Register

7	6	5	4	3	2	1	0
RESERVED						RESERVED	
R-X						R/W-X	

Table 164. R161 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	X	
1-0	RESERVED	R/W	X	Reserved

2.163 R162 Register (Address = A2h) [reset = X]

R162 is shown in Figure 163 and described in Table 165.

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Figure 163. R162 Register

7	6	5	4	3	2	1	0
RESERVED				RESERVED			
R-X				R/W-X			

Table 165. R162 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	X	
3-0	RESERVED	R/W	X	Reserved

2.164 R163 Register (Address = A3h) [reset = X]

R163 is shown in Figure 164 and described in Table 166.

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Figure 164. R163 Register

7	6	5	4	3	2	1	0
RESERVED				RESERVED			
R/W-X				R/W-X			

Table 166. R163 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	X	Reserved
3-0	RESERVED	R/W	X	Reserved

2.165 R164 Register (Address = A4h) [reset = X]

R164 is shown in Figure 165 and described in Table 167.

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Figure 165. R164 Register

7	6	5	4	3	2	1	0
RESERVED		RESERVED			RESERVED		
R-X		R/W-X			R/W-X		

Table 167. R164 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	
5-3	RESERVED	R/W	X	Reserved
2-0	RESERVED	R/W	X	Reserved

2.166 R165 Register (Address = A5h) [reset = X]

R165 is shown in Figure 166 and described in Table 168.

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Figure 166. R165 Register

7	6	5	4	3	2	1	0
NVMSCRC							
R-X							

Table 168. R165 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	NVMSCRC	R	X	NVM Stored CRC

2.167 R166 Register (Address = A6h) [reset = X]

R166 is shown in Figure 167 and described in Table 169.

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Figure 167. R166 Register

7	6	5	4	3	2	1	0
NVMCNT							
R-X							

Table 169. R166 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	NVMCNT	R	X	NVM Program Count The NVMCNT increments automatically after every EEPROM Erase/Program Cycle (after a subsequent power-cycle or hard reset). The NVMCNT value is retrieved automatically after reset or after a NVM Commit operation.

2.168 R167 Register (Address = A7h) [reset = 0h]

R167 is shown in Figure 168 and described in Table 170.

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Figure 168. R167 Register

7	6	5	4	3	2	1	0
RESERVED	REGCOMMIT	NVMCRCERR	RESERVED	NVMCOMMIT	NVMBUSY	NVM_ERASE_PROG	
R-0h	R/W1C-0h	R-0h	R/W-0h	R/W1C-0h	R-0h	R/W1C-0h	

Table 170. R167 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	REGCOMMIT	R/W1C	0h	REG Commit to NVM SRAM Array The REGCOMMIT bit is used to initiate a transfer from the on-chip registers back to the corresponding location in the NVM SRAM Array. The REGCOMMIT bit is automatically cleared to 0 when the transfer is complete.
5	NVMCRCERR	R	0h	NVM CRC Error Indication This bit will read 1 when a CRC Error has been detected reading back from on-chip EEPROM during device initialization, where the NVMLCRC value does not match NVMSCRC. This bit can only be cleared by successful EEPROM programming and power-on/reset cycle, such that the NVMLCRC value matches NVMSCRC.
4	RESERVED	R/W	0h	Reserved
3	NVMCOMMIT	R/W1C	0h	NVM Commit to Registers The NVMCOMMIT bit is used to initiate a transfer of the on-chip EEPROM contents to internal registers. The transfer happens automatically after reset or when NVMCOMMIT is set to 1. The NVMCOMMIT bit is automatically cleared to 0. The registers cannot be read while a NVM Commit operation is taking place.
2	NVMBUSY	R	0h	NVM Program Busy Indication This bit will read 1 when an EEPROM Erase/Program cycle is active, during which the EEPROM cannot be accessed.

Table 170. R167 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1-0	NVM_ERASE_PROG	R/W1C	0h	NVM Erase/Program Start This bit field is used to initiate an internal EEPROM Erase/Program sequence. The sequence is only executed if the immediately preceding register transaction was a write to the NVMUNLK register with the appropriate unlock code. The NVM Erase/Program sequence takes about 230 ms total (115 ms for Erase or Program). 0h = NVM Idle 3h = Start NVM Erase/Program

2.169 R168 Register (Address = A8h) [reset = 0h]

R168 is shown in Figure 169 and described in Table 171.

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Figure 169. R168 Register

7	6	5	4	3	2	1	0
NVMLCRC							
R-0h							

Table 171. R168 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	NVMLCRC	R	0h	NVM Live CRC This field holds the Live CRC computed from the EEPROM data during device initialization. During initialization, the internal EEPROM controller does a CRC check to compare the Live CRC value with the Stored CRC value written to EEPROM (NVMSCRC byte) in the last NVM program cycle. If the Live and Stored CRC values match (no CRC error), the EEPROM data is valid and the device controller allows normal start-up operation to contiue; otherwise, if Live and Stored CRC do not match (CRC error detected), the EEPROM data is considered invalid and the controller halts start-up operation after register load (e.g. PLL lock sequence, etc.). The CRC error status can be read from the NVMCRCERR bit.

2.170 R169 Register (Address = A9h) [reset = 0h]

R169 is shown in Figure 170 and described in Table 172.

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Figure 170. R169 Register

7	6	5	4	3	2	1	0
RESERVED				MEMADR[12:8]			
R-0h				R/W-0h			

Table 172. R169 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	
4-0	MEMADR[12:8]	R/W	0h	Bits 12:8 of MEMADR

2.171 R170 Register (Address = AAh) [reset = 0h]

R170 is shown in Figure 171 and described in Table 173.

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Figure 171. R170 Register

7	6	5	4	3	2	1	0
MEMADR							
R/W-0h							

Table 173. R170 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MEMADR	R/W	0h	Memory Address The MEMADR value determines the starting address for access to the on-chip memories. NVMDAT register = NVM EEPROM Data Array (Read only) RAMDAT register = NVM SRAM Data Array (Read/Write) ROMDAT register = ROM Data Array (Read only)

2.172 R171 Register (Address = ABh) [reset = 0h]

R171 is shown in Figure 172 and described in Table 174.

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Figure 172. R171 Register

7	6	5	4	3	2	1	0
NVMDAT							
R-0h							

Table 174. R171 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	NVMDAT	R	0h	EEPROM Read Data

2.173 R172 Register (Address = ACh) [reset = 0h]

R172 is shown in Figure 173 and described in Table 175.

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Figure 173. R172 Register

7	6	5	4	3	2	1	0
RAMDAT							
R/W-0h							

Table 175. R172 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RAMDAT	R/W	0h	RAM Read/Write Data

2.174 R173 Register (Address = ADh) [reset = 0h]

R173 is shown in Figure 174 and described in Table 176.

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Figure 174. R173 Register

7	6	5	4	3	2	1	0
RESERVED							
R-0h							

Table 176. R173 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R	0h	Reserved

2.175 R174 Register (Address = AEh) [reset = 0h]

R174 is shown in Figure 175 and described in Table 177.

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Figure 175. R174 Register

7	6	5	4	3	2	1	0
NVMUNLK							
R/W-0h							

Table 177. R174 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	NVMUNLK	R/W	0h	NVM Program Unlock This register must be written with a value of EAh (unlock code) immediately before setting the NVM_ERASE_PROG bits to 11b. Otherwise, the EEPROM Erase/Program sequence will not be triggered. EEPROM programming requires atomic writes to NVMUNLK followed by NVM_ERASE_PROG.

2.176 R175 Register (Address = AFh) [reset = 0h]

R175 is shown in Figure 176 and described in Table 178.

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Figure 176. R175 Register

7	6	5	4	3	2	1	0
RESERVED				REGCOMMIT_PG			
R-0h				R/W-0h			

Table 178. R175 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	
3-0	REGCOMMIT_PG	R/W	0h	Register Commit Page This must always be set to 0h, as there is only 1 register page in EEPROM.

2.177 R176 Register (Address = B0h) [reset = X]

R176 is shown in Figure 177 and described in Table 179.

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Figure 177. R176 Register

7	6	5	4	3	2	1	0
RESERVED		RESERVED	RESERVED	REF_A_DPLL1_EN	RESERVED	RESERVED	REF_B_DPLL2_EN
R-X		R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X

Table 179. R176 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	
5	RESERVED	R/W	X	Reserved
4	RESERVED	R/W	X	Reserved
3	REF_A_DPLL1_EN	R/W	X	Enables ref path "A" to DPLL1 TDC
2	RESERVED	R/W	X	Reserved
1	RESERVED	R/W	X	Reserved
0	REF_B_DPLL2_EN	R/W	X	Enables ref path "B" to DPLL2 TDC

2.178 R177 Register (Address = B1h) [reset = X]

R177 is shown in Figure 178 and described in Table 180.

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Figure 178. R177 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 180. R177 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.179 R178 Register (Address = B2h) [reset = X]

R178 is shown in Figure 179 and described in Table 181.

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Figure 179. R178 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 181. R178 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.180 R179 Register (Address = B3h) [reset = X]

R179 is shown in Figure 180 and described in Table 182.

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Figure 180. R179 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 182. R179 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.181 R180 Register (Address = B4h) [reset = X]

R180 is shown in Figure 181 and described in Table 183.

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Figure 181. R180 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 183. R180 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.182 R181 Register (Address = B5h) [reset = X]

R181 is shown in Figure 182 and described in Table 184.

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Figure 182. R181 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 184. R181 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.183 R182 Register (Address = B6h) [reset = X]

R182 is shown in Figure 183 and described in Table 185.

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Figure 183. R182 Register

7	6	5	4	3	2	1	0
MUTE_DPLL2_TCXO	MUTE_DPLL2_PHLOCK	MUTE_DPLL2_LOCK	MUTE_APLL2_LOCK	MUTE_DPLL1_TCXO	MUTE_DPLL1_PHLOCK	MUTE_DPLL1_LOCK	MUTE_APLL1_LOCK
R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X

Table 185. R182 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	MUTE_DPLL2_TCXO	R/W	X	DPLL2 mute enabled during TCXO loop and Reference loop staggered Output mute is released when DPLL2 reference loop filter is enabled.
6	MUTE_DPLL2_PHLOCK	R/W	X	DPLL2 mute enabled during phase lock
5	MUTE_DPLL2_LOCK	R/W	X	DPLL2 mute enabled during dpll lock
4	MUTE_APLL2_LOCK	R/W	X	APLL2 mute enabled during PLL lock
3	MUTE_DPLL1_TCXO	R/W	X	DPLL1 mute enabled during TCXO loop and Reference loop staggered Output mute is released when DPLL1 reference loop filter is enabled.
2	MUTE_DPLL1_PHLOCK	R/W	X	DPLL1 mute enabled during phase lock
1	MUTE_DPLL1_LOCK	R/W	X	DPLL1 mute enabled during dpll lock
0	MUTE_APLL1_LOCK	R/W	X	APLL1 mute enabled during PLL lock

2.184 R183 Register (Address = B7h) [reset = X]

R183 is shown in Figure 184 and described in Table 186.

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Figure 184. R183 Register

7	6	5	4	3	2	1	0
DETECT_MODE_REF3		DETECT_MODE_REF2		DETECT_MODE_REF1		DETECT_MODE_REF0	
R/W-X		R/W-X		R/W-X		R/W-X	

Table 186. R183 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	DETECT_MODE_REF3	R/W	X	REFx Amplitude Detector Mode for LVCMOS input mode 0h = Rising Slew Rate Detector 1h = Rising and Falling Slew Rate Detector 2h = Falling Slew Rate Detector
5-4	DETECT_MODE_REF2	R/W	X	REFx Amplitude Detector Mode for LVCMOS input mode 0h = Rising Slew Rate Detector 1h = Rising and Falling Slew Rate Detector 2h = Falling Slew Rate Detector
3-2	DETECT_MODE_REF1	R/W	X	REFx Amplitude Detector Mode for LVCMOS input mode 0h = Rising Slew Rate Detector 1h = Rising and Falling Slew Rate Detector 2h = Falling Slew Rate Detector

Table 186. R183 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1-0	DETECT_MODE_REF0	R/W	X	REFx Amplitude Detector Mode for LVCMOS input mode 0h = Rising Slew Rate Detector 1h = Rising and Falling Slew Rate Detector 2h = Falling Slew Rate Detector

2.185 R184 Register (Address = B8h) [reset = X]

R184 is shown in Figure 185 and described in Table 187.

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Figure 185. R184 Register

7	6	5	4	3	2	1	0
GPIO6_TYPE	GPIO5_TYPE	STAT1_TYPE	STAT0_TYPE	GPIO6_STAT_POL	GPIO5_STAT_POL	STAT1_POL	STAT0_POL
R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X

Table 187. R184 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO6_TYPE	R/W	X	Driver Type for GPIO[6:5] and STATUS[1:0] Outputs 0h = NMOS Open-drain driver 1h = LVCMOS driver
6	GPIO5_TYPE	R/W	X	Driver Type for GPIO[6:5] and STATUS[1:0] Outputs 0h = NMOS Open-drain driver 1h = LVCMOS driver
5	STAT1_TYPE	R/W	X	Driver Type for GPIO[6:5] and STATUS[1:0] Outputs 0h = NMOS Open-drain driver 1h = LVCMOS driver
4	STAT0_TYPE	R/W	X	Driver Type for GPIO[6:5] and STATUS[1:0] Outputs 0h = NMOS Open-drain driver 1h = LVCMOS driver
3	GPIO6_STAT_POL	R/W	X	GPIO6 Status Output Polarity 0h = Active High 1h = Active Low
2	GPIO5_STAT_POL	R/W	X	GPIO5 Status Output Polarity 0h = Active High 1h = Active Low
1	STAT1_POL	R/W	X	STATUS1 Status Output Polarity 0h = Active High 1h = Active Low
0	STAT0_POL	R/W	X	STATUS0 Status Output Polarity 0h = Active High 1h = Active Low

2.186 R185 Register (Address = B9h) [reset = X]

R185 is shown in Figure 186 and described in Table 188.

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Figure 186. R185 Register

7	6	5	4	3	2	1	0
DPLL_TCXO_MDIV_DBLR	RESERVED			DPLL_TCXO_MDIV			
R/W-X	R-X			R/W-X			

Table 188. R185 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	DPLL_TCXO_MDIV_DBLR	R/W	X	DPLL TCXO MDIV Doubler Enable
6-5	RESERVED	R	X	
4-0	DPLL_TCXO_MDIV	R/W	X	DPLL TCXO M Divider Divide value = Register value + 1. Valid register value is 00h to 1Fh.

2.187 R186 Register (Address = BAh) [reset = X]

R186 is shown in Figure 187 and described in Table 189.

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Figure 187. R186 Register

7	6	5	4	3	2	1	0
RESERVED		TCXO_DETECT_MODE		RESERVED	TCXO_FDET_BYP	TCXO_DETECT_BYP	TCXO_BUFSEL
R-X		R/W-X		R-X	R/W-X	R/W-X	R/W-X

Table 189. R186 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	
5-4	TCXO_DETECT_MODE	R/W	X	TCXO Input Amplitude Detector Mode 0h = Rising Slew Rate Detector 1h = Rising and Falling Slew Rate Detector 2h = Falling Slew Rate Detector
3	RESERVED	R	X	
2	TCXO_FDET_BYP	R/W	X	TCXO Frequency Detector Bypass If bypassed, the TCXO detector status is ignored and the XO input is considered valid by the PLL control state machines 0h = Detector Enabled 1h = Detector Bypassed (Ignored)
1	TCXO_DETECT_BYP	R/W	X	TCXO Amplitude Detector Bypass If bypassed, the TCXO detector status is ignored and the XO input is considered valid by the PLL control state machines 0h = Detector Enabled 1h = Detector Bypassed (Ignored)
0	TCXO_BUFSEL	R/W	X	TCXO Input Buffer Enable

2.188 R187 Register (Address = BBh) [reset = X]

R187 is shown in Figure 188 and described in Table 190.

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Figure 188. R187 Register

7	6	5	4	3	2	1	0
RESERVED				LVL_SEL_REF1		LVL_SEL_REF0	
R/W-X				R/W-X		R/W-X	

Table 190. R187 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	X	Reserved
3-2	LVL_SEL_REF1	R/W	X	REFx Input Amplitude Detector Specifies the minimum differential input peak-to-peak swing to be qualified. 0h = 400 mVpp 1h = 500 mVpp 2h = 600 mVpp
1-0	LVL_SEL_REF0	R/W	X	REFx Input Amplitude Detector Specifies the minimum differential input peak-to-peak swing to be qualified. 0h = 400 mVpp 1h = 500 mVpp 2h = 600 mVpp

2.189 R188 Register (Address = BCh) [reset = X]

R188 is shown in Figure 189 and described in Table 191.

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Figure 189. R188 Register

7	6	5	4	3	2	1	0
RESERVED				LVL_SEL_REF3		LVL_SEL_REF2	
R/W-X				R/W-X		R/W-X	

Table 191. R188 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	X	Reserved
3-2	LVL_SEL_REF3	R/W	X	REFx Input Amplitude Detector Specifies the minimum differential input peak-to-peak swing to be qualified. 0h = 400 mVpp 1h = 500 mVpp 2h = 600 mVpp
1-0	LVL_SEL_REF2	R/W	X	REFx Input Amplitude Detector Specifies the minimum differential input peak-to-peak swing to be qualified. 0h = 400 mVpp 1h = 500 mVpp 2h = 600 mVpp

2.190 R189 Register (Address = BDh) [reset = X]

R189 is shown in Figure 190 and described in Table 192.

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Figure 190. R189 Register

7	6	5	4	3	2	1	0
RESERVED		REF0_EARLY_DET_EN	REF0_PH_VALID_EN	REF0_VALTMR_EN	REF0_PPM_EN	REF0_MISSCLK_EN	REF0_AMPDET_EN
R-X		R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X

Table 192. R189 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	
5	REF0_EARLY_DET_EN	R/W	X	Ref0 Early Clock Detect Enable
4	REF0_PH_VALID_EN	R/W	X	Ref0 Phase Valid Detect Enable
3	REF0_VALTMR_EN	R/W	X	Ref0 Validation Timer Enable
2	REF0_PPM_EN	R/W	X	Ref0 Frequency ppm Detect Enable
1	REF0_MISSCLK_EN	R/W	X	Ref0 Missing Clock Detect Enable
0	REF0_AMPDET_EN	R/W	X	Ref0 Amplitude Detect Enable

2.191 R190 Register (Address = BEh) [reset = X]

R190 is shown in Figure 191 and described in Table 193.

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Figure 191. R190 Register

7	6	5	4	3	2	1	0
RESERVED		REF1_EARLY_DET_EN	REF1_PH_VALID_EN	REF1_VALTMR_EN	REF1_PPM_EN	REF1_MISSCLK_EN	REF1_AMPDET_EN
R-X		R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X

Table 193. R190 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	
5	REF1_EARLY_DET_EN	R/W	X	Ref1 Early Clock Detect Enable
4	REF1_PH_VALID_EN	R/W	X	Ref1 Phase Valid Detect Enable
3	REF1_VALTMR_EN	R/W	X	Ref1 Validation Timer Enable
2	REF1_PPM_EN	R/W	X	Ref1 Frequency ppm Detect Enable
1	REF1_MISSCLK_EN	R/W	X	Ref1 Missing Clock Detect Enable
0	REF1_AMPDET_EN	R/W	X	Ref1 Amplitude Detect Enable

2.192 R191 Register (Address = BFh) [reset = X]

R191 is shown in Figure 192 and described in Table 194.

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Figure 192. R191 Register

7	6	5	4	3	2	1	0
RESERVED		REF2_EARLY_DET_EN	REF2_PH_VALID_EN	REF2_VALTMR_EN	REF2_PPM_EN	REF2_MISSCLK_EN	REF2_AMPDET_EN
R-X		R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X

Table 194. R191 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	
5	REF2_EARLY_DET_EN	R/W	X	Ref2 Early Clock Detect Enable
4	REF2_PH_VALID_EN	R/W	X	Ref2 Phase Valid Detect Enable
3	REF2_VALTMR_EN	R/W	X	Ref2 Validation Timer Enable
2	REF2_PPM_EN	R/W	X	Ref2 Frequency ppm Detect Enable
1	REF2_MISSCLK_EN	R/W	X	Ref2 Missing Clock Detect Enable
0	REF2_AMPDET_EN	R/W	X	Ref2 Amplitude Detect Enable

2.193 R192 Register (Address = C0h) [reset = X]

R192 is shown in Figure 193 and described in Table 195.

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Figure 193. R192 Register

7	6	5	4	3	2	1	0
RESERVED		REF3_EARLY_DET_EN	REF3_PH_VALID_EN	REF3_VALTMR_EN	REF3_PPM_EN	REF3_MISSCLK_EN	REF3_AMPDET_EN
R-X		R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X

Table 195. R192 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	
5	REF3_EARLY_DET_EN	R/W	X	Ref3 Early Clock Detect Enable
4	REF3_PH_VALID_EN	R/W	X	Ref3 Phase Valid Detect Enable
3	REF3_VALTMR_EN	R/W	X	Ref3 Validation Timer Enable
2	REF3_PPM_EN	R/W	X	Ref3 Frequency ppm Detect Enable
1	REF3_MISSCLK_EN	R/W	X	Ref3 Missing Clock Detect Enable
0	REF3_AMPDET_EN	R/W	X	Ref3 Amplitude Detect Enable

2.194 R193 Register (Address = C1h) [reset = X]

R193 is shown in Figure 194 and described in Table 196.

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Figure 194. R193 Register

7	6	5	4	3	2	1	0
RESERVED		RESERVED					
R-X		R/W-X					

Table 196. R193 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	
5-0	RESERVED	R/W	X	Reserved

2.195 R194 Register (Address = C2h) [reset = X]

R194 is shown in Figure 195 and described in Table 197.

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Figure 195. R194 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 197. R194 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.196 R195 Register (Address = C3h) [reset = X]

R195 is shown in Figure 196 and described in Table 198.

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Figure 196. R195 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 198. R195 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.197 R196 Register (Address = C4h) [reset = X]

R196 is shown in Figure 197 and described in Table 199.

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Figure 197. R196 Register

7	6	5	4	3	2	1	0
RESERVED		RESERVED					
R-X		R/W-X					

Table 199. R196 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	
5-0	RESERVED	R/W	X	Reserved

2.198 R197 Register (Address = C5h) [reset = X]

R197 is shown in Figure 198 and described in Table 200.

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Figure 198. R197 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 200. R197 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.199 R198 Register (Address = C6h) [reset = X]

R198 is shown in Figure 199 and described in Table 201.

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Figure 199. R198 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 201. R198 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.200 R199 Register (Address = C7h) [reset = X]

R199 is shown in Figure 200 and described in Table 202.

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Figure 200. R199 Register

7	6	5	4	3	2	1	0
RESERVED		RESERVED					
R-X		R/W-X					

Table 202. R199 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	
5-0	RESERVED	R/W	X	Reserved

2.201 R200 Register (Address = C8h) [reset = X]

R200 is shown in Figure 201 and described in Table 203.

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Figure 201. R200 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 203. R200 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.202 R201 Register (Address = C9h) [reset = X]

R201 is shown in Figure 202 and described in Table 204.

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Figure 202. R201 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 204. R201 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.203 R202 Register (Address = CAh) [reset = X]

R202 is shown in Figure 203 and described in Table 205.

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Figure 203. R202 Register

7	6	5	4	3	2	1	0
RESERVED		RESERVED					
R-X		R/W-X					

Table 205. R202 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	
5-0	RESERVED	R/W	X	Reserved

2.204 R203 Register (Address = CBh) [reset = X]

R203 is shown in Figure 204 and described in Table 206.

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Figure 204. R203 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 206. R203 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.205 R204 Register (Address = CCh) [reset = X]

R204 is shown in Figure 205 and described in Table 207.

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Figure 205. R204 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 207. R204 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.206 R205 Register (Address = CDh) [reset = X]

R205 is shown in Figure 206 and described in Table 208.

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Figure 206. R205 Register

7	6	5	4	3	2	1	0
RESERVED				REF3_MISSCLK_VCOSEL	REF2_MISSCLK_VCOSEL	REF1_MISSCLK_VCOSEL	REF0_MISSCLK_VCOSEL
R/W-0h				R/W-X	R/W-X	R/W-X	R/W-X

Table 208. R205 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0h	Reserved
3	REF3_MISSCLK_VCOSEL	R/W	X	REFx Missing Clock Detector VCO selection 0h = VCO 1 1h = VCO 2
2	REF2_MISSCLK_VCOSEL	R/W	X	REFx Missing Clock Detector VCO selection 0h = VCO 1 1h = VCO 2
1	REF1_MISSCLK_VCOSEL	R/W	X	REFx Missing Clock Detector VCO selection 0h = VCO 1 1h = VCO 2

Table 208. R205 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	REF0_MISSCLK_VCOSEL	R/W	X	REFx Missing Clock Detector VCO selection 0h = VCO 1 1h = VCO 2

2.207 R206 Register (Address = CEh) [reset = X]

R206 is shown in Figure 207 and described in Table 209.

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Figure 207. R206 Register

7	6	5	4	3	2	1	0
RESERVED		RESERVED					
R-X		R/W-X					

Table 209. R206 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	
5-0	RESERVED	R/W	X	Reserved

2.208 R207 Register (Address = CFh) [reset = X]

R207 is shown in Figure 208 and described in Table 210.

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Figure 208. R207 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 210. R207 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.209 R208 Register (Address = D0h) [reset = X]

R208 is shown in Figure 209 and described in Table 211.

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Figure 209. R208 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 211. R208 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.210 R209 Register (Address = D1h) [reset = X]

R209 is shown in Figure 210 and described in Table 212.

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Figure 210. R209 Register

7	6	5	4	3	2	1	0
RESERVED		RESERVED					
R-X		R/W-X					

Table 212. R209 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	
5-0	RESERVED	R/W	X	Reserved

2.211 R210 Register (Address = D2h) [reset = X]

R210 is shown in Figure 211 and described in Table 213.

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Figure 211. R210 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 213. R210 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.212 R211 Register (Address = D3h) [reset = X]

R211 is shown in Figure 212 and described in Table 214.

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Figure 212. R211 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 214. R211 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.213 R212 Register (Address = D4h) [reset = X]

R212 is shown in Figure 213 and described in Table 215.

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Figure 213. R212 Register

7	6	5	4	3	2	1	0
RESERVED		RESERVED					
R-X		R/W-X					

Table 215. R212 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	
5-0	RESERVED	R/W	X	Reserved

2.214 R213 Register (Address = D5h) [reset = X]

R213 is shown in Figure 214 and described in Table 216.

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Figure 214. R213 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 216. R213 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.215 R214 Register (Address = D6h) [reset = X]

R214 is shown in Figure 215 and described in Table 217.

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Figure 215. R214 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 217. R214 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.216 R215 Register (Address = D7h) [reset = X]

R215 is shown in Figure 216 and described in Table 218.

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Figure 216. R215 Register

7	6	5	4	3	2	1	0
RESERVED		RESERVED					
R-X		R/W-X					

Table 218. R215 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	
5-0	RESERVED	R/W	X	Reserved

2.217 R216 Register (Address = D8h) [reset = X]

R216 is shown in Figure 217 and described in Table 219.

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Figure 217. R216 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 219. R216 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.218 R217 Register (Address = D9h) [reset = X]

R217 is shown in Figure 218 and described in Table 220.

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Figure 218. R217 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 220. R217 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.219 R218 Register (Address = DAh) [reset = X]

R218 is shown in Figure 219 and described in Table 221.

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Figure 219. R218 Register

7	6	5	4	3	2	1	0
RESERVED							SET_HOLD_CLK
R-X							R/W-X

Table 221. R218 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	X	
0	SET_HOLD_CLK	R/W	X	Selects the XO pins or TCXO_IN pin as the Holdover clock and "0-ppm" Comparison clock for all reference input (INx) frequency ppm monitors 0h = TCXO 1h = XO

2.220 R219 Register (Address = DBh) [reset = X]

R219 is shown in Figure 220 and described in Table 222.

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Figure 220. R219 Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED						
R-X	R/W-X						

Table 222. R219 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	X	
6-0	RESERVED	R/W	X	Reserved

2.221 R220 Register (Address = DCh) [reset = X]

R220 is shown in Figure 221 and described in Table 223.

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Figure 221. R220 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 223. R220 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.222 R221 Register (Address = DDh) [reset = X]

R221 is shown in Figure 222 and described in Table 224.

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Figure 222. R221 Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED						
R-X	R/W-X						

Table 224. R221 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	X	
6-0	RESERVED	R/W	X	Reserved

2.223 R222 Register (Address = DEh) [reset = X]

R222 is shown in Figure 223 and described in Table 225.

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Figure 223. R222 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 225. R222 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.224 R223 Register (Address = DFh) [reset = X]

R223 is shown in Figure 224 and described in Table 226.

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Figure 224. R223 Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED						
R-X	R/W-X						

Table 226. R223 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	X	
6-0	RESERVED	R/W	X	Reserved

2.225 R224 Register (Address = E0h) [reset = X]

R224 is shown in Figure 225 and described in Table 227.

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Figure 225. R224 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 227. R224 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.226 R225 Register (Address = E1h) [reset = X]

R225 is shown in Figure 226 and described in Table 228.

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Figure 226. R225 Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED						
R-X	R/W-X						

Table 228. R225 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	X	
6-0	RESERVED	R/W	X	Reserved

2.227 R226 Register (Address = E2h) [reset = X]

R226 is shown in Figure 227 and described in Table 229.

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Figure 227. R226 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 229. R226 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.228 R227 Register (Address = E3h) [reset = X]

R227 is shown in Figure 228 and described in Table 230.

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Figure 228. R227 Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED						
R-X	R/W-X						

Table 230. R227 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	X	
6-0	RESERVED	R/W	X	Reserved

2.229 R228 Register (Address = E4h) [reset = X]

R228 is shown in Figure 229 and described in Table 231.

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Figure 229. R228 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 231. R228 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.230 R229 Register (Address = E5h) [reset = X]

R229 is shown in Figure 230 and described in Table 232.

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Figure 230. R229 Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED						
R-X	R/W-X						

Table 232. R229 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	X	
6-0	RESERVED	R/W	X	Reserved

2.231 R230 Register (Address = E6h) [reset = X]

R230 is shown in Figure 231 and described in Table 233.

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Figure 231. R230 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 233. R230 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.232 R231 Register (Address = E7h) [reset = X]

R231 is shown in Figure 232 and described in Table 234.

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Figure 232. R231 Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED						
R-X	R/W-X						

Table 234. R231 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	X	
6-0	RESERVED	R/W	X	Reserved

2.233 R232 Register (Address = E8h) [reset = X]

R232 is shown in Figure 233 and described in Table 235.

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Figure 233. R232 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 235. R232 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.234 R233 Register (Address = E9h) [reset = X]

R233 is shown in Figure 234 and described in Table 236.

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Figure 234. R233 Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED						
R-X	R/W-X						

Table 236. R233 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	X	
6-0	RESERVED	R/W	X	Reserved

2.235 R234 Register (Address = EAh) [reset = X]

R234 is shown in Figure 235 and described in Table 237.

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Figure 235. R234 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 237. R234 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.236 R235 Register (Address = EBh) [reset = X]

R235 is shown in Figure 236 and described in Table 238.

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Figure 236. R235 Register

7	6	5	4	3	2	1	0
RESERVED		RESERVED		RESERVED		RESERVED	
R/W-X		R/W-X		R/W-X		R/W-X	

Table 238. R235 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	X	Reserved
5-4	RESERVED	R/W	X	Reserved
3-2	RESERVED	R/W	X	Reserved
1-0	RESERVED	R/W	X	Reserved

2.237 R236 Register (Address = ECh) [reset = X]

R236 is shown in Figure 237 and described in Table 239.

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Figure 237. R236 Register

7	6	5	4	3	2	1	0
RESERVED				RESERVED			
R-X				R/W-X			

Table 239. R236 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	X	
3-0	RESERVED	R/W	X	Reserved

2.238 R237 Register (Address = EDh) [reset = X]

R237 is shown in Figure 238 and described in Table 240.

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Figure 238. R237 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 240. R237 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.239 R238 Register (Address = EEh) [reset = X]

R238 is shown in Figure 239 and described in Table 241.

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Figure 239. R238 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 241. R238 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.240 R239 Register (Address = EFh) [reset = X]

R239 is shown in Figure 240 and described in Table 242.

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Figure 240. R239 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 242. R239 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.241 R240 Register (Address = F0h) [reset = X]

R240 is shown in Figure 241 and described in Table 243.

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Figure 241. R240 Register

7	6	5	4	3	2	1	0
RESERVED				RESERVED			
R-X				R/W-X			

Table 243. R240 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	X	
3-0	RESERVED	R/W	X	Reserved

2.242 R241 Register (Address = F1h) [reset = X]

R241 is shown in Figure 242 and described in Table 244.

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Figure 242. R241 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 244. R241 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.243 R242 Register (Address = F2h) [reset = X]

R242 is shown in Figure 243 and described in Table 245.

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Figure 243. R242 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 245. R242 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.244 R243 Register (Address = F3h) [reset = X]

R243 is shown in Figure 244 and described in Table 246.

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Figure 244. R243 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 246. R243 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.245 R244 Register (Address = F4h) [reset = X]

R244 is shown in Figure 245 and described in Table 247.

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Figure 245. R244 Register

7	6	5	4	3	2	1	0
RESERVED				RESERVED			
R-X				R/W-X			

Table 247. R244 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	X	
3-0	RESERVED	R/W	X	Reserved

2.246 R245 Register (Address = F5h) [reset = X]

R245 is shown in Figure 246 and described in Table 248.

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Figure 246. R245 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 248. R245 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.247 R246 Register (Address = F6h) [reset = X]

R246 is shown in Figure 247 and described in Table 249.

Return to Summary Table.

Figure 247. R246 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 249. R246 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.248 R247 Register (Address = F7h) [reset = X]

R247 is shown in Figure 248 and described in Table 250.

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Figure 248. R247 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 250. R247 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.249 R248 Register (Address = F8h) [reset = X]

R248 is shown in Figure 249 and described in Table 251.

Return to Summary Table.

Figure 249. R248 Register

7	6	5	4	3	2	1	0
RESERVED				RESERVED			
R-X				R/W-X			

Table 251. R248 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	X	
3-0	RESERVED	R/W	X	Reserved

2.250 R249 Register (Address = F9h) [reset = X]

R249 is shown in Figure 250 and described in Table 252.

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Figure 250. R249 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 252. R249 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.251 R250 Register (Address = FAh) [reset = X]

R250 is shown in Figure 251 and described in Table 253.

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Figure 251. R250 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 253. R250 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.252 R251 Register (Address = FBh) [reset = X]

R251 is shown in Figure 252 and described in Table 254.

Return to Summary Table.

Figure 252. R251 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 254. R251 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.253 R252 Register (Address = FCh) [reset = X]

R252 is shown in Figure 253 and described in Table 255.

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Figure 253. R252 Register

7	6	5	4	3	2	1	0
RESERVED				RESERVED			
R-X				R/W-X			

Table 255. R252 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	X	
3-0	RESERVED	R/W	X	Reserved

2.254 R253 Register (Address = FDh) [reset = X]

R253 is shown in Figure 254 and described in Table 256.

Return to Summary Table.

Figure 254. R253 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 256. R253 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.255 R254 Register (Address = FEh) [reset = X]

R254 is shown in Figure 255 and described in Table 257.

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Figure 255. R254 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 257. R254 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.256 R255 Register (Address = FFh) [reset = X]

R255 is shown in Figure 256 and described in Table 258.

Return to Summary Table.

Figure 256. R255 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 258. R255 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.257 R256 Register (Address = 100h) [reset = X]

R256 is shown in Figure 257 and described in Table 259.

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Figure 257. R256 Register

7	6	5	4	3	2	1	0
RESERVED				RESERVED			
R-X				R/W-X			

Table 259. R256 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	X	
3-0	RESERVED	R/W	X	Reserved

2.258 R257 Register (Address = 101h) [reset = X]

R257 is shown in Figure 258 and described in Table 260.

Return to Summary Table.

Figure 258. R257 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 260. R257 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.259 R258 Register (Address = 102h) [reset = X]

R258 is shown in Figure 259 and described in Table 261.

Return to Summary Table.

Figure 259. R258 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 261. R258 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.260 R259 Register (Address = 103h) [reset = X]

R259 is shown in Figure 260 and described in Table 262.

Return to Summary Table.

Figure 260. R259 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 262. R259 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.261 R260 Register (Address = 104h) [reset = X]

R260 is shown in Figure 261 and described in Table 263.

Return to Summary Table.

Figure 261. R260 Register

7	6	5	4	3	2	1	0
RESERVED				RESERVED			
R-X				R/W-X			

Table 263. R260 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	X	
3-0	RESERVED	R/W	X	Reserved

2.262 R261 Register (Address = 105h) [reset = X]

R261 is shown in Figure 262 and described in Table 264.

Return to Summary Table.

Figure 262. R261 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 264. R261 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.263 R262 Register (Address = 106h) [reset = X]

R262 is shown in Figure 263 and described in Table 265.

Return to Summary Table.

Figure 263. R262 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 265. R262 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.264 R263 Register (Address = 107h) [reset = X]

R263 is shown in Figure 264 and described in Table 266.

Return to Summary Table.

Figure 264. R263 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 266. R263 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.265 R264 Register (Address = 108h) [reset = X]

R264 is shown in Figure 265 and described in Table 267.

Return to Summary Table.

Figure 265. R264 Register

7	6	5	4	3	2	1	0
RESERVED				RESERVED			
R-X				R/W-X			

Table 267. R264 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	X	
3-0	RESERVED	R/W	X	Reserved

2.266 R265 Register (Address = 109h) [reset = X]

R265 is shown in Figure 266 and described in Table 268.

Return to Summary Table.

Figure 266. R265 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 268. R265 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.267 R266 Register (Address = 10Ah) [reset = X]

R266 is shown in Figure 267 and described in Table 269.

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Figure 267. R266 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 269. R266 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.268 R267 Register (Address = 10Bh) [reset = X]

R267 is shown in Figure 268 and described in Table 270.

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Figure 268. R267 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 270. R267 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.269 R268 Register (Address = 10Ch) [reset = X]

R268 is shown in Figure 269 and described in Table 271.

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Figure 269. R268 Register

7	6	5	4	3	2	1	0
RESERVED				RESERVED			
R-X				R/W-X			

Table 271. R268 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	X	
4-0	RESERVED	R/W	X	Reserved

2.270 R269 Register (Address = 10Dh) [reset = X]

R269 is shown in Figure 270 and described in Table 272.

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Figure 270. R269 Register

7	6	5	4	3	2	1	0
RESERVED				RESERVED			
R-X				R/W-X			

Table 272. R269 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	X	
4-0	RESERVED	R/W	X	Reserved

2.271 R270 Register (Address = 10Eh) [reset = X]

R270 is shown in Figure 271 and described in Table 273.

Return to Summary Table.

Figure 271. R270 Register

7	6	5	4	3	2	1	0
RESERVED				RESERVED			
R-X				R/W-X			

Table 273. R270 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	X	
4-0	RESERVED	R/W	X	Reserved

2.272 R271 Register (Address = 10Fh) [reset = X]

R271 is shown in Figure 272 and described in Table 274.

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Figure 272. R271 Register

7	6	5	4	3	2	1	0
RESERVED				RESERVED			
R-X				R/W-X			

Table 274. R271 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	X	
4-0	RESERVED	R/W	X	Reserved

2.273 R272 Register (Address = 110h) [reset = X]

R272 is shown in Figure 273 and described in Table 275.

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Figure 273. R272 Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED						
R-X	R/W-X						

Table 275. R272 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	X	
6-0	RESERVED	R/W	X	Reserved

2.274 R273 Register (Address = 111h) [reset = X]

R273 is shown in Figure 274 and described in Table 276.

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Figure 274. R273 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 276. R273 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.275 R274 Register (Address = 112h) [reset = X]

R274 is shown in Figure 275 and described in Table 277.

Return to Summary Table.

Figure 275. R274 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 277. R274 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.276 R275 Register (Address = 113h) [reset = X]

R275 is shown in Figure 276 and described in Table 278.

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Figure 276. R275 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 278. R275 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.277 R276 Register (Address = 114h) [reset = X]

R276 is shown in Figure 277 and described in Table 279.

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Figure 277. R276 Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED						
R-X	R/W-X						

Table 279. R276 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	X	
6-0	RESERVED	R/W	X	Reserved

2.278 R277 Register (Address = 115h) [reset = X]

R277 is shown in Figure 278 and described in Table 280.

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Figure 278. R277 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 280. R277 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.279 R278 Register (Address = 116h) [reset = X]

R278 is shown in Figure 279 and described in Table 281.

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Figure 279. R278 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 281. R278 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.280 R279 Register (Address = 117h) [reset = X]

R279 is shown in Figure 280 and described in Table 282.

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Figure 280. R279 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 282. R279 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.281 R280 Register (Address = 118h) [reset = X]

R280 is shown in Figure 281 and described in Table 283.

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Figure 281. R280 Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED						
R-X	R/W-X						

Table 283. R280 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	X	
6-0	RESERVED	R/W	X	Reserved

2.282 R281 Register (Address = 119h) [reset = X]

R281 is shown in Figure 282 and described in Table 284.

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Figure 282. R281 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 284. R281 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.283 R282 Register (Address = 11Ah) [reset = X]

R282 is shown in Figure 283 and described in Table 285.

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Figure 283. R282 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 285. R282 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.284 R283 Register (Address = 11Bh) [reset = X]

R283 is shown in Figure 284 and described in Table 286.

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Figure 284. R283 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 286. R283 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.285 R284 Register (Address = 11Ch) [reset = X]

R284 is shown in Figure 285 and described in Table 287.

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Figure 285. R284 Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED						
R-X	R/W-X						

Table 287. R284 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	X	
6-0	RESERVED	R/W	X	Reserved

2.286 R285 Register (Address = 11Dh) [reset = X]

R285 is shown in Figure 286 and described in Table 288.

Return to Summary Table.

Figure 286. R285 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 288. R285 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.287 R286 Register (Address = 11Eh) [reset = X]

R286 is shown in Figure 287 and described in Table 289.

Return to Summary Table.

Figure 287. R286 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 289. R286 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.288 R287 Register (Address = 11Fh) [reset = X]

R287 is shown in Figure 288 and described in Table 290.

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Figure 288. R287 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 290. R287 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.289 R288 Register (Address = 120h) [reset = X]

R288 is shown in Figure 289 and described in Table 291.

Return to Summary Table.

Figure 289. R288 Register

7	6	5	4	3	2	1	0
RESERVED		RESERVED					
R-X		R/W-X					

Table 291. R288 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	
5-0	RESERVED	R/W	X	Reserved

2.290 R289 Register (Address = 121h) [reset = X]

R289 is shown in Figure 290 and described in Table 292.

Return to Summary Table.

Figure 290. R289 Register

7	6	5	4	3	2	1	0
RESERVED		RESERVED					
R-X		R/W-X					

Table 292. R289 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	
5-0	RESERVED	R/W	X	Reserved

2.291 R290 Register (Address = 122h) [reset = X]

R290 is shown in Figure 291 and described in Table 293.

Return to Summary Table.

Figure 291. R290 Register

7	6	5	4	3	2	1	0
RESERVED		RESERVED					
R-X		R/W-X					

Table 293. R290 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	
5-0	RESERVED	R/W	X	Reserved

2.292 R291 Register (Address = 123h) [reset = X]

R291 is shown in Figure 292 and described in Table 294.

Return to Summary Table.

Figure 292. R291 Register

7	6	5	4	3	2	1	0
RESERVED		RESERVED					
R-X		R/W-X					

Table 294. R291 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	
5-0	RESERVED	R/W	X	Reserved

2.293 R292 Register (Address = 124h) [reset = X]

R292 is shown in Figure 293 and described in Table 295.

Return to Summary Table.

Figure 293. R292 Register

7	6	5	4	3	2	1	0
RESERVED	DPLL1_REF1_AUTO_PRTY			RESERVED	DPLL1_REF0_AUTO_PRTY		
R/W-X	R/W-X			R/W-X	R/W-X		

Table 295. R292 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	X	Reserved
6-4	DPLL1_REF1_AUTO_PRTY	R/W	X	Sets priorty for Ref1. See DPLL1_REF0_AUTO_PRTY bit settings.
3	RESERVED	R/W	X	Reserved
2-0	DPLL1_REF0_AUTO_PRTY	R/W	X	Sets priorty for Ref0 0h = Ignore 1h = 1 (Highest priority) 2h = 2 3h = 3 4h = 4 5h = 5 6h = 6 (Lowest priority)

2.294 R293 Register (Address = 125h) [reset = X]

R293 is shown in Figure 294 and described in Table 296.

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Figure 294. R293 Register

7	6	5	4	3	2	1	0
RESERVED	DPLL1_REF3_AUTO_PRTY			RESERVED	DPLL1_REF2_AUTO_PRTY		
R/W-X	R/W-X			R/W-X	R/W-X		

Table 296. R293 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	X	Reserved
6-4	DPLL1_REF3_AUTO_PRTY	R/W	X	Sets priorty for Ref3 See DPLL1_REF0_AUTO_PRTY bit settings.
3	RESERVED	R/W	X	Reserved
2-0	DPLL1_REF2_AUTO_PRTY	R/W	X	Sets priorty for Ref2 See DPLL1_REF0_AUTO_PRTY bit settings.

2.295 R294 Register (Address = 126h) [reset = X]

R294 is shown in Figure 295 and described in Table 297.

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Figure 295. R294 Register

7	6	5	4	3	2	1	0
RESERVED	DPLL1_REF5_AUTO_PRTY			RESERVED	RESERVED		
R/W-X	R/W-X			R/W-X	R/W-X		

Table 297. R294 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	X	Reserved
6-4	DPLL1_REF5_AUTO_PRTY	R/W	X	Sets priorty for Ref5 See DPLL1_REF0_AUTO_PRTY bit settings.
3	RESERVED	R/W	X	Reserved
2-0	RESERVED	R/W	X	Reserved

2.296 R295 Register (Address = 127h) [reset = X]

R295 is shown in Figure 296 and described in Table 298.

Return to Summary Table.

Figure 296. R295 Register

7	6	5	4	3	2	1	0
RESERVED			DPLL1_VAL_FL_EN	DPLL1_VAL_PL_EN	DPLL1_VAL_TCXO_EN	RESERVED	DPLL1_TCXO_LOOPBACK_EN
R-X			R/W-X	R/W-X	R/W-X	R-X	R/W-X

Table 298. R295 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	X	
4	DPLL1_VAL_FL_EN	R/W	X	Assert reference valid for loopback mode immediately after frequency lock

Table 298. R295 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	DPLL1_VAL_PL_EN	R/W	X	Assert reference valid for loopback mode after either phase lock or timeout counter
2	DPLL1_VAL_TCXO_EN	R/W	X	Assert reference valid for loopback mode after TCXO timeout counter
1	RESERVED	R	X	
0	DPLL1_TCXO_LOOPBACK_EN	R/W	X	Enable Loopback DPLL2 to DPLL1 TCXO Loop

2.297 R296 Register (Address = 128h) [reset = X]

R296 is shown in Figure 297 and described in Table 299.

Return to Summary Table.

Figure 297. R296 Register

7	6	5	4	3	2	1	0
RESERVED		DPLL1_REF_MAN_SEL	DPLL1_REF_MAN_REG_SEL			DPLL1_SWITCH_MODE	
R-X		R/W-X	R/W-X			R/W-X	

Table 299. R296 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	
5	DPLL1_REF_MAN_SEL	R/W	X	Controls source of manual selection 0h = Software register (DPLL1_REF_MAN_REG_SEL) 1h = Hardware pins (INSEL0_[1:0])
4-2	DPLL1_REF_MAN_REG_SEL	R/W	X	Controls software manual Ref selection 0h = Reference 0 1h = Reference 1 2h = Reference 2 3h = Reference 3 4h = Reserved 5h = Reference 5
1-0	DPLL1_SWITCH_MODE	R/W	X	Controls switchover mode 0h = Auto non-revertive 1h = Auto revertive 2h = Manual fallback 3h = Manual holdover

2.298 R297 Register (Address = 129h) [reset = X]

R297 is shown in Figure 298 and described in Table 300.

Return to Summary Table.

Figure 298. R297 Register

7	6	5	4	3	2	1	0
RESERVED	DPLL2_REF1_AUTO_PRTY			RESERVED	DPLL2_REF0_AUTO_PRTY		
R/W-X	R/W-X			R/W-X	R/W-X		

Table 300. R297 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	X	Reserved
6-4	DPLL2_REF1_AUTO_PRTY	R/W	X	Sets priorty for Ref1 See DPLL2_REF0_AUTO_PRTY bit settings.
3	RESERVED	R/W	X	Reserved
2-0	DPLL2_REF0_AUTO_PRTY	R/W	X	Sets priorty for Ref0 0h = Ignore 1h = 1 (Highest priority) 2h = 2 3h = 3 4h = 4 5h = 5 6h = 6 (Lowest priority)

2.299 R298 Register (Address = 12Ah) [reset = X]

R298 is shown in Figure 299 and described in Table 301.

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Figure 299. R298 Register

7	6	5	4	3	2	1	0
RESERVED	DPLL2_REF3_AUTO_PRTY			RESERVED	DPLL2_REF2_AUTO_PRTY		
R/W-X	R/W-X			R/W-X	R/W-X		

Table 301. R298 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	X	Reserved
6-4	DPLL2_REF3_AUTO_PRTY	R/W	X	Sets priorty for Ref3 See DPLL2_REF0_AUTO_PRTY bit settings.
3	RESERVED	R/W	X	Reserved
2-0	DPLL2_REF2_AUTO_PRTY	R/W	X	Sets priorty for Ref2 See DPLL2_REF0_AUTO_PRTY bit settings.

2.300 R299 Register (Address = 12Bh) [reset = X]

R299 is shown in Figure 300 and described in Table 302.

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Figure 300. R299 Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED			RESERVED	DPLL2_REF4_AUTO_PRTY		
R/W-X	R/W-X			R/W-X	R/W-X		

Table 302. R299 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	X	Reserved
6-4	RESERVED	R/W	X	Reserved
3	RESERVED	R/W	X	Reserved

Table 302. R299 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	DPLL2_REF4_AUTO_PRTY	R/W	X	Sets priorty for Ref4 See DPLL2_REF0_AUTO_PRTY bit settings.

2.301 R300 Register (Address = 12Ch) [reset = X]

R300 is shown in Figure 301 and described in Table 303.

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Figure 301. R300 Register

7	6	5	4	3	2	1	0
RESERVED			DPLL2_VAL_FL_EN	DPLL2_VAL_PL_EN	DPLL2_VAL_TCXO_EN	RESERVED	DPLL2_TCXO_LOOPBACK_EN
R-X			R/W-X	R/W-X	R/W-X	R-X	R/W-X

Table 303. R300 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	X	
4	DPLL2_VAL_FL_EN	R/W	X	Assert reference valid for loopback mode after immediately after frequency lock
3	DPLL2_VAL_PL_EN	R/W	X	Assert reference valid for loopback mode after either phase lock or timeout counter
2	DPLL2_VAL_TCXO_EN	R/W	X	Assert reference valid for loopback mode after TCXO timeout counter
1	RESERVED	R	X	
0	DPLL2_TCXO_LOOPBACK_EN	R/W	X	Loopback DPLL1 to DPLL2 TCXO loop

2.302 R301 Register (Address = 12Dh) [reset = X]

R301 is shown in Figure 302 and described in Table 304.

Return to Summary Table.

Figure 302. R301 Register

7	6	5	4	3	2	1	0
RESERVED		DPLL2_REF_MAN_SEL	DPLL2_REF_MAN_REG_SEL			DPLL2_SWITCH_MODE	
R-X		R/W-X	R/W-X			R/W-X	

Table 304. R301 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	
5	DPLL2_REF_MAN_SEL	R/W	X	Controls source of manual selection 0h = Software register (DPLL2_REF_MAN_REG_SEL) 1h = Hardware pins (INSEL1_[1:0])

Table 304. R301 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-2	DPLL2_REF_MAN_REG_SEL	R/W	X	Controls software manual Ref selection 0h = Reference 0 1h = Reference 1 2h = Reference 2 3h = Reference 3 4h = Reference 4
1-0	DPLL2_SWITCH_MODE	R/W	X	Controls switchover mode 0h = Auto non-revertive 1h = Auto revertive 2h = Manual fallback 3h = Manual holdover

2.303 R302 Register (Address = 12Eh) [reset = X]

R302 is shown in Figure 303 and described in Table 305.

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Figure 303. R302 Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED	DPLL1_SWITCHOVER_ALWAYS	DPLL1_FASTLOCK_ALWAYS	RESERVED	DPLL1_HLDOVR_MODE	DPLL1_LOOP_MODE	
R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	

Table 305. R302 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	X	Reserved
6	RESERVED	R/W	X	Reserved
5	DPLL1_SWITCHOVER_ALWAYS	R/W	X	DPLL1 switchover mode. If set to 1 and FASTLOCK_ALWAYS is 0, the switchover be hitless (minimal phase transient). If set to 0 and FASTLOCK_ALWAYS is 1, switchover is achieved using Fastlock and a phase hit will be propagated to the outputs during the switch. If set to 0 and FASTLOCK_ALWAYS is 0, the switchover will be hitless if the time spent in holdover is less than the switchover timer setting; otherwise, the switchover will be achieved using Fastlock.
4	DPLL1_FASTLOCK_ALWAYS	R/W	X	DPLL1 Fast Lock always enabled
3	RESERVED	R/W	X	Reserved
2	DPLL1_HLDOVR_MODE	R/W	X	DPLL1 Holdover mode control when tuning word history unavailable 0h = Enter free run mode (asserts user-defined DPLL1_TUNING_FREE_RUN word) 1h = Hold last control value prior to holdover
1-0	DPLL1_LOOP_MODE	R/W	X	DPLL1 Loop Mode control 0h = 1-loop (APLL free-run) 1h = 2-loop REF-DPLL 2h = 2-loop TCXO-DPLL 3h = 3-loop

2.304 R303 Register (Address = 12Fh) [reset = X]

R303 is shown in Figure 304 and described in Table 306.

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Figure 304. R303 Register

7	6	5	4	3	2	1	0
RESERVED			DPLL1_SWITCHOVER_TMR_EXP				
R-X			R/W-X				

Table 306. R303 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	X	
4-0	DPLL1_SWITCHOVER_TMR_EXP	R/W	X	DPLL1 Switchover Timer exponent

2.305 R304 Register (Address = 130h) [reset = X]

R304 is shown in Figure 305 and described in Table 307.

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Figure 305. R304 Register

7	6	5	4	3	2	1	0
RESERVED					DPLL1_SWITCHOVER_TMR_MANT[10:8]		
R-X					R/W-X		

Table 307. R304 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	X	
2-0	DPLL1_SWITCHOVER_TMR_MANT[10:8]	R/W	X	Bits 10:8 of DPLL1_SWITCHOVER_TMR_MANT

2.306 R305 Register (Address = 131h) [reset = X]

R305 is shown in Figure 306 and described in Table 308.

Return to Summary Table.

Figure 306. R305 Register

7	6	5	4	3	2	1	0
DPLL1_SWITCHOVER_TMR_MANT							
R/W-X							

Table 308. R305 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL1_SWITCHOVER_TMR_MANT	R/W	X	DPLL1 Switchover Timer mantissa

2.307 R306 Register (Address = 132h) [reset = X]

R306 is shown in Figure 307 and described in Table 309.

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Figure 307. R306 Register

7	6	5	4	3	2	1	0
DPLL1_REF0_RDIV[15:8]							
R/W-X							

Table 309. R306 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL1_REF0_RDIV[15:8]	R/W	X	Bits 15:8 of DPLL1_REF0_RDIV

2.308 R307 Register (Address = 133h) [reset = X]

R307 is shown in Figure 308 and described in Table 310.

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Figure 308. R307 Register

7	6	5	4	3	2	1	0
DPLL1_REF0_RDIV							
R/W-X							

Table 310. R307 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL1_REF0_RDIV	R/W	X	DPLL1 Ref0 divider

2.309 R308 Register (Address = 134h) [reset = X]

R308 is shown in Figure 309 and described in Table 311.

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Figure 309. R308 Register

7	6	5	4	3	2	1	0
DPLL1_REF1_RDIV[15:8]							
R/W-X							

Table 311. R308 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL1_REF1_RDIV[15:8]	R/W	X	Bits 15:8 of DPLL1_REF1_RDIV

2.310 R309 Register (Address = 135h) [reset = X]

R309 is shown in Figure 310 and described in Table 312.

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Figure 310. R309 Register

7	6	5	4	3	2	1	0
DPLL1_REF1_RDIV							
R/W-X							

Table 312. R309 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL1_REF1_RDIV	R/W	X	DPLL1 Ref1 divider

2.311 R310 Register (Address = 136h) [reset = X]

R310 is shown in Figure 311 and described in Table 313.

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Figure 311. R310 Register

7	6	5	4	3	2	1	0
DPLL1_REF2_RDIV[15:8]							
R/W-X							

Table 313. R310 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL1_REF2_RDIV[15:8]	R/W	X	Bits 15:8 of DPLL1_REF2_RDIV

2.312 R311 Register (Address = 137h) [reset = X]

R311 is shown in Figure 312 and described in Table 314.

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Figure 312. R311 Register

7	6	5	4	3	2	1	0
DPLL1_REF2_RDIV							
R/W-X							

Table 314. R311 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL1_REF2_RDIV	R/W	X	DPLL1 Ref2 divider

2.313 R312 Register (Address = 138h) [reset = X]

R312 is shown in Figure 313 and described in Table 315.

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Figure 313. R312 Register

7	6	5	4	3	2	1	0
DPLL1_REF3_RDIV[15:8]							
R/W-X							

Table 315. R312 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL1_REF3_RDIV[15:8]	R/W	X	Bits 15:8 of DPLL1_REF3_RDIV

2.314 R313 Register (Address = 139h) [reset = X]

R313 is shown in Figure 314 and described in Table 316.

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Figure 314. R313 Register

7	6	5	4	3	2	1	0
DPLL1_REF3_RDIV							
R/W-X							

Table 316. R313 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL1_REF3_RDIV	R/W	X	DPLL1 Ref3 divider

2.315 R314 Register (Address = 13Ah) [reset = X]

R314 is shown in Figure 315 and described in Table 317.

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Figure 315. R314 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 317. R314 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.316 R315 Register (Address = 13Bh) [reset = X]

R315 is shown in Figure 316 and described in Table 318.

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Figure 316. R315 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 318. R315 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.317 R316 Register (Address = 13Ch) [reset = X]

R316 is shown in Figure 317 and described in Table 319.

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Figure 317. R316 Register

7	6	5	4	3	2	1	0
DPLL1_REF5_RDIV[15:8]							
R/W-X							

Table 319. R316 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL1_REF5_RDIV[15:8]	R/W	X	Bits 15:8 of DPLL1_REF5_RDIV

2.318 R317 Register (Address = 13Dh) [reset = X]

R317 is shown in Figure 318 and described in Table 320.

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Figure 318. R317 Register

7	6	5	4	3	2	1	0
DPLL1_REF5_RDIV							
R/W-X							

Table 320. R317 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL1_REF5_RDIV	R/W	X	DPLL1 Ref5 divider

2.319 R318 Register (Address = 13Eh) [reset = X]

R318 is shown in Figure 319 and described in Table 321.

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Figure 319. R318 Register

7	6	5	4	3	2	1	0
RESERVED			RESERVED	OCXO_MDIV_DPLL1_TDC_SEL		RESERVED	RESERVED
R-X			R/W-X	R/W-X		R/W-X	R/W-X

Table 321. R318 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	X	
4	RESERVED	R/W	X	Reserved
3-2	OCXO_MDIV_DPLL1_TDC_SEL	R/W	X	DPLL1 TDC Selector. 0h = Disable 1h = TCXO 3h = VCO2 Loopback (FBCLK)
1	RESERVED	R/W	X	Reserved
0	RESERVED	R/W	X	Reserved

2.320 R319 Register (Address = 13Fh) [reset = X]

R319 is shown in Figure 320 and described in Table 322.

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Figure 320. R319 Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED		RESERVED	RESERVED			
R/W-X	R-X		R/W-X	R/W-X			

Table 322. R319 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	X	Reserved
6-5	RESERVED	R	X	
4	RESERVED	R/W	X	Reserved
3-0	RESERVED	R/W	X	Reserved

2.321 R320 Register (Address = 140h) [reset = X]

R320 is shown in Figure 321 and described in Table 323.

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Figure 321. R320 Register

7	6	5	4	3	2	1	0
RESERVED							RESERVED
R-X							R/W-X

Table 323. R320 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	X	
0	RESERVED	R/W	X	Reserved

2.322 R321 Register (Address = 141h) [reset = X]

R321 is shown in Figure 322 and described in Table 324.

Return to Summary Table.

Figure 322. R321 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 324. R321 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.323 R322 Register (Address = 142h) [reset = X]

R322 is shown in Figure 323 and described in Table 325.

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Figure 323. R322 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 325. R322 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.324 R323 Register (Address = 143h) [reset = X]

R323 is shown in Figure 324 and described in Table 326.

Return to Summary Table.

Figure 324. R323 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 326. R323 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.325 R324 Register (Address = 144h) [reset = X]

R324 is shown in Figure 325 and described in Table 327.

Return to Summary Table.

Figure 325. R324 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 327. R324 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.326 R325 Register (Address = 145h) [reset = X]

R325 is shown in Figure 326 and described in Table 328.

Return to Summary Table.

Figure 326. R325 Register

7	6	5	4	3	2	1	0
RESERVED				RESERVED	RESERVED		RESERVED
R/W-X				R/W-0h	R/W-X		R-X

Table 328. R325 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	X	Reserved
3	RESERVED	R/W	0h	Reserved
2-1	RESERVED	R/W	X	Reserved
0	RESERVED	R	X	

2.327 R326 Register (Address = 146h) [reset = X]

R326 is shown in Figure 327 and described in Table 329.

Return to Summary Table.

Figure 327. R326 Register

7	6	5	4	3	2	1	0
RESERVED				RESERVED	RESERVED	RESERVED	
R-X				R/W-X	R/W-X	R/W-X	

Table 329. R326 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	X	
3	RESERVED	R/W	X	Reserved
2	RESERVED	R/W	X	Reserved
1-0	RESERVED	R/W	X	Reserved

2.328 R327 Register (Address = 147h) [reset = X]

R327 is shown in Figure 328 and described in Table 330.

Return to Summary Table.

Figure 328. R327 Register

7	6	5	4	3	2	1	0
RESERVED				RESERVED			
R-X				R/W-X			

Table 330. R327 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	X	
4-0	RESERVED	R/W	X	Reserved

2.329 R328 Register (Address = 148h) [reset = X]

R328 is shown in Figure 329 and described in Table 331.

Return to Summary Table.

Figure 329. R328 Register

7	6	5	4	3	2	1	0
RESERVED						RESERVED	
R-X						R/W-X	

Table 331. R328 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	X	
1-0	RESERVED	R/W	X	Reserved

2.330 R329 Register (Address = 149h) [reset = X]

R329 is shown in Figure 330 and described in Table 332.

Return to Summary Table.

Figure 330. R329 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 332. R329 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.331 R330 Register (Address = 14Ah) [reset = X]

R330 is shown in Figure 331 and described in Table 333.

Return to Summary Table.

Figure 331. R330 Register

7	6	5	4	3	2	1	0
RESERVED		RESERVED					
R-X		R/W-X					

Table 333. R330 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	
5-0	RESERVED	R/W	X	Reserved

2.332 R331 Register (Address = 14Bh) [reset = X]

R331 is shown in Figure 332 and described in Table 334.

Return to Summary Table.

Figure 332. R331 Register

7	6	5	4	3	2	1	0
RESERVED		RESERVED					
R-X		R/W-X					

Table 334. R331 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	
5-0	RESERVED	R/W	X	Reserved

2.333 R332 Register (Address = 14Ch) [reset = X]

R332 is shown in Figure 333 and described in Table 335.

Return to Summary Table.

Figure 333. R332 Register

7	6	5	4	3	2	1	0
RESERVED		RESERVED					
R-X		R/W-X					

Table 335. R332 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	
5-0	RESERVED	R/W	X	Reserved

2.334 R333 Register (Address = 14Dh) [reset = X]

R333 is shown in Figure 334 and described in Table 336.

Return to Summary Table.

Figure 334. R333 Register

7	6	5	4	3	2	1	0
RESERVED				RESERVED			
R-X				R/W-X			

Table 336. R333 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	X	
4-0	RESERVED	R/W	X	Reserved

2.335 R334 Register (Address = 14Eh) [reset = X]

R334 is shown in Figure 335 and described in Table 337.

Return to Summary Table.

Figure 335. R334 Register

7	6	5	4	3	2	1	0
RESERVED				RESERVED			
R-X				R/W-X			

Table 337. R334 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	X	
4-0	RESERVED	R/W	X	Reserved

2.336 R335 Register (Address = 14Fh) [reset = X]

R335 is shown in Figure 336 and described in Table 338.

Return to Summary Table.

Figure 336. R335 Register

7	6	5	4	3	2	1	0
RESERVED				RESERVED			
R-X				R/W-X			

Table 338. R335 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	X	
4-0	RESERVED	R/W	X	Reserved

2.337 R336 Register (Address = 150h) [reset = X]

R336 is shown in Figure 337 and described in Table 339.

Return to Summary Table.

Figure 337. R336 Register

7	6	5	4	3	2	1	0
RESERVED			RESERVED				
R-X			R/W-X				

Table 339. R336 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	X	
4-0	RESERVED	R/W	X	Reserved

2.338 R337 Register (Address = 151h) [reset = X]

R337 is shown in Figure 338 and described in Table 340.

Return to Summary Table.

Figure 338. R337 Register

7	6	5	4	3	2	1	0
RESERVED			RESERVED				
R-X			R/W-X				

Table 340. R337 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	X	
4-0	RESERVED	R/W	X	Reserved

2.339 R338 Register (Address = 152h) [reset = X]

R338 is shown in Figure 339 and described in Table 341.

Return to Summary Table.

Figure 339. R338 Register

7	6	5	4	3	2	1	0
RESERVED			RESERVED				
R-X			R/W-X				

Table 341. R338 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	X	
4-0	RESERVED	R/W	X	Reserved

2.340 R339 Register (Address = 153h) [reset = X]

R339 is shown in Figure 340 and described in Table 342.

Return to Summary Table.

Figure 340. R339 Register

7	6	5	4	3	2	1	0
RESERVED			RESERVED				
R-X			R/W-X				

Table 342. R339 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	X	
4-0	RESERVED	R/W	X	Reserved

2.341 R340 Register (Address = 154h) [reset = X]

R340 is shown in Figure 341 and described in Table 343.

Return to Summary Table.

Figure 341. R340 Register

7	6	5	4	3	2	1	0
RESERVED			RESERVED				
R-X			R/W-X				

Table 343. R340 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	X	
4-0	RESERVED	R/W	X	Reserved

2.342 R341 Register (Address = 155h) [reset = X]

R341 is shown in Figure 342 and described in Table 344.

Return to Summary Table.

Figure 342. R341 Register

7	6	5	4	3	2	1	0
RESERVED			RESERVED				
R-X			R/W-X				

Table 344. R341 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	X	
4-0	RESERVED	R/W	X	Reserved

2.343 R342 Register (Address = 156h) [reset = X]

R342 is shown in Figure 343 and described in Table 345.

Return to Summary Table.

Figure 343. R342 Register

7	6	5	4	3	2	1	0
RESERVED			RESERVED				
R-X			R/W-X				

Table 345. R342 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	X	
4-0	RESERVED	R/W	X	Reserved

2.344 R343 Register (Address = 157h) [reset = X]

R343 is shown in Figure 344 and described in Table 346.

Return to Summary Table.

Figure 344. R343 Register

7	6	5	4	3	2	1	0
RESERVED			RESERVED				
R-X			R/W-X				

Table 346. R343 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	X	
4-0	RESERVED	R/W	X	Reserved

2.345 R344 Register (Address = 158h) [reset = X]

R344 is shown in Figure 345 and described in Table 347.

Return to Summary Table.

Figure 345. R344 Register

7	6	5	4	3	2	1	0
RESERVED						RESERVED	
R-X						R/W-X	

Table 347. R344 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	X	
1-0	RESERVED	R/W	X	Reserved

2.346 R345 Register (Address = 159h) [reset = X]

R345 is shown in Figure 346 and described in Table 348.

Return to Summary Table.

Figure 346. R345 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 348. R345 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.347 R346 Register (Address = 15Ah) [reset = X]

R346 is shown in Figure 347 and described in Table 349.

Return to Summary Table.

Figure 347. R346 Register

7	6	5	4	3	2	1	0
RESERVED						RESERVED	
R-X						R/W-X	

Table 349. R346 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	X	
1-0	RESERVED	R/W	X	Reserved

2.348 R347 Register (Address = 15Bh) [reset = X]

R347 is shown in Figure 348 and described in Table 350.

Return to Summary Table.

Figure 348. R347 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 350. R347 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.349 R348 Register (Address = 15Ch) [reset = X]

R348 is shown in Figure 349 and described in Table 351.

Return to Summary Table.

Figure 349. R348 Register

7	6	5	4	3	2	1	0
RESERVED						RESERVED	
R-X						R/W-X	

Table 351. R348 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	X	
1-0	RESERVED	R/W	X	Reserved

2.350 R349 Register (Address = 15Dh) [reset = X]

R349 is shown in Figure 350 and described in Table 352.

Return to Summary Table.

Figure 350. R349 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 352. R349 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.351 R350 Register (Address = 15Eh) [reset = X]

R350 is shown in Figure 351 and described in Table 353.

Return to Summary Table.

Figure 351. R350 Register

7	6	5	4	3	2	1	0
RESERVED				RESERVED			
R-X				R/W-X			

Table 353. R350 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	X	
3-0	RESERVED	R/W	X	Reserved

2.352 R351 Register (Address = 15Fh) [reset = X]

R351 is shown in Figure 352 and described in Table 354.

Return to Summary Table.

Figure 352. R351 Register

7	6	5	4	3	2	1	0
RESERVED						RESERVED	RESERVED
R-X						R/W-X	R/W-X

Table 354. R351 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	X	
1	RESERVED	R/W	X	Reserved
0	RESERVED	R/W	X	Reserved

2.353 R352 Register (Address = 160h) [reset = X]

R352 is shown in Figure 353 and described in Table 355.

Return to Summary Table.

Figure 353. R352 Register

7	6	5	4	3	2	1	0
RESERVED						RESERVED	
R-X						R/W-X	

Table 355. R352 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	X	
1-0	RESERVED	R/W	X	Reserved

2.354 R353 Register (Address = 161h) [reset = X]

R353 is shown in Figure 354 and described in Table 356.

Return to Summary Table.

Figure 354. R353 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 356. R353 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.355 R354 Register (Address = 162h) [reset = X]

R354 is shown in Figure 355 and described in Table 357.

Return to Summary Table.

Figure 355. R354 Register

7	6	5	4	3	2	1	0
RESERVED		RESERVED					
R-X		R/W-X					

Table 357. R354 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	
5-0	RESERVED	R/W	X	Reserved

2.356 R355 Register (Address = 163h) [reset = X]

R355 is shown in Figure 356 and described in Table 358.

Return to Summary Table.

Figure 356. R355 Register

7	6	5	4	3	2	1	0
RESERVED		RESERVED					
R-X		R/W-X					

Table 358. R355 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	
5-0	RESERVED	R/W	X	Reserved

2.357 R356 Register (Address = 164h) [reset = X]

R356 is shown in Figure 357 and described in Table 359.

Return to Summary Table.

Figure 357. R356 Register

7	6	5	4	3	2	1	0
RESERVED		RESERVED					
R-X		R/W-X					

Table 359. R356 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	
5-0	RESERVED	R/W	X	Reserved

2.358 R357 Register (Address = 165h) [reset = X]

R357 is shown in Figure 358 and described in Table 360.

Return to Summary Table.

Figure 358. R357 Register

7	6	5	4	3	2	1	0
RESERVED						RESERVED	
R-X						R/W-X	

Table 360. R357 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	X	
1-0	RESERVED	R/W	X	Reserved

2.359 R358 Register (Address = 166h) [reset = X]

R358 is shown in Figure 359 and described in Table 361.

Return to Summary Table.

Figure 359. R358 Register

7	6	5	4	3	2	1	0
RESERVED			RESERVED				
R-X			R/W-X				

Table 361. R358 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	X	
4-0	RESERVED	R/W	X	Reserved

2.360 R359 Register (Address = 167h) [reset = X]

R359 is shown in Figure 360 and described in Table 362.

Return to Summary Table.

Figure 360. R359 Register

7	6	5	4	3	2	1	0
RESERVED		RESERVED					
R-X		R/W-X					

Table 362. R359 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	
5-0	RESERVED	R/W	X	Reserved

2.361 R360 Register (Address = 168h) [reset = X]

R360 is shown in Figure 361 and described in Table 363.

Return to Summary Table.

Figure 361. R360 Register

7	6	5	4	3	2	1	0
RESERVED		RESERVED					
R-X		R/W-X					

Table 363. R360 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	
5-0	RESERVED	R/W	X	Reserved

2.362 R361 Register (Address = 169h) [reset = X]

R361 is shown in Figure 362 and described in Table 364.

Return to Summary Table.

Figure 362. R361 Register

7	6	5	4	3	2	1	0
DPLL1_CLK_FB_DIV_EN	RESERVED		DPLL1_CLK_FB_DIV				
R/W-X	R-X		R/W-X				

Table 364. R361 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	DPLL1_CLK_FB_DIV_EN	R/W	X	DPLL1 CLK Feedback Divider enable
6-5	RESERVED	R	X	
4-0	DPLL1_CLK_FB_DIV	R/W	X	DPLL1 CLK Feedback Divider value

2.363 R362 Register (Address = 16Ah) [reset = X]

R362 is shown in Figure 363 and described in Table 365.

Return to Summary Table.

Figure 363. R362 Register

7	6	5	4	3	2	1	0
RESERVED				DPLL1_REF_FB_PRE_DIV			
R-X				R/W-X			

Table 365. R362 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	X	
3-0	DPLL1_REF_FB_PRE_DIV	R/W	X	DPLL1 REF Feedback Pre Divider value 0h = 2 1h = 3 Fh = 17

2.364 R363 Register (Address = 16Bh) [reset = X]

R363 is shown in Figure 364 and described in Table 366.

Return to Summary Table.

Figure 364. R363 Register

7	6	5	4	3	2	1	0
RESERVED			DPLL1_REF_FB_DIV[29:24]				
R-X			R/W-X				

Table 366. R363 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	
5-0	DPLL1_REF_FB_DIV[29:24]	R/W	X	Bits 29:24 of DPLL1_REF_FB_DIV

2.365 R364 Register (Address = 16Ch) [reset = X]

R364 is shown in Figure 365 and described in Table 367.

Return to Summary Table.

Figure 365. R364 Register

7	6	5	4	3	2	1	0
DPLL1_REF_FB_DIV[23:16]							
R/W-X							

Table 367. R364 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL1_REF_FB_DIV[23:16]	R/W	X	Bits 23:16 of DPLL1_REF_FB_DIV

2.366 R365 Register (Address = 16Dh) [reset = X]

R365 is shown in Figure 366 and described in Table 368.

Return to Summary Table.

Figure 366. R365 Register

7	6	5	4	3	2	1	0
DPLL1_REF_FB_DIV[15:8]							
R/W-X							

Table 368. R365 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL1_REF_FB_DIV[15:8]	R/W	X	Bits 15:8 of DPLL1_REF_FB_DIV

2.367 R366 Register (Address = 16Eh) [reset = X]

R366 is shown in Figure 367 and described in Table 369.

Return to Summary Table.

Figure 367. R366 Register

7	6	5	4	3	2	1	0
DPLL1_REF_FB_DIV							
R/W-X							

Table 369. R366 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL1_REF_FB_DIV	R/W	X	DPLL1 REF Feedback Divider value

2.368 R367 Register (Address = 16Fh) [reset = X]

R367 is shown in Figure 368 and described in Table 370.

Return to Summary Table.

Figure 368. R367 Register

7	6	5	4	3	2	1	0
DPLL1_REF_NUM[39:32]							
R/W-X							

Table 370. R367 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL1_REF_NUM[39:32]	R/W	X	Bits 39:32 of DPLL1_REF_NUM

2.369 R368 Register (Address = 170h) [reset = X]

R368 is shown in Figure 369 and described in Table 371.

Return to Summary Table.

Figure 369. R368 Register

7	6	5	4	3	2	1	0
DPLL1_REF_NUM[31:24]							
R/W-X							

Table 371. R368 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL1_REF_NUM[31:24]	R/W	X	Bits 31:24 of DPLL1_REF_NUM

2.370 R369 Register (Address = 171h) [reset = X]

R369 is shown in Figure 370 and described in Table 372.

Return to Summary Table.

Figure 370. R369 Register

7	6	5	4	3	2	1	0
DPLL1_REF_NUM[23:16]							
R/W-X							

Table 372. R369 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL1_REF_NUM[23:16]	R/W	X	Bits 23:16 of DPLL1_REF_NUM

2.371 R370 Register (Address = 172h) [reset = X]

R370 is shown in Figure 371 and described in Table 373.

Return to Summary Table.

Figure 371. R370 Register

7	6	5	4	3	2	1	0
DPLL1_REF_NUM[15:8]							
R/W-X							

Table 373. R370 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL1_REF_NUM[15:8]	R/W	X	Bits 15:8 of DPLL1_REF_NUM

2.372 R371 Register (Address = 173h) [reset = X]

R371 is shown in Figure 372 and described in Table 374.

Return to Summary Table.

Figure 372. R371 Register

7	6	5	4	3	2	1	0
DPLL1_REF_NUM							
R/W-X							

Table 374. R371 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL1_REF_NUM	R/W	X	DPLL1 REF FB Divider Numerator

2.373 R372 Register (Address = 174h) [reset = X]

R372 is shown in Figure 373 and described in Table 375.

Return to Summary Table.

Figure 373. R372 Register

7	6	5	4	3	2	1	0
DPLL1_REF_DEN[39:32]							
R/W-X							

Table 375. R372 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL1_REF_DEN[39:32]	R/W	X	Bits 39:32 of DPLL1_REF_DEN

2.374 R373 Register (Address = 175h) [reset = X]

R373 is shown in Figure 374 and described in Table 376.

Return to Summary Table.

Figure 374. R373 Register

7	6	5	4	3	2	1	0
DPLL1_REF_DEN[31:24]							
R/W-X							

Table 376. R373 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL1_REF_DEN[31:24]	R/W	X	Bits 31:24 of DPLL1_REF_DEN

2.375 R374 Register (Address = 176h) [reset = X]

R374 is shown in Figure 375 and described in Table 377.

Return to Summary Table.

Figure 375. R374 Register

7	6	5	4	3	2	1	0
DPLL1_REF_DEN[23:16]							
R/W-X							

Table 377. R374 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL1_REF_DEN[23:16]	R/W	X	Bits 23:16 of DPLL1_REF_DEN

2.376 R375 Register (Address = 177h) [reset = X]

R375 is shown in Figure 376 and described in Table 378.

Return to Summary Table.

Figure 376. R375 Register

7	6	5	4	3	2	1	0
DPLL1_REF_DEN[15:8]							
R/W-X							

Table 378. R375 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL1_REF_DEN[15:8]	R/W	X	Bits 15:8 of DPLL1_REF_DEN

2.377 R376 Register (Address = 178h) [reset = X]

R376 is shown in Figure 377 and described in Table 379.

Return to Summary Table.

Figure 377. R376 Register

7	6	5	4	3	2	1	0
DPLL1_REF_DEN							
R/W-X							

Table 379. R376 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL1_REF_DEN	R/W	X	DPLL1 REF FB Divider denominator

2.378 R377 Register (Address = 179h) [reset = X]

R377 is shown in Figure 378 and described in Table 380.

Return to Summary Table.

Figure 378. R377 Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED		RESERVED		DPLL1_REF_ORDER		
R-X	R/W-X		R/W-X		R/W-X		

Table 380. R377 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	X	
6-5	RESERVED	R/W	X	Reserved
4-3	RESERVED	R/W	X	Reserved
2-0	DPLL1_REF_ORDER	R/W	X	DPLL1 REF SDM order

2.379 R378 Register (Address = 17Ah) [reset = X]

R378 is shown in Figure 379 and described in Table 381.

Return to Summary Table.

Figure 379. R378 Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED						
R-X	R/W-X						

Table 381. R378 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	X	
6-0	RESERVED	R/W	X	Reserved

2.380 R379 Register (Address = 17Bh) [reset = X]

R379 is shown in Figure 380 and described in Table 382.

Return to Summary Table.

Figure 380. R379 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 382. R379 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.381 R380 Register (Address = 17Ch) [reset = X]

R380 is shown in Figure 381 and described in Table 383.

Return to Summary Table.

Figure 381. R380 Register

7	6	5	4	3	2	1	0
RESERVED		RESERVED					
R-X		R/W-X					

Table 383. R380 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	
5-0	RESERVED	R/W	X	Reserved

2.382 R381 Register (Address = 17Dh) [reset = X]

R381 is shown in Figure 382 and described in Table 384.

Return to Summary Table.

Figure 382. R381 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 384. R381 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.383 R382 Register (Address = 17Eh) [reset = X]

R382 is shown in Figure 383 and described in Table 385.

Return to Summary Table.

Figure 383. R382 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 385. R382 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.384 R383 Register (Address = 17Fh) [reset = X]

R383 is shown in Figure 384 and described in Table 386.

Return to Summary Table.

Figure 384. R383 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 386. R383 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.385 R384 Register (Address = 180h) [reset = X]

R384 is shown in Figure 385 and described in Table 387.

Return to Summary Table.

Figure 385. R384 Register

7	6	5	4	3	2	1	0
RESERVED		RESERVED					
R-X		R/W-X					

Table 387. R384 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	
5-0	RESERVED	R/W	X	Reserved

2.386 R385 Register (Address = 181h) [reset = X]

R385 is shown in Figure 386 and described in Table 388.

Return to Summary Table.

Figure 386. R385 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 388. R385 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.387 R386 Register (Address = 182h) [reset = X]

R386 is shown in Figure 387 and described in Table 389.

Return to Summary Table.

Figure 387. R386 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 389. R386 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.388 R387 Register (Address = 183h) [reset = X]

R387 is shown in Figure 388 and described in Table 390.

Return to Summary Table.

Figure 388. R387 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 390. R387 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.389 R388 Register (Address = 184h) [reset = X]

R388 is shown in Figure 389 and described in Table 391.

Return to Summary Table.

Figure 389. R388 Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED						
R-X	R/W-X						

Table 391. R388 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	X	
6-0	RESERVED	R/W	X	Reserved

2.390 R389 Register (Address = 185h) [reset = X]

R389 is shown in Figure 390 and described in Table 392.

Return to Summary Table.

Figure 390. R389 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 392. R389 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.391 R390 Register (Address = 186h) [reset = X]

R390 is shown in Figure 391 and described in Table 393.

Return to Summary Table.

Figure 391. R390 Register

7	6	5	4	3	2	1	0
RESERVED		RESERVED					
R-X		R/W-X					

Table 393. R390 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	
5-0	RESERVED	R/W	X	Reserved

2.392 R391 Register (Address = 187h) [reset = X]

R391 is shown in Figure 392 and described in Table 394.

Return to Summary Table.

Figure 392. R391 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 394. R391 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.393 R392 Register (Address = 188h) [reset = X]

R392 is shown in Figure 393 and described in Table 395.

Return to Summary Table.

Figure 393. R392 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 395. R392 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.394 R393 Register (Address = 189h) [reset = X]

R393 is shown in Figure 394 and described in Table 396.

Return to Summary Table.

Figure 394. R393 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 396. R393 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.395 R394 Register (Address = 18Ah) [reset = X]

R394 is shown in Figure 395 and described in Table 397.

Return to Summary Table.

Figure 395. R394 Register

7	6	5	4	3	2	1	0
RESERVED		RESERVED					
R-X		R/W-X					

Table 397. R394 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	
5-0	RESERVED	R/W	X	Reserved

2.396 R395 Register (Address = 18Bh) [reset = X]

R395 is shown in Figure 396 and described in Table 398.

Return to Summary Table.

Figure 396. R395 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 398. R395 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.397 R396 Register (Address = 18Ch) [reset = X]

R396 is shown in Figure 397 and described in Table 399.

Return to Summary Table.

Figure 397. R396 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 399. R396 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.398 R397 Register (Address = 18Dh) [reset = X]

R397 is shown in Figure 398 and described in Table 400.

Return to Summary Table.

Figure 398. R397 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 400. R397 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.399 R398 Register (Address = 18Eh) [reset = X]

R398 is shown in Figure 399 and described in Table 401.

Return to Summary Table.

Figure 399. R398 Register

7	6	5	4	3	2	1	0
RESERVED			DPLL1_REF_SYNC_PH_OFFSET[44:40]				
R-X			R/W-X				

Table 401. R398 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	X	
4-0	DPLL1_REF_SYNC_PH_OFFSET[44:40]	R/W	X	Bits 44:40 of DPLL1_REF_SYNC_PH_OFFSET

2.400 R399 Register (Address = 18Fh) [reset = X]

R399 is shown in Figure 400 and described in Table 402.

Return to Summary Table.

Figure 400. R399 Register

7	6	5	4	3	2	1	0
DPLL1_REF_SYNC_PH_OFFSET[39:32]							
R/W-X							

Table 402. R399 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL1_REF_SYNC_PH_OFFSET[39:32]	R/W	X	Bits 39:32 of DPLL1_REF_SYNC_PH_OFFSET

2.401 R400 Register (Address = 190h) [reset = X]

R400 is shown in Figure 401 and described in Table 403.

Return to Summary Table.

Figure 401. R400 Register

7	6	5	4	3	2	1	0
DPLL1_REF_SYNC_PH_OFFSET[31:24]							
R/W-X							

Table 403. R400 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL1_REF_SYNC_PH_OFFSET[31:24]	R/W	X	Bits 31:24 of DPLL1_REF_SYNC_PH_OFFSET

2.402 R401 Register (Address = 191h) [reset = X]

R401 is shown in Figure 402 and described in Table 404.

Return to Summary Table.

Figure 402. R401 Register

7	6	5	4	3	2	1	0
DPLL1_REF_SYNC_PH_OFFSET[23:16]							
R/W-X							

Table 404. R401 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL1_REF_SYNC_PH_OFFSET[23:16]	R/W	X	Bits 23:16 of DPLL1_REF_SYNC_PH_OFFSET

2.403 R402 Register (Address = 192h) [reset = X]

R402 is shown in Figure 403 and described in Table 405.

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Figure 403. R402 Register

7	6	5	4	3	2	1	0
DPLL1_REF_SYNC_PH_OFFSET[15:8]							
R/W-X							

Table 405. R402 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL1_REF_SYNC_PH_OFFSET[15:8]	R/W	X	Bits 15:8 of DPLL1_REF_SYNC_PH_OFFSET

2.404 R403 Register (Address = 193h) [reset = X]

R403 is shown in Figure 404 and described in Table 406.

Return to Summary Table.

Figure 404. R403 Register

7	6	5	4	3	2	1	0
DPLL1_REF_SYNC_PH_OFFSET							
R/W-X							

Table 406. R403 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL1_REF_SYNC_PH_OFFSET	R/W	X	DPLL1 REF Zero Delay Mode Phase Offset

2.405 R404 Register (Address = 194h) [reset = X]

R404 is shown in Figure 405 and described in Table 407.

Return to Summary Table.

Figure 405. R404 Register

7	6	5	4	3	2	1	0
RESERVED						RESERVED	RESERVED
R-X						R/W-X	R/W-X

Table 407. R404 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	X	
1	RESERVED	R/W	X	Reserved
0	RESERVED	R/W	X	Reserved

2.406 R405 Register (Address = 195h) [reset = X]

R405 is shown in Figure 406 and described in Table 408.

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Figure 406. R405 Register

7	6	5	4	3	2	1	0
RESERVED		RESERVED					
R-X		R/W-X					

Table 408. R405 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	
5-0	RESERVED	R/W	X	Reserved

2.407 R406 Register (Address = 196h) [reset = X]

R406 is shown in Figure 407 and described in Table 409.

Return to Summary Table.

Figure 407. R406 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 409. R406 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.408 R407 Register (Address = 197h) [reset = X]

R407 is shown in Figure 408 and described in Table 410.

Return to Summary Table.

Figure 408. R407 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 410. R407 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.409 R408 Register (Address = 198h) [reset = X]

R408 is shown in Figure 409 and described in Table 411.

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Figure 409. R408 Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED		RESERVED	RESERVED			
R/W-X	R-X		R/W-X	R/W-X			

Table 411. R408 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	X	Reserved
6-5	RESERVED	R	X	
4	RESERVED	R/W	X	Reserved
3-0	RESERVED	R/W	X	Reserved

2.410 R409 Register (Address = 199h) [reset = X]

R409 is shown in Figure 410 and described in Table 412.

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Figure 410. R409 Register

7	6	5	4	3	2	1	0
RESERVED				RESERVED	RESERVED		
R/W-X				R/W-0h	R-X		

Table 412. R409 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	X	Reserved
3	RESERVED	R/W	0h	Reserved
2-0	RESERVED	R	X	

2.411 R410 Register (Address = 19Ah) [reset = X]

R410 is shown in Figure 411 and described in Table 413.

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Figure 411. R410 Register

7	6	5	4	3	2	1	0
RESERVED			RESERVED				
R-X			R/W-X				

Table 413. R410 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	X	
4-0	RESERVED	R/W	X	Reserved

2.412 R411 Register (Address = 19Bh) [reset = X]

R411 is shown in Figure 412 and described in Table 414.

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Figure 412. R411 Register

7	6	5	4	3	2	1	0
RESERVED						RESERVED	
R-X						R/W-X	

Table 414. R411 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	X	
1-0	RESERVED	R/W	X	Reserved

2.413 R412 Register (Address = 19Ch) [reset = X]

R412 is shown in Figure 413 and described in Table 415.

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Figure 413. R412 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 415. R412 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.414 R413 Register (Address = 19Dh) [reset = X]

R413 is shown in Figure 414 and described in Table 416.

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Figure 414. R413 Register

7	6	5	4	3	2	1	0
RESERVED				RESERVED			
R-X				R/W-X			

Table 416. R413 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	X	
4-0	RESERVED	R/W	X	Reserved

2.415 R414 Register (Address = 19Eh) [reset = X]

R414 is shown in Figure 415 and described in Table 417.

Return to Summary Table.

Figure 415. R414 Register

7	6	5	4	3	2	1	0
RESERVED				RESERVED			
R-X				R/W-X			

Table 417. R414 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	X	
4-0	RESERVED	R/W	X	Reserved

2.416 R415 Register (Address = 19Fh) [reset = X]

R415 is shown in Figure 416 and described in Table 418.

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Figure 416. R415 Register

7	6	5	4	3	2	1	0
RESERVED				RESERVED			
R-X				R/W-X			

Table 418. R415 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	X	
4-0	RESERVED	R/W	X	Reserved

2.417 R416 Register (Address = 1A0h) [reset = X]

R416 is shown in Figure 417 and described in Table 419.

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Figure 417. R416 Register

7	6	5	4	3	2	1	0
RESERVED			RESERVED				
R-X			R/W-X				

Table 419. R416 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	X	
4-0	RESERVED	R/W	X	Reserved

2.418 R417 Register (Address = 1A1h) [reset = X]

R417 is shown in Figure 418 and described in Table 420.

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Figure 418. R417 Register

7	6	5	4	3	2	1	0
RESERVED			RESERVED				
R-X			R/W-X				

Table 420. R417 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	X	
4-0	RESERVED	R/W	X	Reserved

2.419 R418 Register (Address = 1A2h) [reset = X]

R418 is shown in Figure 419 and described in Table 421.

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Figure 419. R418 Register

7	6	5	4	3	2	1	0
RESERVED			RESERVED				
R-X			R/W-X				

Table 421. R418 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	X	
4-0	RESERVED	R/W	X	Reserved

2.420 R419 Register (Address = 1A3h) [reset = X]

R419 is shown in Figure 420 and described in Table 422.

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Figure 420. R419 Register

7	6	5	4	3	2	1	0
RESERVED			RESERVED				
R-X			R/W-X				

Table 422. R419 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	X	
4-0	RESERVED	R/W	X	Reserved

2.421 R420 Register (Address = 1A4h) [reset = X]

R420 is shown in Figure 421 and described in Table 423.

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Figure 421. R420 Register

7	6	5	4	3	2	1	0
RESERVED			RESERVED				
R-X			R/W-X				

Table 423. R420 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	X	
4-0	RESERVED	R/W	X	Reserved

2.422 R421 Register (Address = 1A5h) [reset = X]

R421 is shown in Figure 422 and described in Table 424.

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Figure 422. R421 Register

7	6	5	4	3	2	1	0
RESERVED			RESERVED				
R-X			R/W-X				

Table 424. R421 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	X	
4-0	RESERVED	R/W	X	Reserved

2.423 R422 Register (Address = 1A6h) [reset = X]

R422 is shown in Figure 423 and described in Table 425.

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Figure 423. R422 Register

7	6	5	4	3	2	1	0
RESERVED				RESERVED			
R-X				R/W-X			

Table 425. R422 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	X	
4-0	RESERVED	R/W	X	Reserved

2.424 R423 Register (Address = 1A7h) [reset = X]

R423 is shown in Figure 424 and described in Table 426.

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Figure 424. R423 Register

7	6	5	4	3	2	1	0
RESERVED						RESERVED	
R-X						R/W-X	

Table 426. R423 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	X	
1-0	RESERVED	R/W	X	Reserved

2.425 R424 Register (Address = 1A8h) [reset = X]

R424 is shown in Figure 425 and described in Table 427.

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Figure 425. R424 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 427. R424 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.426 R425 Register (Address = 1A9h) [reset = X]

R425 is shown in Figure 426 and described in Table 428.

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Figure 426. R425 Register

7	6	5	4	3	2	1	0
RESERVED						RESERVED	
R-X						R/W-X	

Table 428. R425 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	X	
1-0	RESERVED	R/W	X	Reserved

2.427 R426 Register (Address = 1AAh) [reset = X]

R426 is shown in Figure 427 and described in Table 429.

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Figure 427. R426 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 429. R426 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.428 R427 Register (Address = 1ABh) [reset = X]

R427 is shown in Figure 428 and described in Table 430.

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Figure 428. R427 Register

7	6	5	4	3	2	1	0
RESERVED		RESERVED					
R-X		R/W-X					

Table 430. R427 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	
5-0	RESERVED	R/W	X	Reserved

2.429 R428 Register (Address = 1ACh) [reset = X]

R428 is shown in Figure 429 and described in Table 431.

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Figure 429. R428 Register

7	6	5	4	3	2	1	0
RESERVED		RESERVED					
R-X		R/W-X					

Table 431. R428 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	
5-0	RESERVED	R/W	X	Reserved

2.430 R429 Register (Address = 1ADh) [reset = X]

R429 is shown in Figure 430 and described in Table 432.

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Figure 430. R429 Register

7	6	5	4	3	2	1	0
RESERVED						RESERVED	
R-X						R/W-X	

Table 432. R429 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	X	
1-0	RESERVED	R/W	X	Reserved

2.431 R430 Register (Address = 1AEh) [reset = X]

R430 is shown in Figure 431 and described in Table 433.

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Figure 431. R430 Register

7	6	5	4	3	2	1	0
RESERVED				DPLL1_TCXO_FB_PRE_DIV			
R-X				R/W-X			

Table 433. R430 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	X	
3-0	DPLL1_TCXO_FB_PRE_DIV	R/W	X	DPLL1 TCXO Feedback Pre Divider value 0h = 2 1h = 3 Fh = 17

2.432 R431 Register (Address = 1AFh) [reset = X]

R431 is shown in Figure 432 and described in Table 434.

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Figure 432. R431 Register

7	6	5	4	3	2	1	0
RESERVED				DPLL1_TCXO_FB_DIV[29:24]			
R-X				R/W-X			

Table 434. R431 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	
5-0	DPLL1_TCXO_FB_DIV[29:24]	R/W	X	Bits 29:24 of DPLL1_TCXO_FB_DIV

2.433 R432 Register (Address = 1B0h) [reset = X]

R432 is shown in Figure 433 and described in Table 435.

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Figure 433. R432 Register

7	6	5	4	3	2	1	0
DPLL1_TCXO_FB_DIV[23:16]							
R/W-X							

Table 435. R432 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL1_TCXO_FB_DIV[23:16]	R/W	X	Bits 23:16 of DPLL1_TCXO_FB_DIV

2.434 R433 Register (Address = 1B1h) [reset = X]

R433 is shown in Figure 434 and described in Table 436.

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Figure 434. R433 Register

7	6	5	4	3	2	1	0
DPLL1_TCXO_FB_DIV[15:8]							
R/W-X							

Table 436. R433 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL1_TCXO_FB_DIV[15:8]	R/W	X	Bits 15:8 of DPLL1_TCXO_FB_DIV

2.435 R434 Register (Address = 1B2h) [reset = X]

R434 is shown in Figure 435 and described in Table 437.

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Figure 435. R434 Register

7	6	5	4	3	2	1	0
DPLL1_TCXO_FB_DIV							
R/W-X							

Table 437. R434 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL1_TCXO_FB_DIV	R/W	X	DPLL1 TCXO Feedback Divider value

2.436 R435 Register (Address = 1B3h) [reset = X]

R435 is shown in Figure 436 and described in Table 438.

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Figure 436. R435 Register

7	6	5	4	3	2	1	0
DPLL1_TCXO_NUM[39:32]							
R/W-X							

Table 438. R435 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL1_TCXO_NUM[39:32]	R/W	X	Bits 39:32 of DPLL1_TCXO_NUM

2.437 R436 Register (Address = 1B4h) [reset = X]

R436 is shown in Figure 437 and described in Table 439.

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Figure 437. R436 Register

7	6	5	4	3	2	1	0
DPLL1_TCXO_NUM[31:24]							
R/W-X							

Table 439. R436 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL1_TCXO_NUM[31:24]	R/W	X	Bits 31:24 of DPLL1_TCXO_NUM

2.438 R437 Register (Address = 1B5h) [reset = X]

R437 is shown in Figure 438 and described in Table 440.

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Figure 438. R437 Register

7	6	5	4	3	2	1	0
DPLL1_TCXO_NUM[23:16]							
R/W-X							

Table 440. R437 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL1_TCXO_NUM[23:16]	R/W	X	Bits 23:16 of DPLL1_TCXO_NUM

2.439 R438 Register (Address = 1B6h) [reset = X]

R438 is shown in Figure 439 and described in Table 441.

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Figure 439. R438 Register

7	6	5	4	3	2	1	0
DPLL1_TCXO_NUM[15:8]							
R/W-X							

Table 441. R438 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL1_TCXO_NUM[15:8]	R/W	X	Bits 15:8 of DPLL1_TCXO_NUM

2.440 R439 Register (Address = 1B7h) [reset = X]

R439 is shown in Figure 440 and described in Table 442.

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Figure 440. R439 Register

7	6	5	4	3	2	1	0
DPLL1_TCXO_NUM							
R/W-X							

Table 442. R439 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL1_TCXO_NUM	R/W	X	DPLL1 TCXO FB Divider Numerator

2.441 R440 Register (Address = 1B8h) [reset = X]

R440 is shown in Figure 441 and described in Table 443.

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Figure 441. R440 Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED		RESERVED		DPLL1_TCXO_ORDER		
R-X	R/W-X		R/W-X		R/W-X		

Table 443. R440 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	X	
6-5	RESERVED	R/W	X	Reserved
4-3	RESERVED	R/W	X	Reserved
2-0	DPLL1_TCXO_ORDER	R/W	X	DPLL1 TCXO SDM order

2.442 R441 Register (Address = 1B9h) [reset = X]

R441 is shown in Figure 442 and described in Table 444.

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Figure 442. R441 Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED	DPLL2_SWITCHOVER_ALWAYS	DPLL2_FASTLOCK_ALWAYS	RESERVED	DPLL2_HLDOVR_MODE	DPLL2_LOOP_MODE	
R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	

Table 444. R441 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	X	Reserved
6	RESERVED	R/W	X	Reserved
5	DPLL2_SWITCHOVER_ALWAYS	R/W	X	DPLL2 switchover mode. If set to 1 and FASTLOCK_ALWAYS is 0, the switchover be hitless (minimal phase transient). If set to 0 and FASTLOCK_ALWAYS is 1, switchover is achieved using Fastlock and a phase hit will be propagated to the outputs during the switch. If set to 0 and FASTLOCK_ALWAYS is 0, the switchover will be hitless if the time spent in holdover is less than the switchover timer setting; otherwise, the switchover will be achieved using Fastlock.
4	DPLL2_FASTLOCK_ALWAYS	R/W	X	DPLL2 Fast Lock always enabled
3	RESERVED	R/W	X	Reserved
2	DPLL2_HLDOVR_MODE	R/W	X	DPLL2 Holdover mode control when tuning word history unavailable 0h = Enter free run mode (asserts user-defined DPLL2_TUNING_FREE_RUN word) 1h = Hold last control value prior to holdover
1-0	DPLL2_LOOP_MODE	R/W	X	DPLL2 Loop Mode control 0h = 1-loop (APLL free-run) 1h = 2-loop REF-DPLL 2h = 2-loop TCXO-DPLL 3h = 3-loop

2.443 R442 Register (Address = 1BAh) [reset = X]

R442 is shown in Figure 443 and described in Table 445.

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Figure 443. R442 Register

7	6	5	4	3	2	1	0
RESERVED				DPLL2_SWITCHOVER_TMR_EXP			
R-X				R/W-X			

Table 445. R442 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	X	
4-0	DPLL2_SWITCHOVER_TMR_EXP	R/W	X	DPLL2 Switchover Timer exponent

2.444 R443 Register (Address = 1BBh) [reset = X]

R443 is shown in Figure 444 and described in Table 446.

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Figure 444. R443 Register

7	6	5	4	3	2	1	0
RESERVED					DPLL2_SWITCHOVER_TMR_MANT[10:8]		
R-X					R/W-X		

Table 446. R443 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	X	
2-0	DPLL2_SWITCHOVER_TMR_MANT[10:8]	R/W	X	Bits 10:8 of DPLL2_SWITCHOVER_TMR_MANT

2.445 R444 Register (Address = 1BCh) [reset = X]

R444 is shown in Figure 445 and described in Table 447.

Return to Summary Table.

Figure 445. R444 Register

7	6	5	4	3	2	1	0
DPLL2_SWITCHOVER_TMR_MANT							
R/W-X							

Table 447. R444 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL2_SWITCHOVER_TMR_MANT	R/W	X	DPLL2 Switchover Timer mantissa

2.446 R445 Register (Address = 1BDh) [reset = X]

R445 is shown in Figure 446 and described in Table 448.

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Figure 446. R445 Register

7	6	5	4	3	2	1	0
DPLL2_REF0_RDIV[15:8]							
R/W-X							

Table 448. R445 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL2_REF0_RDIV[15:8]	R/W	X	Bits 15:8 of DPLL2_REF0_RDIV

2.447 R446 Register (Address = 1BEh) [reset = X]

R446 is shown in Figure 447 and described in Table 449.

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Figure 447. R446 Register

7	6	5	4	3	2	1	0
DPLL2_REF0_RDIV							
R/W-X							

Table 449. R446 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL2_REF0_RDIV	R/W	X	DPLL2 Ref0 divider

2.448 R447 Register (Address = 1BFh) [reset = X]

R447 is shown in Figure 448 and described in Table 450.

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Figure 448. R447 Register

7	6	5	4	3	2	1	0
DPLL2_REF1_RDIV[15:8]							
R/W-X							

Table 450. R447 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL2_REF1_RDIV[15:8]	R/W	X	Bits 15:8 of DPLL2_REF1_RDIV

2.449 R448 Register (Address = 1C0h) [reset = X]

R448 is shown in Figure 449 and described in Table 451.

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Figure 449. R448 Register

7	6	5	4	3	2	1	0
DPLL2_REF1_RDIV							
R/W-X							

Table 451. R448 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL2_REF1_RDIV	R/W	X	DPLL2 Ref1 divider

2.450 R449 Register (Address = 1C1h) [reset = X]

R449 is shown in Figure 450 and described in Table 452.

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Figure 450. R449 Register

7	6	5	4	3	2	1	0
DPLL2_REF2_RDIV[15:8]							
R/W-X							

Table 452. R449 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL2_REF2_RDIV[15:8]	R/W	X	Bits 15:8 of DPLL2_REF2_RDIV

2.451 R450 Register (Address = 1C2h) [reset = X]

R450 is shown in Figure 451 and described in Table 453.

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Figure 451. R450 Register

7	6	5	4	3	2	1	0
DPLL2_REF2_RDIV							
R/W-X							

Table 453. R450 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL2_REF2_RDIV	R/W	X	DPLL2 Ref2 divider

2.452 R451 Register (Address = 1C3h) [reset = X]

R451 is shown in Figure 452 and described in Table 454.

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Figure 452. R451 Register

7	6	5	4	3	2	1	0
DPLL2_REF3_RDIV[15:8]							
R/W-X							

Table 454. R451 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL2_REF3_RDIV[15:8]	R/W	X	Bits 15:8 of DPLL2_REF3_RDIV

2.453 R452 Register (Address = 1C4h) [reset = X]

R452 is shown in Figure 453 and described in Table 455.

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Figure 453. R452 Register

7	6	5	4	3	2	1	0
DPLL2_REF3_RDIV							
R/W-X							

Table 455. R452 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL2_REF3_RDIV	R/W	X	DPLL2 Ref3 divider

2.454 R453 Register (Address = 1C5h) [reset = X]

R453 is shown in Figure 454 and described in Table 456.

Return to Summary Table.

Figure 454. R453 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 456. R453 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.455 R454 Register (Address = 1C6h) [reset = X]

R454 is shown in Figure 455 and described in Table 457.

Return to Summary Table.

Figure 455. R454 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 457. R454 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.456 R455 Register (Address = 1C7h) [reset = X]

R455 is shown in Figure 456 and described in Table 458.

Return to Summary Table.

Figure 456. R455 Register

7	6	5	4	3	2	1	0
DPLL2_REF5_RDIV[15:8]							
R/W-X							

Table 458. R455 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL2_REF5_RDIV[15:8]	R/W	X	Bits 15:8 of DPLL2_REF5_RDIV

2.457 R456 Register (Address = 1C8h) [reset = X]

R456 is shown in Figure 457 and described in Table 459.

Return to Summary Table.

Figure 457. R456 Register

7	6	5	4	3	2	1	0
DPLL2_REF5_RDIV							
R/W-X							

Table 459. R456 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL2_REF5_RDIV	R/W	X	DPLL2 Ref5 divider Valid divide values are 1 (0001h) to 65535 (FFFFh).

2.458 R457 Register (Address = 1C9h) [reset = X]

R457 is shown in Figure 458 and described in Table 460.

Return to Summary Table.

Figure 458. R457 Register

7	6	5	4	3	2	1	0
RESERVED			RESERVED	OCXO_MDIV_DPLL2_TDC_SEL		RESERVED	RESERVED
R-X			R/W-X	R/W-X		R/W-X	R/W-X

Table 460. R457 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	X	
4	RESERVED	R/W	X	Reserved
3-2	OCXO_MDIV_DPLL2_TDC_SEL	R/W	X	DPLL2 TDC Selector 0h = Disable 1h = TCXO 3h = VCO2 Loopback (FBCLK)
1	RESERVED	R/W	X	Reserved
0	RESERVED	R/W	X	Reserved

2.459 R458 Register (Address = 1CAh) [reset = X]

R458 is shown in Figure 459 and described in Table 461.

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Figure 459. R458 Register

7	6	5	4	3	2	1	0
DPLL2_TDC_REF_DLY_GEN_EN	RESERVED		RESERVED	RESERVED			
R/W-X	R-X		R/W-X	R/W-X			

Table 461. R458 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	DPLL2_TDC_REF_DLY_GEN_EN	R/W	X	DPLL2 Reference TDC delay generation enable
6-5	RESERVED	R	X	
4	RESERVED	R/W	X	Reserved
3-0	RESERVED	R/W	X	Reserved

2.460 R459 Register (Address = 1CBh) [reset = X]

R459 is shown in Figure 460 and described in Table 462.

Return to Summary Table.

Figure 460. R459 Register

7	6	5	4	3	2	1	0
RESERVED							RESERVED
R-X							R/W-X

Table 462. R459 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	X	
0	RESERVED	R/W	X	Reserved

2.461 R460 Register (Address = 1CCh) [reset = X]

R460 is shown in Figure 461 and described in Table 463.

Return to Summary Table.

Figure 461. R460 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 463. R460 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.462 R461 Register (Address = 1CDh) [reset = X]

R461 is shown in Figure 462 and described in Table 464.

Return to Summary Table.

Figure 462. R461 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 464. R461 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.463 R462 Register (Address = 1CEh) [reset = X]

R462 is shown in Figure 463 and described in Table 465.

Return to Summary Table.

Figure 463. R462 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 465. R462 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.464 R463 Register (Address = 1CFh) [reset = X]

R463 is shown in Figure 464 and described in Table 466.

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Figure 464. R463 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 466. R463 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.465 R464 Register (Address = 1D0h) [reset = X]

R464 is shown in Figure 465 and described in Table 467.

Return to Summary Table.

Figure 465. R464 Register

7	6	5	4	3	2	1	0
RESERVED				RESERVED	RESERVED		RESERVED
R/W-X				R/W-0h	R/W-X		R-X

Table 467. R464 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	X	Reserved
3	RESERVED	R/W	0h	Reserved
2-1	RESERVED	R/W	X	Reserved
0	RESERVED	R	X	

2.466 R465 Register (Address = 1D1h) [reset = X]

R465 is shown in Figure 466 and described in Table 468.

Return to Summary Table.

Figure 466. R465 Register

7	6	5	4	3	2	1	0
RESERVED				RESERVED	RESERVED	RESERVED	
R-X				R/W-X	R/W-X	R/W-X	

Table 468. R465 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	X	
3	RESERVED	R/W	X	Reserved
2	RESERVED	R/W	X	Reserved
1-0	RESERVED	R/W	X	Reserved

2.467 R466 Register (Address = 1D2h) [reset = X]

R466 is shown in Figure 467 and described in Table 469.

Return to Summary Table.

Figure 467. R466 Register

7	6	5	4	3	2	1	0
RESERVED			RESERVED				
R-X			R/W-X				

Table 469. R466 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	X	
4-0	RESERVED	R/W	X	Reserved

2.468 R467 Register (Address = 1D3h) [reset = X]

R467 is shown in Figure 468 and described in Table 470.

Return to Summary Table.

Figure 468. R467 Register

7	6	5	4	3	2	1	0
RESERVED						RESERVED	
R-X						R/W-X	

Table 470. R467 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	X	
1-0	RESERVED	R/W	X	Reserved

2.469 R468 Register (Address = 1D4h) [reset = X]

R468 is shown in Figure 469 and described in Table 471.

Return to Summary Table.

Figure 469. R468 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 471. R468 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.470 R469 Register (Address = 1D5h) [reset = X]

R469 is shown in Figure 470 and described in Table 472.

Return to Summary Table.

Figure 470. R469 Register

7	6	5	4	3	2	1	0
RESERVED		RESERVED					
R-X		R/W-X					

Table 472. R469 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	
5-0	RESERVED	R/W	X	Reserved

2.471 R470 Register (Address = 1D6h) [reset = X]

R470 is shown in Figure 471 and described in Table 473.

Return to Summary Table.

Figure 471. R470 Register

7	6	5	4	3	2	1	0
RESERVED		RESERVED					
R-X		R/W-X					

Table 473. R470 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	
5-0	RESERVED	R/W	X	Reserved

2.472 R471 Register (Address = 1D7h) [reset = X]

R471 is shown in Figure 472 and described in Table 474.

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Figure 472. R471 Register

7	6	5	4	3	2	1	0
RESERVED		RESERVED					
R-X		R/W-X					

Table 474. R471 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	
5-0	RESERVED	R/W	X	Reserved

2.473 R472 Register (Address = 1D8h) [reset = X]

R472 is shown in Figure 473 and described in Table 475.

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Figure 473. R472 Register

7	6	5	4	3	2	1	0
RESERVED		RESERVED					
R-X		R/W-X					

Table 475. R472 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	X	
4-0	RESERVED	R/W	X	Reserved

2.474 R473 Register (Address = 1D9h) [reset = X]

R473 is shown in Figure 474 and described in Table 476.

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Figure 474. R473 Register

7	6	5	4	3	2	1	0
RESERVED			RESERVED				
R-X			R/W-X				

Table 476. R473 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	X	
4-0	RESERVED	R/W	X	Reserved

2.475 R474 Register (Address = 1DAh) [reset = X]

R474 is shown in Figure 475 and described in Table 477.

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Figure 475. R474 Register

7	6	5	4	3	2	1	0
RESERVED			RESERVED				
R-X			R/W-X				

Table 477. R474 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	X	
4-0	RESERVED	R/W	X	Reserved

2.476 R475 Register (Address = 1DBh) [reset = X]

R475 is shown in Figure 476 and described in Table 478.

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Figure 476. R475 Register

7	6	5	4	3	2	1	0
RESERVED			RESERVED				
R-X			R/W-X				

Table 478. R475 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	X	
4-0	RESERVED	R/W	X	Reserved

2.477 R476 Register (Address = 1DCh) [reset = X]

R476 is shown in Figure 477 and described in Table 479.

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Figure 477. R476 Register

7	6	5	4	3	2	1	0
RESERVED			RESERVED				
R-X			R/W-X				

Table 479. R476 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	X	
4-0	RESERVED	R/W	X	Reserved

2.478 R477 Register (Address = 1DDh) [reset = X]

R477 is shown in Figure 478 and described in Table 480.

Return to Summary Table.

Figure 478. R477 Register

7	6	5	4	3	2	1	0
RESERVED			RESERVED				
R-X			R/W-X				

Table 480. R477 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	X	
4-0	RESERVED	R/W	X	Reserved

2.479 R478 Register (Address = 1DEh) [reset = X]

R478 is shown in Figure 479 and described in Table 481.

Return to Summary Table.

Figure 479. R478 Register

7	6	5	4	3	2	1	0
RESERVED			RESERVED				
R-X			R/W-X				

Table 481. R478 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	X	
4-0	RESERVED	R/W	X	Reserved

2.480 R479 Register (Address = 1DFh) [reset = X]

R479 is shown in Figure 480 and described in Table 482.

Return to Summary Table.

Figure 480. R479 Register

7	6	5	4	3	2	1	0
RESERVED			RESERVED				
R-X			R/W-X				

Table 482. R479 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	X	
4-0	RESERVED	R/W	X	Reserved

2.481 R480 Register (Address = 1E0h) [reset = X]

R480 is shown in Figure 481 and described in Table 483.

Return to Summary Table.

Figure 481. R480 Register

7	6	5	4	3	2	1	0
RESERVED			RESERVED				
R-X			R/W-X				

Table 483. R480 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	X	
4-0	RESERVED	R/W	X	Reserved

2.482 R481 Register (Address = 1E1h) [reset = X]

R481 is shown in Figure 482 and described in Table 484.

Return to Summary Table.

Figure 482. R481 Register

7	6	5	4	3	2	1	0
RESERVED			RESERVED				
R-X			R/W-X				

Table 484. R481 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	X	
4-0	RESERVED	R/W	X	Reserved

2.483 R482 Register (Address = 1E2h) [reset = X]

R482 is shown in Figure 483 and described in Table 485.

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Figure 483. R482 Register

7	6	5	4	3	2	1	0
RESERVED			RESERVED				
R-X			R/W-X				

Table 485. R482 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	X	
4-0	RESERVED	R/W	X	Reserved

2.484 R483 Register (Address = 1E3h) [reset = X]

R483 is shown in Figure 484 and described in Table 486.

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Figure 484. R483 Register

7	6	5	4	3	2	1	0
RESERVED						RESERVED	
R-X						R/W-X	

Table 486. R483 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	X	
1-0	RESERVED	R/W	X	Reserved

2.485 R484 Register (Address = 1E4h) [reset = X]

R484 is shown in Figure 485 and described in Table 487.

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Figure 485. R484 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 487. R484 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.486 R485 Register (Address = 1E5h) [reset = X]

R485 is shown in Figure 486 and described in Table 488.

Return to Summary Table.

Figure 486. R485 Register

7	6	5	4	3	2	1	0
RESERVED						RESERVED	
R-X						R/W-X	

Table 488. R485 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	X	
1-0	RESERVED	R/W	X	Reserved

2.487 R486 Register (Address = 1E6h) [reset = X]

R486 is shown in Figure 487 and described in Table 489.

Return to Summary Table.

Figure 487. R486 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 489. R486 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.488 R487 Register (Address = 1E7h) [reset = X]

R487 is shown in Figure 488 and described in Table 490.

Return to Summary Table.

Figure 488. R487 Register

7	6	5	4	3	2	1	0
RESERVED						RESERVED	
R-X						R/W-X	

Table 490. R487 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	X	
1-0	RESERVED	R/W	X	Reserved

2.489 R488 Register (Address = 1E8h) [reset = X]

R488 is shown in Figure 489 and described in Table 491.

Return to Summary Table.

Figure 489. R488 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 491. R488 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.490 R489 Register (Address = 1E9h) [reset = X]

R489 is shown in Figure 490 and described in Table 492.

Return to Summary Table.

Figure 490. R489 Register

7	6	5	4	3	2	1	0
RESERVED				RESERVED			
R-X				R/W-X			

Table 492. R489 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	X	
3-0	RESERVED	R/W	X	Reserved

2.491 R490 Register (Address = 1EAh) [reset = X]

R490 is shown in Figure 491 and described in Table 493.

Return to Summary Table.

Figure 491. R490 Register

7	6	5	4	3	2	1	0
RESERVED						RESERVED	RESERVED
R-X						R/W-X	R/W-X

Table 493. R490 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	X	
1	RESERVED	R/W	X	Reserved
0	RESERVED	R/W	X	Reserved

2.492 R491 Register (Address = 1EBh) [reset = X]

R491 is shown in Figure 492 and described in Table 494.

Return to Summary Table.

Figure 492. R491 Register

7	6	5	4	3	2	1	0
RESERVED						RESERVED	
R-X						R/W-X	

Table 494. R491 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	X	
1-0	RESERVED	R/W	X	Reserved

2.493 R492 Register (Address = 1ECh) [reset = X]

R492 is shown in Figure 493 and described in Table 495.

Return to Summary Table.

Figure 493. R492 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 495. R492 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.494 R493 Register (Address = 1EDh) [reset = X]

R493 is shown in Figure 494 and described in Table 496.

Return to Summary Table.

Figure 494. R493 Register

7	6	5	4	3	2	1	0
RESERVED		RESERVED					
R-X		R/W-X					

Table 496. R493 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	
5-0	RESERVED	R/W	X	Reserved

2.495 R494 Register (Address = 1EEh) [reset = X]

R494 is shown in Figure 495 and described in Table 497.

Return to Summary Table.

Figure 495. R494 Register

7	6	5	4	3	2	1	0
RESERVED		RESERVED					
R-X		R/W-X					

Table 497. R494 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	
5-0	RESERVED	R/W	X	Reserved

2.496 R495 Register (Address = 1EFh) [reset = X]

R495 is shown in Figure 496 and described in Table 498.

Return to Summary Table.

Figure 496. R495 Register

7	6	5	4	3	2	1	0
RESERVED		RESERVED					
R-X		R/W-X					

Table 498. R495 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	
5-0	RESERVED	R/W	X	Reserved

2.497 R496 Register (Address = 1F0h) [reset = X]

R496 is shown in Figure 497 and described in Table 499.

Return to Summary Table.

Figure 497. R496 Register

7	6	5	4	3	2	1	0
RESERVED						RESERVED	
R-X						R/W-X	

Table 499. R496 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	X	
1-0	RESERVED	R/W	X	Reserved

2.498 R497 Register (Address = 1F1h) [reset = X]

R497 is shown in Figure 498 and described in Table 500.

Return to Summary Table.

Figure 498. R497 Register

7	6	5	4	3	2	1	0
RESERVED				RESERVED			
R-X				R/W-X			

Table 500. R497 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	X	
4-0	RESERVED	R/W	X	Reserved

2.499 R498 Register (Address = 1F2h) [reset = X]

R498 is shown in Figure 499 and described in Table 501.

Return to Summary Table.

Figure 499. R498 Register

7	6	5	4	3	2	1	0
RESERVED		RESERVED					
R-X		R/W-X					

Table 501. R498 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	
5-0	RESERVED	R/W	X	Reserved

2.500 R499 Register (Address = 1F3h) [reset = X]

R499 is shown in Figure 500 and described in Table 502.

Return to Summary Table.

Figure 500. R499 Register

7	6	5	4	3	2	1	0
RESERVED		RESERVED					
R-X		R/W-X					

Table 502. R499 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	
5-0	RESERVED	R/W	X	Reserved

2.501 R500 Register (Address = 1F4h) [reset = X]

R500 is shown in Figure 501 and described in Table 503.

Return to Summary Table.

Figure 501. R500 Register

7	6	5	4	3	2	1	0
DPLL2_CLK_FB_DIV_EN	RESERVED		DPLL2_CLK_FB_DIV				
R/W-X	R-X		R/W-X				

Table 503. R500 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	DPLL2_CLK_FB_DIV_EN	R/W	X	DPLL2 CLK Feedback Divider enable
6-5	RESERVED	R	X	
4-0	DPLL2_CLK_FB_DIV	R/W	X	DPLL2 CLK Feedback Divider value

2.502 R501 Register (Address = 1F5h) [reset = X]

R501 is shown in Figure 502 and described in Table 504.

Return to Summary Table.

Figure 502. R501 Register

7	6	5	4	3	2	1	0
RESERVED				DPLL2_REF_FB_PRE_DIV			
R-X				R/W-X			

Table 504. R501 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	X	
3-0	DPLL2_REF_FB_PRE_DIV	R/W	X	DPLL2 REF Feedback Pre Divider value 0h = 2 1h = 3 Fh = 17

2.503 R502 Register (Address = 1F6h) [reset = X]

R502 is shown in Figure 503 and described in Table 505.

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Figure 503. R502 Register

7	6	5	4	3	2	1	0
RESERVED		DPLL2_REF_FB_DIV[29:24]					
R-X		R/W-X					

Table 505. R502 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	
5-0	DPLL2_REF_FB_DIV[29:24]	R/W	X	Bits 29:24 of DPLL2_REF_FB_DIV

2.504 R503 Register (Address = 1F7h) [reset = X]

R503 is shown in Figure 504 and described in Table 506.

Return to Summary Table.

Figure 504. R503 Register

7	6	5	4	3	2	1	0
DPLL2_REF_FB_DIV[23:16]							
R/W-X							

Table 506. R503 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL2_REF_FB_DIV[23:16]	R/W	X	Bits 23:16 of DPLL2_REF_FB_DIV

2.505 R504 Register (Address = 1F8h) [reset = X]

R504 is shown in Figure 505 and described in Table 507.

Return to Summary Table.

Figure 505. R504 Register

7	6	5	4	3	2	1	0
DPLL2_REF_FB_DIV[15:8]							
R/W-X							

Table 507. R504 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL2_REF_FB_DIV[15:8]	R/W	X	Bits 15:8 of DPLL2_REF_FB_DIV

2.506 R505 Register (Address = 1F9h) [reset = X]

R505 is shown in Figure 506 and described in Table 508.

Return to Summary Table.

Figure 506. R505 Register

7	6	5	4	3	2	1	0
DPLL2_REF_FB_DIV							
R/W-X							

Table 508. R505 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL2_REF_FB_DIV	R/W	X	DPLL2 REF Feedback Divider value

2.507 R506 Register (Address = 1FAh) [reset = X]

R506 is shown in Figure 507 and described in Table 509.

Return to Summary Table.

Figure 507. R506 Register

7	6	5	4	3	2	1	0
DPLL2_REF_NUM[39:32]							
R/W-X							

Table 509. R506 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL2_REF_NUM[39:32]	R/W	X	Bits 39:32 of DPLL2_REF_NUM

2.508 R507 Register (Address = 1FBh) [reset = X]

R507 is shown in Figure 508 and described in Table 510.

Return to Summary Table.

Figure 508. R507 Register

7	6	5	4	3	2	1	0
DPLL2_REF_NUM[31:24]							
R/W-X							

Table 510. R507 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL2_REF_NUM[31:24]	R/W	X	Bits 31:24 of DPLL2_REF_NUM

2.509 R508 Register (Address = 1FCh) [reset = X]

R508 is shown in Figure 509 and described in Table 511.

Return to Summary Table.

Figure 509. R508 Register

7	6	5	4	3	2	1	0
DPLL2_REF_NUM[23:16]							
R/W-X							

Table 511. R508 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL2_REF_NUM[23:16]	R/W	X	Bits 23:16 of DPLL2_REF_NUM

2.510 R509 Register (Address = 1FDh) [reset = X]

R509 is shown in Figure 510 and described in Table 512.

Return to Summary Table.

Figure 510. R509 Register

7	6	5	4	3	2	1	0
DPLL2_REF_NUM[15:8]							
R/W-X							

Table 512. R509 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL2_REF_NUM[15:8]	R/W	X	Bits 15:8 of DPLL2_REF_NUM

2.511 R510 Register (Address = 1FEh) [reset = X]

R510 is shown in Figure 511 and described in Table 513.

Return to Summary Table.

Figure 511. R510 Register

7	6	5	4	3	2	1	0
DPLL2_REF_NUM							
R/W-X							

Table 513. R510 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL2_REF_NUM	R/W	X	DPLL2 REF FB Divider Numerator

2.512 R511 Register (Address = 1FFh) [reset = X]

R511 is shown in Figure 512 and described in Table 514.

Return to Summary Table.

Figure 512. R511 Register

7	6	5	4	3	2	1	0
DPLL2_REF_DEN[39:32]							
R/W-X							

Table 514. R511 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL2_REF_DEN[39:32]	R/W	X	Bits 39:32 of DPLL2_REF_DEN

2.513 R512 Register (Address = 200h) [reset = X]

R512 is shown in Figure 513 and described in Table 515.

Return to Summary Table.

Figure 513. R512 Register

7	6	5	4	3	2	1	0
DPLL2_REF_DEN[31:24]							
R/W-X							

Table 515. R512 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL2_REF_DEN[31:24]	R/W	X	Bits 31:24 of DPLL2_REF_DEN

2.514 R513 Register (Address = 201h) [reset = X]

R513 is shown in Figure 514 and described in Table 516.

Return to Summary Table.

Figure 514. R513 Register

7	6	5	4	3	2	1	0
DPLL2_REF_DEN[23:16]							
R/W-X							

Table 516. R513 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL2_REF_DEN[23:16]	R/W	X	Bits 23:16 of DPLL2_REF_DEN

2.515 R514 Register (Address = 202h) [reset = X]

R514 is shown in Figure 515 and described in Table 517.

Return to Summary Table.

Figure 515. R514 Register

7	6	5	4	3	2	1	0
DPLL2_REF_DEN[15:8]							
R/W-X							

Table 517. R514 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL2_REF_DEN[15:8]	R/W	X	Bits 15:8 of DPLL2_REF_DEN

2.516 R515 Register (Address = 203h) [reset = X]

R515 is shown in Figure 516 and described in Table 518.

Return to Summary Table.

Figure 516. R515 Register

7	6	5	4	3	2	1	0
DPLL2_REF_DEN							
R/W-X							

Table 518. R515 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL2_REF_DEN	R/W	X	DPLL2 REF FB Divider denominator

2.517 R516 Register (Address = 204h) [reset = X]

R516 is shown in Figure 517 and described in Table 519.

Return to Summary Table.

Figure 517. R516 Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED		RESERVED		DPLL2_REF_ORDER		
R-X	R/W-X		R/W-X		R/W-X		

Table 519. R516 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	X	
6-5	RESERVED	R/W	X	Reserved
4-3	RESERVED	R/W	X	Reserved
2-0	DPLL2_REF_ORDER	R/W	X	DPLL2 REF SDM order

2.518 R517 Register (Address = 205h) [reset = X]

R517 is shown in Figure 518 and described in Table 520.

Return to Summary Table.

Figure 518. R517 Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED						
R-X	R/W-X						

Table 520. R517 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	X	
6-0	RESERVED	R/W	X	Reserved

2.519 R518 Register (Address = 206h) [reset = X]

R518 is shown in Figure 519 and described in Table 521.

Return to Summary Table.

Figure 519. R518 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 521. R518 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.520 R519 Register (Address = 207h) [reset = X]

R519 is shown in Figure 520 and described in Table 522.

Return to Summary Table.

Figure 520. R519 Register

7	6	5	4	3	2	1	0
RESERVED		RESERVED					
R-X		R/W-X					

Table 522. R519 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	
5-0	RESERVED	R/W	X	Reserved

2.521 R520 Register (Address = 208h) [reset = X]

R520 is shown in Figure 521 and described in Table 523.

Return to Summary Table.

Figure 521. R520 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 523. R520 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.522 R521 Register (Address = 209h) [reset = X]

R521 is shown in Figure 522 and described in Table 524.

Return to Summary Table.

Figure 522. R521 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 524. R521 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.523 R522 Register (Address = 20Ah) [reset = X]

R522 is shown in Figure 523 and described in Table 525.

Return to Summary Table.

Figure 523. R522 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 525. R522 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.524 R523 Register (Address = 20Bh) [reset = X]

R523 is shown in Figure 524 and described in Table 526.

Return to Summary Table.

Figure 524. R523 Register

7	6	5	4	3	2	1	0
RESERVED		RESERVED					
R-X		R/W-X					

Table 526. R523 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	
5-0	RESERVED	R/W	X	Reserved

2.525 R524 Register (Address = 20Ch) [reset = X]

R524 is shown in Figure 525 and described in Table 527.

Return to Summary Table.

Figure 525. R524 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 527. R524 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.526 R525 Register (Address = 20Dh) [reset = X]

R525 is shown in Figure 526 and described in Table 528.

Return to Summary Table.

Figure 526. R525 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 528. R525 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.527 R526 Register (Address = 20Eh) [reset = X]

R526 is shown in Figure 527 and described in Table 529.

Return to Summary Table.

Figure 527. R526 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 529. R526 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.528 R527 Register (Address = 20Fh) [reset = X]

R527 is shown in Figure 528 and described in Table 530.

Return to Summary Table.

Figure 528. R527 Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED						
R-X	R/W-X						

Table 530. R527 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	X	
6-0	RESERVED	R/W	X	Reserved

2.529 R528 Register (Address = 210h) [reset = X]

R528 is shown in Figure 529 and described in Table 531.

Return to Summary Table.

Figure 529. R528 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 531. R528 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.530 R529 Register (Address = 211h) [reset = X]

R529 is shown in Figure 530 and described in Table 532.

Return to Summary Table.

Figure 530. R529 Register

7	6	5	4	3	2	1	0
RESERVED		RESERVED					
R-X		R/W-X					

Table 532. R529 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	
5-0	RESERVED	R/W	X	Reserved

2.531 R530 Register (Address = 212h) [reset = X]

R530 is shown in Figure 531 and described in Table 533.

Return to Summary Table.

Figure 531. R530 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 533. R530 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.532 R531 Register (Address = 213h) [reset = X]

R531 is shown in Figure 532 and described in Table 534.

Return to Summary Table.

Figure 532. R531 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 534. R531 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.533 R532 Register (Address = 214h) [reset = X]

R532 is shown in Figure 533 and described in Table 535.

Return to Summary Table.

Figure 533. R532 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 535. R532 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.534 R533 Register (Address = 215h) [reset = X]

R533 is shown in Figure 534 and described in Table 536.

Return to Summary Table.

Figure 534. R533 Register

7	6	5	4	3	2	1	0
RESERVED		RESERVED					
R-X		R/W-X					

Table 536. R533 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	
5-0	RESERVED	R/W	X	Reserved

2.535 R534 Register (Address = 216h) [reset = X]

R534 is shown in Figure 535 and described in Table 537.

Return to Summary Table.

Figure 535. R534 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 537. R534 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.536 R535 Register (Address = 217h) [reset = X]

R535 is shown in Figure 536 and described in Table 538.

Return to Summary Table.

Figure 536. R535 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 538. R535 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.537 R536 Register (Address = 218h) [reset = X]

R536 is shown in Figure 537 and described in Table 539.

Return to Summary Table.

Figure 537. R536 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 539. R536 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.538 R537 Register (Address = 219h) [reset = X]

R537 is shown in Figure 538 and described in Table 540.

Return to Summary Table.

Figure 538. R537 Register

7	6	5	4	3	2	1	0
RESERVED			DPLL2_REF_SYNC_PH_OFFSET[44:40]				
R-X			R/W-X				

Table 540. R537 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	X	
4-0	DPLL2_REF_SYNC_PH_OFFSET[44:40]	R/W	X	Bits 44:40 of DPLL2_REF_SYNC_PH_OFFSET

2.539 R538 Register (Address = 21Ah) [reset = X]

R538 is shown in Figure 539 and described in Table 541.

Return to Summary Table.

Figure 539. R538 Register

7	6	5	4	3	2	1	0
DPLL2_REF_SYNC_PH_OFFSET[39:32]							
R/W-X							

Table 541. R538 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL2_REF_SYNC_PH_OFFSET[39:32]	R/W	X	Bits 39:32 of DPLL2_REF_SYNC_PH_OFFSET

2.540 R539 Register (Address = 21Bh) [reset = X]

R539 is shown in Figure 540 and described in Table 542.

Return to Summary Table.

Figure 540. R539 Register

7	6	5	4	3	2	1	0
DPLL2_REF_SYNC_PH_OFFSET[31:24]							
R/W-X							

Table 542. R539 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL2_REF_SYNC_PH_OFFSET[31:24]	R/W	X	Bits 31:24 of DPLL2_REF_SYNC_PH_OFFSET

2.541 R540 Register (Address = 21Ch) [reset = X]

R540 is shown in Figure 541 and described in Table 543.

Return to Summary Table.

Figure 541. R540 Register

7	6	5	4	3	2	1	0
DPLL2_REF_SYNC_PH_OFFSET[23:16]							
R/W-X							

Table 543. R540 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL2_REF_SYNC_PH_OFFSET[23:16]	R/W	X	Bits 23:16 of DPLL2_REF_SYNC_PH_OFFSET

2.542 R541 Register (Address = 21Dh) [reset = X]

R541 is shown in Figure 542 and described in Table 544.

Return to Summary Table.

Figure 542. R541 Register

7	6	5	4	3	2	1	0
DPLL2_REF_SYNC_PH_OFFSET[15:8]							
R/W-X							

Table 544. R541 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL2_REF_SYNC_PH_OFFSET[15:8]	R/W	X	Bits 15:8 of DPLL2_REF_SYNC_PH_OFFSET

2.543 R542 Register (Address = 21Eh) [reset = X]

R542 is shown in Figure 543 and described in Table 545.

Return to Summary Table.

Figure 543. R542 Register

7	6	5	4	3	2	1	0
DPLL2_REF_SYNC_PH_OFFSET							
R/W-X							

Table 545. R542 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL2_REF_SYNC_PH_OFFSET	R/W	X	DPLL2 REF Zero Delay Mode Phase Offset

2.544 R543 Register (Address = 21Fh) [reset = X]

R543 is shown in Figure 544 and described in Table 546.

Return to Summary Table.

Figure 544. R543 Register

7	6	5	4	3	2	1	0
RESERVED						RESERVED	RESERVED
R-X						R/W-X	R/W-X

Table 546. R543 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	X	
1	RESERVED	R/W	X	Reserved
0	RESERVED	R/W	X	Reserved

2.545 R544 Register (Address = 220h) [reset = X]

R544 is shown in Figure 545 and described in Table 547.

Return to Summary Table.

Figure 545. R544 Register

7	6	5	4	3	2	1	0
RESERVED		RESERVED					
R-X		R/W-X					

Table 547. R544 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	
5-0	RESERVED	R/W	X	Reserved

2.546 R545 Register (Address = 221h) [reset = X]

R545 is shown in Figure 546 and described in Table 548.

Return to Summary Table.

Figure 546. R545 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 548. R545 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.547 R546 Register (Address = 222h) [reset = X]

R546 is shown in Figure 547 and described in Table 549.

Return to Summary Table.

Figure 547. R546 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 549. R546 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.548 R547 Register (Address = 223h) [reset = X]

R547 is shown in Figure 548 and described in Table 550.

Return to Summary Table.

Figure 548. R547 Register

7	6	5	4	3	2	1	0
DPLL2_TDC_TCXO_DLY_GEN_EN	RESERVED		RESERVED	RESERVED			
R/W-X	R-X		R/W-X	R/W-X			

Table 550. R547 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	DPLL2_TDC_TCXO_DLY_GEN_EN	R/W	X	DPLL2 TCXO TDC delay generation enable
6-5	RESERVED	R	X	
4	RESERVED	R/W	X	Reserved
3-0	RESERVED	R/W	X	Reserved

2.549 R548 Register (Address = 224h) [reset = X]

R548 is shown in Figure 549 and described in Table 551.

Return to Summary Table.

Figure 549. R548 Register

7	6	5	4	3	2	1	0
RESERVED				RESERVED	RESERVED		
R/W-X				R/W-0h	R-X		

Table 551. R548 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	X	Reserved
3	RESERVED	R/W	0h	Reserved
2-0	RESERVED	R	X	

2.550 R549 Register (Address = 225h) [reset = X]

R549 is shown in Figure 550 and described in Table 552.

Return to Summary Table.

Figure 550. R549 Register

7	6	5	4	3	2	1	0
RESERVED				RESERVED			
R-X				R/W-X			

Table 552. R549 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	X	
4-0	RESERVED	R/W	X	Reserved

2.551 R550 Register (Address = 226h) [reset = X]

R550 is shown in Figure 551 and described in Table 553.

Return to Summary Table.

Figure 551. R550 Register

7	6	5	4	3	2	1	0
RESERVED						RESERVED	
R-X						R/W-X	

Table 553. R550 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	X	
1-0	RESERVED	R/W	X	Reserved

2.552 R551 Register (Address = 227h) [reset = X]

R551 is shown in Figure 552 and described in Table 554.

Return to Summary Table.

Figure 552. R551 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 554. R551 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.553 R552 Register (Address = 228h) [reset = X]

R552 is shown in Figure 553 and described in Table 555.

Return to Summary Table.

Figure 553. R552 Register

7	6	5	4	3	2	1	0
RESERVED			RESERVED				
R-X			R/W-X				

Table 555. R552 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	X	
4-0	RESERVED	R/W	X	Reserved

2.554 R553 Register (Address = 229h) [reset = X]

R553 is shown in Figure 554 and described in Table 556.

Return to Summary Table.

Figure 554. R553 Register

7	6	5	4	3	2	1	0
RESERVED			RESERVED				
R-X			R/W-X				

Table 556. R553 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	X	
4-0	RESERVED	R/W	X	Reserved

2.555 R554 Register (Address = 22Ah) [reset = X]

R554 is shown in Figure 555 and described in Table 557.

Return to Summary Table.

Figure 555. R554 Register

7	6	5	4	3	2	1	0
RESERVED			RESERVED				
R-X			R/W-X				

Table 557. R554 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	X	
4-0	RESERVED	R/W	X	Reserved

2.556 R555 Register (Address = 22Bh) [reset = X]

R555 is shown in Figure 556 and described in Table 558.

Return to Summary Table.

Figure 556. R555 Register

7	6	5	4	3	2	1	0
RESERVED			RESERVED				
R-X			R/W-X				

Table 558. R555 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	X	
4-0	RESERVED	R/W	X	Reserved

2.557 R556 Register (Address = 22Ch) [reset = X]

R556 is shown in Figure 557 and described in Table 559.

Return to Summary Table.

Figure 557. R556 Register

7	6	5	4	3	2	1	0
RESERVED			RESERVED				
R-X			R/W-X				

Table 559. R556 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	X	
4-0	RESERVED	R/W	X	Reserved

2.558 R557 Register (Address = 22Dh) [reset = X]

R557 is shown in Figure 558 and described in Table 560.

Return to Summary Table.

Figure 558. R557 Register

7	6	5	4	3	2	1	0
RESERVED			RESERVED				
R-X			R/W-X				

Table 560. R557 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	X	
4-0	RESERVED	R/W	X	Reserved

2.559 R558 Register (Address = 22Eh) [reset = X]

R558 is shown in Figure 559 and described in Table 561.

Return to Summary Table.

Figure 559. R558 Register

7	6	5	4	3	2	1	0
RESERVED			RESERVED				
R-X			R/W-X				

Table 561. R558 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	X	
4-0	RESERVED	R/W	X	Reserved

2.560 R559 Register (Address = 22Fh) [reset = X]

R559 is shown in Figure 560 and described in Table 562.

Return to Summary Table.

Figure 560. R559 Register

7	6	5	4	3	2	1	0
RESERVED			RESERVED				
R-X			R/W-X				

Table 562. R559 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	X	
4-0	RESERVED	R/W	X	Reserved

2.561 R560 Register (Address = 230h) [reset = X]

R560 is shown in Figure 561 and described in Table 563.

Return to Summary Table.

Figure 561. R560 Register

7	6	5	4	3	2	1	0
RESERVED			RESERVED				
R-X			R/W-X				

Table 563. R560 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	X	
4-0	RESERVED	R/W	X	Reserved

2.562 R561 Register (Address = 231h) [reset = X]

R561 is shown in Figure 562 and described in Table 564.

Return to Summary Table.

Figure 562. R561 Register

7	6	5	4	3	2	1	0
RESERVED			RESERVED				
R-X			R/W-X				

Table 564. R561 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	X	
4-0	RESERVED	R/W	X	Reserved

2.563 R562 Register (Address = 232h) [reset = X]

R562 is shown in Figure 563 and described in Table 565.

Return to Summary Table.

Figure 563. R562 Register

7	6	5	4	3	2	1	0
RESERVED						RESERVED	
R-X						R/W-X	

Table 565. R562 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	X	
1-0	RESERVED	R/W	X	Reserved

2.564 R563 Register (Address = 233h) [reset = X]

R563 is shown in Figure 564 and described in Table 566.

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Figure 564. R563 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 566. R563 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.565 R564 Register (Address = 234h) [reset = X]

R564 is shown in Figure 565 and described in Table 567.

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Figure 565. R564 Register

7	6	5	4	3	2	1	0
RESERVED						RESERVED	
R-X						R/W-X	

Table 567. R564 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	X	
1-0	RESERVED	R/W	X	Reserved

2.566 R565 Register (Address = 235h) [reset = X]

R565 is shown in Figure 566 and described in Table 568.

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Figure 566. R565 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 568. R565 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.567 R566 Register (Address = 236h) [reset = X]

R566 is shown in Figure 567 and described in Table 569.

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Figure 567. R566 Register

7	6	5	4	3	2	1	0
RESERVED		RESERVED					
R-X		R/W-X					

Table 569. R566 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	
5-0	RESERVED	R/W	X	Reserved

2.568 R567 Register (Address = 237h) [reset = X]

R567 is shown in Figure 568 and described in Table 570.

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Figure 568. R567 Register

7	6	5	4	3	2	1	0
RESERVED		RESERVED					
R-X		R/W-X					

Table 570. R567 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	
5-0	RESERVED	R/W	X	Reserved

2.569 R568 Register (Address = 238h) [reset = X]

R568 is shown in Figure 569 and described in Table 571.

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Figure 569. R568 Register

7	6	5	4	3	2	1	0
RESERVED						RESERVED	
R-X						R/W-X	

Table 571. R568 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	X	
1-0	RESERVED	R/W	X	Reserved

2.570 R569 Register (Address = 239h) [reset = X]

R569 is shown in Figure 570 and described in Table 572.

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Figure 570. R569 Register

7	6	5	4	3	2	1	0
RESERVED				DPLL2_TCXO_FB_PRE_DIV			
R-X				R/W-X			

Table 572. R569 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	X	
3-0	DPLL2_TCXO_FB_PRE_DIV	R/W	X	DPLL2 TCXO Feedback Pre Divider value 0h = 2 1h = 3 Fh = 17

2.571 R570 Register (Address = 23Ah) [reset = X]

R570 is shown in Figure 571 and described in Table 573.

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Figure 571. R570 Register

7	6	5	4	3	2	1	0
RESERVED				DPLL2_TCXO_FB_DIV[29:24]			
R-X				R/W-X			

Table 573. R570 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	
5-0	DPLL2_TCXO_FB_DIV[29:24]	R/W	X	Bits 29:24 of DPLL2_TCXO_FB_DIV

2.572 R571 Register (Address = 23Bh) [reset = X]

R571 is shown in Figure 572 and described in Table 574.

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Figure 572. R571 Register

7	6	5	4	3	2	1	0
DPLL2_TCXO_FB_DIV[23:16]							
R/W-X							

Table 574. R571 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL2_TCXO_FB_DIV[23:16]	R/W	X	Bits 23:16 of DPLL2_TCXO_FB_DIV

2.573 R572 Register (Address = 23Ch) [reset = X]

R572 is shown in Figure 573 and described in Table 575.

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Figure 573. R572 Register

7	6	5	4	3	2	1	0
DPLL2_TCXO_FB_DIV[15:8]							
R/W-X							

Table 575. R572 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL2_TCXO_FB_DIV[15:8]	R/W	X	Bits 15:8 of DPLL2_TCXO_FB_DIV

2.574 R573 Register (Address = 23Dh) [reset = X]

R573 is shown in Figure 574 and described in Table 576.

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Figure 574. R573 Register

7	6	5	4	3	2	1	0
DPLL2_TCXO_FB_DIV							
R/W-X							

Table 576. R573 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL2_TCXO_FB_DIV	R/W	X	DPLL2 TCXO Feedback Divider value

2.575 R574 Register (Address = 23Eh) [reset = X]

R574 is shown in Figure 575 and described in Table 577.

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Figure 575. R574 Register

7	6	5	4	3	2	1	0
DPLL2_TCXO_NUM[39:32]							
R/W-X							

Table 577. R574 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL2_TCXO_NUM[39:32]	R/W	X	Bits 39:32 of DPLL2_TCXO_NUM

2.576 R575 Register (Address = 23Fh) [reset = X]

R575 is shown in Figure 576 and described in Table 578.

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Figure 576. R575 Register

7	6	5	4	3	2	1	0
DPLL2_TCXO_NUM[31:24]							
R/W-X							

Table 578. R575 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL2_TCXO_NUM[31:24]	R/W	X	Bits 31:24 of DPLL2_TCXO_NUM

2.577 R576 Register (Address = 240h) [reset = X]

R576 is shown in Figure 577 and described in Table 579.

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Figure 577. R576 Register

7	6	5	4	3	2	1	0
DPLL2_TCXO_NUM[23:16]							
R/W-X							

Table 579. R576 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL2_TCXO_NUM[23:16]	R/W	X	Bits 23:16 of DPLL2_TCXO_NUM

2.578 R577 Register (Address = 241h) [reset = X]

R577 is shown in Figure 578 and described in Table 580.

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Figure 578. R577 Register

7	6	5	4	3	2	1	0
DPLL2_TCXO_NUM[15:8]							
R/W-X							

Table 580. R577 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL2_TCXO_NUM[15:8]	R/W	X	Bits 15:8 of DPLL2_TCXO_NUM

2.579 R578 Register (Address = 242h) [reset = X]

R578 is shown in Figure 579 and described in Table 581.

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Figure 579. R578 Register

7	6	5	4	3	2	1	0
DPLL2_TCXO_NUM							
R/W-X							

Table 581. R578 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL2_TCXO_NUM	R/W	X	DPLL2 TCXO FB Divider Numerator

2.580 R579 Register (Address = 243h) [reset = X]

R579 is shown in Figure 580 and described in Table 582.

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Figure 580. R579 Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED		RESERVED		DPLL2_TCXO_ORDER		
R-X	R/W-X		R/W-X		R/W-X		

Table 582. R579 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	X	
6-5	RESERVED	R/W	X	Reserved
4-3	RESERVED	R/W	X	Reserved
2-0	DPLL2_TCXO_ORDER	R/W	X	DPLL2 TCXO MASH order

2.581 R580 Register (Address = 244h) [reset = X]

R580 is shown in Figure 581 and described in Table 583.

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Figure 581. R580 Register

7	6	5	4	3	2	1	0
RESERVED					DPLL1_DCO_SEL_REF_TCXOB	DPLL1_IGNORE_GPIO_PIN	DPLL1_FDEV_EN
R-X					R/W-X	R/W-X	R/W-X

Table 583. R580 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	X	
2	DPLL1_DCO_SEL_REF_TCXOB	R/W	X	DPLL1 bit to select DCO mode 0h = TCXO-DPLL 1h = REF-DPLL
1	DPLL1_IGNORE_GPIO_PIN	R/W	X	DPLL1 Freq Incr/Decr updates via pin are ignored
0	DPLL1_FDEV_EN	R/W	X	DPLL1 Freq Incr/Decr enable via pin or reg control

2.582 R581 Register (Address = 245h) [reset = X]

R581 is shown in Figure 582 and described in Table 584.

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Figure 582. R581 Register

7	6	5	4	3	2	1	0
RESERVED					DPLL2_DCO_SEL_REF_TCXOB	DPLL2_IGNORE_GPIO_PIN	DPLL2_FDEV_EN
R-X					R/W-X	R/W-X	R/W-X

Table 584. R581 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	X	
2	DPLL2_DCO_SEL_REF_TCXOB	R/W	X	DPLL2 bit to select DCO mode 0h = TCXO-DPLL 1h = REF-DPLL
1	DPLL2_IGNORE_GPIO_PIN	R/W	X	DPLL2 Freq Incr/Decr updates via pin are ignored
0	DPLL2_FDEV_EN	R/W	X	DPLL2 Freq Incr/Decr enable via pin or reg control

2.583 R582 Register (Address = 246h) [reset = X]

R582 is shown in Figure 583 and described in Table 585.

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Figure 583. R582 Register

7	6	5	4	3	2	1	0
RESERVED				DPLL1_FDEV[37:32]			
R-X				R/W-X			

Table 585. R582 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	
5-0	DPLL1_FDEV[37:32]	R/W	X	Bits 37:32 of DPLL1_FDEV

2.584 R583 Register (Address = 247h) [reset = X]

R583 is shown in Figure 584 and described in Table 586.

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Figure 584. R583 Register

7	6	5	4	3	2	1	0
DPLL1_FDEV[31:24]							
R/W-X							

Table 586. R583 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL1_FDEV[31:24]	R/W	X	Bits 31:24 of DPLL1_FDEV

2.585 R584 Register (Address = 248h) [reset = X]

R584 is shown in Figure 585 and described in Table 587.

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Figure 585. R584 Register

7	6	5	4	3	2	1	0
DPLL1_FDEV[23:16]							
R/W-X							

Table 587. R584 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL1_FDEV[23:16]	R/W	X	Bits 23:16 of DPLL1_FDEV

2.586 R585 Register (Address = 249h) [reset = X]

R585 is shown in Figure 586 and described in Table 588.

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Figure 586. R585 Register

7	6	5	4	3	2	1	0
DPLL1_FDEV[15:8]							
R/W-X							

Table 588. R585 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL1_FDEV[15:8]	R/W	X	Bits 15:8 of DPLL1_FDEV

2.587 R586 Register (Address = 24Ah) [reset = X]

R586 is shown in Figure 587 and described in Table 589.

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Figure 587. R586 Register

7	6	5	4	3	2	1	0
DPLL1_FDEV							
R/W-X							

Table 589. R586 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL1_FDEV	R/W	X	DPLL1 Freq Incr/Decr Numerator Step Word This step word is computed based on the desired DCO frequecy step size in ppb (parts-per-billion).

2.588 R587 Register (Address = 24Bh) [reset = 0h]

R587 is shown in Figure 588 and described in Table 590.

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Figure 588. R587 Register

7	6	5	4	3	2	1	0
RESERVED							DPLL1_FDEV_REG_UPDATE
R-0h							R/W-0h

Table 590. R587 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0h	
0	DPLL1_FDEV_REG_UPDATE	R/W	0h	DPLL1 Freq Incr/Decr register control Writing this register applies one FINC/FDEC of the Numerator as defined by the FDEV register. 0h = Increment Frequency 1h = Decrement Frequency

2.589 R588 Register (Address = 24Ch) [reset = X]

R588 is shown in Figure 589 and described in Table 591.

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Figure 589. R588 Register

7	6	5	4	3	2	1	0
RESERVED		DPLL2_FDEV[37:32]					
R-X		R/W-X					

Table 591. R588 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	
5-0	DPLL2_FDEV[37:32]	R/W	X	Bits 37:32 of DPLL2_FDEV

2.590 R589 Register (Address = 24Dh) [reset = X]

R589 is shown in Figure 590 and described in Table 592.

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Figure 590. R589 Register

7	6	5	4	3	2	1	0
DPLL2_FDEV[31:24]							
R/W-X							

Table 592. R589 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL2_FDEV[31:24]	R/W	X	Bits 31:24 of DPLL2_FDEV

2.591 R590 Register (Address = 24Eh) [reset = X]

R590 is shown in Figure 591 and described in Table 593.

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Figure 591. R590 Register

7	6	5	4	3	2	1	0
DPLL2_FDEV[23:16]							
R/W-X							

Table 593. R590 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL2_FDEV[23:16]	R/W	X	Bits 23:16 of DPLL2_FDEV

2.592 R591 Register (Address = 24Fh) [reset = X]

R591 is shown in Figure 592 and described in Table 594.

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Figure 592. R591 Register

7	6	5	4	3	2	1	0
DPLL2_FDEV[15:8]							
R/W-X							

Table 594. R591 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL2_FDEV[15:8]	R/W	X	Bits 15:8 of DPLL2_FDEV

2.593 R592 Register (Address = 250h) [reset = X]

R592 is shown in Figure 593 and described in Table 595.

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Figure 593. R592 Register

7	6	5	4	3	2	1	0
DPLL2_FDEV							
R/W-X							

Table 595. R592 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL2_FDEV	R/W	X	DPLL2 Freq Incr/Decr Numerator Step Word This step word is computed based on the desired DCO frequecy step size in ppb (parts-per-billion).

2.594 R593 Register (Address = 251h) [reset = 0h]

R593 is shown in Figure 594 and described in Table 596.

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Figure 594. R593 Register

7	6	5	4	3	2	1	0
RESERVED							DPLL2_FDEV_REG_UPDATE
R-0h							R/W-0h

Table 596. R593 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0h	
0	DPLL2_FDEV_REG_UPDATE	R/W	0h	DPLL2 Freq Incr/Decr register control Writing this register applies one FINC/FDEC of the Numerator as defined by the FDEV register. 0h = Increment Frequency 1h = Decrement Frequency

2.595 R594 Register (Address = 252h) [reset = X]

R594 is shown in Figure 595 and described in Table 597.

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Figure 595. R594 Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	DPLL1_ZDM_SYNC_EN	DPLL1_ZDM_EN
R-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X

Table 597. R594 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	X	
6	RESERVED	R/W	X	Reserved
5	RESERVED	R/W	X	Reserved
4	RESERVED	R/W	X	Reserved
3	RESERVED	R/W	X	Reserved
2	RESERVED	R/W	X	Reserved
1	DPLL1_ZDM_SYNC_EN	R/W	X	DPLL1 Zero Delay Synchronization enable
0	DPLL1_ZDM_EN	R/W	X	DPLL1 ZDM enable

2.596 R595 Register (Address = 253h) [reset = X]

R595 is shown in Figure 596 and described in Table 598.

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Figure 596. R595 Register

7	6	5	4	3	2	1	0
RESERVED				RESERVED			
R/W-X				R/W-X			

Table 598. R595 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	X	Reserved
3-0	RESERVED	R/W	X	Reserved

2.597 R596 Register (Address = 254h) [reset = X]

R596 is shown in Figure 597 and described in Table 599.

Return to Summary Table.

Figure 597. R596 Register

7	6	5	4	3	2	1	0
RESERVED				RESERVED			
R/W-X				R/W-X			

Table 599. R596 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	X	Reserved
4-0	RESERVED	R/W	X	Reserved

2.598 R597 Register (Address = 255h) [reset = X]

R597 is shown in Figure 598 and described in Table 600.

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Figure 598. R597 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 600. R597 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.599 R598 Register (Address = 256h) [reset = X]

R598 is shown in Figure 599 and described in Table 601.

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Figure 599. R598 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 601. R598 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.600 R599 Register (Address = 257h) [reset = X]

R599 is shown in Figure 600 and described in Table 602.

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Figure 600. R599 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 602. R599 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.601 R600 Register (Address = 258h) [reset = X]

R600 is shown in Figure 601 and described in Table 603.

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Figure 601. R600 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 603. R600 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.602 R601 Register (Address = 259h) [reset = 0h]

R601 is shown in Figure 602 and described in Table 604.

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Figure 602. R601 Register

7	6	5	4	3	2	1	0
RESERVED						RESERVED	
R-0h						R/W-0h	

Table 604. R601 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0h	
1-0	RESERVED	R/W	0h	Reserved

2.603 R602 Register (Address = 25Ah) [reset = X]

R602 is shown in Figure 603 and described in Table 605.

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Figure 603. R602 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 605. R602 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.604 R603 Register (Address = 25Bh) [reset = X]

R603 is shown in Figure 604 and described in Table 606.

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Figure 604. R603 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 606. R603 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.605 R604 Register (Address = 25Ch) [reset = X]

R604 is shown in Figure 605 and described in Table 607.

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Figure 605. R604 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 607. R604 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.606 R605 Register (Address = 25Dh) [reset = X]

R605 is shown in Figure 606 and described in Table 608.

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Figure 606. R605 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 608. R605 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.607 R606 Register (Address = 25Eh) [reset = X]

R606 is shown in Figure 607 and described in Table 609.

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Figure 607. R606 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 609. R606 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.608 R607 Register (Address = 25Fh) [reset = X]

R607 is shown in Figure 608 and described in Table 610.

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Figure 608. R607 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 610. R607 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.609 R608 Register (Address = 260h) [reset = X]

R608 is shown in Figure 609 and described in Table 611.

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Figure 609. R608 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 611. R608 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.610 R609 Register (Address = 261h) [reset = X]

R609 is shown in Figure 610 and described in Table 612.

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Figure 610. R609 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 612. R609 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.611 R610 Register (Address = 262h) [reset = X]

R610 is shown in Figure 611 and described in Table 613.

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Figure 611. R610 Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
R-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X

Table 613. R610 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	X	
6	RESERVED	R/W	X	Reserved
5	RESERVED	R/W	X	Reserved
4	RESERVED	R/W	X	Reserved
3	RESERVED	R/W	X	Reserved
2	RESERVED	R/W	X	Reserved
1	RESERVED	R/W	X	Reserved
0	RESERVED	R/W	X	Reserved

2.612 R611 Register (Address = 263h) [reset = X]

R611 is shown in Figure 612 and described in Table 614.

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Figure 612. R611 Register

7	6	5	4	3	2	1	0
RESERVED				RESERVED			
R/W-X				R/W-X			

Table 614. R611 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	X	Reserved
3-0	RESERVED	R/W	X	Reserved

2.613 R612 Register (Address = 264h) [reset = X]

R612 is shown in Figure 613 and described in Table 615.

Return to Summary Table.

Figure 613. R612 Register

7	6	5	4	3	2	1	0
RESERVED				RESERVED			
R/W-X				R/W-X			

Table 615. R612 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	X	Reserved
4-0	RESERVED	R/W	X	Reserved

2.614 R613 Register (Address = 265h) [reset = X]

R613 is shown in Figure 614 and described in Table 616.

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Figure 614. R613 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 616. R613 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.615 R614 Register (Address = 266h) [reset = X]

R614 is shown in Figure 615 and described in Table 617.

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Figure 615. R614 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 617. R614 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.616 R615 Register (Address = 267h) [reset = X]

R615 is shown in Figure 616 and described in Table 618.

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Figure 616. R615 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 618. R615 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.617 R616 Register (Address = 268h) [reset = X]

R616 is shown in Figure 617 and described in Table 619.

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Figure 617. R616 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 619. R616 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.618 R617 Register (Address = 269h) [reset = 0h]

R617 is shown in Figure 618 and described in Table 620.

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Figure 618. R617 Register

7	6	5	4	3	2	1	0
RESERVED						RESERVED	
R-0h						R/W-0h	

Table 620. R617 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0h	
1-0	RESERVED	R/W	0h	Reserved

2.619 R618 Register (Address = 26Ah) [reset = X]

R618 is shown in Figure 619 and described in Table 621.

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Figure 619. R618 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 621. R618 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.620 R619 Register (Address = 26Bh) [reset = X]

R619 is shown in Figure 620 and described in Table 622.

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Figure 620. R619 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 622. R619 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.621 R620 Register (Address = 26Ch) [reset = X]

R620 is shown in Figure 621 and described in Table 623.

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Figure 621. R620 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 623. R620 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.622 R621 Register (Address = 26Dh) [reset = X]

R621 is shown in Figure 622 and described in Table 624.

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Figure 622. R621 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 624. R621 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.623 R622 Register (Address = 26Eh) [reset = X]

R622 is shown in Figure 623 and described in Table 625.

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Figure 623. R622 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 625. R622 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.624 R623 Register (Address = 26Fh) [reset = X]

R623 is shown in Figure 624 and described in Table 626.

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Figure 624. R623 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 626. R623 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.625 R624 Register (Address = 270h) [reset = X]

R624 is shown in Figure 625 and described in Table 627.

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Figure 625. R624 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 627. R624 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.626 R625 Register (Address = 271h) [reset = X]

R625 is shown in Figure 626 and described in Table 628.

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Figure 626. R625 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 628. R625 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	X	Reserved

2.627 R626 Register (Address = 272h) [reset = X]

R626 is shown in Figure 627 and described in Table 629.

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Figure 627. R626 Register

7	6	5	4	3	2	1	0
RESERVED		DPLL1_TUNING_FREE_RUN[37:32]					
R-X		R/W-X					

Table 629. R626 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	
5-0	DPLL1_TUNING_FREE_RUN[37:32]	R/W	X	Bits 37:32 of DPLL1_TUNING_FREE_RUN

2.628 R627 Register (Address = 273h) [reset = X]

R627 is shown in Figure 628 and described in Table 630.

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Figure 628. R627 Register

7	6	5	4	3	2	1	0
DPLL1_TUNING_FREE_RUN[31:24]							
R/W-X							

Table 630. R627 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL1_TUNING_FREE_RUN[31:24]	R/W	X	Bits 31:24 of DPLL1_TUNING_FREE_RUN

2.629 R628 Register (Address = 274h) [reset = X]

R628 is shown in Figure 629 and described in Table 631.

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Figure 629. R628 Register

7	6	5	4	3	2	1	0
DPLL1_TUNING_FREE_RUN[23:16]							
R/W-X							

Table 631. R628 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL1_TUNING_FREE_RUN[23:16]	R/W	X	Bits 23:16 of DPLL1_TUNING_FREE_RUN

2.630 R629 Register (Address = 275h) [reset = X]

R629 is shown in Figure 630 and described in Table 632.

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Figure 630. R629 Register

7	6	5	4	3	2	1	0
DPLL1_TUNING_FREE_RUN[15:8]							
R/W-X							

Table 632. R629 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL1_TUNING_FREE_RUN[15:8]	R/W	X	Bits 15:8 of DPLL1_TUNING_FREE_RUN

2.631 R630 Register (Address = 276h) [reset = X]

R630 is shown in Figure 631 and described in Table 633.

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Figure 631. R630 Register

7	6	5	4	3	2	1	0
DPLL1_TUNING_FREE_RUN							
R/W-X							

Table 633. R630 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL1_TUNING_FREE_RUN	R/W	X	DPLL1 Free-run tuning word

2.632 R631 Register (Address = 277h) [reset = X]

R631 is shown in Figure 632 and described in Table 634.

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Figure 632. R631 Register

7	6	5	4	3	2	1	0
DPLL1_REF_HIST_INTMD				RESERVED	DPLL1_REF_HIST_HOLD	DPLL1_REF_HIST_SWRST	DPLL1_REF_HIST_EN
R/W-X				R-X	R/W-X	R/W-0h	R/W-X

Table 634. R631 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	DPLL1_REF_HIST_INTMD	R/W	X	Controls intermediate updates to DPLL1 REF tuning history Updates only occur during first averaging period Tavg after reset. Programming restriction: DPLL1_REF_HIST_INTMD <= DPLL1_REF_HISTCNT. 0h = No intermediate update 1h = 1 intermediate update at Tavg/2 2h = 2 intermediate update at Tavg/4, Tavg/2 3h = 3 intermediate updates at Tavg/8, Tavg/4, Tavg/2 Fh = 15 intermediate updates at $Tavg/2^K$ to Tavg/2 (K=0 to HIST_INTMD)
3	RESERVED	R	X	
2	DPLL1_REF_HIST_HOLD	R/W	X	DPLL1 REF Tuning History persistant bit If set, tuning history is not reset on holdover exit, switchover, or history software reset.
1	DPLL1_REF_HIST_SWRST	R/W	0h	Resets DPLL1 REF Tuning History if persistent bit not set
0	DPLL1_REF_HIST_EN	R/W	X	Enables DPLL1 REF tuning history monitor

2.633 R632 Register (Address = 278h) [reset = X]

R632 is shown in Figure 633 and described in Table 635.

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Figure 633. R632 Register

7	6	5	4	3	2	1	0
RESERVED			DPLL1_REF_HISTCNT				
R-X			R/W-X				

Table 635. R632 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	X	
4-0	DPLL1_REF_HISTCNT	R/W	X	DPLL1 REF Tuning History Timer Valid range is 0 to 30.

2.634 R633 Register (Address = 279h) [reset = X]

R633 is shown in Figure 634 and described in Table 636.

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Figure 634. R633 Register

7	6	5	4	3	2	1	0
RESERVED	DPLL1_REF_HISTDLY[30:24]						
R-X	R/W-X						

Table 636. R633 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	X	
6-0	DPLL1_REF_HISTDLY[30:24]	R/W	X	Bits 30:24 of DPLL1_REF_HISTDLY

2.635 R634 Register (Address = 27Ah) [reset = X]

R634 is shown in Figure 635 and described in Table 637.

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Figure 635. R634 Register

7	6	5	4	3	2	1	0
DPLL1_REF_HISTDLY[23:16]							
R/W-X							

Table 637. R634 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL1_REF_HISTDLY[23:16]	R/W	X	Bits 23:16 of DPLL1_REF_HISTDLY

2.636 R635 Register (Address = 27Bh) [reset = X]

R635 is shown in Figure 636 and described in Table 638.

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Figure 636. R635 Register

7	6	5	4	3	2	1	0
DPLL1_REF_HISTDLY[15:8]							
R/W-X							

Table 638. R635 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL1_REF_HISTDLY[15:8]	R/W	X	Bits 15:8 of DPLL1_REF_HISTDLY

2.637 R636 Register (Address = 27Ch) [reset = X]

R636 is shown in Figure 637 and described in Table 639.

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Figure 637. R636 Register

7	6	5	4	3	2	1	0
DPLL1_REF_HISTDLY							
R/W-X							

Table 639. R636 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL1_REF_HISTDLY	R/W	X	DPLL1 REF Tuning History delay REF_HISTDLY must be less than $2^{HISTCNT}$.

2.638 R637 Register (Address = 27Dh) [reset = X]

R637 is shown in Figure 638 and described in Table 640.

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Figure 638. R637 Register

7	6	5	4	3	2	1	0
RESERVED		DPLL2_TUNING_FREE_RUN[37:32]					
R-X		R/W-X					

Table 640. R637 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	X	
5-0	DPLL2_TUNING_FREE_RUN[37:32]	R/W	X	Bits 37:32 of DPLL2_TUNING_FREE_RUN

2.639 R638 Register (Address = 27Eh) [reset = X]

R638 is shown in Figure 639 and described in Table 641.

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Figure 639. R638 Register

7	6	5	4	3	2	1	0
DPLL2_TUNING_FREE_RUN[31:24]							
R/W-X							

Table 641. R638 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL2_TUNING_FREE_RUN[31:24]	R/W	X	Bits 31:24 of DPLL2_TUNING_FREE_RUN

2.640 R639 Register (Address = 27Fh) [reset = X]

R639 is shown in Figure 640 and described in Table 642.

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Figure 640. R639 Register

7	6	5	4	3	2	1	0
DPLL2_TUNING_FREE_RUN[23:16]							
R/W-X							

Table 642. R639 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL2_TUNING_FREE_RUN[23:16]	R/W	X	Bits 23:16 of DPLL2_TUNING_FREE_RUN

2.641 R640 Register (Address = 280h) [reset = X]

R640 is shown in Figure 641 and described in Table 643.

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Figure 641. R640 Register

7	6	5	4	3	2	1	0
DPLL2_TUNING_FREE_RUN[15:8]							
R/W-X							

Table 643. R640 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL2_TUNING_FREE_RUN[15:8]	R/W	X	Bits 15:8 of DPLL2_TUNING_FREE_RUN

2.642 R641 Register (Address = 281h) [reset = X]

R641 is shown in Figure 642 and described in Table 644.

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Figure 642. R641 Register

7	6	5	4	3	2	1	0
DPLL2_TUNING_FREE_RUN							
R/W-X							

Table 644. R641 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL2_TUNING_FREE_RUN	R/W	X	DPLL2 Free-run tuning word

2.643 R642 Register (Address = 282h) [reset = X]

R642 is shown in Figure 643 and described in Table 645.

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Figure 643. R642 Register

7	6	5	4	3	2	1	0
DPLL2_REF_HIST_INTMD				RESERVED	DPLL2_REF_HIST_HOLD	DPLL2_REF_HIST_SWRST	DPLL2_REF_HIST_EN
R/W-X				R-X	R/W-X	R/W-0h	R/W-X

Table 645. R642 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	DPLL2_REF_HIST_INTMD	R/W	X	Controls intermediate updates to DPLL2 REF tuning history Updates only occur during first averaging period Tavg after reset. Programming restriction: DPLL2_REF_HIST_INTMD <= DPLL2_REF_HISTCNT. 0h = No intermediate update 1h = 1 intermediate update at Tavg/2 2h = 2 intermediate update at Tavg/4, Tavg/2 3h = 3 intermediate updates at Tavg/8, Tavg/4, Tavg/2 Fh = 15 intermediate updates at Tavg/2^K to Tavg/2 (K=0 to HIST_INTMD)
3	RESERVED	R	X	
2	DPLL2_REF_HIST_HOLD	R/W	X	DPLL2 REF Tuning History persistant bit If set the tuning history is not reset on holdover exit, switchover or history software reset.
1	DPLL2_REF_HIST_SWRST	R/W	0h	Resets DPLL2 REF Tuning History if persistent bit not set
0	DPLL2_REF_HIST_EN	R/W	X	Enables DPLL2 REF tuning history monitor

2.644 R643 Register (Address = 283h) [reset = X]

R643 is shown in Figure 644 and described in Table 646.

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Figure 644. R643 Register

7	6	5	4	3	2	1	0
RESERVED				DPLL2_REF_HISTCNT			
R-X				R/W-X			

Table 646. R643 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	X	
4-0	DPLL2_REF_HISTCNT	R/W	X	DPLL2 REF Tuning History Timer Valid range is 0 to 30.

2.645 R644 Register (Address = 284h) [reset = X]

R644 is shown in Figure 645 and described in Table 647.

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Figure 645. R644 Register

7	6	5	4	3	2	1	0
RESERVED	DPLL2_REF_HISTDLY[30:24]						
R-X	R/W-X						

Table 647. R644 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	X	
6-0	DPLL2_REF_HISTDLY[30:24]	R/W	X	Bits 30:24 of DPLL2_REF_HISTDLY

2.646 R645 Register (Address = 285h) [reset = X]

R645 is shown in Figure 646 and described in Table 648.

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Figure 646. R645 Register

7	6	5	4	3	2	1	0
DPLL2_REF_HISTDLY[23:16]							
R/W-X							

Table 648. R645 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL2_REF_HISTDLY[23:16]	R/W	X	Bits 23:16 of DPLL2_REF_HISTDLY

2.647 R646 Register (Address = 286h) [reset = X]

R646 is shown in Figure 647 and described in Table 649.

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Figure 647. R646 Register

7	6	5	4	3	2	1	0
DPLL2_REF_HISTDLY[15:8]							
R/W-X							

Table 649. R646 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL2_REF_HISTDLY[15:8]	R/W	X	Bits 15:8 of DPLL2_REF_HISTDLY

2.648 R647 Register (Address = 287h) [reset = X]

R647 is shown in Figure 648 and described in Table 650.

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Figure 648. R647 Register

7	6	5	4	3	2	1	0
DPLL2_REF_HISTDLY							
R/W-X							

Table 650. R647 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL2_REF_HISTDLY	R/W	X	DPLL2 REF Tuning History delay REF_HISTDLY must be less than $2^{HISTCNT}$.

2.649 R676 Register (Address = 2A4h) [reset = 0h]

R676 is shown in Figure 649 and described in Table 651.

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Figure 649. R676 Register

7	6	5	4	3	2	1	0
RESERVED		SWRCH					
R-0h		R/W1C-0h					

Table 651. R676 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	
5-0	SWRCH	R/W1C	0h	Software Reset Output Channels Allows the Output Channel dividers to be reset. 0h = CH0 1h = CH1 2h = CH23 3h = CH45 4h = CH6 5h = CH7

2.650 R677 Register (Address = 2A5h) [reset = 0h]

R677 is shown in Figure 650 and described in Table 652.

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Figure 650. R677 Register

7	6	5	4	3	2	1	0
RESERVED						SWR2PLL	SWR1PLL
R-0h						R/W1C-0h	R/W1C-0h

Table 652. R677 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0h	
1	SWR2PLL	R/W1C	0h	Software Reset PLL2 Setting SWR2PLL to 1 resets the PLL2 Calibrator, the PLL2 N Divider, R Divider and VCO Divider. The PLL2 Calibrator then takes control of the N Divider reset. This bit is automatically cleared to 0. It does not reset the divider driving the CMOS Outputs.
0	SWR1PLL	R/W1C	0h	Software Reset PLL1 Setting SWR1PLL to 1 resets the PLL1 Calibrator, the PLL1 N Divider, R Divider and VCO Divider. The PLL1 Calibrator then takes control of the N Divider reset. This bit is automatically cleared to 0. It does not reset the divider driving the CMOS Outputs.

2.651 R678 Register (Address = 2A6h) [reset = X]

R678 is shown in Figure 651 and described in Table 653.

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Figure 651. R678 Register

7	6	5	4	3	2	1	0
RESERVED				RESERVED			
R/W-X				R-X			

Table 653. R678 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	X	Reserved
4-0	RESERVED	R	X	

2.652 R681 Register (Address = 2A9h) [reset = X]

R681 is shown in Figure 652 and described in Table 654.

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Figure 652. R681 Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED			RESERVED	RESERVED		
R-X	R/W-X			R-X	R/W-X		

Table 654. R681 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	X	
6-4	RESERVED	R/W	X	Reserved
3	RESERVED	R	X	
2-0	RESERVED	R/W	X	Reserved

2.653 R682 Register (Address = 2AAh) [reset = X]

R682 is shown in Figure 653 and described in Table 655.

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Figure 653. R682 Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED			RESERVED	RESERVED		
R/W-X	R/W-X			R-X	R/W-X		

Table 655. R682 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	X	Reserved
6-4	RESERVED	R/W	X	Reserved
3	RESERVED	R	X	
2-0	RESERVED	R/W	X	Reserved

2.654 R683 Register (Address = 2ABh) [reset = X]

R683 is shown in Figure 654 and described in Table 656.

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Figure 654. R683 Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED			RESERVED	RESERVED		
R-X	R/W-X			R-X	R/W-X		

Table 656. R683 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	X	
6-4	RESERVED	R/W	X	Reserved
3	RESERVED	R	X	
2-0	RESERVED	R/W	X	Reserved

2.655 R684 Register (Address = 2ACh) [reset = X]

R684 is shown in Figure 655 and described in Table 657.

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Figure 655. R684 Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED			RESERVED	RESERVED		
R-X	R/W-X			R-X	R/W-X		

Table 657. R684 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	X	
6-4	RESERVED	R/W	X	Reserved
3	RESERVED	R	X	
2-0	RESERVED	R/W	X	Reserved

2.656 R685 Register (Address = 2ADh) [reset = X]

R685 is shown in Figure 656 and described in Table 658.

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Figure 656. R685 Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED			RESERVED	RESERVED		
R-X	R/W-X			R-X	R/W-X		

Table 658. R685 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	X	
6-4	RESERVED	R/W	X	Reserved
3	RESERVED	R	X	

Table 658. R685 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	RESERVED	R/W	X	Reserved

2.657 R686 Register (Address = 2AEh) [reset = X]

R686 is shown in Figure 657 and described in Table 659.

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Figure 657. R686 Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED			RESERVED	RESERVED		
R-X	R/W-X			R-X	R/W-X		

Table 659. R686 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	X	
6-4	RESERVED	R/W	X	Reserved
3	RESERVED	R	X	
2-0	RESERVED	R/W	X	Reserved

2.658 R687 Register (Address = 2AFh) [reset = X]

R687 is shown in Figure 658 and described in Table 660.

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Figure 658. R687 Register

7	6	5	4	3	2	1	0
RESERVED					RESERVED		
R-X					R/W-X		

Table 660. R687 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	X	
2-0	RESERVED	R/W	X	Reserved

2.659 R688 Register (Address = 2B0h) [reset = X]

R688 is shown in Figure 659 and described in Table 661.

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Figure 659. R688 Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED			RESERVED	RESERVED		
R-X	R/W-X			R-X	R/W-X		

Table 661. R688 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	X	
6-4	RESERVED	R/W	X	Reserved
3	RESERVED	R	X	
2-0	RESERVED	R/W	X	Reserved

2.660 R691 Register (Address = 2B3h) [reset = X]

R691 is shown in Figure 660 and described in Table 662.

Return to Summary Table.

Figure 660. R691 Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X

Table 662. R691 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	X	Reserved
6	RESERVED	R/W	X	Reserved
5	RESERVED	R/W	X	Reserved
4	RESERVED	R/W	X	Reserved
3	RESERVED	R/W	X	Reserved
2	RESERVED	R/W	X	Reserved
1	RESERVED	R/W	X	Reserved
0	RESERVED	R/W	X	Reserved

2.661 R715 Register (Address = 2CBh) [reset = X]

R715 is shown in Figure 661 and described in Table 663.

Return to Summary Table.

Figure 661. R715 Register

7	6	5	4	3	2	1	0
RESERVED				RESERVED			
R-X				R/W-X			

Table 663. R715 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	X	
3-0	RESERVED	R/W	X	Reserved

2.662 R716 Register (Address = 2CCh) [reset = X]

R716 is shown in Figure 662 and described in Table 664.

Return to Summary Table.

Figure 662. R716 Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED				RESERVED	RESERVED	
R/W-X	R-X				R/W-X	R-X	

Table 664. R716 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	X	Reserved
6-3	RESERVED	R	X	
2	RESERVED	R/W	X	Reserved
1-0	RESERVED	R	X	

2.663 R717 Register (Address = 2CDh) [reset = X]

R717 is shown in Figure 663 and described in Table 665.

Return to Summary Table.

Figure 663. R717 Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED				RESERVED	RESERVED	
R/W-X	R-X				R/W-X	R-X	

Table 665. R717 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	X	Reserved
6-3	RESERVED	R	X	
2	RESERVED	R/W	X	Reserved
1-0	RESERVED	R	X	

2.664 R718 Register (Address = 2CEh) [reset = X]

R718 is shown in Figure 664 and described in Table 666.

Return to Summary Table.

Figure 664. R718 Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED				RESERVED	RESERVED	
R/W-X	R-X				R/W-X	R-X	

Table 666. R718 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	X	Reserved
6-3	RESERVED	R	X	
2	RESERVED	R/W	X	Reserved
1-0	RESERVED	R	X	

2.665 R719 Register (Address = 2CFh) [reset = X]

R719 is shown in Figure 665 and described in Table 667.

Return to Summary Table.

Figure 665. R719 Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED				RESERVED	RESERVED	
R/W-X	R-X				R/W-X	R-X	

Table 667. R719 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	X	Reserved
6-3	RESERVED	R	X	
2	RESERVED	R/W	X	Reserved
1-0	RESERVED	R	X	

2.666 R736 Register (Address = 2E0h) [reset = 0h]

R736 is shown in Figure 666 and described in Table 668.

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Figure 666. R736 Register

7	6	5	4	3	2	1	0
RESERVED			OCXO_MDIV_STATUS_OUT_SEL		RESERVED		
R-0h			R/W-0h		R-0h		

Table 668. R736 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	
4-3	OCXO_MDIV_STATUS_OUT_SEL	R/W	0h	When the DPLL TCXO MDIV is selected by a status output, this bit field selects the output signal routed to the pin. 0h = Disabled 1h = TCXO M Divider output 2h = VCO 1 Loopback (FBCLK) 3h = VCO2 Loopback (FBCLK)
2-0	RESERVED	R	0h	

2.667 R741 Register (Address = 2E5h) [reset = 0h]

R741 is shown in Figure 667 and described in Table 669.

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Figure 667. R741 Register

7	6	5	4	3	2	1	0
RESERVED			RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
R-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 669. R741 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	
4	RESERVED	R/W	0h	Reserved
3	RESERVED	R/W	0h	Reserved
2	RESERVED	R/W	0h	Reserved
1	RESERVED	R/W	0h	Reserved
0	RESERVED	R/W	0h	Reserved

2.668 R742 Register (Address = 2E6h) [reset = 0h]

R742 is shown in Figure 668 and described in Table 670.

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Figure 668. R742 Register

7	6	5	4	3	2	1	0
REF3VALSTAT	REF2VALSTAT	REF1VALSTAT	REF0VALSTAT	RESERVED			
R-0h	R-0h	R-0h	R-0h	R-0h			

Table 670. R742 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	REF3VALSTAT	R	0h	REFx valid state 1h = valid.
6	REF2VALSTAT	R	0h	REFx valid state 1h = valid.
5	REF1VALSTAT	R	0h	REFx valid state 1h = valid.
4	REF0VALSTAT	R	0h	REFx valid state 1h = valid.
3-0	RESERVED	R	0h	

2.669 R764 Register (Address = 2FCh) [reset = 0h]

R764 is shown in Figure 669 and described in Table 671.

Return to Summary Table.

Figure 669. R764 Register

7	6	5	4	3	2	1	0
RESERVED				RESERVED	RESERVED	RESERVED	RESERVED
R-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 671. R764 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	
3	RESERVED	R/W	0h	Reserved
2	RESERVED	R/W	0h	Reserved
1	RESERVED	R/W	0h	Reserved
0	RESERVED	R/W	0h	Reserved

2.670 R766 Register (Address = 2FEh) [reset = 0h]

R766 is shown in Figure 670 and described in Table 672.

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Figure 670. R766 Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 672. R766 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0h	Reserved
6	RESERVED	R/W	0h	Reserved
5	RESERVED	R/W	0h	Reserved
4	RESERVED	R/W	0h	Reserved
3	RESERVED	R/W	0h	Reserved
2	RESERVED	R/W	0h	Reserved
1	RESERVED	R/W	0h	Reserved
0	RESERVED	R/W	0h	Reserved

2.671 R767 Register (Address = 2FFh) [reset = 0h]

R767 is shown in Figure 671 and described in Table 673.

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Figure 671. R767 Register

7	6	5	4	3	2	1	0
RESERVED		DPLL1_REFSEL_STAT					
R-0h		R-0h					

Table 673. R767 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	
5-0	DPLL1_REFSEL_STAT	R	0h	Reads the DPLL1 Reference Select Control bits 0h = Holdover 1h = Reference 0 2h = Reference 1 4h = Reference 2 8h = Reference 3 20h = VCO2 Loopback (FBCLK)

2.672 R770 Register (Address = 302h) [reset = 0h]

R770 is shown in Figure 672 and described in Table 674.

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Figure 672. R770 Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 674. R770 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0h	Reserved
6	RESERVED	R/W	0h	Reserved
5	RESERVED	R/W	0h	Reserved
4	RESERVED	R/W	0h	Reserved
3	RESERVED	R/W	0h	Reserved
2	RESERVED	R/W	0h	Reserved
1	RESERVED	R/W	0h	Reserved
0	RESERVED	R/W	0h	Reserved

2.673 R771 Register (Address = 303h) [reset = 0h]

R771 is shown in Figure 673 and described in Table 675.

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Figure 673. R771 Register

7	6	5	4	3	2	1	0
RESERVED		DPLL2_REFSEL_STAT					
R-0h		R-0h					

Table 675. R771 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	
5-0	DPLL2_REFSEL_STAT	R	0h	Reads the DPLL2 Reference Select Control bits 0h = Holdover 1h = Reference 0 2h = Reference 1 4h = Reference 2 8h = Reference 3 10h = VCO1 Loopback (FBCLK)

2.674 R775 Register (Address = 307h) [reset = X]

R775 is shown in Figure 674 and described in Table 676.

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Figure 674. R775 Register

7	6	5	4	3	2	1	0
RESERVED				RESERVED	RESERVED		
R-X				R/W-X	R-X		

Table 676. R775 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	X	
3	RESERVED	R/W	X	Reserved
2-0	RESERVED	R	X	

2.675 R776 Register (Address = 308h) [reset = X]

R776 is shown in Figure 675 and described in Table 677.

Return to Summary Table.

Figure 675. R776 Register

7	6	5	4	3	2	1	0
RESERVED							RESERVED
R-X							R/W-X

Table 677. R776 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	X	
0	RESERVED	R/W	X	Reserved

2.676 R784 Register (Address = 310h) [reset = X]

R784 is shown in Figure 676 and described in Table 678.

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Figure 676. R784 Register

7	6	5	4	3	2	1	0
RESERVED				RESERVED	RESERVED		
R-X				R/W-X	R-X		

Table 678. R784 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	X	
3	RESERVED	R/W	X	Reserved
2-0	RESERVED	R	X	

2.677 R785 Register (Address = 311h) [reset = X]

R785 is shown in Figure 677 and described in Table 679.

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Figure 677. R785 Register

7	6	5	4	3	2	1	0
RESERVED							RESERVED
R-X							R/W-X

Table 679. R785 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	X	
0	RESERVED	R/W	X	Reserved

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