# SIGNAL PATH designer℠

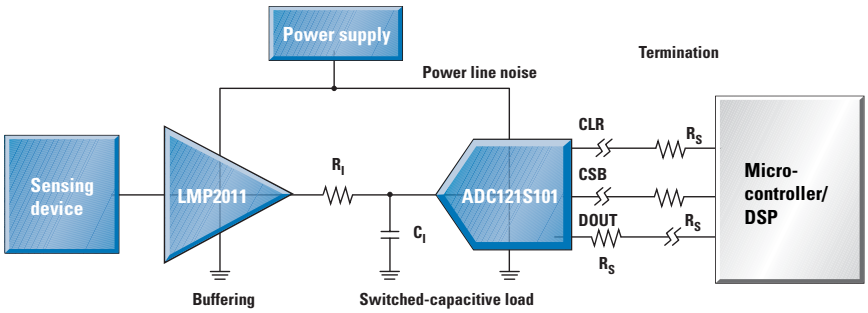
*Tips, tricks, and techniques from the signal-path experts*

No. 102




## Maximizing Signal-Path Performance

*— By Chuck Sins, Applications Engineer*




**Precision Signal Path**

The signal path offers many opportunities for the system designer. In the analog-to-digital converter (ADC) signal path, making good design choices in buffering a sensing device, charging the switch-capacitive input of an ADC, and minimizing noise sources will maximize performance. All of these examples will be addressed in this issue of the *Signal Path Designer.*

### Buffering a Sensing Device

When a sensing device is unable to drive the capacitive load of an ADC, it can be buffered with an operational amplifier (op amp). Since many applications require operation from a single supply, it is important to select an op amp that operates at the same voltage as the ADC. While sharing supply voltages helps reduce system complexity and cost, supply voltages place constraints on the input and output capability of the op amp. For ADCs such as the ADC121S101 where the reference voltage ($V_{REF}$) is both the supply voltage and the reference, op amps such as the LMP2011 with rail-to-rail output (RRO) capability are preferred. The LMP2011 with RRO capability allows the system designer to utilize the full dynamic range of the ADC, providing access to all of the output codes.

Once an op amp with suitable input/output capabilities has been selected, its gain bandwidth needs to be considered. For cases where the stimulus source's maximum output is less than $V_{REF}$, gain may be required from the buffering stage. The gain bandwidth product (GBWP) of an op amp specifies its band-

**NEXT ISSUE:**
**High-Speed Signals, Clocks, and Data Capture**

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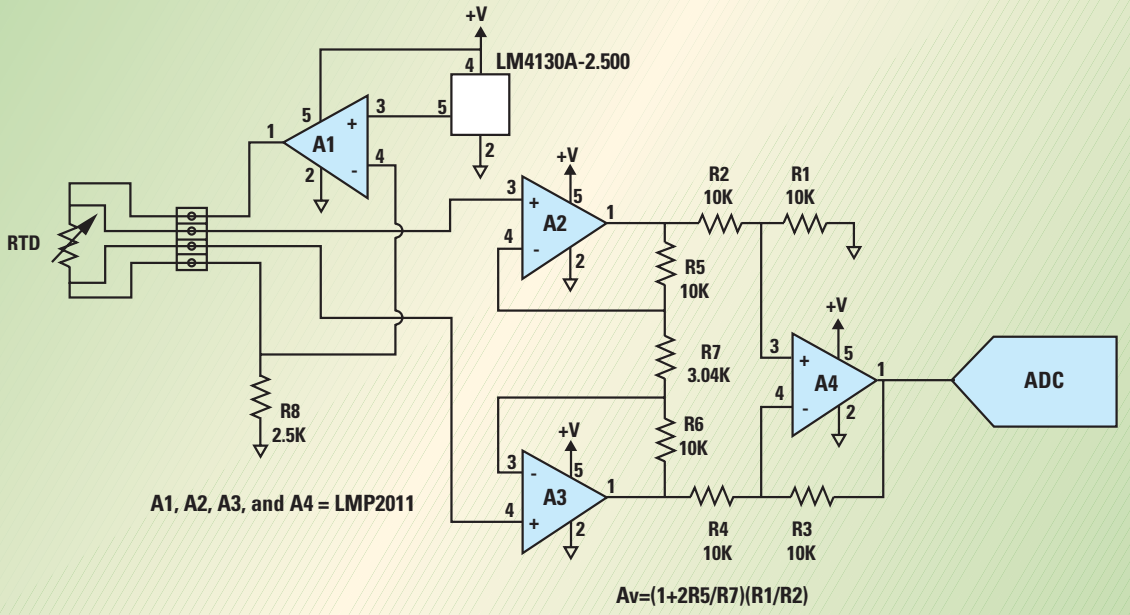
# High Precision-Rail-to-Rail Output Amplifiers


## Delivering High Precision Over Time and Temperature

### LMP2011 Typical Application Diagram




| LMP2011/12/14 Key Features | System Benefits |
|---|---|
| • 60 µV $V_{OS}$ max over temp (- 40°C to +125°C ) | • Offers high accuracy measurements with continued accuracy over temperature |
| • Low voltage noise (35 nV/$\sqrt{Hz}$) and no 1/f | • Increase signal accuracy during low frequency measurements |
| • High CMRR (130 dB), PSRR (120 dB) | • High accuracy across voltages |
| • Gain (130 dB) and 3 MHz GBW product | • Wide frequency range at higher gains |

# Maximizing Signal-Path Performance

width (-3 dB frequency) when configured as a unity gain amplifier. Since GBWP remains constant for a given op amp, a closed loop configuration with a gain of $A_{CL}$ lowers the bandwidth by a factor of $A_{CL}$: $BW = \frac{GBWP}{A_{CL}}$

For example, the LMP2011 with a GBWP of 3 MHz will have a bandwidth of 300 kHz when configured with an $A_{CL}$ of 10 V/V.

Because the closed-loop bandwidth is the -3 dB frequency of the amplifier, it is the frequency where the amplifier output is 70.7% of its input value. So at the –3 dB frequency there is a 29.3% error in output amplitude. Errors in ADCs are measured in units of least significant bits (LSBs). One LSB is defined as $V_{REF}/2^n$ where $V_{REF}$ is the reference voltage and n is the ADC resolution. For example, 1 LSB of an 8-bit ADC is $V_{REF}/256$. For a system requiring $^1/_2$ LSB of accuracy from its ADC, the input stimulus must have gain accuracy of $(1-1/2^{n+1})$ or 99.8% for an 8-bit ADC. To guarantee that the op amp has sufficient gain accuracy for a given system requirement, it is necessary to calculate the maximum operating frequency ($f_{max}$) for the op amp. This is accomplished by approximating the frequency response of an op amp to be that of a single pole filter. The curve shown in ***Figure 1*** has the gain ($A_V$) and -3 dB frequency ($f_o$) normalized to 1.

The expression for this curve is

$$A_V = \frac{1}{\sqrt{1+(f)^2}}.$$

or solving for f,

$$f = \sqrt{\frac{1}{A_V^2} - 1}.$$

To achieve $^1/_2$ LSB of error from an 8-bit system, the normalized $f_{max}$ of an op amp is

$$f = \sqrt{\frac{1}{(0.998)^2} - 1} = 0.062 \cdot$$

Therefore, for an 8-bit ADC with a $^1/_2$ LSB accuracy requirement, the op amp's effective bandwidth is 0.062 x GBWP. The LMP2011 with a GBWP of 3 MHz would have an effective bandwidth of 186 kHz when configured for unity gain. The effective bandwidth is further reduced if a gain greater than unity is required. The normalized $f_{max}$ for

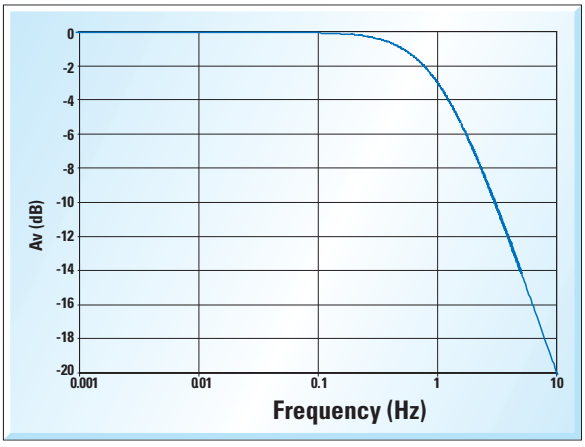



**Figure 1. Op-Amp Frequency Response**

$^1/_2$ LSB of error for ADCs of various resolutions can be calculated as: $\text{Normalized } f_{max} = \sqrt{\frac{1}{\left(1-\frac{1}{2^{n+1}}\right)^2} - 1}.$

## Transferring Charge to a Switched-Capacitive Load

The op amp was added to the ADC signal path to drive the capacitive load. However, the ADC's input is a switched-capacitive load *(see Figure 2)*.

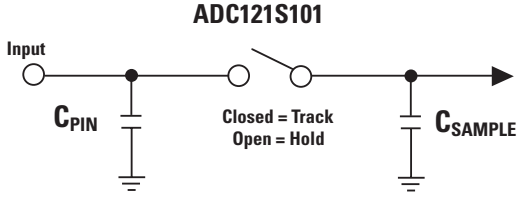
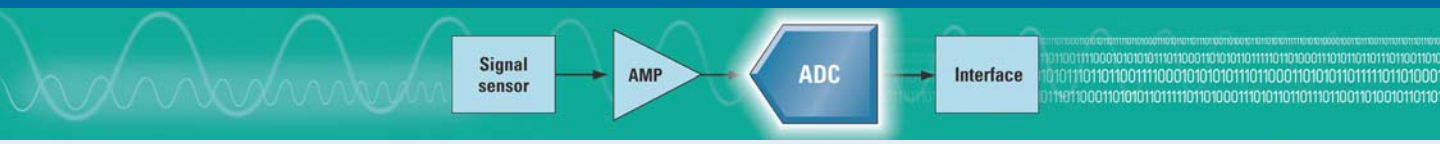


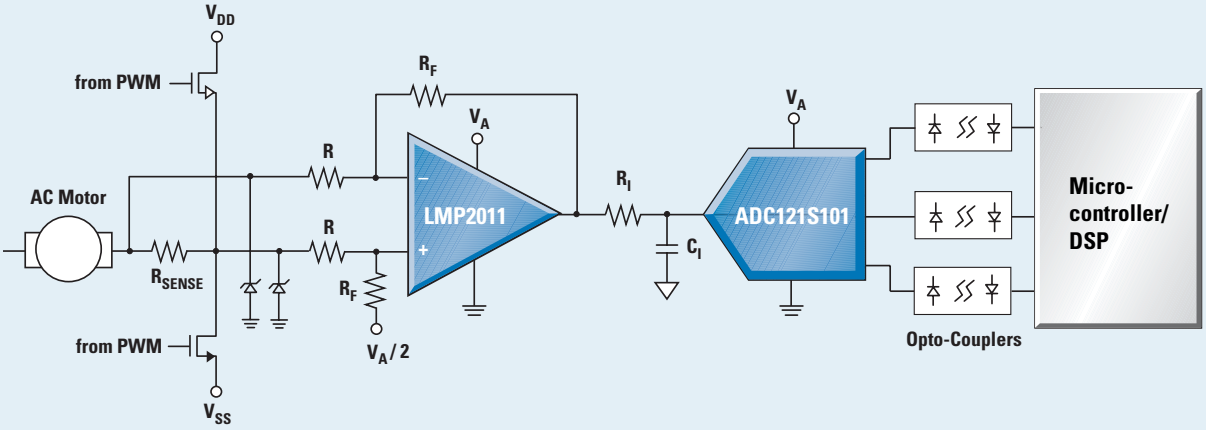

**Figure 2. ADC121S101 Input**

The ADC121S101 in "hold" mode has an input capacitance, $C_{PIN}$, of less than 4 pF, and in "track" mode has an input capacitance, $C_{SAMPLE}$ plus $C_{PIN}$, of less than 30 pF. To minimize the error caused by the changing input capacitance, a capacitor ($C_I$) is connected from the input pin to ground. The $C_I$, which is much larger than the input capacitance of the ADC when in "track" mode, provides the current to quickly charge the ADC's sampling capacitor. An isolation resistor is generally added to isolate the additional load capacitance from the op-amp output *(see Figure 3)*.

# Low power, high precision 8/10/12-bit, 1 MSPS ADCs




## ADC121S101 Typical Application Diagram

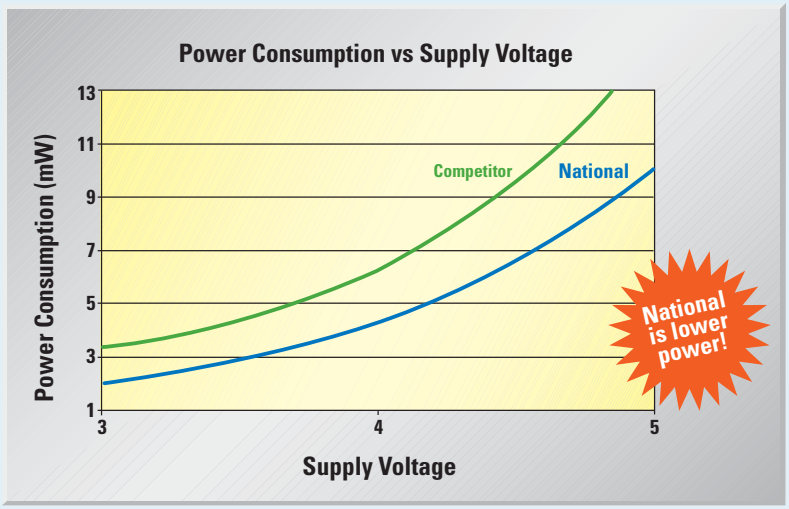



### ADC121S101, ADC101S101, and ADC081S10 Features (typical)

- Speed range: 500 KSPS to 1 MSPS
- Integral non-linearity (INL): ±0.4 LSB
- Differential non-linearity (DNL): ±0.5 LSB
- Signal-to-noise ratio (SNR): 72.5 dB
- Signal-to-noise and distortion ratio (SINAD): 72 dB
- Spurious free dynamic range (SFDR): 82 dB
- Power consumption: 2 mW at 3V
- Supply voltage: 2.7 to 5.25V

### Family Benefits

- Guaranteed performance over speed
- Pin and function compatible family
- Excellent static and dynamic performance
- Extremely low power
- Miniature packages reduce board space



# Maximizing Signal-Path Performance

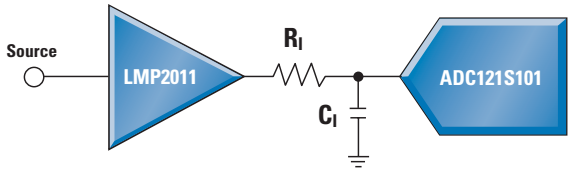



**Figure 3. Quick-Charge Circuit**

There are three important factors to consider in choosing appropriate values for the RC network. First, the designer needs to be aware that the RC network forms a low pass filter in the signal path. Therefore, the network can attenuate the sampled signal as the input frequency approaches the pole defined by $\frac{1}{2\pi RC}$. This is extremely critical for applications where ADC gain is important and no gain-calibration scheme is employed. Second, refrain from making the series resistor too large. While an increased resistance value decreases the phase delay at the output of the op amp (maintaining op-amp stability), it prevents the parallel combination of internal and external capacitance at the ADC input from fully charging during the ADC "track" time. Typical resistor values are less than 100 ohms. Third, make the external capacitor many times larger than the input capacitance while in "track" mode. Achieving this will minimize the drop in voltage on the capacitor when the ADC switches from "hold" to "track" mode.

The settling-time requirement of the op amp is determined by the amount of time the ADC spends in "track" mode. This is the amount of time that the op amp has to replenish the charge and reestablish the voltage on the capacitor prior to the ADC switching to "hold" mode. The time constant for recharging the capacitance at the input pin is defined by the series resistance value and the parallel combination of the internal and external capacitances. If the op amp fails to stabilize the voltage at the input by the time the ADC enters "hold" mode, inconsistent and erroneous conversions will result.

As a starting point for selecting values for $R_I$ and $C_I$, the pole of the RC network may be set to the sampling frequency of the ADC. If this causes too much attenuation for the highest input frequency, the designer can decrease the capacitance or resistance values accordingly. The minimum resistor value should be set by the output drive capability of the op amp. Smaller resistor values are preferred since they limit distortion. However, the amplifier stability must be guaranteed over the full input frequency range, amplitude, and temperature of the application.

## Managing Component Tolerance

If an inverting amplifier is used for the amplifier configuration ***(see Figure 4)***, it is easy to calculate the error coefficient due to component tolerance. Since the gain is defined as $-R_F/R_G$, the maximum deviation from the ideal will occur when $R_F$ is maximum and $R_G$ is minimum or when $R_F$ is minimum and $R_F$ is maximum. If resistors with a tolerance of 1% are used, the maximum error will be 2%.

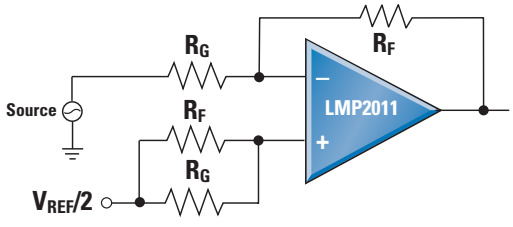



**Figure 4. Inverting Amplifier Configuration**

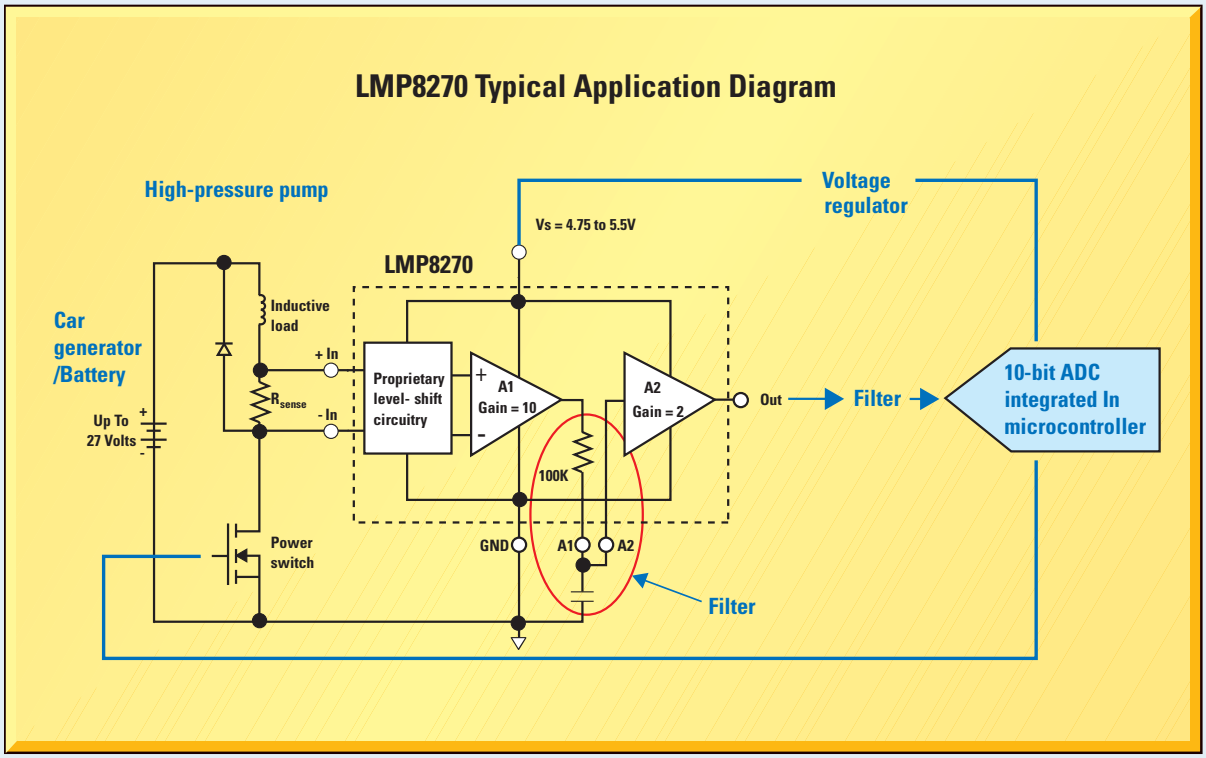
Applications where gain calibration schemes are not utilized must limit the dynamic range of the ADC. For an 8-bit ADC, 1 LSB represents 0.39% of $V_{REF}$ ($V_{REF}$ /$2^n$). Therefore, a 2% gain error due to resistor tolerance equates to a 12 LSB loss in dynamic range, 6 LSB (rounded up from 5.13) from the maximum output code and 6 LSB from the minimum.

## Minimizing Power Line Noise

While component tolerance is one source of error in the ADC signal path, noise on power lines due to digital circuitry is another. Noise can couple into an ADC and an op amp through their supply pins. Typically, devices such as the LMP2011 have excellent power supply rejection ratios (PSRR) and will not be affected. However, ADCs such as the

# High Common Mode, Voltage-Difference Amplifier


## Precision Current Measurement in Automotive and Industrial Environments




| LMP8270 Key Features | System Benefits |
|---|---|
| • Input offset voltage 1 mV max | • Initial system accuracy |
| • TCVos 15 µV/°C max | • Continued accuracy over temperature |
| • CMRR 80 dB min | • Accurate under wide dynamic input currents |
| • Extended CMVR -2V to 36V | • Supports a wide range of input voltages |
| • Output voltage swing rail-to-rail | • Supports ADC input voltage levels |
| • Supply voltage 4.75V to 5.5V | • Compatible with ADC voltage supplies |
| • Temp range -40°C to 125°C | • Supports most automotive/industrial applications |
| • Supply current 1 mA | • Minimum power consumption |

# Maximizing Signal-Path Performance

ADC121S101 whose supply voltage is also the $V_{REF}$ have a PSRR value of 0 dB (no PSRR). The output drivers of the ADC itself have fast edge rates that cause the ADC to draw varying amounts of current. The noise introduced on the supply line can upset the ADC and other analog circuitry connected to it. A dual capacitor decoupling scheme with the smallest capacitor, typically 0.1 µF, placed within 1 cm of the supply pin and a 1.0 µF to 10 µF capacitor placed nearby is an excellent starting place for limiting supply noise. If analog and digital supply pins are connected to the same voltage source, a choke may be used between the pins. The choke will appear as a short at DC and a resistor at the higher frequencies where isolation is desired.

While good supply decoupling is always recommended, it is best to try and minimize the load capacitance seen by the output of the ADC so less current is required. Charging load capacitance causes noise spikes on the supply line while discharging load capacitance adds noise to the ADC substrate. There are several techniques to minimize load capacitance. The easiest way is to drive only a single device and place it as close as possible to the ADC output. It is also helpful to limit the effect of driving load capacitance by using series resistors, which limit the current required to charge or discharge the load capacitance and reduce the slew rate of the output. Limit the value of the series resistance to less than 100Ω to avoid violating the timing requirements of the digital circuitry. High-frequency systems may not tolerate the use of series resistors. Thus, it is essential that the driven circuitry be very close to the ADC output.

## Maximizing Clock Integrity

Similar to ADC outputs, the ADC clock line can add noise to the system. The clock line should be treated as a transmission line when its length exceeds its rise time divided by 6 times the trace delay:

$$\text{line length} > \frac{t_{rise}}{6 \times t_{delay}}.$$

Trace delay is typically 150 ps per inch on an FR4 board. Treating a trace as a transmission line involves making the trace a controlled impedance with proper termination. This will help avoid signal reflection that can cause distortion. Distortion of the clock waveform leads to changes in the cycle-to-cycle clock period, better known as jitter. As the clock timing changes, there is variation in the exact point an ADC samples the waveform. With jitter, the ADC samples a point higher or lower on the signal than it ideally would. The net result of the time variation in the signal sampling point is noise. The maximum amount of jitter allowed for 1 LSB of error is $\frac{1}{2\pi f_{in}}$. For half an LSB of error, replace n with n+1.

Another technique for avoiding line reflection is line termination. There are two methods for terminating traces, near-end and far-end termination. Near-end termination requires a resistor in series with the line located close to the output of the signal source. The signal source resistance plus this series resistor should equal the characteristic impedance of the line. When near-end termination is insufficient, far-end termination is required. Far-end termination requires a resistor to ground at the clock input to the ADC. The terminating resistor is placed very close to the ADC input pin and the value should equal the characteristic impedance of the line.

When the clock source is required to drive multiple inputs, far-end termination alone may not be satisfactory. Far-end termination attenuates the signal level. Driving several inputs, each with a terminating resistor, may attenuate the clock voltage to the point that the logic thresholds are no longer met. For this instance, AC-termination is more appropriate. AC-termination requires a resistor in series with a capacitor to ground at the input to the ADC. This attenuates the AC component but not the DC component. For example, a signal that swings from 0 to 5V would remain centered around 2.5V in a system that is AC-terminated. The clock would still be attenuated but would be optimally centered between the CMOS trip points, allowing minimum signal swing to meet logic level-specifications.

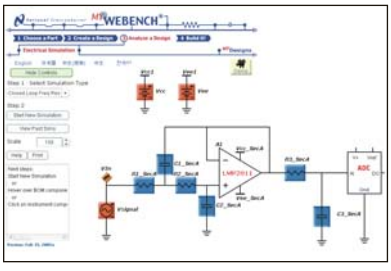
## Summary

By making smart design choices in buffering a sensing device, charging the switch-capacitive input of an ADC, and minimizing noise sources, the performance of the analog signal path is maximized. ■

# Design Tools

***INTRODUCING...***

## Signal-Path Design Tool

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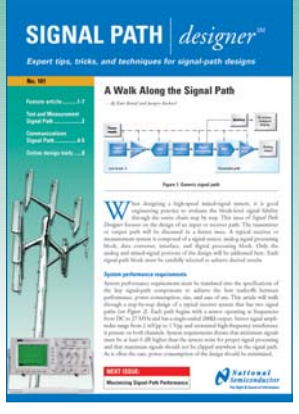


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