How to cut PLC output power dissipation in half using an adaptive supply

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The 4-20 mA current loop is a common signaling scheme for control systems. Field transmitters send sensor readings as 4-20 mA signals, and programmable logic controller (PLC) 4-20 mA outputs control many actuators. Increased channel count for PLC modules is a major industrial trend but creates a challenge for PLC current output modules because of power dissipation.

The output stage of the PLC current output channel shown in **Figure 1** is powered by a supply voltage (VS) and connected to an external load (RL). If the maximum RL specified is 800Ω and the assumed headroom voltage (VH) is 4V, for driving 20mA, Vs needs to be ≥20V.

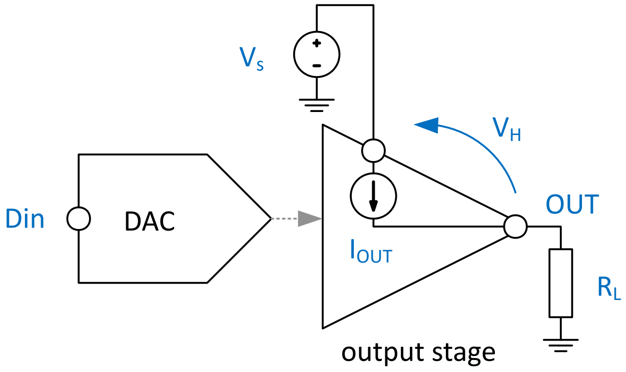


***Figure 1.** Power losses at the output stage.*

If you connect the same module to a small load or short circuit, the power loss within the channel will be VH × 20mA = 0.4W. This is quite high. Many modules limit the maximum load to 600Ω to reduce overall power losses. Derating the module output is another approach that manufacturers use, where the ambient temperature determines how many channels the user can enable, and the maximum current in each.

Equation 1 calculates power loss in the output stage.

$$P_{loss} = I_{OUT}(V_s - R_L I_{OUT}) \tag{1}$$

Note

The most convenient approach to adaptive power is to use a DAC that intrinsically supports adaptive power and integrates the output stage. TI's one-channel DAC8771 and four-channel DAC8775 integrate a buck-boost converter per channel with VS between 12V and 36V, generating both negative and positive variable supplies (with a maximum span of 36V) using a single external inductor per channel.

Choosing the right DC/DC

Finding the proper DC/DC converter for adaptive power is challenging because of these requirements, which are contradictory:

- High efficiency at low loads (4-20 mA). Because this is generally possible in pulse frequency modulation (PFM), the DC/DC has to support this mode. Expect an approximate 50% efficiency improvement vs. forced pulse-width modulation (PWM) mode.
- Relatively high peak current (>0.5A) for fast settling. The peak current divided by the decoupling capacitances determines the output maximum voltage rate of change.
- VOUT within 4V to 24V, achieved by either a buck or boost converter based on the input voltage.
- A relatively small inductor to reduce solution size. A high switching frequency (≥300kHz) is required.
- Available in a small package.

Some parts that fulfill these requirements are:

LMR516xx: 65V input, PFM versions at 400kHz/1.1MHz, 0.6A/1A output current

LMR544xx: 36V input, PFM at 1.1MHz, 0.6A/1A output

LMR3650x: 3V-65V input, adjustable 200kHz-2.2MHz, 0.1A/0.15A output (if fast settling is not critical)

Controlling the DC/DC output

Nonfixed DC/DC converters use a feedback node kept at a constant reference voltage level through a high gain amplifier. By connecting a resistive potential divider between the converter output voltage and the feedback node, you can control the output voltage, as shown in **Figure 3**.

Because the converter keeps VREF fixed, you can calculate VS using **Equation 2**.

$$V_s = V_{REF}(1 + R_B/R_T) \tag{2}$$

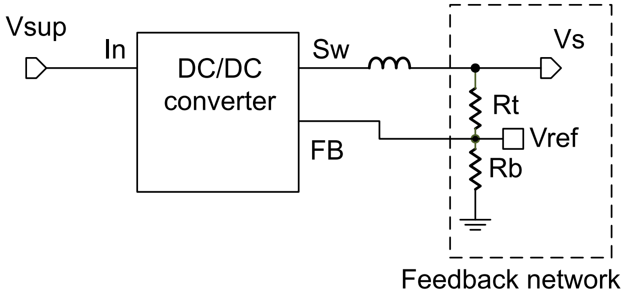


Figure 2. Feedback network for a DC/DC converter.

The change of output voltage requires changing the feedback divider. **Figure 3** shows three different ways to change the divider: variable sourcing current (a), variable sinking current (b), or using a variable voltage source and resistor (c). **Figure 3** also shows the transfer function (control variable, current or voltage vs. VS).

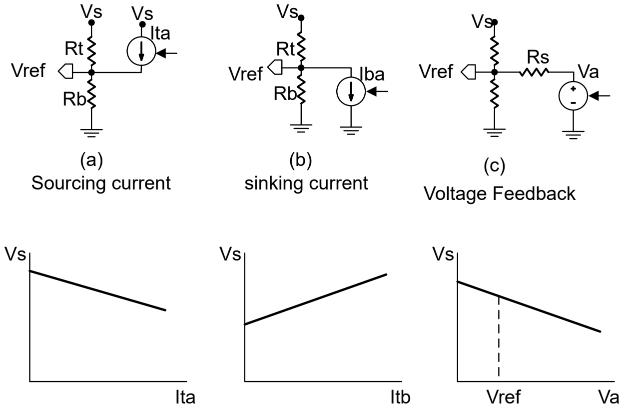


Figure 3. Adaptive control circuits and their transfer functions.

Applying Kirchoff's current law on the VREF node in each case yields the transfer function for case a:

$$I_{ta} + (V_S - V_{REF})/R_t = V_{REF}/R_b \tag{3}$$

Rearranging **Equation 3** results in **Equation 4**:

$$V_S = (1 + R_t/R_b)V_{REF} - I_{ta}R_t \tag{4}$$

Equation 5 shows similar calculation for case b:

$$V_S = (1 + R_t/R_b)V_{REF} + I_{ba}R_t \tag{5}$$

Equation 6 calculates case c:

$$V_S = (1 + R_t/R_b + R_t/R_s)V_{REF} - R_t/R_s V_a \tag{6}$$

A simple calculation can find the proper range of the control variable to achieve the required VS range given the reference voltage level present on the feedback pin and the chosen resistor values.

Example circuit using sourcing current

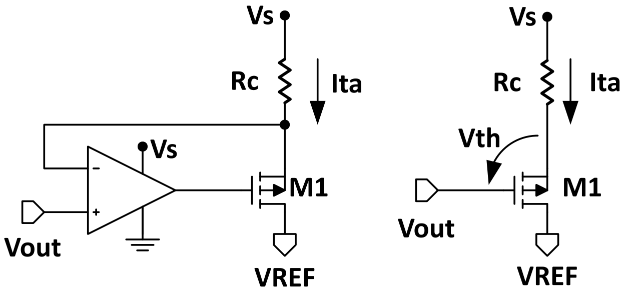
Figure 4 shows the construction of a high-side current source using an operational amplifier, PMOS transistor M1, and a resistor. Equation 8 calculates the current generated as:

$$I_{ta} = (V_S - V_{OUT})/R_c \tag{7}$$

You will need to consider the input/output and supply range of the operational amplifier and the maximum gate-to-source voltage (VGS) of M1. Further simplifying the circuit by removing the operational amplifier, **Equation 8** calculates the current generated as:

$$I_{ta} = (V_S - V_{OUT} + V_{th})/R_c \tag{8}$$

This saves power, cost and area, with some inaccuracy of current from the variation in threshold voltage (Vth).



Current source **simplified source**

Figure 4. Current source feedback circuit.

The TI XTR200 is a 4-20 mA current transmitter with V_S from 8V to 60V and V_H of 3V. If the load is up to 800Ω, V_{OUT} goes up to 16V with 20mA of current. This V_S has to track the output. At V_{OUT} = 0V, V_S = 8V, and at V_{OUT} = 16V, V_S = 19V. Use **Equation 8** and **Equation 5** to calculate resistors Rt, Rb and Rc. You will find that it is not possible to maintain V_H >3V without increasing the headroom for the low V_{OUT}.

Values Rt = 80kΩ, Rb = 3kΩ and Rc = 60kΩ produce the output-supply curve shown in **Figure 5**. Headroom is dependent on the output because this simple design uses only Rc as design variable. More complex circuits can overcome this limitation. But even with this simple circuit, the maximum power dissipation drops to half or less compared to the nonadaptive case. Any low-power rail-to-rail operational amplifier such as the OPA2990 will work in place of U2, as shown in **Figure 6**.

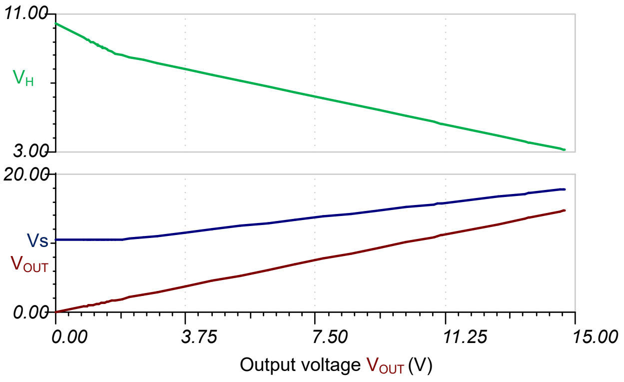


Figure 5. V_S-V_{OUT}, V_H-V_{OUT} relation.

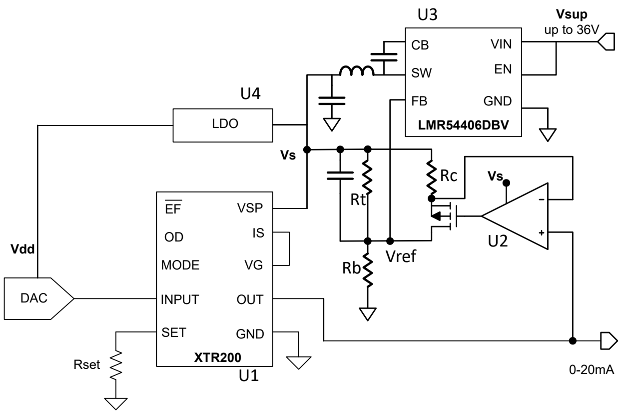


Figure 6. Output stage using the XTR200 with an adaptive supply.

Note

Simulation: The switching regulator simulation is quite long. Replacing the DC/DC with a low-dropout regulator (LDO) that has a similar VREF and similar input and output ranges can speed up DC simulation and enable easy creation of the transfer function graph. If the LDO has a different VREF, insert a voltage-controlled voltage source (VCVS) between the feedback node and the LDO's actual feedback node. For example, if VREF = 1.2V, and you want to design for the TI LMR54406 buck converter, which has a VREF = 0.8V, you can add a VCVS with gain of 1.5 to convert the 0.8V into 1.2V.

Example circuit using voltage feedback

For lower VS applications, use the output stage shown in my application note, "**Protected, Low-Noise, Combined V-I Output Stage as Analog Output Building Block**," working down to 5V.

The LMR51606 DC/DC simplified circuit shown in **Figure 7** omits the input capacitance and electromagnetic interference protection filters. The buck converter uses a small inductor (L1 = 15µH) and output capacitance (22µF) optimized to provide low ripple and enable fast supply ramping.

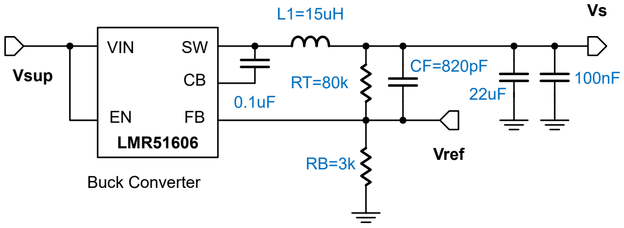


Figure 7. DC/DC circuit.

Use **Equation 2** to calculate the values of Rt and Rb so that Vs = 20.8V when no current is injected into the feedback node so that these values set the maximum supply level.

To achieve better efficiency, the difference amplifier shown in **Figure 8** senses the output headroom, where $V_H = V_S - V_{OUT}$. The difference amplifier has a gain of 0.33V/V so that the steady-state headroom is between 3V and 2.7V based on V_S. The 1MΩ input impedance reduces error on the output current to <0.1%. It is possible to compensate for this error during calibration.

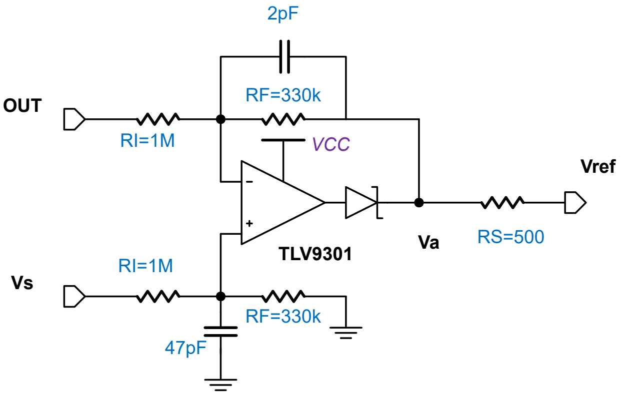


Figure 8. Difference amplifier.

The diode at the operational amplifier output prevents turning sourcing current into sinking, so if the operational amplifier output has a lower voltage than the feedback node, the loop will break. This keeps the upper limit of the VS set by Rt and Rb. The capacitors in the feedback path are essential for dynamic stability of the larger loop, including the DC/DC.

Figure 9 is a simplified overall circuit.

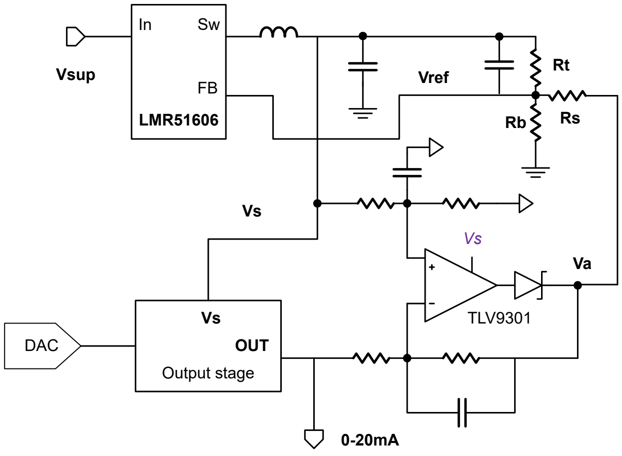


Figure 9. Simplified schematic for adaptive power with a difference amplifier.

Note

Dynamic performance: The output stage response to a DAC output change is typically fast. In contrast, the DC/DC is much slower, and the V_S cannot follow the output at the same pace. Limiting the difference amplifier bandwidth helps smooth this change and allows the converter to ramp properly. In addition, it is necessary to limit the slew rate of the DAC output if it doesn't inherently support slew-rate control. You will have to divide large DAC code changes into smaller changes over a longer period, creating a staircase DAC output that allows the DC/DC converter to settle without overshoot or oscillation.

Measurements and performance

Figure 10 shows the power losses for different output currents as well as various loads. Power losses are calculated as the input power to the DC/DC converter minus the output power to the load. The power losses never exceed 180mW, which translates to >50% of power savings.

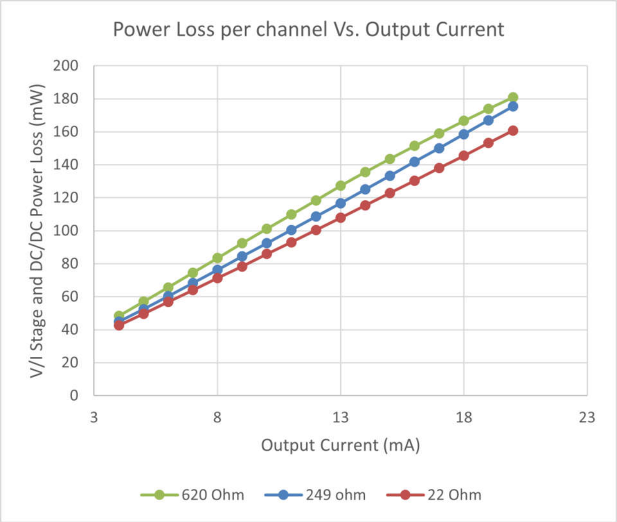


Figure 10. Power losses vs. output current.

Figure 11 shows the efficiency for different currents and loads. The efficiency of the DC/DC converter is calculated as the output power from the converter divided by the input power. The efficiency ranges between 75% and 90%.

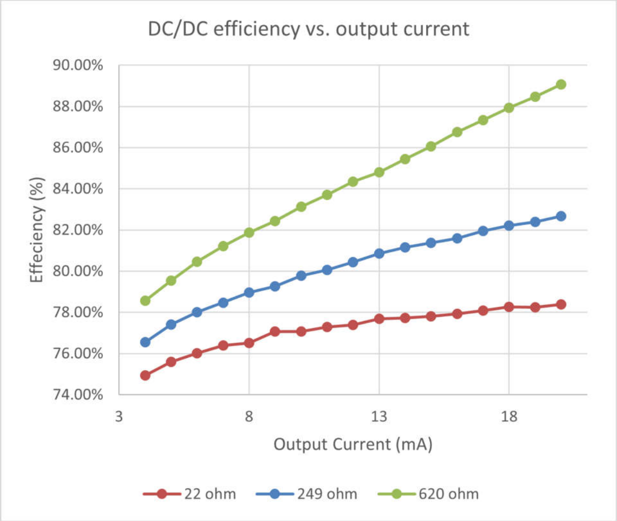


Figure 11. DC/DC efficiency vs. output current.

Precision and noise

A high-resolution analog-to-digital converter measures the effect of the DC/DC ripples on the output, converting 16,000 samples with a 640Ω load at 4 mA and 20 mA, respectively.

Table 1 summarizes the noise calculation and corresponding precision.

Output	4mA	20mA	Unit
Mean	4.019	20.17	mA
Root mean square (RMS) noise	325	530	nA
Peak-to-peak noise	2.78	3.51	µA
RMS resolution	18.2	17.5	Bits

Table 1. Noise performance of the adaptive circuit.

The results show that adaptive power doesn't affect the output stage performance, and can support 16-bit output resolution.

Settling time and dynamic performance

Settling time and the stability of the adaptive power loop are of great importance. Figure 12 shows that input ramping to full-scale in 200µs results in a stable output with simple stepping of the input of the output stage.

Figure 12 shows a 10V step over a 560Ω load, with the full-scale input voltage to the output stage ramped over seven steps to the full scale of 2.5V. The figure also shows a settling time <200µs.

The falling edge is slow because the decoupling and output capacitors need to discharge through the circuit and external load. This doesn't affect performance and is not critical.

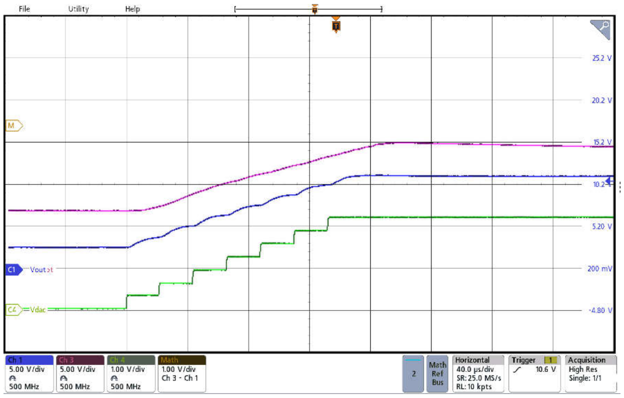


Figure 12. *Settling performance of the output stage and adaptive supply.*

Conclusion

The measurement results demonstrate that adaptive supply techniques deliver tangible benefit by achieving over 50% power savings compared to fixed-supply implementation. The 17.5 to 18.2 bits of RMS resolution prove that thermal management improvements don't come at the expense of signal quality. As PLC modules continue to pack more channels into smaller footprints, the techniques presented here transition from optimization strategies to practical necessities for next-generation industrial automation systems.

Additional resources

- See the TI Developer Conference presentation, "**System Power Savings Using Dynamic Voltage Scaling**."
- Check out the **Less Than 1-W, Quad-Channel, Analog Output Module With Adaptive Power Management Reference Design**.
- For more insight into the role of the feedforward capacitor to enhance dynamic performance, read the application report, "**Optimizing Transient Response of Internally Compensated DC/DC Converters With Feedforward Capacitor**."

About the author

Ahmed Noeman is a systems engineer at Texas Instruments, specializing in defining integrated solutions for industrial applications. Ahmed has more than 20 years of semiconductor experience in areas including system design, IC design and IC verification. Ahmed received an M.S. and B.S. in electrical engineering from Ain Shams University in Egypt.

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