A 3-A, 1.2-V_{OUT} linear regulator with 80% efficiency and P_{LOST} < 1 W

By Jeff Falin (Email: j-falin1@ti.com)
HPA Portable Power Applications

Introduction

Using linear regulators for higher-current (>1-A), low-output voltage applications has been a challenge for many years due to the regulator's dropout requirements, related inefficiency, cumbersome output capacitor requirements for stability, and large inrush currents at startup. The Texas Instruments (TI) dual input rail TPS74x01 solves these problems.

Linear regulator topology review

The primary drawback of linear regulators for higher-current applications is their low efficiency, computed as V_{OUT}/V_{IN}. The power lost (P_{LOST}) in a linear regulator, computed as

$$1-\frac{V_{OUT}}{V_{IN}}\times P_{IN}=(V_{IN}-V_{OUT})\times I_{OUT},$$

must be dissipated by its package. The TO-263 or D2PAK package is the largest surface-mount package in which linear regulators are available. Without additional airflow, its maximum power dissipation capability is approximately 2.75 W (assuming it is soldered to a large copper plane for heat sinking). Many higher-current, "low-dropout" linear regulators with PMOS pass elements have minimum input voltages of 2.5 to 2.7 V, not only to power the internal LDO drive circuitry but also to drive the PMOS FET hard enough to provide higher output currents.

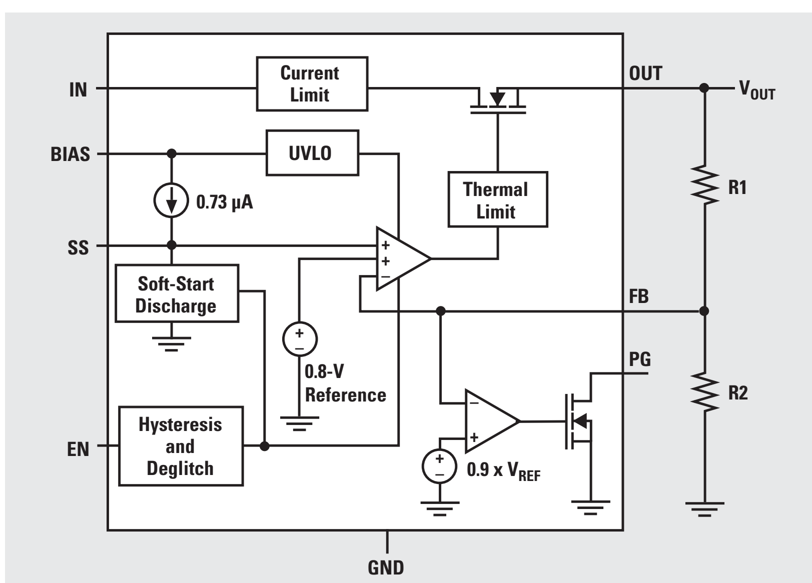
Therefore, using many PMOS-pass-element-based linear regulators for output voltages below 1.8 V and output currents above 2.5 A is cumbersome and costly due to the additional airflow and/or external heat sinking required to dissipate the heat generated by the regulator.

Since NMOS FETs have inherently lower $r_{DS(on)}$ than similarly current-rated PMOS FETs, an NMOS FET pass element needs less $V_{IN} – V_{OUT}$ drop to provide the same current. However, the source-follower configuration of the NMOS-based regulator requires that the gate of the FET be at least a threshold voltage drop (typically 1 V) above the output voltage. The regulator needs either an internal charge pump to provide a higher gate-drive voltage or, more simply, a second low-power input rail from an existing 5-V or 3.3-V bias supply. This is the reasoning behind the development of the dual-rail, NMOS-pass-element-based TPS74x01 family of linear regulators.

Dropout

As shown in Figure 1, the TPS74x01 regulators have two input voltages, one providing the low-current bias voltage to power the internal circuitry that controls the NMOS pass device and one as a second power input. Since all the

Figure 1. Block diagram of the TPS74201 and TPS74401 linear regulators



internal circuits run off the higher BIAS input, the device is capable of achieving regulation from a low-voltage input supply. In fact, the power input, IN, is limited only by the output voltage and dropout of the device.

There are two different specifications for dropout voltage with the TPS74x01. The first is referred to as V_{IN} *dropout* and is for users who wish to apply an external bias voltage to achieve low dropout. This specification assumes that V_{BIAS} is at least 1.62 V above V_{OUT}. Such an application might be a low-ripple, 1.2-V, 3-A power rail for an FPGA transceiver where V_{IN} and V_{BIAS} are provided by 1.5-V and 3.3-V switching supplies, respectively. In this configuration, the 3 × 3-mm QFN package, which is capable of dissipating 1.9 W at 55ºC, needs to dissipate only

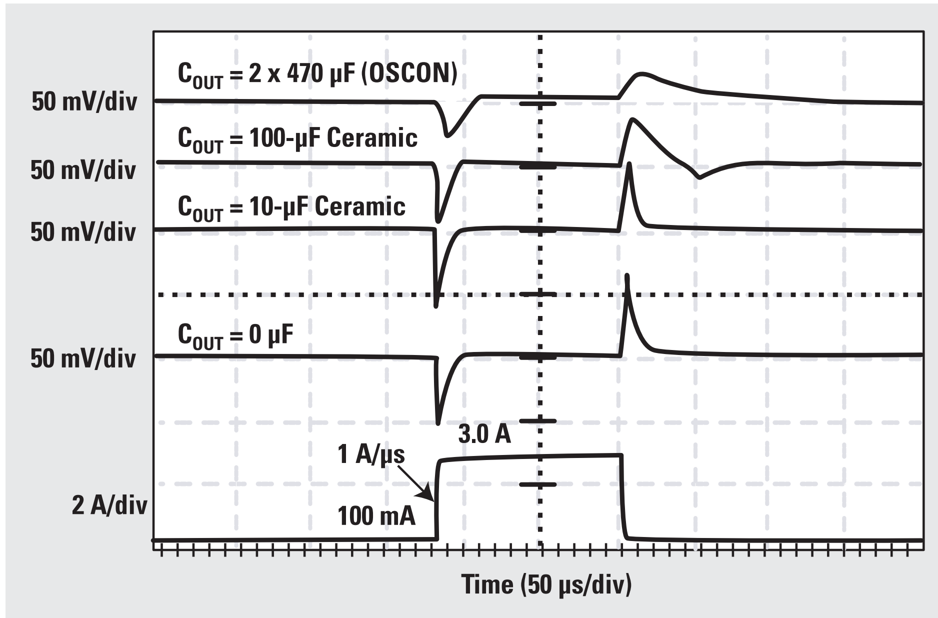
$$(1.5\text{ V} - 1.2\text{ V}) \times 3\text{ A} = 0.9\text{ W},$$

thereby achieving 1.2 V/1.5 V = 80% efficiency.

The second specification is referred to as V_{BIAS} *dropout* and is for users who wish to tie the IN and BIAS pins together. This allows the device to be used in applications where an auxiliary bias voltage is not available or low dropout is not required. Dropout is limited by BIAS in these applications because V_{BIAS} provides the gate drive to the pass FET and therefore must be 1.4 V above V_{OUT}. For example, the TPS74201 can provide a 3.3-V, 1.0-A soft-starting supply (discussed later) from a 5-V rail with 3.3 V/5 V = 66% efficiency and can dissipate

$$(5\text{ V} - 3.3\text{ V}) \times 1.0\text{ A} = 1.7\text{ W}.$$

Figure 2. Load transient response with various output capacitors



Stability and transient response

Until recently, linear regulator loop stability presented a challenge to analog IC designers because one of the control-loop poles, created by the output capacitor and the impedance at the load, varies in frequency location based on the output current. Regulators with the NMOS pass element in source-follower configuration have always been slightly easier to compensate because their output impedances are lower than similarly rated PMOS regulators in common-source configurations. This means that the NMOS regulator's moving pole is higher in frequency than the comparably rated PMOS counterpart and so is further away from the internal error amplifier's pole(s). Older methods of ensuring stability were either to roll off the control-loop response at low frequency, thereby killing transient response, or to counteract the moving pole with a zero created by an output capacitor with a certain amount of equivalent series resistance (ESR). Using a patented feedback control topology, the TPS74x01 family, configured with V_{BIAS} = 3.3 V, V_{IN} = 1.8 V and V_{OUT} = 1.5 V, achieves fast transient response times (see Figure 2) with no output capacitors but is still stable with larger capacitors having ESR. The absence of output voltage ringing after the load transient shows that the regulator is very stable with no output capacitance.

Since the TPS74x01 family is stable with no output capacitor but has such fast transient response, local bypass capacitance for the device under power may be sufficient to meet the transient requirements of many FPGAs and DSPs. This reduces total solution cost by eliminating the need to have multiple bulk capacitors for the power rail.

Soft start and sequencing

Many older linear regulators start up fast because the feedback loop senses the low output voltage and turns on the pass FET hard. For some applications, fast startup is required; however, such fast turn-on causes large inrush currents, up to the current-limit rating of the device, to charge output capacitors. These large currents may pull down the input power bus and cause system-level problems. To achieve a linear and monotonic soft start that reduces peak inrush current during startup and minimizes startup transients seen by the input power bus, the TPS74201 and TPS74401 error amplifiers track the voltage ramp of the external soft-start capacitor until its voltage exceeds the internal reference. The soft-start ramp time is dependent on the soft-start charging current (I_{SS}), soft-start capacitance (C_{SS}), and the internal reference voltage (V_{REF}). It can be calculated with

$$t_{SS} = \frac{V_{REF} \times C_{SS}}{I_{SS}}.$$

Note that since the soft start is voltage-controlled, the startup is not dependent on the output load.

Instead of an SS pin, the TPS74301 version has a TRACK pin. As summarized in Figure 3, with the center tap of a resistor divider from an external supply connected to TRACK, the TPS74301's output voltage will track the external supply until the TRACK voltage reaches 0.8 V. This feature can be used to implement simultaneous or ratiometric sequencing. It is useful for minimizing the stress on ESD structures that are present between the Core and I/O power pins of many processors and/or for managing integrated power-on reset circuitry. All members of the TPS74x01 family facilitate implementation of sequential sequencing by tying the integrated PG signal to the EN pin of a following supply.

Conclusion

With a dual input rail and low dropout voltage, the TPS74x01 family has made linear regulators more appealing than switching regulators, reducing board size and cost and providing comparable efficiency for powering many lower-voltage, higher-output-current power rails. The family's additional features—including controllable soft starting, tracking, and integrated PG—manage start-up problems that have plagued linear regulators in the past. Add in the fast transient response, which minimizes the total number of output capacitors, and you have a nearly ideal dc/dc converter.

References

For more information related to this article, you can download an Acrobat Reader file at www-s.ti.com/sc/techlit/*litnumber* and replace *"litnumber"* with the **TI Lit. #** for the materials listed below.

Document Title	**TI Lit. #**
1. "1.5-A LDO with Programmable Soft-Start," TPS74201 Datasheet	sbvs064
2. "1.5A Ultra-Low Dropout Linear Regulator with Programmable Sequencing," TPS74301 Datasheet	sbvs065
3. "3.0A Ultra-Low Dropout Linear Regulator," TPS74401 Datasheet	sbvs066

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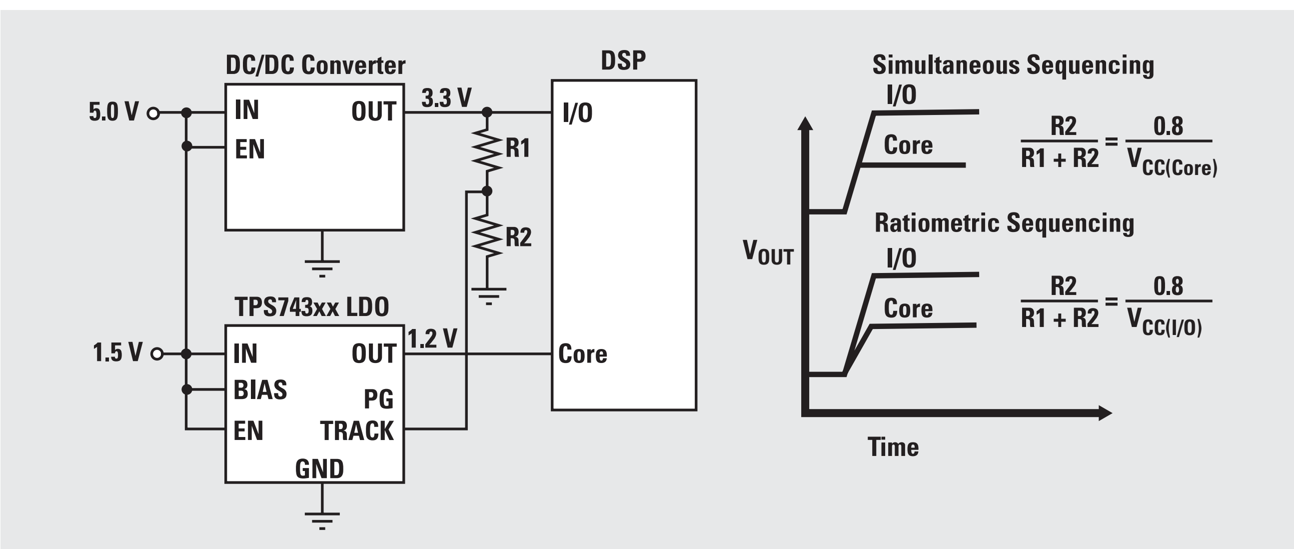
Figure 3. Various sequencing methods using the TRACK pin



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C062706

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Mailing Address: Texas Instruments
Post Office Box 655303
Dallas, Texas 75265