Test Report: PMP23488

540W Flat Screen TV Power Reference Design

Description

This reference design provides the information for a flat screen TV power design with a height limitation of 10mm. The design uses an interleave transition-mode (TM) power factor correction (PFC) for the main board, and two separate LLC resonant daughter boards which can be changed and were designed based on the planar transformer. The typical capability of the reference design is 300W, and the peak capability is 540W.

Resources

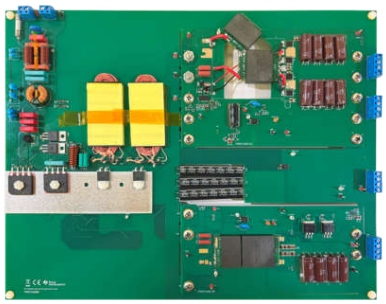
PMP23488	Design Folder
UCC28065, UCC25661	Product Folder
LMG3612, LMG3622	Product Folder
LMG3624, TPSI3050	Product Folder
INA225, LM317	Product Folder
LMG3100R017	Product Folder

Features

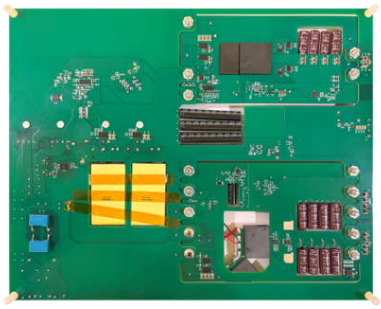
- Full TV design including interleave CrM PFC, two LLCs for backlight and system power design
- Planar transformer design in LLC stages
- Slim power design with 10mm height
- Daughter boards design for LLC stages: check each module independently before system assembly
- <150mW no load standby power, and <300mW input power with 165mW output power
- Primary switch device by GaN for high frequency capability
- No load condition without burst mode to eliminate audible noise

Applications

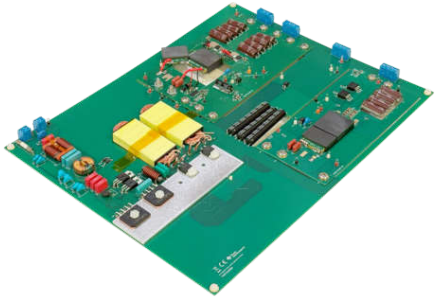
- SMPS power supply for TV
- OLED TV
- LCD TV
- Industrial AC-DC



Top View of Board



Bottom View of Board



Angled View of Board

1 Test Prerequisites

1.1 Voltage and Current Requirements

Table 1-1. Voltage and Current Requirements

Parameter	Specifications
Input AC Voltage	90V to 265V
Input line frequency	50 to 60Hz
Output Voltage 1 at Powre_On is Low	7.5 to 9.5V
Output Current 1 at Powre_On is Low	0 to 50mA
Output Voltage 1 at Powre_On is High	12.5V
Output Current 1 at Powre_On is High	6A
Output Voltage 2	25V
Output Current 2	1.125A Peak 10.5A
Output Voltage 3 (Backlight)	18.38 to 22.5V
Output Current 3 (Backlight)	10A

1.2 Safety Warning

Do not touch the board or the electrical circuits while the board is energized because of high voltages capable of causing an electrical shock hazard. Make sure the high voltage is fully discharged before handling the board.

1.3 Dimensions

Length × Width × Height: 355mm × 283mm × 10mm

1.4 Test Setup

The block diagram of the flat screen TV power is shown in Figure 1-1. The diagram includes three parts: main board which is the interleave PFC stage, and two daughter boards, one board for the system power (V_{out} 1 and V_{out} 2), and the other board is for the backlight (V_{out} 3). The test procedure is:

1. Make sure all connections. Set the standby load current on V_{out} 1 (<50mA)
2. Applied input AC voltage on the main board. V_{out} 1 and V_{out} 2 should be ready when the AC voltage >80V. V_{out} 1 is 7.5 ~ 9V and V_{out} 2 is about 17 ~ 19V.
3. Apply 5V on Power_On pin to enable the PFC and backlight power (V_{out} 3). V_{out} 1 and V_{out} 2 should be 12.5V and 25V. It is possible to load higher current on the system. V_{out} 3 is 18V.
4. Apply external power source on Vout_Adj pin start from 0V. Adjust the voltage on the DC source and confirm the V_{out} 3 to be the voltage to be tested

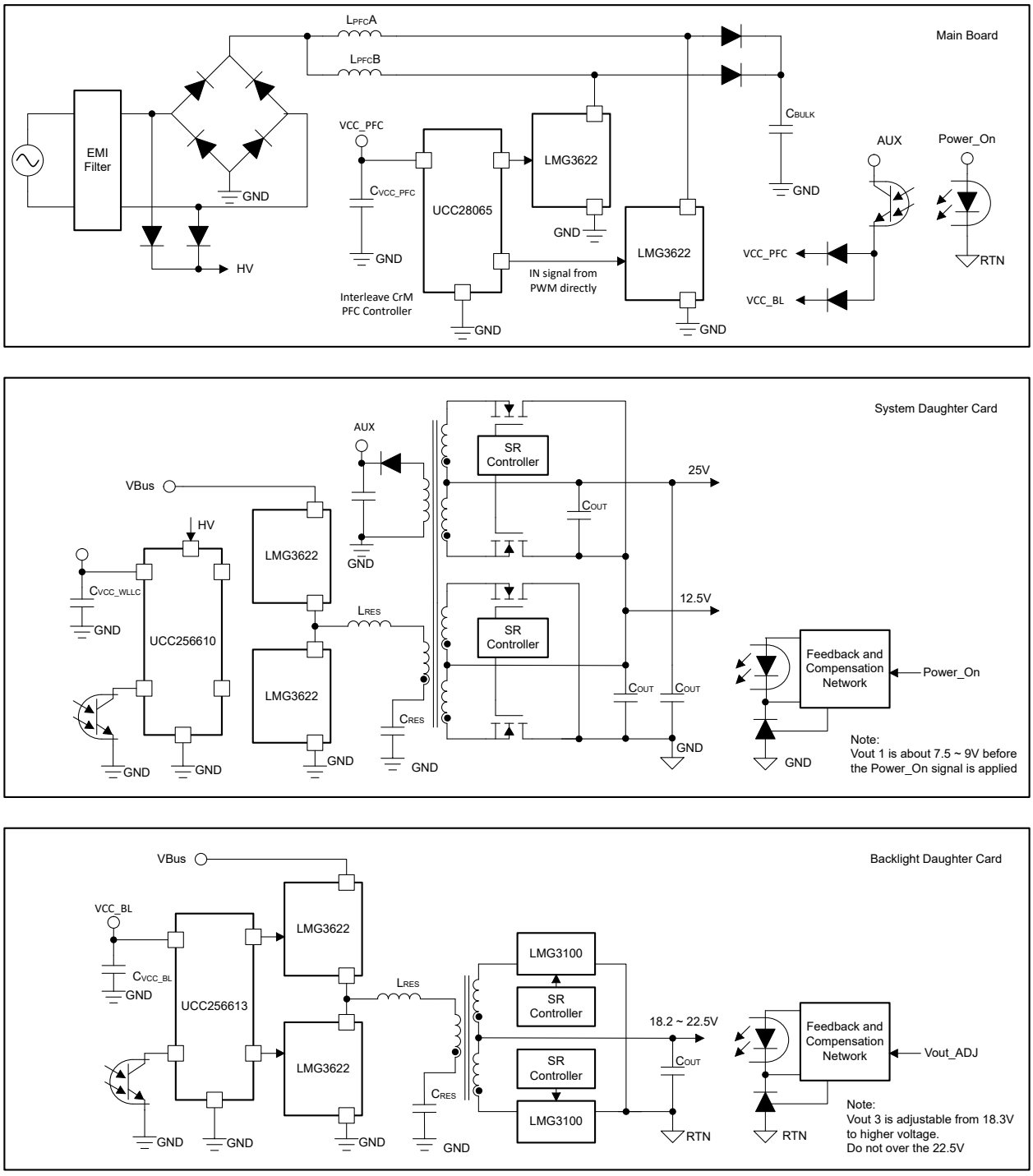


Figure 1-1. Test Setup

2 Testing and Results

2.1 Efficiency Graphs

Efficiency is shown in Figure 2-1.

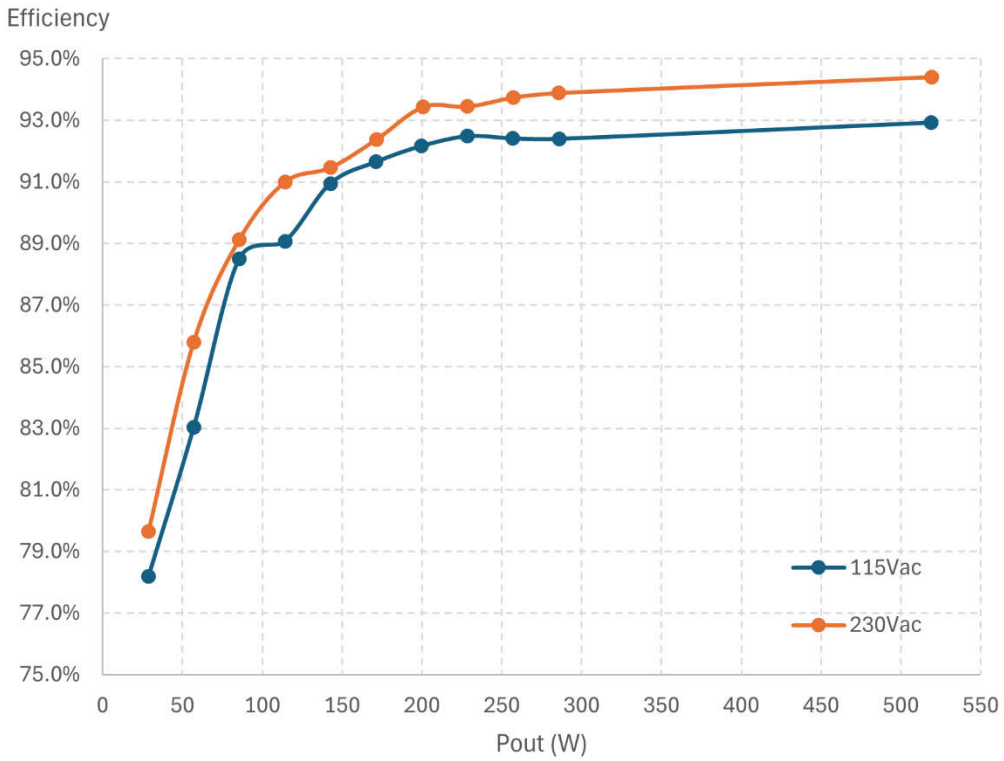


Figure 2-1. Efficiency Graph

2.2 Efficiency Data

No load and tiny load input power is shown in Table 2-1, and the efficiency data is shown in Table 2-2.

Table 2-1. Efficiency Data

V_{IN} (V)	No Load	165mW	330mW
115V / 60Hz	47.57mW	263.79mW	483.59mW
230V / 50Hz	108.04mW	301.08mW	498.51mW

Table 2-2. Efficiency Data

V_{IN} (V)	V_{OUT} 1 (V)	I_{OUT} 1 (A)	V_{OUT} 2 (V)	I_{OUT} 2 (A)	V_{OUT} 3 (V)	I_{OUT} 3 (A)	P_{IN} (W)	P_{OUT} (W)	P_{LOSS} (W)	Efficiency (%)
115	12.444	6.0019	24.898	10.503	18.286	10.004	558.66	519.1245	39.54	92.92%
115.05	12.445	6.0019	24.927	1.1288	18.288	10.015	309.52	285.9856	23.53	92.40%
114.98	12.447	5.4018	24.926	1.0069	18.288	8.9928	277.88	256.7945	21.09	92.41%
115.05	12.447	4.8019	24.921	0.9019	18.288	7.9966	247.06	228.4873	18.57	92.48%
114.97	12.448	4.2022	24.918	0.7819	18.288	6.9906	216.62	199.6365	16.98	92.16%
115.03	12.448	3.6034	24.882	0.6769	18.288	5.9947	186.94	171.3288	15.61	91.65%
114.96	12.488	3.0031	24.909	0.5578	18.288	4.9947	156.95	142.74	14.21	90.95%
115.04	12.448	2.4028	24.905	0.4528	18.288	4.0003	128.37	114.3445	14.03	89.07%
114.98	12.448	1.8031	24.916	0.3319	18.289	3.0003	96.709	85.5871	11.12	88.50%
115.05	12.447	1.2034	24.857	0.2269	18.289	1.9994	68.875	57.1858	11.69	83.03%
115	12.447	0.6034	24.753	0.1238	18.289	0.9991	36.896	28.84748	8.05	78.19%
230.0	12.442	6.002	24.901	10.50	18.287	10.004	549.89	519.154	30.74	94.41%

Table 2-2. Efficiency Data (continued)

V_{IN} (V)	V_{OUT} 1 (V)	I_{OUT} 1 (A)	V_{OUT} 2 (V)	I_{OUT} 2 (A)	V_{OUT} 3 (V)	I_{OUT} 3 (A)	P_{IN} (W)	P_{OUT} (W)	P_{LOSS} (W)	Efficiency (%)
230.1	12.448	6.002	24.935	1.13	18.286	10.004	304.38	285.7914	18.59	93.89%
230.1	12.449	5.402	24.931	1.02	18.287	9.003	274.54	257.3704	17.17	93.75%
230.0	12.449	4.802	24.928	0.90	18.287	8.003	244.63	228.6031	16.03	93.45%
230.1	12.449	4.203	24.922	0.82	18.287	7.002	214.86	200.7663	14.09	93.44%
230.0	12.449	3.603	24.916	0.68	18.287	6.000	185.59	171.4426	14.15	92.38%
230.1	12.449	3.003	24.912	0.56	18.287	5.000	156.04	142.722	13.32	91.47%
230.0	12.449	2.403	24.908	0.45	18.288	4.000	125.66	114.352	11.31	91.00%
230.0	12.448	1.803	24.919	0.33	18.288	3.000	96.034	85.58509	10.45	89.12%
230.0	12.447	1.203	24.863	0.23	18.288	1.999	66.649	57.18516	9.46	85.80%
230.0	12.448	0.603	24.75	0.12	18.289	0.999	36.224	28.84771	7.38	79.64%

2.3 Thermal Images

2.3.1 PFC Stage

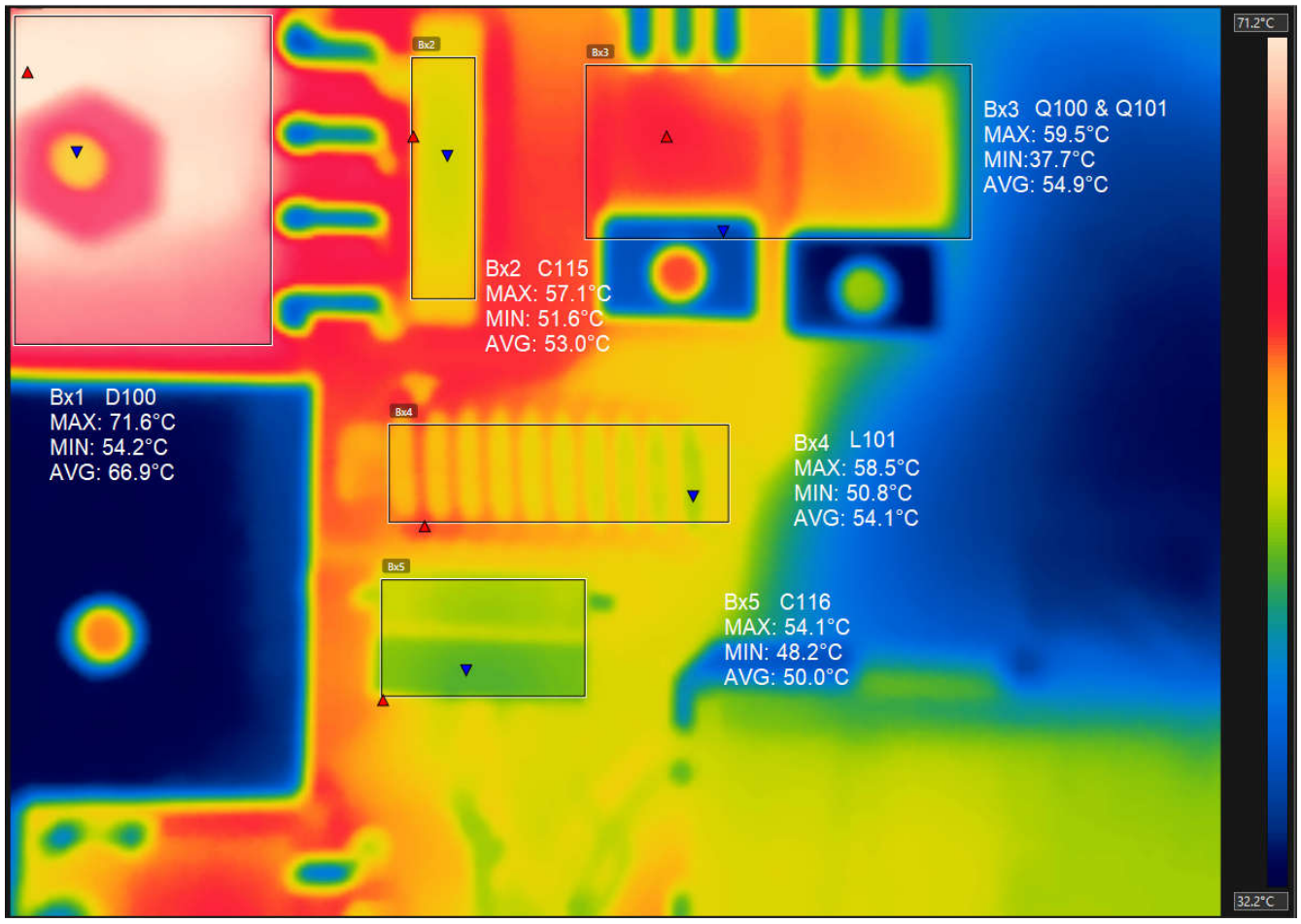


Figure 2-2. Thermal Image of the PFC Stage On the Top Side of PCB

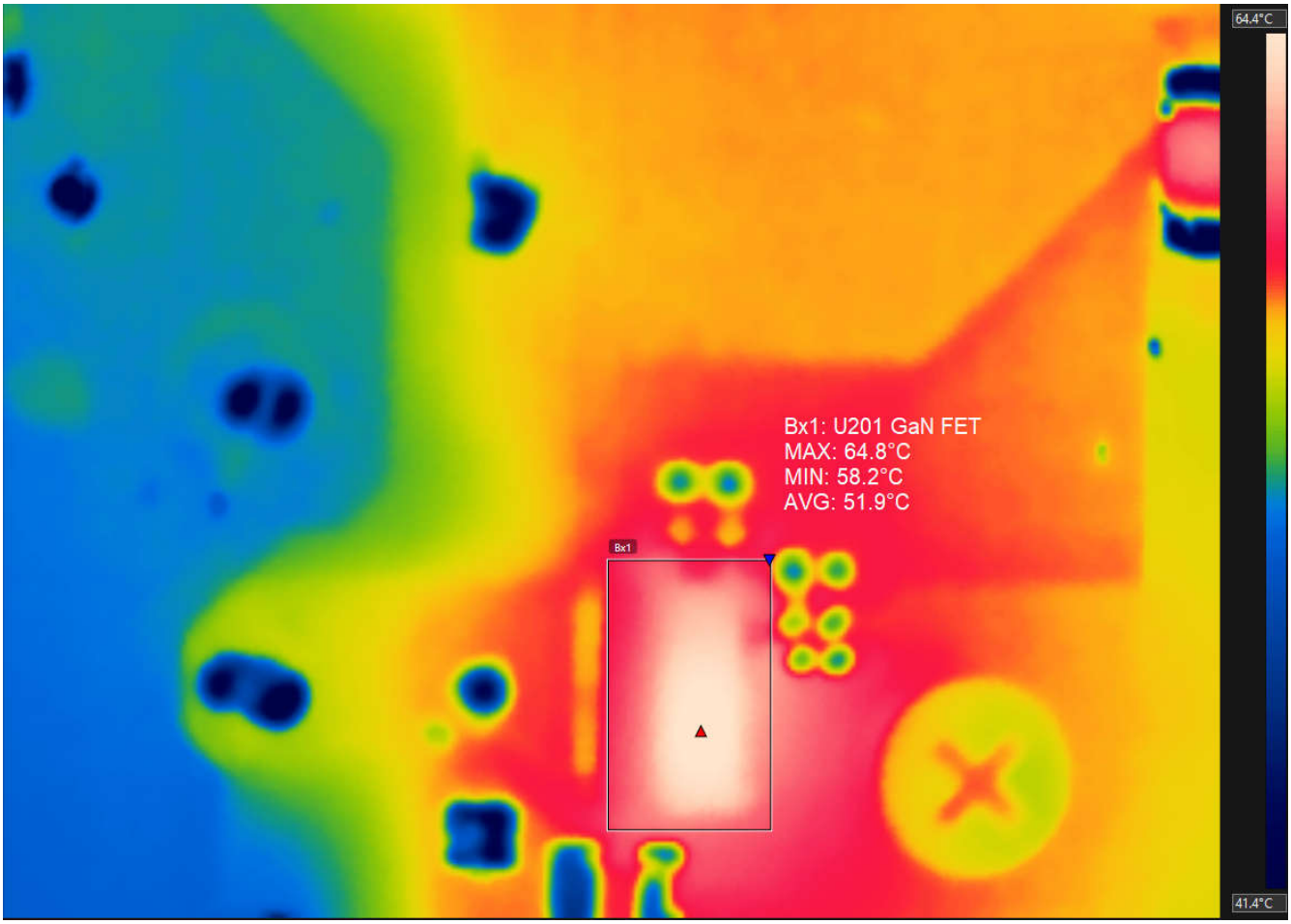


Figure 2-3. Thermal Image On the Top Side of PCB; Main Switch GaN Device is 64.8°C

2.3.2 Thermal Image of System LLC Stage

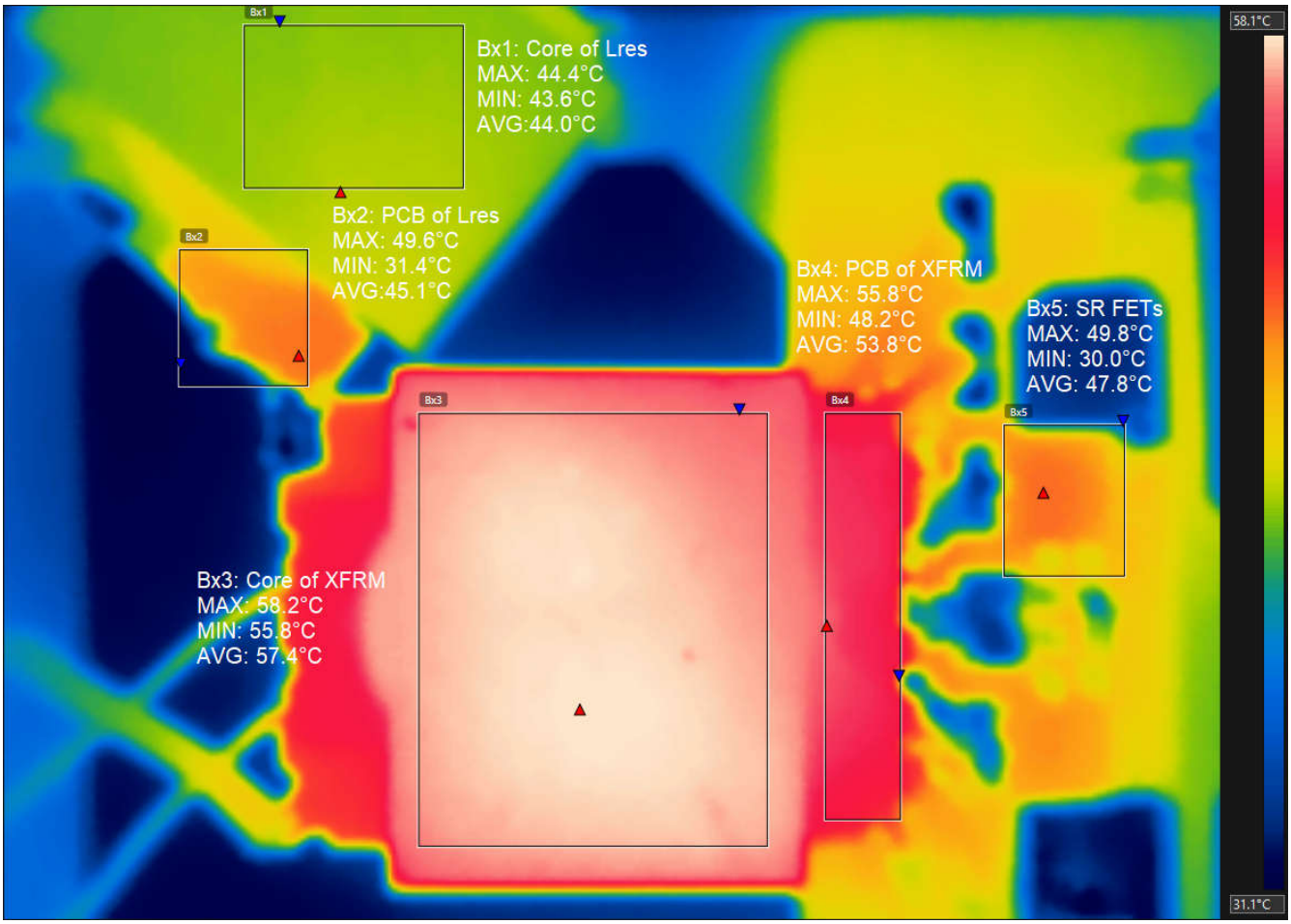


Figure 2-4. Thermal Image On the Top Side of PCB

2.3.3 Thermal Image of Backlight LLC Stage

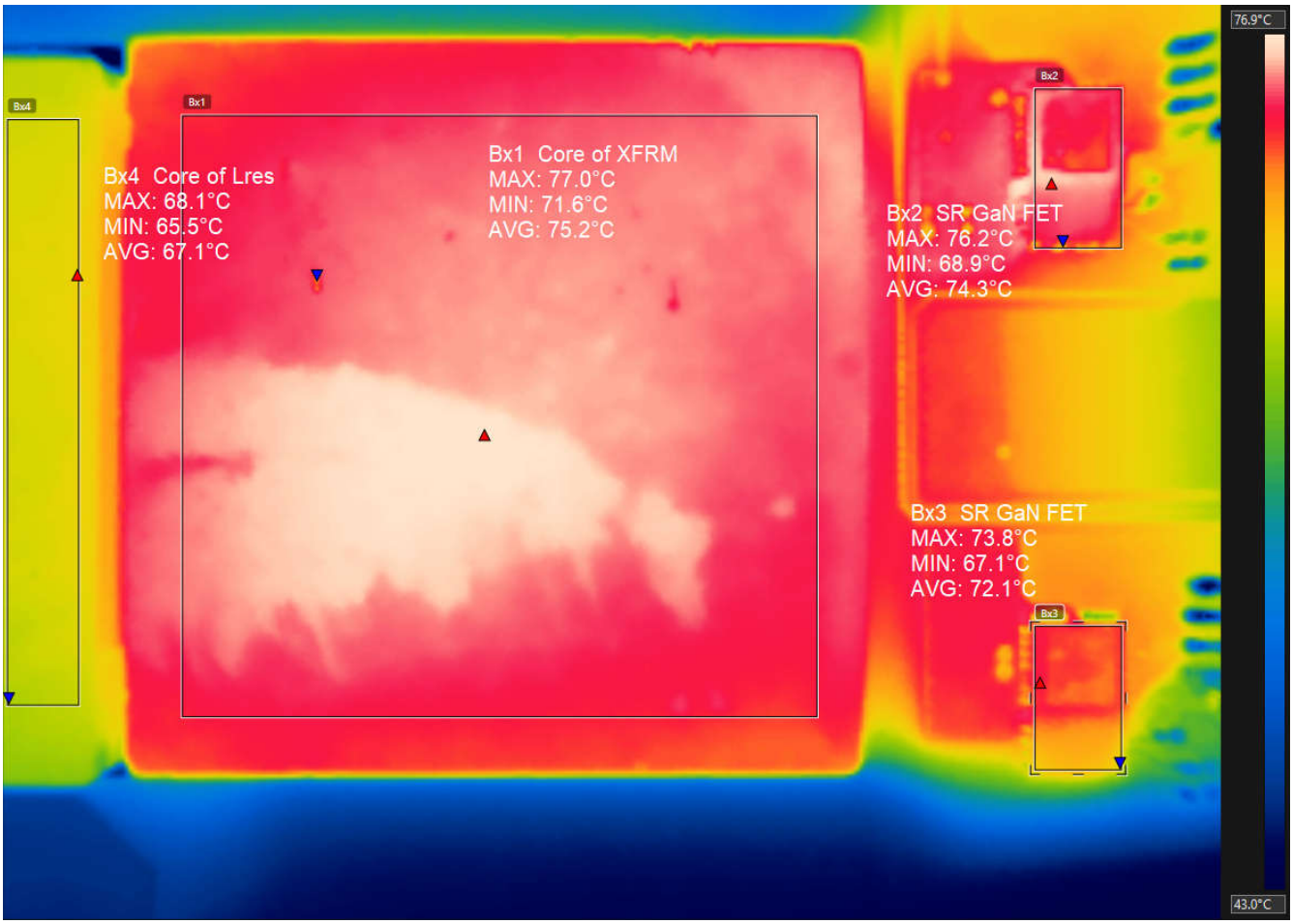


Figure 2-5. Thermal Image On the Bottom Side of PCB With V_{out} at 18.28V-10A

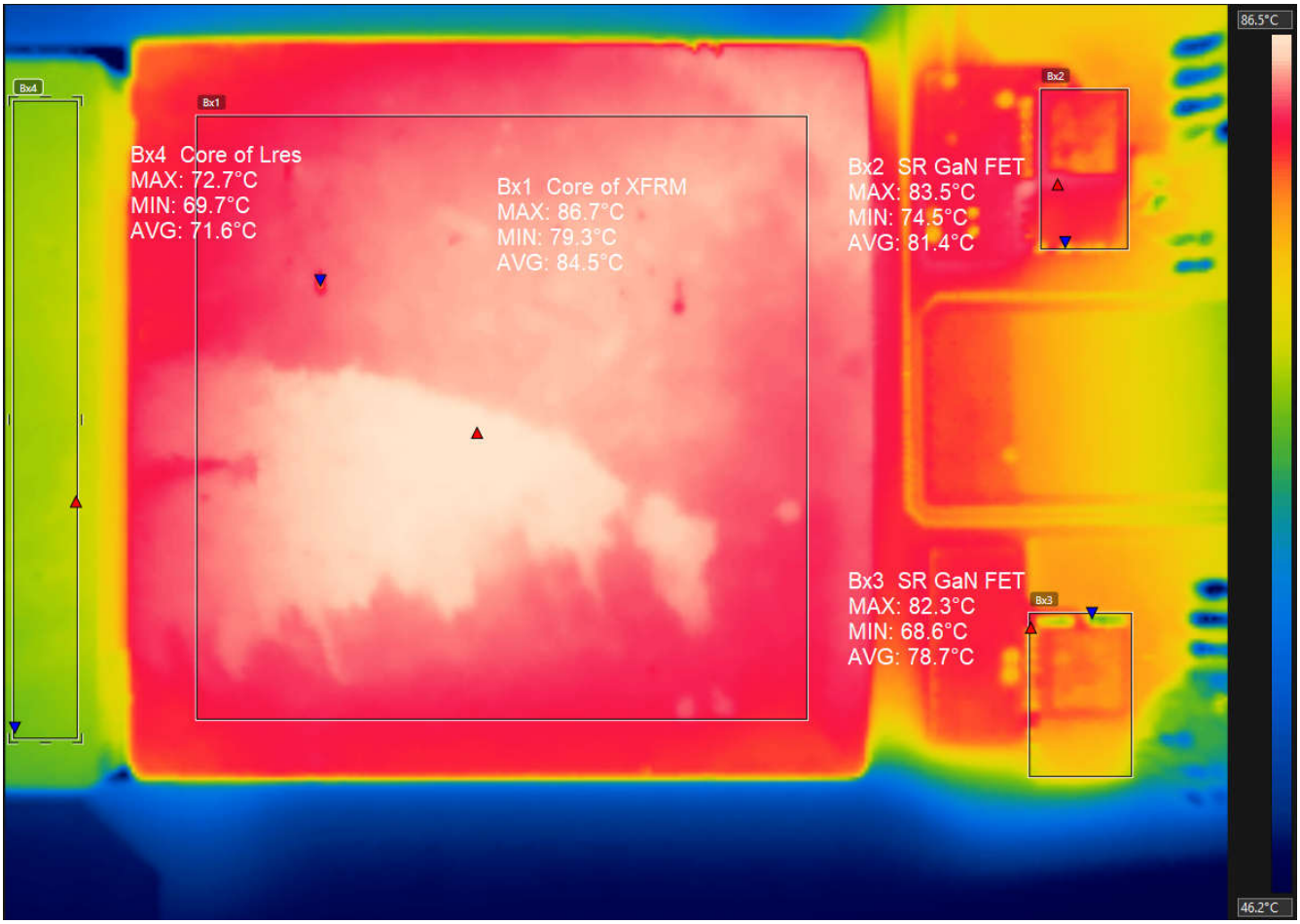


Figure 2-6. Thermal Image On the Bottom Side of PCB With V_{out} at 20V-10A

2.4 PF Value

PF value is shown in Figure 2-7.

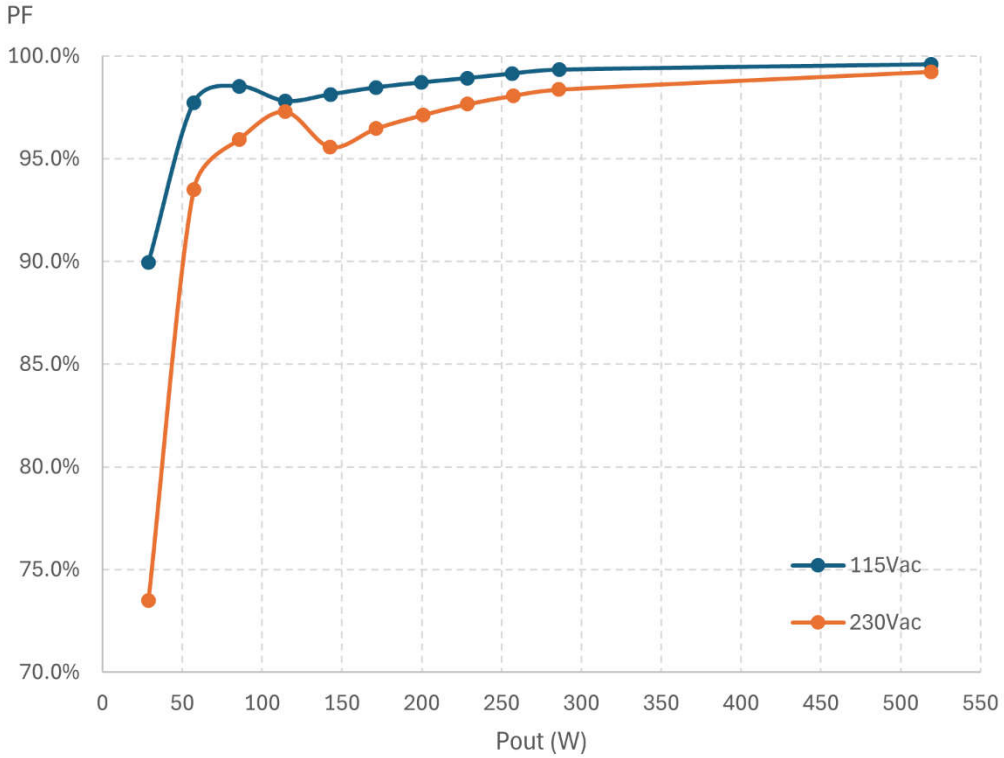


Figure 2-7. PF Value Based On the Output Power

3 Waveforms

3.1 Switching

3.1.1 PFC Switching waveform

Interleave PFC Switching behavior is shown in Figure 3-1 and Figure 3-2.

CH1 is the switching waveform of phase A, and CH 2 is the switching waveform of phase B. CH6 is the combination current waveform of two inductors.

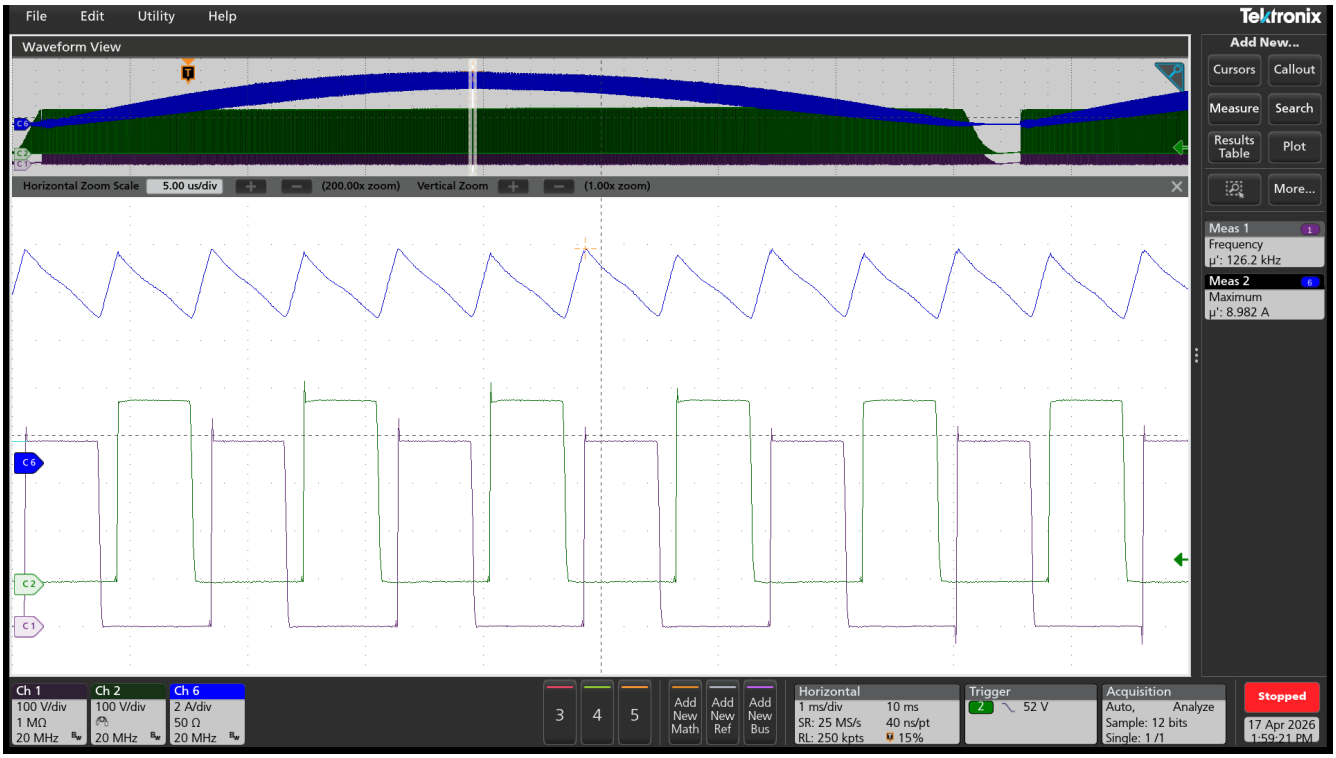


Figure 3-1. Switching Waveform of PFC Stage at 115Vac / 60Hz Input Voltage

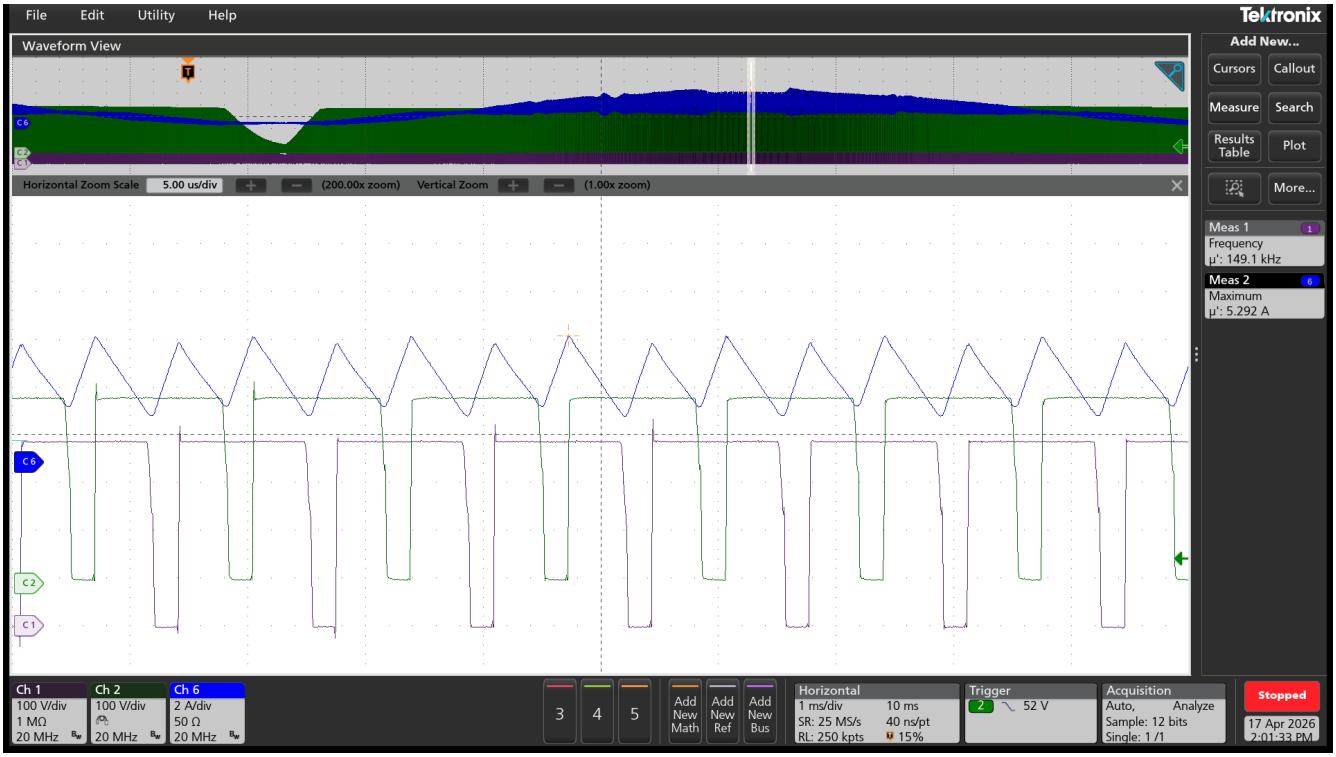


Figure 3-2. Switching Waveform of PFC Stage at 230Vac / 50Hz Input Voltage

3.1.2 System LLC Switching Waveform

Wide range LLC Switching behavior is shown in Figure 3-3 through Figure 3-7.

CH1 is the waveform of switching node, CH6 is the primary side resonant current.

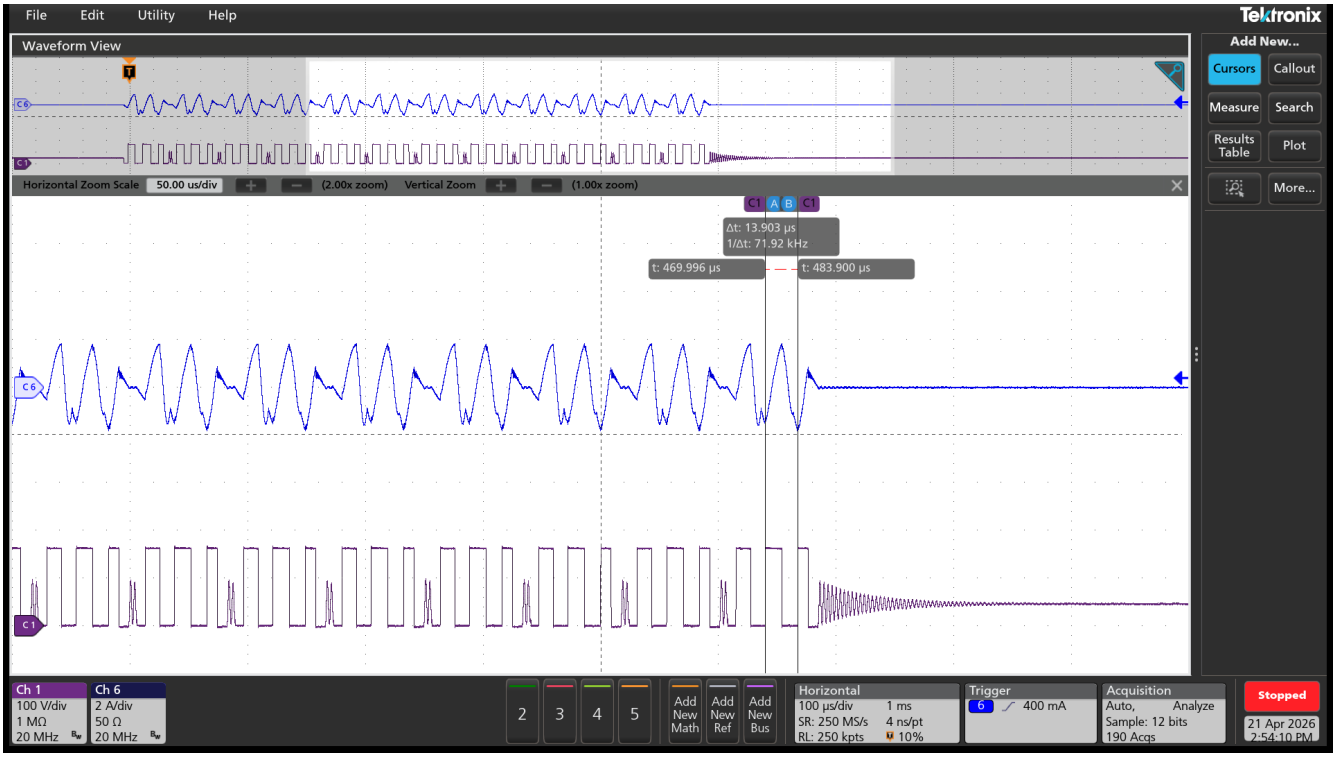


Figure 3-3. Switching Waveform With 165mW Load at 115Vac / 60Hz Input Voltage

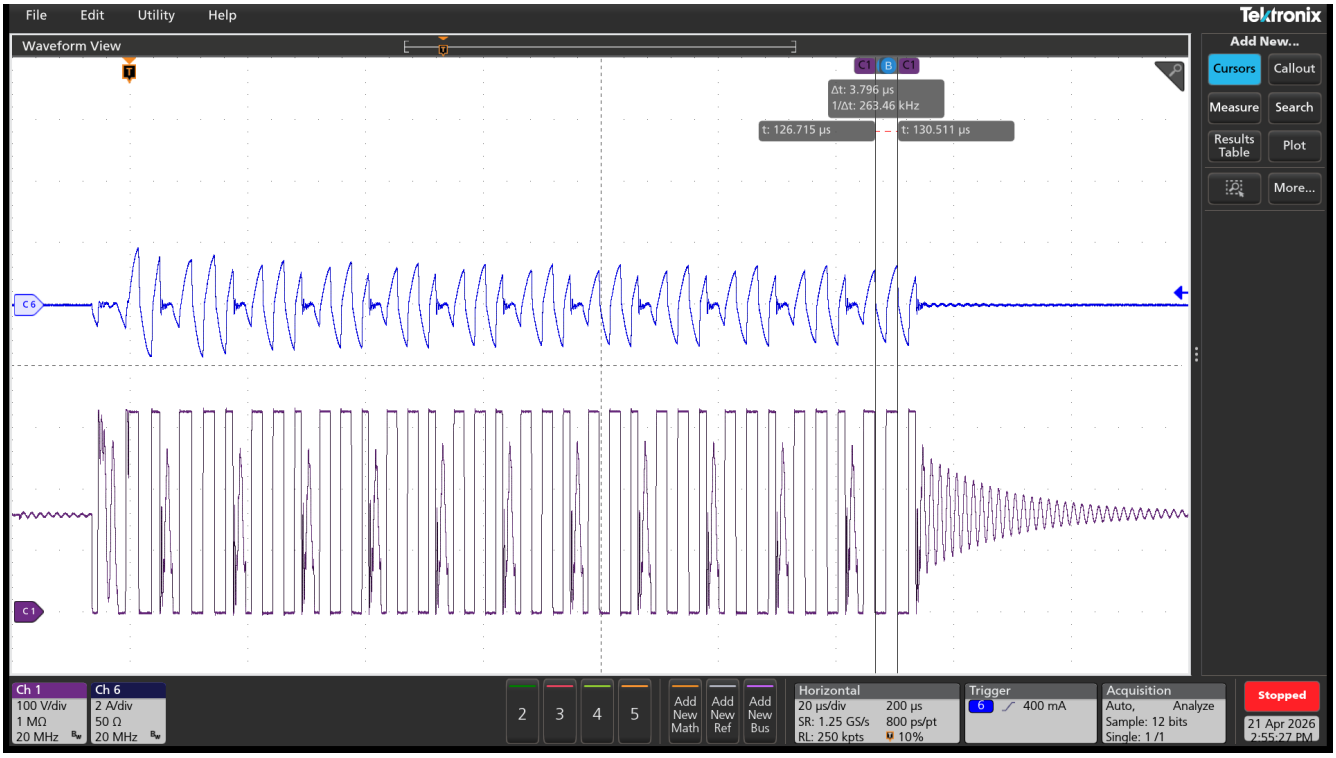


Figure 3-4. Switching Waveform With 165mW Load at 230Vac / 50Hz Input Voltage

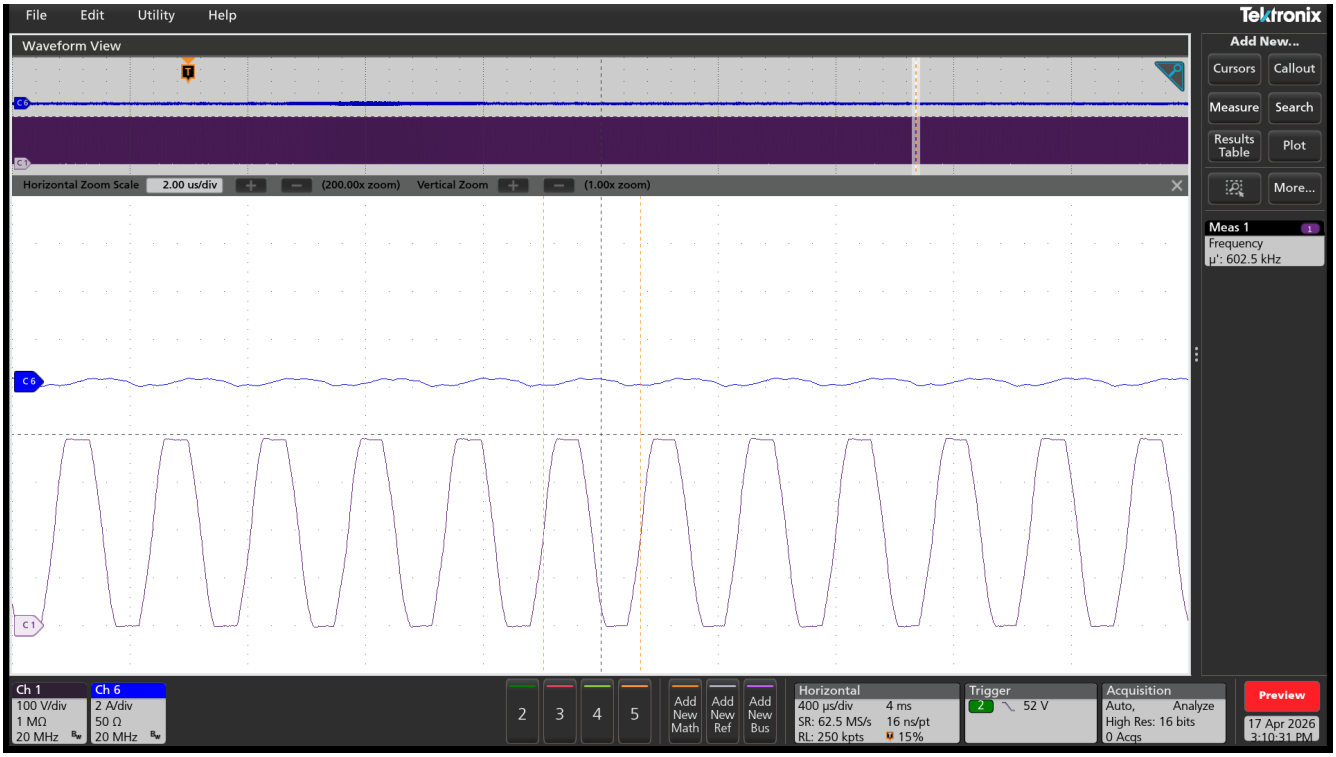


Figure 3-5. Switching Waveform With No Load With PS_ON Pull High; System Runs at 602.5KHz

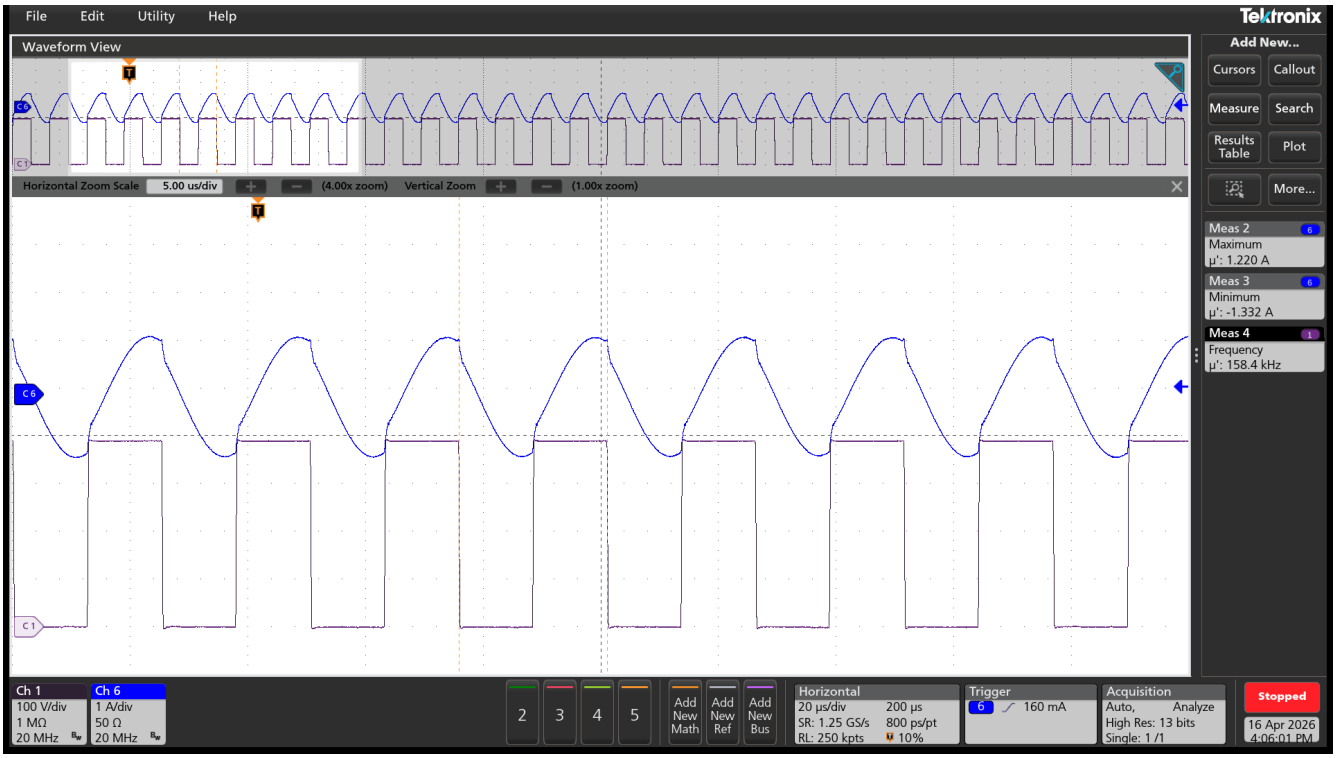


Figure 3-6. Switching Waveform at Full Load With PS_ON pull high; System Runs at 158.4KHz

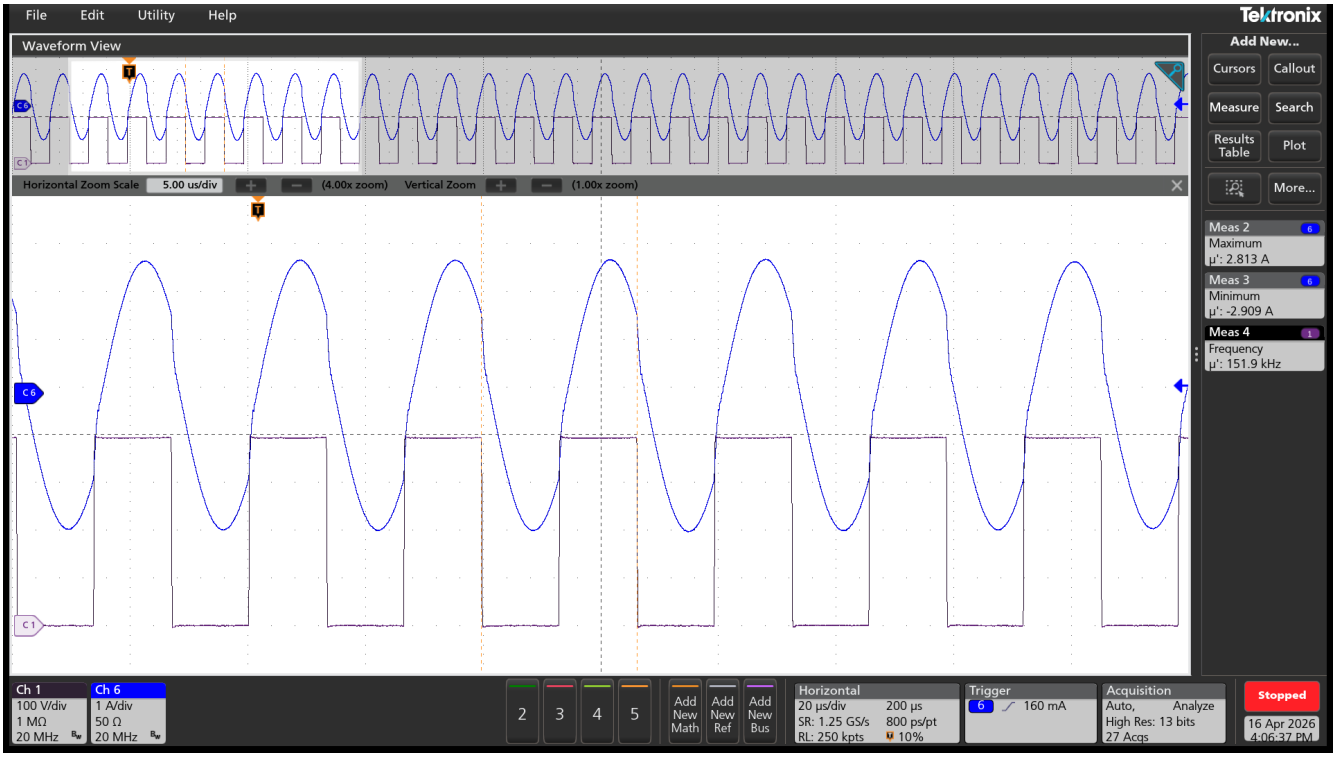


Figure 3-7. Switching Waveform at Peak Load With PS_ON Pull High. System Runs at 151.9KHz

3.1.3 Backlight Switching Waveform

Backlight LLC Switching behavior is shown in Figure 3-8 through Figure 3-11.

CH1 is the waveform of switching node, CH6 is the primary side resonant current.

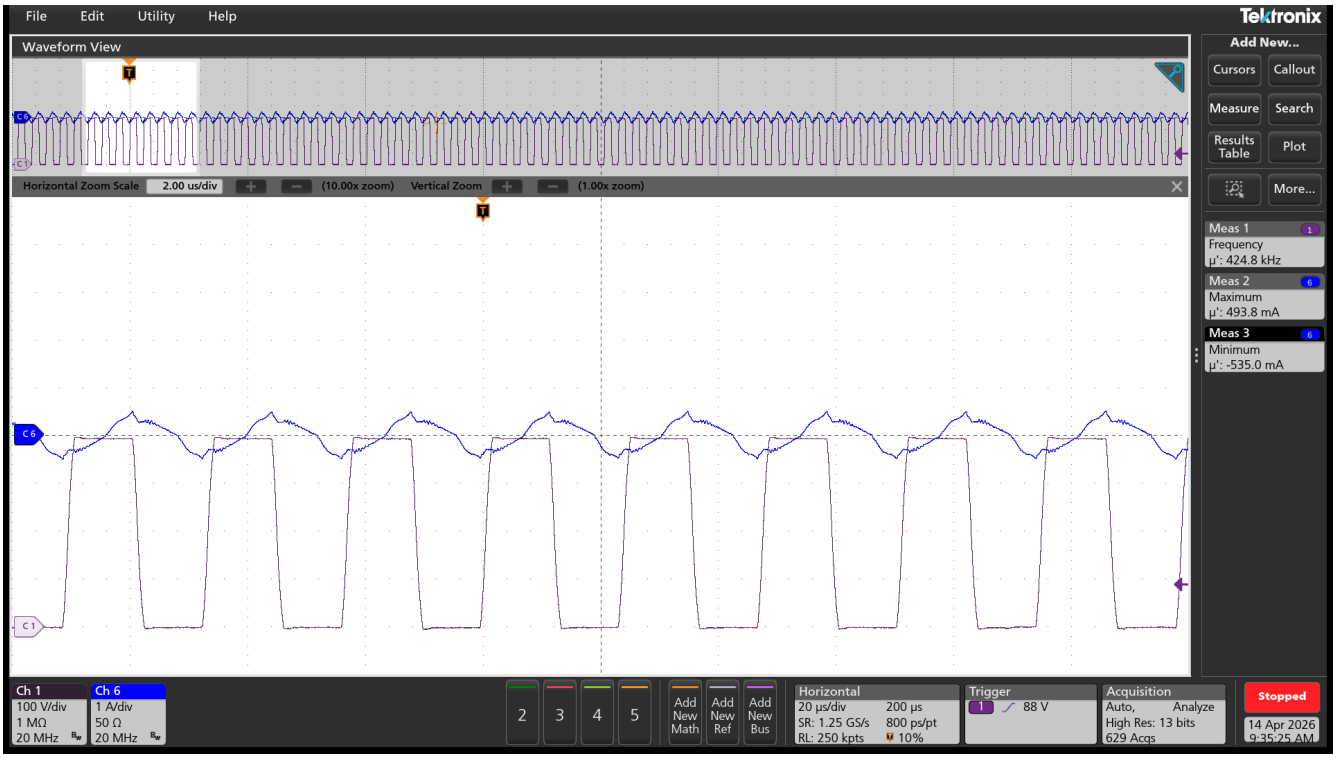


Figure 3-8. Switching Waveform at No Load; System Runs at 424.8KHz

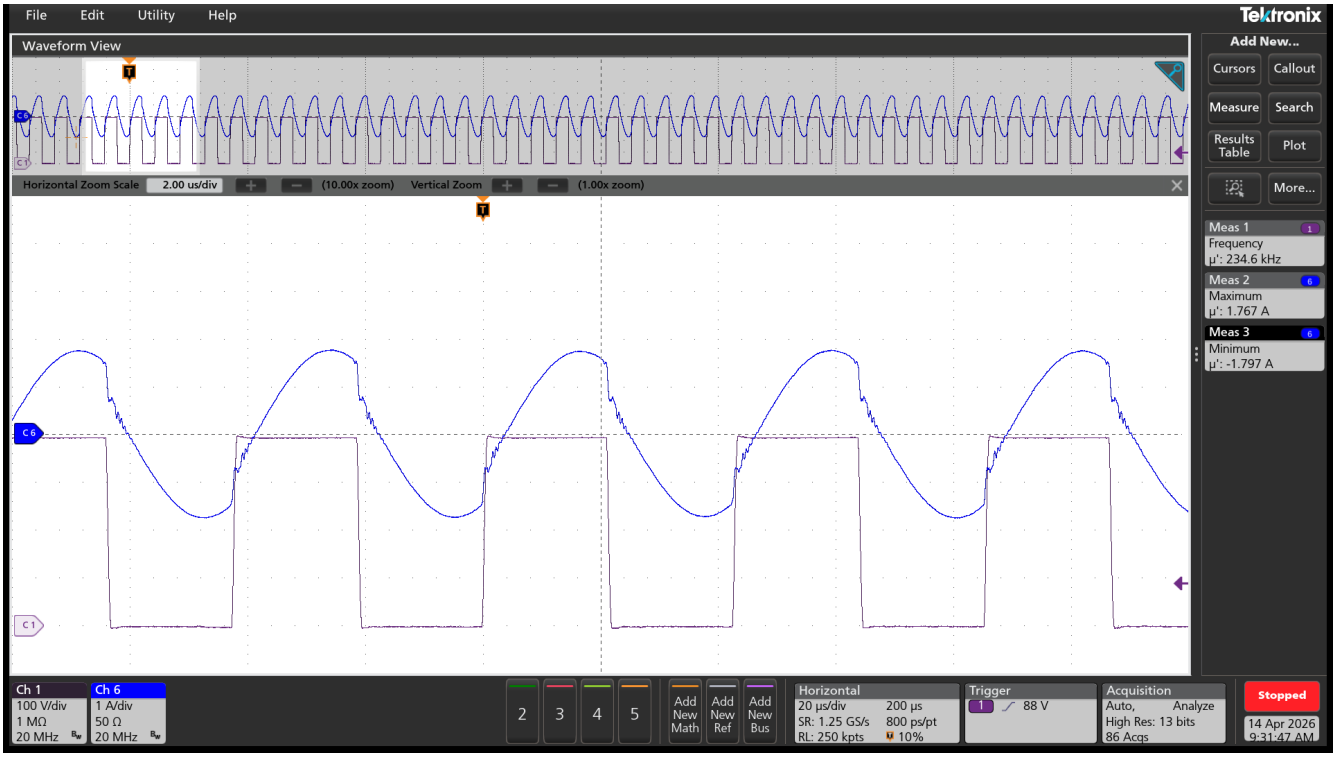


Figure 3-9. Switching Waveform at 18.28V-10A; System Runs at 234.6KHz

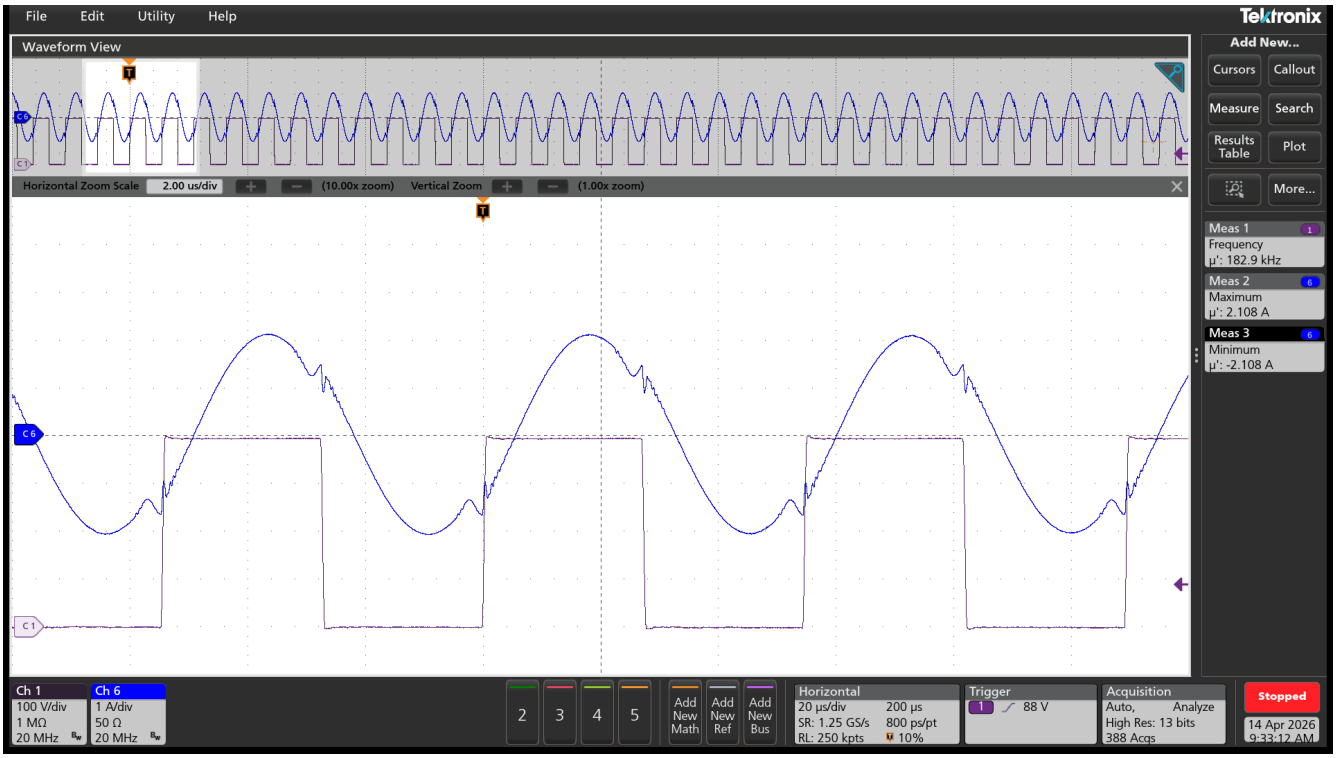


Figure 3-10. Switching Waveform at 20V-10A; System Runs at 182.9KHz

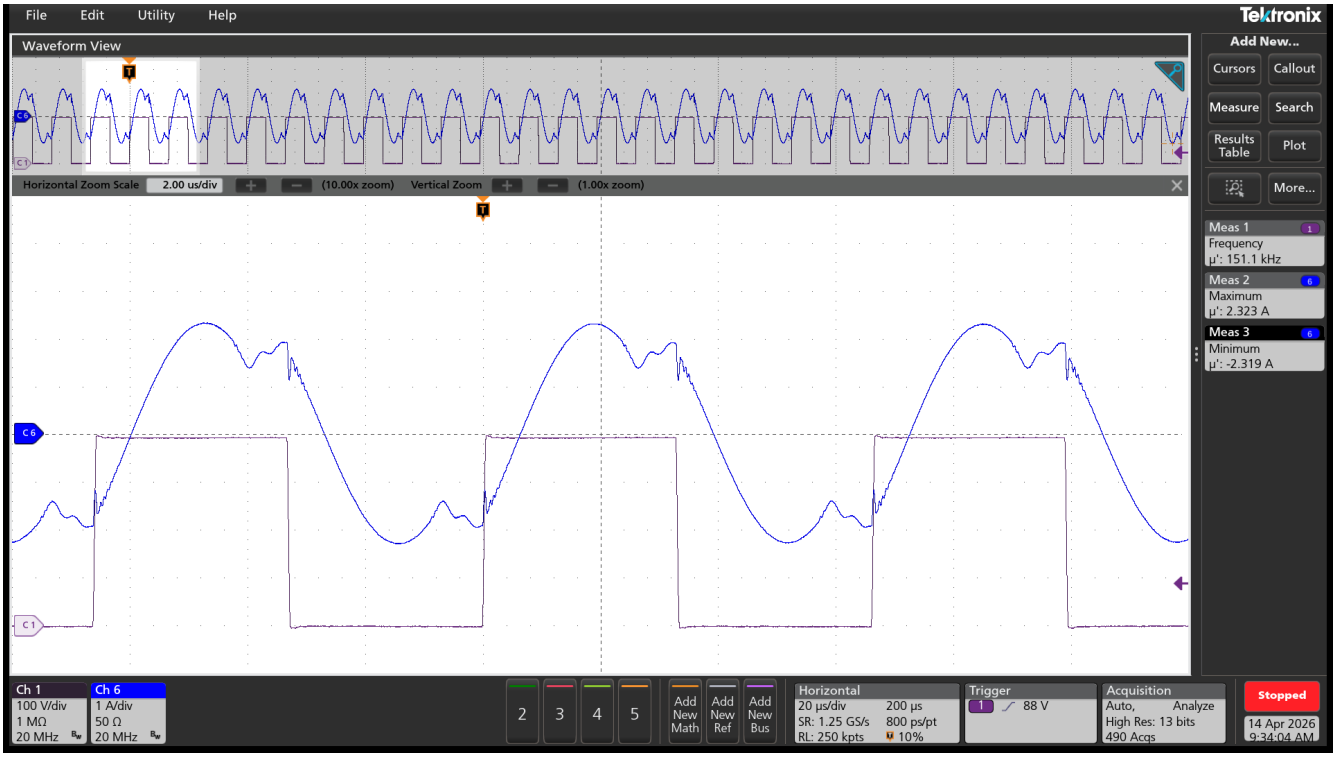


Figure 3-11. Switching Waveform at 22.5V-10A. System Runs at 151.1KHz

3.2 Output Voltage Ripple

3.2.1 System LLC Output Ripple

Output ripple of System LLC is shown in Figure 3-12. The ripple is measured at 12.5V-6A and 25V-1.125A load current

CH2 is the ripple of 12.5V and CH3 is the ripple of 25V.

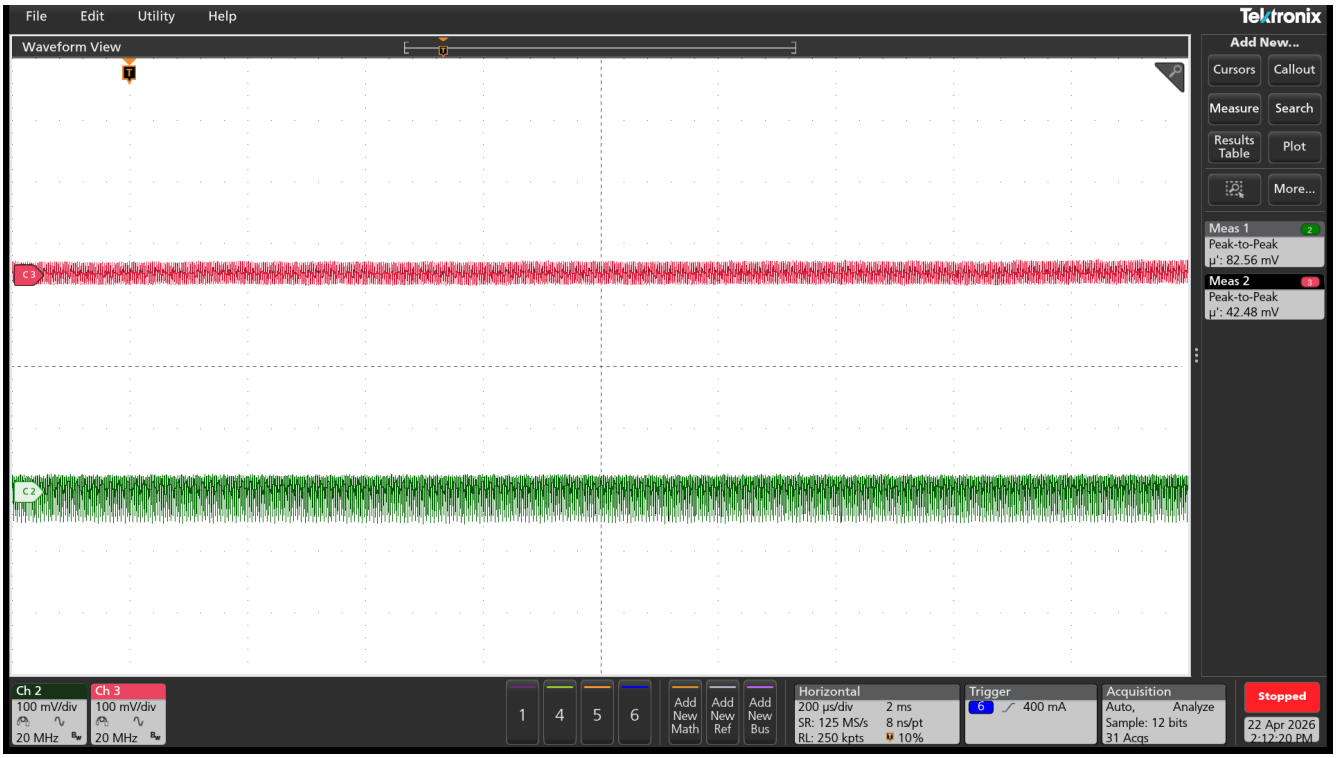


Figure 3-12. Output Voltage Ripple, 12.5V Ripple is 82.56V and 25V Ripple is 42.48V

3.2.2 Backlight LLC Output Ripple

Output ripple of backlight LLC is shown in Figure 3-13 through Figure 3-15.

CH2 is output ripple and CH6 is output current.

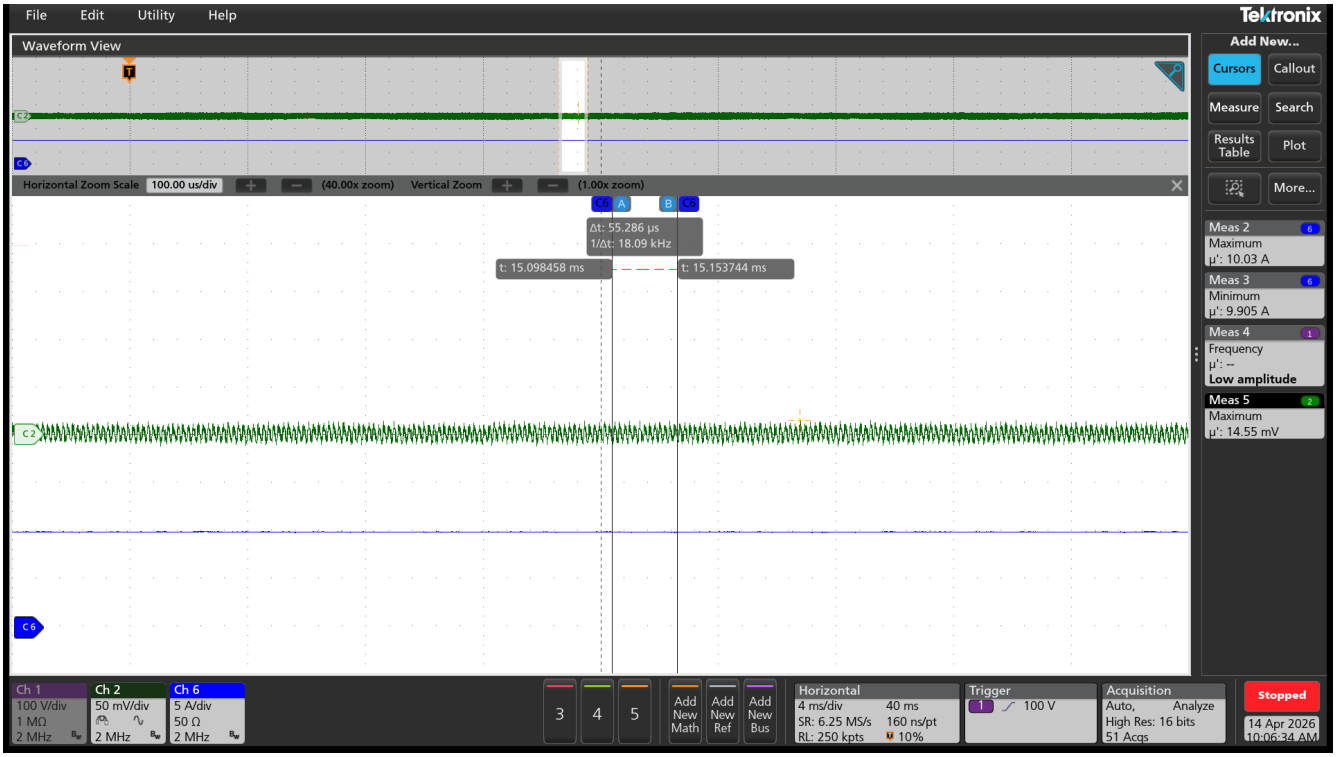


Figure 3-13. Output Voltage at 18.28V-10A; The Output Ripple is About 30mV

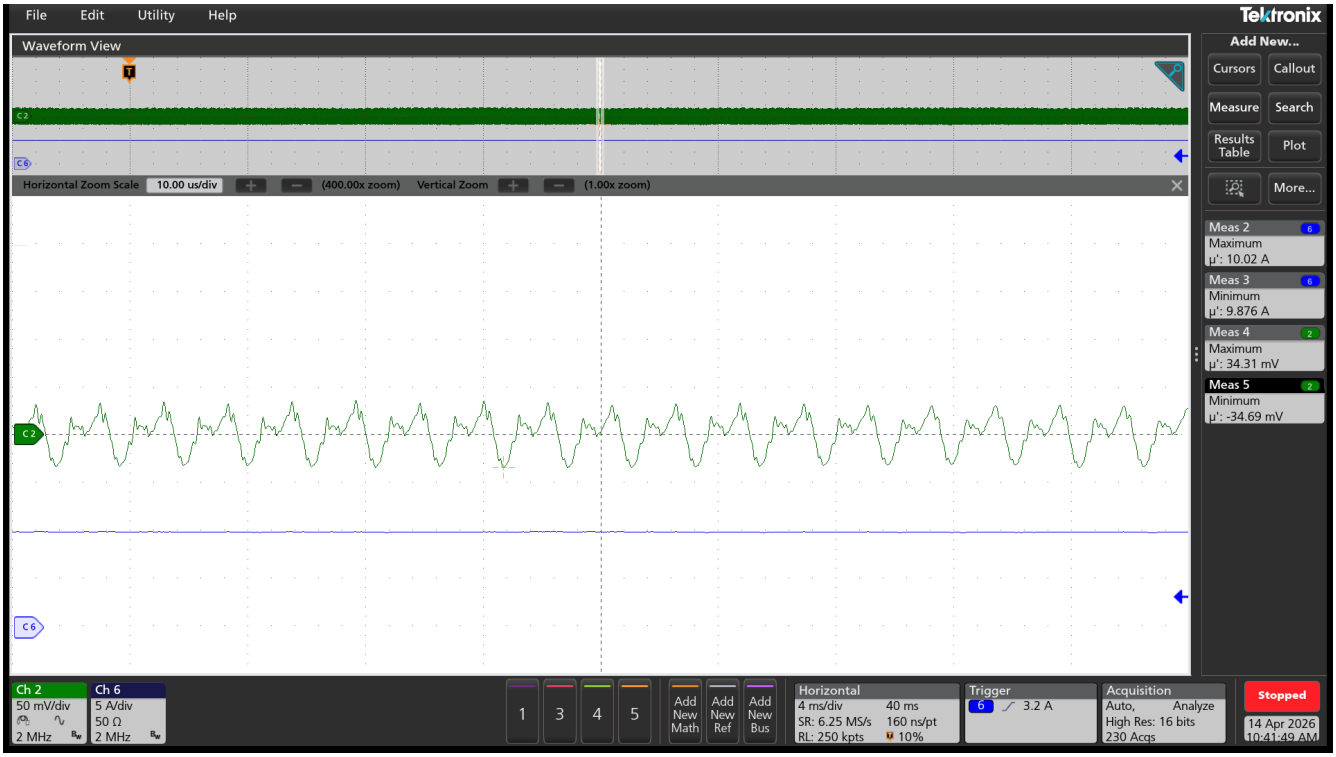


Figure 3-14. Output Voltage Ripple at 20V-10A; The Output Ripple is 69mV

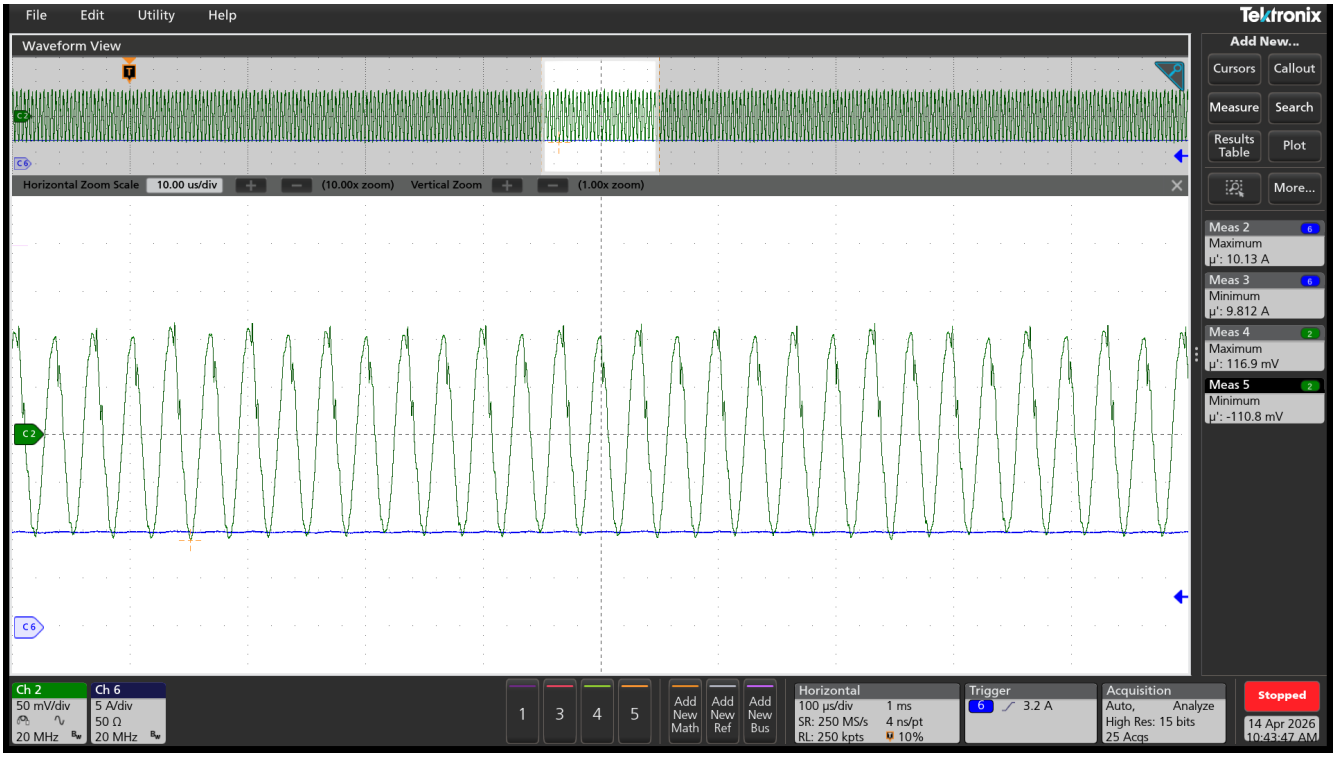


Figure 3-15. Output Voltage Ripple at 22.5V-10A. Output Ripple is 227.7mV

3.3 Dynamic Response

3.3.1 Dynamic Response of the System LLC

Dynamic response of the system LLC is shown in Figure 3-16 and Figure 3-17.

CH2: AC voltage of 12.5V, CH3: AC voltage of 25V, CH6: Output Current

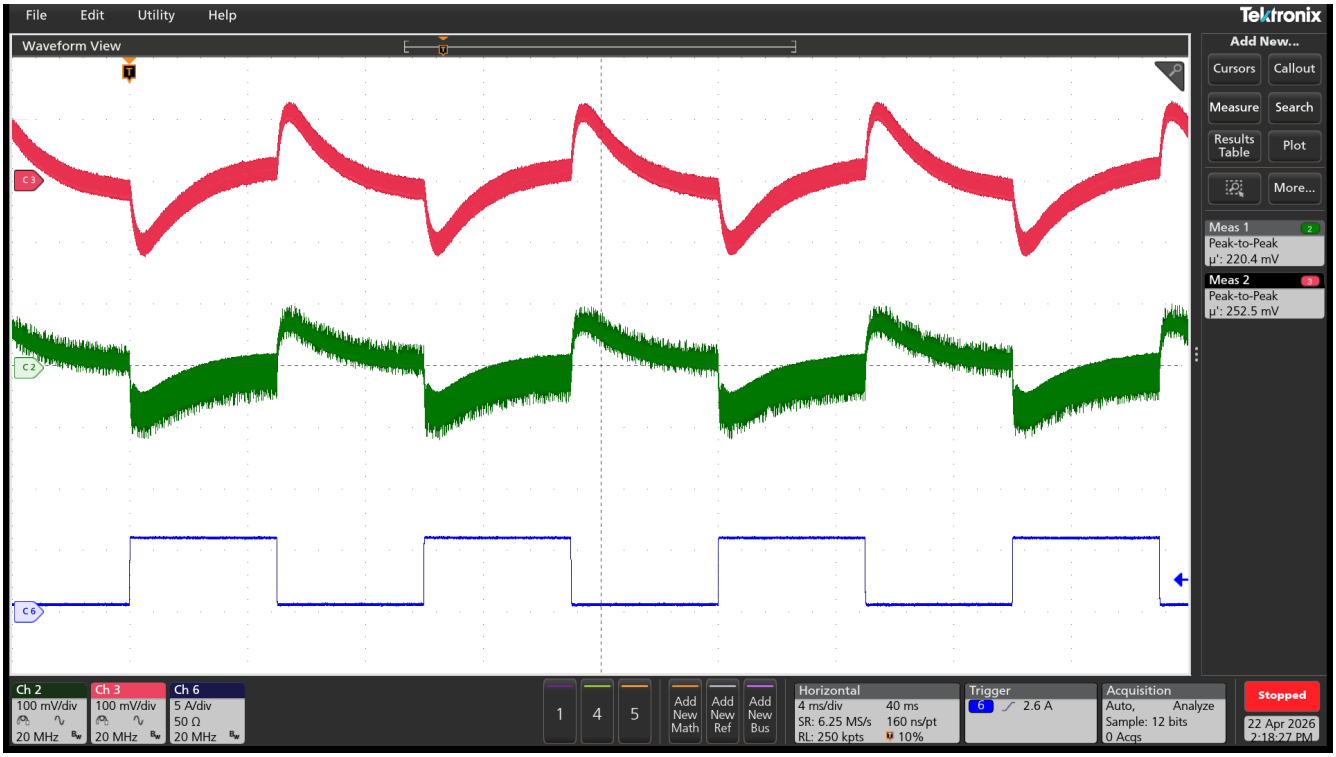


Figure 3-16. System LLC Dynamic Response; Keeps 25V Fixed 1.125A, and 12.5V Swap From 0.6A to 6A

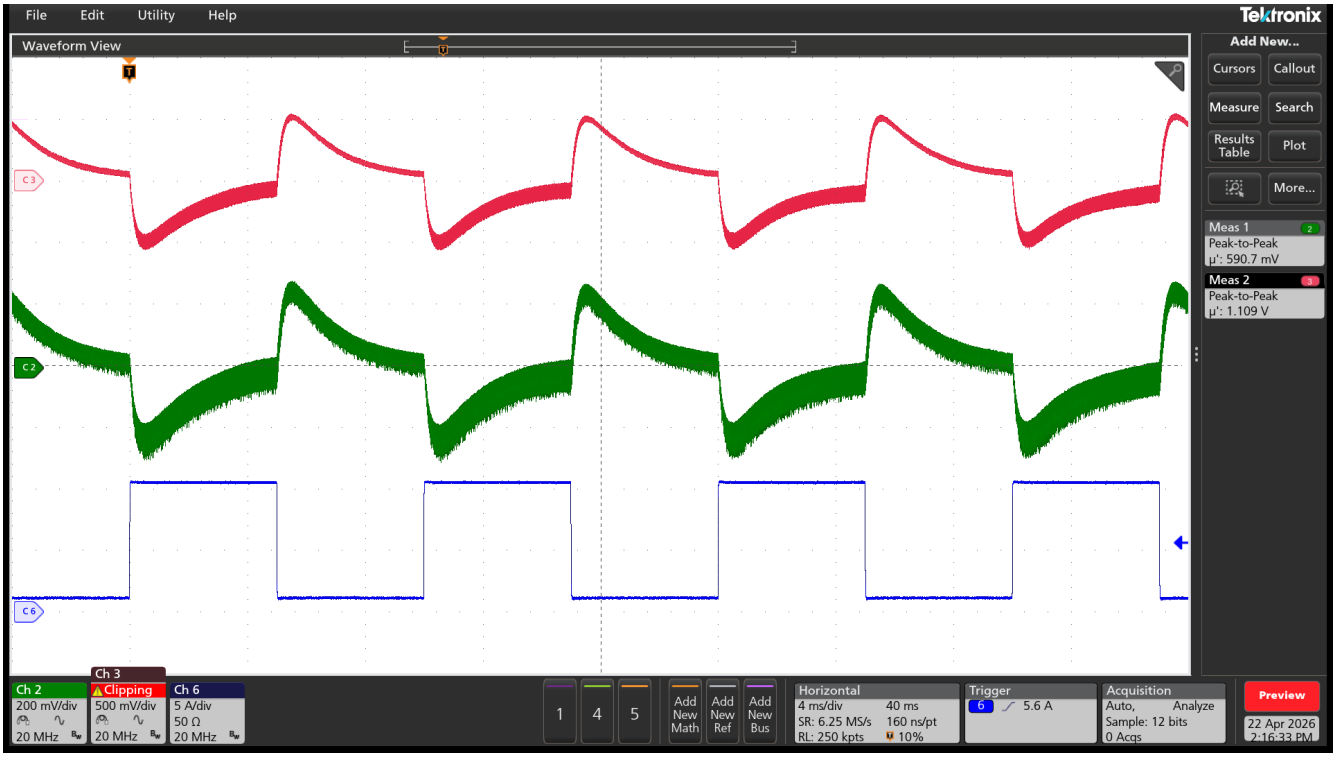


Figure 3-17. System LLC Dynamic Response; Keeps 12.5V Fixed 6A, and 25V Swap From 1.125A to 10.5A

3.3.2 Dynamic Response of the Backlight LLC

Dynamic response of the system LLC at different output voltages is shown in Figure 3-18 through Figure 3-20.

CH2: AC voltage of 12.5V, CH3: AC voltage of 25V, CH6: Output Current

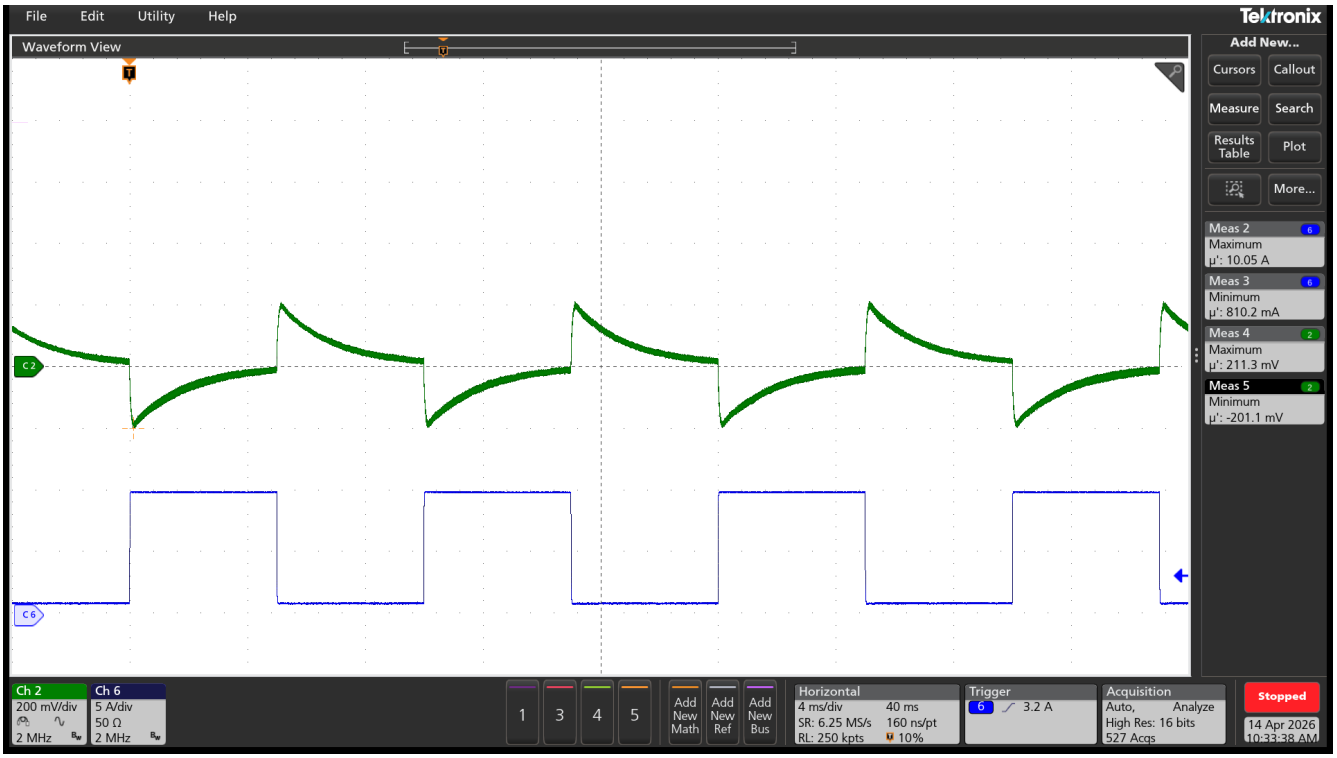


Figure 3-18. Backlight LLC Dynamic Response; V_{out} = 18.28V, Output Load Between 1A to 10A

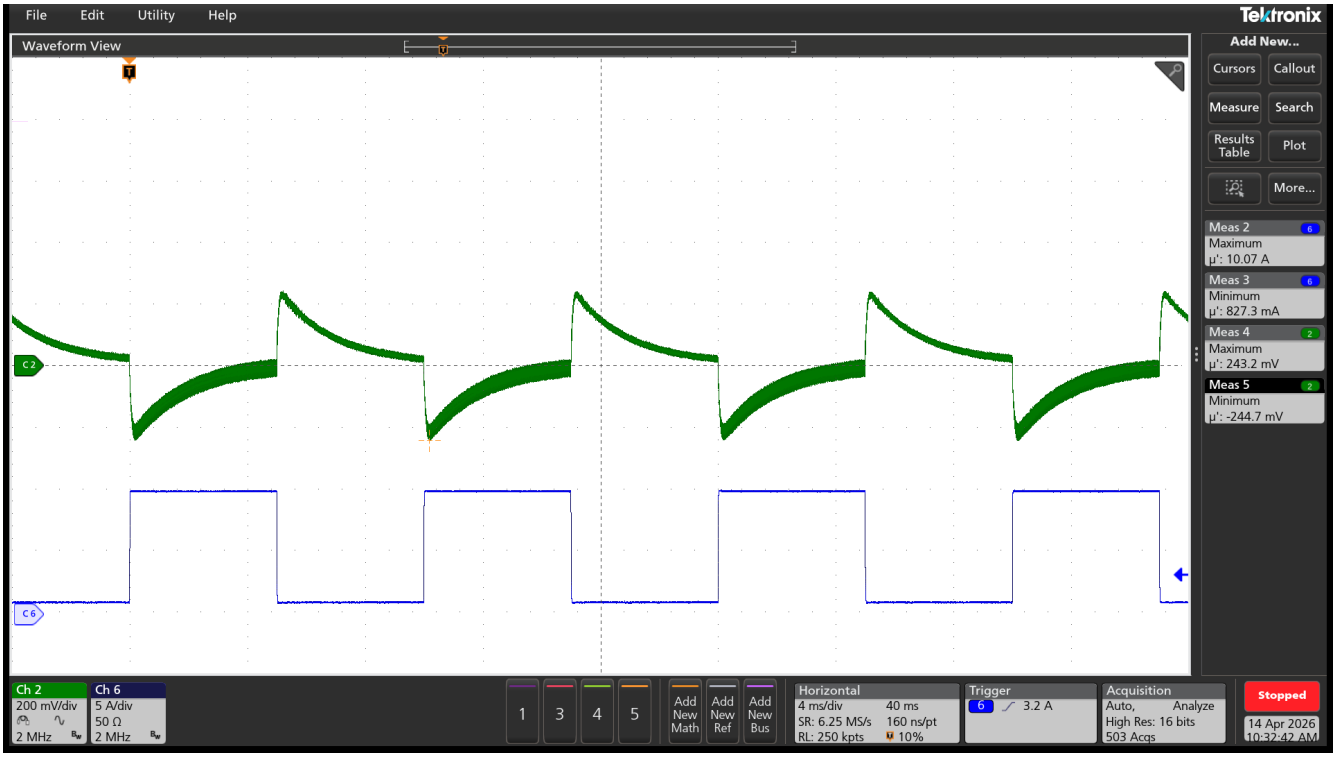


Figure 3-19. Backlight LLC Dynamic Response. V_{out} = 20V, Output Load Between 1A to 10A

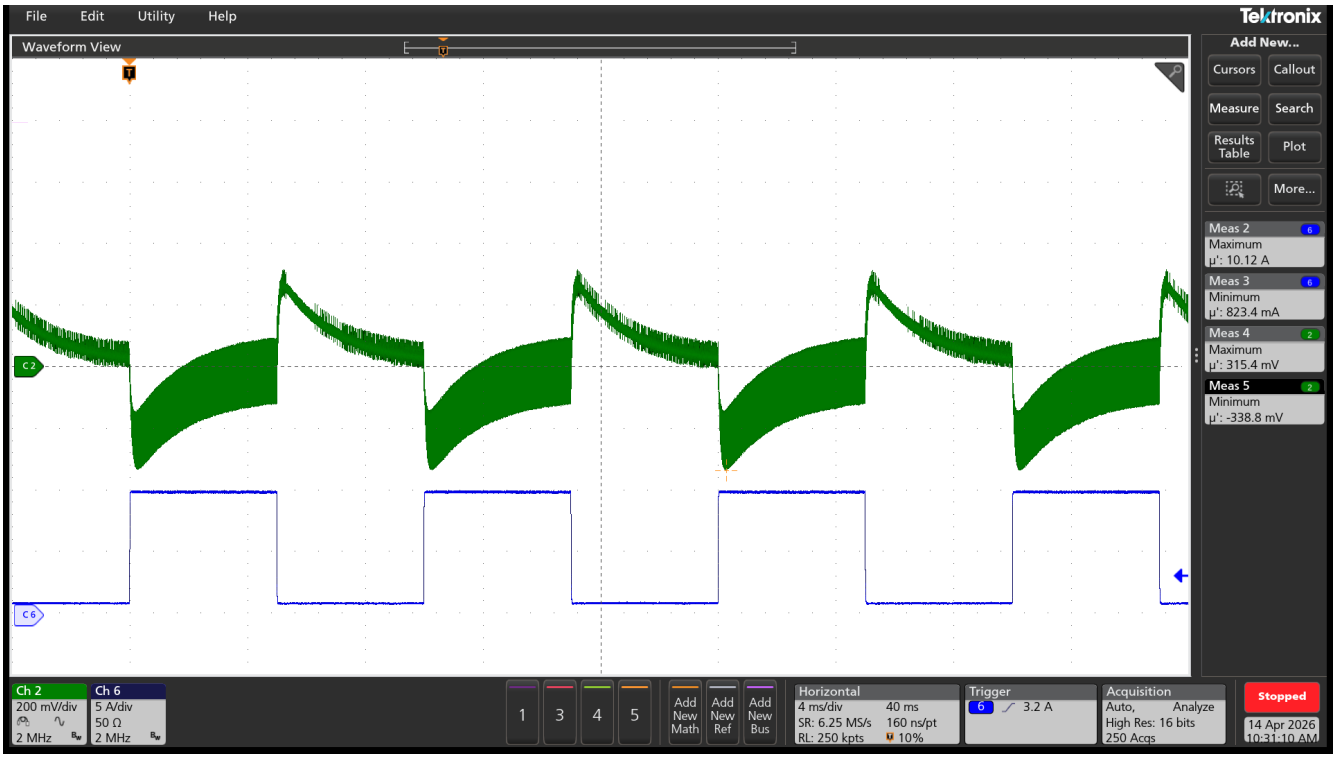


Figure 3-20. Backlight LLC Dynamic Response; V_{out} = 22.5V, Output Load Between 1A to 10A

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