

280W Digital Asymmetrical Half Bridge (AHB) DC-DC Converter Reference Design



Description

This document provides the test report for a digitally controlled asymmetrical half-bridge (AHB) converter, a flyback-derived resonant topology designed for high-efficiency and wide-output power conversion. The control algorithm implements zero-voltage switching (ZVS) control using a fast pulse-width modulation (PWM) on-time calculation and adaptive zero-voltage detection (ZVD) technique to maintain boundary ZVS across varying input and load conditions. The control algorithm also includes programmable zero - crossing detection (ZCD) count control, adaptive soft-start, and inductance compensation algorithms to maintain stable performance under production variations.

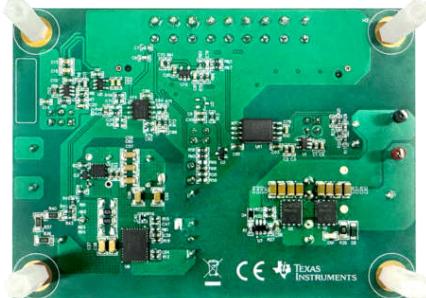
This evaluation board achieves a peak efficiency of 97.8% at 28V and 9A condition; targeting high-power applications (greater than 100W) such as USB PD adapters, industrial chargers, and power tools.

Resources

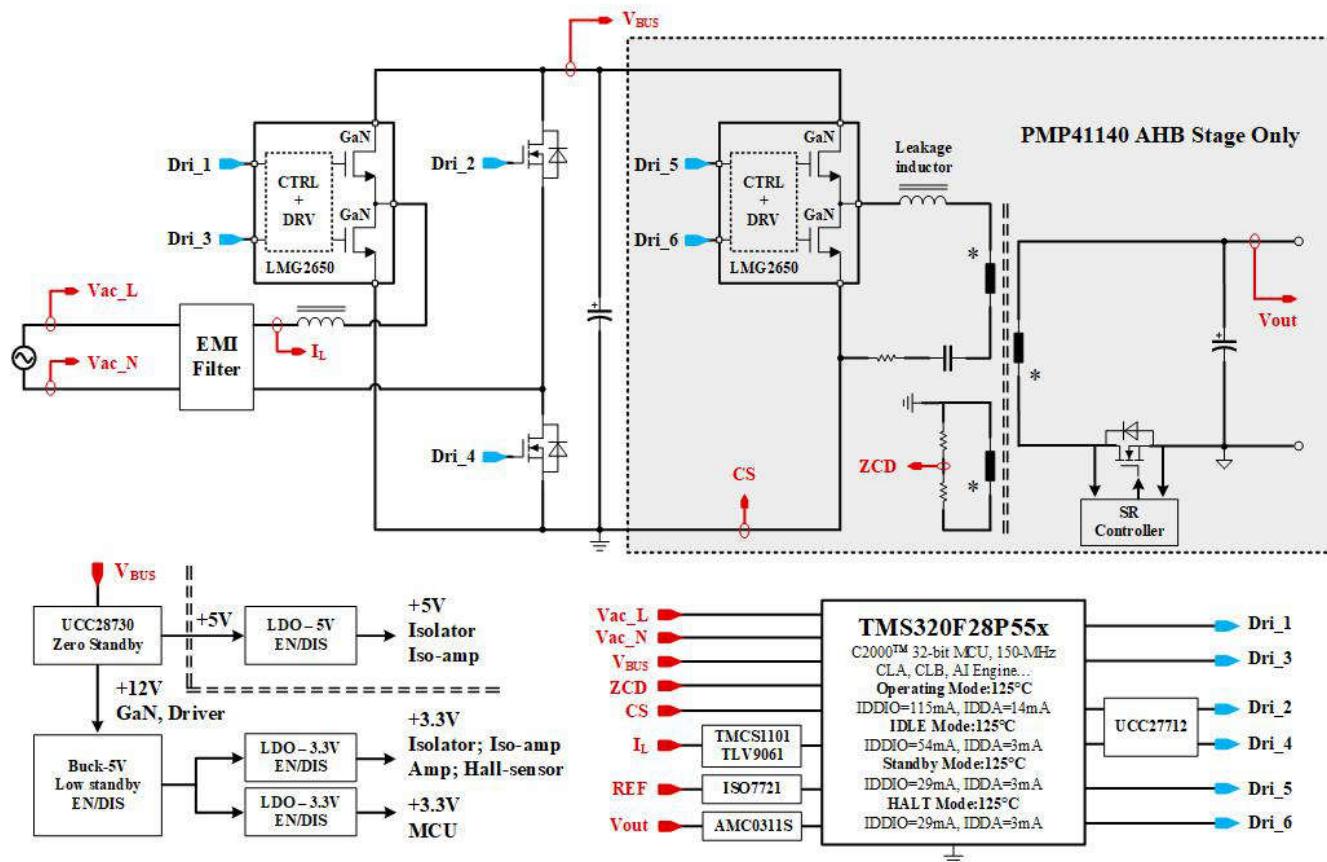
PMP41140	Design Folder
TMDSCNCD28P55X	Product Folder
LMG2650	Product Folder
AMC1311	Product Folder
TPS54202	Product Folder
OPA365	Product Folder



PMP41140 - Top View



PMP41140 - Bottom View



Note

The simplified block diagram demonstrates a whole AD-DC isolated system including Totem-pole PFC stage and Asymmetrical Half Bridge stage, F28P55x series DSP has capability to control both these two stages in one device. PMP41140 reference design board only demonstrates the AHB stage operating for evaluation.

1 Test Prerequisites

1.1 Voltage and Current Requirements

Table 1-1. Voltage and Current Requirements

Parameter	Specifications
Input voltage	300VDC - 420VDC
Input voltage	9VDC - 28VDC
Output current	12AMAX

1.2 Required Equipment

- TMDSCNCD28P55X development tools
- DC Source: Chroma 62150H-1000S
- Electronic load: Chroma 63203A-600-210
- Oscilloscope: Tektronix MDO34

1.3 Safety Warning

Do not touch the board or the electrical circuits while the board is energized because of high voltages capable of causing an electrical shock hazard. Make sure the high voltage is fully discharged before handling the board.

1.4 Dimensions

Length × Width × Height = 100mm × 75mm × 46mm.

1.5 Test Setup

1. For FW setup, please refer to the PMP41140 software user's guide.
2. Plug in control card, download the code and configure necessary parameters.
3. Plug in the external bias supply for primary 12V and secondary 5V.
4. Short J3 with jumper.
5. Connect DC source and electronic load.
6. Power up DC source higher than 300V, then 9V default output voltage is built up.

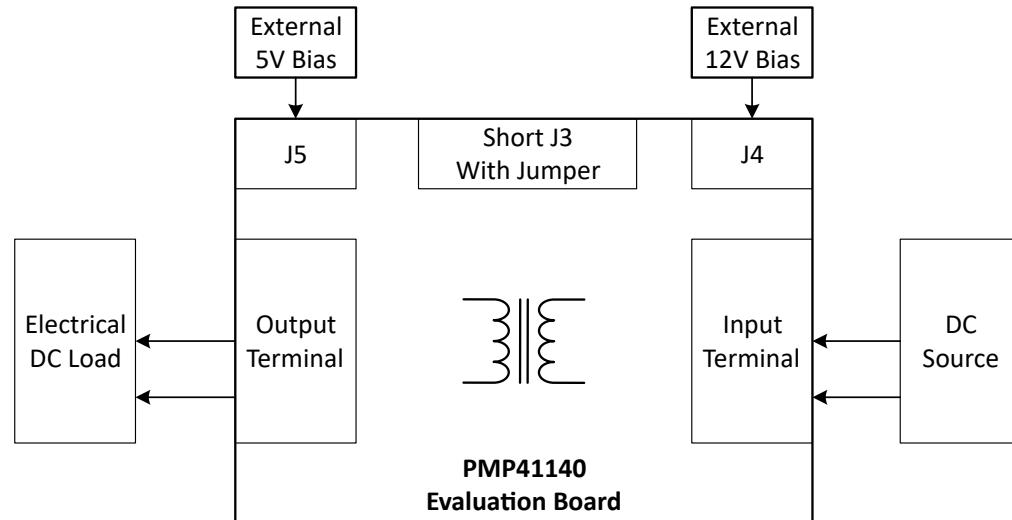


Figure 1-1. Test Setup For Hardware

2 Testing and Results

2.1 Efficiency Graphs

Efficiency is shown in [Figure 2-1](#).

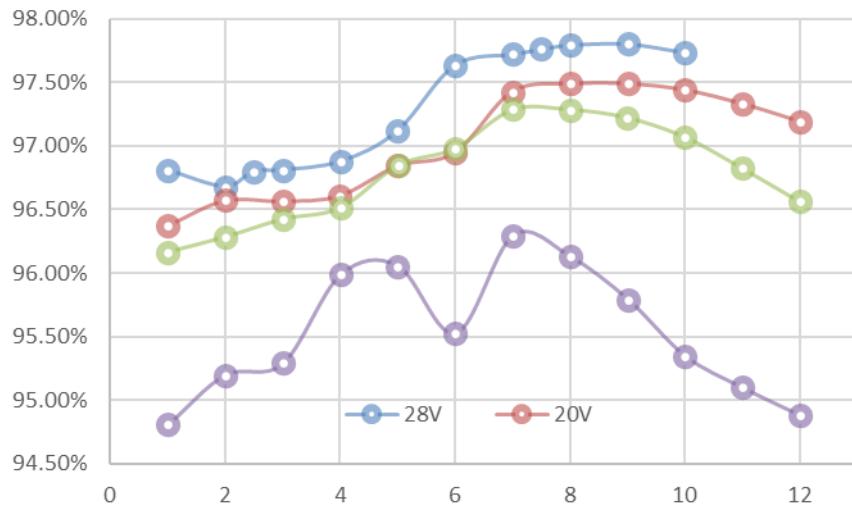


Figure 2-1. Efficiency Graph

2.2 Efficiency Data

Efficiency data is shown in [Table 2-1](#) through [Table 2-4](#).

Table 2-1. Efficiency Results With 28V Output

VIN (V)	VOUT (V)	IOUT (A)	PIN (W)	POUT (W)	PLOSS (W)	Efficiency (%)
390	28.253	9.9928	288.86	282.3266	6.5334	97.74%
390	28.261	9.0028	260.14	254.4281	5.7119	97.80%
390	28.252	7.9978	231.05	225.9538	5.0962	97.79%
390	28.256	7.5019	216.83	211.9737	4.8563	97.76%
390	28.195	7.0088	202.22	197.6131	4.6069	97.72%
390	28.303	6.0038	174.04	169.9256	4.1144	97.64%
390	28.242	4.9988	145.37	141.1761	4.1939	97.12%
390	28.251	4.0097	116.93	113.278	3.6520	96.88%
390	28.243	3.0047	87.658	84.86174	2.7963	96.81%
390	28.233	2.5022	72.981	70.64461	2.3364	96.80%
390	28.239	2.0025	58.491	56.5486	1.9424	96.68%
390	28.215	0.9994	29.127	28.19807	0.9289	96.81%

Table 2-2. Efficiency Results With 20V Output

VIN (V)	VOUT (V)	IOUT (A)	PIN (W)	POUT (W)	PLOSS (W)	Efficiency (%)
390	20.181	11.993	249.02	242.0307	6.9893	97.19%
390	20.181	11.004	228.16	222.0717	6.0883	97.33%
390	20.18	9.9984	207.07	201.7677	5.3023	97.44%
390	20.233	9.0084	186.96	182.267	4.6930	97.49%
390	20.181	8.0044	165.7	161.5368	4.1632	97.49%
390	20.176	6.9984	144.93	141.1997	3.7303	97.43%

Table 2-2. Efficiency Results With 20V Output (continued)

VIN (V)	VOUT (V)	IOUT (A)	PIN (W)	POUT (W)	PLOSS (W)	Efficiency (%)
390	20.181	6.0084	125.07	121.2555	3.8145	96.95%
390	20.118	5.0044	103.96	100.6785	3.2815	96.84%
390	20.177	3.9994	83.528	80.69589	2.8321	96.61%
390	20.177	3.0084	62.859	60.70049	2.1585	96.57%
390	20.178	2.0044	41.881	40.44478	1.4362	96.57%
390	20.177	1.0003	20.943	20.18305	0.7599	96.37%

Table 2-3. Efficiency Results With 15V Output

VIN (V)	VOUT (V)	IOUT (A)	PIN (W)	POUT (W)	PLOSS (W)	Efficiency (%)
390	15.134	11.999	188.06	181.5929	6.4671	96.56%
390	15.106	10.994	171.52	166.0754	5.4446	96.83%
390	15.115	10.003	155.76	151.1953	4.5647	97.07%
390	15.131	8.9981	140.04	136.1503	3.8897	97.22%
390	15.124	8.0091	124.51	121.1296	3.3804	97.29%
390	15.119	7.0041	108.85	105.895	2.9550	97.29%
390	15.124	5.9991	93.556	90.73039	2.8256	96.98%
390	15.119	5.0091	78.197	75.73258	2.4644	96.85%
390	15.117	4.005	62.73	60.54359	2.1864	96.51%
390	15.126	2.9981	47.031	45.34926	1.6817	96.42%
390	15.116	2.0091	31.541	30.36956	1.1714	96.29%
390	15.111	1.005	15.792	15.18656	0.6054	96.17%

Table 2-4. Efficiency Results With 9V Output

VIN (V)	VOUT (V)	IOUT (A)	PIN (W)	POUT (W)	PLOSS (W)	Efficiency (%)
390	9.081	12.002	114.87	108.9902	5.8798	94.88%
390	9.1	10.997	105.23	100.0727	5.1573	95.10%
390	9.077	9.9919	95.12	90.69648	4.4235	95.35%
390	9.069	9.0019	85.225	81.63823	3.5868	95.79%
390	9.066	7.9978	75.429	72.50805	2.9209	96.13%
390	9.072	7.0069	66.013	63.5666	2.4464	96.29%
390	9.074	6.0019	57.013	54.46124	2.5518	95.52%
390	9.076	4.9959	47.205	45.34279	1.8622	96.06%
390	9.08	4.0069	37.904	36.38265	1.5213	95.99%
390	9.072	3.0009	28.57	27.22416	1.3458	95.29%
390	9.059	1.9959	18.993	18.08086	0.9121	95.20%
390	9.068	1.0059	9.621	9.121501	0.4995	94.81%

2.3 Thermal Images

The thermal image is shown in [Figure 2-2](#) through [Figure 2-5](#).

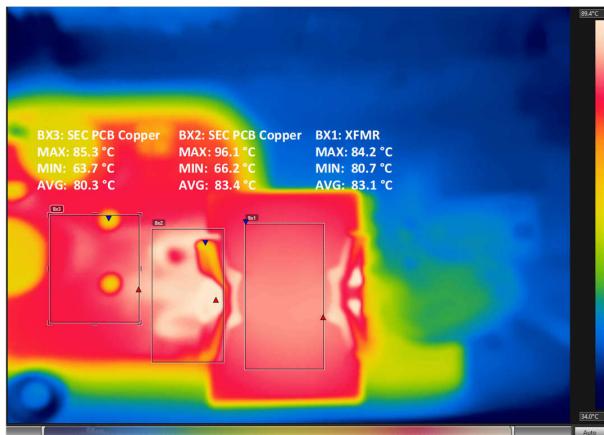


Figure 2-2. Thermal Image of 28V at 10A - Top View

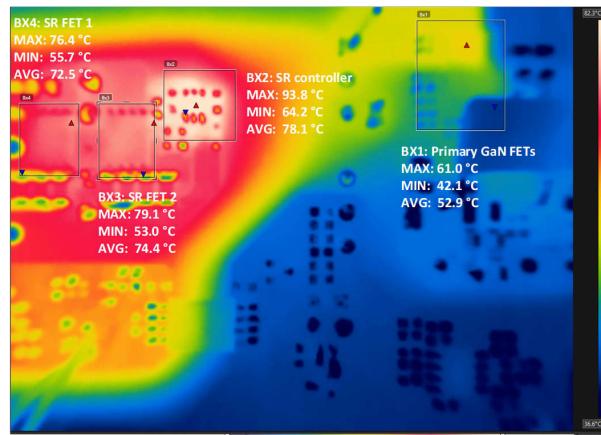


Figure 2-3. Thermal Image of 28V at 10A - Bottom View

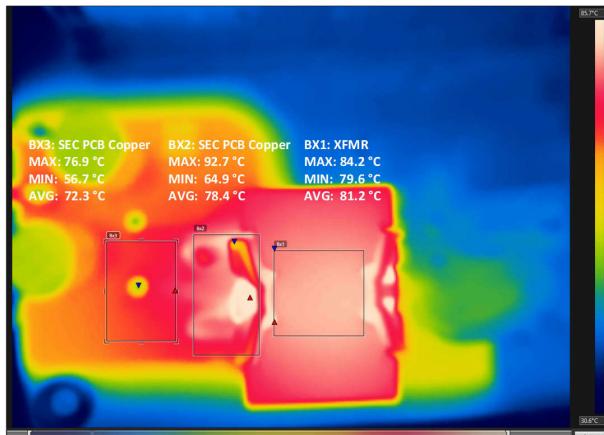


Figure 2-4. Thermal Image of 20V at 12A - Top View

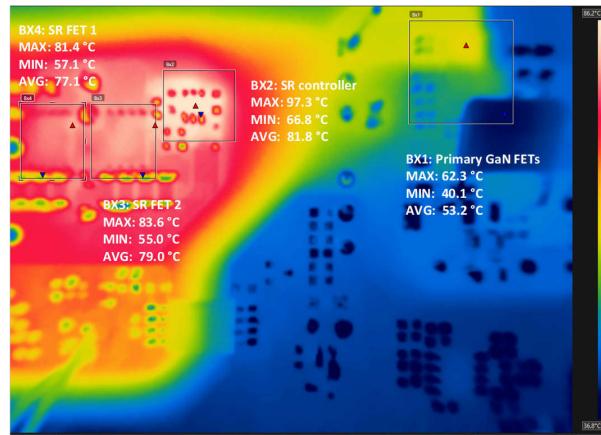


Figure 2-5. Thermal Image of 20V at 12A - Bottom View

3 Waveforms

3.1 Switching

Switching behavior waveforms are shown in [Figure 3-1](#) through [Figure 3-8](#).

CH1 (Gray): Primary switching node voltage (100V/div)

CH2 (Red): Primary resonant current (1A/div)

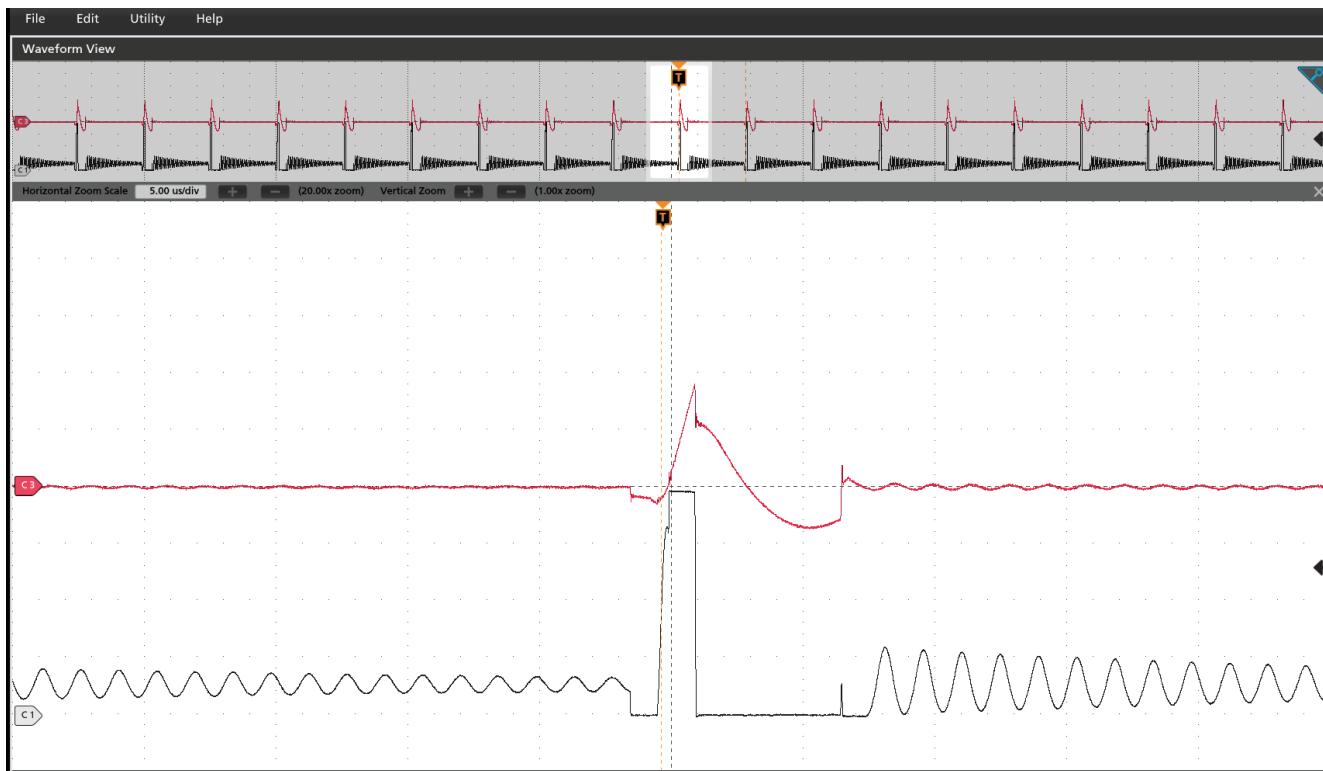


Figure 3-1. Switching Waveforms of 9V at 1A Output

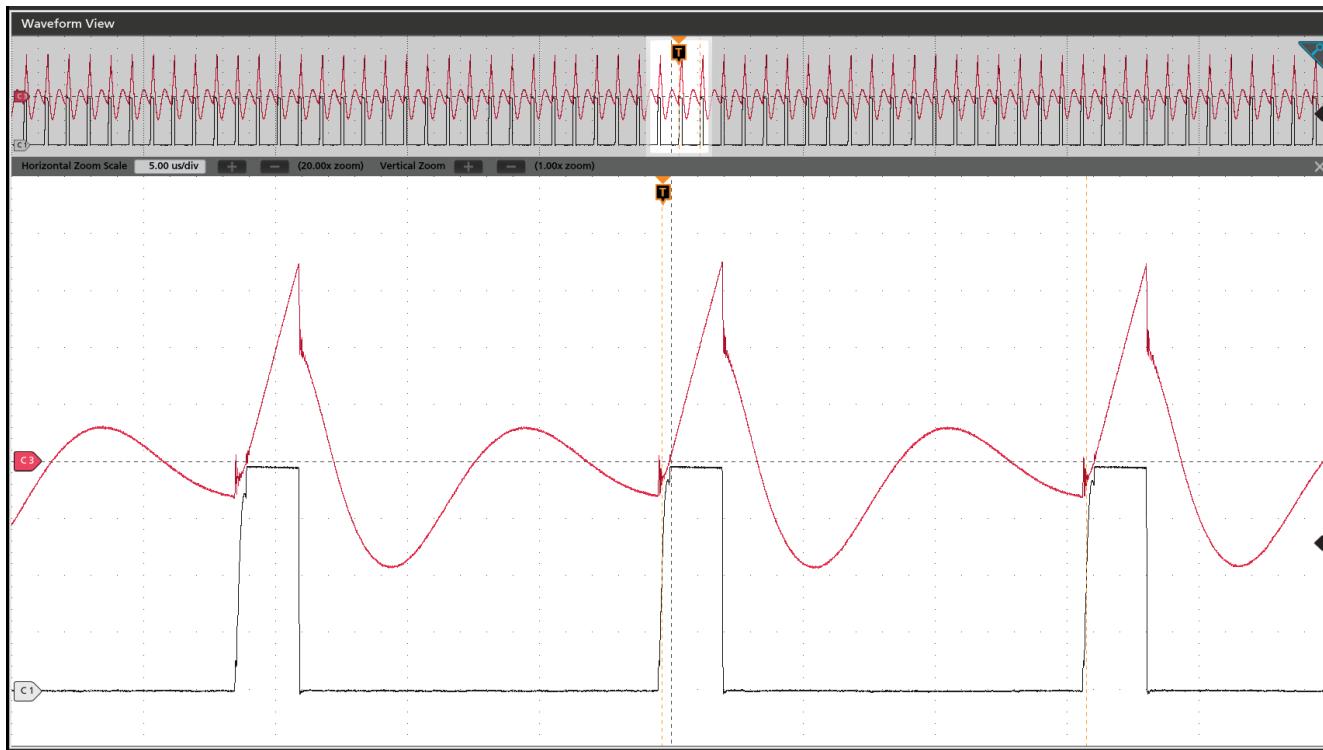


Figure 3-2. Switching Waveforms of 9V at 12A Output

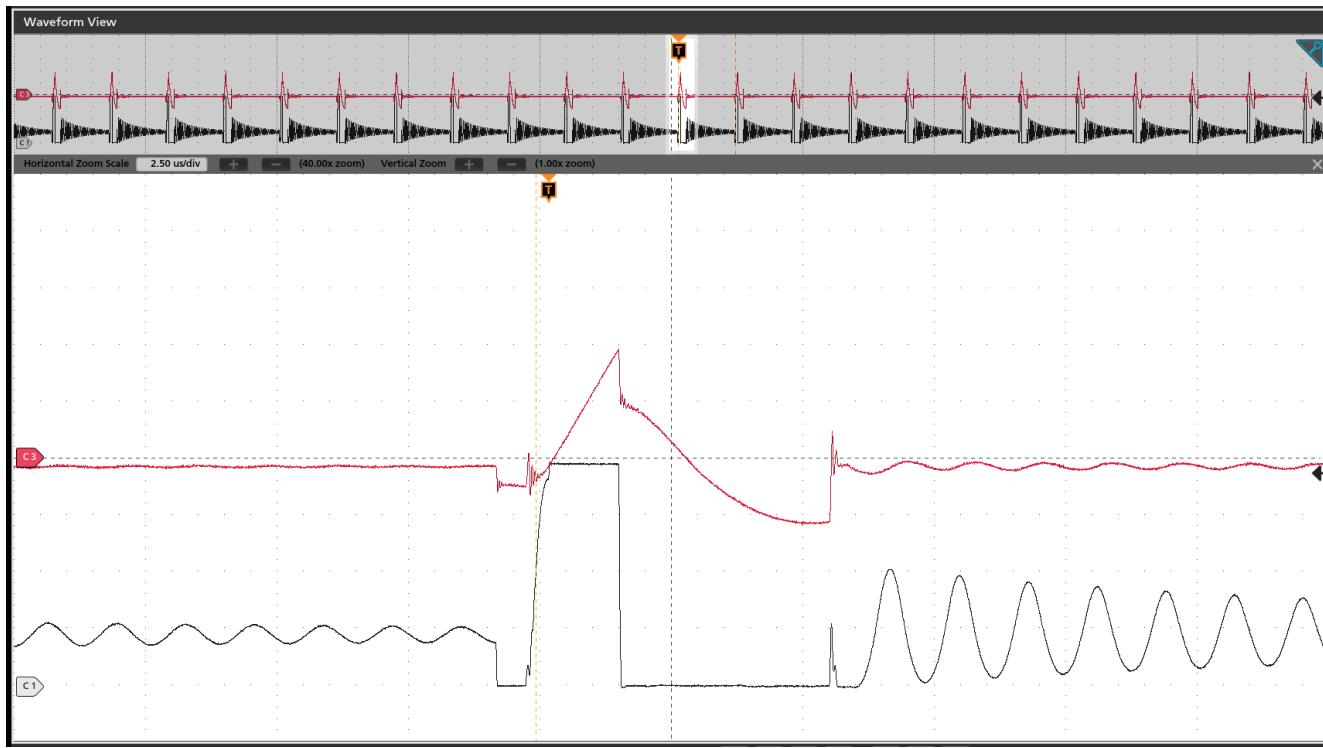


Figure 3-3. Switching Waveforms of 15V at 1A Output

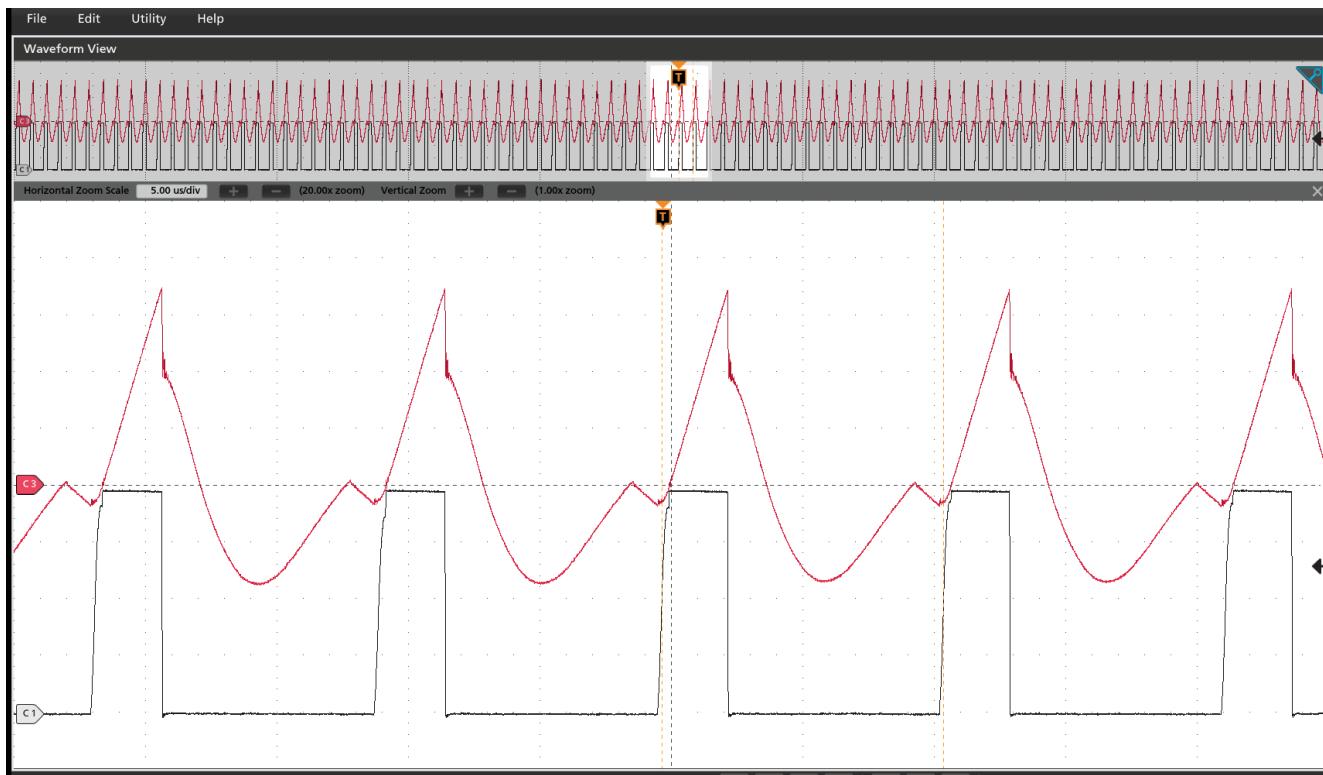


Figure 3-4. Switching Waveforms of 15V at 12A Output

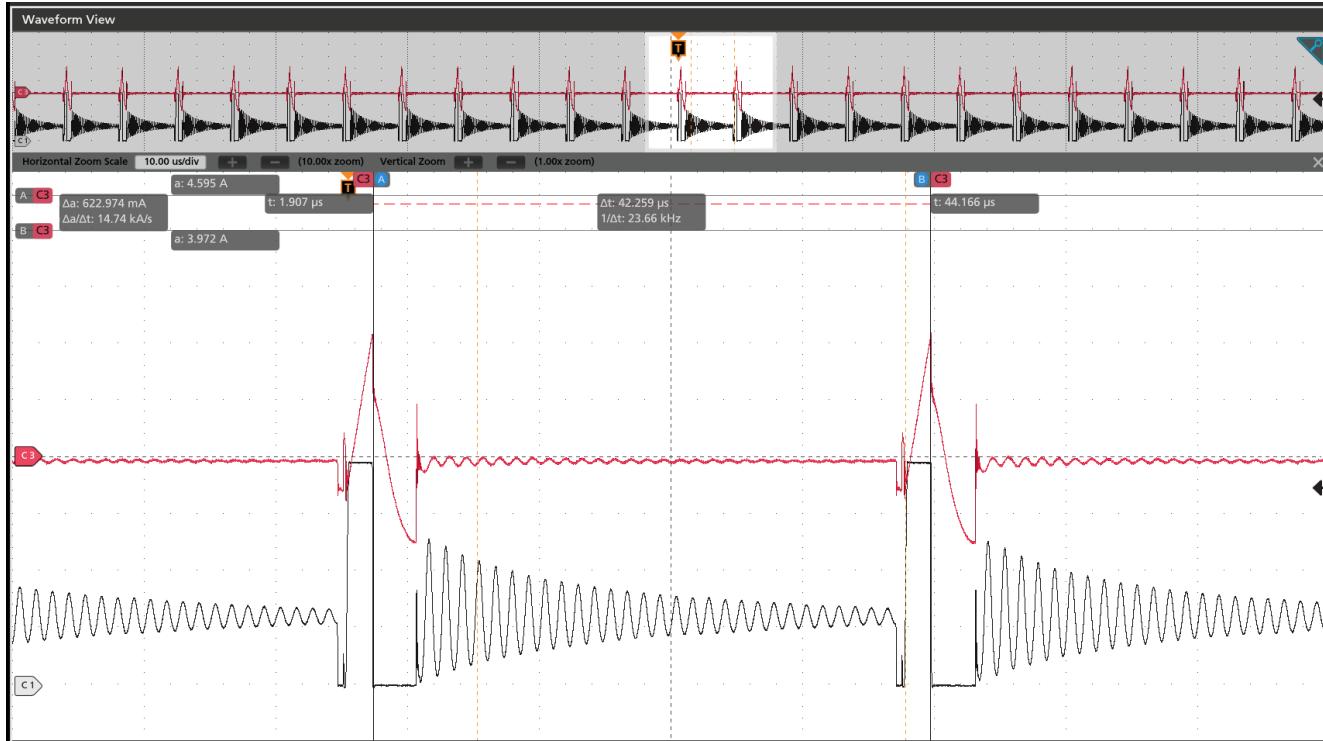


Figure 3-5. Switching Waveforms of 20V at 1A Output

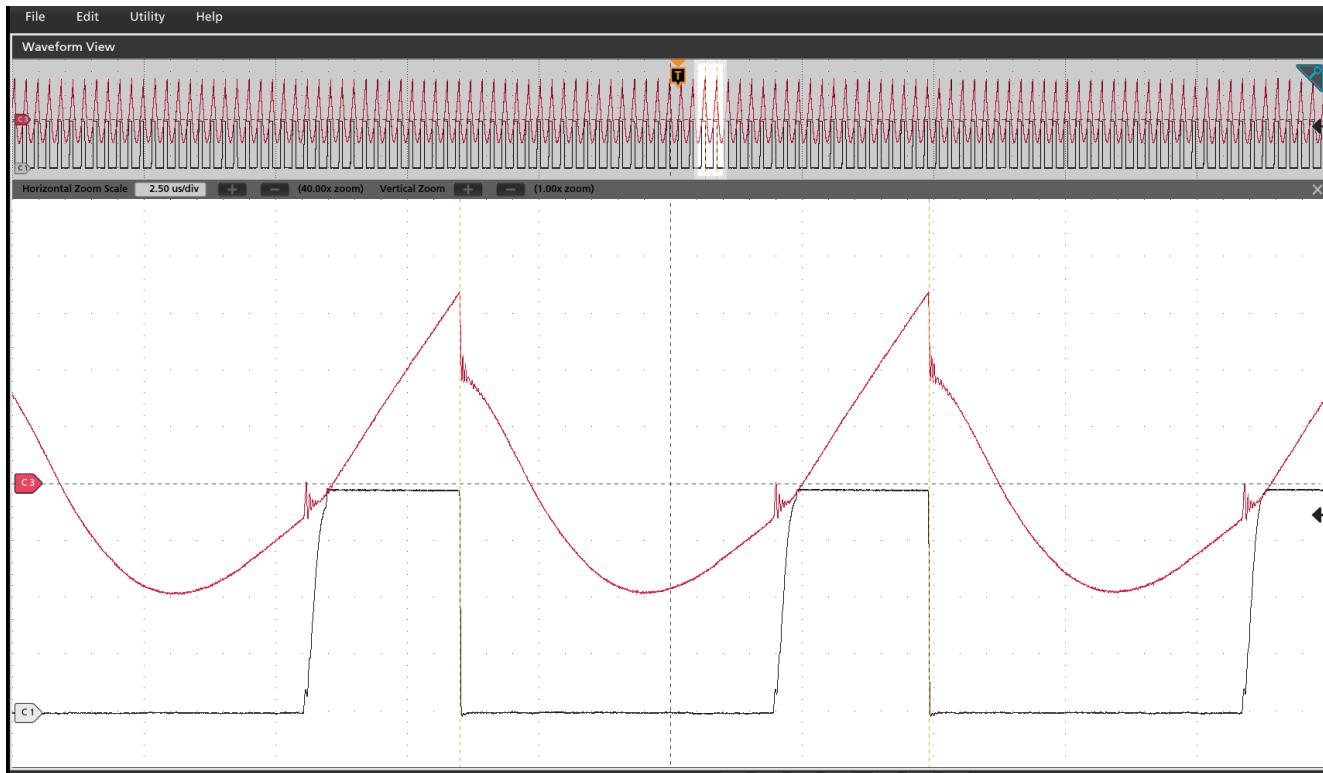


Figure 3-6. Switching Waveforms of 20V at 12A Output

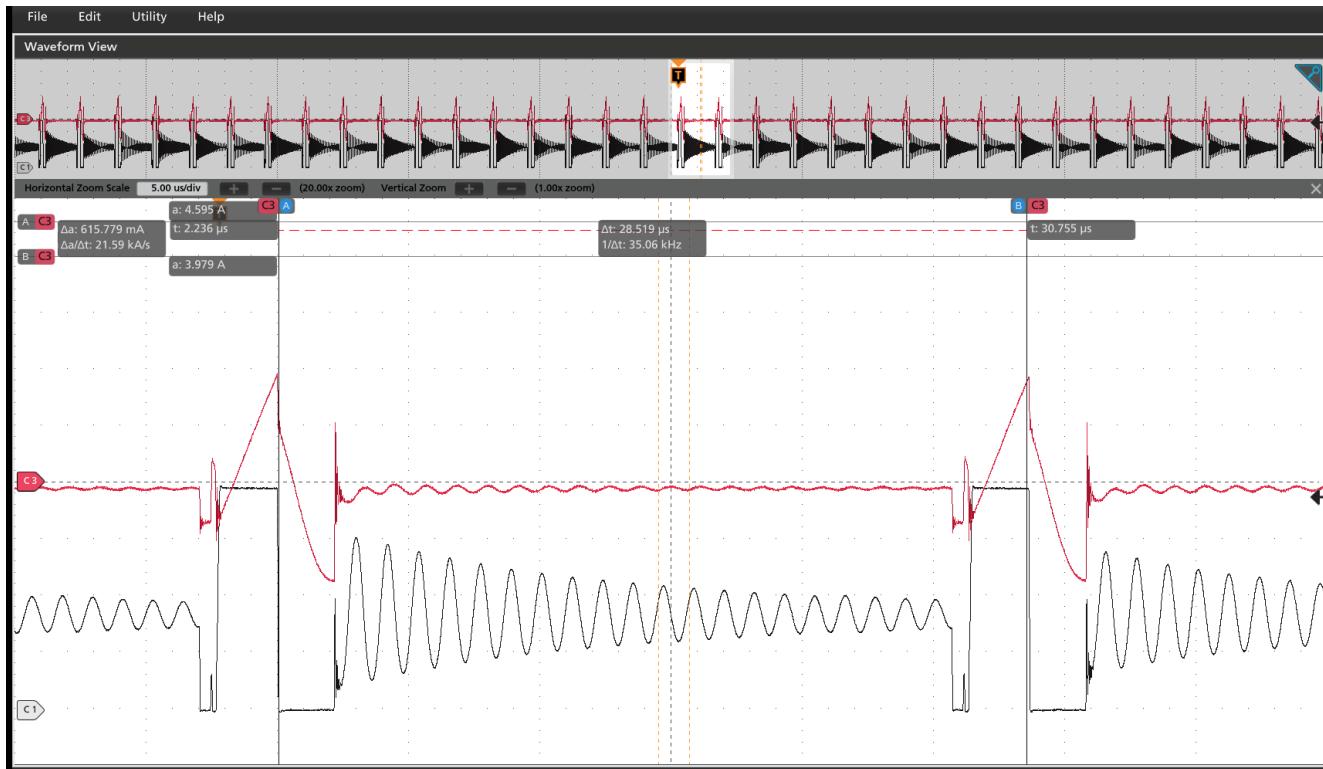


Figure 3-7. Switching Waveforms of 28V at 1A Output

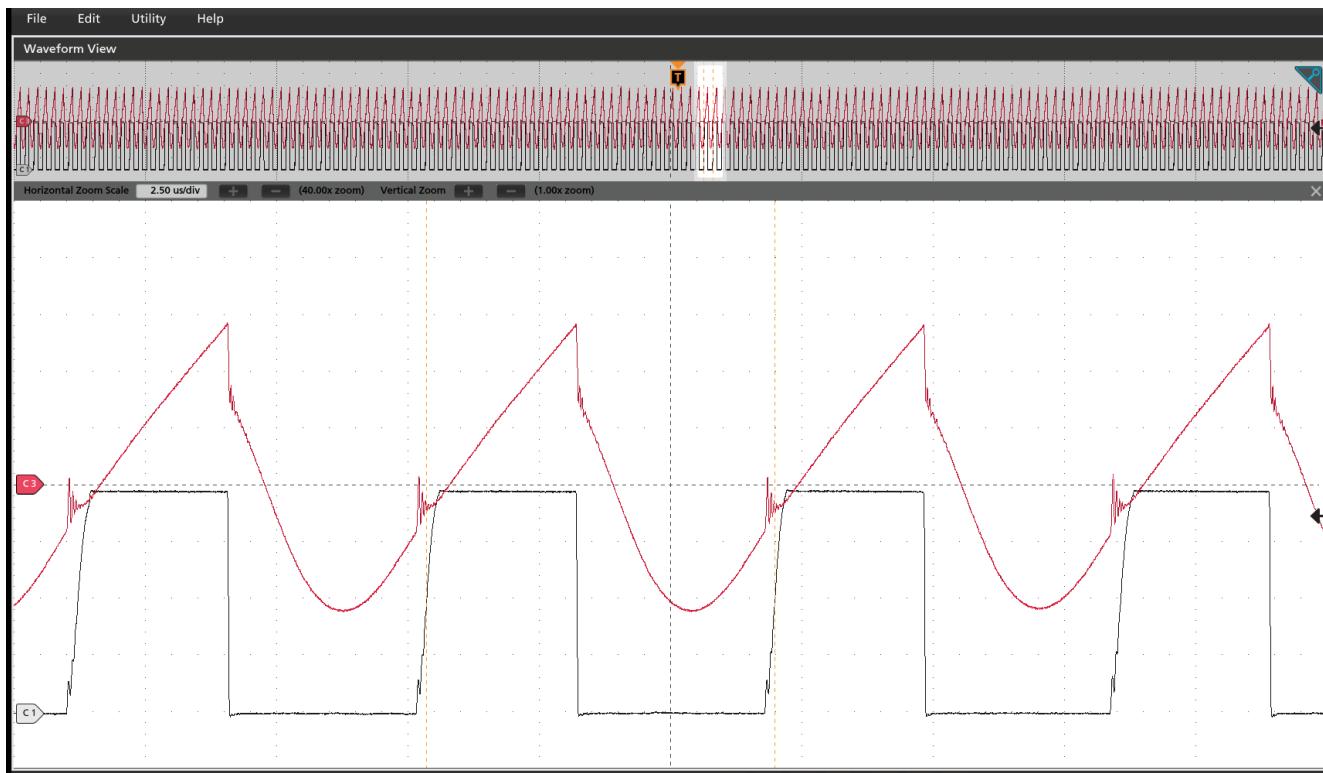


Figure 3-8. Switching Waveforms of 28V at 10A Output

3.2 Start-up Sequence

Start-up behavior waveforms are shown in [Figure 3-9](#).

CH1 (Dark Blue): LS PWM

CH2 (Light Blue): Primary switching node voltage

CH3 (Green): Primary resonant current

CH4 (Red): Output voltage

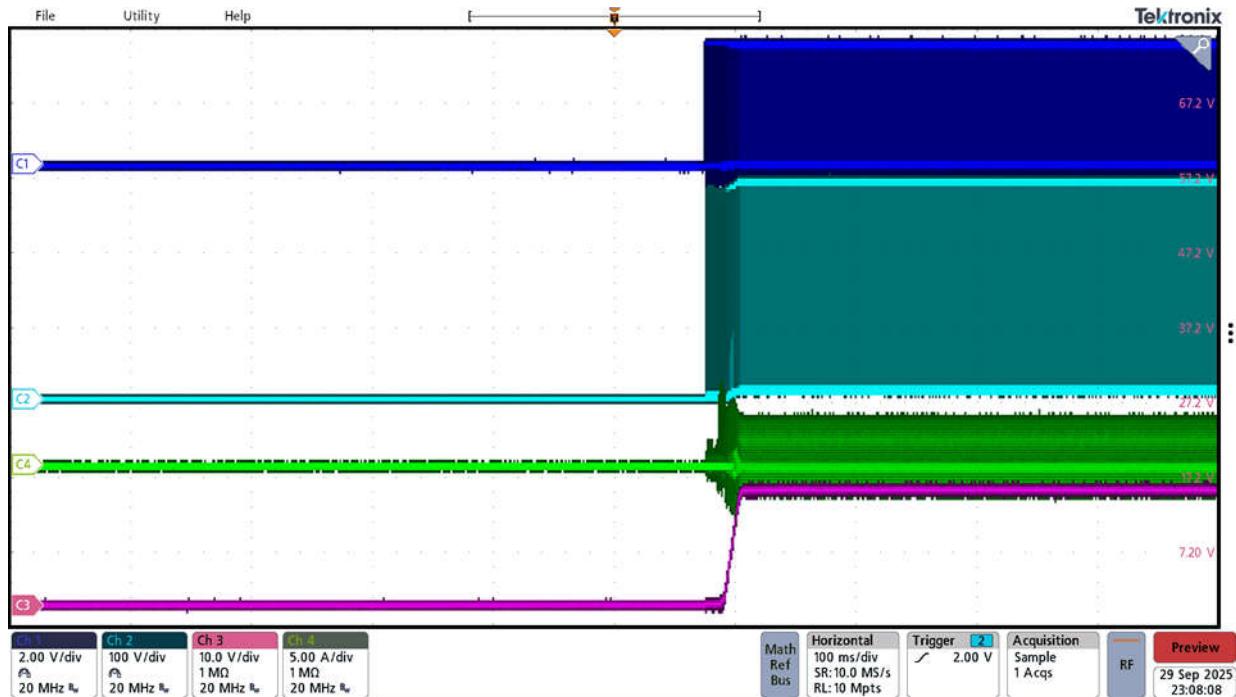


Figure 3-9. Soft-Start Operating Waveforms With 320V Input, 15V at 9A Constant Current Load

3.3 Undervoltage Protection

Undervoltage protection waveforms are shown in [Figure 3-10](#).

CH1 (Dark Blue): LS PWM

CH2 (Light Blue): Primary switching node voltage

CH3 (Green): Primary resonant current

CH4 (Red): Output voltage

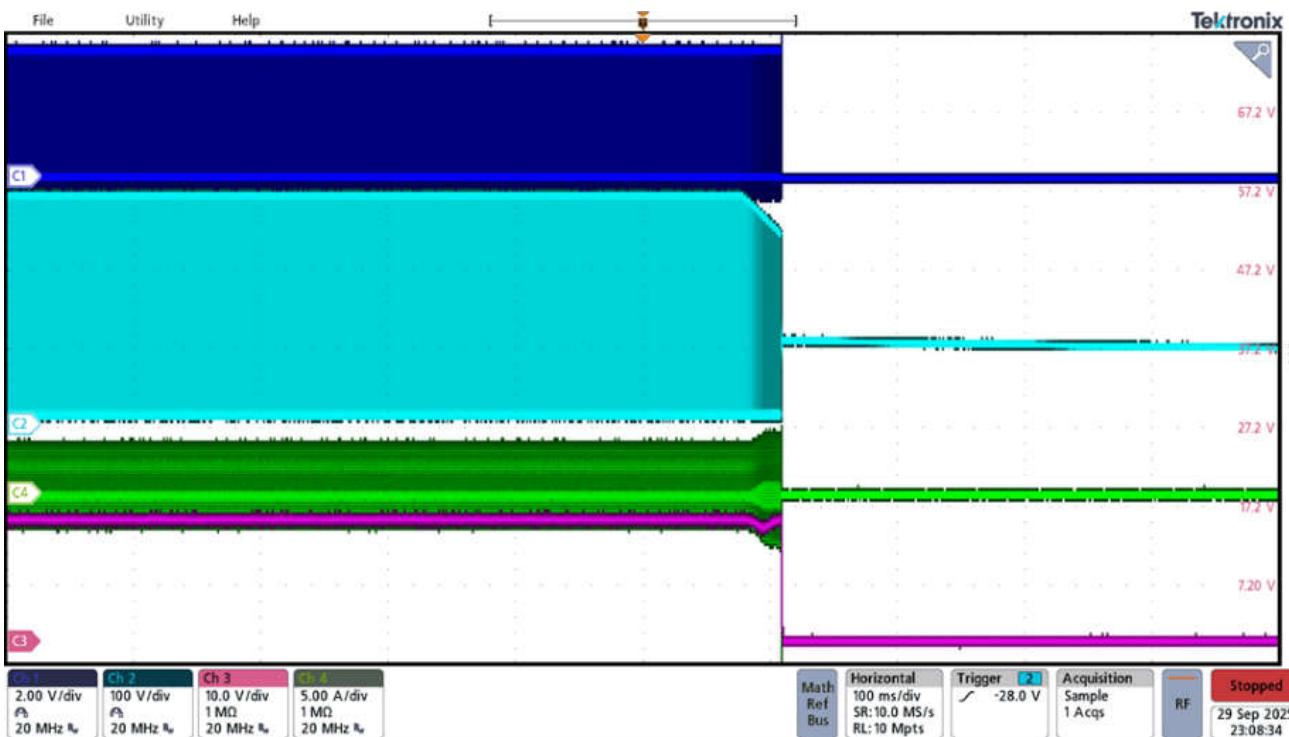


Figure 3-10. Undervoltage Protection Operating Waveforms With 320V Input, 15V at 9A Constant Current Load (Threshold: 300V)

3.4 Wide Range Adjustable Output Voltage Capability

Wide range adjustable output voltage capability behavior waveforms are shown in Figure 3-11.

CH1 (Dark Blue): Output voltage

CH3 (Red): Primary switching node voltage

CH4 (Green): Primary resonant current

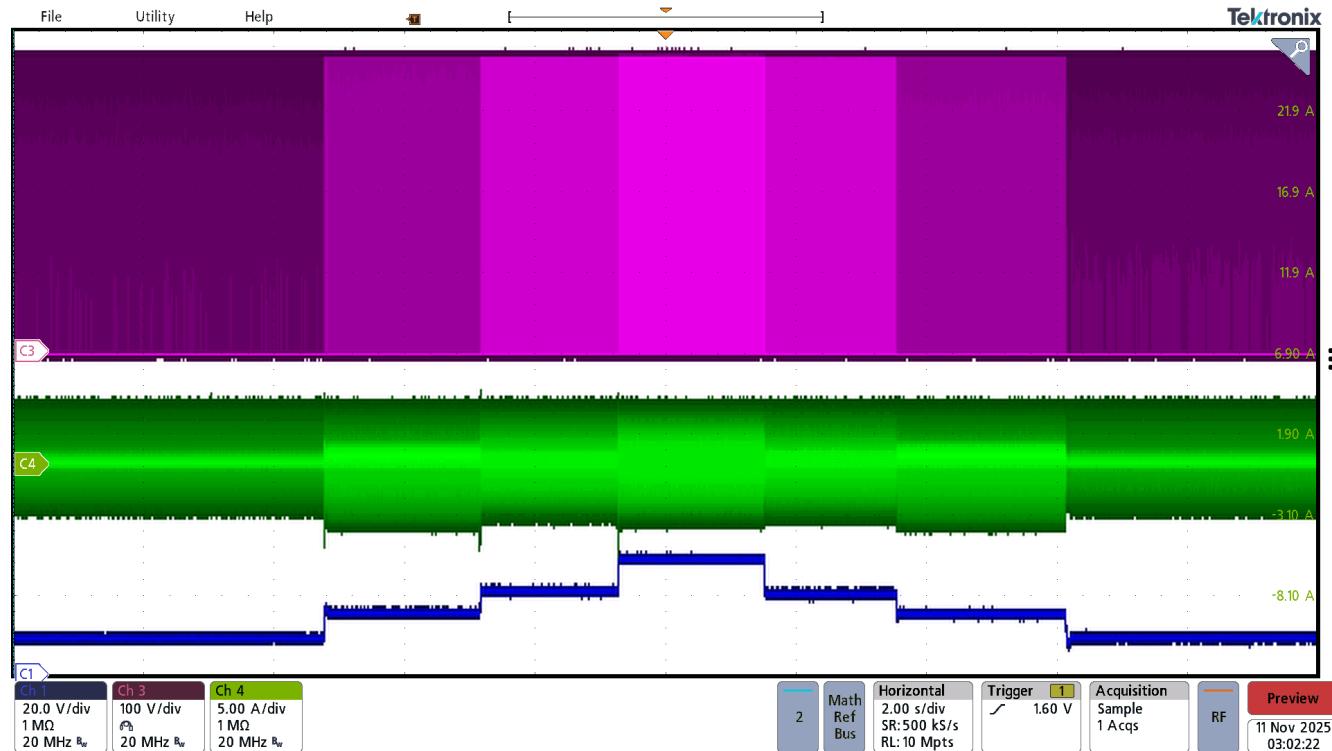


Figure 3-11. Output Voltage Adjusting 9V->15V->20V->28V->20V->15V->9V with 370V Input 9A Constant Current Load

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