Application Note

TPS6594/LP8764 PMIC Application Guide (III)

Lijia Zhu

ABSTRACT

This document was translated from a simplified Chinese source. (ZHCAFE8)

With the rapid development of new energy vehicles, the automotive industry is shifting from electrification to intelligence. Advanced driver assistance systems (ADAS) are being quickly deployed by major OEMs and Tier 1 suppliers. As a result, the TDA4 is being widely used across various terminal applications such as ADAS domain controllers, body domain controllers, and LiDAR. TI's new-generation PMIC family, represented by the TPS6594 and LP8764, is not only an ideal power solution for the TDA4 SOC but also a good choice for other SOCs. The TPS6594 and LP8764 offer high integration, high scalability, and support for high-level functional safety. With numerous and complex features, they are challenging to implement. This series of articles will cover topics about the TPS6594 and LP8764 PMICs, such as key mechanisms, system design considerations, common issue-locating strategies, and custom PMIC firmware (NVM). This is the third article in this series, which discusses considerations in the PMIC system design process.

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1 Introduction

The TPS6594 and LP8764 families are TI's next-generation PMICs, offering high integration, scalability, and functional safety. The LP8764 chip shares a similar architecture with the TPS6594 and is often used in systems as a secondary PMIC for the TPS6594. In terms of functional safety, the TPS6594 and LP8764 are developed to satisfy ISO26262 requirements during the design phase and incorporate a number of functional safety detection mechanisms to support ASIL D functional safety. Due to the complexity of PMICs, many issues can be encountered during application, which may lead to improper system operation if not addressed early in the design phase. This article describes several issues to be aware of early in the design phase.

2 List of Design Considerations

2.1 BUCK Output Capacitor and Inductor Selection

The parameters for loop stability vary under different conditions of input voltage, output voltage, switching frequency, and number of phases. The TPS6594 and LP8764 both integrate BUCK loop-compensation circuitry, so the BUCK output inductors and capacitors must be selected within the ranges recommended in the datasheets based on the operating scenario. There are 7 operating scenarios described in each of the TPS6594 and LP8764 datasheets, each of which corresponds to a range for the capacitor and inductor values.

TPS6594 BUCK operating scenarios:

1. 4.4MHz VOUT Less than 1.9V, Multiphase or High COUT Single Phase
2. DDR VTT Termination, 2.2MHz Single Phase Only
3. 4.4MHz VOUT Less than 1.9V, Low COUT, Single Phase Only
4. 4.4MHz VOUT Greater than 1.7V, Single Phase Only
5. 2.2MHz Full VOUT Range and VIN Greater than 4.5V, Single Phase Only
6. 2.2MHz VOUT Less than 1.9V Multiphase or Single Phase
7. 2.2MHz Full VOUT and Full VIN Range, Single Phase Only

LP8764 BUCK operating scenarios:

1. 4.4MHz Single-Phase and Multi-Phase Configuration
2. 2.2MHz Single-Phase Configuration for DDR Termination
3. 4.4MHz Single-Phase Configuration Low Output Voltage
4. 4.4MHz Single-Phase Configuration High Output Voltage
5. 2.2MHz Single-Phase Configuration with 5.0V VIN
6. 2.2MHz Single-Phase and Multi-Phase Configuration
7. 2.2MHz Single-Phase Generic Configuration

Upon closer examination, it is observed that scenarios may overlap. As shown in Figure 2-1, the scenarios "4.4MHz Single-Phase Configuration Low Output Voltage" and "4.4MHz Single-Phase and Multi-Phase Configuration" for the LP8764 both satisfy the system requirements of 5V input and 1.8V output. The device parameters can be selected by referring to either scenario, depending on the actual situation.

Electrical Characteristics - 4.4MHz Single-Phase Configuration Low Output Voltage							
3.45	V_{PVIN_Bx}	Input voltage range		3.0	3.3	5.5	V
3.46	V_{VOUT_Bx}	Output voltage programmable range		0.3		1.9	V
3.47	C_{IN_Bx}	Input filtering capacitance(1) (2)		3	22		µF
3.48a	$C_{OUT-Local(Buckx)}$	Output capacitance, local(2)		10	22		µF
3.48b	$C_{OUT-TOTAL\_Bx}$	Output capacitance, total (local and POL)(2)		25		100	µF
3.49a	L_{Bx}	Power inductor	Inductance	154	220	286	nH
3.49b			DCR		10		mΩ

Electrical Characteristics - 4.4MHz Single-Phase and Multi-Phase Configuration							
3.23	V_{PVIN_Bx}	Input voltage range		3.0	3.3	5.5	V
3.24	V_{VOUT_Bx}	Output voltage programmable range		0.3		1.9	V
3.25	C_{IN_Bx}	Input filtering capacitance(1) (2)		3	22		µF
3.26a	$C_{OUT-Local(Buckx)}$	Output capacitance, local(2)	Per phase	10	22		µF
3.27b	$C_{OUT-TOTAL\_Bx}$	Output capacitance, total (local and POL)(2)	Per phase	50		250	µF
3.28a	L_{Bx}	Power inductor	Inductance	154	220	286	nH
3.28b			DCR		10		mΩ

Figure 2-1. LP8764 BUCK Input/Output Capacitor and Inductor Requirements for Specific Scenarios

Figure 2-2 shows the capacitor variants recommended in the datasheet, all with an ESR of approximately 10mΩ at the switching frequency. One of these typical variants is selected to present its ESR curve. In practical applications, it is impossible to select components strictly according to the datasheet recommendations. As shown in Figure 2-1, the datasheet tables do not limit the parasitic parameters, such as capacitor ESR. In practice, it has been found that when multiple capacitors are used in parallel or capacitors with lower ESR are used, especially when the capacitance is at the boundary (minimum value), special attention must be paid to the potential risk of instability due to the ESR.

The simulations shown in Figure 2-3 and Figure 2-4 are examples of this for the LP8764 device. Considering the current requirements for a small system footprint and light load dynamics, the scenario "4.4MHz Single-Phase Configuration Low Output Voltage," which uses lower output capacitance, was selected as a reference for choosing the capacitors and inductors. Smaller output capacitors do not affect loop stability; they only partially sacrifice the transient response performance, which is acceptable for the current application. By selecting two capacitors with different ESR values but the same capacitance to simulate the scenarios of multiple small capacitors in parallel versus a single large capacitor, the loop simulation shows that with an output capacitor of 10mΩ ESR, the loop is stable even at the minimum capacitance specified in Figure 1 (25uF total). However, with a capacitor of 2mΩ ESR, the loop is unstable.

TI provides SIMPLIS models for devices. It is recommended to simulate the loop by incorporating the model for the selected device during the early design phase.

MANUFACTURER	PART NUMBER	VALUE	CASE SIZE	DIMENSIONS L × W × H (mm)	VOLTAGE RATING
Murata	GCM32EC71A476KE02	47 µF (10%)	1210		10 V
TDK	CGA6P1X7S1A476M250AC	47 µF (20%)	1210		10 V
Murata	GCM32ER70J476ME19	47 µF (20%)	1210	3.2 × 2.5 × 2.5	6.3 V
TDK	CGA6P1X7S0J476M250AC	47 µF (20%)	1210		6.3 V
TDK	CGA5L1X7T0G476M	47 µF (20%)	1206		4 V
Murata	GCM31CR71A226KE02	22 µF (10%)	1206	3.2 × 1.6 × 1.6	10 V
TDK	CGA5L1X7S1A226M160AC	22 µF (20%)	1206		10 V
Murata	GCM21BD70J226ME36	22 µF (20%)	0805	2.0 × 1.25 × 1.25	6.3 V
TDK	CGA4J1X7T0J226M	22 µF (20%)	0805		6.3 V
Murata	NFM18HC106D0G (3-T)	10 µF (20%)	0603	1.6 × 0.8 × 1.25	4 V

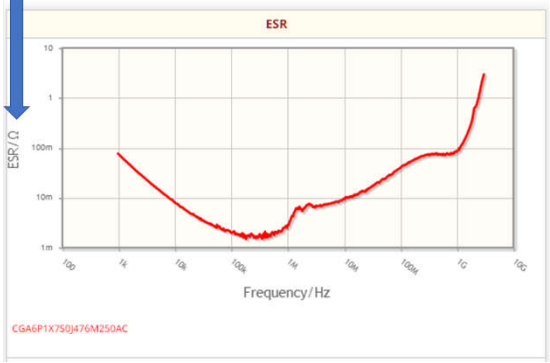

Figure 2-2. Recommended BUCK Output Capacitor Variants in LP8764 Datasheet

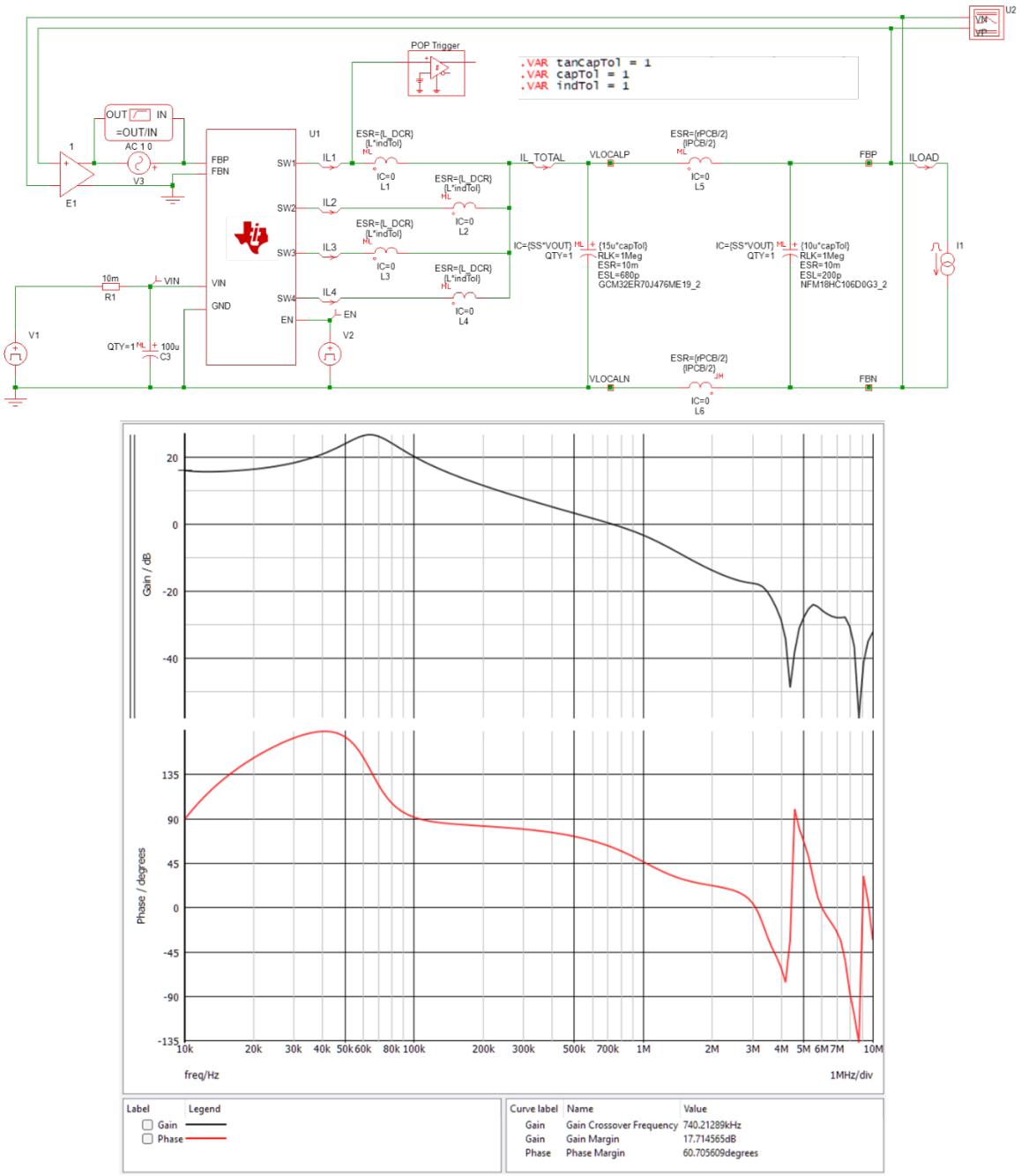

Figure 2-3. LP8764 Loop Simulation 1

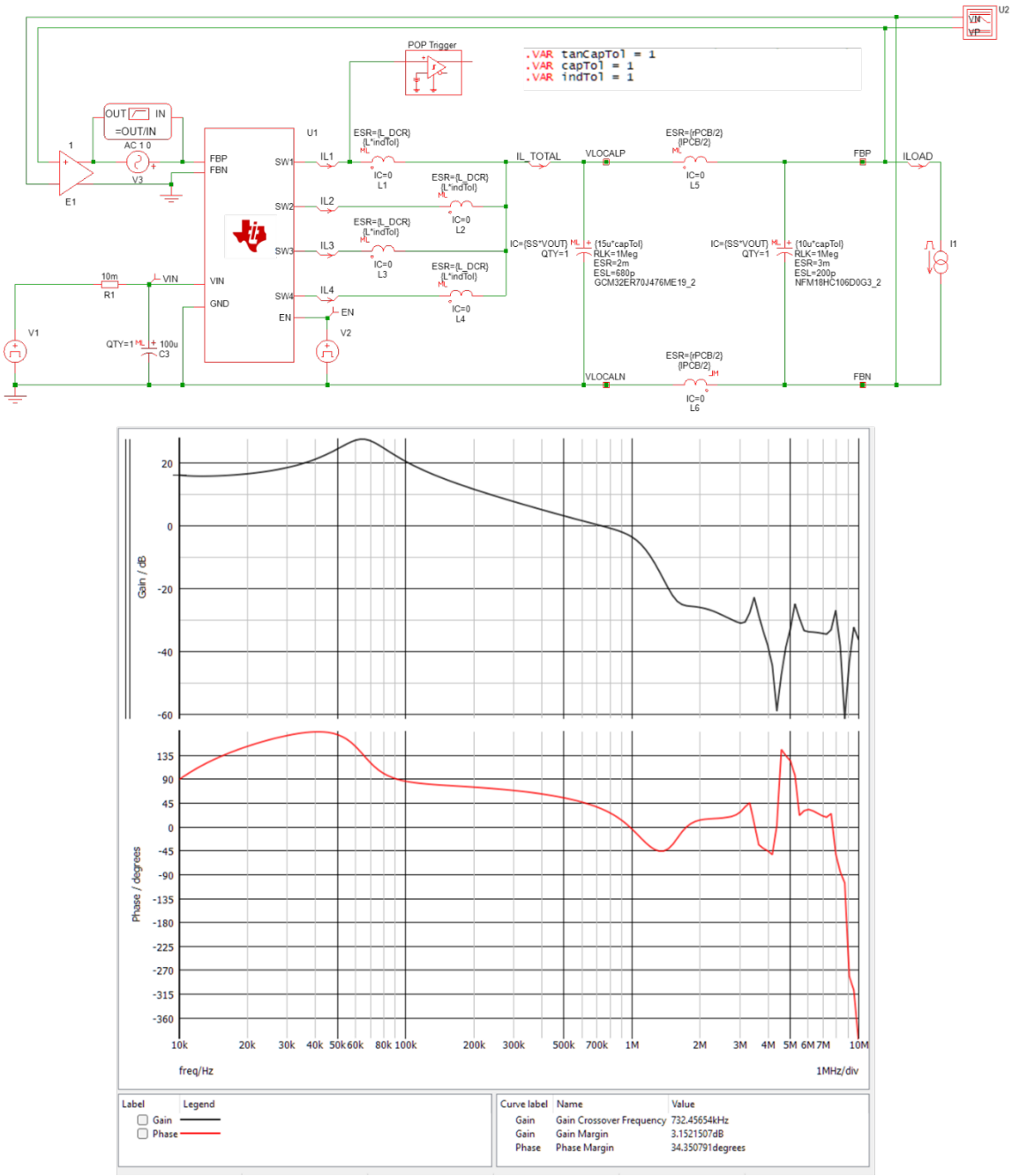

Figure 2-4. LP8764 Loop Simulation 2

2.2 Reverse Leakage Path Suppression

The PMIC has an output residual voltage detection mechanism. Residual voltages on any rail during the startup stage will block the normal startup of the device. These residual voltages are typically caused by reverse leakage due to improper design. Similarly, the NMOS's Fail Short BIST mechanism is also affected by leakage. Therefore, special attention must be paid to block potential reverse leakage paths during the system design.

The top figure of Figure 2-5 shows a typical example of reverse leakage using PDN 1A. In the early design phase, reverse leakage avoidance was not considered, and the CAN IO supply was provided by a 3.3V primary power supply output. During system startup, the CAN starts before the PMIC, and the CAN bus is in the recessive state. At this point, RXD outputs a high level, which leaks onto the VDD IO rail through the ESD diodes inside the TDA4. This leakage then passes through the parasitic body diode of the load switch and couples

onto the VCCA rail, causing VCCA to rise abnormally. As a result, the Fail Short BIST mechanism fails, and the system cannot boot.

The correct design is shown in the bottom figure of Figure 2-5, where the power supply (or IO power supply) sequence of all peripheral chips connected to the TDA4 must be controlled by the PMIC. If system requirements or peripheral device constraints make this impossible, an isolation device, such as the SN74LVC4T245, must be placed between the peripheral device and the TDA4 IO port. This isolation device has a separate OE pin. By adding an external pull-down resistor on the board to ensure that the OE pin is low during power-up, and using software to drive the OE pin high after the TDA4 is powered up, leakage isolation can be achieved.

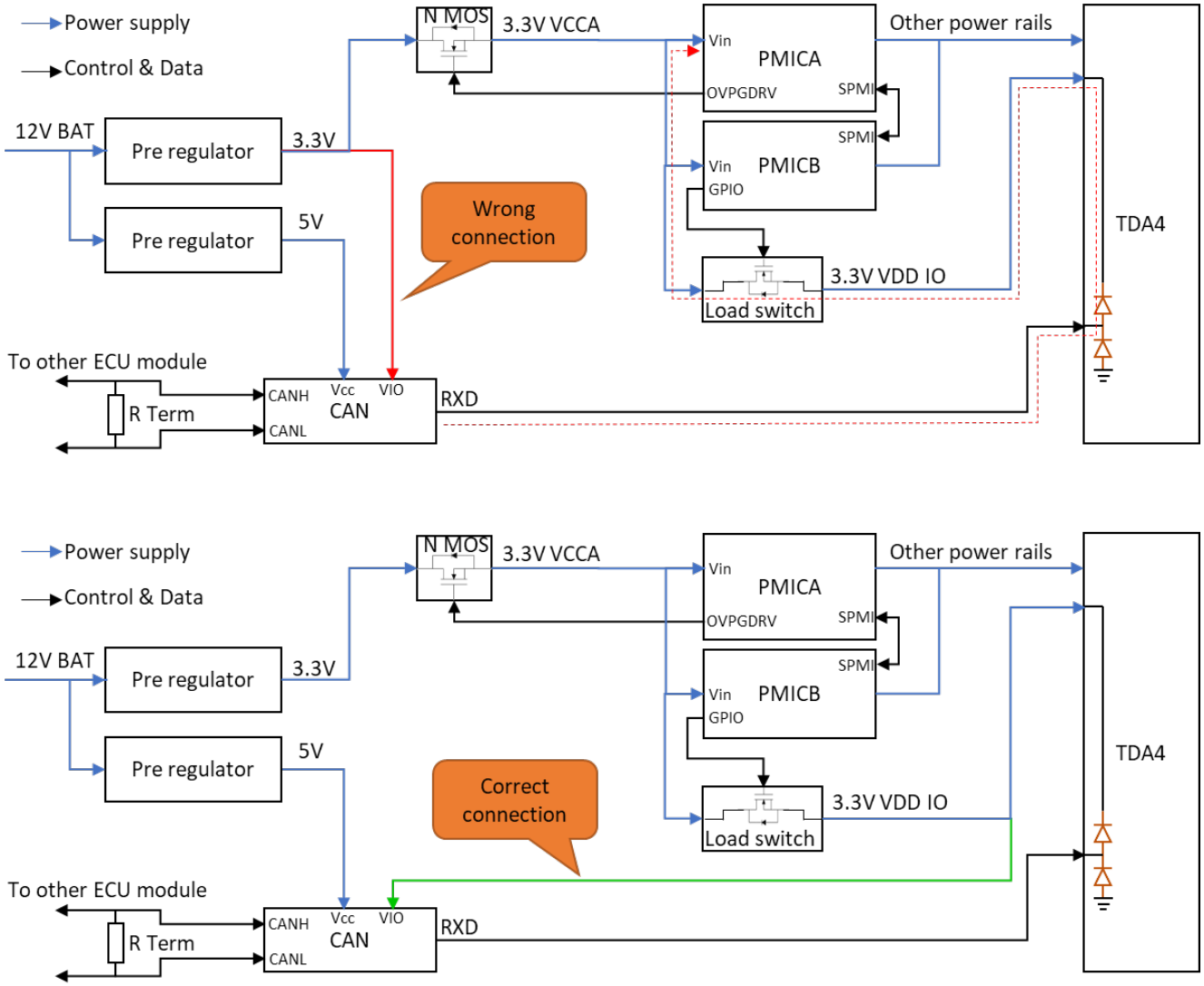

Figure 2-5. Example Design Causing Reverse Leakage

2.3 Primary BUCK Selection

Figure 2-6 shows a common system block diagram and module input voltage (PWR12V0) waveform during a ramp-up test. PWR12V0 is connected to the enable pin of the primary BUCK after a resistor divider. It ramps up with a very slow slope in the ramp-up test, typically taking tens of minutes to rise from 0V to 12V. A ramp-up test generally requires the system to resume normal operation after the supply voltage returns to normal.

However, the system repeatedly restarts near the turn-on point, and VCCA repeatedly drops below UV, causing the recovery counter to reach the upper limit and lock up in a safe recovery state. The PMIC must be power-cycled to exit this state. The system fails the ramp-up test.

Figure 2-7 shows the waveform and mechanism analysis for repeated undervoltage restart near this turn-on point:

1. At T0, PWR12V0 exceeds the UVLO rise threshold of the primary BUCK, and the primary BUCK outputs PWR3V3. At this point, the PMIC is enabled low; because only the PMIC itself draws current, PWR12V0 is pulled down slightly but not below the UVLO fall threshold (there is a 200mV hysteresis between the UVLO rise and fall thresholds, fixed by hardware).
2. By T1, PG of the primary BUCK is pulled high, the EN pin of the PMIC is pulled up, and the PMIC starts to power up the SOC in the power-up sequence.
3. Depending on the power-up sequence of the PMIC, at T2, the Core supply of the SOC is powered up (indicated as PMIC out in the diagram). At this point, the SOC draws a huge current, pulling down PWR3V3, which in turn causes PWR12V0 to drop below the UVLO fall threshold of the primary BUCK, causing the system to shut down.
4. Having detected a drop in VCCA, the PMIC enters the SAFE RECOVERY state and shuts down all outputs. At this point, the current required by the system decreases, allowing PWR12V0 to go back to the turn-on point. After a time delay (determined by the primary BUCK mechanism), the primary BUCK restarts at T3.

   At T4, the active discharge function of the PMIC itself and the PMIC output BUCK draws current (for the behavior of the blue line, see also the analysis in section 2.5 of this article), causing PWR12V0 to drop below the UVLO fall threshold. At T5, the active discharge is complete. Because only the PMIC itself draws current at this point, PWR12V0 remains above the UVLO fall threshold.

   The process from T2 to T5 involves the protection mechanism of the upstream power supply (which varies depending on power supply characteristics) and the discharge mechanism of the PMIC. These two mechanisms are coupled with each other to generate the observed waveform. They can be regarded as a single black box. In other words, consider the condition where PWR12V0 is pulled low because the load draws current at T2, leading to a system shutdown, and then recovers to a stable level at T5, causing the system to restart once, as a single event.
5. After T5, the system returns to the first step and repeats this loop. Every time it goes through a loop, the RECOVERY COUNTER increments by 1. After reaching 15, the PMIC stops in the SAFE RECOVERY state and shuts down all outputs, preventing the system from starting.

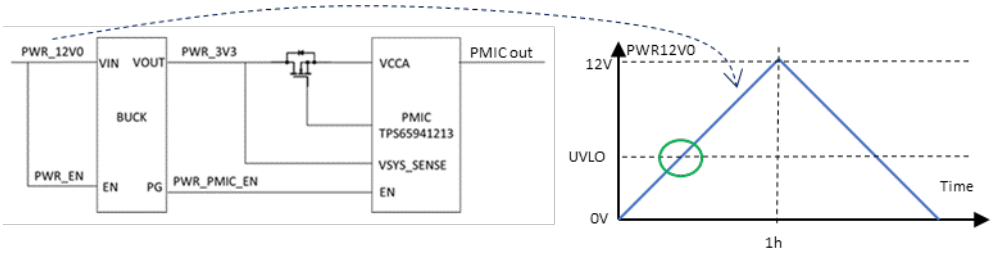

Figure 2-6. System Design and Ramp-up Test

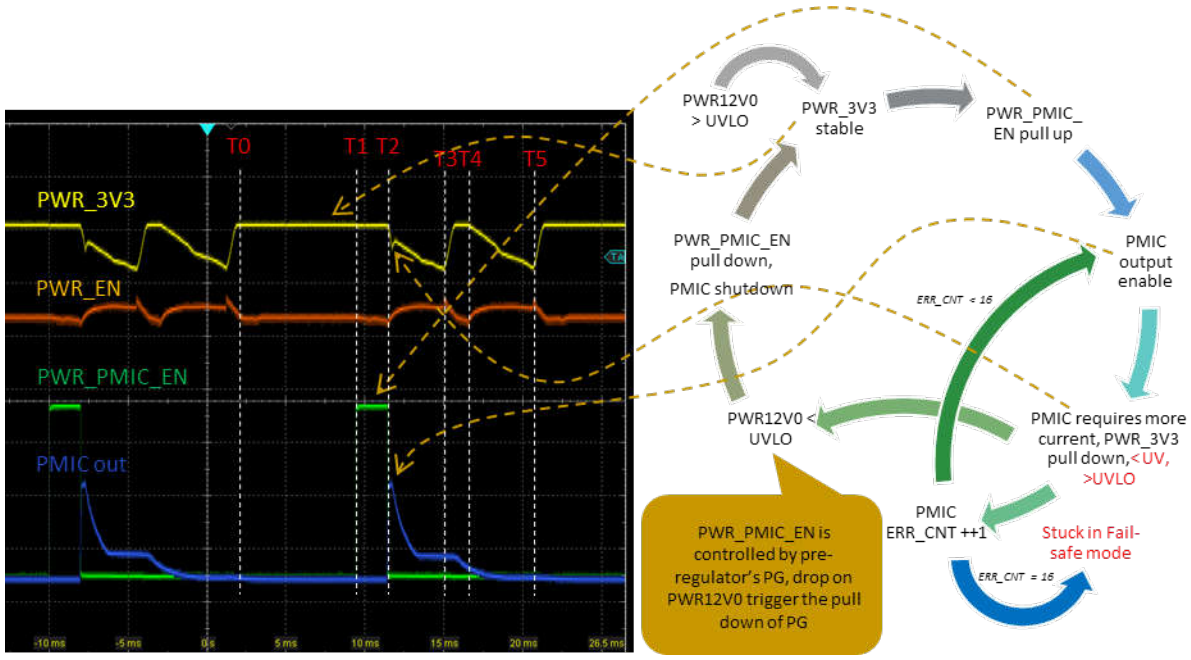

Figure 2-7. Cause Analysis for Repeated System Restart During Ramp-up Test

To avoid the loop described earlier, it is recommended to select a primary BUCK with enable hysteresis and set the hysteresis threshold appropriately. As shown in Figure 2-8, near the turn-on point, if the thresholds include sufficient hysteresis, when the PMIC turn-on causes PWR12V0 to drop, the voltage remains above the turn-off point of the primary BUCK, and the primary BUCK continues to output, thereby avoiding the under-voltage power-cycling described earlier.

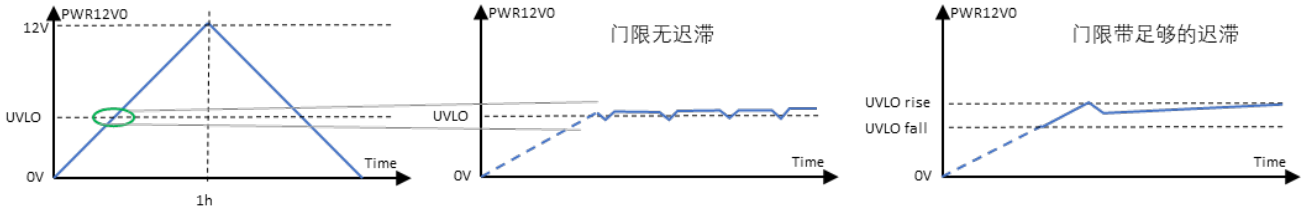

Figure 2-8. Diagram of Enable Hysteresis Near Turn-on Point

Based on the simplified system diagram shown in Figure 2-9, when the load draws current, the high-side MOSFET of the BUCK turns on at the maximum duty cycle the chip supports, and the low-side MOSFET conducts for a very short duration. Therefore, the analysis can be simplified to consider only the high-side MOSFET and input/output capacitors and inductors. The load is abstracted as RL, and Zin represents the parasitic impedance from the power supply to the input of the primary BUCK. At T0, the system is in steady state, with Vin' and Vin both equal to the voltage at the turn-on point. Vout is the set voltage, such as 3.3V, with no current drawn by RL.

This circuit is a fourth-order LC circuit. Calculating its time-domain transient characteristics requires solving a fourth-order differential equation, which is very complex. Instead, the energy conservation approach can be used to qualitatively analyze the effects of various parameters on the Vin voltage drop.

For capacitors and inductors, the energy they store is given by:

$$W_C = \frac{1}{2}CU^2 \quad (1)$$

$$W_L = \frac{1}{2}LI^2 \quad (2)$$

1. At the instant the PMIC's enable pin is pulled up, output capacitor C1 supplies current to the i1 load through the green current path. The heavier the load R_L, the faster the output voltage drops. The larger the C1 value, the more energy is stored, and the slower Vout drops (the smaller the drop per unit time).
2. After the C1 voltage decreases, the primary BUCK's FB pin detects a voltage drop, turning on the high-side MOSFET. Current flows from C2 through the inductor along the orange path i2 to charge C1. The larger the C2 and L values are, the more energy is stored, and the less the C2 voltage (V_{in}) drops. When the high-side MOSFET is turned on, the higher the Vout, the less energy C2 and L must supply to C1. In other words, a larger C1 indirectly leads to a smaller drop in Vin. At the same time, the higher the C1 voltage at T0, the more initial energy, and the smaller the Vin drop.
3. The smaller the parasitic impedance between the supply and the input of the primary BUCK, the faster the C2 voltage recovers, and the smaller the V_{in} drop.

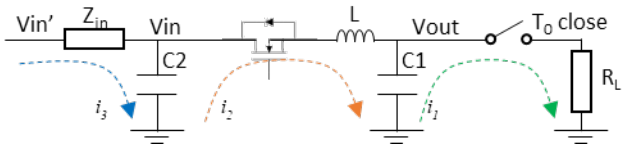

Figure 2-9. Simplified Load Current-Drawing Diagram

The above analysis reveals that the drop in voltage is related to three sets of parameters:

1. Load characteristics, including the maximum current required by the load and the power-up slope of the PMIC. Once the system design is finalized, the load chip is fixed, and the power-up slope of the PMIC is fixed by NVM. Therefore, these parameters are fixed by design.
2. Input/output capacitors of the primary BUCK, output inductor, and parasitic parameters from the power supply to the input of the primary BUCK. In practical applications, the capacitor and inductor values must be selected based on a combination of ripple, inductor saturation current, heat dissipation, and so forth. Also, the parasitic parameters can be minimized during design. Therefore, there is little room for adjusting these parameters.
3. UVLO rise threshold. The lower the UVLO rise threshold, the larger the voltage drop. The typical turn-on voltage for automotive modules ranges from 6V to 9V. A lower UVLO rise threshold is meaningless, while a higher one narrows the module's operating voltage range.

The lower the UVLO rise threshold of the primary BUCK, the higher the hysteresis is required. Generally speaking, the UVLO rise threshold and hysteresis are adjusted using two external resistors, but it is not a good idea to repeatedly adjust these resistors by soldering. A better approach is to use a UVLO rise threshold equivalent to the supply voltage. The specific procedure is as follows:

1. Set the UVLO rise threshold of the primary PMIC to the lowest voltage the chip supports (by modifying the external resistors), or below the expected minimum UVLO rise threshold.
2. The supply voltage to the system is set to the expected minimum turn-on voltage, such as 6V, to power up the system quickly. This action is equivalent to powering up the system after the supply voltage slowly ramps up to the UVLO rise threshold.
3. The oscilloscope detects and records the voltage drop at the input of the primary BUCK. Some headroom can be added to this voltage as the set value for hysteresis.
4. If the turn-off voltage is found to be too low, increase the UVLO rise threshold appropriately, and the hysteresis will be reduced synchronously. Then repeat the above steps.

2.4 Output Inductor Value Selection for Primary BUCK

VCCA overshoot might occur when the system is powered down (by cutting off the entire board power). Figure 2-10 shows the scenario where VCCA overshoots above OV when the system is powered down, and Figure 2-11 shows a worse case where VCCA overshoots to the VCCA OVP threshold, triggering OVPDRV to pull low. This excessively high voltage affects the long-term reliability of the system.

The cause of this issue is analyzed as shown in Figure 2-12. After a normal power-down, the primary BUCK continues to operate for a period of time due to the input capacitor, with the output voltage decreasing

continuously. When the input voltage drops below the primary BUCK's turn-off point, its SW stops switching and enters a Hi-Z state, after which VCCA slowly falls due to the energy stored in the preceding inductor and output capacitor. The inductor current continues to flow to the PMIC. When VCCA drops to the PMIC's UV threshold, the orderly power-down logic of the PMIC is triggered. In this case, the current required by the PMIC drops suddenly, but the current in the preceding inductor cannot change abruptly. Therefore, the current surges into the output capacitor, causing VCCA overshoot.

The magnitude of the VCCA overshoot is related to the primary BUCK inductor value. A larger inductor value results in a higher VCCA overshoot, which can directly damage the PMIC in severe cases. Therefore, it is important during design to ensure that the output inductor value of the primary BUCK is not too large. This value can be determined by simulating the load transient characteristics. If a larger inductor value has already been used, it is possible to mitigate the issue after power-up by using I2C to decrease the PMIC BUCK's power-up and power-down slopes (BUCKx_CONFIG register bits 0-2) as a software workaround.

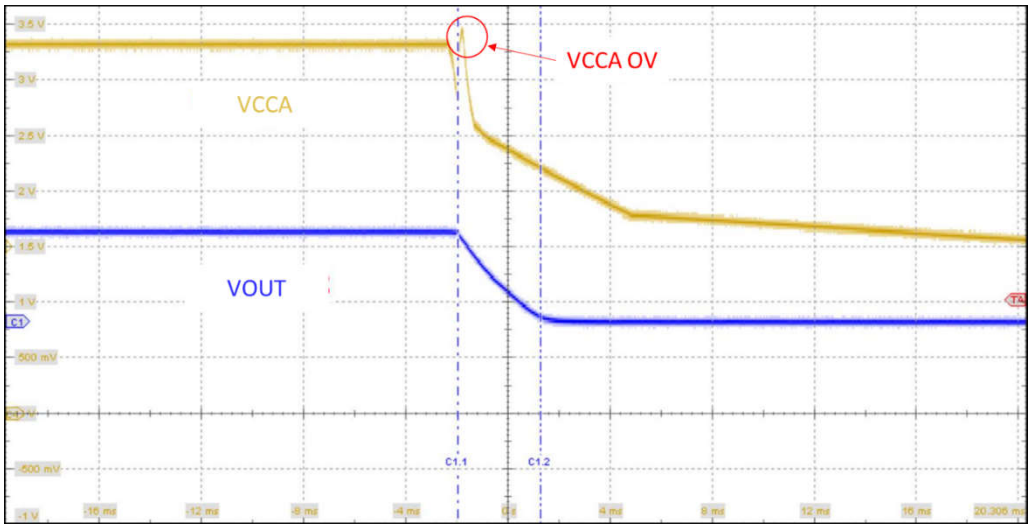

Figure 2-10. VCCA OV Waveform at Shutdown

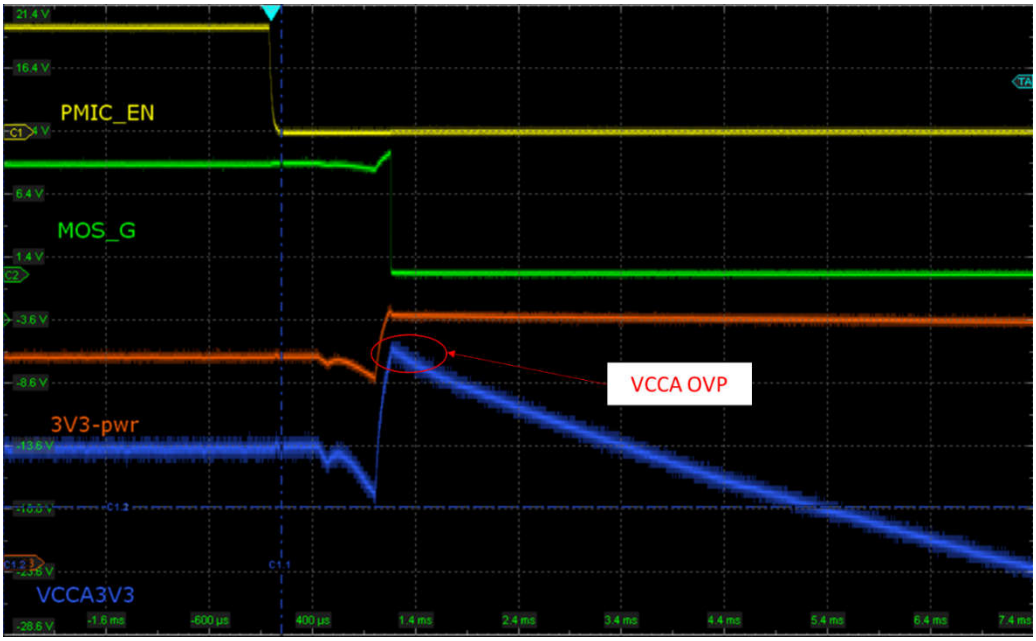

Figure 2-11. VCCA OVP Waveform at Shutdown

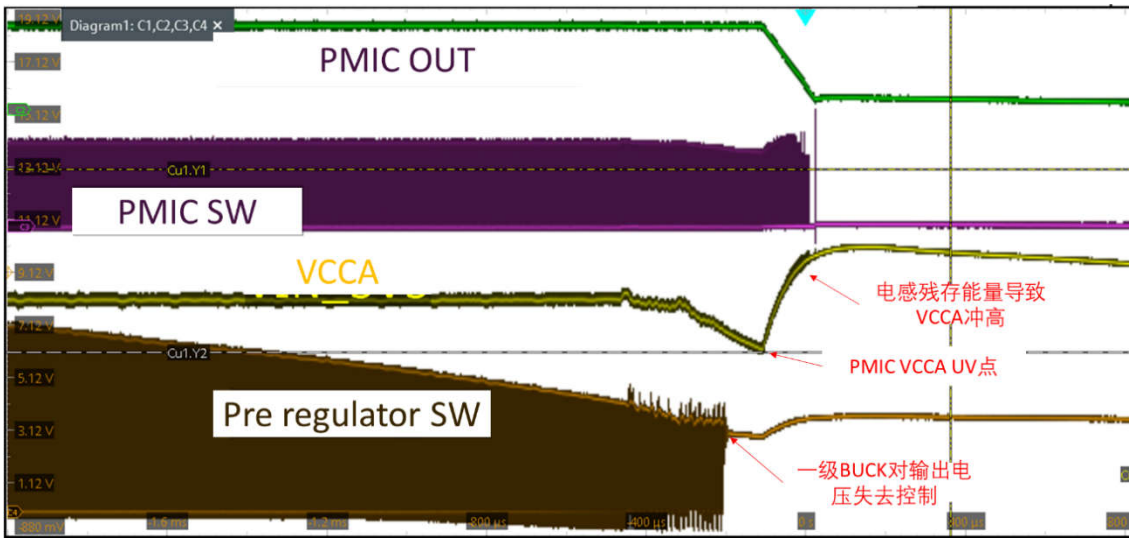

Figure 2-12. System Node Waveforms at VCCA Overshoot

2.5 Application Considerations for Fusa MCU with PMIC

Some designs use a standalone Fusa MCU working in coordination with a PMIC + SOC system. In such designs, scenarios arise where the MCU controls the power-up and power-down of the SOC system (including the PMIC). Figure 2-13 shows an architecture common to such a design. The MCU controls the enable pin of the primary supply of the PMIC. When the MCU detects a fault in the SOC system, a common recovery approach is to pull down the enable pin of the primary BUCK to restart the SOC system.

However, the MCU must reserve enough time for the SOC system to restart. The PMIC has a residual voltage detection mechanism; even if the enable pin has been pulled high, the PMIC will not start until the residual voltage is fully discharged. If the MCU logic is to retry the restart when the PMIC output is not available within a short period of time, the system will be trapped in an endless loop and always fail to start. The wait time for the MCU must be reserved based on the time spent on residual voltage discharge, which can be measured and provided to software after the hardware design is complete. Figure 2-14 shows the waveforms of the MCU restarting the SOC system. The first restart failed because the MCU did not wait long enough before attempting to restart the SOC system again. On the second attempt, it waited long enough, and the system started normally. The PMIC's residual voltage discharge mechanism is marked in Figure 2-14, and it features both Active and Passive discharge logic.

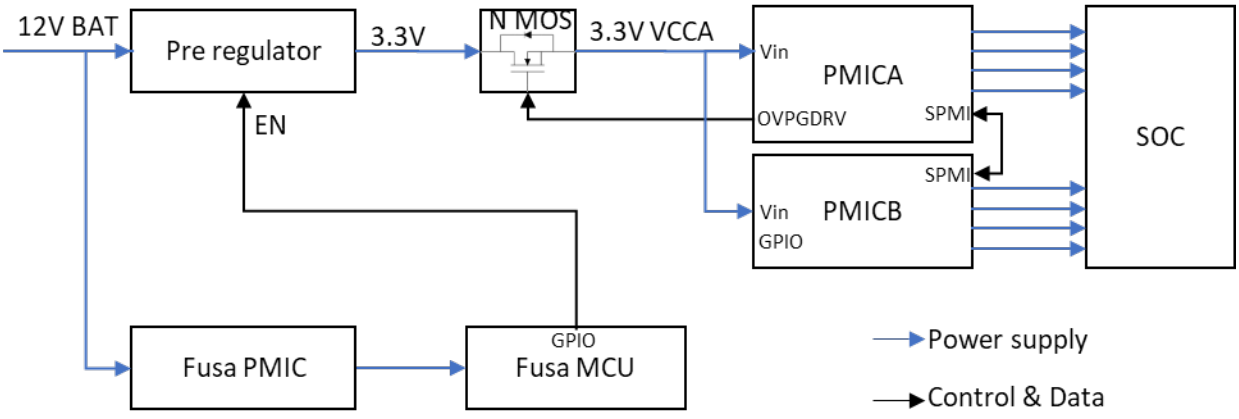

Figure 2-13. MCU + SOC System Architecture

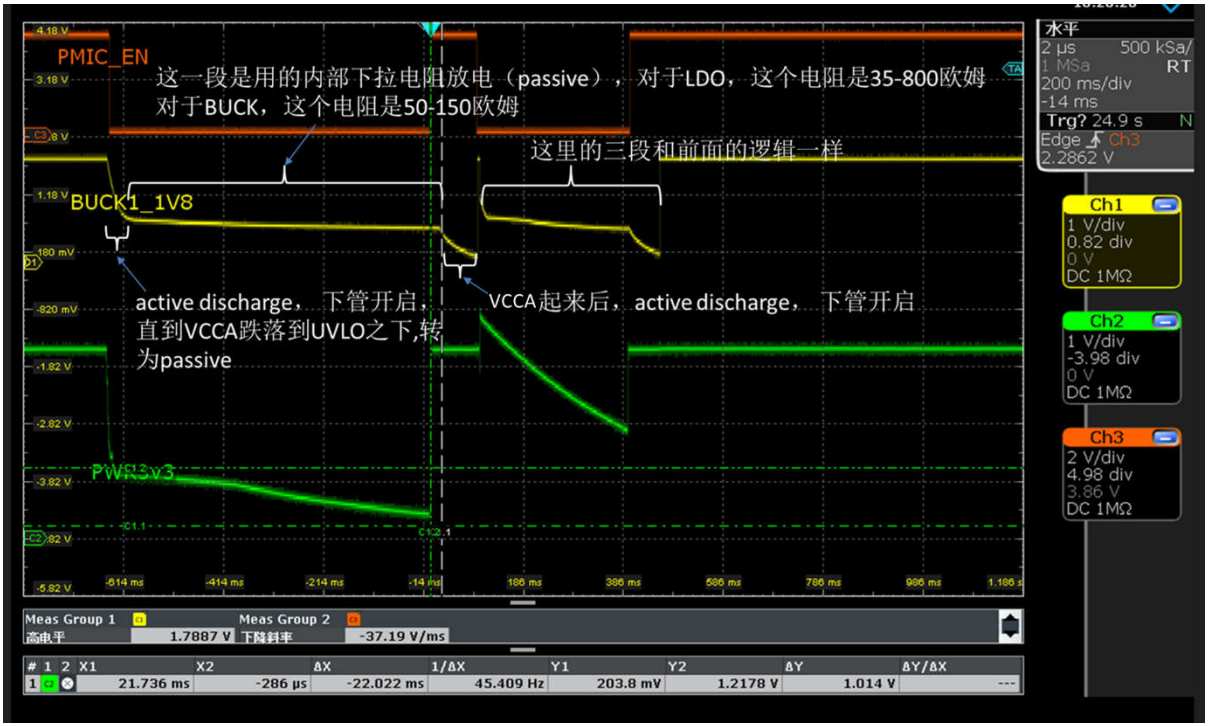

Figure 2-14. PMIC Rail Waveforms for MCU Restarting SOC System

2.6 Application Considerations for LP8764 VMON Input

As shown in Figure 2-15, the LP8764 has an additional VMON module that monitors voltage signals from GPIO7/8. These signals are typically critical discrete power rails on the system, and the PMIC monitors these voltages to deliver higher-level functional safety. However, the maximum monitoring voltage supported by GPIO7/8 does not exceed 5V. To monitor external rails greater than 5V, an additional resistor divider network is required. Considering the system power consumption, the divider resistors cannot be too small. Generally, resistors in the 10kΩ range are chosen for voltage division. The system diagram is shown in Figure 2-16.

The input IO of the LP8764 features a fail-safe design. This special design requires sufficient current to flow into the chip to turn on the internal PN junction. In low-current scenarios, a stage appears at the level of the VINT + PN junction forward voltage (1.8V + 0.4V = 2.2V). The lower the input current, the longer the voltage remains at this stage.

This prolonged stage can cause VMON BIST to fail, resulting in system startup failure. There are several solutions:

1. During system-level design, select kΩ-level divider resistors. Based on the test results shown in Figure 2-17, this level of resistance generally does not result in a stage.
2. Adjust the resistor dividers to make sure that the voltage divided down and fed into the PMIC is lower than 2.2V.
3. Adjust the VMON on time in the power-up sequence in NVM to add a longer delay, which is generally applicable for custom NVM scenarios.

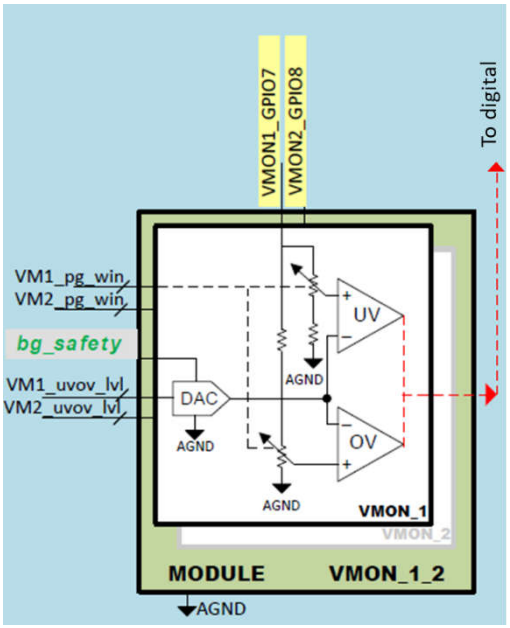

Figure 2-15. LP8764 VMON Module

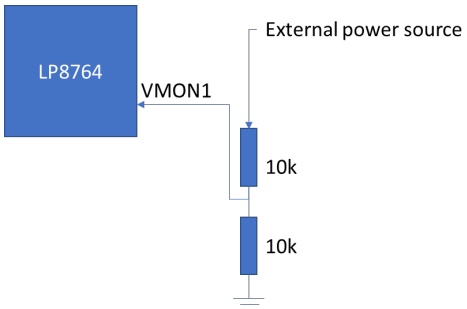

Figure 2-16. LP8764 VMON External Resistor Divider Application Diagram

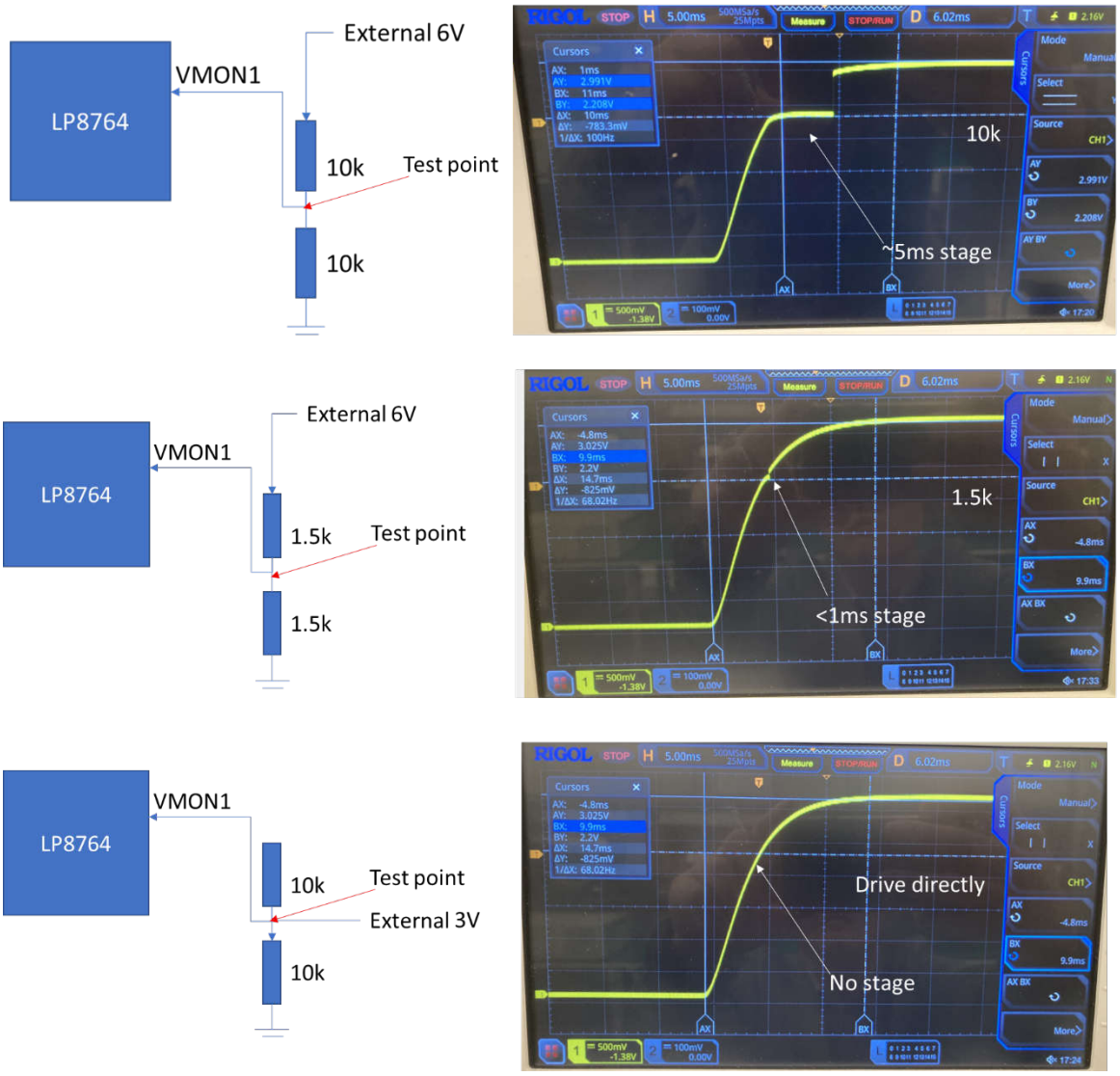

Figure 2-17. LP8764 VMON Input Waveforms With Different Drive Currents

3 References

1. Datasheet "TPS6594-Q1 Power Management IC (PMIC) with 5 BUCKs and 4 LDOs for Safety-Relevant Automotive Applications"
2. Datasheet "LP8764-Q1 Four-Phase, 20-A Buck Converter With Integrated Switches"
3. User Guide "TPS65941213-Q1 and LP876411B4-Q1 PMIC User Guide for J721E, PDN-1A"
4. User Guide "TPS6594-Q1 Schematic PCB Checklist application note"

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