Application Note

TPS6594/LP8764 PMIC Application Guide (Part I)

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ABSTRACT

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With the rapid development of new energy vehicles, automobiles are transitioning from electrification to intelligence. As high-level assisted driving quickly lands across major OEMs and Tier 1 suppliers, TDA4 is being widely used in various terminal applications such as ADAS domain controllers, body domain controllers, and LiDAR. TI's new generation PMIC family, represented by TPS6594/LP8764, is not only the optimal power solution for TDA4 SOCs, but also an excellent choice for powering other models of SOCs. TPS6594/LP8764 features high integration, high scalability, and support for high-level functional safety. Because it has many functions and is relatively complex, there will be considerable difficulty in application. This series of articles will share insights from aspects such as the main internal mechanisms of the TPS6594/LP8764 PMIC chips, system design considerations, common problem troubleshooting ideas, and custom PMIC firmware (NVM). This article is the first in the series, introducing the main internal mechanisms of the PMIC chips.

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1 Introduction

The TPS6594/LP8764 series is TI's new generation of PMIC products, featuring high integration, high scalability, and high functional safety. As shown in the Figure 1-1, TPS6594 integrates 5 BUCK converters and 4 LDOs internally, possessing very high integration. At the same time, the first 4 routes among the 5 BUCK routes can be flexibly configured via firmware (NVM) into multiple output modes (4-phase parallel output, 3-phase parallel + 1 independent BUCK, 2-phase parallel + 2 independent BUCKs, two 2-phase parallel outputs, and four independent BUCK outputs). The LDOs can work either in LDO mode or in bypass mode. In bypass mode, the LDO is used merely as a high-side switch to control the power-up sequence without generating additional voltage drop. Meanwhile, TPS6594 possesses rich GPIOs, which can be configured through NVM for multiple functions, including external wake-up input, watchdog feed input, enable input, external voltage monitoring input, and enable control for external high-side switches/LDOs/BUCKs, further improving the scalability of the device. The LP8764 chip has a similar chip architecture to the TPS6594 chip, with the difference that it only contains 4 BUCK outputs (which can be flexibly configured into five output modes just like the 6594) and has no LDOs. Its architecture is shown in Figure 1-2.

TPS6594/LP8764 uses the SPMI interface for status synchronization between multiple PMICs. The state machines of multiple PMICs working in parallel can be regarded as a whole. In terms of functional safety, the TPS6594 was developed in accordance with the requirements of ISO26262 during the design phase. The device is designed with a large number of functional safety detection mechanisms, including watchdogs, overvoltage and undervoltage monitoring and protection for input power rails, overcurrent, overvoltage/undervoltage, and residual voltage monitoring and protection for output power rails, communication integrity protection, and register integrity protection mechanisms. On the hardware level, it satisfies over 99% single-point fault coverage and supports ASIL D level functional safety. LP8764 uses the same IP as TPS6594 and is often used as a secondary PMIC in cooperation with TPS6594 in the system.

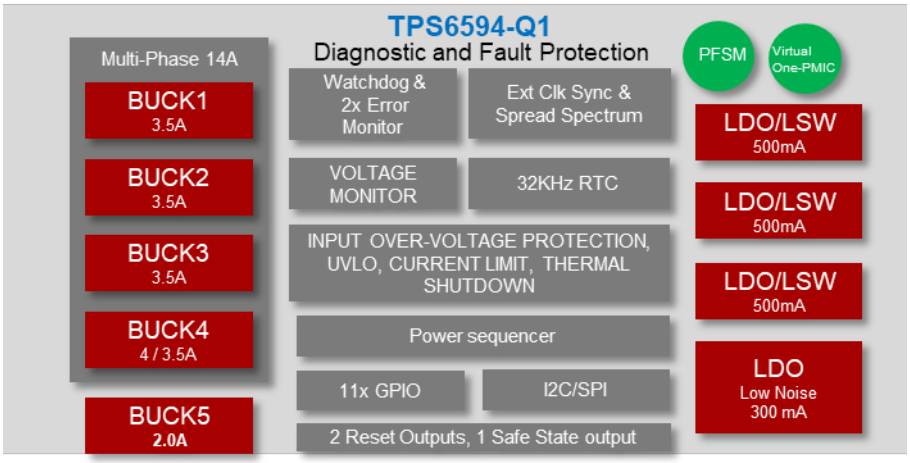

Figure 1-1. TPS6594 Structural Block Diagram

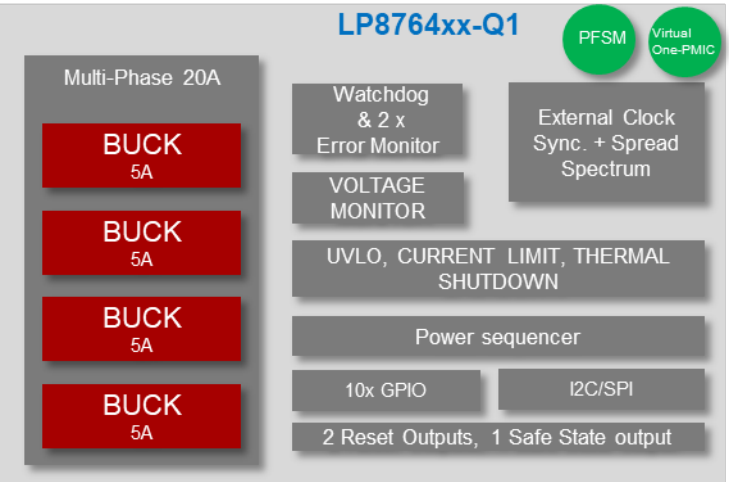

Figure 1-2. LP8764 Structural Block Diagram

TPS6594 and LP8764 currently each have a derivative model, TPS6593 and LP8769, and their differences are shown in Figure 1-3.

General Part Number	区别
TPS6594-Q1 TPS6593-Q1	TPS6593在TPS6594基础上裁剪了输入的OVP保护功能，仅支持小系统到ASIL B，系统级别仍支持ASIL D
LP8764-Q1 LP8769-Q1	LP8769在LP8764基础上提升了输出精度，考虑输出AC+DC精度和监控精度，体现在负载端LP8764可以做到 +/- 5精度，LP8769在输出电压低至700mV 条件下，可以做到 +-3%精度

Figure 1-3. Summary of TPS6594 and LP8764 Series Models

2 Introduction to Main Modules of TPS6594

The functional modules of TPS6594 and LP8764 are similar. Here, TPS6594 is taken as an example to introduce the main internal modules of the chip. The internal architecture block diagram of TPS6594 is shown in Figure 2-1. According to the sequence of numbers marked in the figure, we can roughly divide it into the following modules:

1. VSYS Input Control Module
2. Power Distribution Module
3. Voltage Monitoring Module
4. BUCK Module
5. LDO Module
6. IO Module
7. Digital Logic Module

LP8764 does not have the VSYS input control module and the LDO module; other modules are highly similar to TPS6594 and can be cross-referenced. This article will introduce the functions and behavioral logic of these modules one by one. Due to space limitations, content related to the digital logic module will be described in subsequent articles.

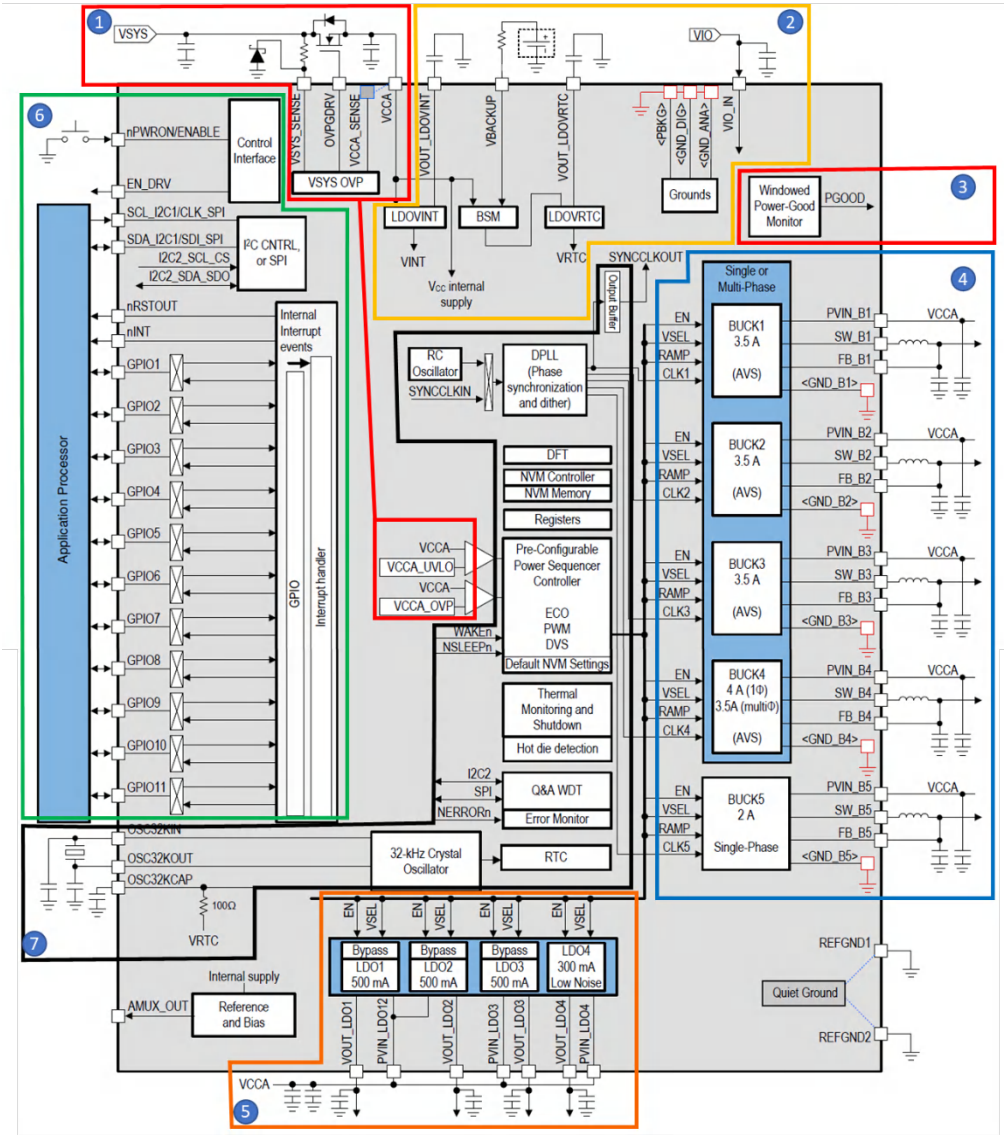

Figure 2-1. TPS6594 Internal Architecture Block Diagram

2.1 VSYS Input Control Module

TPS6594 is a low-voltage input PMIC, and its maximum input voltage does not exceed 6V. However, automotive systems are generally powered by 12V batteries, which requires the system to add a pre-stage primary BUCK to convert the 12V high voltage into a low voltage less than 6V. TPS6594 has no special requirements for the functional safety level of this primary BUCK. This chip is designed with a functional safety mechanism that connects a controlled NMOS in series between the pre-stage output and the chip input, which can avoid system cascading failure brought by the failure of the first-stage BUCK. Users need to design the circuit according to the Assumption of Usage in the functional safety documentation to achieve the system-level ASIL D functional safety goal.

TPS6594 is designed with a VSYS control mechanism to control this NMOS, and its structure is shown in Figure 2-2. The OVPDRV Charge Pump module provides a high voltage to turn on the external NMOS. The VSYS_OVP_Monitor monitors the input VSYS voltage and compares it with the internal bandgap reference. If it exceeds the set VSYS_OVP_Rising threshold (5.8~6V, where the range means this threshold varies with different chips), it turns off the NMOS to ensure subsequent modules are not affected.

When the voltage on VSYS_SENSE exceeds the VSYS_OVP_Rising threshold, an internal Gate Discharge module discharges the NMOS gate voltage to achieve a fast shutdown effect. The Discharge circuit can quickly discharge charges of a maximum 4nF gate capacitance. At the same time, the voltage on VCCA is quickly discharged by the internal VCCA_PD module, and its discharge resistance is around 140 ohms.

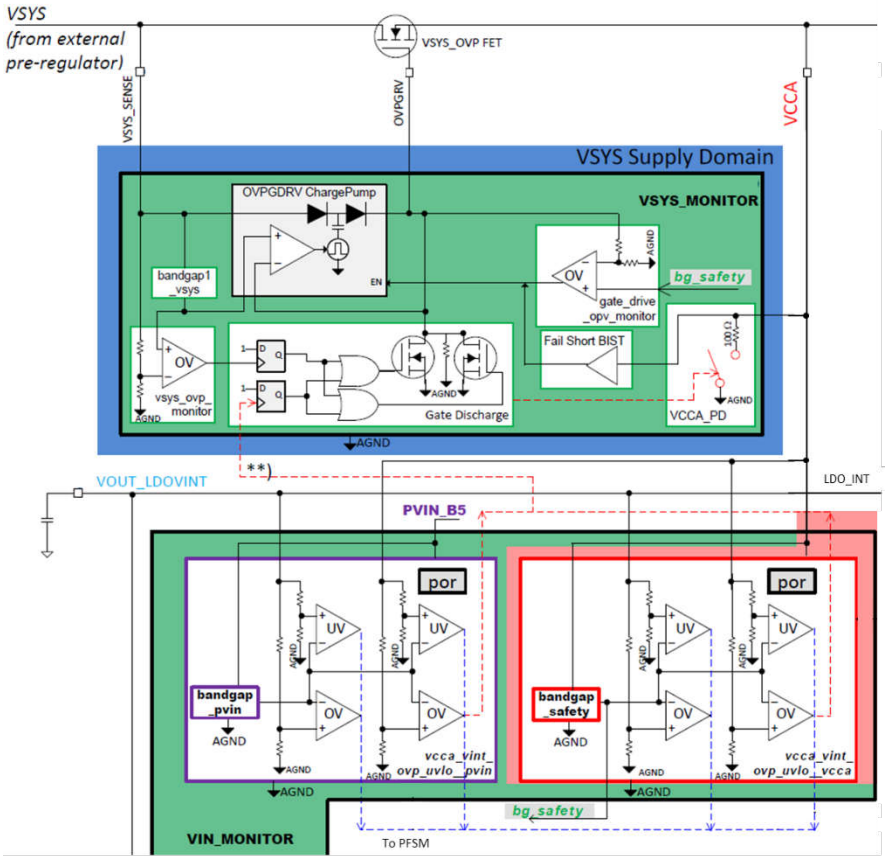

Figure 2-2. TPS6594 VSYS Control Module Architecture Block Diagram

TPS6594 is designed with a special Fail Short BIST test to guarantee that the D and S of the NMOS possess a sufficiently large impedance to isolate VSYS and VCCA in the off state. The Fail Short BIST will perform a pre-turn-on action on the NMOS after the VSYS voltage reaches the power-on threshold of VSYS_UVLO_Rising_TH (2.4~2.7V), and then judge whether the D and S of the NMOS are short-circuited based on whether the voltage on VCCA exceeds the threshold of OVP_FET_Short_TH. This BIST action is unrelated to whether the enable pin of the chip is pulled up or not. A normal power-up waveform is shown in Figure 2-3. We do not need to pay

attention to the state of the enable pin here. It can be seen that before OVPDRV is completely turned on, there will be a small triangle that allows part of the energy to flow through the NMOS, and a step will subsequently appear on VCCA. This step will not drop because the power-on threshold of VCCA (2.7~3V) is not reached at this time, so this part of energy will not be consumed, nor will it rise further, because the NMOS has turned off at this time and no more energy is injected. The chip judges whether the D and S of the NMOS are short-circuited by detecting whether this step voltage is lower than $V_{OVP\_FET\_Short\_TH}$ (0.3~0.42V).

Figure 2-3. TPS6594 Fail Short BIST PASS Waveform

In addition to the direct monitoring of VSYS on the input side, the state of the NMOS is also affected by the VCCA voltage. There are two input voltage monitoring modules backing up each other inside the TPS6594. To distinguish them from the VCCA monitor module introduced later, they are called VIN monitors here. When the VCCA voltage exceeds the VCCA_OVP_Rising threshold (for 3.3V VIN it is 3.9~4.1V, for 5V VIN it is 5.6~5.8V), the Gate Discharge module is turned on to make OVPDRV 0V, turning off the NMOS to protect subsequent circuits, and the signal path is shown as the red dashed line.

At the same time, these two monitoring circuits backing up each other also monitor the overvoltage (>1.98V) / undervoltage (<1.62V) of VINT and the UVLO of VCCA (written as VPOR in the manual, which has two thresholds of rising and falling, with a value around 2.7V, possessing a 100mV hysteresis interval). These several signals control the de-assertion of reset of the digital logic, and the signal path is shown as the blue dashed line. If any one of these three conditions is not satisfied, even if the enable pin is pulled high, the PMIC still will not power up.

This control mechanism of VSYS is a beneficial mechanism for achieving high functional safety goals, but it can cause interference to troubleshooting. Once VSYS or VCCA triggers overvoltage protection (note it is OVP, not the OV mentioned later), VCCA will lose power, leading to the loss of all register information. Therefore, during the troubleshooting process, the hardware can be modified to shield the VSYS control mechanism. The method is to short-circuit the D and S of the NMOS, and connect the VSYS SENSE pin to ground. At this time, regardless of whether VSYS/VCCA is overvoltage or not, VSYS and VCCA are always connected, the digital logic part of the PMIC always works, and register information will always be retained.

2.2 Power Distribution Network

The internal power distribution architecture of TPS6594 is shown in Figure 2-4, which can be divided into several parts: VSYS domain, VCCA domain, VINT domain, VRTC domain, and VIO domain. Among them, the VSYS

domain includes the VSYS control module introduced previously. Modules in the VCCA domain draw power directly from VCCA, including the VIN monitor monitoring VCCA introduced earlier, the internal reference source, the LDO supplying power to the EEPROM, two LDOs supplying power to the INT domain and RTC domain, and the VBACKUP main/backup power switching module, etc.

Modules in the VINT domain are powered by the 1.8V output regulated by INTLDO. The VINT voltage can be measured at pin number 2. This part of modules includes internal digital circuits, clock modules, BUCK/LDO control and monitoring modules, IO modules, and an additional VCCA monitoring module, etc.

The VRTC domain is similar to the VINT domain, powered by a separate LDO, namely LDORTC, and the voltage is also 1.8V. This voltage can be measured on pin 3 of the chip. This part of modules represents all parts that need to remain working in sleep mode, including the RTC clock and wake-up circuits, etc. When VCCA is in UVLO, LDOINT turns off, but the LDORTC voltage can choose to draw power from the VBACKUP pin. At this time, the most basic RTC function will continue to work.

The VIO domain is relatively special. In actual circuits, it generally needs to draw power from the output of the PMIC, and it only includes the input and output part circuits of some IO pins. The input and output circuits of some IOs are powered by LDOINT and LDORTC; therefore, attention needs to be paid in application that the high levels of different IOs are different.

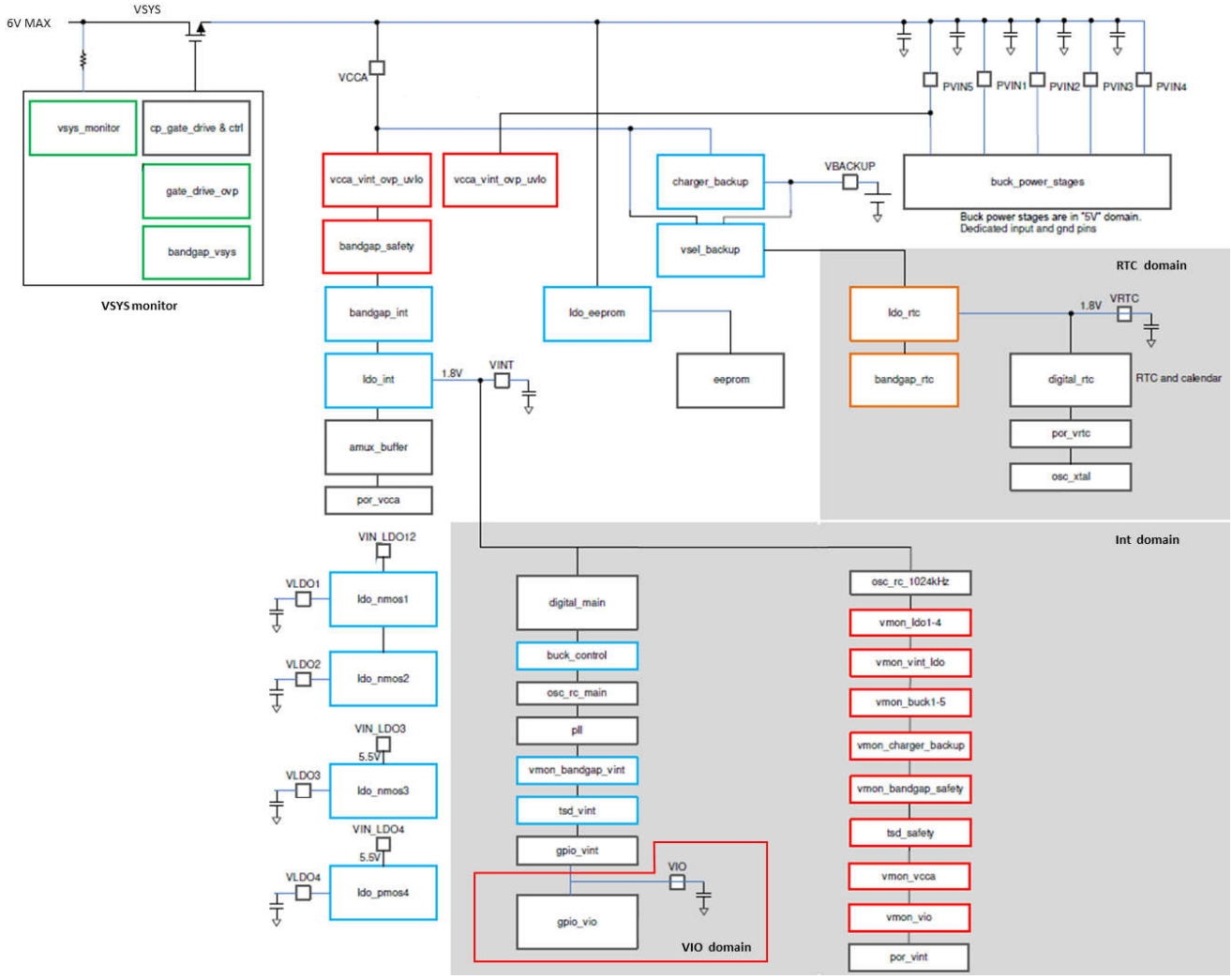

Figure 2-4. TPS6594 Power Architecture Block Diagram

2.3 Voltage Monitoring Mechanism

The internal voltage monitoring modules of TPS6594 are shown in Figure 2-5, with three major categories in total: VCCA VMON, BUCK VMON, and LDO VMON. Among them, the VMON modules for BUCK and LDO are very similar, both possessing three detection sub-modules: overvoltage (OV), undervoltage (UV), and residual voltage (RV), which will be introduced together later. Inside the LP8764, there are also independent VMON modules used to monitor external voltage signals sent from GPIO7/8. Its working principle is similar to the VCCA VMON voltage monitoring mechanism, so it will not be expanded upon separately here.

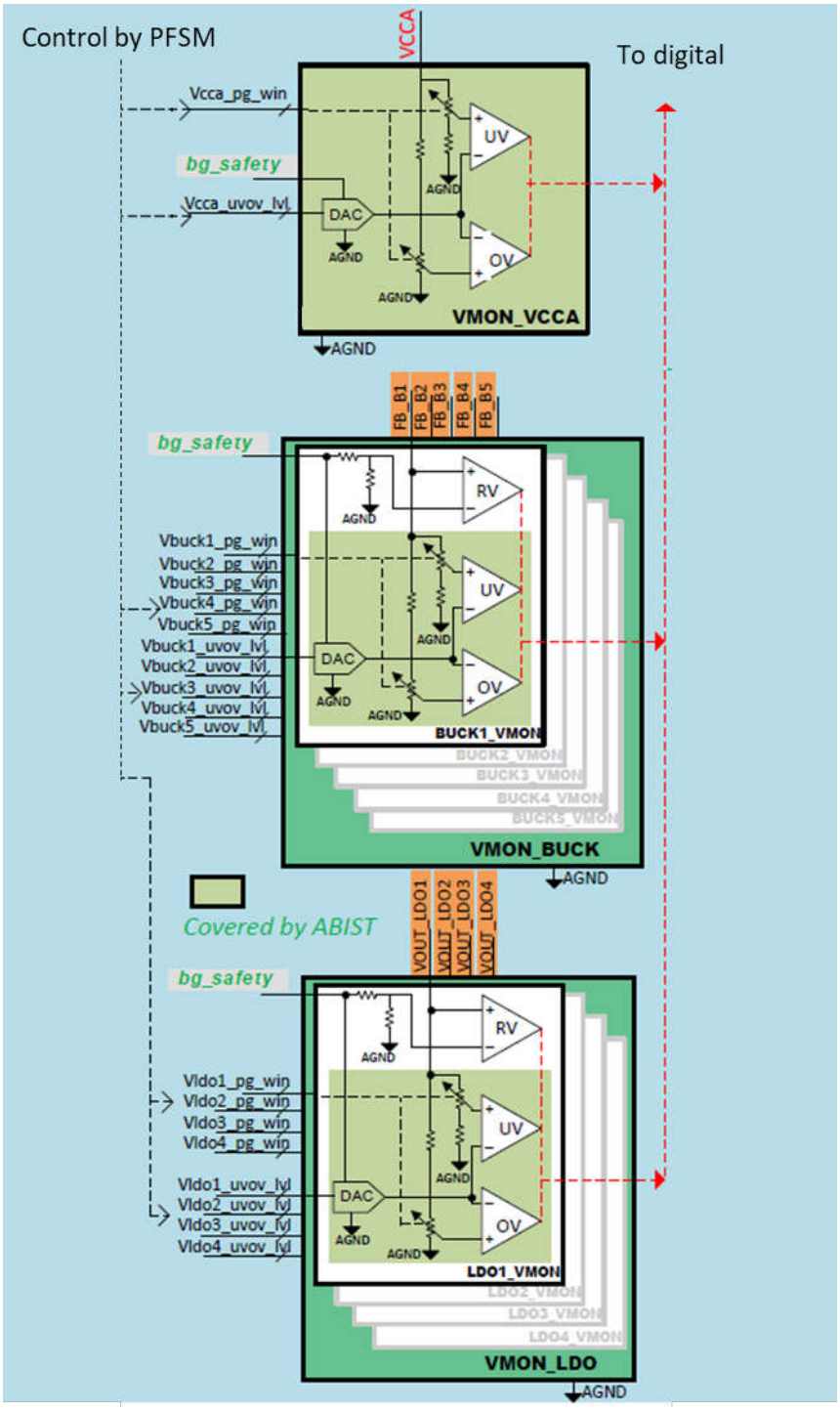

Figure 2-5. TPS6594 VMON Mechanism Block Diagram

VCCA VMON is a redundant monitoring mechanism independent of the VIN monitor mentioned earlier. The threshold of the VIN monitor is set by hardware, and its result directly acts on the VSYS control module to make the device be in a power-down protection state. However, the threshold of VCCA VMON is set by NVM (firmware in non-volatile memory), and its result only affects the state transitions of FFSM (fixed finite state machine) and PFSM (programmable finite state machine). The programmable characteristic of PFSM determines that the output of VCCA VMON will exhibit different results according to different PFSMs. Content regarding NVM and state machines will be introduced in the second article of the series.

The VCCA monitor consists of two comparators, OV and UV. The two inputs of the OV comparator are the VCCA voltage and the target voltage (uvov_lvl) + percentage threshold (pg_win) set by NVM. The two inputs of the UV comparator are the VCCA voltage and the target voltage (uvov_lvl) - percentage threshold (pg_win) set by NVM.

After understanding the two monitoring mechanisms of VCCA (OVP and OV), one can better understand which mechanism was triggered by VCCA UVLO, VCCA OVP, VCCA UV, VCCA OV, VSYS UVLO, and VSYS OVP respectively, as well as the corresponding chip states and recovery conditions. Below they are arranged and summarized from low to high according to the triggering level height:

1. VSYS UVLO: The VSYS voltage is lower than the VSYS_UVLO_Rising_TH (2.4~2.7V) threshold, the VSYS control logic is in a reset state, OVPDRV is 0V, and the NMOS turns off. When the voltage on VSYS is higher than the VSYS_UVLO_Rising_TH threshold, Fail Short BIST begins, and the NMOS is turned on.
2. VCCA UVLO: This is the UV mechanism of the VIN monitor being triggered. The voltage on VCCA is lower than the VCCA_UVLO threshold (about 2.7V), and the digital logic part of the chip is in a reset state. Higher than the VCCA UVLO threshold, the chip digital logic works but the state machine will not enter the initialization state.
3. VCCA UV: This is the UV mechanism of VCCA VMON being triggered. During the startup phase, the VCCA voltage must be higher than the VCCA UV threshold for the state machine to enter the initialization state. In normal working conditions, when VCCA UV triggers, the chip decides the state change according to the content of PFSM, which could be shutting down to enter the safe state or performing no operation.
4. VCCA OV: This is the OV mechanism of VCCA VMON being triggered. This monitoring mechanism is valid only in normal working status. The chip decides the state change according to the content of PFSM, which could be shutting down to enter the safe state or performing no operation.
5. VCCA OVP: This is the OV mechanism of the VIN monitor being triggered. When VCCA OVP triggers, OVPDRV is 0V, turning off the NMOS. Note that after VCCA OVP triggers, the VSYS control module has a deadlock mechanism; it is not that OVPDRV will recover as soon as VCCA OVP disappears. VSYS needs to fall below the VSYS_UVLO_Rising_TH (2.4~2.7V) threshold to reset the VSYS digital logic before OVPDRV will pull high again.
6. VSYS OVP: This is the OV of the VSYS monitor being triggered. OVPDRV is 0V, and the NMOS turns off immediately. Even if the overvoltage on VSYS disappears, the NMOS still will not turn on. VSYS must fall below the VSYS_RC_TH threshold for at least tVSYS_RC_TH (5ms) to restart the chip before the NMOS will turn on again.

The VMON modules of BUCK and LDO include three comparators, among which the principles of OV and UV are the same as those of VCCA VMON, so they will not be expanded upon much. he results of each BUCK/LDO output voltage exceeding thresholds are sent to the PFSM to decide the state transitions of the chip according to PFSM settings. The residual voltage detection mechanism (RV) will detect the voltage on the output pins before each power rail starts up, ensuring the residual voltage is below threshold requirements, used to avoid system damage that residual voltage might cause.

The RV mechanism has two application scenarios. One is to detect the residual voltage of the power rail before power-up; during the startup phase, residual voltage will block the device from entering the BOOT BIST state from the INIT state. Before the residual voltage disappears, all power rails have no output. The second is the detection of the voltage on the power rail when the power rail shuts down, but this function is rarely used and generally not used.

For BUCK, residual voltage may come from a previous power-down that was not completely executed, or a short circuit between the PVIN pin and the SW pin, or a short circuit of the high-side MOS FET inside the chip. For

LDO, residual voltage may mean a previous power-down was not completely executed, a short circuit between the PVIN pin and the LDO output pin, or a short circuit of the internal power MOS of the chip, etc.

As shown in Figure 2-6 is the schematic diagram of residual voltage detection after BUCK power-down. The left side is the pass case, and the right side is the fail case. After reaching the timeout threshold, if the output pin voltage is still greater than TH_SC_RV (140~160mV), it outputs warning information to the PFSM. Extra attention is needed: the warning for RV detection fail and the warning for BUCK output short circuit use the same interrupt register bit (BUCKx_SC_INT). It must be carefully distinguished during the troubleshooting process. The BUCK RV timeout threshold needs to be calculated according to the formula: BUCKn_RV_TIMEOUT = BUCKn_VSET / BUCKn_SLEW_RATE + 100 µs, where BUCKn_VSET is the set voltage of the current BUCK route, and BUCKn_SLEW_RATE is the power-up/down slope of the current BUCK route, set by registers.

The RV detection of LDO is very similar to BUCK, with the difference that its timeout threshold is directly set by the register LDOn_RV_TIMEOUT, instead of being calculated according to the power-up/down slope. Same as BUCK, LDO RV fail also shares one interrupt bit (LDOx_SC_INT) with LDO short circuit.

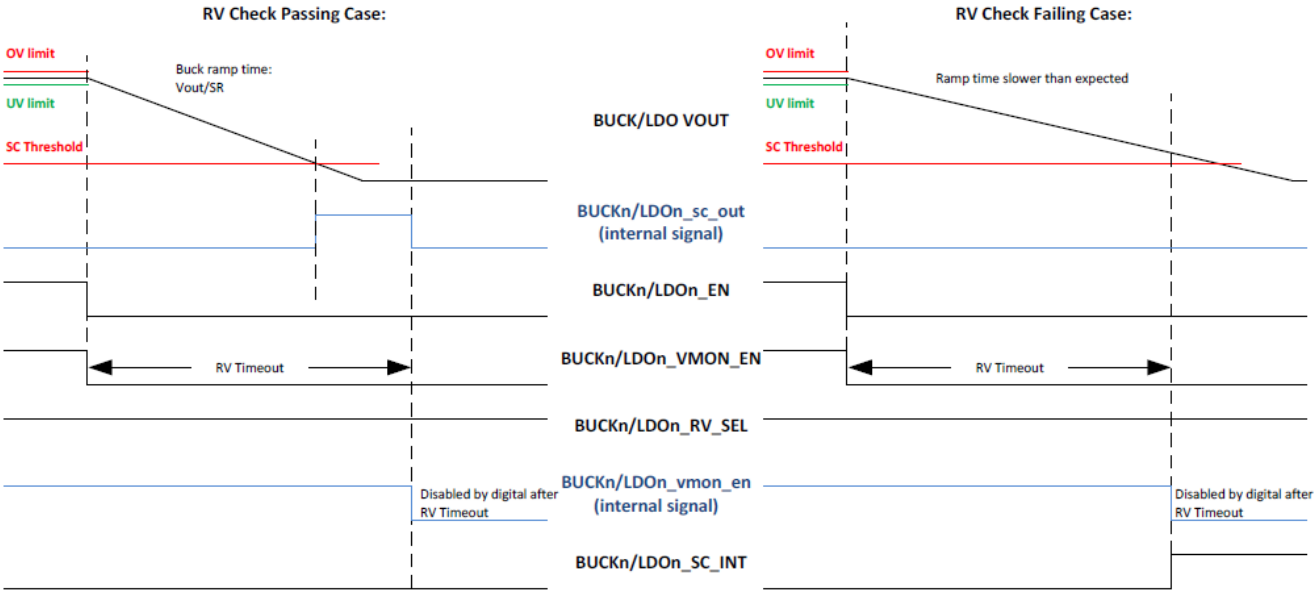

Figure 2-6. TPS6594 RV Mechanism Schematic Diagram

2.4 BUCK Module

Before understanding the BUCK module, it is necessary to first understand the clock tree of the system. There are three clocks inside the PMIC, and the clock tree is shown in Figure 2-7. The 128kHz clock is provided to the VMON module, and used by the charge pumps of LDOs and BUCKs. There are two 20MHz clocks in total; one is the main clock, and the other is the reference for the main clock to provide a high functional safety guarantee. The 20M main clock acts as the SW clock of BUCK after passing through the DPLL. Meanwhile, the PMIC supports inputting a clock from the external side to synchronize with the SW of the external BUCK. When an external clock input exists, the EXT_CLK_INT interrupt is set, and the chip automatically switches to using the external clock. TPS6594 likewise supports sending the internal clock to the external side to synchronize other BUCK chips. SYNCCLKOUT can be set on GPIO8, GPIO9, or GPIO10 for output.

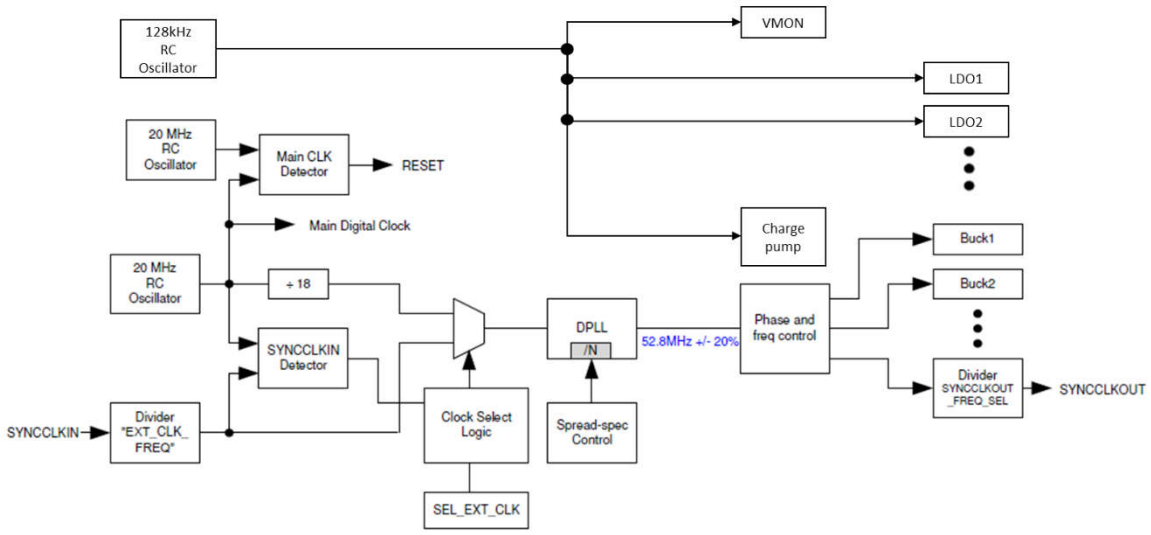

Figure 2-7. TPS6594 Internal Clock Tree

There are 5 routes of BUCKs in total in TPS6594. The block diagram of the BUCK module is shown in Figure 2-8, including BUCK control digital circuits, upper and lower power transistors, charge pumps, loop comparators, SW short circuit detection modules, and current limit modules. The parts of BUCK control digital circuits, upper and lower power transistors, charge pumps, and loop comparators are similar to ordinary BUCKs, so they will not be expanded upon much here.

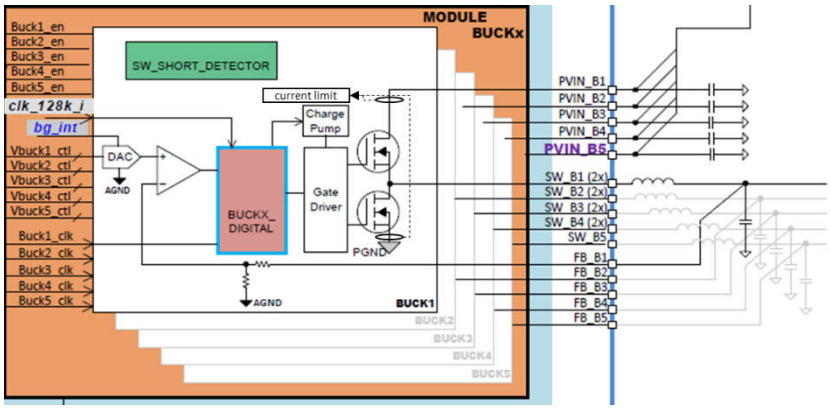

Figure 2-8. TPS6594 BUCK Module Block Diagram

The special place for these several routes of BUCKs in TPS6594 is that BUCK1-BUCK4 can be flexibly combined into multiple multi-phase modes, and unused FB ports can be used to monitor externally inputted voltages. Depending on different settings of NVM, multi-phase configurations include five modes in total, which can be judged through the complete model number of TPS6594:

1. BUCK1/2/3/4, which is a four-phase parallel output, named as TPS659411xx, for example, TPS65941120.
2. BUCK1/2/3+BUCK4, which is a three-phase parallel + one route of independent output, named as TPS659412xx, for example, TPS65941213.
3. BUCK1/2+BUCK3+BUCK4, which is a two-phase parallel + two routes of independent output, named as TPS659413xx, for example, TPS65941319.
4. BUCK1+BUCK2+BUCK3+BUCK4, which is four routes of independent outputs, named as TPS659414xx, for example, TPS659411421.
5. BUCK1/2+BUCK3/4, which is two routes of two-phase parallel, named as TPS659415xx, for example, TPS65941515.

It can be seen that the third to last digit represents different BUCK output configurations, while the last two digits represent different NVM version numbers.

When BUCK works independently, there are automatic light-load mode and forced PWM mode available for choice. The two modes need to be set through corresponding bits in NVM. In automatic light-load mode, when the load current is small, SW emits pulses intermittently to improve efficiency under light load.

In multi-phase mode, the PMIC supports automatically increasing or decreasing phases according to load conditions. Therefore, under light load conditions, seeing that only the SW of BUCK1 (for the fifth BUCK setting, it is BUCK1 and BUCK3) has waveforms is completely reasonable. The SW waveform test results with both automatic light-load and automatic phase adding/subtracting enabled are shown in Figure 2-9 and Figure 2-10. From Figure 12, it can be seen that under light load conditions, the device is in PFM mode. The load gradually increases, and SW gradually changes into PWM mode. At this time, only SW1 is turned on. The switching threshold from PFM to PWM is about 600mA, and the threshold for switching back from PWM to PFM is about 300mA. From Figure 13, it can be seen that with the increase of load current, SW2 to SW4 turn on gradually, and the switching thresholds are around 2A, 4A, 6A sequentially. Note that this is the test result of load from small to large, roughly at 0.8A, 1.8A, 2.4A.

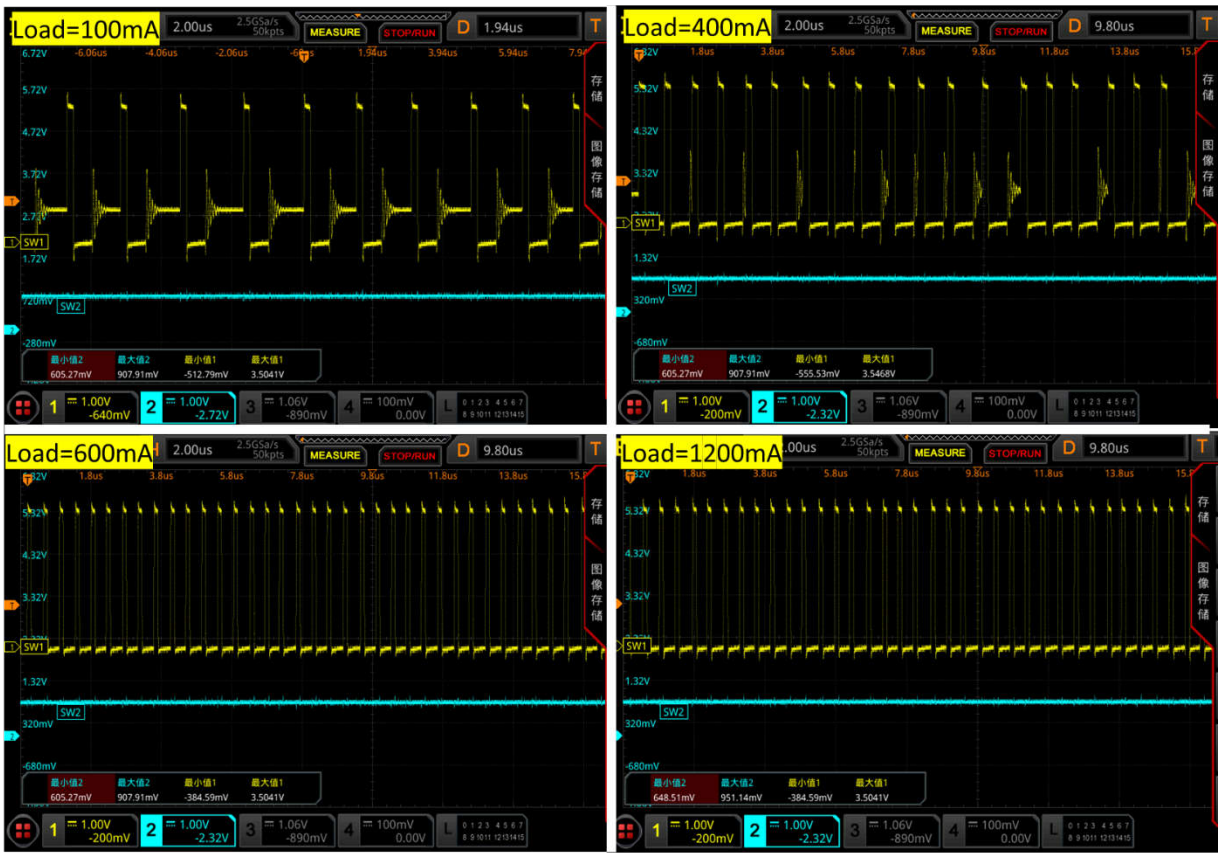

Figure 2-9. SW Changes with Load Current 1

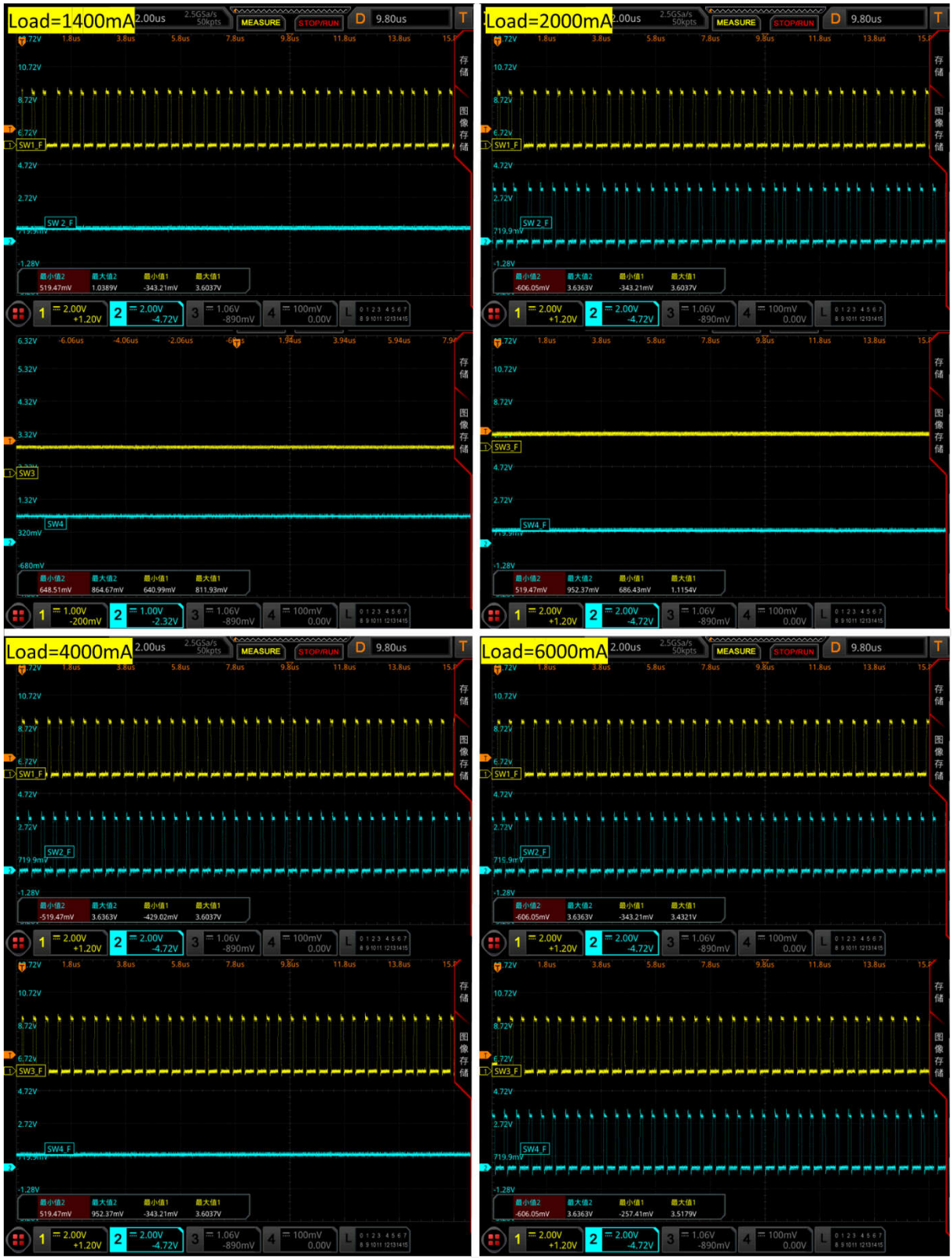

Figure 2-10. SW Changes with Load Current 2

During BUCK operation, it will detect the current on the power MOS and compare it with the set current threshold ILIM. The threshold of the upper transistor is set by BUCKx_ILIM of registers, having several levels: 2.5A, 3.5A, 4.5A, and 5.5A. The threshold of the lower transistor is a fixed 2A. If within one cycle the upper transistor

current exceeds the set ILIM value or the lower transistor current does not fall below the 2A threshold, a BUCKx_ILIM_INT interrupt will be reported. Attention is needed: what this current detection mechanism detects is not a direct detection of the load current, but an indirect monitoring of the inductor current by detecting the currents of the upper and lower transistors. As can be seen from the relationship between inductor current and load current shown in Figure 2-11, using this mechanism to detect load overcurrent will have two problems. One is that it is very rough, having only 4 levels. The second is that it is an indirect measurement. When setting the BUCKx_ILIM threshold, it must be considered to take into account the current ripple of the inductor on the basis of the load current, while reserving a certain margin on the basis of the inductor peak current.

Generally speaking, in several sub-models of TPS6594 and LP8764 pre-set with NVM by TI, PFSM will not be affected by the ILIM INT interrupt, realized by setting the EN_ILIM_FSM_CTRL bit to 0. Under this state, even if overcurrent occurs, the system will not shut down. Load overcurrent is more often monitored by BUCK output UV.

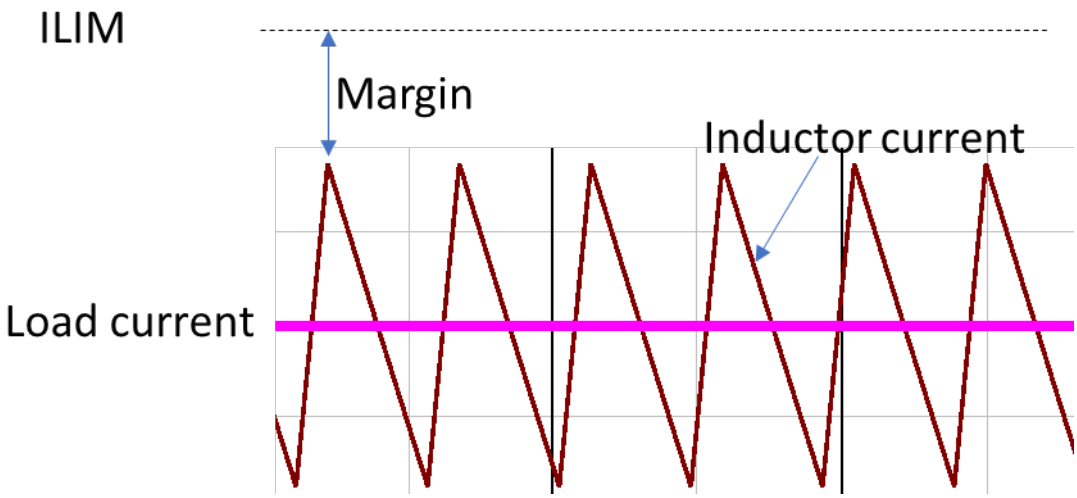

Figure 2-11. Relationship between Inductor Current and Load Current

BUCK judges whether SW is short-circuited to ground by detecting the output voltage. Potential factors causing a short circuit to ground may be the lower transistor short-circuiting to ground or the load short-circuiting to ground. Short circuit detection and RV detection share one hardware circuit; therefore, they also share the same threshold and the same interrupt bit, namely BUCKx_SC_INT. When a short circuit occurs, the device will decide whether to shut down according to the setting of PFSM.

2.5 LDO Module

The LDO block diagram is shown in Figure 2-12, in which LDO1-3 use a charge pump to drive NMOS, and LDO4 is a low-noise LDO, using PMOS. The output capability of LDO1-3 is around 500mA, and the output current capability of LDO4 is around 300mA. According to different settings of registers, LDO can work either in LDO mode or in bypass mode. The LDO in bypass mode no longer has a step-down function but merely acts as a Load switch to control the power-up sequence. Same as BUCK, LDO also has a VOUT short circuit detection mechanism. When VOUT is lower than the TH_SC_RV threshold, the device reports an LDOx_SC_INT interrupt. Here, same as BUCK, LDO short circuit and RV share one register bit. Same as BUCK performing detection for upper and lower transistor currents, LDO also has power transistor overcurrent protection, with a threshold of Ishort(LDOn), set by hardware. LDO4 is lower than LDO1-3, and attention needs to be paid during application to avoid overcurrent.

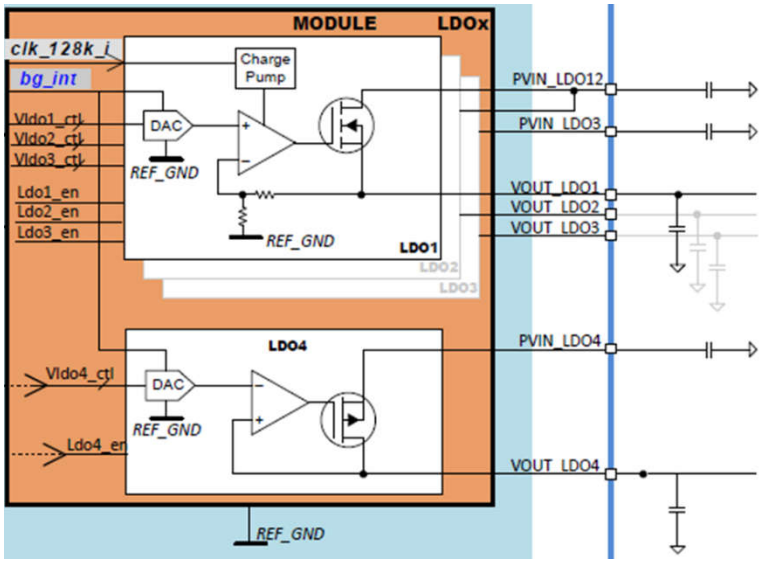

Figure 2-12. TPS6594 LDO Module Block Diagram

2.6 IO Module

The TPS6594 IO module includes 11 GPIOs and three specific-function IOs: nINT, EN_DRV, and nRSTOUT. Among them, GPIOs can be configured through registers to be multiplexed as the de-assertion of reset pin of SOC (nRSTOUT_SOC), power good indication (PGOOD), ESM inputs of SOC and MCU (nERR_MCU & nERR_SoC), watchdog feeding (TRIG_WDOG), disabling watchdog (DISABLE_WDOG), external wake-up (WKUP1, WKUP2), and low-power wake-up (LP_WKUP1, LP_WKUP2) functions, etc. As shown in the GPIO block diagram in Figure 2-13, it can be seen that different GPIOs are powered by different power supplies; therefore, parts of the multiplexed functions can only be used on fixed GPIOs. For example, LPWKUP can only be multiplexed on GPIO3/4 because these two IOs are powered by VRTC. In application, the functions that each GPIO can multiplex need to be reasonably allocated by referring to the manual content.

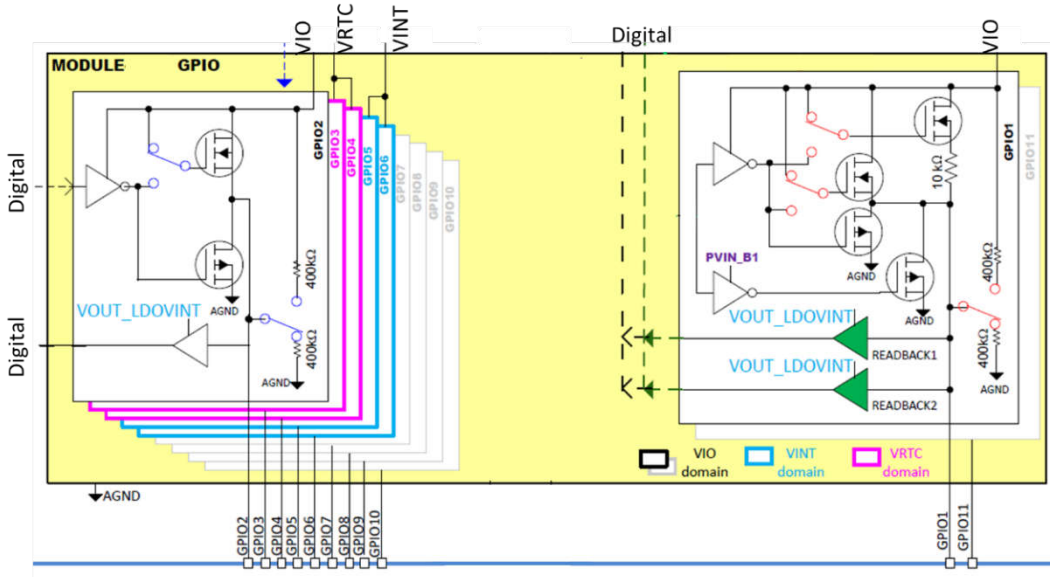

Figure 2-13. TPS6594 GPIO Module Block Diagram

nRSTOUT is the de-assertion of reset pin of the SOC. During the power-up process, this pin remains at a low level until all power rails finish powering up, then this pin will be pulled high to de-assert reset of the MCU.

nINT is the interrupt indication pin. When there is an interrupt in the interrupt registers of 5A-6C, this pin is pulled low. Attention is needed that some interrupts will also be generated during normal power-up. Interrupts include fault warning entries as well as other information. The existence of these interrupts will lead to the nINT pin being at a low level even during normal power-up. This pin will pull high only after software operations clear all interrupt information.

The EN_DRV pin is used to control the enable pin of system peripherals, and a typical application is shown in Figure 2-14.

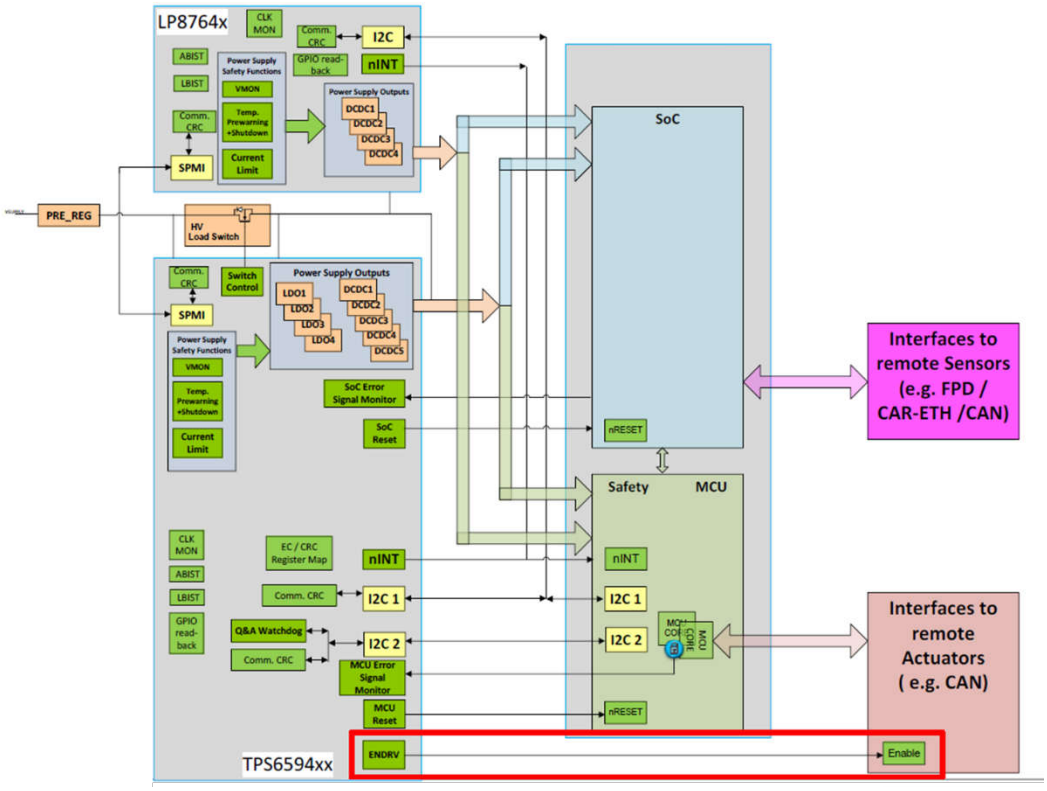

Figure 2-14. TPS6594 ENDRV Typical Application Schematic Diagram

The pulling low of the EN_DRV pin is controlled by PMIC hardware, and the pulling high is operated by software writing to registers. When any interrupt appears in the system, this pin is pulled low, and the priority of this pulling low is higher than the priority of pulling high by register operations. To pull high this pin, it is required to follow the operation flowchart below:

1. Begin normal watchdog feeding or disable the watchdog.
2. Begin having normal ESM input or disable the ESM mechanism.
3. Clear all interrupts of the 5A-6C interrupt registers.
4. Set 0x82 bit3 to 0.
5. Set 0x80 bit0 to 1.

3 References

1. Datasheet "TPS6594-Q1 Power Management IC (PMIC) with 5 BUCKs and 4 LDOs for Safety-Relevant Automotive Applications"
2. Datasheet "LP8764-Q1 Four-Phase, 20-A Buck Converter With Integrated Switches"
3. Datasheet "TPS6594-Q1 Safety Manual" (request through mySecure)
4. Datasheet "LP8764-Q1 Safety Manual" (request through mySecure)

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