Advanced High-Side Switch With Dynamic Current Limit for IO-Link Master

Introduction

High side switches are often used in industrial systems to drive different kind of loads. Depending on the load there are different requirements for the switch. A capacitive load behaves different than an inductive or resistive load. A special challenge for high side switches is a capacitive load at high output currents or the L+ line of an IO-Link master port. During switching, a high-power dissipation is a challenge for the device. This can be overcome by changing the drive current dynamically.

Implementation

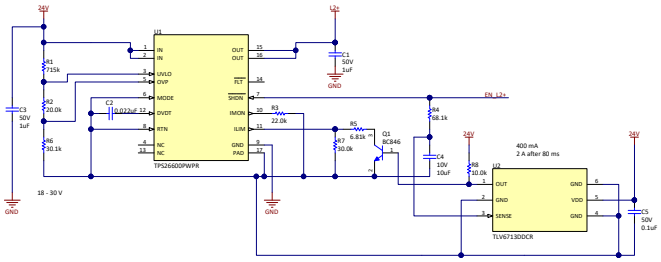
In this application a TPS26600 eFuse is used to implement a high side switch with advanced features and monitoring options.

This eFuse already has an integrated FET, as well as configurable OVP and UVLO. Moreover it has an adjustable current limit, shutdown control as well as current sense and a fault output. It also includes an input reverse polarity protection (IRPP) and reverse current blocking (RCB).

To realize a dynamic current limit it is necessary to change the current limit resistor during operation. A low current will prevent the device from running into thermal shutdown when starting to charge a large capacitive load as it might be found in some actuators or IO-Link devices.

After a certain time when the inrush phase is completed, it switches to a higher current limit of e.g. 2 A.

Figure 1. Schematic of eFuse With Current Control



This increase in current after an inrush time can be implemented by changing the current set resistor after turn on. The control signal (going to the SHDN pin) is used for generating a delay and changing the current set resistor. In Figure 1 the schematic of this implementation is shown. The delay is generated by an RC delay followed by a comparator to have an accurate switching point. It is driving a transistor, that switches a resistor in parallel to the fixed current set transistor. When designing such a circuit keep in mind that an RC delay is not a very accurate way for generating timings, as capacitors in that range are often within a 20% tolerance. Also the high and low level of the enable signal will influence the time.

The comparator used here has an internal reference of 0.4 V and is therefore very convenient for this application. The timing is set by R4 and C4, it can be estimated as: t = (0.4 V * 10 µF) / (3.3 V / 68.1 kΩ) = 83 ms.

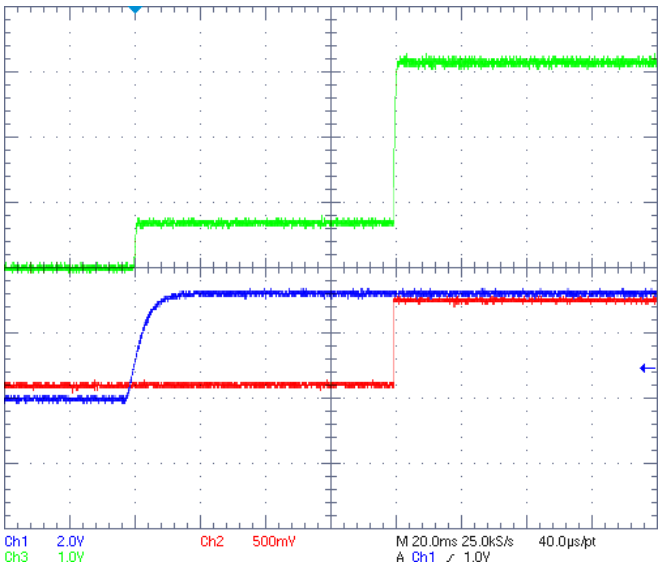
The current is set with R7 at the beginning as I = 12000 / 30 kΩ = 0.4 A. After 83 ms with R5 and R7 (parallel resistance is 5.55 kΩ) to I = 12000 / 5.55 kΩ = 2.16A.

Test Results

For testing this circuit, a resistive load of 12 Ω is connect to the output and the current is monitored at the IMON pin during switching on. Figure 2 shows the waveforms. The current sense is shown on channel three (magenta). Channel one (yellow) shows the enable signal. As soon as the enable goes high, a limited current of 0.4 A is going into the load.

After 80 ms, the out signal of the comparator goes high (channel two, blue) switching the current limit to 2.1 A.

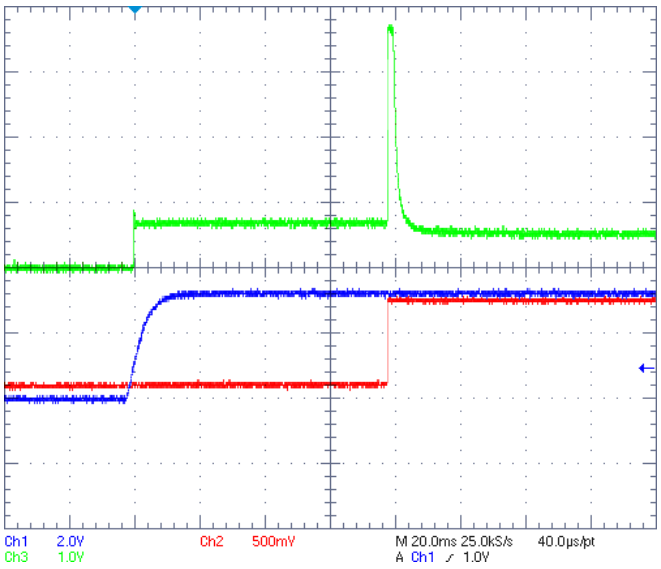
Figure 2. eFuse With Resistive Load



A resistive load is usually not a problem, as the voltage follows the current immediately and the power dissipation in the switch is not very high. More interesting is a capacitive load. During the turn on, the capacitor has to be charged from zero, reulting in a very high current and low output voltage at the beginning. This results in a very high power dissipation (24 V * 2 A = 48 W) for a short time. Even though the time is short, this will trigger an over temperature limit and the starting will either fail or restart until the capacitor is fully charged.

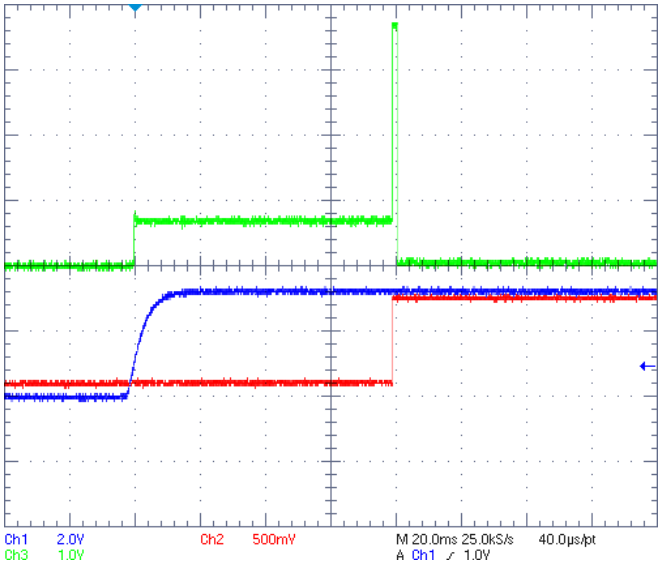
In such a case, starting with a low current will improve this and prevent triggering the temperature limit. Starting with a limit of 0.4 A is less than 10 W of dissipation, which is much better to handle. In Figure 3 this case is shown. The capacitive load (with parallel resistance) is precharged during the first 80 ms with a lower current (and therefore lower power dissipation). After 80 ms the current limit is switched to 2 A. The capacitor is not yet fully charged, but not at zero any more. So with a short current pulse the high side switch does not have to handle the voltage drop of 24 V anymore and not the 48 W of pulse power.

Figure 3. eFuse With Capacitive Load



A third test is done with a resistor of 1 Ω at the output as required by the IO-Link test specification. Figure 4 shows the scope plot. This shows the eFuse is able to limit the current to 0.4 A for at least 80 ms. But after switching to 2 A, it can handle this for only a few milliseconds. Here the power dissipation is too high, causing the device to overheat internally and shut off. However this behavior fulfills the requirements for an IO-Link master port.

Figure 4. eFuse With 1 Ohm Load Output



The configuration shown here is a good approach for driving capacitive loads without stressing a high side switch to trip a thermal shutoff. Also it is suitable to drive the L+ line of an IO-Link master. There it is required by the test specification to deliver 400 mA for 50 ms into a load of 1 Ω, which can easily be done with this approach.

All the time the current through the device can be monitored by an MCU at the IMON pin.

Another approach to dynamically change the current can be realized by using a DAC or a PWM to inject a voltage into the ILIM resistor. Doing this to implement a constant power limit for a wide voltage input is described in Described in the LED-lighting control reference design for machine vision (TIDA-01081).

Table 1. Alternative Device Recommendations

Device	Optimized Parameters	Performance Trade-Off
TPS26620		Same device with lower 800 mA current
TPS26630	Same device with higher 6 A current	

References

http://www.ti.com/tool/TIDA-01081

http://www.ti.com/tool/TIDA-010016

http://www.ti.com/product/TPS2660

http://www.io-link.com/share/Downloads/Testspec/IOL-Test-Spec_10032_V112_Jul14.pdf

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