Using the TPS51116EVM

The TPS51116EVM evaluation module (EVM) is a dual-output converter for DDR, DDR2 and DDR3 memory modules. It uses a 10-A synchronous buck converter to provide the core voltage (VDDQ) for DDR memory modules. The EVM is designed to use a 4.5-V to 28-V supply voltage and a 4.75-V to 5.25-V controller bias supply. This allows the EVM to start up from a single 5-V supply or operate from a wide range of supply voltages with low power 5-V bias supply. The TPS51116EVM provides several jumpers and switches to allow the user to evaluate all of the TPS51116's configurations including lossless $R_{DS(on)}$ or resistive current sensing, current mode or D-CAP™ semi-hysteretic operation, DDR, DDR2 or DDR3 voltage standards and the S3 and S5 sleep states.

Contents

List of Figures

List of Tables

1 Description

The TPS51116 is designed to be a complete power supply solution for dual data rate (DDR) memory modules covering DDR (2.5 V/1.25 V), and DDR2 (1.8 V/0.9 V) and DDR3 (1.5 V/ 0.75 V) specifications. By combining a high-efficiency synchronous buck switching regulator and a high-current fixed ratio sink/source LDO regulator, the TPS51116 provides high-efficiency generation of the DDR memory cell's core and I/O voltages as well as providing an accurate, high-speed termination voltage. While the TPS51116 is designed to use the VDDQ output to power the termination voltage LDO, another power source can be used, allowing for more control and efficient operation of the termination voltage if lower voltages are available in the system. Powerful, efficient and flexible, the TPS51116 is a single device that can meet all DDR memory power needs.

1.1 Applications

- Dual Data Rate (DDR) High-Speed RAM Supply
- High Performance AGP Video Cards
- Notebook, Desktop and Sever Motherboards
- High Performance Computer
- High Memory Content Consumer Electronics

1.2 Features

- Up to 85% efficiency on the V_{DDQ} switching regulator output
- Dual switching regulator / LDO output for both DDR core and termination voltages
- 3-A sink/source termination voltage LDO regulator
- 10-mA termination reference voltage for DDR input reference
- User selectable DDR, DDR2, DDR3 or externally referenced supply voltages
- User selectable switching regulator or external supply source for LDO termination regulator
- Switches available for testing S3 and S5 sleep states

2 Electrical Performance Specifications

Table 1. Electrical Performance Specifications

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{VIN}	Supply voltage		4.5		28	V
V_{V5IN}	Logic supply voltage		4.75		5.25	
V_{VDDQ}	Switching output voltage	DDR mode	2.45	2.50	2.55	
		DDR2 mode	1.75	1.80	1.85	
		DDR3 mode	1.45	1.50	1.55	
$V_{VDDQ(RIPp-p)}$	Switching output voltage ripple	DDR2 mode, I_{DDQ} = 10 A	10		40	mV
I_{VDDQ}	Switching output current	I_{VTT} = 0 A	0		10	A
V_{VTT}	Termination voltage output	$V_{VDDQSNS}$ = V_{VDDQ}		V_{VDDQ}/2		V
Vtt(tol)	VTT output voltage tolerance to VTTREF		-40		40	mV
Vttripple(p-p)	Termination voltage ripple		0		20	
Vtt_Ref	Reference voltage	$V_{VDDQSNS}$ = V_{VDDQ}		V_{VDDQ}/2		V
Vtt_Ref(tol)	Reference voltage tolerance	I_{VTTREF} < 10 mA	-10		10	mV
η	Switching output efficiency	I_{VTTREF} = 0 mA, DDR2 mode, I_{VDDQ}= 10 mA, V_{IN}= 12 V		78%		
		I_{VTTREF} = 0 mA, DDR2 mode, I_{VDDQ}= 1 A		88%		
		I_{VTTREF} = 0 mA, DDR2 mode, I_{VDDQ}= 7 A		90%		
		I_{VTTREF} = 0 mA, DDR2 mode, I_{VDDQ}= 10 A		88%		

3 Schematic

The TPS51116EVM schematic is shown in Figure 1.

3.1 Jumpers

Standard 100-mil spacing headers JP1 through JP4 provide user configuration settings for the TPS51116EVM. Each jumper bank of three or six pins is provided with a single 100-mil shunt to allow the user to select the desired operation mode.

Table 2. Jumper Functions

JUMPER	SELECTION	DEFAULT
JP1	TPS51116 VDDQ discharge scheme, tracking, non-tracking or no discharge.	Tracking
JP2	Current sensing mode used by the TPS51116.	$R_{DS(on)}$
JP3	Control scheme used by the TPS51116.	D-CAP mode
JP4	Output levels DDR, DDR2, DDR3, or externally adjustable.	DDR2

3.2 Sleep State Switches

Switches SW1 and SW2 select the S5 and S3 sleep states respectively allowing the user to examine the reaction of the TPS51116 controller to these memory sleep states

3.3 Resistors and Shorts

Resistor R8 and short R9 allow the user to select between lossless $R_{DS(on)}$ and conventional resistive current sense. If resistive sensing is selected by JP2, R8 must be in place and R9 removed. If $R_{DS(on)}$ sensing is chosen by JP2, R9 must be in place, but since R9 and R8 are in parallel, R8 can be left on the PCB.

3.4 MOSFETs

The values of the MOSFETs Q1 and Q2 used on the TPS51116EVM are selected to optimize operation of the switching regulator over the 3-V to 28-V operating range for notebook power systems.

In applications with a regulated supply voltage available, it is possible to optimize the MOSFETs used to reduce losses and improve efficiency. For systems running from a fixed 12-V supply, the low duty cycle of the high-side MOSFET favors a higher $R_{DS(on)}$ for lower gate charge and faster switching times. For a regulated 12-V supply voltage, TI recommends Vishay SI4390 for Q1 and SI4378 for Q2 or equivalent MOSFETs.

For applications using a single 5-V supply rail for both the switching regulator and the TPS51116's VDD voltage, the high-side MOSFET duty cycles are higher, and thus favor a lower $R_{DS(on)}$ and somewhat higher gate charge. If a single 5-V supply voltage is used, TI recommends the Vishey SI4378 for both Q1 and Q2.

The use of these MOSFET pairs improves the high-load efficiency of the switching regulator by reducing MOSFET losses, however they may adversely effect lighter load efficiencies with increased switching and gate charge losses. Other MOSFET pairs are possible and even greater performance improvements can be realized by using PowerPak, LFPack or DirectFET MOSFETs at the increased cost of these customized power MOSFET packages. As each application's power needs are unique, each design may require the evaluation of several MOSFET pairs to determine the best MOSFET selection.

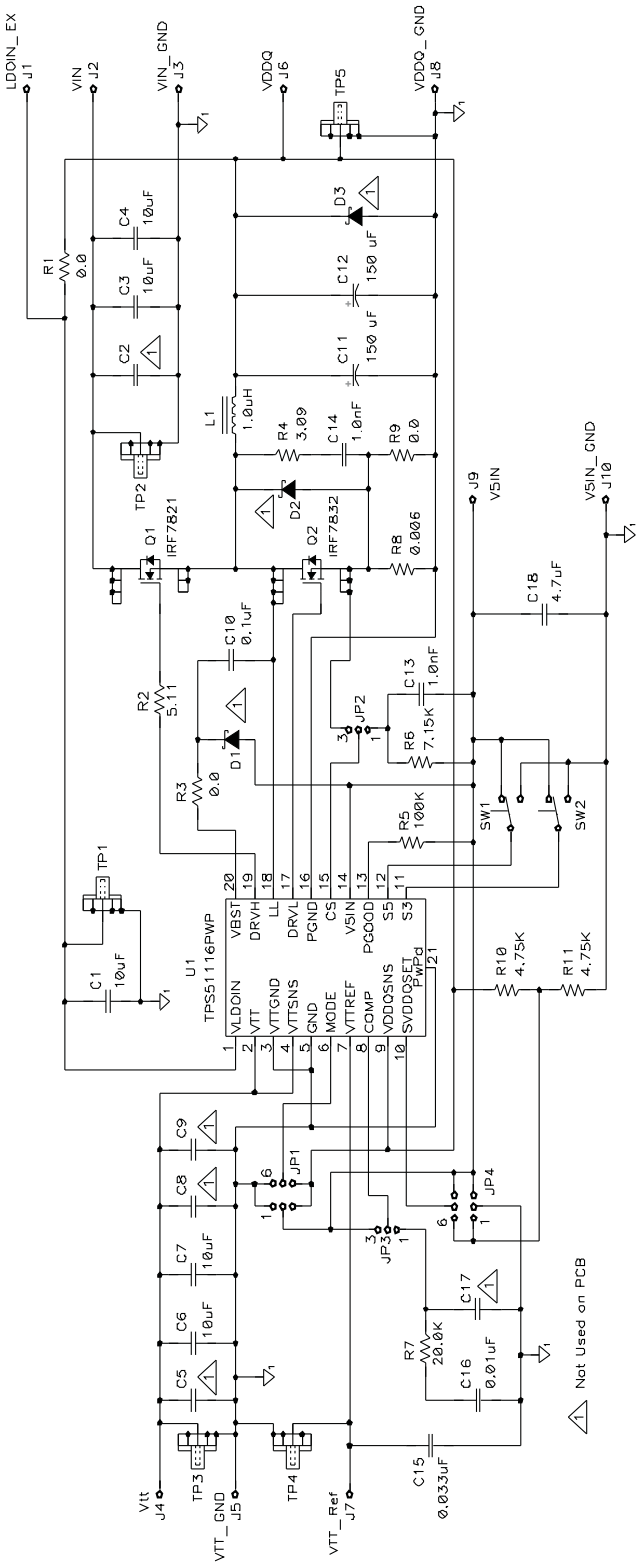


Figure 1. TPS51116 Schematic

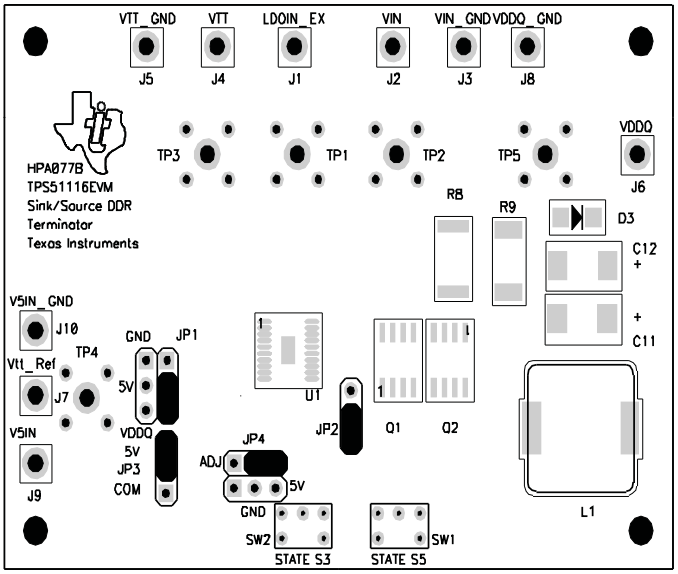
4 Configuration

4.1 User Selectable Configuration Modes

Figure 2 shows the location of the four jumper blocks, two switches and three resistors used to adjust the configuration of TPS51116EVM. Refer to the specific configuration settings sections regarding how to set each jumper, switch or resistor for the specific configuration desired.

CAUTION

Do not install jumpers in positions other than those shown.



State	S3	S4	VDDQ	VTTREF	VTT
S0			ON	ON	ON
S3			ON	ON	OFF
S4/S5			OFF	OFF	OFF

Figure 2. TPS51116EVM Jumper/Switch Locations and Default Positions

4.2 JP1 Tracking Discharge Mode

The TPS51116EVM comes preconfigured in tracking discharge mode. In tracking discharge mode, when the TPS51116 is set to discharge by turning on both S3 and S5 switches, the TPS51116 turns off both MOSFETs and sinks current slowly from the VDDQ output through an internal MOSFET. Because the resistance of this MOSFET is fairly high, the VDDQ level discharges slowly unless a heavy load is placed externally.

To program the EVM for tracking discharge mode set the JP1 jumper to the lower vertical position.

4.3 JP1 Non-Tracking Discharge Mode

The TPS51116EVM can be configured to operate in non-tracking discharge mode. To operate in non-tracking discharge mode the TPS51116 must be set in self-driven LDO supply voltage mode because the TPS51116 sinks up to 3 A from the VDDQ output until V_{VDDQ} discharges to 300 mV. If an external LDO supply is used, selecting non-tracking discharge mode can damage the TPS51116EVM as the LDO attempts to discharge this external supply and sink upto 3 A.

To program the EVM for non-tracking discharge mode set the JP1 jumper to the upper vertical position.

4.4 JP1 No Discharge Mode

The TPS51116EVM can be configured to operate in no discharge mode. In no discharge mode, the TPS51116 simply turns off the supply MOSFETs and leaves the output to be discharged by the load or self-discharge of the output capacitors.

To program the EVM for no discharge mode set the JP1 jumper to the center horizontal position.

4.5 JP2 $R_{DS(on)}$ Current Sensing

The TPS51116EVM comes preconfigured in a lossless $R_{DS(on)}$ current sensing mode. In this mode the TPS51116EVM uses the forward voltage drop of the low-side MOSFET (Q2) to monitor inductor current. If a fault is detected, the output voltage droops as output current rises. If a severe over current fault is detected, it trips the undervoltage comparator. When configured to use $R_{DS(on)}$ overcurrent sensing, the TPS51116 compensates for thermal shift in the $R_{DS(on)}$ of the MOSFET.

For $R_{DS(on)}$ overcurrent sensing, place a 0-Ω resistor or short at R9 and set the JP2 jumper in the lower position.

4.6 JP2 Resistive Current Sensing

The TPS51116EVM can be configured into a resistive current sense mode. In this mode the TPS51116EVM senses inductor current by the voltage drop across R8. As with the $R_{DS(on)}$ current sensing mode, the TPS51116 limits the output current allowing V_{VDDQ} to droop and trip the undervoltage comparator output.

To program the EVM for resistive current sensing, ensure the 2-W, 6 mΩ resistor is installed in position R8, remove any resistor from the R9 position, and set JP2 to the upper position.

4.7 JP3 D-CAP Control Mode

The TPS51116EVM is preconfigured to operate in TI's D-CAP mode. This adaptive constant on-time semi-hysteretic control scheme combines the benefits of fixed frequency steady-state operation with the fast transient response of hysteretic control and a minimum off time to prevent inductor saturation or 100% duty cycle operation. For more information on D-CAP mode, see *D-CAP Mode and Transient Load Response* section. Electrolytic output capacitors should always be used when operating in D-CAP mode. See Appendix A for more information about D-CAP mode.

To program the EVM for D-CAP control mode, set JP3 into the upper position.

4.8 JP3 Current Mode Control

The TPS51116EVM can be configured to operate in a more conventional current mode control. In this mode, the transconductance amplifier's output is connected to the compensation network.

To program the EVM for current mode control, set JP3 into the lower position.

4.9 JP4 DDR Mode

The TPS51116EVM can be configured to operate in DDR mode, setting the switching regulator output voltage (V_{VDDQ}) to 2.5 V and the LDO termination voltage (V_{VTT}) to 1.25 V.

To program the EVM for DDR mode, place the JP4 jumper in the center vertical position.

4.10 JP4 DDR2 Mode

The TPS51116EVM comes preconfigured in DDR2 mode, setting the switching regulator output voltage (V_{VDDQ}) to 1.8 V and the LDO termination voltage (V_{VTT}) to 0.9 V.

To program the EVM for DDR2 mode, place the JP4 jumper in the right horizontal position.

4.11 JP4 DDR3 or Adjustable Output Voltage

The TPS51116EVM can be configured to operate in DDR3 or adjustable output mode, allowing the user to set V_{VDDQ} between 1.5 V and 3.0 V by selecting the R10 and R11 voltage divider and using the internal 750-mV reference. The V_{VTT} output voltage tracks at of this adjustable voltage. The default values for R10 and R11 provide DDR3 voltage levels. These set the switching regulator voltage (V_{VDDQ}) to 1.5 V and the LDO termination voltage (V_{VTT}) to 0.75 V.

To program the EVM for adjustable output voltage mode, place the JP4 jumper in the left horizontal position.

Table 3. Adjustable Output Voltage Resistor Values(1)

V_{VDDQ} (V)	V_{VTT} (V)	R10 (kΩ)	R11 (kΩ)
3.0	1.50	14.3	4.75
2.7	1.35	12.4	4.75
2.0	1.00	8.06	4.75

(1) For adjustable output voltage mode, place the JP4 jumper in the left horizontal position.

4.12 Self-Driven LDO Supply Voltage

The TPS51116EVM comes preconfigured in self-driven LDO supply voltage mode. In this mode, the LDO is supplied directly from the V_{VDDQ} switching regulator's output, eliminating the need for an external supply voltage.

To program the EVM for self-driven LDO supply voltage, place a short in the R1 position.

4.13 External LDO Supply Voltage

The TPS51116EVM can be configured in an external LDO supply voltage mode. In this mode the LDO is supplied by an external voltage source not produced by the TPS51116, allowing the user to select another power rail to provide power to the VLDOIN by removing the 0-Ω resistor from the R1 position and applying an external supply to the LDOIN_EX pin (J1) on the EVM board.

5 Test Set-Up

Figure 3 shows the basic test set up recommended to evaluate the TPS51116EVM. Please note that although all grounds are common, their connections should remain separate as noted in Figure 3.

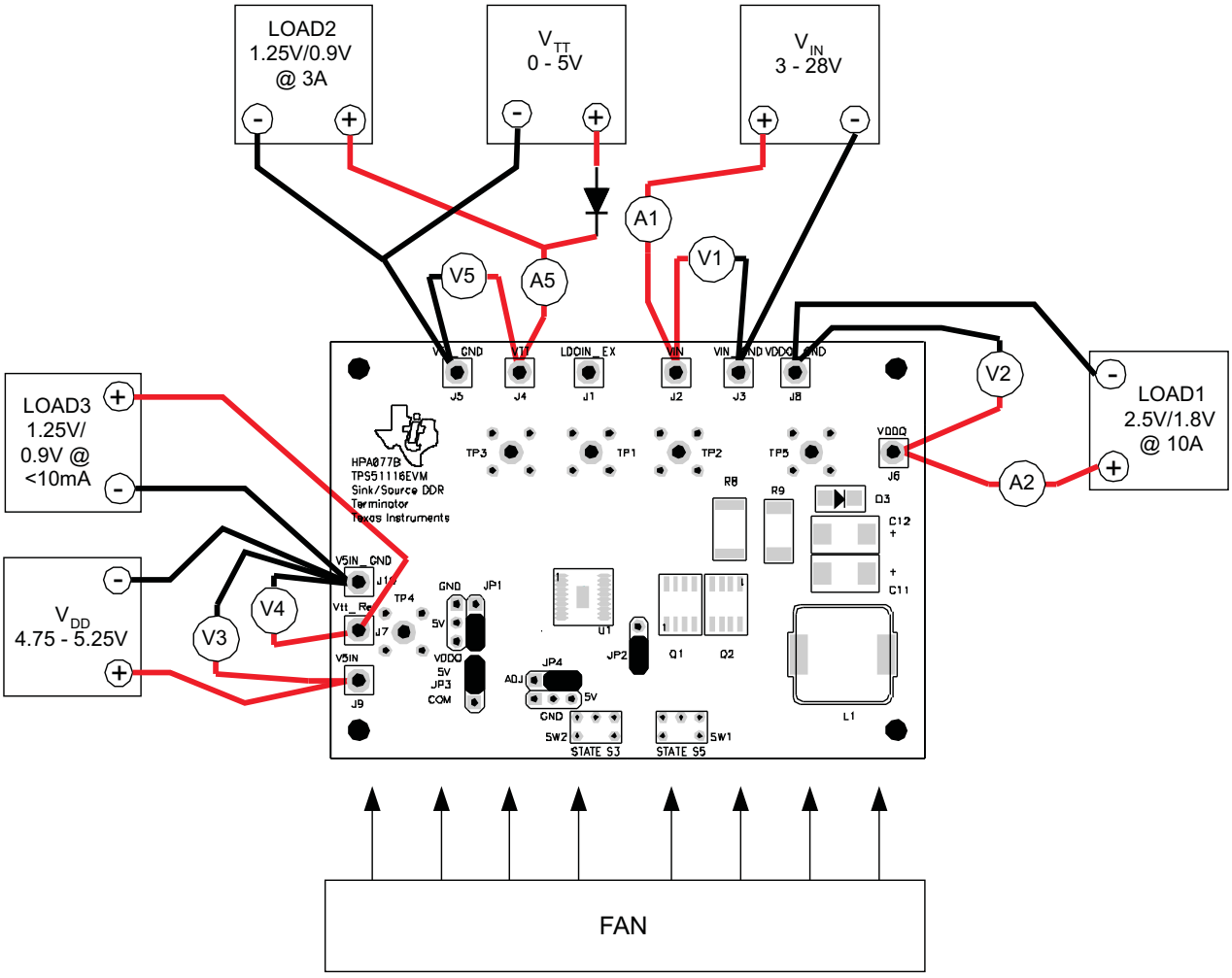


Figure 3. TPS51116EVM Test and Evaluation Setup

5.1 DC Power Source (V_{IN})

V_{IN} should be a DC voltage source capable of delivering between 0 VDC and 30 VDC and between 0 A and 10A with a power handling capability of at least 35 W. V_{IN} should be connected between pins VIN and VIN_GND. V_{IN} supplies power to the switching regulator.

5.2 5-V DC Power Source (V_{DD})

V_{DD} should be a DC voltage source capable of delivering 5 V at 500 mA with a power handling capability of at least 2.5 W. V_{DD} should be connected between pins V5IN and V5IN_GND. VDD supplies the TPS51116 operating current, powers the S3 and S5 sleep state switches and the JP1 through JP4 configuration jumpers.

5.3 Termination Voltage Source (V_{TT})

V_{TT} source is used to test the sink capability of the VTT LDO. V_{TT} must be able to source 3 A of current at 5 V. A diode should be placed in series with V_{TT} to prevent current from flowing into V_{TT}. V_{TT} should be connected between pins Vtt and Vtt_GND. V_{TT} and LOAD3 should never be powered on at the same time.

5.4 Core Voltage Load (LOAD1)

LOAD1 should be an electronic load set in constant current mode capable of sinking between 0 A and 10A at 2.5 V (DDR Mode) or 1.8 V (DDR2 Mode). LOAD1 should be connected between pins VDDQ and VDDQ_GND.

5.5 Termination Voltage Load (LOAD2)

LOAD2 should be an electronic load set in constant current mode capable of sinking between 0 A and 3 A of current at 1.25 V (DDR Mode) or 0.9 V (DDR2 Mode). LOAD2 should be connected between pins Vtt and Vtt_GND. LOAD2 and V_{TT} should never be powered on at the same time.

5.6 Memory Cell Reference Voltage Load (LOAD3)

LOAD3 should be an electronic or resistive load sinking less than 10 mA from the V_{VTTREF} of 1.25 V (DDR Mode) or 0.9 V (DDR2 Mode). LOAD3 should be connected between pins Vtt_Ref and V5IN_GND.

5.7 Fan

This converter includes components that can get hot to the touch. Because this EVM is not enclosed to allow probing of circuit nodes, a small fan capable of between 200 LFM and 400 LFM is recommended to reduce component temperatures when operating the evaluation module.

6 Power-Up/Power-Down Test Procedures

The following test procedure is recommended primarily for powering up and shutting down the EVM. Whenever the EVM is running the fan should be turned on. Also, never walk away from a powered EVM for extended periods of time.

1. Working at an ESD workstation, make sure that any wrist straps, boot straps or mats are connected referencing the user to earth ground before power is applied to the EVM. Electrostatic smock and safety glasses should also be worn.
2. Connect power supplies, loads, voltage meters and current meters as shown in Figure 3
3. Set 100-mil shunt jumpers as described in the *User Configuration Jumper Settings* for desired operational configuration. (***Note: Do not attempt to change jumper settings during operation***)
4. Ensure S3 and S5 are set to the S4/S5 state to ensure the outputs initially disabled before applying the input voltage. See Figure 2 for details.
5. Increase V_{DD} from 0 VDC to 5 VDC. Using V3, verify V_{DD} voltage between 4.75 V and 5.25 V.
6. Increase V_{IN} from 0 VDCto 12 VDC. Using V1, verify V_{IN} voltage between 11 V and 13 V.
7. Switch S3 and S5 to the S0 state to enable the outputs. See Figure 2 for details.
8. Vary LOAD1 from 0 ADC to 10 ADC.
9. Ensure that V_{TT} is off before starting LOAD2.
10. Vary LOAD2 from 0 A to 3 A (0 A to -3A on meter A5) to test LDO source capability.
11. Set LOAD2 to 0 A before turning on V_{TT}.
12. Vary V_{TT} to obtain A5 between 0 A to +3 A. to test LDO sink capability. (Note: Running both V_{TT} and LOAD2 at the same time causes V_{TT} to source additional current through LOAD2. A5 reads the summation of the LOAD2 current and LDO sink current)
13. Vary LOAD3 from 0 mA to 10mA. (Note: Do not exceed 10 mA on LOAD3)
14. Vary V_{IN} from 4.5 V to 28 V.
15. Vary V_{DD} from 4.75 V to 5.25 V.
16. Use state S3 and state S5 switches to test sleep states.
17. Increase V_{IN} to 12 VDC
18. Decrease LOAD3 to 0 mA.
19. Decrease LOAD2 to 0 A.
20. Decrease LOAD3 to 0 A.
21. Decrease V_{IN} to 0 V.
22. Decrease V_{DD} to 0V.

7 Performance Data and Characteristic Curves

The TPS51116EVM is design to provide high efficiency over a very wide range of load currents from maximum load of 10 A down to very light loads less than 100 mA. It is important to achieve high efficiency at very light loads because memory modules consume very little current when waiting for instructions in an idle state.

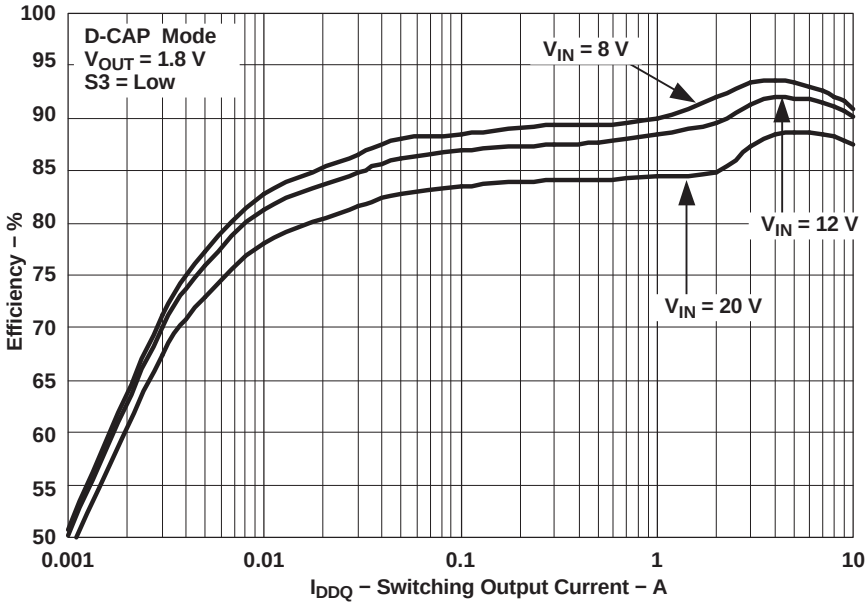


Figure 4. TPS51116EVM Efficiency

The efficiency of the TPS51116EVM is shown in Figure 4. At less than 2-A of load current the TPS51116 is operating in PFM mode as the low-side MOSFET is turned off when inductor current reaches zero to prevent sinking current from the output capacitor. Because the semi-hysteretic valley comparator threshold does not change, output ripple voltage does not increase while in PFM mode. In addition to requiring very good light load efficiency, memory module power supplies must have very good transient responses. As the module goes from idle state to computational state, they may go from very light load to full load and back again in a very short period of time. In order to achieve this fast transient response without requiring large bulk output capacitance, the TPS51116EVM used the TI's D-CAP control mode discussed in detail in the Appendix. In D-CAP mode, the TPS51116EVM is able to immediately respond to a load transient, going from nominal duty cycle to maximum duty cycle in a single switching cycle and return to nominal duty cycle as soon as the output voltage has returned to its regulated value.

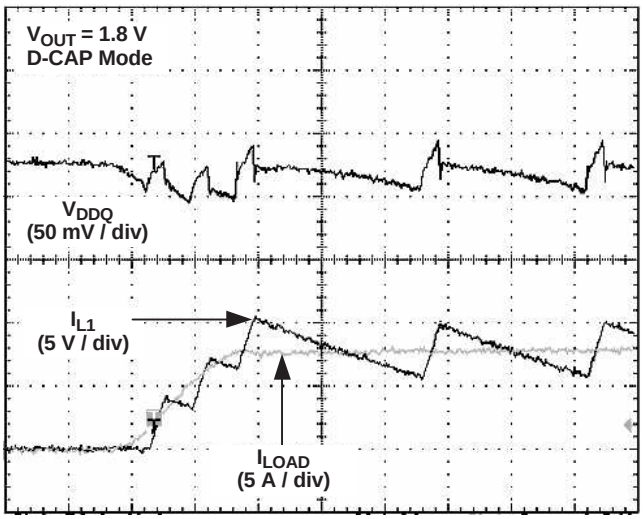


Figure 5. TPS51116EVM 0-A to 8-A Load Transient Response

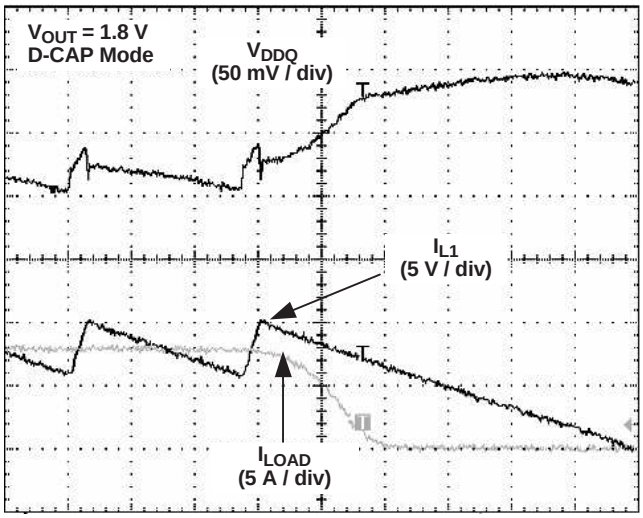


Figure 6. TPS51116EVM - 8-A to 0-A Load Transient Response

Figure 5 shows the switching output ripple voltage, the inductor current and the output load current. The advantage of the semi-hysteretic D-CAP mode is clearly visible. Here an 8-A load transient of 5 A/s causes less than 30 mV of voltage drop and nominal operation is recovered in less than 2 s, that's a single switching cycle at the normal 400 kHz switching frequency.

Figure 6, with the same channel designations of Figure 5 shows the falling transient. As soon as the first main switching pulse is terminated normally, the TPS51116EVM turns on the lowside FET and immediately begins dropping the inductor current as fast as possible by shorting the switch node to ground. The low-side MOSFET is then turned OFF when the inductor current reaches zero and the high-side MOSFET is held off until the output voltage drops below the valley comparator and nominal operation is immediately restored.

8 EVM Assembly Drawing and Layout

TPS51116 is built on a 4-layer copper clad FR4 PCB 2.25” x 3.2” and 0.062 thick with all components on a single side. Figure 7 through Figure 11 detail the PCB assembly, silk screen and copper layers for TPS51116EVM. These figures are provided for reference and evaluation purposes only.

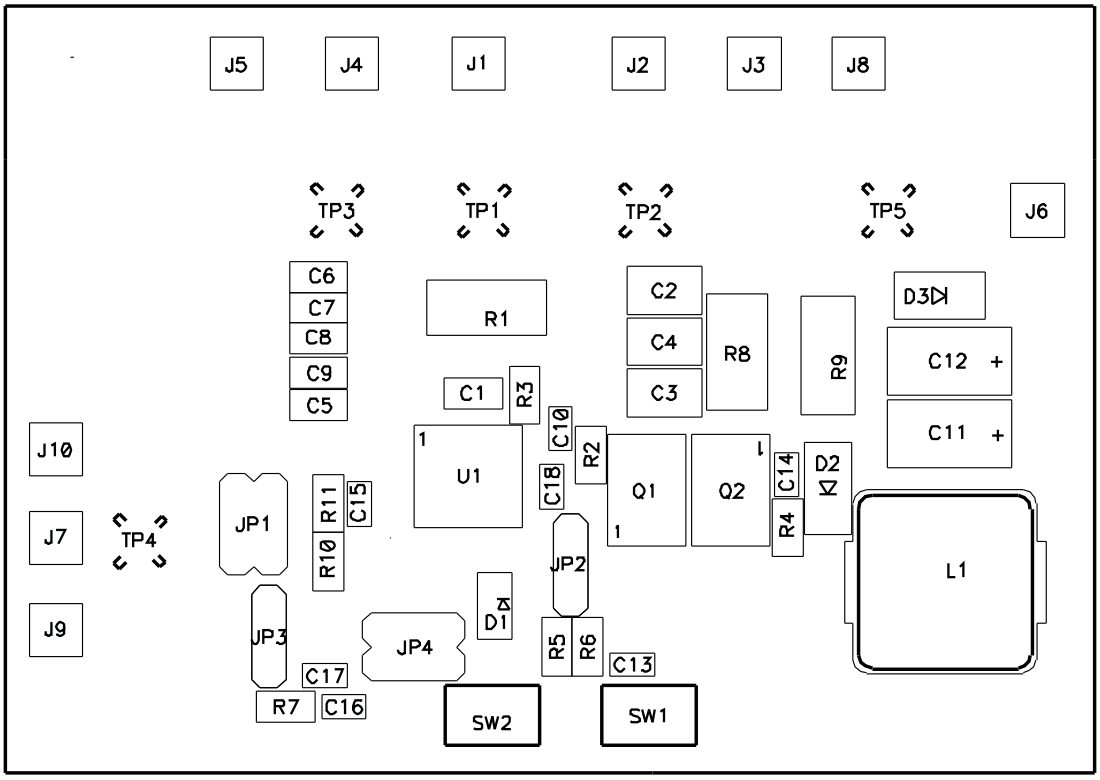


Figure 7. Component Outlines

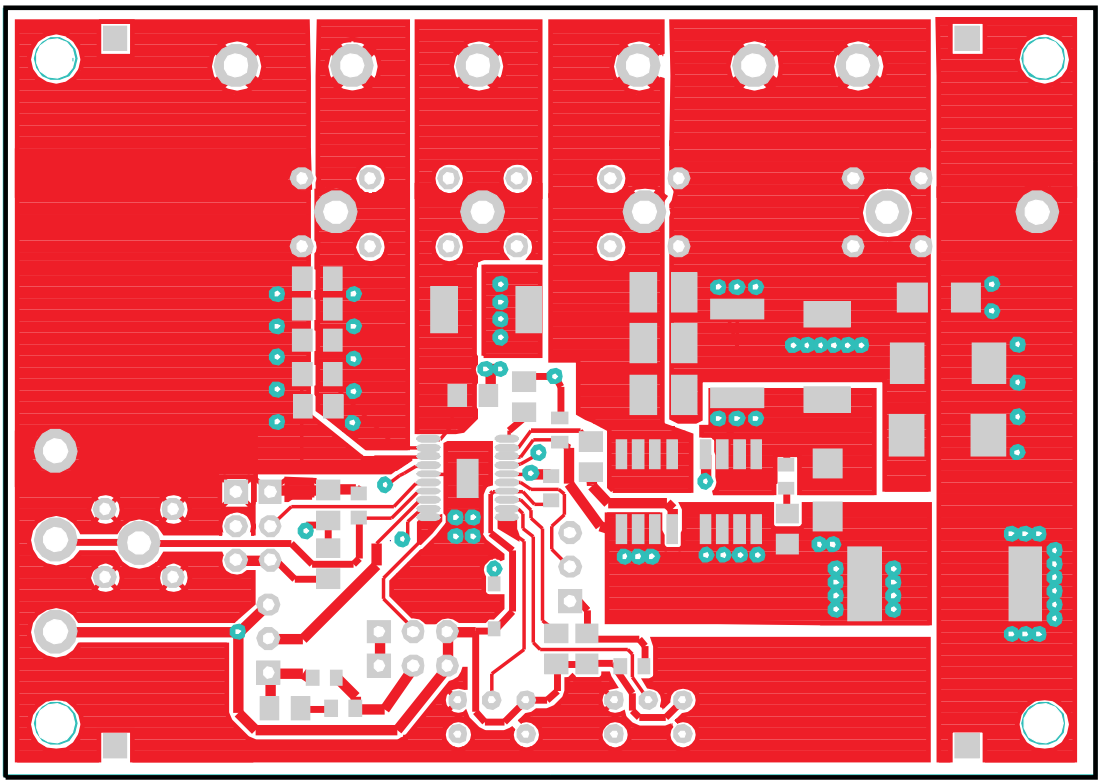


Figure 8. Top Copper Layer (Top View)

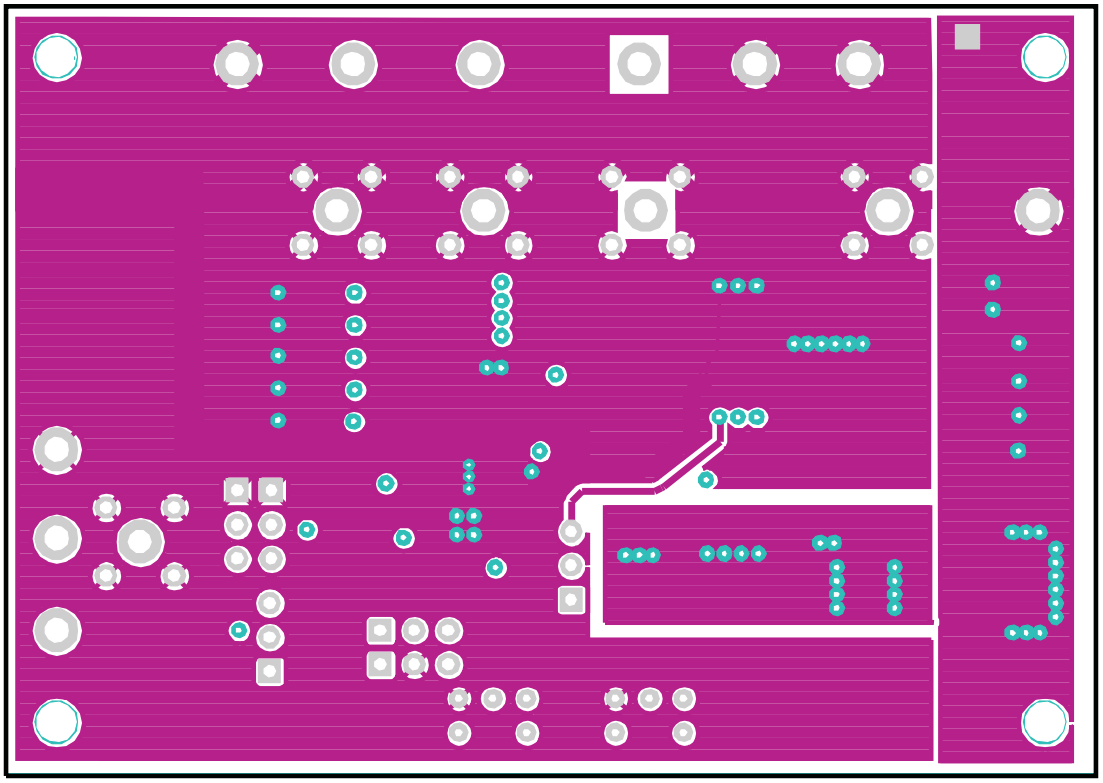


Figure 9. Internal Layer 1 (Top View)

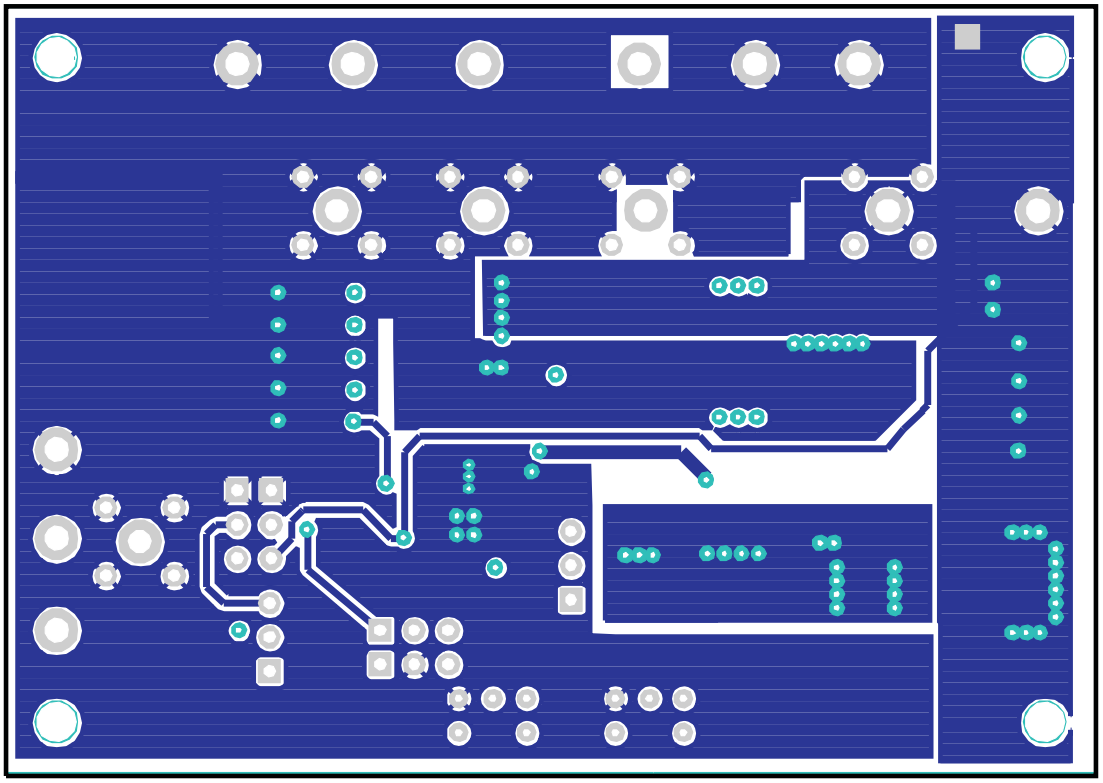


Figure 10. Internal Layer 2 (Top View)

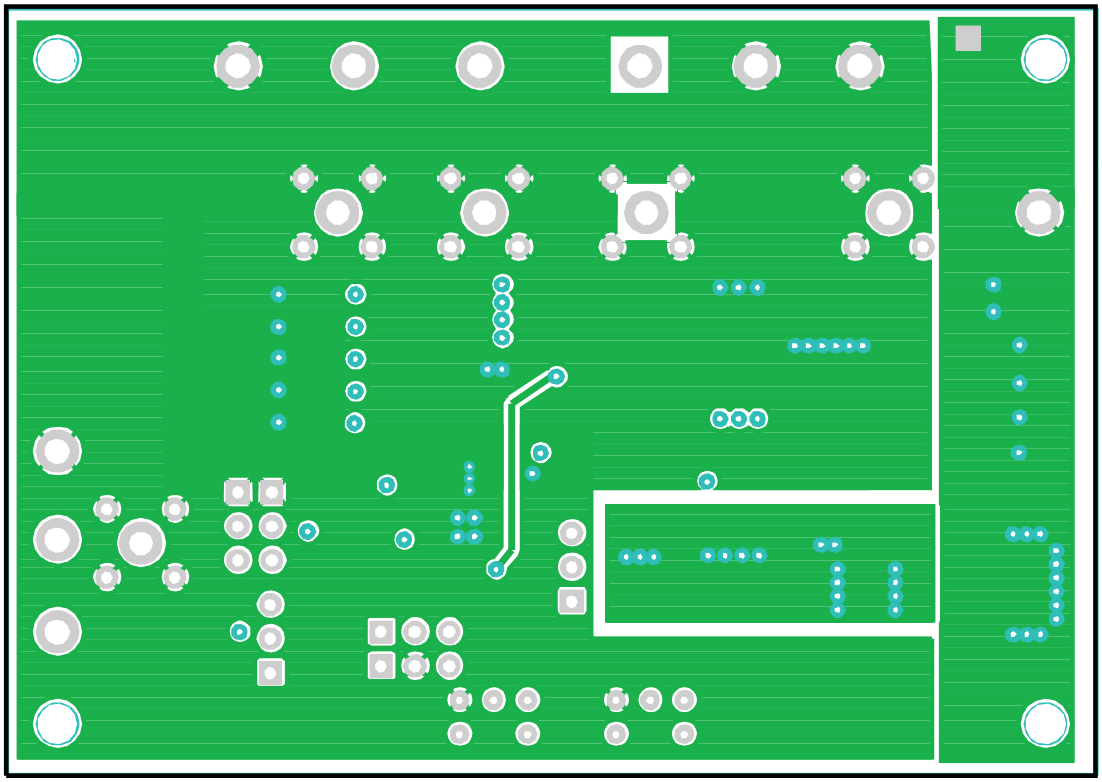


Figure 11. Bottom Copper (Top View)

9 List of Materials

Table 4. List of Materials

QTY	REFERNCE DESIGNATOR	DESCRIPTION	SIZE	MRF	PART NUMBER
2	C3, C4	Capacitor, ceramic, 10 µF, 25 V, X5R, 20%	1210	Vishay	C3225X5R1E106M
3	C1, C6, C7	Capacitor, ceramic, 10 µF, 6.3 V, X5R, 10%	805	TDK	C2012X5R0J106K
1	C10	Capacitor, ceramic, 0.10 µF, 50 V, X75, 10%	603	Standard	Standard
2	C11, C12	Capacitor, POSCAP, 150 µF, 4 V, 45 mΩ, 20%	7343(D)	Sanyo	4TPC150M
2	C13, C14	Capacitor, ceramic, 1.0 nF, 50 V, X7R, 10%	603	Standard	Standard
1	C15	Capacitor, ceramic, 0.033 µF, 50 V, X7R, 10%	603	Standard	Standard
1	C16	Capacitor, ceramic, 0.01 µF, X7R, 50 V, 20%	603	Standard	Standard
1	C18	Capacitor, ceramic, 4.7 µF, 6.3 V, X5R, 10%	603	TDK	C1608X5R0J475K
1	L1	Inductor, SMT, 1.0 µH, 29 A, 2.3 mΩ	0.51 ɔ0.51	Vishay	IHLP5050-01
1	Q1	MOSFET, N-channel, 30 V, 11 A, 9.1 mΩ	SO-8	Int'l Rectifier	IRF7821
1	Q2	MOSFET, N-channel, 30 V, 16-A, 4.0 mΩ	SO-8	Int'l Rectifier	IRF7832
2	R1, R9	Resistor, chip, 0 Ω, 1 W, 1%	1225	TYEE	Standard
1	R2	Resistor, chip, 5.11 Ω, 1/10 W, 1%	805	Standard	Standard
1	R3	Resistor, chip, 0 Ω, 1/10 W, 1%	805	Standard	Standard
1	R4	Resistor, chip, 3.09 Ω, 1/10 W, 1%	805	Standard	Standard
1	R5	Resistor, chip, 100 kΩ, 1/10 W, 1%	805	Standard	Standard
1	R6	Resistor, chip, 7.15 kΩ, 1/10 W, 1%	805	Standard	Standard
1	R7	Resistor, chip, 20.0 kΩ, 1/10 W, 1%	805	Standard	Standard
1	R8	Resistor, current sense, 0.006 Ω	2512	Standard	Standard
2	R11, R10	Resistor, chip, 4.75 kΩ, 1/10 W, 1%	805	Standard	Standard
1	U1	High-Voltage Synchronous Switcher with VTT Regulator	PWP-20	Texas Instruments	TPS51116PWP

Appendix A

A.1 D-CAP Mode and Transient Response

TI's adaptive constant ON-time semi-hysteretic control scheme or D-CAP technology uses V_{IN} and V_{OUT} to determine an ON-time. After this ON-time, the controller waits a minimum off time, then detects a valley in the output voltage, and turns back on after the output voltage has dropped below a threshold voltage. By using a variant of voltage feed-forward, the constant ON-time is adapted to maintain a near constant switching frequency during steady state operation, but allows for the advantages of hysteretic control during a load transient.

Turning a positive load transient, the output voltage drops below the threshold and the OFF-time comparator reacts as soon as the minimum OFF-time has elapsed, increasing the switching frequency and immediately driving the output to its maximum duty cycle. Once the output has charged above the valley threshold, the OFF-time is again set by the decay of the output voltage. Since there is no compensation capacitor to charge or discharge, the TPS51116 is able to immediately react to load transient without recovery ringing. (See Figure 5 and Figure 6).

In Figure 5, a 0 A to 8 A load transient with the output voltage and the inductor ripple current. On the positive transient edge, the TPS51116 has reacted to the 8-A transient load and returned to steady state operation within 2 ms. Despite the transient, there has been less than 50 mV of overshoot and no ringing on the output. On the negative transient edge (as shown in Figure 6), the synchronous MOSFET has been turned on within one switching cycle and held on until the output voltage recovers from the output transient, at which point it immediately recovers its steady state operation since the ON-time is fixed by the input to output voltage ratio and is not a function of the voltage across a compensation capacitor. This allows the TPS51116 to react to sever load transients extremely quickly, allowing the use of less bulk capacitance while maintaining tighter control of the sensitive output voltage.

It is important to note that the D-CAP mode depends on the output voltage relating directly to the inductor current. This dictates that at the switching frequency, approximately 400 kHz during steady state operation, the output capacitors should approximate a resistive load. Ceramic and ultra-low ESR capacitors can impose a significant phase shift and interfere with D-CAP mode operation. Thus, it is not recommended that one use ceramic capacitors when operating in D-CAP mode.

FCC Warning

This evaluation board/kit is intended for use for **ENGINEERING DEVELOPMENT, DEMONSTRATION, OR EVALUATION PURPOSES ONLY** and is not considered by TI to be a finished end-product fit for general customer use. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

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Should this evaluation board/kit not meet the specifications indicated in the User's Guide, the board/kit may be returned within 30 days from the date of delivery for a full refund. THE FOREGOING WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE.

The user assumes all responsibility and liability for proper and safe handling of the goods. Further, the user indemnifies TI from all claims arising from the handling or use of the goods. Due to the open construction of the product, it is the user's responsibility to take any and all appropriate precautions with regard to electrostatic discharge.

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 4.75 V to 5.25 V and 3 V to 28 V and the output voltage range of 1.5 V to 3.4 V and 0.75 V to 1.70 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 60°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

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   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

WARNING

Evaluation Kits are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.

User shall operate the Evaluation Kit within TI’s recommended guidelines and any applicable legal or environmental requirements as well as reasonable and customary safeguards. Failure to set up and/or operate the Evaluation Kit within TI’s recommended guidelines may result in personal injury or death or property damage. Proper set up entails following TI’s instructions for electrical ratings of interface circuits such as input, output and electrical loads.

NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGREDATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 *Regulatory Notices:*

3.1 *United States*

3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

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4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

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10. *Governing Law:* These terms and conditions shall be governed by and interpreted in accordance with the laws of the State of Texas, without reference to conflict-of-laws principles. User agrees that non-exclusive jurisdiction for any dispute arising out of or relating to these terms and conditions lies within courts located in the State of Texas and consents to venue in Dallas County, Texas. Notwithstanding the foregoing, any judgment may be enforced in any United States or foreign court, and TI may seek injunctive relief in any United States or foreign court.

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