TEXAS INSTRUMENTS

TPS40007-Based Converter Delivers 10-A Output

User's Guide

DYNAMIC WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 0 V_{DC} to 5.5 V_{DC}.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 50°C. The EVM is designed to operate properly with certain components above 50°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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TEXAS
INSTRUMENTS

TPS40007-Based Converter Delivers 10-A Output

Mark Dennis   *DC to DC Controller Products*

Contents

1   Introduction

The TPS40007 is a voltage-mode, synchronous buck PWM controller that uses TI's proprietary Predictive Gate Drive™ technology to wring maximum efficiency from step-down converters. This controller provides a bootstrap circuit to allow the use of an N-channel MOSFET as the topside buck switch to reduce conduction losses and increase silicon device utilization. Predictive Gate Drive™ technology controls the delay from main switch turn-off to synchronous rectifier turn-on and also the delay from rectifier turn-off to main switch turn-on. This allows minimization of the losses in the MOSFET body diodes, both conduction and reverse recovery. This design note provides details on a buck converter that converts an input of 3 V to 5 V down to a 2.5-V output level using the TPS40007 controller.

A schematic for the board is shown in Figure 1. The list of material is provided in section 7 of this User's Guide.

2   Features

The specification for this board is as follows:

- V_{IN} = 3.3 V to 5 V
- V_{OUT} = 2.5 V +/–3%
- I_{OUT} = 0 A to 10 A
- Efficiency = > 95% with V_{IN} = 3.3 V, I_{LOAD} = 4 A
- Output voltage ripple < 2% V_{OUT}
- Power semiconductor devices: Each MOSFET is a single SO-8 package

3   Schematic
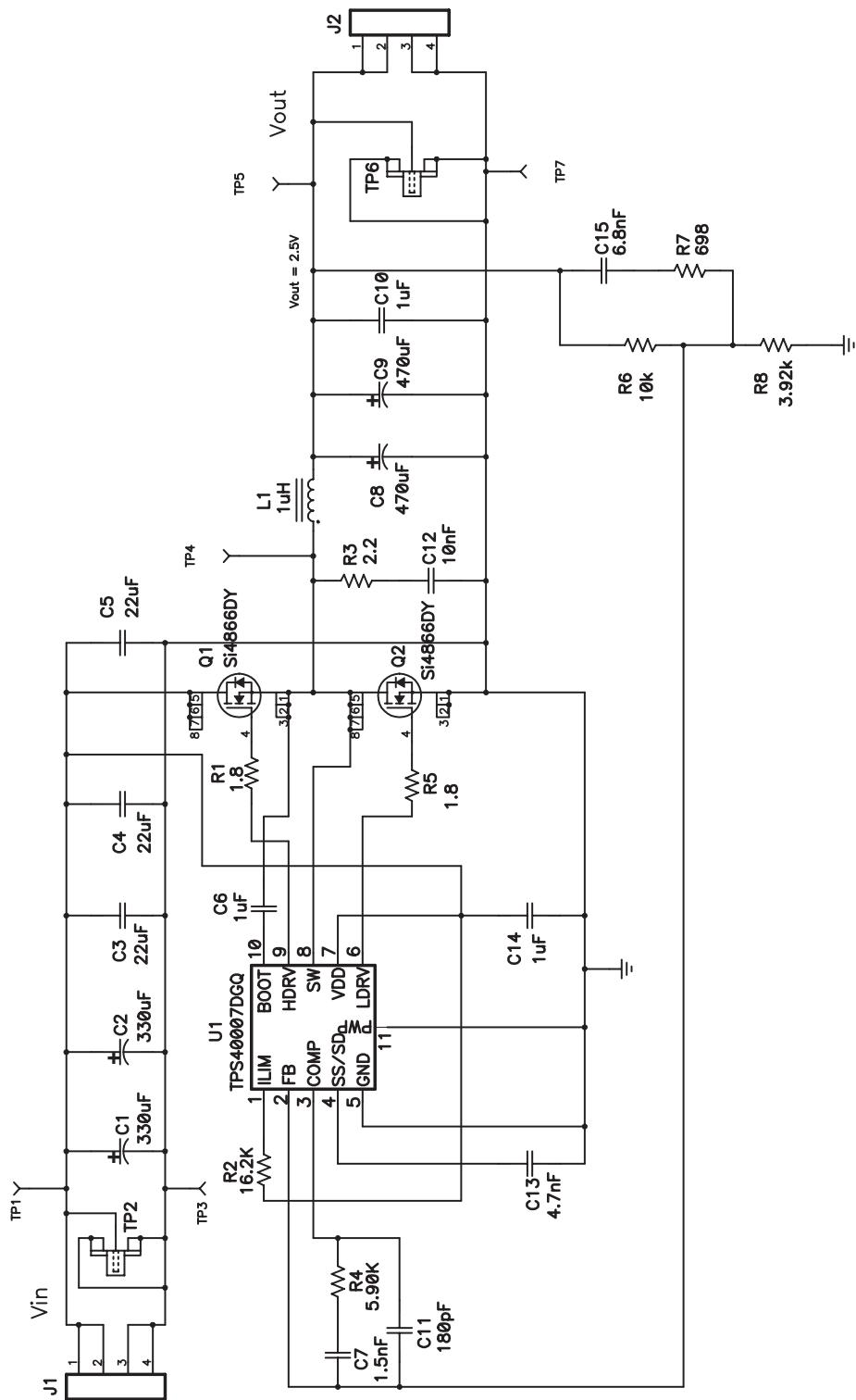
Figure 1. Application Diagram for the TPS40007EVM–001

4 Design Procedure

4.1 Controller Selection

The TPS40007 synchronous buck controller is selected for this high-current application because the 300-kHz switching frequency enables higher efficiency. The TPS40009 is available for applications needing 600-kHz operation for reducing component size. However, at higher frequency the efficiency is generally reduced, leading to more on-board power dissipation.

4.2 Inductance Value

The output inductor value is selected to set the ripple current to a value most suited to overall circuit functionality. An inductor selection that is too small leads to larger ripple current that increases RMS current losses in the inductor and MOSFETs, and also leads to more ripple voltage on the output. The inductor value is calculated by equation (1),

$$L_{MIN} = \frac{V_{OUT}}{f \times I_{RIPPLE}} \left(1 - \frac{V_{OUT}}{V_{IN(max)}}\right) = \frac{2.5\ V}{300\ kHz \times 4\ A} \times \left(1 - \frac{2.5\ V}{5\ V}\right) = 1.0\ \mu H \tag{1}$$

in which I_{RIPPLE} is chosen to be 40% of I_{OUT}, or 4 A at max V_{IN}. This high value of ripple current is selected to keep the inductor small to minimize the $R_{DS(on)}$ losses due to the high output current. A synchronous rectifier controller that maintains continuous inductor current down to no load eliminates concerns arising from crossing the DCM boundary. A standard value of 1 μH with a resistance of 3.5 mΩ is selected. At full load the power loss is only 0.35 W, which is only 1.4% of the 25-W output power.

4.3 Input Capacitor Selection

Bulk input capacitor selection is based on allowable input voltage ripple and required RMS current carrying capability. In typical buck converter applications, the converter is fed from an upstream power converter with its own output capacitance. In this standalone supply, onboard capacitance is added to handle input voltage ripple and RMS current considerations. For this power level, input voltage ripple of 150 mV is reasonable, and a conservative minimum value of capacitance is calculated as

$$C = \frac{I \times \Delta t}{\Delta V} = \frac{10\ A \times 2.5\ \mu s}{0.15\ V} = 167\ \mu F \tag{2}$$

In addition to this minimum capacitance requirement, the RMS current stresses must be considered. In this converter, the large duty cycle causes the input RMS current to be nearly as large as the output current. This simplified formula calculates the RMS current for a trapazoidal current waveform, shown in equation (3).

$$I_{RMS} = I \times \sqrt{D} = I \times \sqrt{\frac{V_{OUT}}{V_{IN(min)}}} = 10\ A \times \sqrt{\frac{2.5\ V}{3.0\ V}} = 9.1\ A \tag{3}$$

Additional terms for the ripple component of the current add only a small amount to the total RMS current, and can be neglected. To meet this initial requirement with small size and cost, a combination of capacitors is considered. To carry the high frequency ripple current, three 22-μF, X5R ceramic capacitors are placed close to the power circuitry. Although these capacitors have an extremely small resistance, the datasheet indicates that the part undergoes a 30°C temperature rise with 2 A_{RMS} current at 500 kHz, so more current capability is needed. Two 330-μF POSCAPs with an RMS current capability of 4.4 A each is selected. In typical embedded converters, these POSCAPs is not required if the upstream converter feeding this buck has sufficient current handling capability.

4.4 Output Capacitor Selection

Selection of the output capacitor is based on many application variables, including function, cost, size, and availability. First, the minimum allowable output capacitance should be determined by the amount of inductor ripple current and one-half the allowable output ripple, as given in equation (4).

$$C_{OUT(min)} = \frac{I_{RIPPLE}}{8 \times f \times V_{RIPPLE}} = \frac{4 \text{ A}}{8 \times 300 \text{ kHz} \times 25 \text{ mV}} = 67 \text{ } \mu F \tag{4}$$

This only affects the capacitive component of the ripple voltage. In addition, the voltage component due to the capacitor ESR must be considered, shown in equation (5).

$$ESR_{Cout} \leq \frac{V_{RIPPLE}}{I_{RIPPLE}} = \frac{25 \text{ mV}}{4 \text{ A}} = 6.25 \text{ m}\Omega \tag{5}$$

To minimize capacitor size while maintaining good transient response, two 470-µF POSCAPs (with an ESR of 10 mΩ each) are fitted in paralleled with a 1-µF ceramic capacitor.

4.5 MOSFET Selection

One constraint of this design is the use of one SO-8 MOSFET in the upper switch device and one SO-8 in the lower synchronous rectifier location in the buck converter power stage. The upper device loss is usually dominated by switching loss, so a device with lower gate charge and switching times was selected. Since this application has a relatively high output voltage, the upper device runs at a high duty cycle and needs to have a low $R_{DS(on)}$ to keep conduction losses low, and an 8-mΩ device with a maximum gate charge of 30 nC is selected. The same device is fitted in the bottom switch location to achieve high efficiency.

4.6 Short Circuit Protection

The TPS40003 implements short circuit protection by comparing the voltage across the topside MOSFET while it is on to a voltage dropped from VDD by R_{LIM} due to an internal current source of 15 µA inside pin 1. Due to tolerances in the current source and variations in the power MOSFET on-voltage versus temperature, the short circuit level can protect against gross overcurrent conditions only, and should be set much higher than rated load. In this particular case, R_{LIM} is selected as shown in equation (6).

$$R_{LIM} = R2 = \frac{3 \times I_{OUT} \times R_{DS(on)}}{15 \text{ } \mu A} = \frac{3 \times 10 \text{ A} \times 0.008 \text{ } \Omega}{15 \text{ } \mu A} = 15 \text{ k}\Omega \tag{6}$$

For this design, a standard value of 16.2 kΩ is selected for R2. The factor of 3 in the equation accounts for the variations in component tolerances (both initial and over temperature) and output current ripple. The component tolerances include MOSFET $R_{DS(on)}$, I_{LIM} sink current, and the V_{OS} offset voltage of SW vs I_{LIM}.

4.7 Compensation Design

The TPS40007 uses voltage mode control in conjunction with a high frequency error amplifier. The power circuit L-C double pole corner frequency f_C is located in equation (7).

$$\text{Freq}_{LC} = \frac{1}{2 \times \pi \times \sqrt{L_{OUT} \times C_{OUT}}} = 5.1 \text{ kHz} \tag{7}$$

The output capacitor ESR zero is calculated by equation (8),

$$F_{Z(esr)} = \frac{1}{2 \times \pi \times R_{ESR} \times C_{OUT}} = 33.8 \text{ kHz} \tag{8}$$

where the two POSCAPs ESR of 5 mΩ is used in the calculation because the 1 μF is effectively out of the picture at these relatively low frequencies.

The feedback compensation network is implemented to provide two zeroes and three poles. The first pole is placed near the origin to improve dc regulation.

The first zero is placed below f_C at 2.2 kHz in equation (9).

$$f_{z1} = \frac{1}{2 \times \pi \times (R_6 + R_7) \times C_{15}} \tag{9}$$

The second zero is placed at 18 kHz shown in equation (10).

$$f_{z2} = \frac{1}{2 \times \pi \times R_4 \times C_7} \tag{10}$$

The first pole is placed near the ESR zero frequency in equation (11),

$$f_{p1} = \frac{1}{2 \times \pi \times R_7 \times C_{15}} \tag{11}$$

and the second pole is placed at one-half the switching frequency at 150 kHz to allow a high-speed transient response, shown in equation (12).

$$f_{p2} = \frac{1}{2 \times \pi \times R_4 \times \left(\frac{C_7 \times C_{11}}{C_7 + C_{11}}\right)} \tag{12}$$

Figure 2 is presents the measured loop gain and phase characteristics. At the loop crossover frequency of 20 kHz the phase margin is approximately 50 degrees.

GAIN AND PHASE MARGIN
vs
FREQUENCY
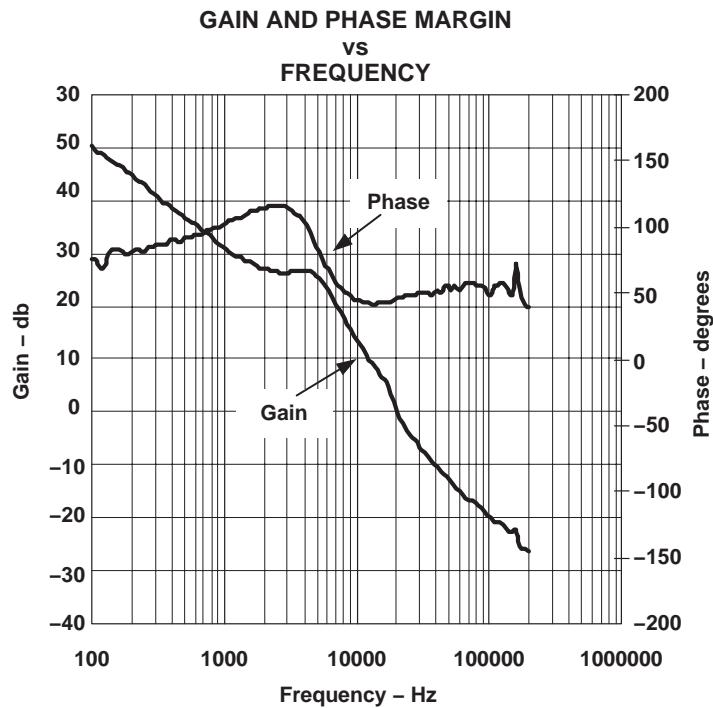
Figure 2.

4.8   Snubber Component Selection

The switch node where Q1 and L1 come together is very noisy. An R-C network fitted between this node and ground can help reduce ringing and voltage overshoot on Q2. This ringing noise should be minimized to prevent it from confusing the control circuitry which is monitoring this node for current limit, Predictive Gate Drive™, and DCM control functions.

As a starting point, the snubber capacitor, C12, is generally chosen to be 5 to 8 times larger than the parasitic capacitance at the node, which is primarily C_{OS} of Q2. Since C_{OS} is around 1600 pF for Q2 at 5 V, C12 is chosen to be 10 nF. R3 is empirically determined to be 2.2 Ω, which minimizes the ringing and overshoot at the switch node. With the relatively low input voltage of 5 V, the power loss, ½ CV^2f, is relatively small at 37 mW.

5   PowerPAD™ Packaging

The TPS4000X family is available in the DGQ version of TI's PowerPAD™ thermally enhanced package. In the PowerPAD™, a thermally conductive epoxy is utilized to attach the integrated circuit die to the leadframe die pad, which is exposed on the bottom of the completed package. The leadframe die pad can be soldered to the PCB using standard solder flow techniques when maximum heat dissipation is required. However, depending on power dissipation requirements, the PowerPAD™ may not need to soldered to the PCB.

The thermally conductive epoxy bonding the circuit die to the leadframe die pad causes a high resistance from the leadframe die pad to the device ground pin 5. When the PowerPad™ package is soldered to the PCB, the leadframe die pad can be connected to ground (pin 5), but this is not required. The leadframe die pad should not be connected to other potentials in the circuit.

The PowerPAD™ package helps to keep the junction temperature rise relatively low even with the power dissipation inherent in the onboard MOSFET drivers. This power loss is proportional to switching frequency, drive voltage, and the gate charge needed to enhance the N-channel MOSFETs. Effective heat removal allows the use of ultra small packaging while maintaining high component reliability.

To effectively remove heat from the PowerPAD™ package, a thermal land should be provided directly underneath the package. This thermal land usually has vias that help to spread heat to internal copper layers and/or the opposite side of the PCB. The vias should not have thermal reliefs that are often used on ground planes, because this reduces the copper area to transfer heat. Additionally, the vias should be small enough so that the holes are effectively plugged when plated. This prevents the solder from wicking away from the connection between the PCB surface and the bottom of the part. A typical footprint pattern is shown in Figure 2, but does not include the additional copper plane which includes the vias above and below the device.
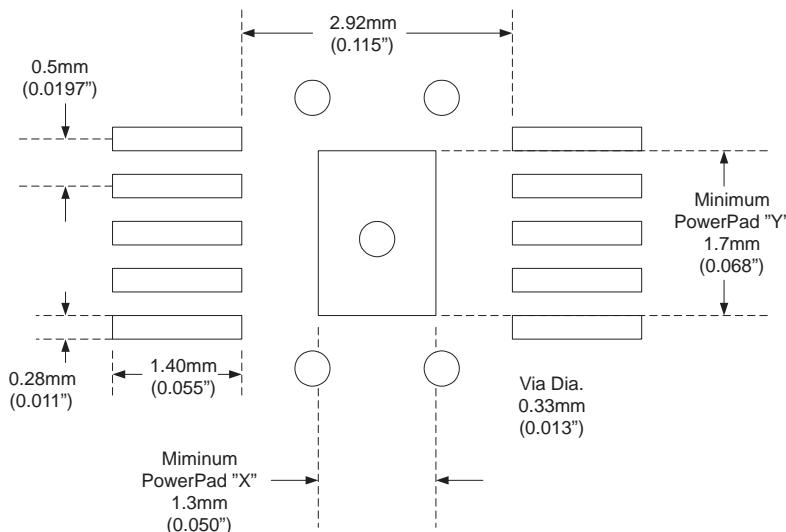
Figure 3. PowerPAD™ PCB Layout Guidelines

The Texas Instrument document, PowerPAD™ Thermally Enhanced Package Application Report (Texas Instrument Literature Number SLMA002) should be consulted for more information on the PowerPAD™ package. This report offers in-depth information on the package, assembly and rework techniques, and illustrative examples of the thermal performance of the PowerPAD™ package.

6 Test Results/Performance Data

6.1 Test Setup
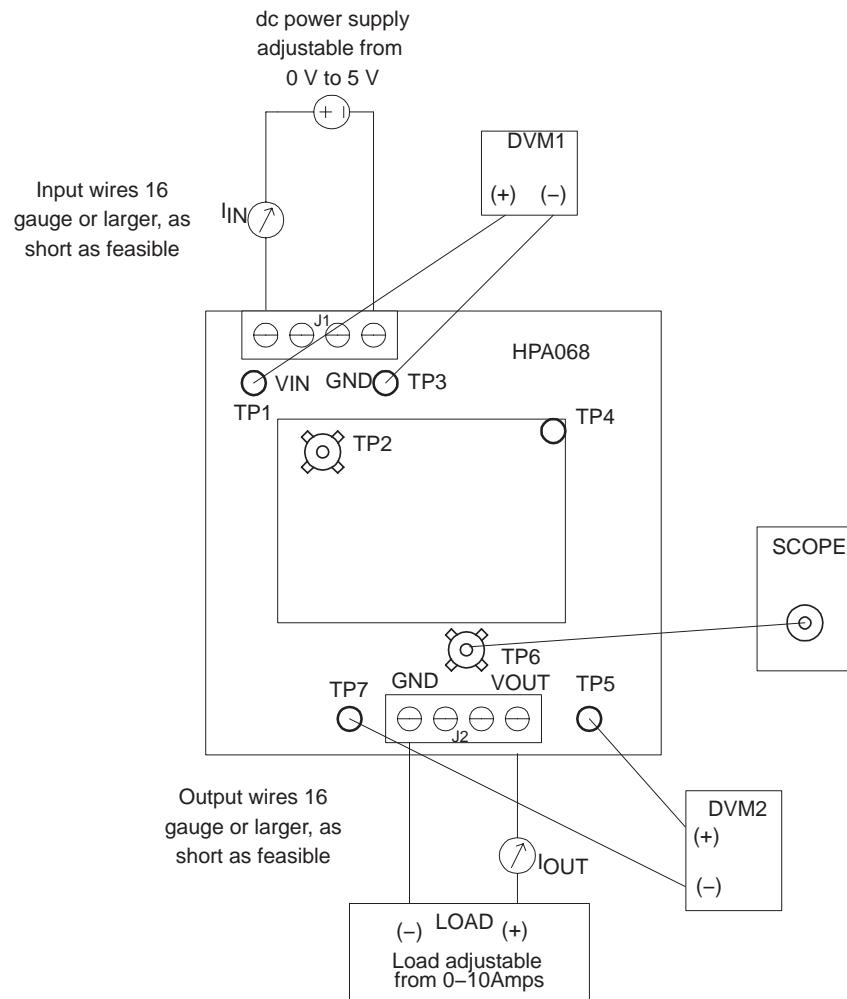
Figure 4. Test Setup

Typical efficiency curves are shown in Figure 5 for 3.3-V input. It should be stressed that measuring high efficiencies requires the utmost care in instrumentation. The power losses are so low that small errors can lead to large variations in measured efficiency. The input and output voltages are measured on the PCB as shown in the test diagram to avoid the losses associated with the input and output connectors.

**EFFICIENCY
vs
OUTPUT CURRENT**
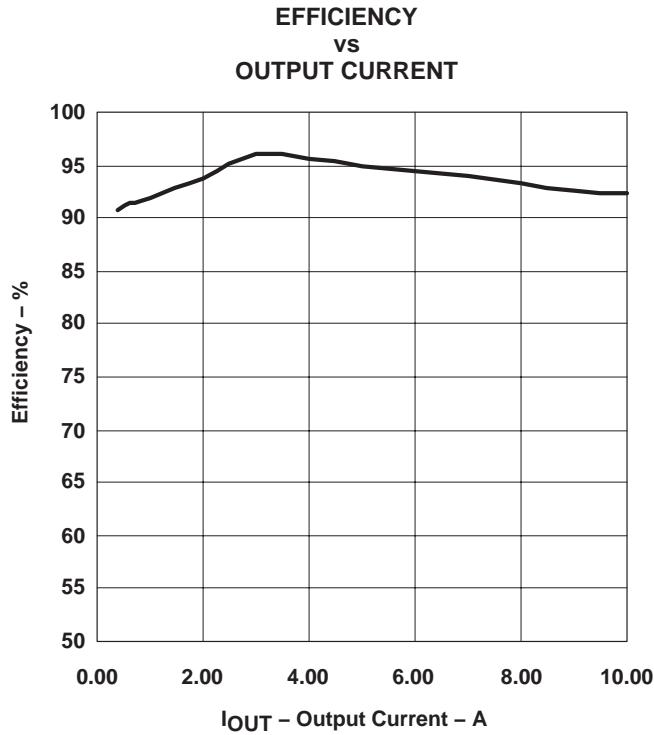
Figure 5.

Figure 6 shows the switch node at V_{IN} = 5 V and I_{OUT} =10 A. As the picture indicates, there is almost negligible body diode conduction using the Predictive Gate Drive™ technique.

TYPICAL SWITCH NODE WAVEFORM

t – Time – 500 ns/div
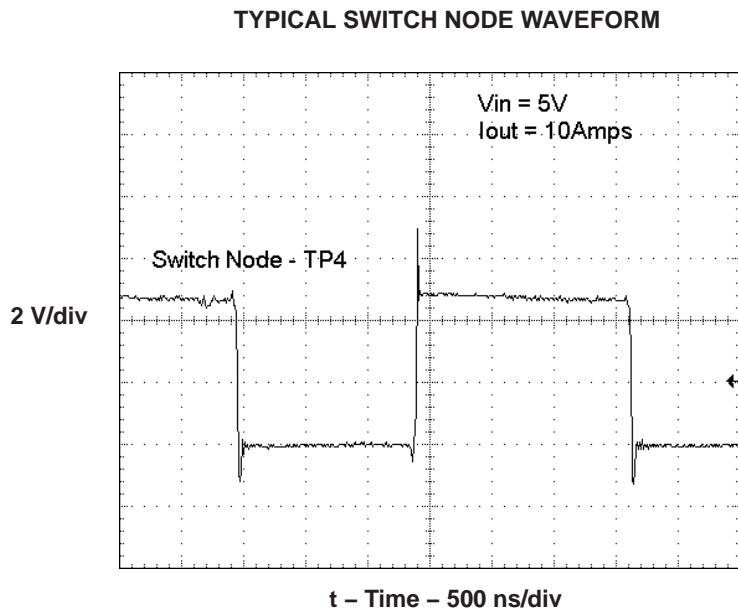
Figure 6.

Figure 7 shows the output voltage ripple at high V_{IN} and full load, which is the worst case condition for output voltage ripple.

OUTPUT VOLTAGE RIPPLE

Vout @ 10mV/div
Iout = 10Amps
Vin = 5V

10 mV/div

t – Time – 1 μs/div
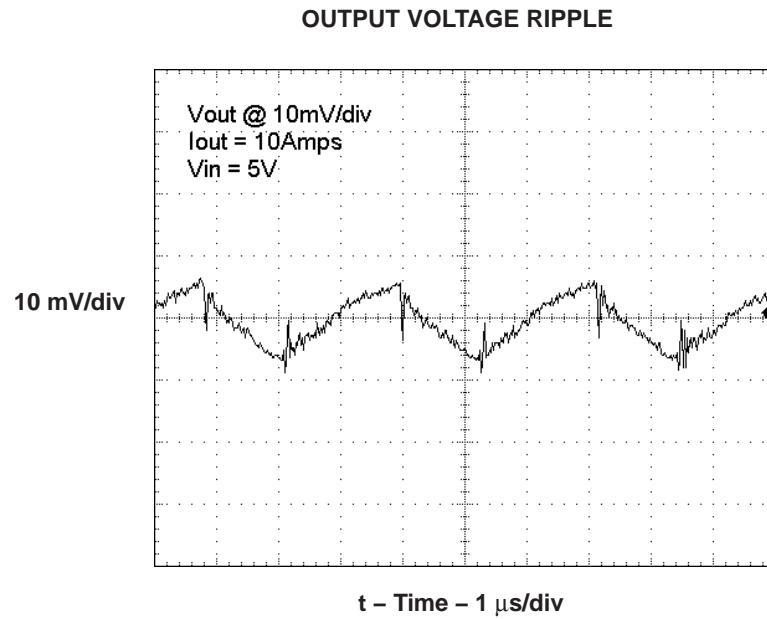
Figure 7.

Figure 8 shows the transient response with a 50% load step from 2.5 A to 7.5 A.

TRANSIENT RESPONSE

Vout @ 50mV/div

50 mV/div

Iout @ 5A/div

t – Time – 20 μs/div
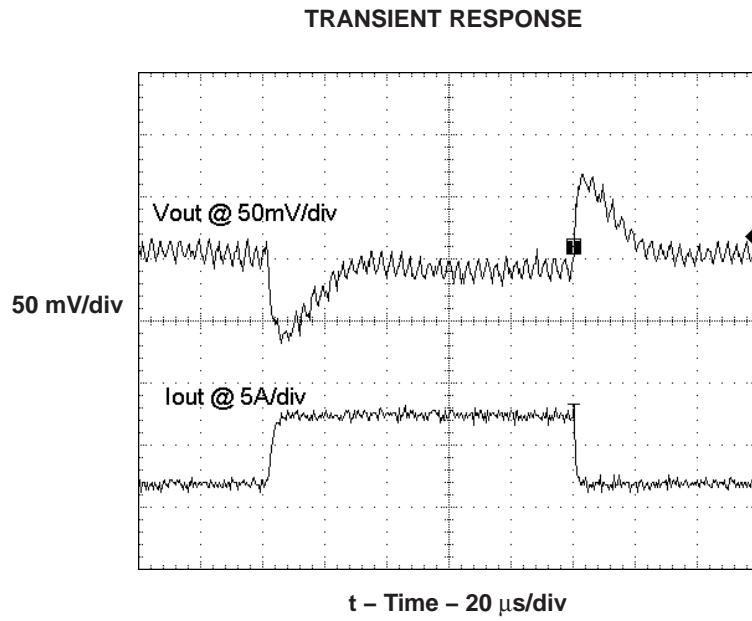
Figure 8.

7   PCB Layout

The PCB top assembly and copper layers are shown in Figures 9 through 11.
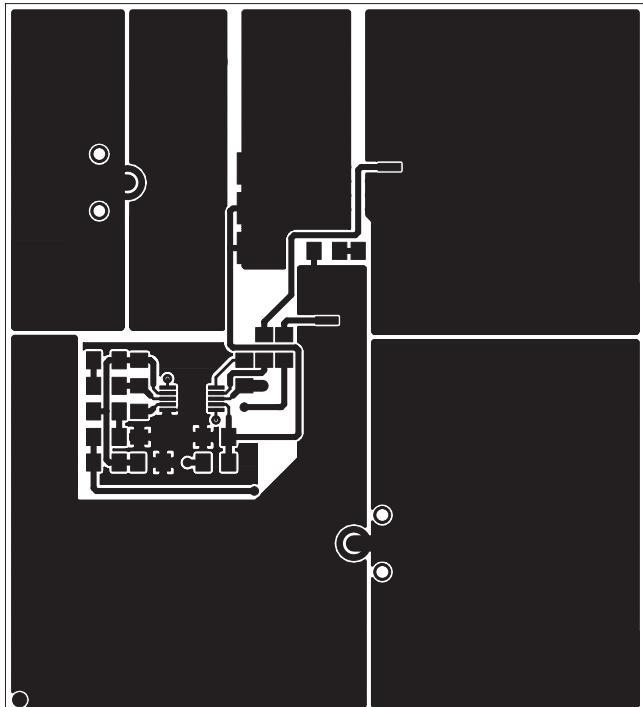
Figure 9
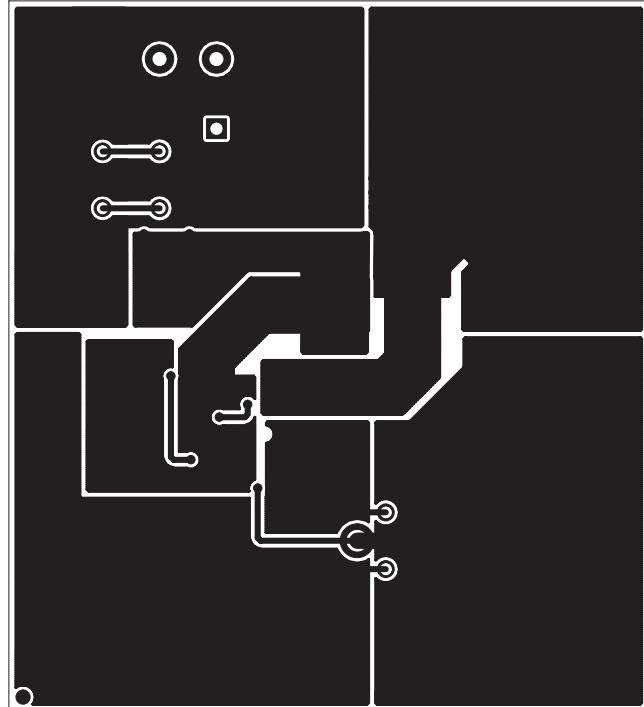
Figure 10
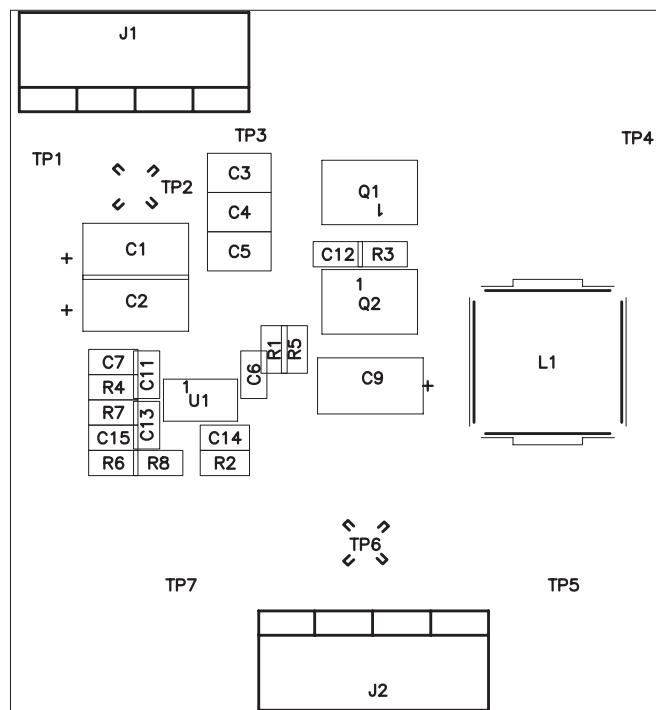
Figure 11

8   List of Material

Table 1 lists the components used in this design. With minor component tweaks this design could be modified to meet a wide range of applications.

|	Reference	Qty	Description	Manufacturer	Part Number
Capacitor	C1, C2	2	POSCAP, 330 µF, 6.3 V, 10 milliohm, 20%, 7343 (D)	Sanyo	6TPD330M
	C11	1	Ceramic, 180 pF, 50 V, NPO, 10%, 805	Vishay	VJ0805A181KXAAT
	C12	1	Ceramic, 0.01µF, 50 V, X7R, 10%, 805	Vishay	VJ0805Y103KXAAT
	C13	1	Ceramic, 0.0047 µF, 50 V, X7R, 10%, 805	Vishay	VJ0805Y472KXAAT
	C15	1	Ceramic, 6.8 nF, 50 V, X7R, 10%, 805	Vishay	VJ0805Y682KXAAT
	C3, C4, C5	3	Ceramic, 22 µF, 6.3 V, X5R, 20%, 1210	Panasonic	ECJ–4YB0J226M
	C6, C10, C14	3	Ceramic, 1 µF, 10 V, X5R, 10%, 805	Panasonic	ECJ–2YB1A105K
	C7	1	Ceramic, 1.5 nF, 50 V, X7R, 10%, 805	Vishay	VJ0805Y152KXAAT
	C8, C9	2	POSCAP, 470 µF, 4 V, 10 mΩ, 20%, 7343 (D)	Sanyo	4TPD470M
Terminal Block	J1, J2	2	4-pin, 15 A, 5.1 mm, 291126	OST	ED2227
Inductor	L1	1	Inductor, SMT, 1 µH, 15 A, 3.5 mΩ, 0.51 x 0.51	Vishay	IHLP–5050CE–01
MOSFET	Q1, Q2	2	MOSFET, N-channel, 12 V, 17 A, 5.5 mΩ, SO8	Siliconix	Si4866DY
Resistor	R1, R5	1	Chip, 1.8 Ω, 1/10 W, 5%, 805	Std	Std
	R2	1	Chip, 16.2 kΩ, 1/10 W, 1%, 805	Std	Std
	R3	1	Chip, 2.2 Ω, 1/10 W, 5%, 805	Std	Std
	R4	1	Chip, 5.90 kΩ, 1/10 W, 1%, 805	Std	Std
	R6	1	Chip, 10 kΩ, 1/10 W, 1%, 805	Std	Std
	R7	1	Chip, 698 Ω, 1/10 W, 1%, 805	Std	Std
	R8	1	Chip, 3.92 Ω, 1/10 W, 1%, 805	Std	Std
JACK	TP1, TP4, TP5,	3	Red, 1 mm, 0.038", 6400"	Farnell	240–345
Adapter	TP2, TP6	2	3.5-mm probe clip (or 131–5031–00), 72900	Tektronix	131–4244–00
JACK	TP3, TP7	1	Black, 1mm, 0.038",6400"	Farnell	240–333
Device	U1	1	Low Input Voltage Mode, Syncronous Buck Controller DGQ10	TI	TPS40007DGQ

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3   *Regulatory Notices:*

   3.1   *United States*

     3.1.1   *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

     3.1.2   *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

   3.2   *Canada*

     3.2.1   *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,

2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or

3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

【無線電波を送信する製品の開発キットをお使いになる際の注意事項】 開発キットの中には技術基準適合証明を受けて

いないものがあります。 技術適合証明を受けていないもののご使用に際しては、電波法遵守のため、以下のいずれかの

措置を取っていただく必要がありますのでご注意ください。

1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

なお、本製品は、上記の「ご使用にあたっての注意」を譲渡先、移転先に通知しない限り、譲渡、移転できないものとします。

上記を遵守頂けない場合は、電波法の罰則が適用される可能性があることをご留意ください。 日本テキサス・イ

ンスツルメンツ株式会社

東京都新宿区西新宿６丁目２４番１号

西新宿三井ビル

3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

電力線搬送波通信についての開発キットをお使いになる際の注意事項については、次のところをご覧ください。https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-for-power-line-communication.html

3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4   *EVM Use Restrictions and Warnings:*

    4.1   EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

    4.2   User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

    4.3   *Safety-Related Warnings and Restrictions:*

        4.3.1   User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

        4.3.2   EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

    4.4   User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5.   *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

6.   *Disclaimers:*

    6.1   EXCEPT AS SET FORTH ABOVE, EVMS AND ANY MATERIALS PROVIDED WITH THE EVM (INCLUDING, BUT NOT LIMITED TO, REFERENCE DESIGNS AND THE DESIGN OF THE EVM ITSELF) ARE PROVIDED "AS IS" AND "WITH ALL FAULTS." TI DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, REGARDING SUCH ITEMS, INCLUDING BUT NOT LIMITED TO ANY EPIDEMIC FAILURE WARRANTY OR IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF ANY THIRD PARTY PATENTS, COPYRIGHTS, TRADE SECRETS OR OTHER INTELLECTUAL PROPERTY RIGHTS.

    6.2   EXCEPT FOR THE LIMITED RIGHT TO USE THE EVM SET FORTH HEREIN, NOTHING IN THESE TERMS SHALL BE CONSTRUED AS GRANTING OR CONFERRING ANY RIGHTS BY LICENSE, PATENT, OR ANY OTHER INDUSTRIAL OR INTELLECTUAL PROPERTY RIGHT OF TI, ITS SUPPLIERS/LICENSORS OR ANY OTHER THIRD PARTY, TO USE THE EVM IN ANY FINISHED END-USER OR READY-TO-USE FINAL PRODUCT, OR FOR ANY INVENTION, DISCOVERY OR IMPROVEMENT, REGARDLESS OF WHEN MADE, CONCEIVED OR ACQUIRED.

7.   *USER'S INDEMNITY OBLIGATIONS AND REPRESENTATIONS.* USER WILL DEFEND, INDEMNIFY AND HOLD TI, ITS LICENSORS AND THEIR REPRESENTATIVES HARMLESS FROM AND AGAINST ANY AND ALL CLAIMS, DAMAGES, LOSSES, EXPENSES, COSTS AND LIABILITIES (COLLECTIVELY, "CLAIMS") ARISING OUT OF OR IN CONNECTION WITH ANY HANDLING OR USE OF THE EVM THAT IS NOT IN ACCORDANCE WITH THESE TERMS. THIS OBLIGATION SHALL APPLY WHETHER CLAIMS ARISE UNDER STATUTE, REGULATION, OR THE LAW OF TORT, CONTRACT OR ANY OTHER LEGAL THEORY, AND EVEN IF THE EVM FAILS TO PERFORM AS DESCRIBED OR EXPECTED.

8. *Limitations on Damages and Liability:*

   8.1 *General Limitations.* IN NO EVENT SHALL TI BE LIABLE FOR ANY SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL, OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF THESE TERMS OR THE USE OF THE EVMS , REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. EXCLUDED DAMAGES INCLUDE, BUT ARE NOT LIMITED TO, COST OF REMOVAL OR REINSTALLATION, ANCILLARY COSTS TO THE PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES, RETESTING, OUTSIDE COMPUTER TIME, LABOR COSTS, LOSS OF GOODWILL, LOSS OF PROFITS, LOSS OF SAVINGS, LOSS OF USE, LOSS OF DATA, OR BUSINESS INTERRUPTION. NO CLAIM, SUIT OR ACTION SHALL BE BROUGHT AGAINST TI MORE THAN TWELVE (12) MONTHS AFTER THE EVENT THAT GAVE RISE TO THE CAUSE OF ACTION HAS OCCURRED.

   8.2 *Specific Limitations.* IN NO EVENT SHALL TI'S AGGREGATE LIABILITY FROM ANY USE OF AN EVM PROVIDED HEREUNDER, INCLUDING FROM ANY WARRANTY, INDEMITY OR OTHER OBLIGATION ARISING OUT OF OR IN CONNECTION WITH THESE TERMS, , EXCEED THE TOTAL AMOUNT PAID TO TI BY USER FOR THE PARTICULAR EVM(S) AT ISSUE DURING THE PRIOR TWELVE (12) MONTHS WITH RESPECT TO WHICH LOSSES OR DAMAGES ARE CLAIMED. THE EXISTENCE OF MORE THAN ONE CLAIM SHALL NOT ENLARGE OR EXTEND THIS LIMIT.

9. *Return Policy.* Except as otherwise provided, TI does not offer any refunds, returns, or exchanges. Furthermore, no return of EVM(s) will be accepted if the package has been opened and no return of the EVM(s) will be accepted if they are damaged or otherwise not in a resalable condition. If User feels it has been incorrectly charged for the EVM(s) it ordered or that delivery violates the applicable order, User should contact TI. All refunds will be made in full within thirty (30) working days from the return of the components(s), excluding any postage or packaging costs.

10. *Governing Law:* These terms and conditions shall be governed by and interpreted in accordance with the laws of the State of Texas, without reference to conflict-of-laws principles. User agrees that non-exclusive jurisdiction for any dispute arising out of or relating to these terms and conditions lies within courts located in the State of Texas and consents to venue in Dallas County, Texas. Notwithstanding the foregoing, any judgment may be enforced in any United States or foreign court, and TI may seek injunctive relief in any United States or foreign court.

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