EVM User's Guide: TAS2572EVM

TAS2572 Evaluation Module

Description

The TAS2572EVM has been designed to demonstrate the performance of TAS2572 in a dual-mono configuration. This tool utilizes the AC-MB motherboard to provide an interface and supply voltages to the EVM daughter card. Up to four devices can share a common bus through I^2S/TDM + I^2C interfaces; two EVMs can be mounted one on top of each other, as shown in Section 2.9.

Get Started

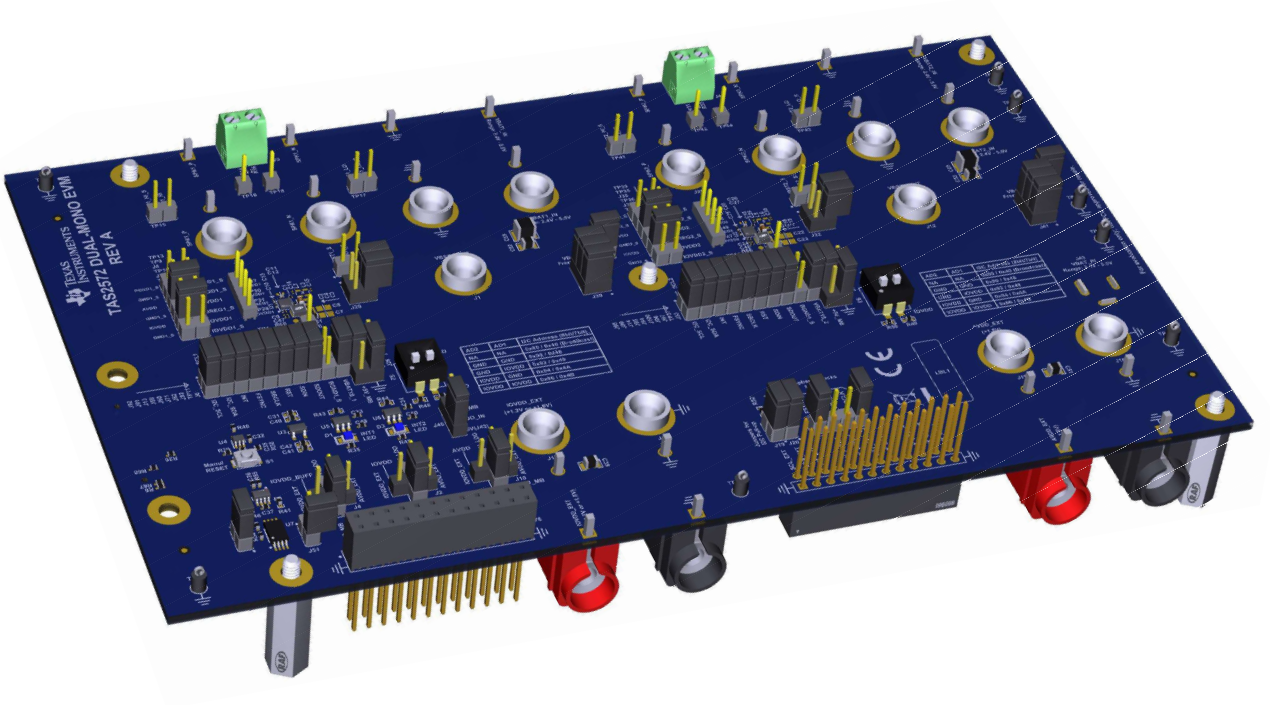
1. Download TAS2572 data sheet.
2. Order the EVM at TAS2572 product folder.
3. Request access and download PPC3 from TAS2572 product folder.
4. Visit and ask questions at e2e forum.

Features

- Mono or dual-mono speaker evaluation
- Interface using PurePath Console 3 Windows® software
- EVM interconnection for up to 4 audio channels
- USB input
- External I^2C and I^2S/TDM host controller connection available

Applications

- Mobile Phone, Tablets and Wearables
- Smart Speakers with Voice Assistance
- Bluetooth and Wireless Speakers



TAS2572 Dual-Mono Evaluation Module

1 Evaluation Module Overview

1.1 Introduction

This user's guide describes the function and use of the TAS2572EVM. This document includes the hardware configuration instructions, a quick-start guide, jumper and connector descriptions, software description, schematics, and printed circuit board (PCB) layout that demonstrate TI's recommended practices for these devices.

This section provides details on what is included inside the evaluation module box, what are TAS2572 capabilities and operation ranges, as well as what is the additional test equipment that can be required for a full audio evaluation.

1.2 Kit Contents

The evaluation kit consists of the following items:

- TAS2572EVM
- AC-MB controller board

A speaker is not included in the kit, however any speaker can be connected to each of the amplifiers outputs using the banana jacks or screw headers.

Similarly, a power supply is not part of the kit, but the barrel jack connector can be connected to any power supply in a range of 2.4V to 5.5V.

1.3 Specification

The TAS2572 is a digital input Class-D audio amplifier optimized for delivering best battery life for real use case of Music playback and Voice calls.

The integrated boost operation is flexible so that TAS2572 can be implemented in 1S, 2S and 3S battery applications. TAS2572EVM showcases the 1S battery broadly used in mobile and industrial applications.

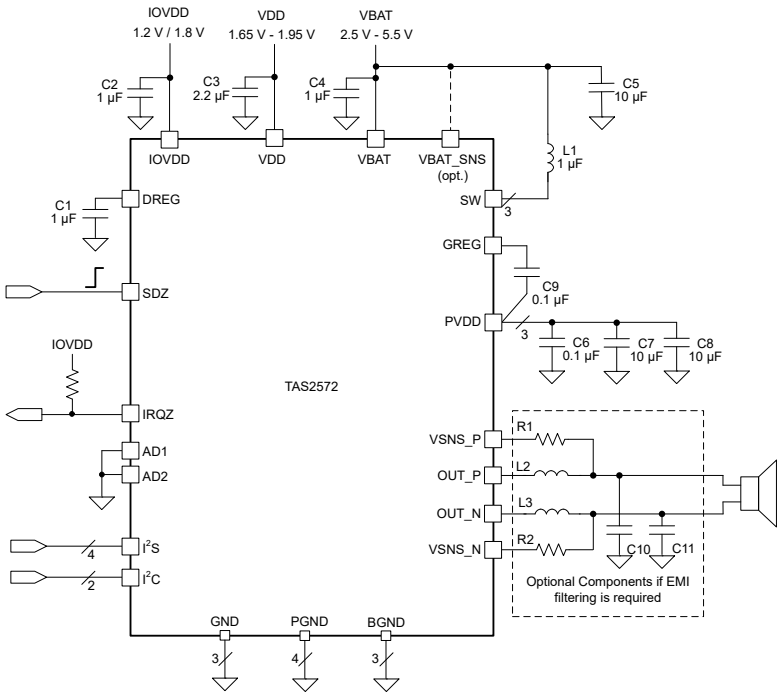


Figure 1-1. Application Diagram for 1 S Battery System

For 2 S battery applications, the boost inductor can be supplied by a higher supply from 4.5V to 9 V. VBAT pin must still be supplied by a voltage from 2.5V to 5.5V.

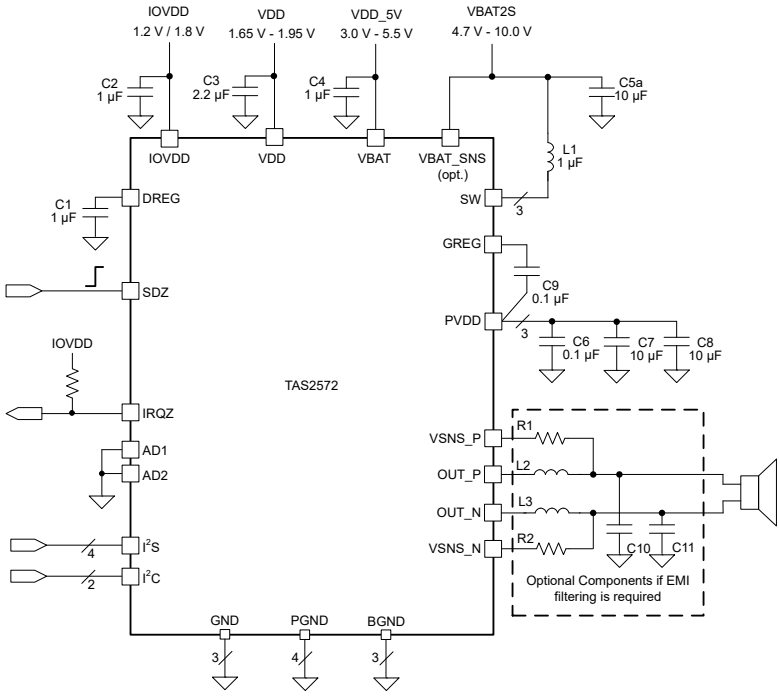


Figure 1-2. Application Diagram for 2 S Battery System

In a 3 S battery application, the integrated boost can be bypassed, and an external power rail up to 14 V can supply PVDD directly. The boost inductor is not required in this case and SW pins are left open. VBAT pin must still be supplied by a voltage from 2.5V to 5.5V.

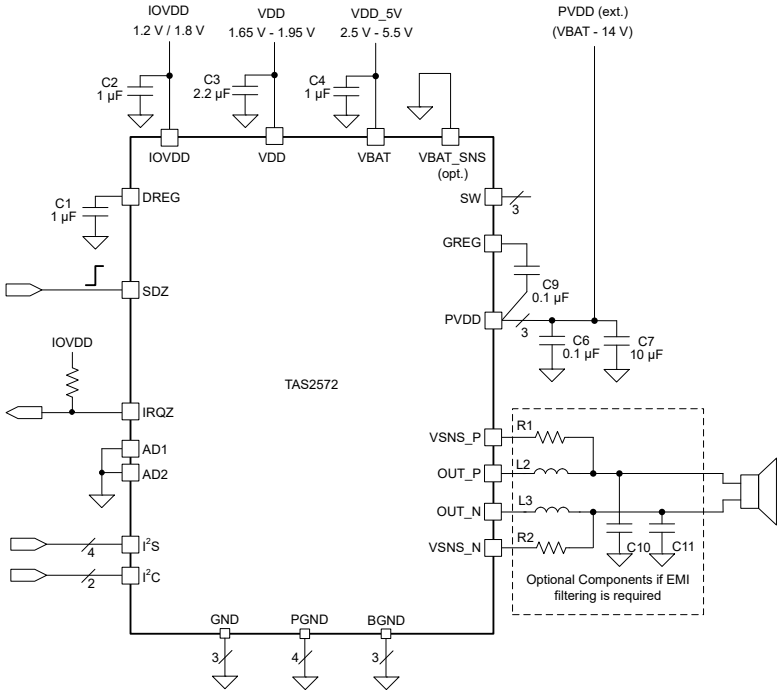


Figure 1-3. Application Diagram for 3 S Battery System

1.4 Device Information

TAS2572 is a mono, digital-input, Class-D audio amplifier optimized for efficiently driving high peak power into small loudspeaker applications. The Class-D amplifier is capable of delivering 6W of max average power into 8

Ω load at a battery voltage of 4.2 V. Integrated speaker voltage and current sense provides real time monitoring of loud speakers. Up to four devices can share a common bus via I^2S/TDM + I^2C interfaces.

2 Hardware

2.1 AC-MB Settings

2.1.1 Audio Serial Interface Settings

The AC-MB provides the digital audio signals to the evaluation module from the USB, optical connector, stereo jack, and external audio serial interface (ASI) header. Figure 2-1 shows a block diagram of the ASI routing on the AC-MB.

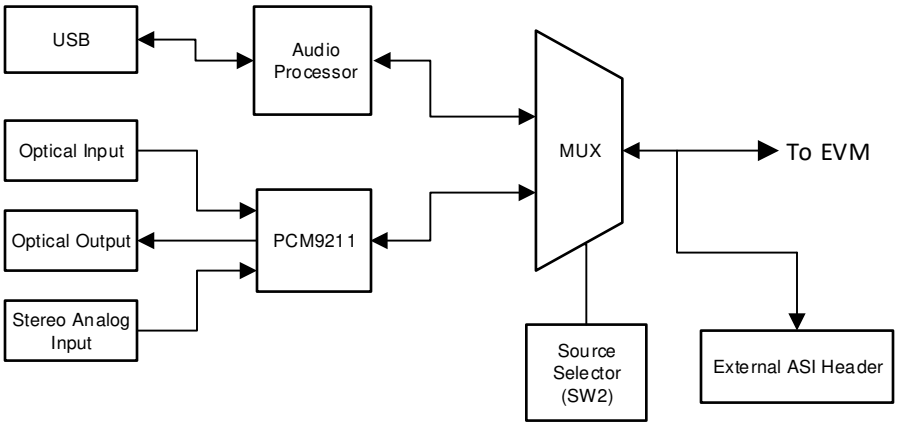


Figure 2-1. AC-MB Audio Serial Interface Routing

Switch SW2 on the AC-MB selects the audio serial bus that interfaces with the TAS2572EVM daughter card. Next to switch SW2, the AC-MB has a quick reference table to identify the audio serial interface source options and switch settings. The AC-MB acts as the controller for the audio serial interface, with three different modes of operation: USB, optical or analog, or external ASI.

2.1.2 USB

The serial interface clocks and data are provided from the USB interface. The sampling rate and format are determined by the USB audio class driver on the operating system.

The default settings for the USB audio interface are 32-bit frame size, 48-kHz sampling rate, BCLK and FSYNC ratio is 256, and the format is time division multiplexing (TDM).

The AC-MB is detected by the OS as an audio device with the name TI USB Audio UAC2.0. Figure 2-2 illustrates the AC-MB audio setting for the USB mode of operation.

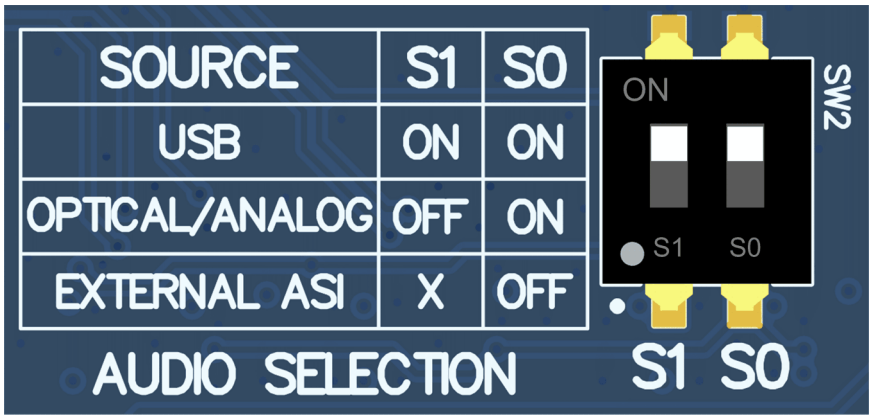


Figure 2-2. AC-MB USB Audio Setting

2.1.3 External

In this mode, the audio serial interface clocks for the evaluation board are provided through connector J7 from an external source. This architecture allows the use of an external system to communicate with the evaluation board, such as a different host processor or test equipment (for instance, Audio Precision PSIA). The clocks generated from the USB interface and PCM9211 are isolated with this setting. Figure 2-3 shows the AC-MB audio setting for the external mode of operation.

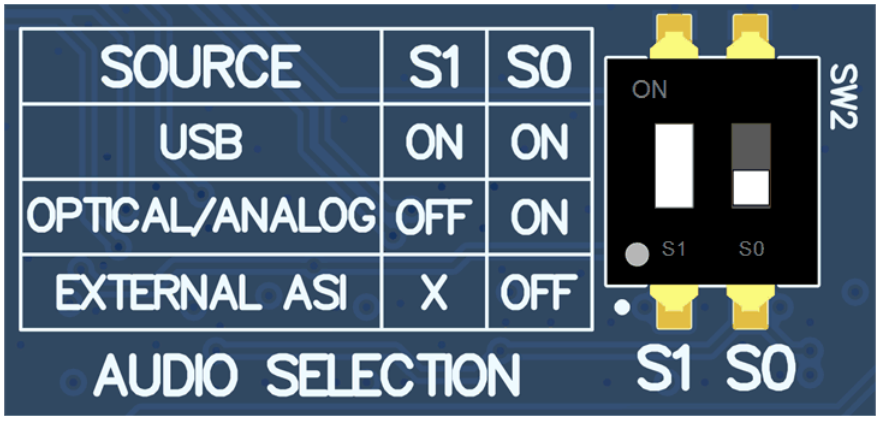


Figure 2-3. AC-MB External Audio Setting

Figure 2-4 shows how to connect the external audio interface, with the bottom row for the signal and the top row for ground.

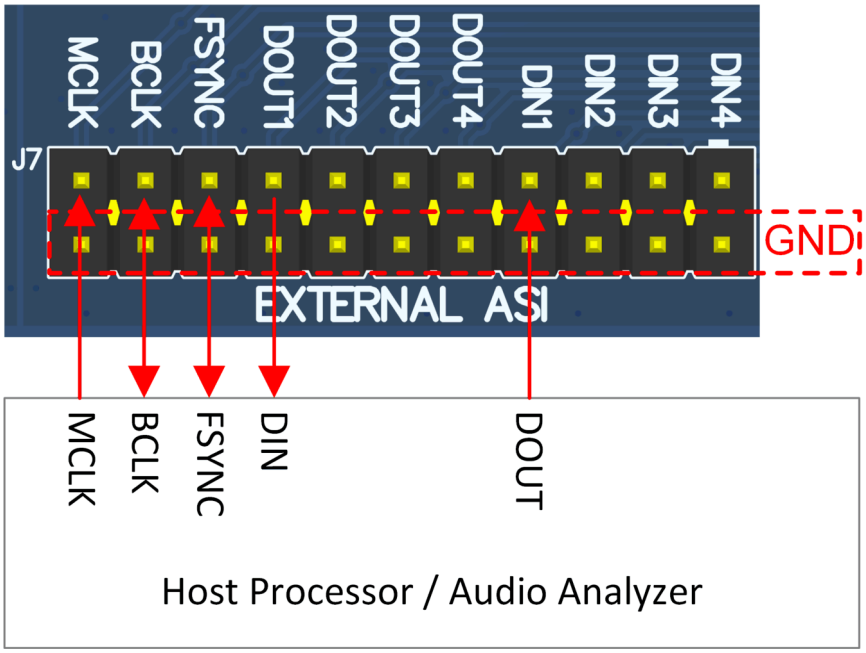


Figure 2-4. AC-MB Connection with External Audio Serial Interface

2.2 AC-MB Power Supply

The AC-MB motherboard is powered from a single 5-V power supply. However, the motherboard has different low-dropout regulators (LDOs) integrated that provide the required power supplies to the different blocks of the board. Figure 3-1 shows a block diagram depicting the power structure of the AC-MB. The AC-MB can be powered from the host computer by using the USB 5-V power supply (VBUS) by shorting header J5, USB POWER. Additionally, the AC-MB can be powered from an external power supply connected to terminal J4, EXTERNAL POWER. Header J5 must be open for external supply operation. The IOVDD voltage for the digital signals that is provided to the evaluation module is generated on the motherboard from the main power supply (USB or external). The voltage levels available are 1.2V, 1.8V and 3.3V, and can be selected via the J3 header IOVDD. Default setting for TAS2572EVM operation is 1.8V; **3.3V operation cannot be used for TAS2572EVM**. When the motherboard is fully powered and the power supplies from the onboard LDOs are correct, the green POWER LED (D3) turns ON. The USB READY LED indicates that a successful USB communication is established between the AC-MB and the host computer.

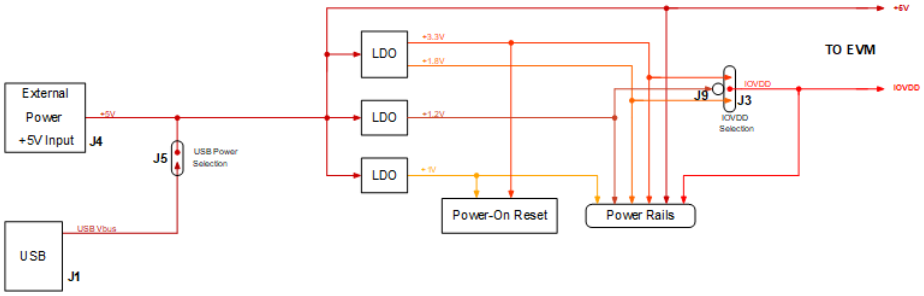


Figure 2-5. Power -Supply Distribution of the AC-MB

2.3 Default Jumper Setting on TAS2572EVM

Figure 4-1 given below illustrates all the default jumper settings for TAS2572EVM.

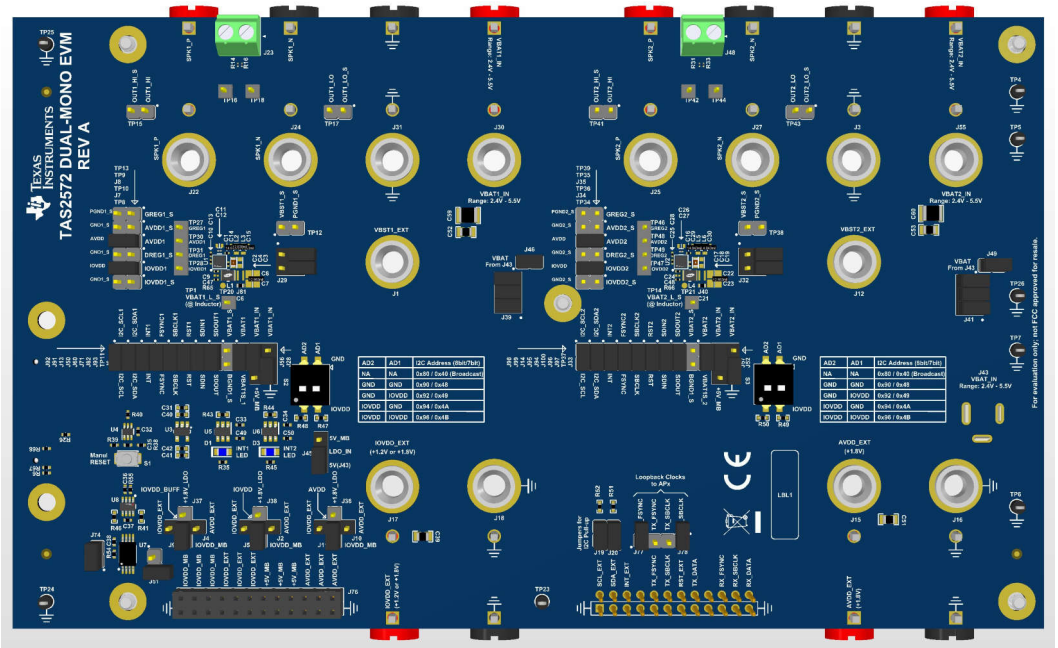


Figure 2-6. Default Jumper Settings

Table 4-1 shows the default positions for all the jumpers on TAS2572EVM.

Table 2-1. Default Jumper Settings

Jumper	Setting	Description
J7	Insert	IOVDD current sense for U1
J8	Insert	AVDD current sense for U1
J29	DNI	External VBST for U1
J6	Insert	VBAT pin current sense for U1
J93	Insert	SDOUT break for U1
J82	Insert	SDIN break for U1
J71	Insert	RST break for U1
J60	Insert	SBCLK break for U1
J50	Insert	FSYNC break for U1
J13	Insert	INT break for U1
J91	Insert	SDA break for U1
J92	Insert	SCL break for U1
J56	Insert (1-2)	VBAT source selector for U1
J28	Insert (2-3)	VBAT_SNS selector for U1
J39	Insert	VBAT source from barrel jack for U1
J46	Insert	VBAT source from barrel jack for U1
J34	Insert	IOVDD current sense for U2
J35	Insert	AVDD current sense for U2
J32	DNI	External VBST for U2
J33	Insert	VBAT pin current sense for U2
J97	Insert	SDOUT break for U2
J96	Insert	SDIN break for U2
J100	Insert	RST break for U2
J94	Insert	SBCLK break for U2
J95	Insert	FSYNC break for U2
J14	Insert	INT break for U2
J99	Insert	SDA break for U2
J98	Insert	SCL break for U2
J57	Insert (1-2)	VBAT source selector for U2
J52	Insert (2-3)	VBAT_SNS selector for U2
J41	Insert	VBAT source from barrel jack for U2
J49	Insert	VBAT source from barrel jack for U2
J74	DNI	EEPROM write protect
J51	DNI	EEPROM address selector
J37-4-9	IOVDD_MB	Buffer source selector
J38-5-2	IOVDD_MB	IOVDD source selector for U1 and U2
J36-11-10	IOVDD_MB	AVDD source selector for U1 and U2
J45	Insert (2-3)	1.8V LDO source selector

Table 2-1. Default Jumper Settings (continued)

Jumper	Setting	Description
J19	Insert	I²C pull-up connect
J20	Insert	I²C pull-up connect
J77	DNI	FSYNC loopback for APx connection
J78	DNI	SBCLK loopback for APx connection

2.4 I²C Target Address Selection

TAS2572EVM has DIP switches S2 and S3 for setting the I²C target address for each channel individually as per the table provided in the silk screen of the PCB. Make sure both the devices have different target address.

Figure 2-7. DIP Switch S2-S3 for I²C Address Selection

2.5 IOVDD and AVDD Power Supply Options on EVM

TAS2572EVM daughter card provide multiple flexible options for IOVDD_BUFF, IOVDD and AVDD power supplies. There are options to select between internal or external voltage sources for each of these supplies individually.

IOVDD_BUFF is 1.8V power supply, which is used for the buffers and voltage translators.

IOVDD is the input/output power supply for TAS2572 device, which can be either 1.2V or 1.8V.

AVDD is the analog power supply for TAS2572 device, which must be 1.8V fixed. If using IOVDD_MB from AC-MB as 1.2V, make sure to select AVDD source to be either external or +1.8V_LDO.

Figure 6-1shows the default jumper setting for IOVDD_BUFF, IOVDD and AVDD. By default, 1.8V coming from the AC-MB motherboard (IOVDD_MB) has been selected for IOVDD_BUFF, IOVDD and AVDD with the help of jumper J9, J5 and J11.

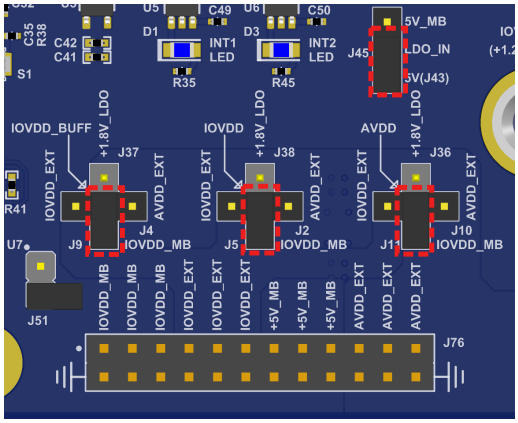


Figure 2-8. Default Jumper Setting for IOVDD_BUFF, IOVDD and AVDD

There are 1.8V and 3.3V LDOs included in the EVM. These LDOs are powered from the supply connected to J43, or these can be supplied either from 5 V rail coming from AC-MB, depending on the configuration of jumper J45.

2.6 VBAT Power Supply for TAS2572 on EVM

By default, the barrel jack connector J43 is used to power VBAT on both TAS2572 channels. Supply 2.4V-5.5V on this connector.

Alternatively, independent connectors can be used for the external VBAT supply for both the channels – VBAT1_IN and VBAT2_IN. Jumpers J39 and J46 must be open to disconnect VBAT to VBAT1_IN form J43 input, and similarly J41 and J49 must be open to disconnect VBAT to VBAT2_IN from J43 input.

For channel-1, external VBAT1_IN can be connected between connectors J30 (or J72) and J31 (or J73) as shown in Figure 7-1.

For channel-2, external VBAT2_IN can be connected between connectors J55 (or J58) and J3 (or J59) as shown in Figure 7-1.

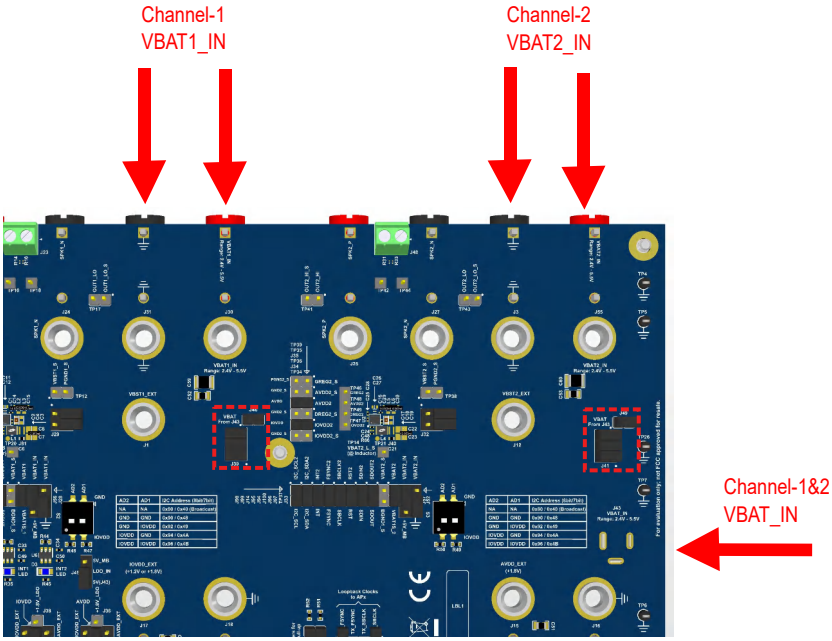


Figure 2-9. VBAT Connector for Channel-1 and Channel-2

2.6.1 VBAT 2S EVM Hardware Configuration

This section shows how to set the EVM jumpers to evaluate TAS2572EVM in a 2 S battery application for VBAT, as depicted in Figure 1-2.

In this case, VBAT pin C1 must still be connected to a power supply range from 3 V up to 5 V, while VBAT_SNS and the boost inductor can be connected to a higher 2 S supply range from 4.5V up to 9 V.

- VBAT pin C1 connection can be connected to USB-5V by changing J56 position to 2-3 instead of 1-2.
- VBAT_SNS pin C4 connection can be modified using J28, this connection is optional.
- 2 S VBAT supply is directly available at J30 (or J72) and J31 (or J73) for channel-1 and J55 (or J58) and J3 (or J59) for channel-2. If using J43 to supply 2 S battery voltage, then make sure to change J45 to use +5V_MB instead.

2.6.2 VBAT 3 S EVM Hardware Configuration

This section shows how to set the EVM jumpers to evaluate TAS2572EVM in a 3 S battery application for VBAT as depicted in Figure 1-3.

VBAT pin C1 must still be connected to a power supply range from 3 V up to 5 V. VBAT_SNS cannot be used so VBAT_SNS must be shorted to GND. The internal boost is not used, so the SW pins are left floating and the inductor can be removed from the circuit.

3 S battery supply range from VBAT pin C1 level up to 14 V is directly connected to PVDD node, the decoupling capacitors and GREG capacitor are still required.

- VBAT pin C1 connection can be connected to USB-5V by changing J56 position to 2-3 instead of 1-2.
- VBAT_SNS pin C4 connection must be left as default with J28 shorted across pins 2-3.
- 3 S VBAT supply must be connected to J1 for channel-1 and J12 for channel-2, short the jumpers across J29 and J32.

2.7 Speaker Outputs

Since TAS2572EVM is a dual-mono EVM, each channel has a speaker output connector.

SPK1_P and SPK1_N are the outputs for channel-1 device, whereas SPK2_P and SPK2_N are the outputs for channel-2. Multiple type of connectors have been provided like horizontal banana barrel connectors, vertical banana sockets, screw terminal connector and pin headers to be able to connect speaker or dummy load with fly-wires or male banana connectors. These can also be used to connect into an audio analyzer analog input cable for performance measurements.

Channel-1 output connectors as shown in Figure 8-1:

- J22 (SPK1_P) and J24 (SPK1_N)
- J21 (SPK1_P) and J26 (SPK1_N)
- J23: Pin-2 (SPK1_P) and Pin-1 (SPK1_N)
- TP-16 (SPK1_P) and TP-18 (SPK1_N)

Channel-2 output connectors as shown in Figure 8-1:

- J47 (SPK2_P) and J54 (SPK2_N)
- J25 (SPK2_P) and J27 (SPK2_N)
- J48: Pin-2 (SPK2_P) and Pin-1 (SPK2_N)
- TP-42 (SPK2_P) and TP-44 (SPK2_N)

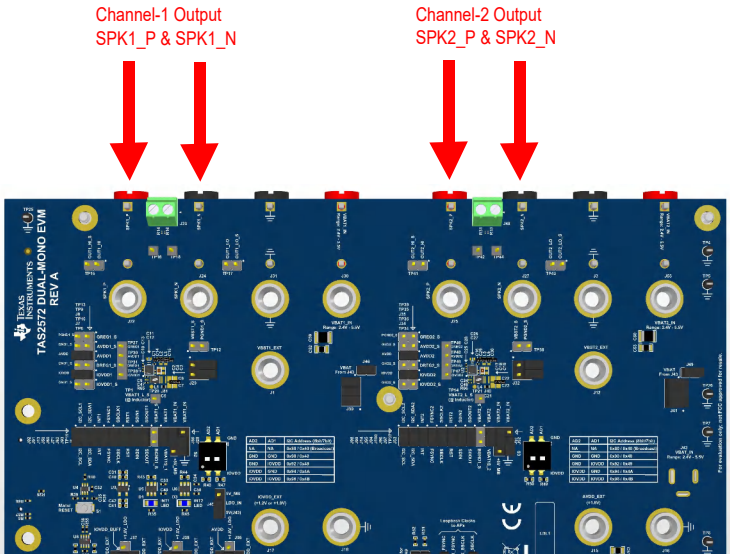


Figure 2-10. Speaker Output Connector for Channel-1 and Channel-2

2.8 1-Channel Configuration

When only 1 of the amplifiers on the TAS2572EVM is required, the other device can be completely isolated from the circuit. This section includes instructions on how to disconnect U2, however the same procedure can be applied to disconnect U1.

- The block of jumpers from J98 through J33 must be disconnected, as well as J57 and J52 in the same row. This removes all digital signals and VBAT supply as well.
- J34 and J35 to the left of U2 must be disconnected as well. This removes IOVDD and AVDD supplies.
- J41 and J49 must be disconnected as well. This removes VBAT connection from J43 to the boost inductor.

2.9 4-Channel Configuration

Two dual-mono EVMs can be interconnected using J75 and J76 headers, mounting one EVM on top of another. This enables the evaluation of a total of 4 audio channels.

When 2 EVMs are interconnected, the following jumper configuration must be considered:

- Short jumper J51 on one of the EVMs, this jumper is open by default.
- Open jumpers J19 and J20 on both EVMs, these jumpers are shorted by default.

In addition to the jumper configurations, make sure each amplifier is set for a different I^2C address using S2 and S3 on each EVM.

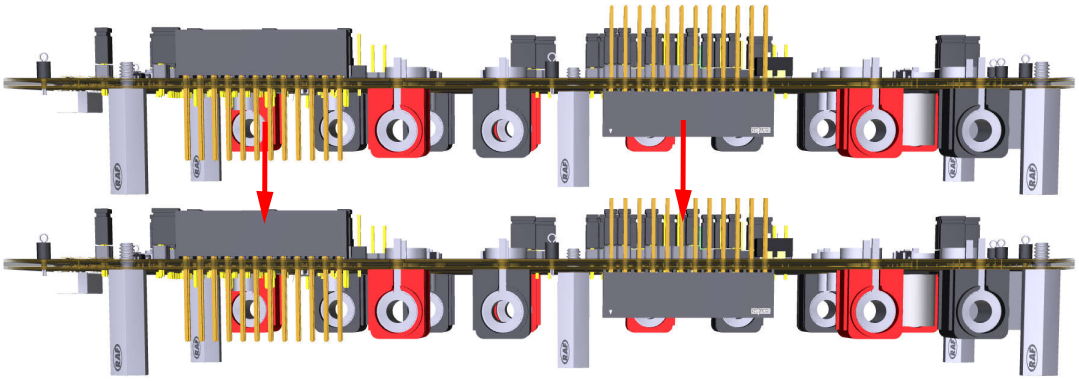


Figure 2-11. 4-Channel EVM Interconnection

2.10 4-Wire Measurement of Load

TAS2572EVM has been design such that the dummy load or speaker load connected to the device can be measured very accurately directly from the device pin including board parasitic and connector contact resistance using 4-wire method in digital multimeter. Pin header have been provided to be able to connect digital multimeter in 4-wire mode as shown below Figure 12-1.

For channel-1: Connect HI of DMM to pin-1 and HI_SNS of DMM to pin-2 of TP15 test point.

Connect LO of DMM to pin-2 and LO_SNS of DMM to pin-1 of TP17 test point.

For channel-2: Connect HI of DMM to pin-1 and HI_SNS of DMM to pin-2 of TP41 test point.

Connect LO of DMM to pin-2 and LO_SNS of DMM to pin-1 of TP43 test point.

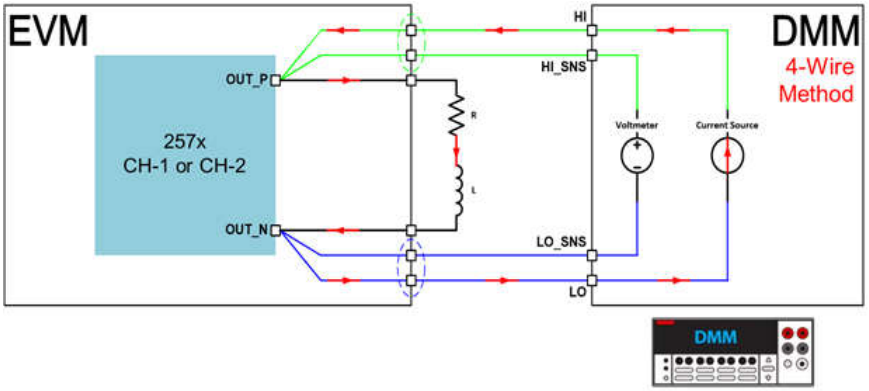


Figure 2-12. Load DC Resistance Measurement in 4-Wire Mode using Digital Multimeter

3 Software

3.1 PurePath Console 3 Quick Startup

PurePath Console 3 configuration tool can be used to interface with TAS2572 using the onboard controller, which in turn sends I^{2}C commands to setup the required register settings.

When PPC3 is executed for the first time, there are no plug-ins included. User must click on the *Sign In* either from the button at the top-right corner or from the *EVM Apps* section. A new window requests the user credentials, input the same myTI account used to request access to PPC3. Once logged in, the requested device applications is available for download and install.

Once the *257x EVM* app has been installed, click on the block with the name to open the GUI. Before proceeding, connect and power up VBAT to J43 and connect the EVM to a host PC using the USB connector on the AC-MB.

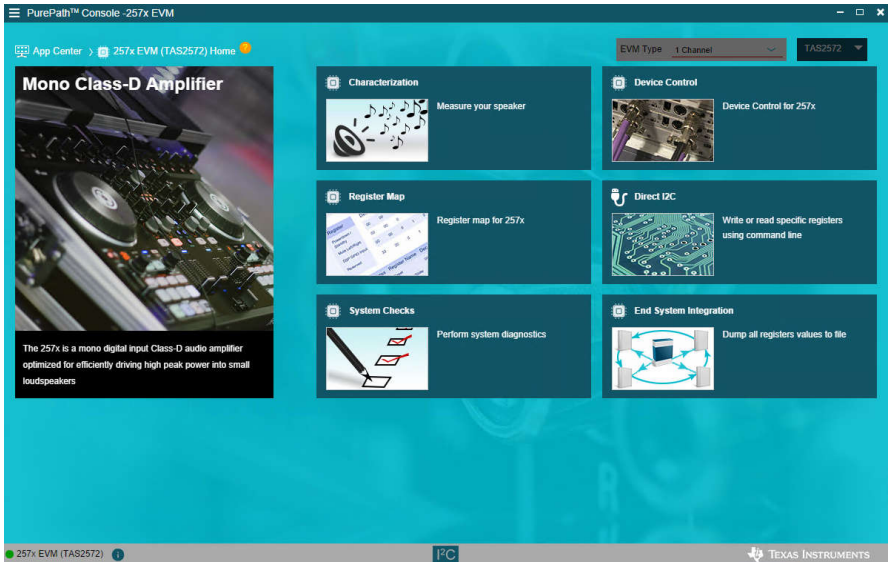


Figure 3-1. 257x EVM App Main Panel

Once the board is powered and connected to USB, and the PPC3 plug-in is running, the PC automatically recognizes the device (TAS2572). PPC3 detect as well as the number of channels, depending on how many of these are being powered and present on the I^{2}C bus.

To initialize the device registers, click on the *Device Control* tile, and then *Apply* at the *Channel Grouping* window.

Channel Grouping allows the user to define groups of devices so that a different configuration can be used for each group. By default, both devices on the EVM are assigned to the same group, so to change one of these to a new group, the device must be deleted from the original group first, and then the device can be added to a different group using the "+" symbol.

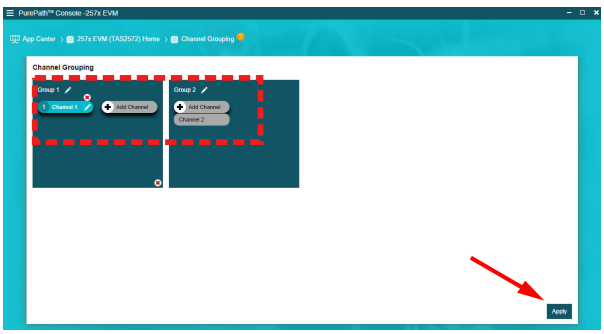


Figure 3-2. Channel Grouping

After a few seconds, the devices are initialized and muted. Click on the *Power Up* button at the top-right corner. Now the devices are completely configured and un-muted, ready to play audio.

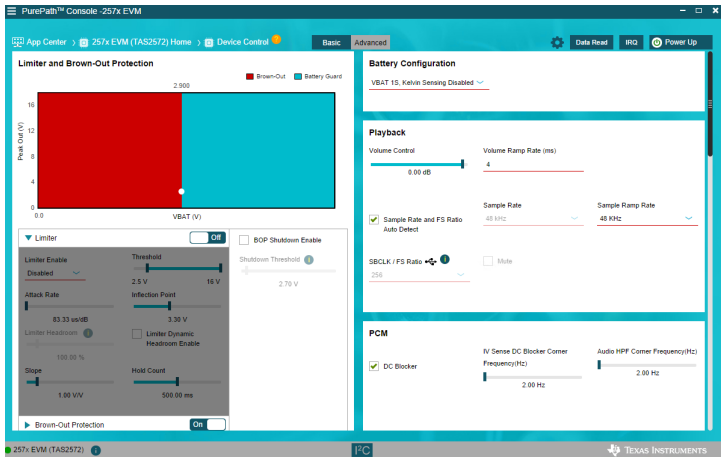


Figure 3-3. Device Control Panel

3.2 PPC3 - 257x EVM Feature Description

3.2.1 Limiter and Brown-Out Protection

TAS2572 features battery tracking brown-out and limiter features. Each of these features can be configured in detail as listed below:

Brown-out protection:

- This feature is enabled by default to start attenuation when VBAT drops below 2.9V. An additional threshold for BOP shutdown can be enabled as well.
- The BOP threshold is the VBAT voltage at which the amplifier starts applying attenuation to the output signal.
- Max attenuation is how much the amplifier reduces the playback signal then BOP is active. This limit goes from 1 dB down to 16.5dB in 0.5dB steps.
- Attack, Hold and Release are the timing parameters for the BOP gain controller.

Limiter:

- This feature is disabled by default. This can be considered an extension of the BOP where gain can be adjusted dynamically depending on the VBAT level so that output voltage stays within a specified limit.
- Threshold parameter sets Vout-peak limit region. If both min and max settings for this threshold are set to the same value, then the threshold becomes a hard limiter instead of a dynamic gain controller.
- Inflection point sets the VBAT voltage at which the limiter reaches the maximum threshold.
- Attack, Hold and Slope parameters set the dynamic gain controller timing settings.

Figure 3-4. Limiter PPC3 Configuration

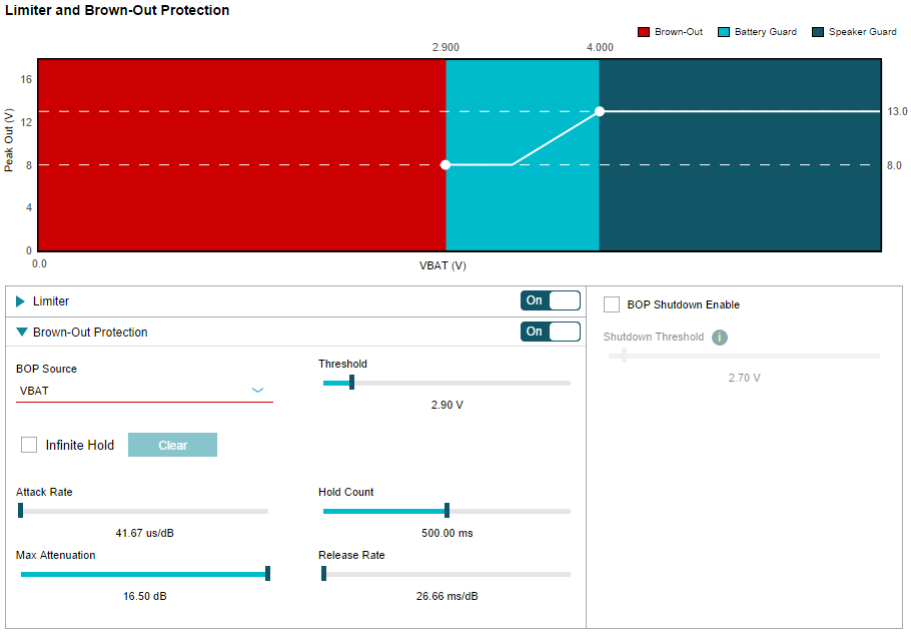


Figure 3-5. Brown-Out Protection PPC3 Configuration

3.2.2 Playback and PCM Configuration

Playback and PCM panels provide configuration for the digital input to analog output signal path.

- Volume Control is the gain on the digital domain which goes from -110dB up to 6 dB.
- Ramp Rate is how the gain ramps up/down when going in and out of mute, or when gain is adjusted.
- By default Sample Rate and SBCLK to FS Ratio are set to automatically detect the input clock frequencies, and adjust the internal clock tree settings based on that. If manual configuration is desired, the checkbox can be disabled, and the USB Audio Settings can be overridden by clicking on the gear icon on the top-right, then click to disable the USB settings.
- DC blocker is enabled by default but can be disabled for the Playback (output) path. Both Playback and Feedback path High-Pass Filter cutoff frequencies can be adjusted manually using the slider or typing a new value in the text box.

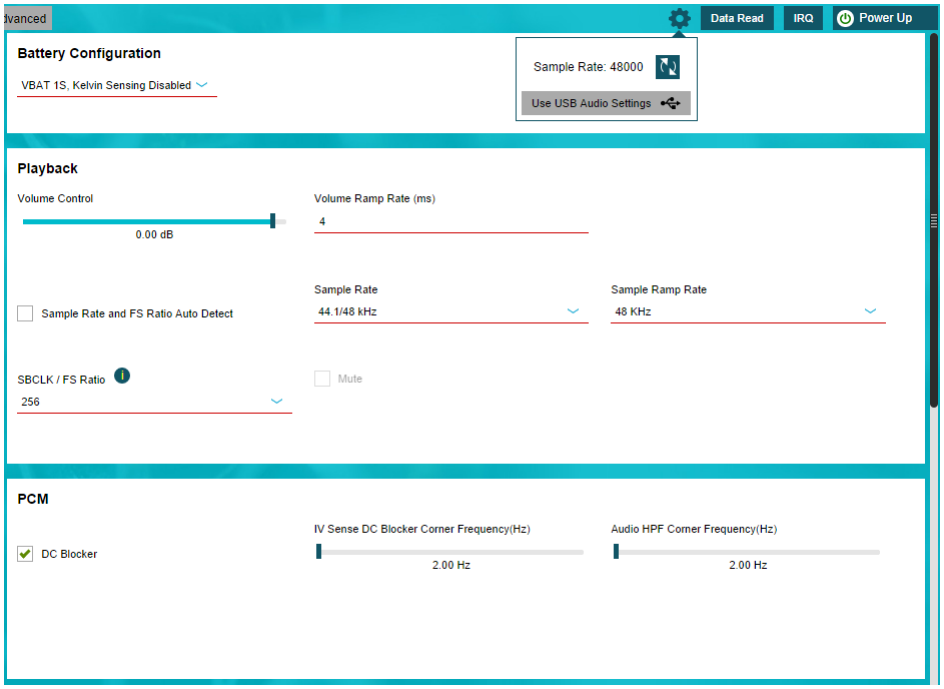


Figure 3-6. Playback and PCM PPC3 Configuration

3.2.3 TDM Receiver and Transmitter PPC3 Configuration

TDM panel includes all the configuration related to the I2S/TDM audio interface. There is a dedicated tab for Receiver (SDIN) and Transmitter (SDOUT). Default settings match with USB controller configuration, however these can be overridden similarly as explained for the previous section.

Receiver configuration can be used to modify the digital audio format in terms of Edge Polarity, Justification, Frame Start Polarity, Offset Bits, Word Length and Slot Length. In addition to that, the input data can be arranged from multiple slots or even select a couple slots to result in a mono-mix playback.

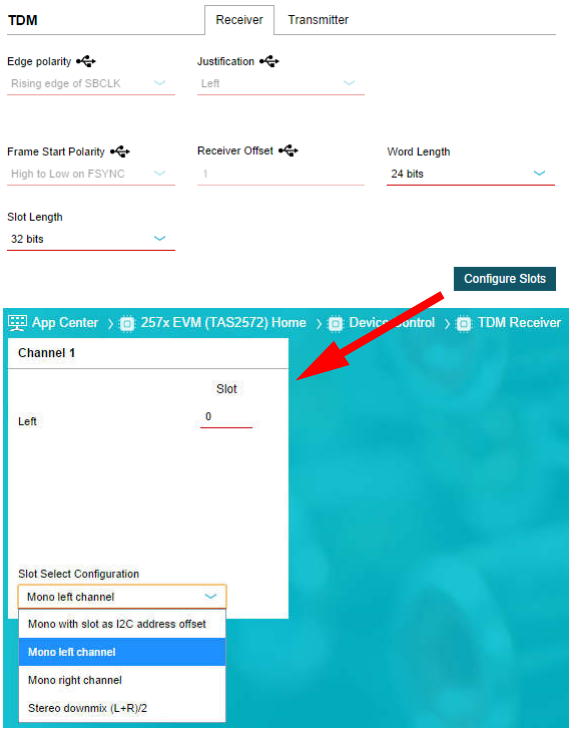


Figure 3-7. TDM Receiver PPC3 Configuration

Transmitter configuration provides similar settings for SDOUT timing. Similarly, the output data slots can be arranged based on the application requirements; take into consideration that SDOUT slots are always considered as 8-bit, so for 16-bit data length 2 slots must be used, and for 32bit data length 4 slots areov required.

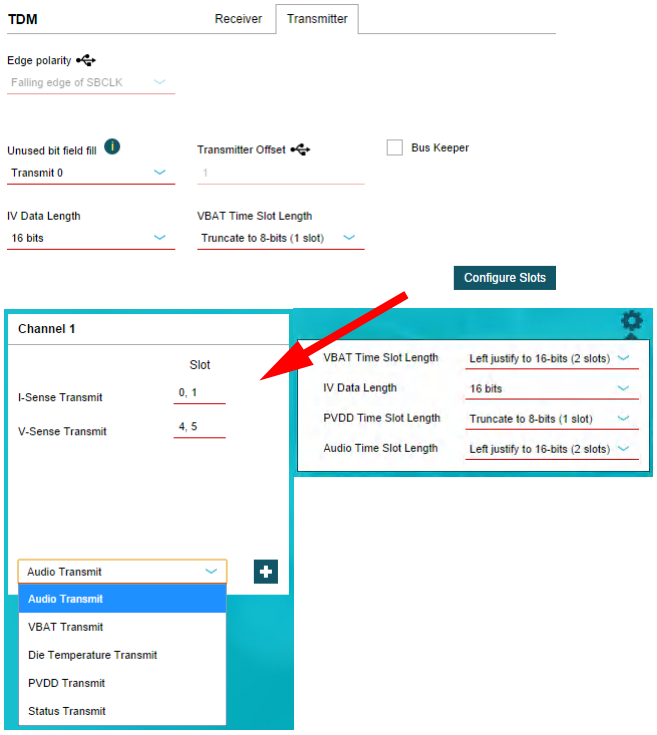


Figure 3-8. TDM Transmitter PCM PPC3 Configuration

3.2.4 Miscellaneous and IRQ$_Z$ Configuration

The miscellaneous section can be used to change different portions of the digital interface pins of the TAS2572.

The over temperature, over current and internal clock error can be configured to latch or retry after a wait time, which is also configurable as 1.5 seconds or 100 milliseconds.

The output of the amplifiier can be set to Hi-Z during shutdown, either due to error interrupt or manual shutdown.

There are internal pull-up resistors that can be enabled and disabled individually at the digital pins such as SBCLK, FSYNC, SDIN, SD$_Z$, AD0 and AD1.

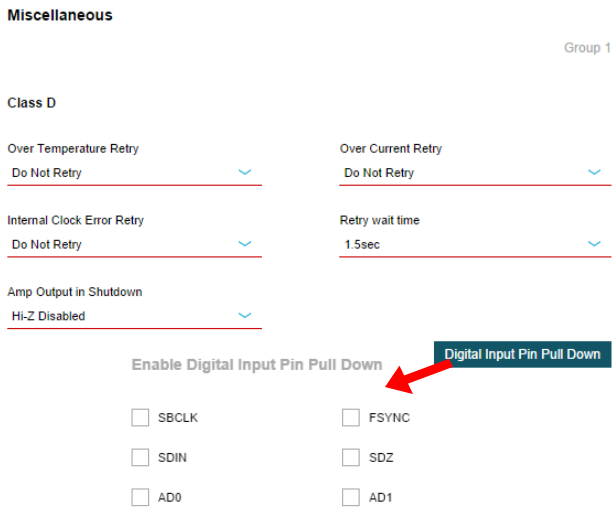


Figure 3-9. Miscellaneous PPC3 Configuration

IRQ$_Z$ section includes all the configurations related to the digital notification of error and interrupts internal to the device.

IRQ$_Z$ pin can be configured to assert when any live or latched interrupt triggers, and can be configured to assert and de-assert automatically once every live interrupt or can also keep pulsing every 4 ms once a latched interrupt is triggered.

By default IRQ$_Z$ pin is an open drain output, however an internal pull-up can be enabled as well. Each of the internal interrupts can be masked or un-masked to trigger the IRQ$_Z$ pin.

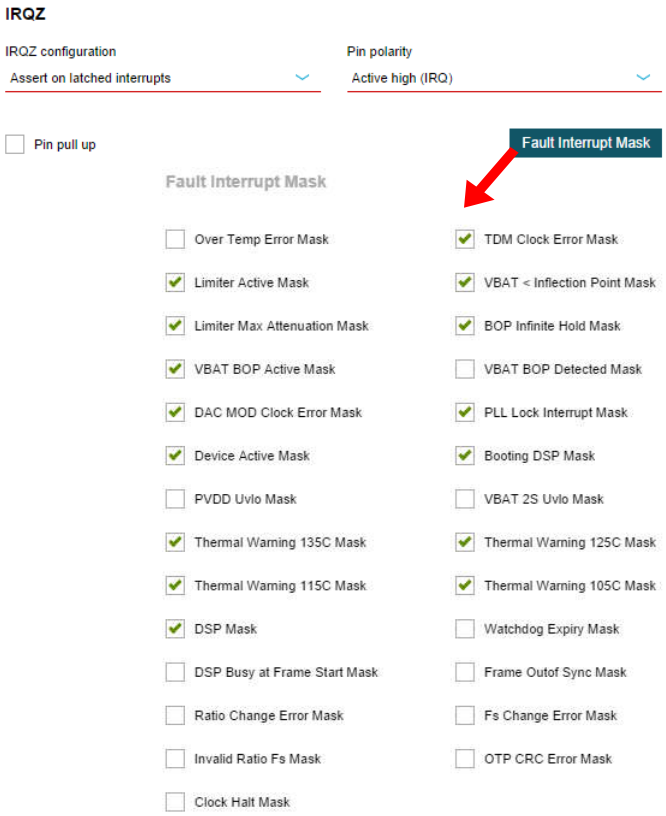


Figure 3-10. IRQ$_Z$ PPC3 Configuration

3.2.5 Tone Generator and Ultrasonic Chirp Generator

TAS2572 features internal tone generator that can be used independently from the digital audio playback. This sine wave generator can be used in the audible frequency band, or for ultrasonic applications as well. However, only one of these cases can be used at a time.

The tone generator is a simple tool that can be used to generate sine waves from 16 Hz up to 20 kHz, which amplitude is configured from -105dB up to 0 dB. There is an optional ramp effect that goes from 0 to 1 second in 10 millisecond steps.

The ultrasonic chirp generator can be used to play a pulsing sweep tone for sine waves with frequencies higher than 20 kHz. The frequency sweep is set by a start frequency and a bandwidth. The frequency change between each sweep step is defined from 100 Hz up to 2 kHz. The amplitude of the chirp can be configured from -80dB and up to -6dB. There is also an optional ramp effect before and after the chirp that goes up to 1 second in 10 millisecond steps. And finally, an Off period between chirps can be configured from 0 to 2 seconds in 10 millisecond steps as well.

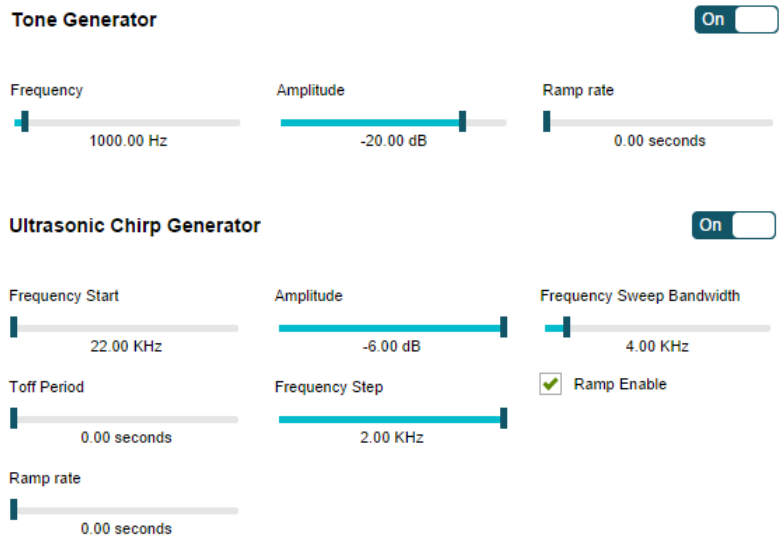


Figure 3-11. Tone and Ultrasonic Chirp Generator PPC3 Configuration

3.2.6 AVDD Bridge, Music Efficiency and Noise Gate

TAS2572 includes several features to improve the amplifier efficiency and prolong the play time in battery powered applications. All these features can be configured individually, and even disable if not required for the application

The noise gate feature can be used to shutdown the amplifier dynamically based on the input audio content amplitude. The threshold can be configured from -120dBFS up to -85dBFS and the hysteresis time from 10 milliseconds up to 1000 milliseconds.

Music efficiency mode enables very low consumption at low output power levels, the threshold is set to 50mW by default and the hysteresis timer can be configured up to 500 milliseconds.

AVDD bridge reduces the power consumption by driving the amplifier output from the AVDD 1.8V power supply, instead of the higher voltage from VBAT, when the output signal is below a set threshold up to 110 milliwatts. The hysteresis timer can be set from 0.1 millisecond up to 50 milliseconds.

In all cases, shorter hysteresis time improves efficiency with a tradeoff in potential audio artifacts due to the fast switching between the different playback/power modes.

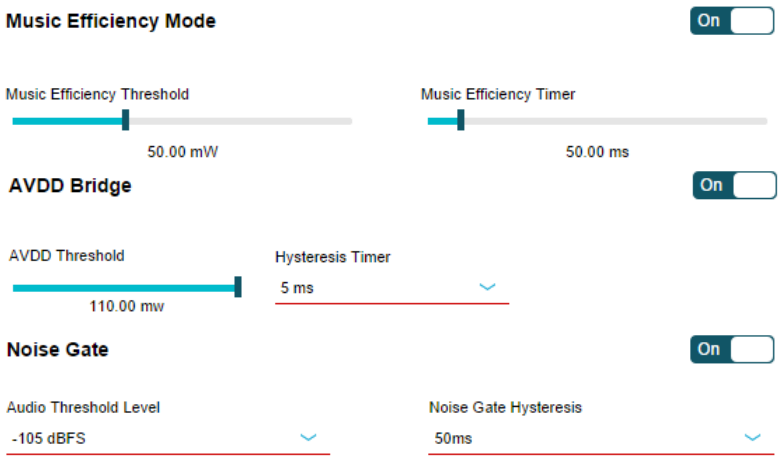


Figure 3-12. AVDD Bridge, Music Efficiency and Noise Gate PPC3 Configuration

3.2.7 Boost and Channel Gain

The channel gain section of the PPC3 GUI provides detailed settings for the integrated boost in TAS2572. Each of the controls are described in the following paragraphs.

Amplifier level is the gain of the amplifier, up to 16dBV the analog gain and beyond that some digital gain can be applied. 0dBV corresponds to 1Vrms.

Max boost voltage is one of the parameters used by the Class-H boost controller, and defines the maximum voltage the boost can step-up.

Peak current limit can be used to select the maximum current flowing through the boost inductor from VBAT supply into SW pin. This can be used when power requirement is lower and a smaller inductor is being used in the application. Similarly the boost soft start current limit is adjustable from no limit and up to 2.4A. One more setting related to the boost inductor is the inductance range, this is set to 1uH by default as this is the value included on the EVM; make sure to adjust this value if using a different inductance value on the end application.

Boost timing related configurations are included in the power-up step time, delay and boost release timer. Delay parameter sets the amount of samples the boost controllers looks ahead in the audio signal to adjust the boost level. Release timer sets the amount of samples required for the boost to reduce the level after the input signal reduces. Finally, the power-up time defines how fast the boost level keeps increasing when input signal does as well. Delay and Boost release timer are automatically calculated based on other parameters such as peak current limit.

PVDD Max and max POUT define limits for the boost in terms of current and voltage during boost operation. These parameters along with peaker current limit are used to calculate the boost timing settings.

All the mentioned settings are used for the internal boost controller, which can be configured as Class-H or Class-G using the Boost Mode control; further detail on these two power modes is covered on this related document. In addition to all that, the device can be configured to set the boost to be always on or always off, as well as fully disable the boost if higher power is not part of the use case, reducing in turn the device power consumption.

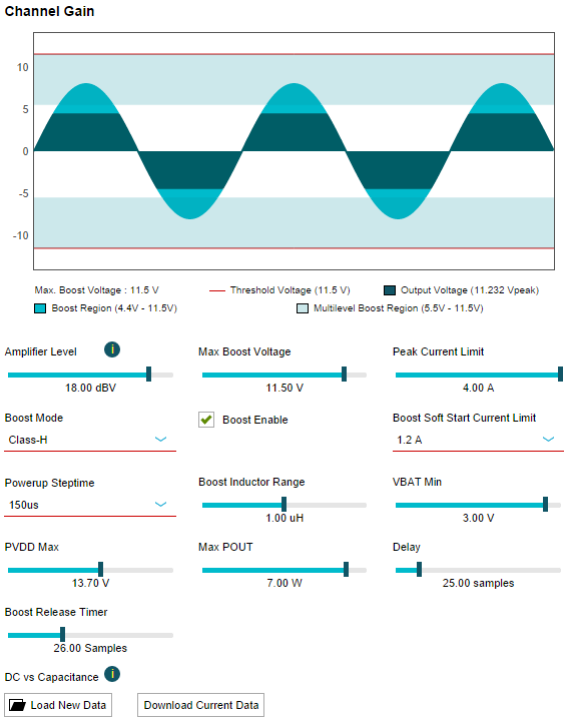


Figure 3-13. Playback and PCM PPC3 Configuration

4 Hardware Design Files

4.1 Schematics

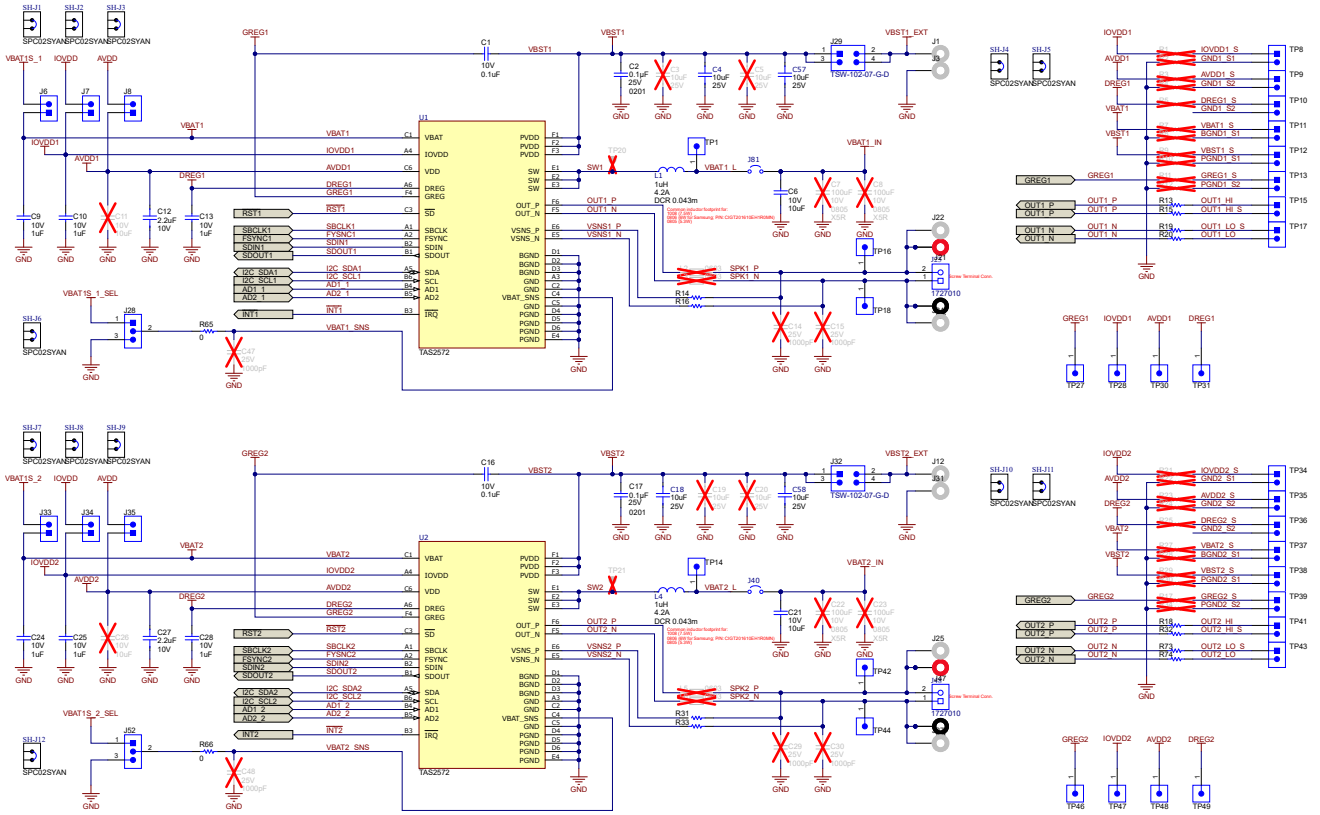


Figure 4-1. TAS2572EVM Schematic (Sheet 1 of 3)

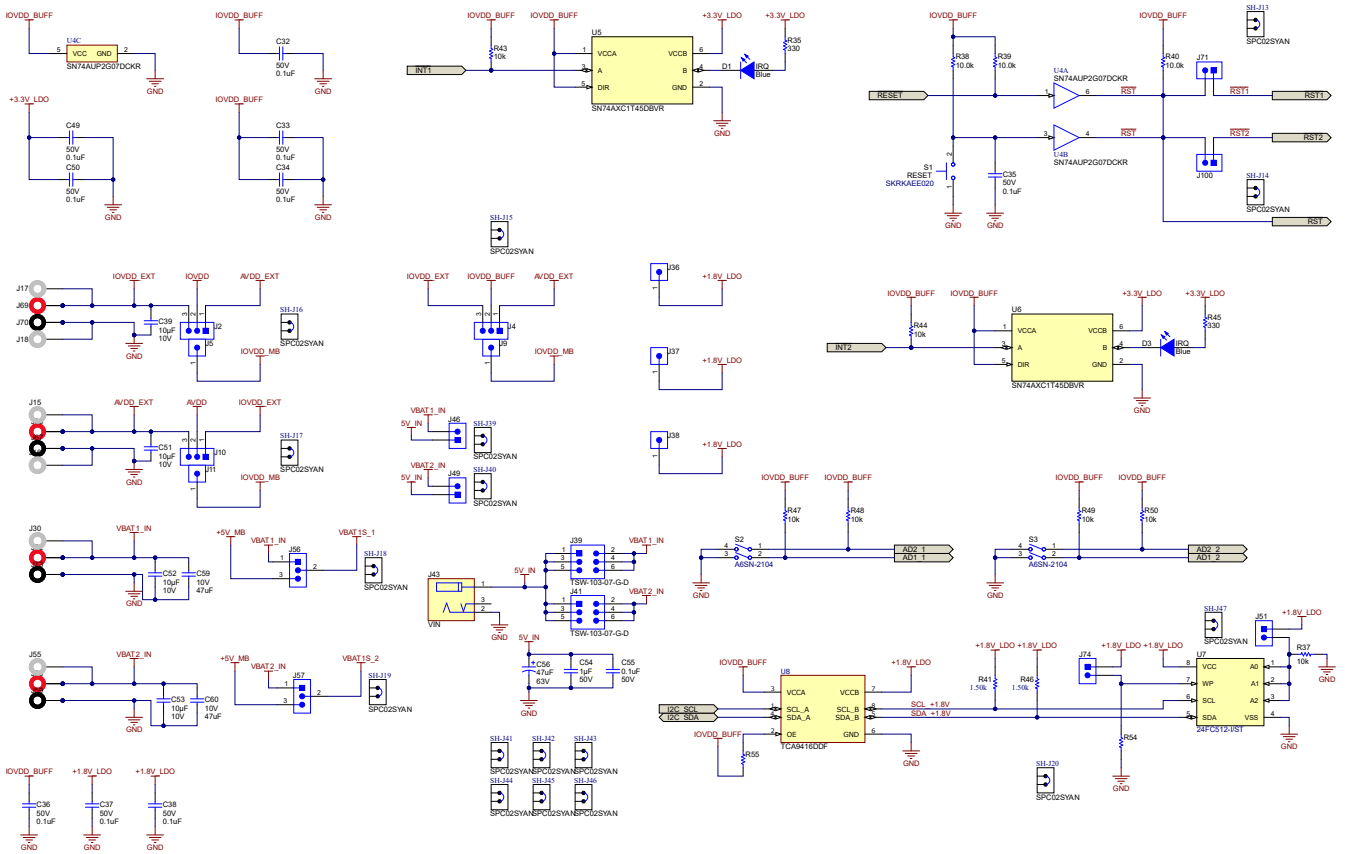


Figure 4-2. TAS2572EVM Schematic (Sheet 2 of 3)

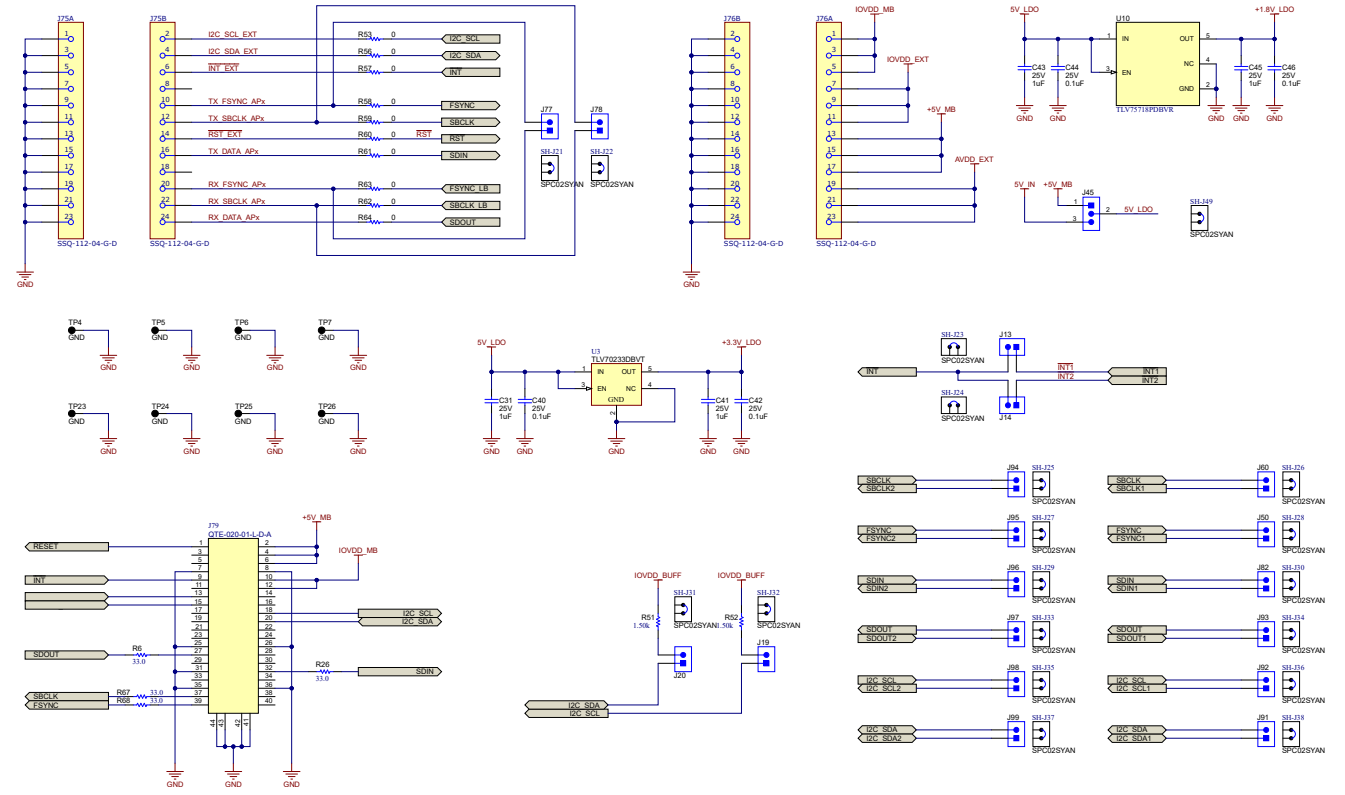


Figure 4-3. TAS2572EVM Schematic (Sheet 3 of 3)

4.2 PCB Layouts

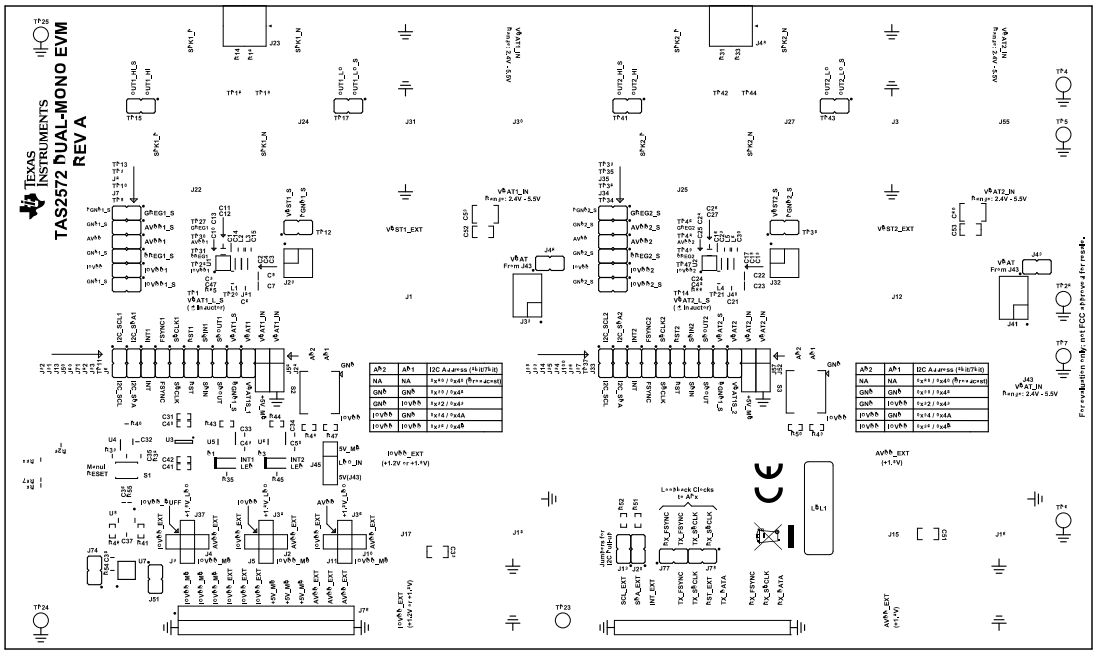


Figure 4-4. TAS2572EVM Top Overlay

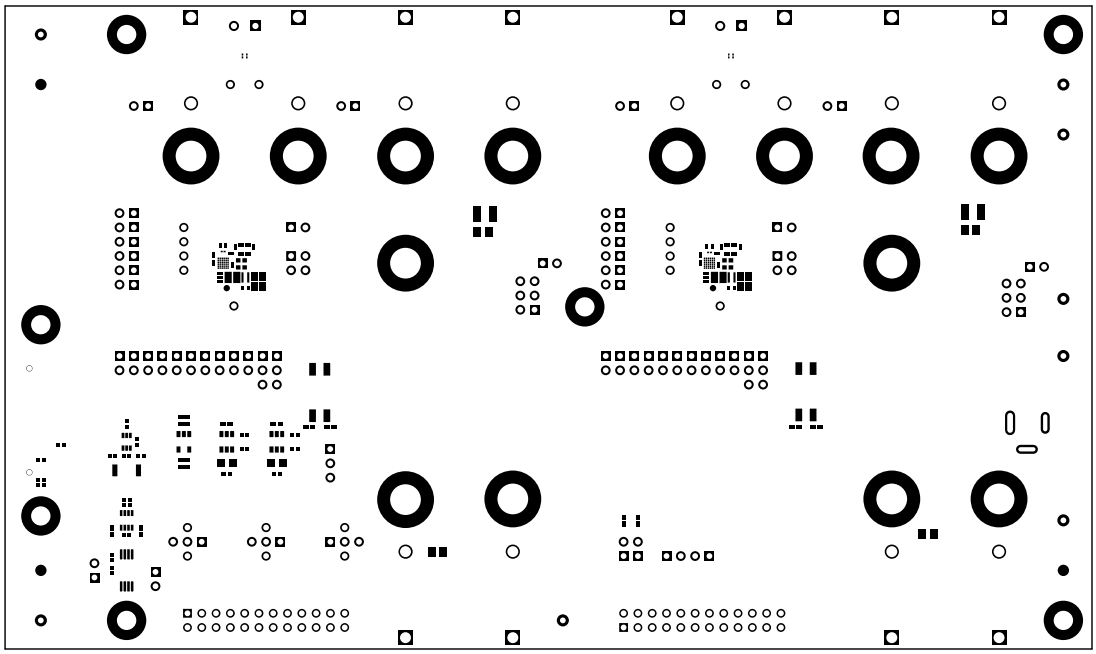


Figure 4-5. TAS2572EVM Top Solder Mask

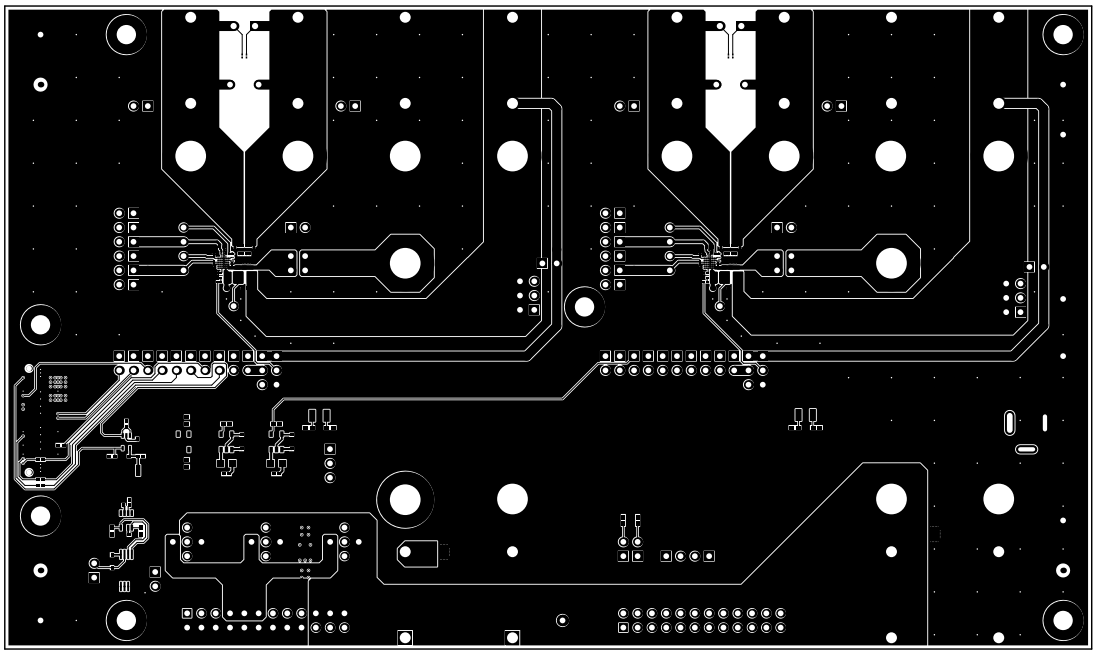


Figure 4-6. TAS2572EVM Top Layer

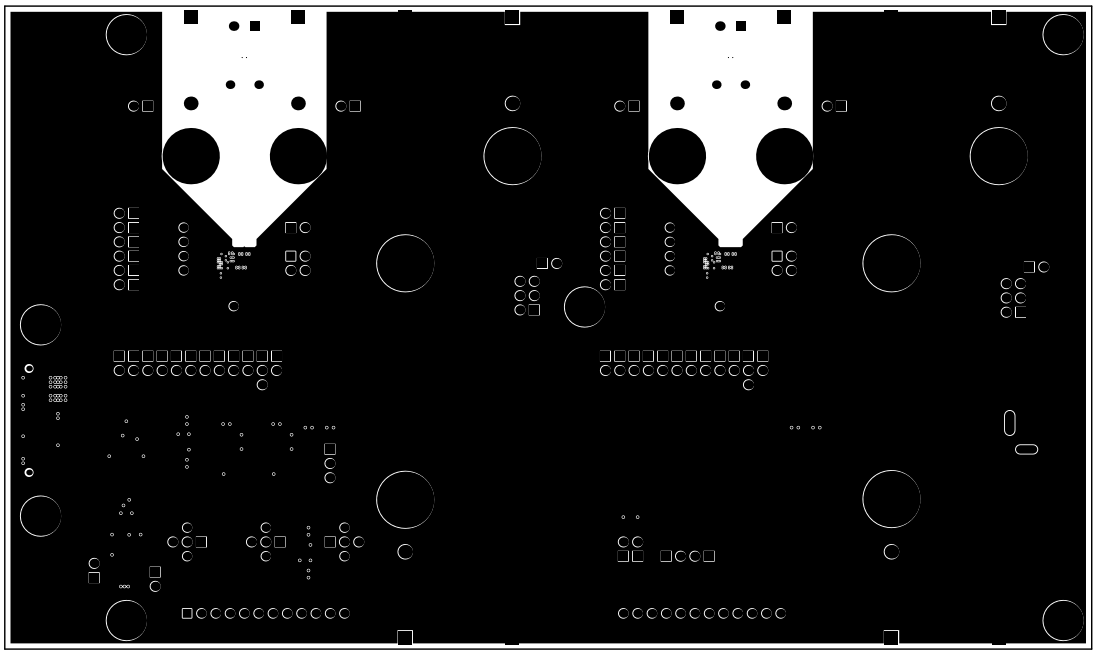


Figure 4-7. TAS2572EVM Layer 2

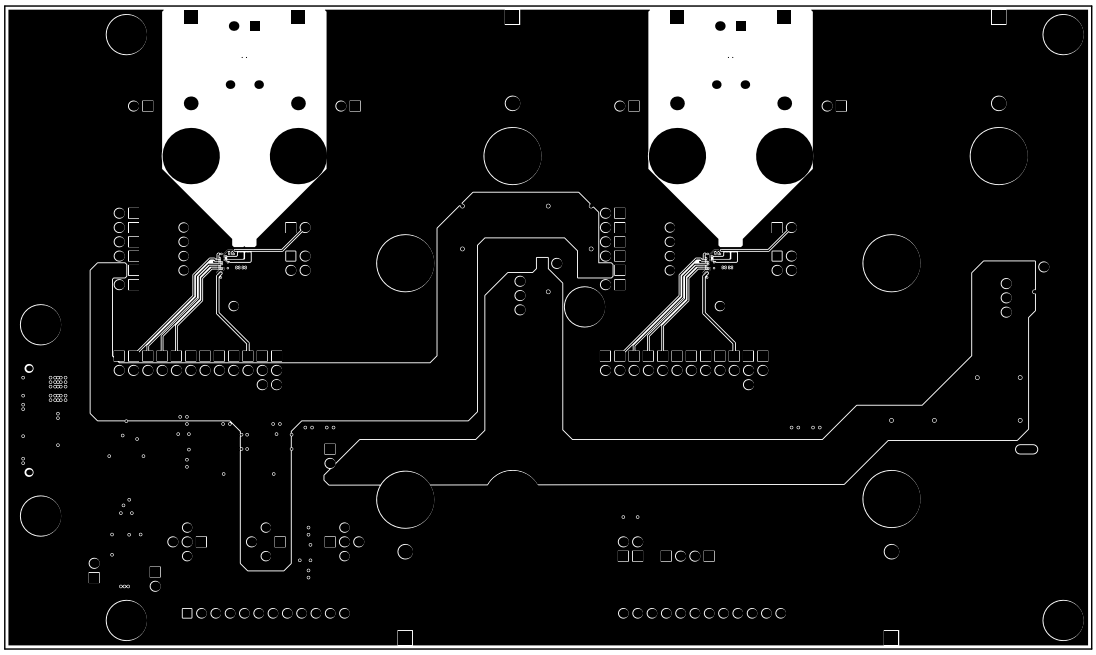


Figure 4-8. TAS2572EVM Layer 3

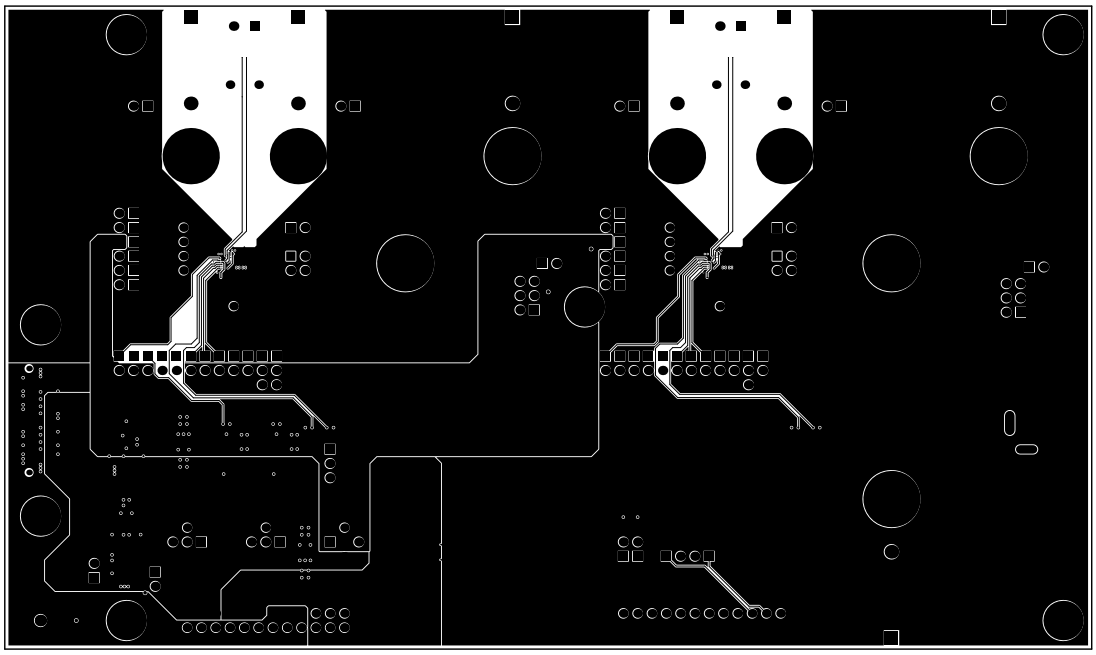


Figure 4-9. TAS2572EVM Layer 4

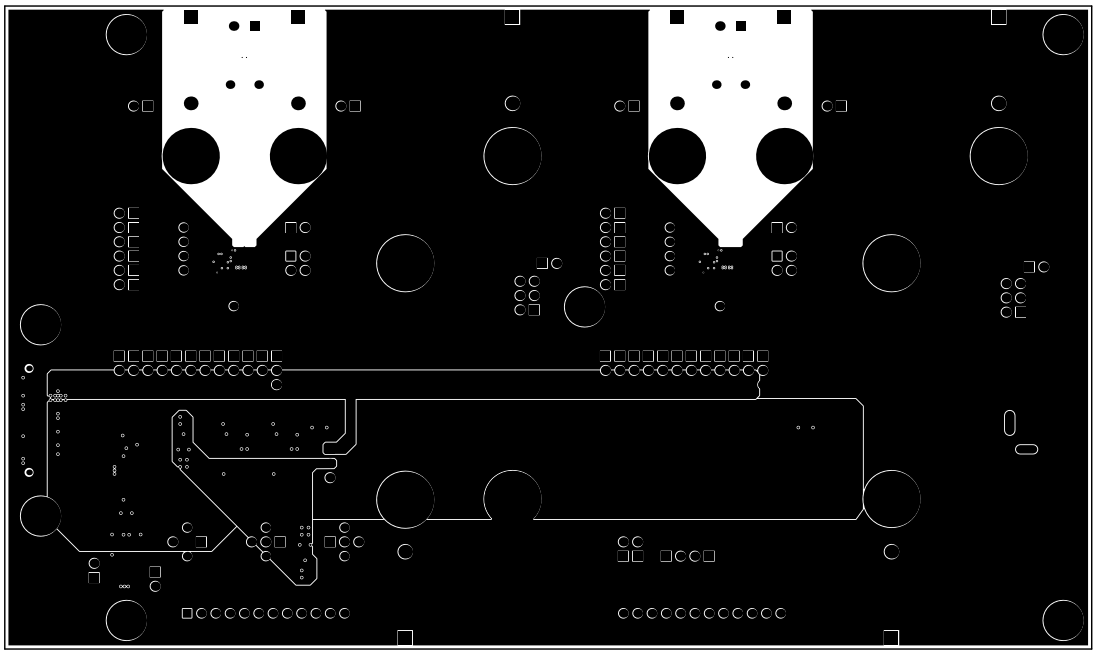


Figure 4-10. TAS2572EVM Layer 5

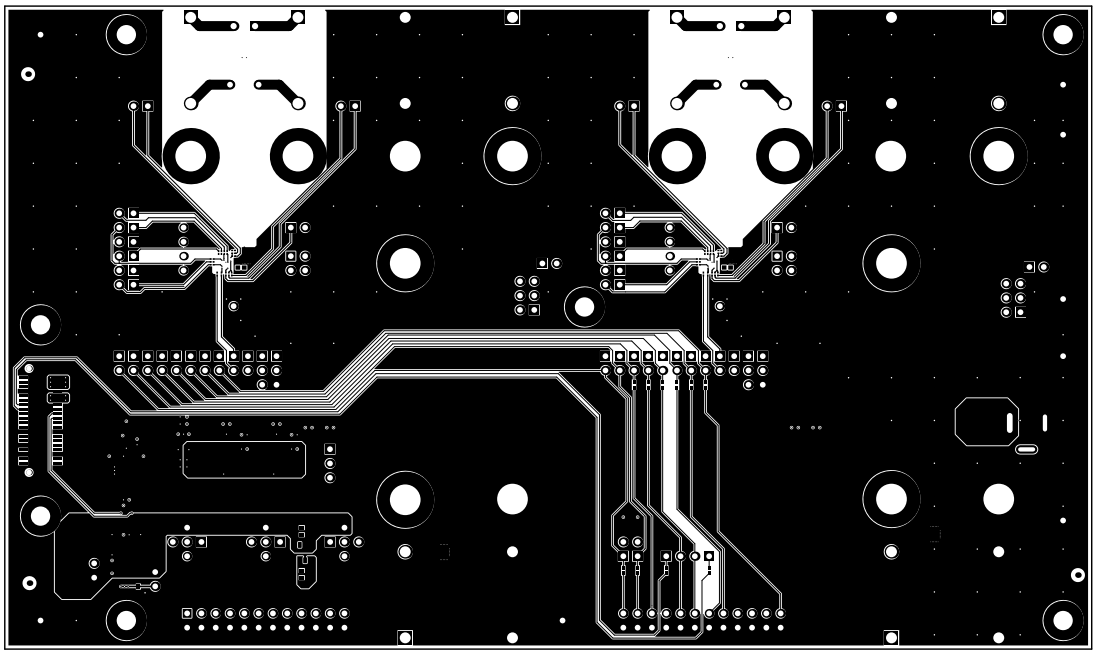


Figure 4-11. TAS2572EVM Bottom Layer

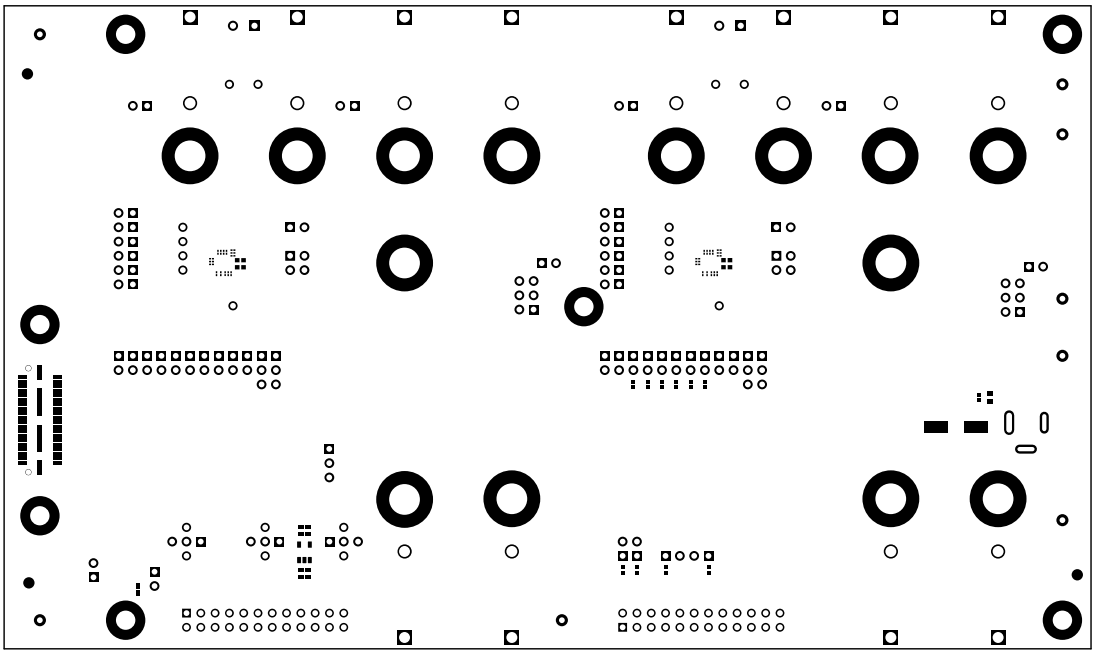


Figure 4-12. TAS2572EVM Bottom Solder Mask

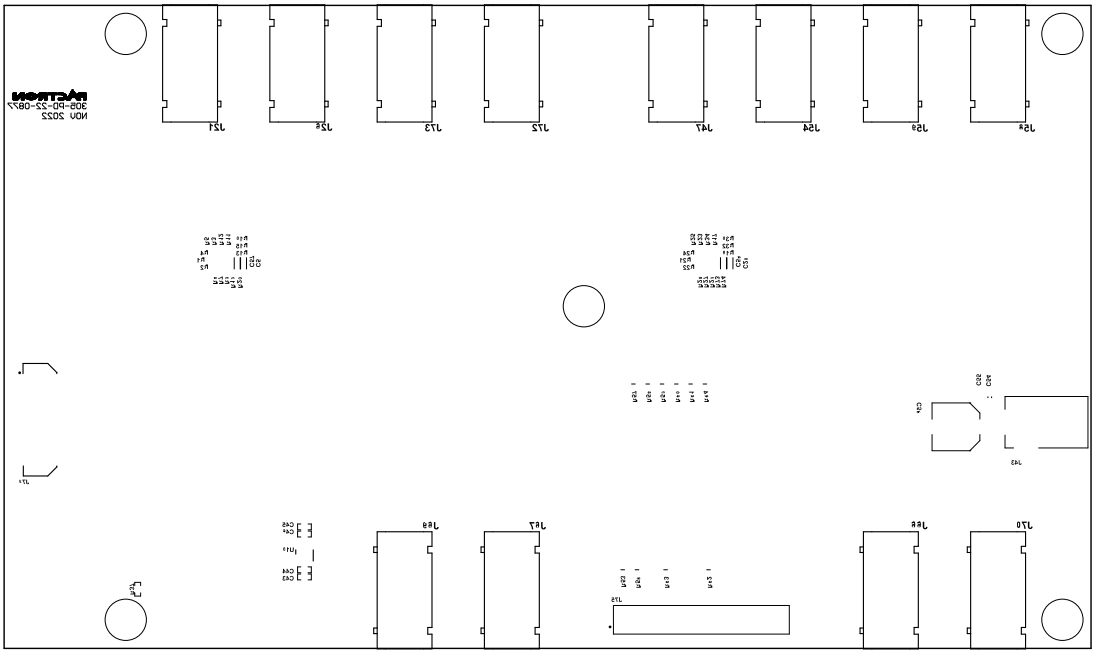


Figure 4-13. TAS2572EVM Bottom Overlay

4.3 Bill of Materials

Table 4-1 lists the bill of materials for the EVM.

Table 4-1. Bill of Materials

Designator	Qty	Value	Description	Package Reference	Part Number	Manufacturer	Alternate Part Number	Alternate Manufacturer
C1, C16	2	0.1uF	CAP, CERM, 0.1 uF, 10 V, +/- 10%, X5R, 0201	0201	CL03A104KP3NNNC	Samsung Electro-Mechanics		
C2, C17	2	0.1uF	CAP, CERM, 0.1 µF, 10 V,+/- 10%, X5R, 0201	0201		SAMSUNG ELECTRO-MECHANICS		
C4, C18, C57, C58	4	10 µF	Cap Ceramic 10 uF 25 V X5R ±20% Pad SMD 0603 +85°C T/R	0603	CL10A106MA8NRNC	Samsung		
C6, C21	2	10uF	CAP, CERM, 10 uF, 10 V, +/- 20%, X5R, 0402	0402	CL05A106MP5NUNC	Samsung Electro-Mechanics		
C9, C10, C13, C24, C25, C28	6	1uF	CAP, CERM, 1 uF, 10 V, +/- 20%, X5R, 0201	0201	CL03A105MP3NSNC	Samsung Electro-Mechanics		
C12, C27	2	2.2µF	Cap Ceramic 2.2uF 10 V X5R ±20% Pad SMD 0201 +85°C T/R	0201	CL03A225MP3CRNC	Samsung		
C31, C41, C43, C45	4	1uF	CAP, CERM, 1 uF, 25 V, +/- 10%, X5R, 0402	0402	C1005X5R1E105K050BC	TDK		
C32, C33, C34, C35, C36, C37, C38, C49, C50, C55	10	0.1uF	CAP, CERM, 0.1 uF, 50 V, +/- 10%, X7R, 0402	0402	C1005X7R1H104K050BB	TDK		
C39, C51, C52, C53	4	10uF	CAP, CERM, 10 µF, 10 V,+/- 10%, X7R, AEC-Q200 Grade 1, 0805	0805	GCJ21BR71A106KE01L	MuRata		
C40, C42, C44, C46	4	0.1uF	CAP, CERM, 0.1 uF, 25 V, +/- 10%, X5R, 0402	0402	GRM155R61E104KA87D	MuRata		
C54	1	1uF	CAP, CERM, 1 µF, 50 V,+/- 20%, X5R, AEC-Q200 Grade 3, 0603	0603	CGA3E3X5R1H105M080AB	TDK		
C56	1	47uF	CAP, AL, 47 uF, 63 V, +/- 20%, 0.65 ohm, AEC-Q200 Grade 2, SMD	SMT Radial F	EEE-FK1J470P	Panasonic		
C59, C60	2	47uF	CAP, CERM, 47 uF, 10 V, +/- 20%, X7R, 1210	1210	GRM32ER71A476ME15L	MuRata		
D1, D3	2	Blue	LED, Blue, SMD	LED_0805	LTST-C170TBKT	Lite-On		
H1, H2, H3, H4, H13	5				HNSS440	B&F Fastener Supply		
H5, H6	2		8 MM RD X 6 MM X M3	10x10mm	M3561-SS	RAF Electronic Hardware		

Table 4-1. Bill of Materials (continued)

Designator	Qty	Value	Description	Package Reference	Part Number	Manufacturer	Alternate Part Number	Alternate Manufacturer
H7, H8, H9, H10, H14	5		Standoff; 1/4 Hex Male/female; 4-40 Thread; Stainless Steel; .750LENGTH	HEX_STANDOFF	4538-440-SS	RAF Electronic Hardware		
J1, J3, J12, J15, J16, J17, J18, J22, J24, J25, J27, J30, J31, J55	14		Standard Banana Jack, Uninsulated, 5.5mm	Keystone_575-4	575-4	Keystone		
J2, J4, J10, J28, J45, J52, J56, J57	8		Header, 100mil, 3x1, Gold, TH	PBC03SAAN	PBC03SAAN	Sullins Connector Solutions		
J5, J9, J11, J36, J37, J38, TP1, TP14, TP16, TP18, TP27, TP28, TP30, TP31, TP42, TP44, TP46, TP47, TP48, TP49	20		Header, 2.54mm, 1x1, Gold, TH	Header, 2.54mm, 1x1, TH	TSW-101-08-G-S	Samtec		
J6, J7, J8, J13, J14, J19, J20, J33, J34, J35, J46, J49, J50, J51, J60, J71, J74, J77, J78, J82, J91, J92, J93, J94, J95, J96, J97, J98, J99, J100, TP8, TP9, TP10, TP11, TP12, TP13, TP15, TP17, TP34, TP35, TP36, TP37, TP38, TP39, TP41, TP43	46		Header, 100mil, 2x1, Gold, TH	Sullins 100mil, 1x2, 230 mil above insulator	PBC02SAAN	Sullins Connector Solutions		
J21, J47, J58, J66, J69, J72	6		Standard Banana Jack, insulated, 10 A, red	571-0500	571-0500	DEM Manufacturing		
J23, J48	2		Conn Term Block, 2POS, 3.81mm, TH	2POS Terminal Block	1727010	Phoenix Contact		
J26, J54, J59, J67, J70, J73	6		Standard Banana Jack, insulated, 10 A, black	571-0100	571-0100	DEM Manufacturing		
J29, J32	2		Header, 100mil, 2x2, Gold, TH	2x2 Header	TSW-102-07-G-D	Samtec		

Table 4-1. Bill of Materials (continued)

Designator	Qty	Value	Description	Package Reference	Part Number	Manufacturer	Alternate Part Number	Alternate Manufacturer
J39, J41	2		Header, 100mil, 3x2, Gold, TH	3x2 Header	TSW-103-07-G-D	Samtec		
J40, J81	2		Jumper-0.015x0.072-0.04p	JUMPER-0.015x0.072-0.04p	Jumper-0.015x0.072-0.04p	Jumper		
J43	1		Power Jack, mini, 2.5mm OD, R/A, TH	Jack, 14.5x11x9mm	RAPC712X	Switchcraft		
J75, J76	2			CONN_RCPT24	SSQ-112-04-G-D	Samtec		
J79	1		Connector, Header, High Speed, 20 pairs, SMT	QTE-020-01-X-D-A	QTE-020-01-L-D-A	Samtec		
L1, L4	2	1uH	POWER INDUCTOR 1uH, ±20%, Isat 4.2A, Itemp 4.1A, DCR Max 0.043Ω, 0806	0806	CIGT201610EH1R0MN	Samsung		
R6, R26, R67, R68	4	33	RES, 33.0, 1%, 0.1 W, 0402	0402	ERJ-2RKF33R0X	Panasonic		
R13, R14, R15, R16, R18, R19, R20, R31, R32, R33, R73, R74	12		RES SMD 0 OHM JUMPER 1/20W 0201	0201 (0603 Metric)	RC0201JR-070RL	Yageo		
R35, R45	2	330	RES, 330, 1%, 0.1 W, AEC-Q200 Grade 0, 0402	0402	ERJ-2RKF3300X	Panasonic		
R37, R43, R44, R47, R48, R49, R50	7	10k	RES, 10 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0402	0402	ERJ-2GEJ103X	Panasonic		
R38, R39, R40, R54, R55	5	10.0k	RES, 10.0 k, 1%, 0.063 W, 0402	0402	RC0402FR-0710KL	Yageo America		
R41, R46, R51, R52	4	1.50k	RES, 1.50 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	RMCF0402FT1K50	Stackpole Electronics Inc		
R53, R56, R57, R58, R59, R60, R61, R62, R63, R64	10	0	RES, 0, 5%, 0.063 W, 0402	0402	ERJ-2GE0R00X	Panasonic		
R65, R66	2	0	RES, 0, 5%, 0.05 W, 0201	0201	CRCW02010000Z0ED	Vishay-Dale		
S1	1		Switch, SPST-NO, 0.05 A, 12 VDC, SMT	3.9x2.9mm	SKRKAEE020	Alps		
S2, S3	2		Switch, Slide, 2 SPST, Off-On, 0.025 A, 24 VDC, SMT	7x7.5mm	A6SN-2104	Omron Electronic Components		

Table 4-1. Bill of Materials (continued)

Designator	Qty	Value	Description	Package Reference	Part Number	Manufacturer	Alternate Part Number	Alternate Manufacturer
SH-J1, SH-J2, SH-J3, SH-J4, SH-J5, SH-J6, SH-J7, SH-J8, SH-J9, SH-J10, SH-J11, SH-J12, SH-J13, SH-J14, SH-J15, SH-J16, SH-J17, SH-J18, SH-J19, SH-J20, SH-J21, SH-J22, SH-J23, SH-J24, SH-J25, SH-J26, SH-J27, SH-J28, SH-J29, SH-J30, SH-J31, SH-J32, SH-J33, SH-J34, SH-J35, SH-J36, SH-J37, SH-J38, SH-J39, SH-J40, SH-J41, SH-J42, SH-J43, SH-J44, SH-J45, SH-J46, SH-J47, SH-J49	48	1x2	Shunt, 100mil, Flash Gold, Black	Closed Top 100mil Shunt	SPC02SYAN	Sullins Connector Solutions		
TP4, TP5, TP6, TP7, TP23, TP24, TP25, TP26	8		Test Point, Miniature, Black, TH	Black Miniature Testpoint	5001	Keystone		
U1, U2	2		SN012578	DSBGA36	TAS2572	Texas Instruments		
U3	1		Single Output LDO, 300 mA, Fixed 3.3 V Output, 2 to 5.5 V Input, with Low IQ, 5-pin SOT-23 (DBV), -40 to 125 degC, Green (RoHS & no Sb/Br)	DBV0005A	TLV70233DBVT	Texas Instruments		
U4	1		Low-Power Dual Buffer/ Driver With Open-Drain Outputs, DCK0006A (SOT-SC70-6)	DCK0006A	SN74AUP2G07DCKR	Texas Instruments		
U5, U6	2		Single-Bit Dual-Supply Bus Transceiver, DBV0006A (SOT-23-6)	DBV0006A	SN74AXC1T45DBVR	Texas Instruments		Texas Instruments

Table 4-1. Bill of Materials (continued)

Designator	Qty	Value	Description	Package Reference	Part Number	Manufacturer	Alternate Part Number	Alternate Manufacturer
U7	1		512K I2C Serial EEPROM, TSSOP	TSSOP-8	24FC512-I/ST	Microchip		
U8	1		TCA9416DDF	SOT23-8	TCA9416DDF	Texas Instruments		
U10	1		1 A low-Iq small-size low-dropout (LDO) regulator, DBV0005A (SOT-23-5)	DBV0005A	TLV75718PDBVR	Texas Instruments	TLV75718PDBVT	Texas Instruments
C3, C5, C19, C20	0	10µF	Cap Ceramic 10 uF 25 V X5R ±20% Pad SMD 0603 +85°C T/R	0603	CL10A106MA8NRNC	Samsung		
C7, C8, C22, C23	0		CAP, CERM, 47 uF, 10 V, +/- 20%, X5R, 0805	0805		TDK		
C11, C26	0	10uF	CAP, CERM, 10 uF, 10 V, +/- 20%, X5R, 0402	0402	CL05A106MP5NUNC	Samsung Electro-Mechanics		
C14, C15, C29, C30, C47, C48	0	1000 pF	CAP, CERM, 1000 pF, 25 V, +/- 10%, X5R, 0201	0201	C0603X5R1E102K030BA	TDK		
H11, H12	0		Standoff, Male/Male Thread, 5.15 mm, M3 x 0.5	Standoff	SO-0515-02-02-01	Samtec		
L2, L3, L5, L6	0	120 ohm	Ferrite Bead, 120 ohm @ 100 MHz, 2 A, 0603	0603	742792625	Wurth Elektronik		
R1, R2, R3, R4, R5, R7, R8, R9, R10, R11, R12, R17, R21, R22, R23, R24, R25, R27, R28, R29, R30, R34	0		RES SMD 0 OHM JUMPER 1/20W 0201	0201 (0603 Metric)	RC0201JR-070RL	Yageo		

5 Additional Information

5.1 Trademarks

Windows® is a registered trademark of Microsoft Corporation.
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6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (July 2023) to Revision A (March 2026)	Page
• Initial public release	1

STANDARD TERMS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an “EVM” or “EVMs”) to the User (“User”) in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.

   1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM (“Software”) shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms that accompany such Software

   1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.

2 *Limited Warranty and Related Remedies/Disclaimers*:

   2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.

   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

WARNING

Evaluation Kits are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.

User shall operate the Evaluation Kit within TI’s recommended guidelines and any applicable legal or environmental requirements as well as reasonable and customary safeguards. Failure to set up and/or operate the Evaluation Kit within TI’s recommended guidelines may result in personal injury or death or property damage. Proper set up entails following TI’s instructions for electrical ratings of interface circuits such as input, output and electrical loads.

NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGREDATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 *Regulatory Notices:*

3.1 *United States*

3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

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