Functional Safety Information

LMT84-Q1
Functional Safety FIT Rate, FMD and Pin FMA

Table of Contents

Trademarks

1 Overview

This document contains information for the LMT84-Q1 (SOT (5) package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

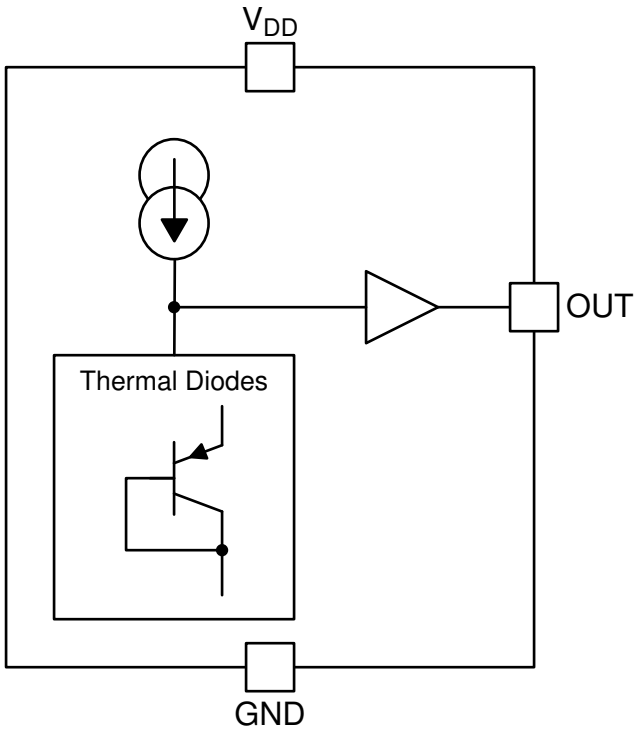

Figure 1-1. Functional Block Diagram

The LMT84-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for the LMT84-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	4
Die FIT rate	2
Package FIT rate	2

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 1mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): From table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	20 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the LMT84-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
VOUT open (Hi-Z)	15
VOUT short to VDD	20
VOUT short to GND	20
VOUT not in specification	45

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the LMT84-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the LMT84-Q1 pin diagram. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the LMT84-Q1 datasheet.

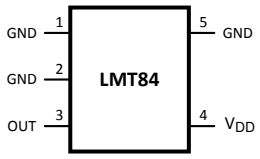

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- The bypass capacitor on the input voltage pin of 0.01µF.
- The series resistors are sized to limit the input currents to the analog inputs to <5mA.
- Capacitive loading on the output pin is limited to 1100pF.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
GND	1	There is no effect on the device and the device operates normally.	D
GND	2	There is no effect on the device and the device operates normally.	D
OUT	3	The output is stuck low. No analog output is present on device.	B
V_{DD}	4	The device is not powered and not functional. Observe that the absolute maximum ratings for all pins of the device are met; otherwise, device damage is plausible.	A
GND	5	There is no effect on the device and the device operates normally.	D

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
GND	1	The expected analog output from the device can be altered.	B
GND	2	The expected analog output from the device can be altered.	B
OUT	3	There is no effect on the device and the device operates normally.	D
V_{DD}	4	The expected analog output from the device can be altered.	B
GND	5	The expected analog output from the device can be altered.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
GND	1	GND	There is no effect on the device and the device operates normally.	D
GND	2	OUT	Device functionality is undetermined. Observe that the absolute maximum ratings for all pins of the device are met,; otherwise, device damage is plausible.	A
OUT	3	V_{DD}	The output is stuck low. No analog output is present on device.	B
V_{DD}	4	GND	Device is not powered and not functional. Observe that the absolute maximum ratings for all pins of the device are met; otherwise, device damage is plausible.	A
GND	5	GND	There is no effect on the device and the device operates normally.	D

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
GND	1	The expected analog output from the device can be altered.	B
GND	2	Device functionality is undetermined. Observe that the absolute maximum ratings for all pins of the device are met; otherwise, device damage is plausible.	A
OUT	3	The device output is stuck high.	B
V_{DD}	4	There is no effect on the device and the device operates normally.	D
GND	5	The expected analog output from the device can be altered.	D

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
April 2026	*	Initial Release

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