Application Note

Sampling the DC Bin: Designing DC-Coupled Amplifier Frontends for High-Speed ADCs

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ABSTRACT

Sampling down in that DC region with a high-speed, RF converter can sometimes feel like a mysterious task, but it is much simpler. Many high-speed converter datasheets don't really give indication that DC sampling is possible, as most datasheet performance specifications for high-speed and RF converters start around 10MHz, which is close to DC, but not truly. The conundrum here is that high-speed typically means AC coupling. The converter datasheet may still have some DC specifications remaining, as many of them are falling by the wayside or just plain left out, even better they are getting more ambiguous to interpret. Who would want to sample the DC bin when the ADC's focus marketplace or application is direct K-band sampling? In this paper, these thoughts are dispelled and a step-by-step guide is provided to make the next DC coupling high-speed signal chain design attempt fruitful!

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Trademarks

1 Introduction

In many scenarios, the designer needs to use a high-speed converter to do two things: sample at higher speeds (Mega- or Giga-samples covering some portion of an RF frequency region), as well as DC. The DC bin can give the designer some useful information too. This can be a sensor level or DC value on a high frequency pulsed waveform, where the DC pedestal within that pulse gives the system some useful information to make decisions at a higher level.

If DC coupling is needed, this typically means the designer cannot use a transformer or balun frontend in the design, which is popular and simple to design with. Some baluns and transformers can have a low frequency range, down into the very low-kHz range, however, sampling true DC just is not possible with a balun or transformer. See Figure 1-1 for a quick snapshot of a few transformers and baluns lower end frequency response, that are on the market today down to the 9kHz range (test equipment limited).

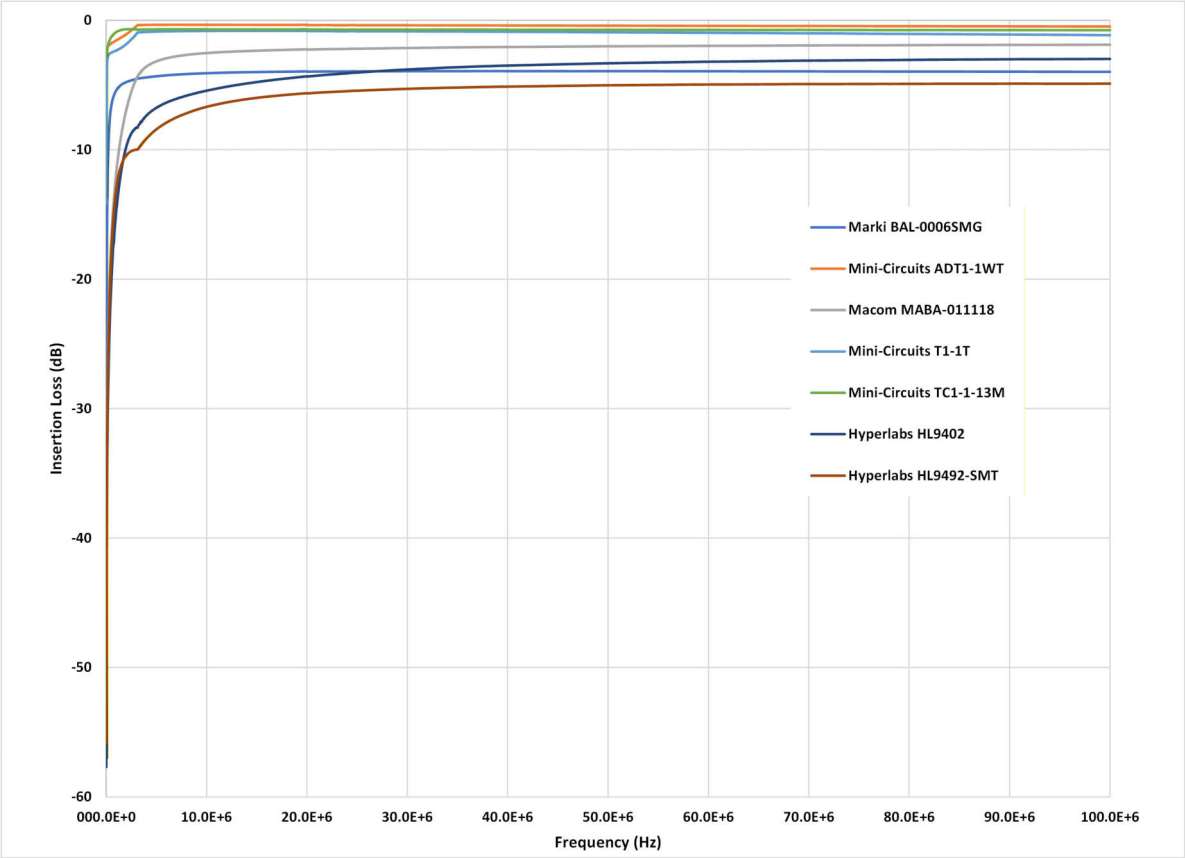

Figure 1-1. Lowend Frequency Response of the Transformer and Balun

At 9kHz (the test equipment limitation for the VNA used to measure the S21 response of these baluns) many of the balun's lowend responses are in the range of -10 to -50dB attenuation or more. Therefore, this is not necessarily a practical design if the user plans to sample true DC.

This typically forces the designer to use an amplifier to couple to the ADC and maintain that DC value. The FDA, or fully differential amplifier, is commonly used instead to preserve the DC value and pass the value along to the ADC for sampling, however, amplifiers do come with some caveats. First, ADCs cannot be paired with just any FDA and enable DC coupling. Here are a few things to check for in the datasheet of the amplifier to make sure the ADC can do the job:

1. The output stage of the amplifier allows for DC coupling.
2. The power supply of the amplfier compliance range is sufficient.
3. The input or output common mode range of the amplifier is sufficient, this is typically related to point two.

Next, the designer can also have a single-ended signal chain, before the signal chain connects to the FDA. If so, the next thing to check is if the FDA can be configured for a single-ended (SE) input and differential (DIFF) output. Sometimes FDAs only allow for DIFF in and DIFF out signal configurations.

If this sort of information is not shown in the FDA datasheet, contact the factory vendor and verify.

2 Find the Right Amplifier

Now that we know that users are going to use an FDA to make the DC coupling interface happen, this document is going to explore a few of the finer points that were noted above.

First, check the output stage of the amplifier. Unless this does not specifically say in the datasheet that the output stage cannot DC couple, check if the output stage has a few pullup or pulldown chokes in the application section of the datasheet. If so, most likely the FDA has an open collector output stage and the low-end has a limited response to a few kHz but not DC.

Second, check the compliance region of the FDA. What does this mean? This means a few things that are a bit tied together. Check the analog input common mode voltage (VCM) of the ADC needs; this is typically in the datasheet of the ADC under the analog input specification tables. Typically noted as VCM in the specification tables. There also can be a VCM pin on the ADC that allows the user to tie this node back to the analog inputs to keep the common mode voltage stable. This is the VCM pin of the ADC, and can also be used to drive the outputs of the FDA to a certain output common mode voltage or VOCM pin located on the FDA. Ultimately, the analog input common mode voltage of the ADC needs to be compliant and support the same VOCM voltage range of the FDA. This information is typically found in the datasheet of the FDA, in the specification tables.

Typically, the VOCM range, is tied to the power supply range or supplies used with the amplifier. Some FDAs are only single supply and some can have dual supply capability. The dual supply amplifier variety is definitely more flexible. The reason this is, because typically output common mode of the FDA or VOCM *floats* to half the supply, when this pin is not driven specifically with a voltage. For example, a 0 to 5V FDA, has a 2.5 VOCM or for a 0 to 3.3V FDA, has a 1.65 VOCM. Now for a dual supply FDA, the flexibility also lies in the range of the supply. For example, you can use the LMH5401 FDA. This FDA has a 5V compliance range, but has a dual supply option. This allows for the amplifier to run on 5V VCC and 0V VSS (ground) or 2.5V VCC and -2.5V VSS…or anywhere in-between, such as 4V VCC and -1V VSS. As long as the sum of the two power supply domains are within the compliance range of 5V or less. See Figure 2-1 for a compliance range example as just described.

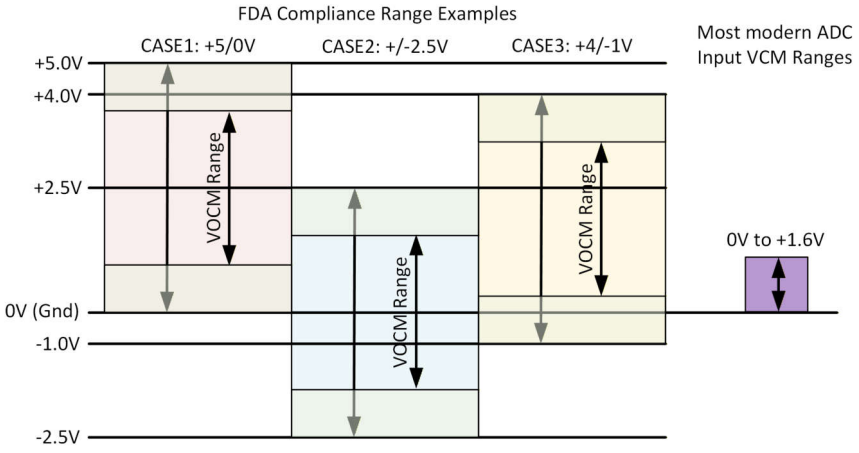

Figure 2-1. LMH5401 Compliance Range Examples vs. Current ADC VCM Ranges

Notice the VOCM range of the amplifier is within the voltage compliance range of the amplifier which allows for various signal levels to be manageable through the amplifier.

3 Understand the ADC and Type

The analog input common mode specifications of the ADC is directly related to the ADC's architecture type. Most high-speed, RF converters fall into two groups. They have an internal buffer stage directly connecting to the analog input pins or they do not have this internal buffer, and the analog input pins connect directly to the internal sampling switch, otherwise, called an unbuffered input. If the converter is buffered, the analog inputs are self-biased and typically have a VCM of half of the analog power supply plus a diode drop above, or AVDD/2+0.7V. Whereas unbuffered converters do not have an internal buffer and require the analog input pins of the ADC to be biased by the VCM pin which must connect into the analog frontend circuit or by biased by the connected FDA. Typically, unbuffered ADCs require a common mode voltage of the analog input pin of halt the analog supply, or AVDD/2.

The main difference between the two types of ADCs, is that a buffered converter is self-biased, meaning the analog inputs *float* to AVDD/2+0.7V and an unbuffered converter needs a bit of help. The analog inputs need a VCM connection on each of the analog input pins to bias those inputs appropriately. There are various ways to implement this *tie* into the analog input frontend, and it is important to follow the datasheet recommendation the evaluation board method for best practice. See Figure 3-1 to understand some general differences between buffered and unbuffered ADC types and AC versus DC coupling connections with FDAs.

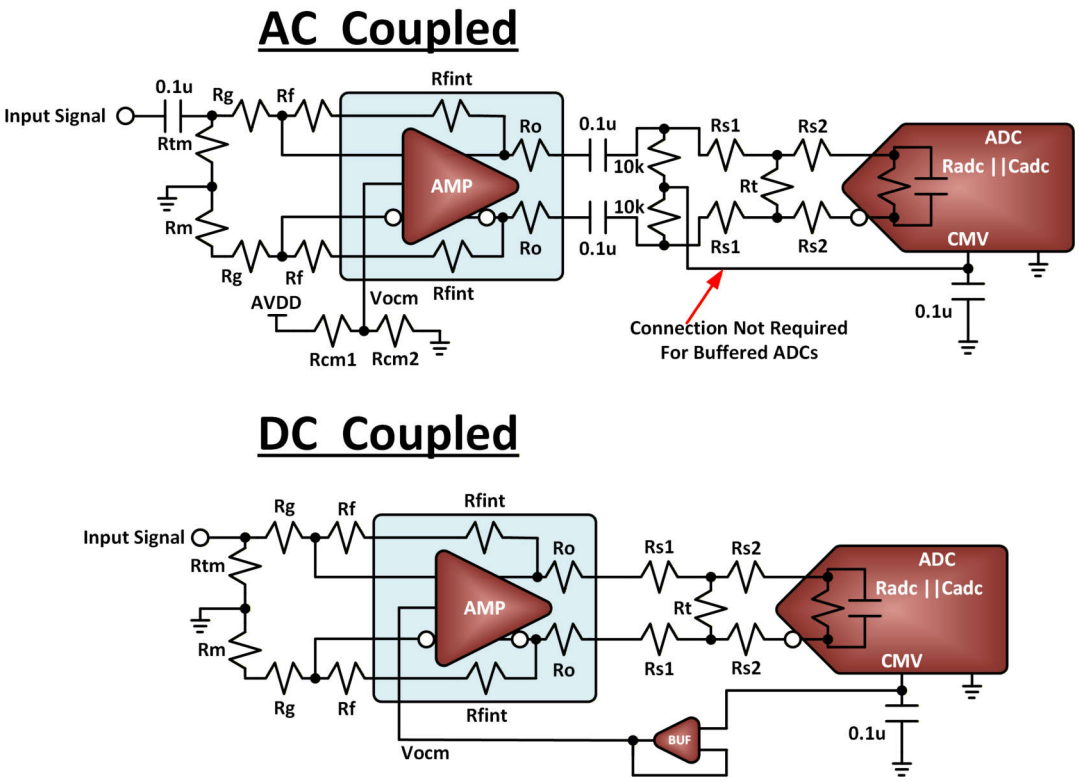

Figure 3-1. Analog Input ADC Connections for Buffered vs. Unbuffered and AC vs. DC Coupled Frontends

Many high-speed ADCs and DACs are being designed and developed on very small process nodes, such as 65nm and lower. This means the power supply nodes of the ADC are getting smaller, such as +1.1V AVDD and even less. This forces the analog input common mode range to be within a sub-volt range or lower. For example, many ADCs on the market today have a VCM that is in the range of +0.95V or smaller. This means the FDA must also have an allowable VOCM output range for both the amplifier and ADC to work properly together. See Figure 3-2 for an example of an ADC's differential input signaling around a 1V common mode voltage.

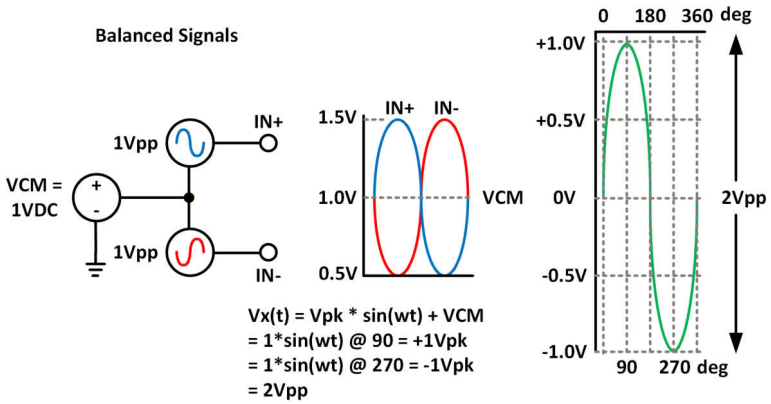

Figure 3-2. ADC Differential Input Signal Example.

Notice the analog input VCM of the converter is important and needs to be satisfied by the external input network frontend, for exanple, – FDA, or otherwise, the converter has performance issues.

By dividing up the signal swing differentially, this interface enables the user to maintain higher voltage levels across the input full-scale range of the converter (that is, one, two or even 3Vpp); therefore, the differential nature of the analog input enables a smaller process node to be accommodated. For more information, see 1.

4 Emulate the FDA and ADC Together to Avoid Pitfalls

Once an FDA and ADC down selection is made, it is best to do a functional simulation to make sure the VOCM and power supplies meet the proper compliance range for your design. To do this quickly and simply, instead of doing all the math as described in the datasheets, simply download the FDA calculator on TI.com. See reference 9.

Here in this FDA calculator tool, select most FDAs that are available at TI.com to understand if this FDA meets specific VCM compliance range to satisfy both the FDA and the functionality of the ADC.

See Figure 4-1 to get a closer look at this specific calculator. This allows for both DIFF in and DIFF out configurations, as well as SE in to DIFF out configurations.

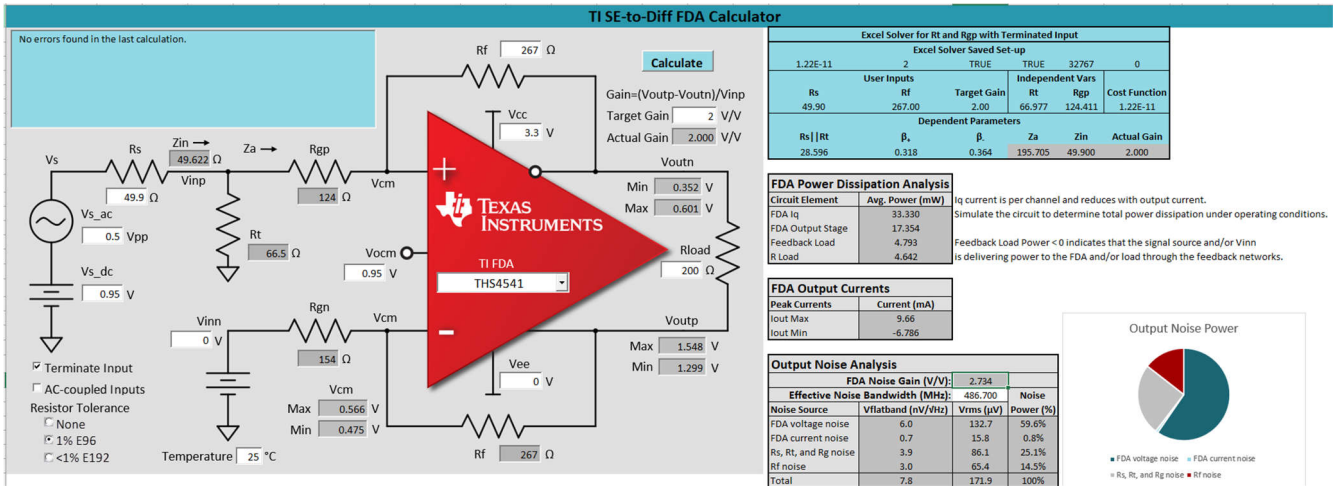

Figure 4-1. FDA Calculator Example Using the THS4541, SE Input to DIFF Output (Shown)

A few last points to make, particularly if the FDA is configured with a single-ended input and differential output. Note Figure 4-1 again. See that both FDA inputs are terminated with different resistor values to be purposely *imbalanced*. This is to force the common mode currents to balance out in this configuration. Therefore, an extra Rt value is required on the signal input of the amplifier, and the values of Rgp and Rgn are slightly unequal to help balance this impedance when only using one input. If this is not done correctly, these common mode currents do not cancel out, and the voltage on the outputs are not necessarily equal. Here's what can manifest if this good circuit has gone bad. See Figure 4-2

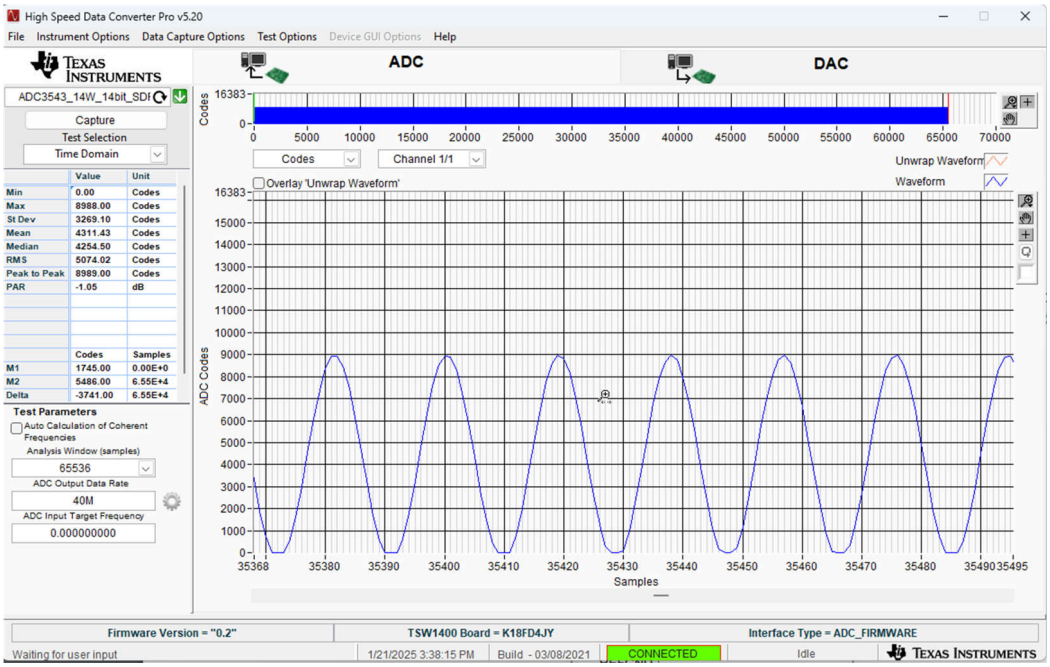

Figure 4-2. Shifted Analog Input Signal Capture from the ADC, due to the Output Common Mode Voltages of the FDA Being Imbalanced Between the P and N Outputs

In this figure we can see, the imbalance is forcing the input signal to be skewed off center from mid-scale. Therefore, the input *bumps* up against the compliance range of the ADC in one direction or the other before it can achieve full-scale input. This causes the ADC to *appear* to be clipping or over-ranging, simply because the VCM compliance is not *centered*. Because of this, the converter will appear have gain and/or offset errors that degrade to the overall measurement being acquired. The designer can find the converter *clips* early and the input signal cannot reach full scale.

To avoid this mishap. Simply work through the recommended example equations in the datasheet for SE to DIFF approaches, or use this handy calculator at TI.com, as seen in Figure 4-1. Otherwise, this effectively creates a *VCM tug of war* between the outputs of the FDA and the inputs of the ADC. These DC common mode values are not matching perfectly between the two devices. And therefore, these two devices will start to “fight” each other and invariably settle somewhere to satisfy each other’s DC needs. Regardless of who wins, the circuit is not healthy, and FDA/ADC combo cannot represent itself in the spectrum properly, as shown in Figure 4-3

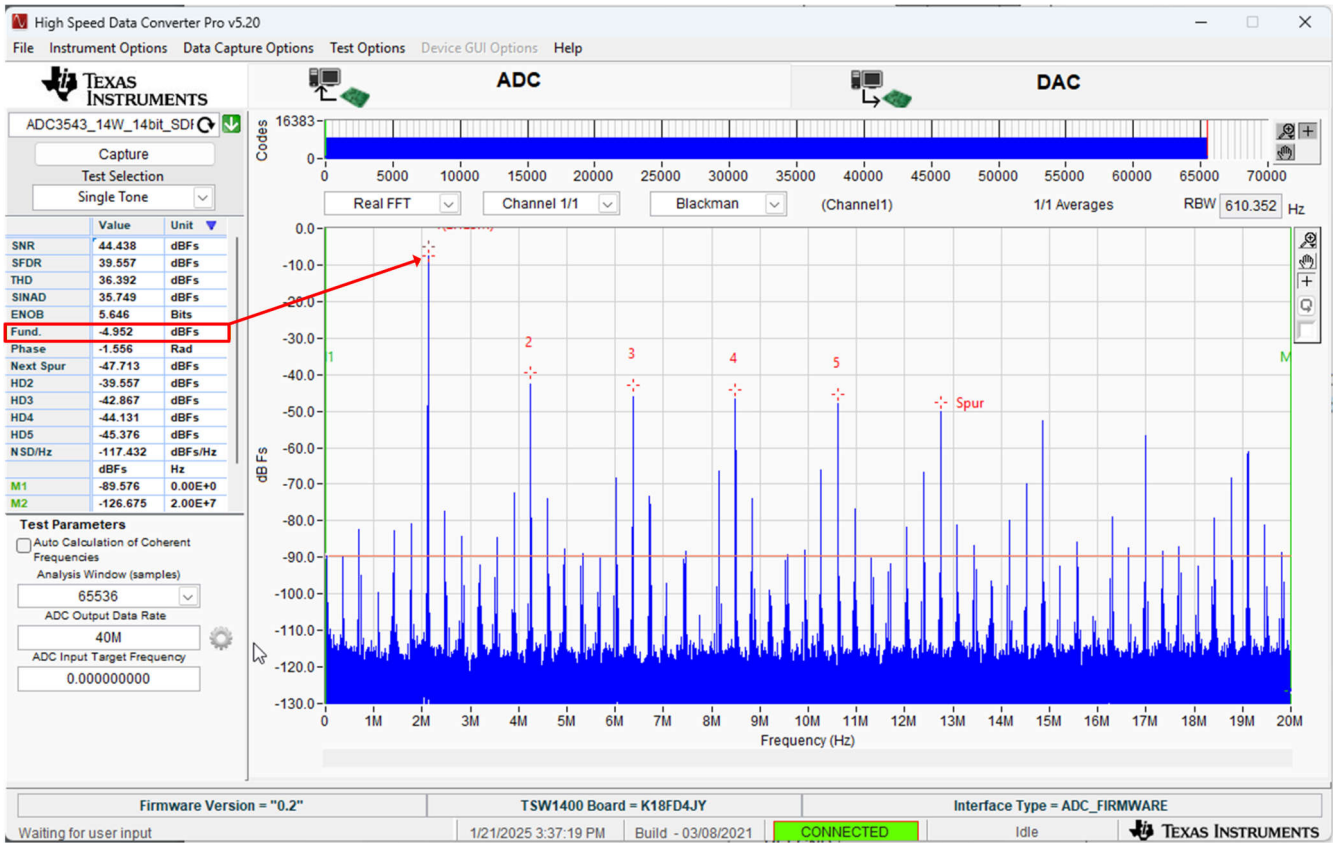

Figure 4-3. HSDCPro Output Spectrum Clipped due to Poor Common Mode Balance

Note to stay away from the ADC's VREF pin or check the datasheet. Most pins with this type of annotation aren't equipped to supply a VCM bias unless they are buffered through an amplifier follower configuration externally. Keep in mind that the VREF pin sets up all the internal reference biases within the converter. This also is a function of the input full-scale of the converter. If the VREF pin is used improperly, for example, loaded down, the input full scale range of the converter may be unintentionally shifted, which also would cause the scenario shown in Figure 4-2 and Figure 4-3 . Therefore, the total dynamic range of the system becomes limited. In summary, leave the VREF pin alone if possible.

5 Five Steps to Achieve DC Coupled-Bliss

Now that we have reviewed key points and understanding of DC coupling in general, as well as amplifier and ADC details to properly design a DC coupled receiver. Let's work through a simple real-world DC-coupled example to make sure we show how to employ all we have learned from the points above.

1. Start with the following requirements, assuming the user wants to DC couple and use an FDA, here are a few parameters that must be considered upfront for the start of the design:

   ADC's sampling rate: 40MSPS

   Receiver (FDA and ADC) bandwidth (BW): DC to 1st Nyquist (20MHz)

   Receiver (FDA and ADC) passband flatness: +1dB across the passband.

   Receiver (FDA and ADC) SNR/SFDR: 75dBc / 85dBc (minimum at -3dBFS)

   FDA maximum input signal drive: 0dBm at 10MHz (or less)

   Note

   This requirement assumes the FDA must have a gain of 2V/V or more a small input signal amplitude into the FDA to achieve full-scale of the ADC.

   FDA configuration: Input = Single-ended, Output = Differential

   For more information on the above requirements and deeper explanations, see *Unraveling the Practical Mysteries Behind RF Converter Front Ends*.
2. Review a listing of TI's current FDA and ADC offerings and after much spreadsheet analysis and tradeoffs, the THS4541 and ADC3543 were chosen for this example. Arguably, this step has been made pretty simple. The idea is to keep in mind that this step can be fairly exhausting when looking at the entire landscape of FDAs and ADCs that fall within the requirements. TI recommends that building a spreadsheet for both the FDA and ADC, highlighting all the relevant specifications as outlined above. See Figure 5-1 as an example.

FDA	Part Number	Power (mW)	Supplies (V)	SFDR (dBFS)@10MHz	Noise (nV/sqrt(Hz))	BW (MHz)	VOCM Range (V)	NF (dB)	Slew Rate (V/uSec)	Rload (ohms)	
1	LMH5401	275	5/Dual	94	1.25	6200	+/-1.4	9.6	17500	200	
2	THS4541	48.5	5/Dual	90	2.2	850	+/-2.3	12	1500	500	
3	THS4532	5	5/Dual	30	10	27	+/-2.4	NA	220	2000	
4	THS4535	25	5/Dual	30	3.6	80	+1.4/-2.1	NA	47	1000	
5	LMH6554	260	5/Dual	102	0.9	2500	+/- 1.25	7.7	6200	200	
ADC	**Part Number**	**Power (mW)**	**Supplies (V)**	**SFDR (dBFS)@10MHz**	**SNR (dBFS)@10MHz**	**BW (MHz)**	**VCM (V)**	**Sampling Rate (MSPS)**	**Resolution (Bits)**	**Input Fullscale (Vpp)**	**Digital Interface Type**
1	ADC3563	77	1.8	94	81.9	230	0.95	65	16	3.2	Serial LVDS
2	ADS4142	105	1.8	87.5	71.1	400	0.95	65	14	2	Parallel CMOS
3	ADC3543	35	1.8	88	79	230	0.95	65	14	2.25	Parallel CMOS
4	ADS5560	250	3.3	89	84	300	1.5	40	16	3.56	Parallel CMOS
5	ADS6142	285	3.3	96	74.7	450	1.5	65	14	2	Parallel CMOS

Figure 5-1. FDA and ADC Spreadsheet Tradeoff Analysis.

3. Now that the FDA and ADC have been down selected, it is best to find out if they are voltage common mode compatible using the spreadsheet above or the FDA and ADC datasheet respectively. As seen in Figure 4-1, the FDA is configured for a SE input and DIFF output, only requiring a 3.3V power supply to satisfy the +0.95V common mode voltage needs of the ADC's analog inputs. Note, that this step could also be accomplished due to the down-selection of FDA and ADC in the spreadsheet in the previous step. This step acts as a good double-check.
4. Next it is best to design an anti-aliasing filter or AAF in between the output of the FDA and inputs of the ADC. This will help reduce the BW requirement as noted above to 20MHz and mitigate any extra noise folding back into baseband, further degrading the ADC's SNR performance requirement. Keep in mind the amplifier is an active device and will inherently have noise and adds to the noise within the ADC's passband region. For more understandings on FDA noise and how this adds to the overall receiver signal chain, for example, – degrades, SNR, see 4 and 6

   Using a simple filter solutions tool from Ansys or similar can provide a good starting point to go with on the design. See Figure 5-2 and Figure 5-3 respectfully. Here, a simple, third order, lowpass Butterworth filter was designed out to 25MHz. The filter cutoff is overdesigned to account for some losses that will take effect when the actual values are implemented on the PCB. See 2 for more details on how to properly design AAFs between FDAs and ADCs. Here we dig deeper on all the little nuances for the use of each component for this FDA and ADC interface.

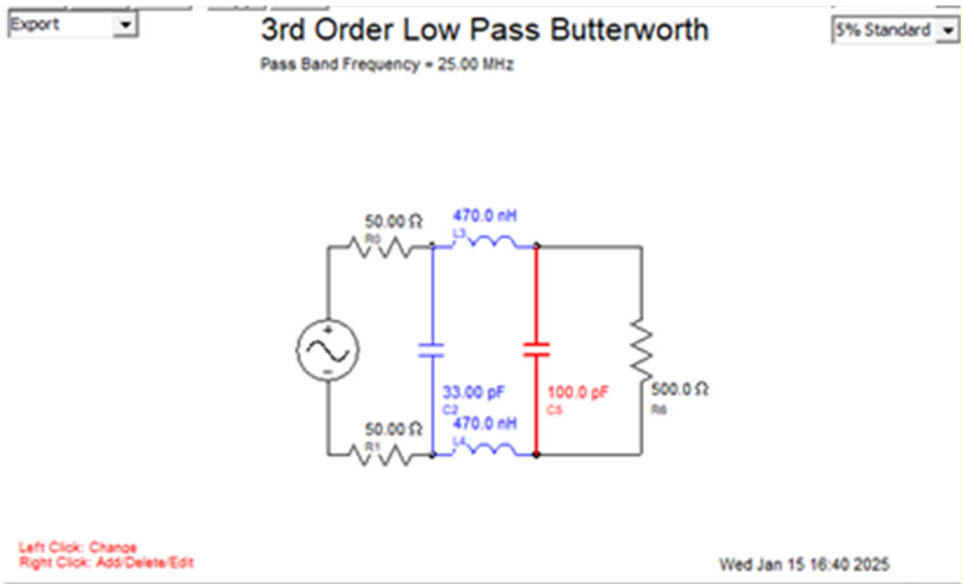

Figure 5-2. 25MHz Differential AAF Design - Schematic

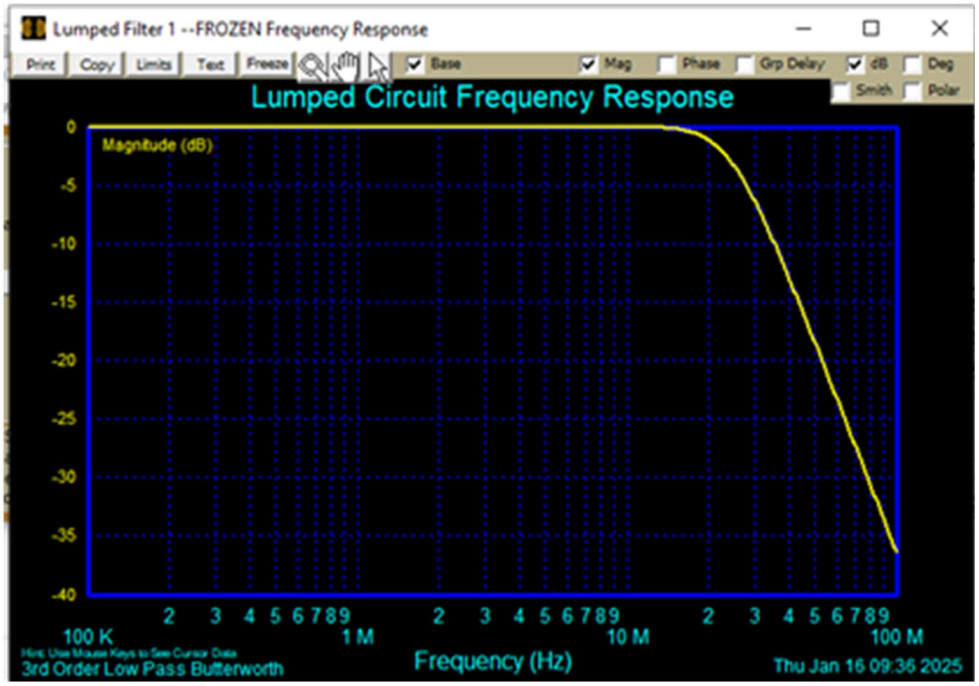

Figure 5-3. 25MHz Differential AAF Design - BW/Insertion Loss Simulation

5. Build the receiver design in the lab based on Figure 5-4 and start accumulating some test measurements as per all the requirements outlined above in Step 1. In this case, this example uses THS4541 FDA and ADC3543 evaluation module test boards (or EVMs) which typically offer several handy modification options to procure designs such as this. Soldering iron not included.

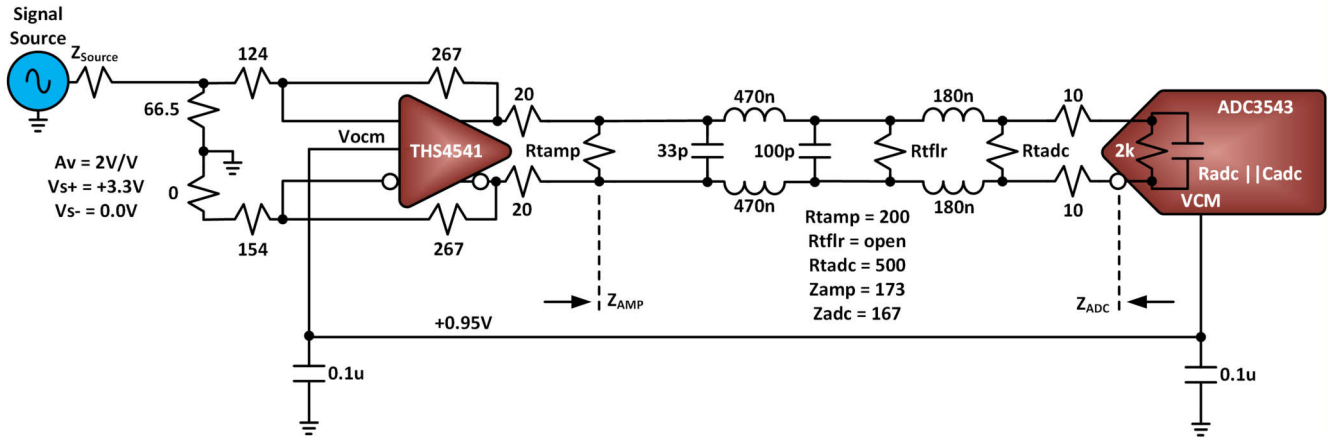

Figure 5-4. Block Diagram Real World DC-Coupled Design Example

The first measurement we need to complete and verify is the passband flatness of the signal chain line up. Here in Figure 5-5, the passband flatness is shown to have approximately 23MHz of BW based on the AAF design that is implemented between the outputs of the amplifier and the inputs of the ADC. As a reference point, it only takes -4.4dB on the input of the amplifier to reach a -3dBFS signal at 10MHz. This allows users to understand the forward or reverse gain or loss across the required BW set by the system parameters. For more information on how to measure passband flatness appropriately, see 8

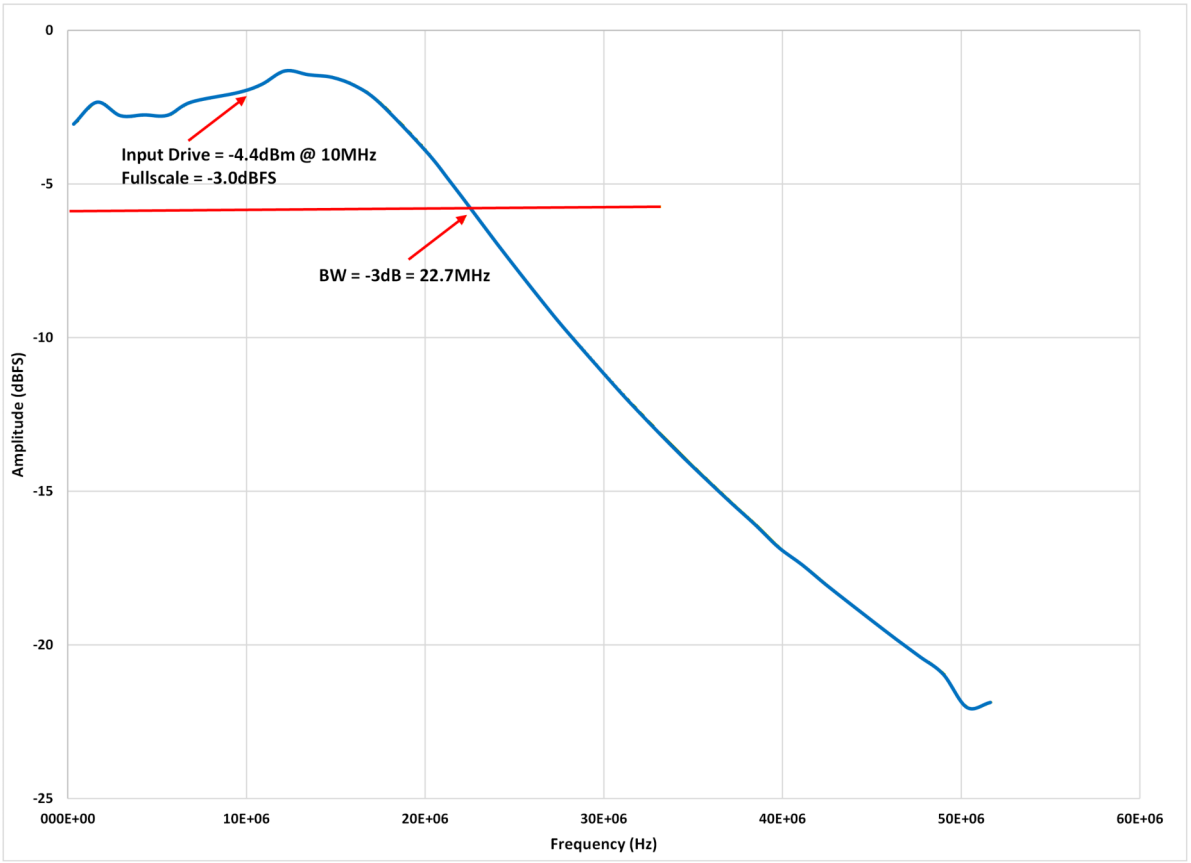

Figure 5-5. Measured Bandwidth, Passband Flatness and Input Drive

Once the passband flatness BW has been verified, the next step is to complete some AC performance sweeps across the application bandwidth. This gives insight on how the performance holds up dynamically to verify that the ADC is still meeting all the other performance requirements for the application. See Figure 5-6 and Figure 5-7 respectfully.

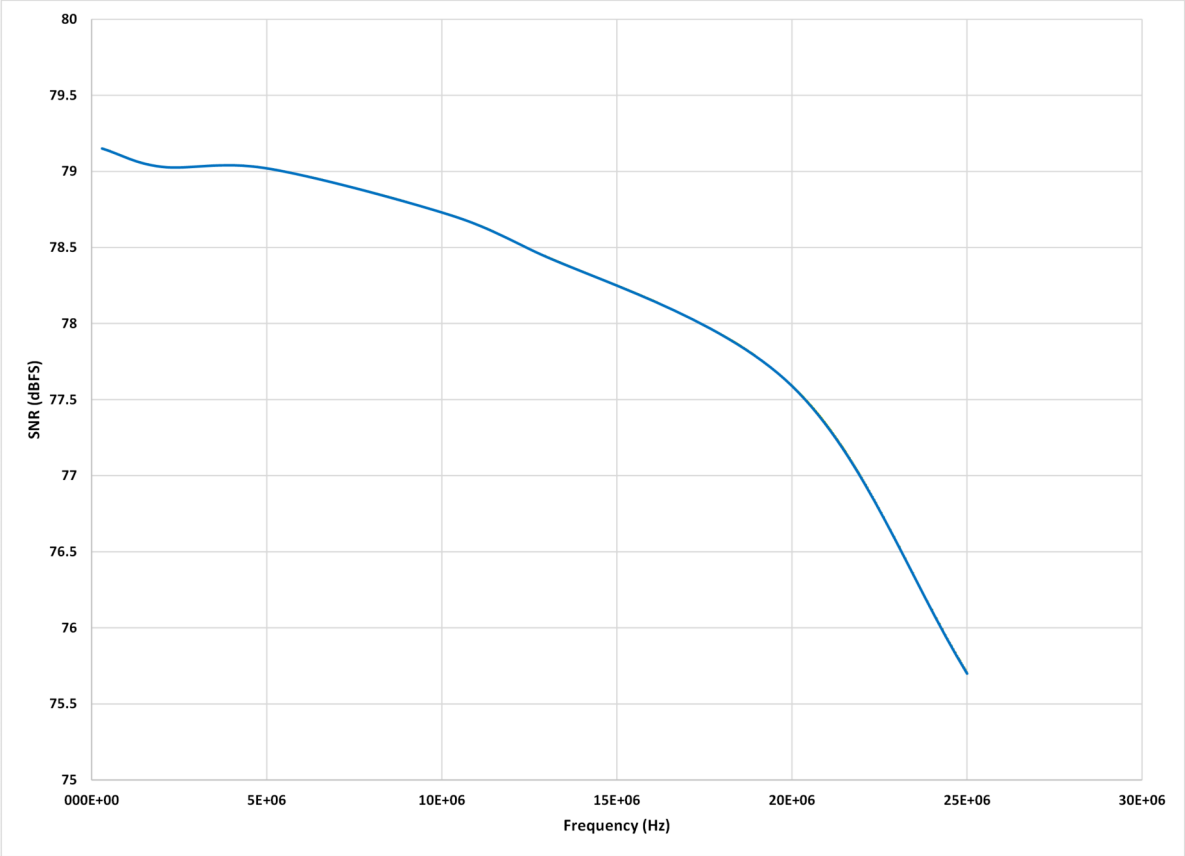

Figure 5-6. Measured SNR Sweep vs. Analog Input Frequency

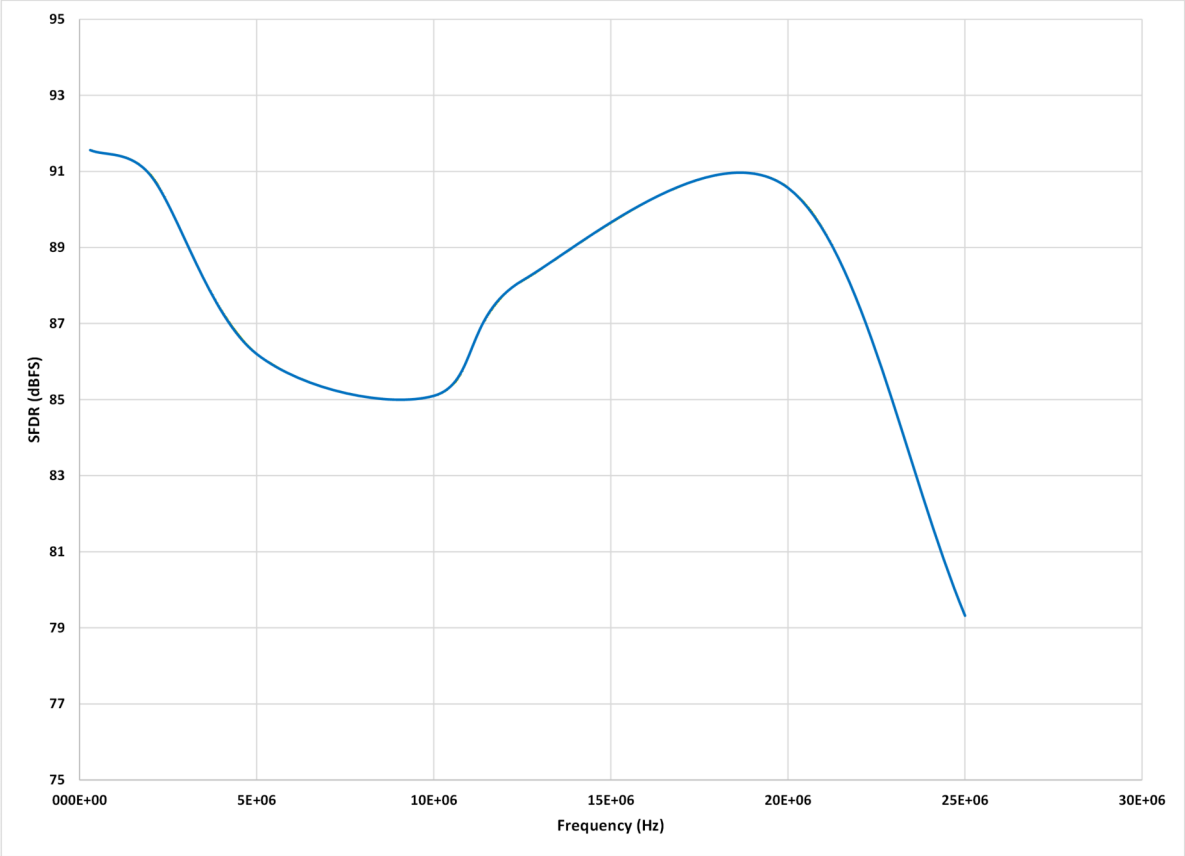

Figure 5-7. Measured SFDR Sweep vs. Analog Input Frequency

As shown, the SNR and SFDR performance across the measured bandwidth is 79 to 75dBFS and 92 to 79dBFS respectfully. All measurements were taken near DC, and 300kHz to 25MHz with a total of 10 frequency points at -3dBFS to derive the curves.

To show the spectral purity of the combined DC coupled FDA and ADC signal chain a few FFTs are shown in Figure 5-8 and Figure 5-9 respectfully, using TI's HSDC Pro data capture software. Near DC, 300kHz, and 20.3MHz analog input tones are shown. Each FFT AC performance measurement is well within the requirements as specified previously.

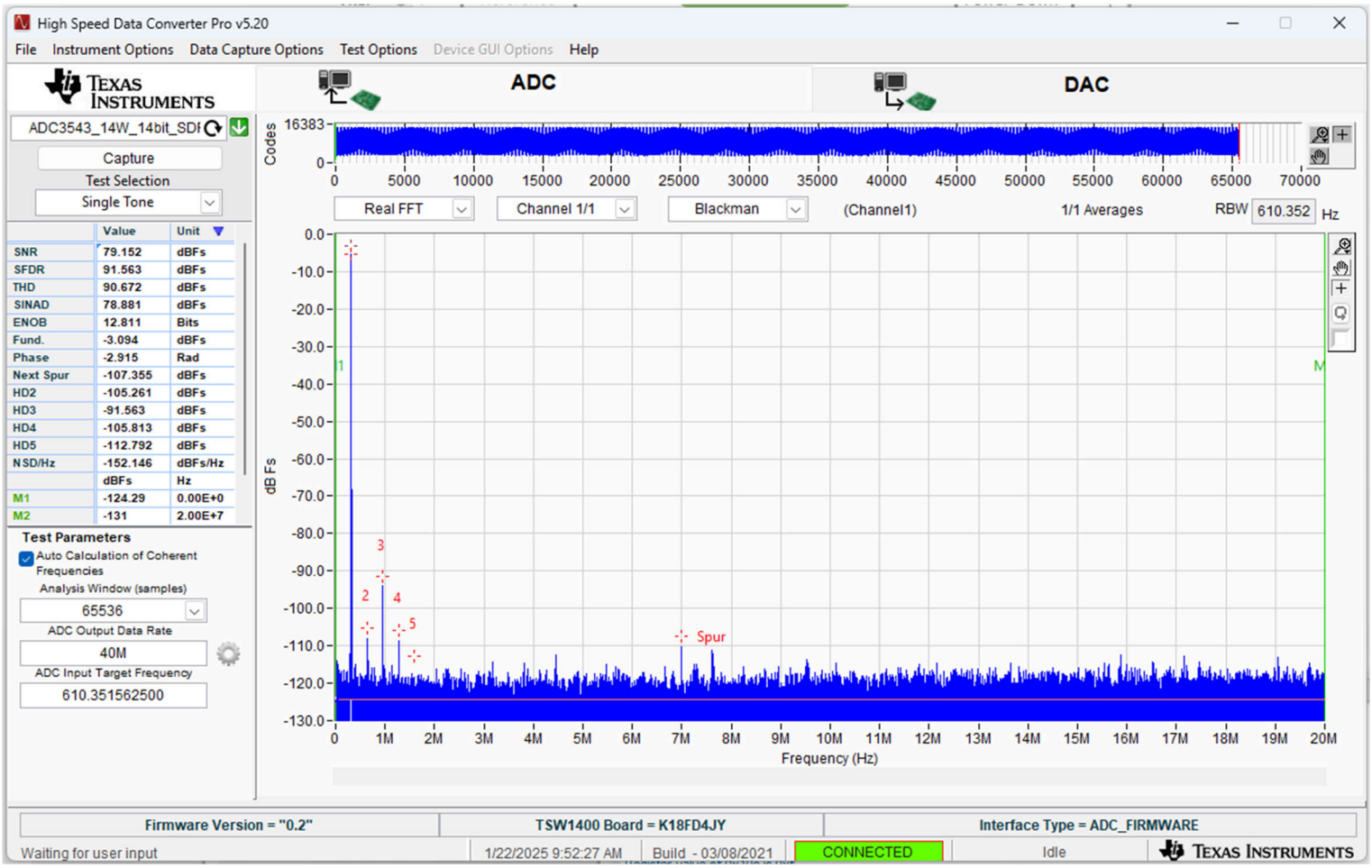

Figure 5-8. Measured FFT Performance: *Near* DC, Fin = 300kHz

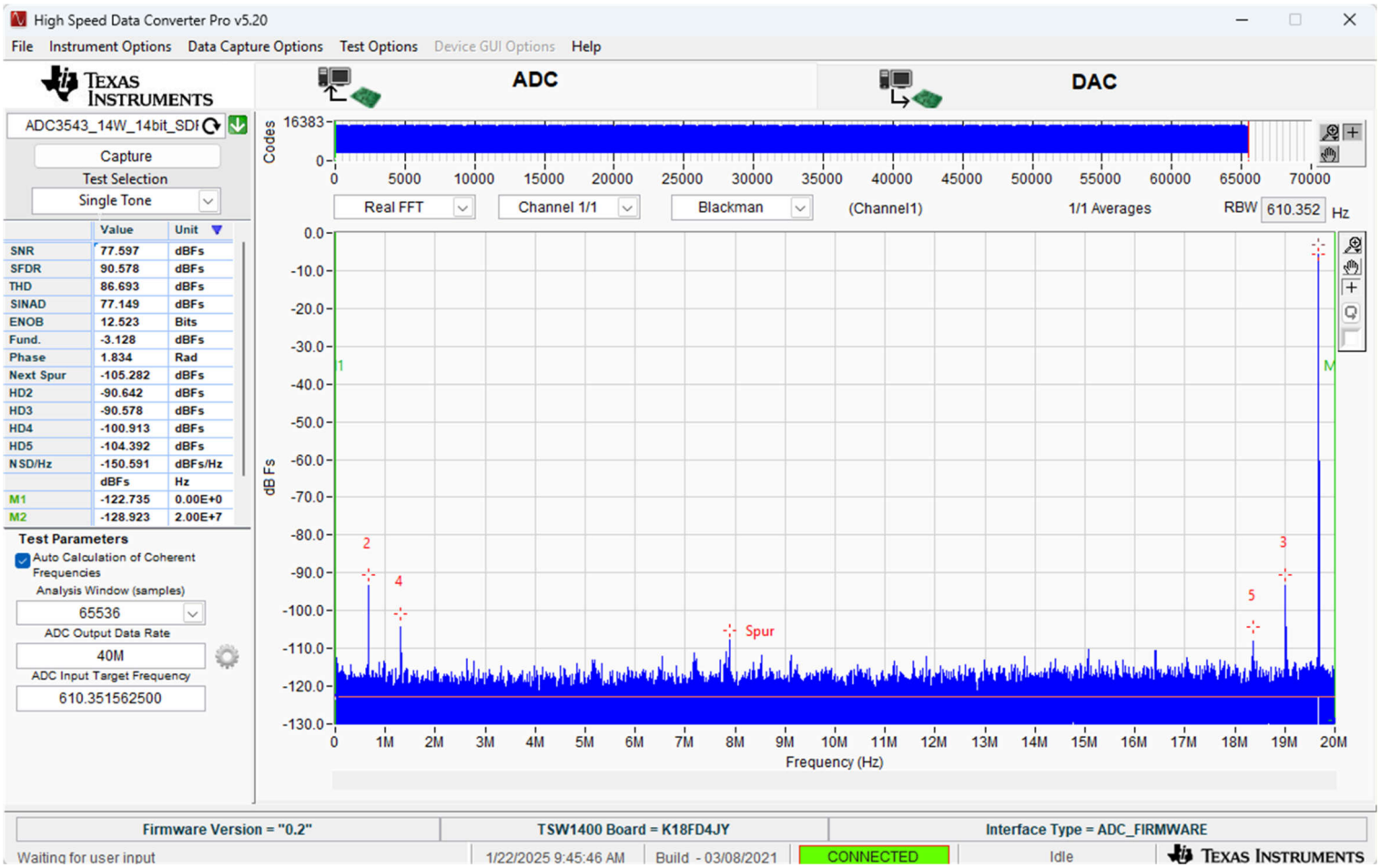

Figure 5-9. Measured FFT Performance: Fin = 20.3MHz

As seen, following this simple five step process can make a user's next high-speed DC couple signal chain design successful. Determine the signal chain requirements upfront, create a simple spreadsheet to help with device comparisons and simply use stock, off-the-shelf EVMs in order to cut-and-paste the signal chain design together if the two components are not already located on the same board to start. With a few standard lab measurements, a user can simply assess the overall design functions and can start to translate the final design into the customer board or system design.

6 Summary

This document has shown how proper DC coupling frontends between FDAs and ADCs can be developed quickly and easily, as long as the noted pitfalls above are avoided. First, understand that an amplifier is required in order to DC couple. Baluns and transformers cannot be used in this type of application scenarios. Also keep in mind that an amplifier adds noise to the overall receiver signal chain, and therefore an AAF must be employed between the two devices to minimize the noise in the output spectrum. Check to make sure the amplifier of choice and ADC are DC compatible, and the common mode voltages are in the normal range of operation of both devices. This is paramount to make a DC coupled design successful. Using handy FDA DIFF Calculator spreadsheets and other tools available on the internet is a good place to start to make sure each device is within the compliance range of other devices. Lastly, use the 5-step process as a guide in which to develop a DC coupled frontend design, otherwise, the next receiver signal chain can clip early or not reach the ADC's full-scale range at all, wreaking dynamic range havoc.

7 References

1. Texas Instruments, Unraveling the Full-Scale Mysteries of Your RF Converter's Analog Inputs, application note.
2. Texas Instruments, How anti-aliasing filter deign techniques improve active RF converter front ends, analog design journal.
3. Electronic Design, *Achieve CM Convergence Between Amps and ADCs*, webpage.
4. Electronic Design, *Noise Considerations in ADC Signal Chains*, webpage.
5. Texas Instruments, *Unraveling the Practical Mysteries Behind RF Converter Front Ends*, presentation.
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7. Texas Instruments, *Sampling around Nyquist holes in highspeed converters*, application note.
8. Texas Instruments, *Proper High-Speed A/D Converter Passband Flatness Revealed*, application note.
9. Texas Instruments, *DIFFAMPGAINCALC Calculation Tool*, calculation tool.
10. Texas Instruments, *HSDCPro Data Capture Software*, software.

8 Revision History

Changes from Revision * (January 2026) to Revision A (May 2026)	Page
• Corrected typo	3

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