Application Note

Design Considerations of Active Clamping Circuit in Full Bridge Converter

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ABSTRACT

In DC-DC converters for electric vehicle applications, full-bridge topologies are extensively utilized, with voltage stress on synchronous rectifiers representing a significant design challenge. This paper is organized as follows: Section 1 examines the fundamental mechanisms underlying voltage stress generation and compares different snubber circuit solutions. Section 2 presents a comprehensive analysis of active clamp (ACL) circuit classifications and the corresponding hardware implementation strategies. Section 3 shows the control principles and software architecture associated with ACL circuits. The findings presented herein aim to serve as a technical reference for engineers engaged in snubber circuit design and optimization.

Table of Contents

Trademarks

1 Introduction

In high-voltage to low-voltage DC-DC conversion applications, full-bridge circuits are extensively employed due to the capability to provide galvanic isolation while facilitating high-power transmission. The full-bridge topology encompasses several architectural variants, including hard-switching full bridge, phase-shifted full bridge (PSFB), dual active bridge (DAB), and full bridge LLC resonant converter topologies. Hard-switching and phase-shifted full-bridge configurations commonly exhibit elevated voltage stress across the secondary-side synchronous rectifiers, necessitating the implementation of semiconductor devices with higher voltage ratings. This requirement consequently increases the bill of materials (BOM) cost. Furthermore, devices with higher voltage ratings inherently possess increased on-state resistance (RDSon), which degrades the overall power conversion efficiency of the system.

1.1 Voltage Stress on Synchronous Rectifier

Consider the phase-shifted full-bridge (PSFB) topology illustrated in Figure 1-1 as a representative example. The primary side comprises a full-bridge configuration, where Q1, Q2, Q3, and Q4 constitute the primary-side power switching devices. The secondary side employs a current-doubler synchronous rectification scheme, with Q5 and Q6 serving as the secondary-side power switches. The transformer is characterized by a turns ratio of N:1, with parasitic leakage inductance Lk and magnetizing inductance Lm. Notably, the leakage inductance Lk requires careful optimization to achieve an appropriate trade-off between the zero-voltage switching (ZVS) operating range and duty cycle loss.

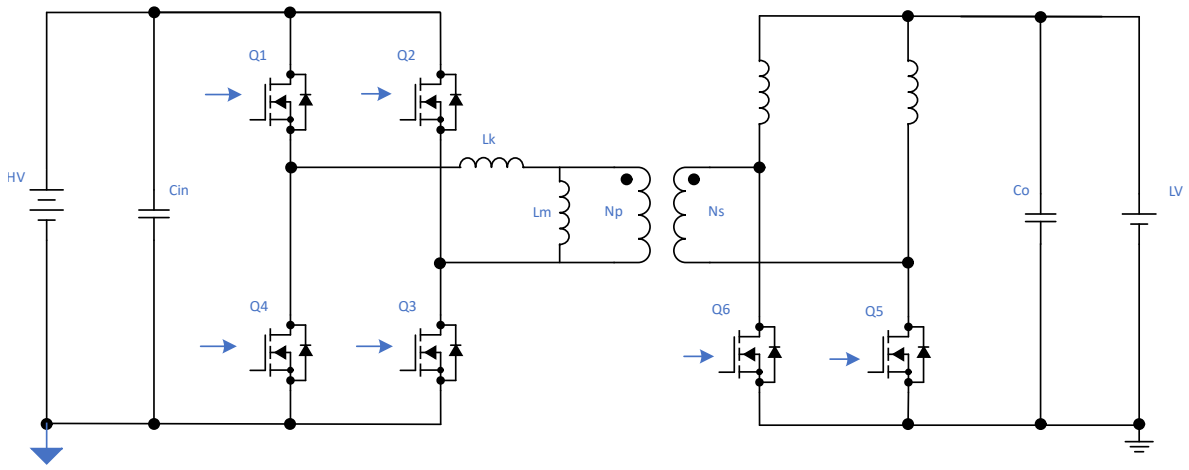

Figure 1-1. Block diagram of the phase-shifted full bridge topology

As shown in Figure 1-2, the elevated voltage stress imposed on the secondary-side MOSFET originates from resonance between Lk and the parasitic output capacitance (Coss) of the secondary MOSFET.

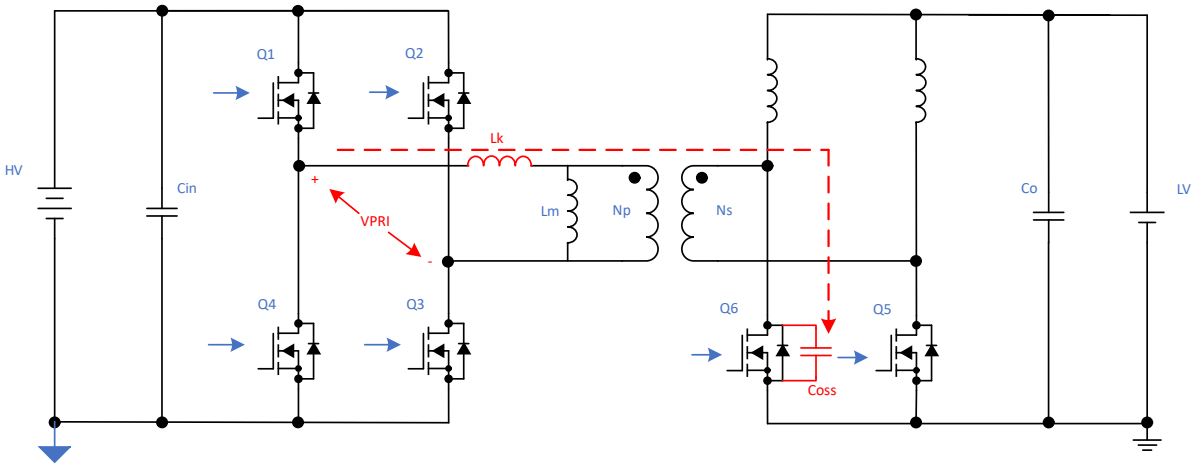

Figure 1-2. Voltage stress caused by resonation

The equivalent circuit depicted in Figure 1-2 can be represented by the simplified model shown in Figure 1-3. In this representation, Lk denotes the primary leakage inductance reflected to the secondary side, Coss represents the output capacitance of the synchronous rectifier, Vin corresponds to the primary-side input voltage, and Io signifies the load current. Upon turn-off of Q6, the initial voltage across Coss is 0V, and the circuit exhibits a zero-state response characteristic of an LC series resonant network. As the reflected input voltage Vin/N charges Coss, resonance occurs between Lk and Coss. In the idealized case where parasitic resistance is neglected, the peak voltage across Coss can theoretically reach twice the steady-state voltage value due to this resonant behavior.

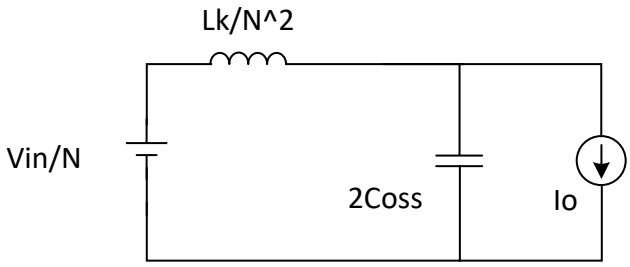

Figure 1-3. Equivalent Circuit of Voltage Stress

For a typical automotive 400V-to-14V DC-DC converter, the maximum input voltage is approximately 430V. Assuming a transformer turns ratio of 6:1 and full-load operation at 3.5kW, theoretical calculations indicate a maximum voltage stress of 143V and a steady-state plateau voltage of 71.5V across the secondary-side switches. Figure 1-4 shows the simulated voltage stress waveform in the absence of any snubber circuit. Without clamping intervention, the peak voltage reaches 125.8V. The deviation from the theoretical maximum

and subsequent decay are attributed to voltage drops across the primary-side power devices and the equivalent series resistance (ESR) inherent in the system.

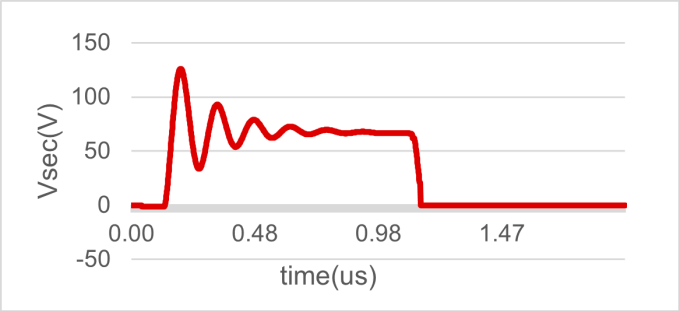

Figure 1-4. Simulation Waveform of Voltage Stress without Snubber Circuit

As evident from Figure 1-4, the transient voltage is directly imposed upon the synchronous rectifier circuit, necessitating the selection of power devices with a voltage rating of 150V in the absence of clamping measures. As previously discussed, this requirement increases both the BOM cost and degrades overall system efficiency due to the higher RDSon of such devices. Consequently, the implementation of snubber circuits to suppress voltage stress represents a more prevalent and cost-effective design approach in practical applications.

1.2 Snubber Circuit Overview

Snubber circuits are generally categorized into two primary classifications: passive snubber circuits and active clamping circuits. The subsequent sections provide a detailed analysis of each circuit topology.

1.2.1 RC Snubber

The RC snubber represents a conventional clamping design that has achieved widespread adoption due to its cost-effectiveness, as illustrated in Figure 1-5. The RC series network is connected in parallel with the synchronous rectifier, where the capacitor serves as an energy buffer while the resistor functions to limit transient current magnitude. Upon turn-off of Q6, when the voltage stress across Q6 exceeds the capacitor voltage, the capacitor undergoes charging through the resistor, thereby clamping the voltage stress to approximately the capacitor voltage level. Conversely, during the turn-on transition of Q6, the capacitor discharges through the resistor into Q6, maintaining charge balance and establishing a steady-state capacitor voltage.

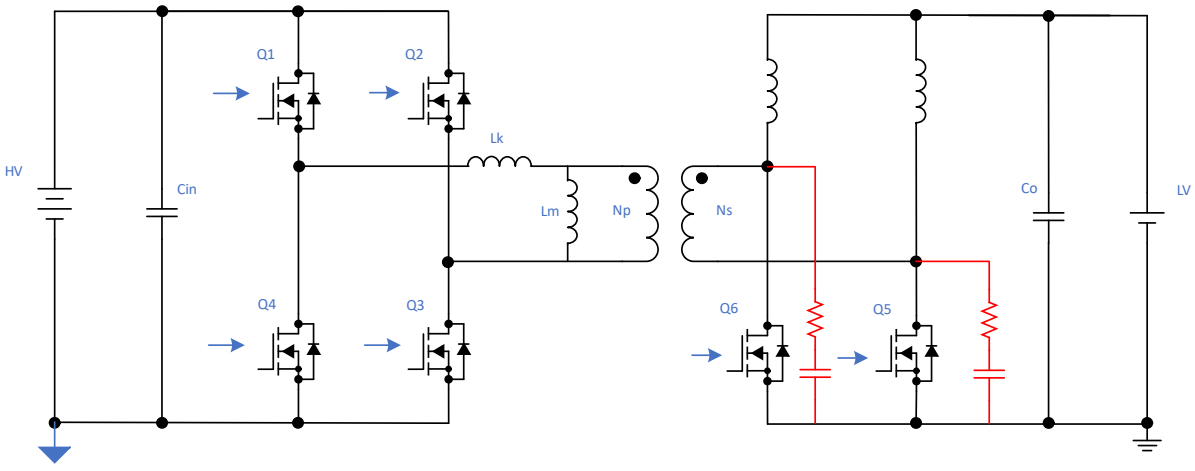

Figure 1-5. Block Diagram of the RC Snubber Circuit

The primary limitation of the RC snubber circuit is that the capacitor discharges through the synchronous rectifier power switch, resulting in complete energy dissipation within the resistor. This mechanism degrades system efficiency and presents significant thermal management challenges due to resistive heating. Figure 1-6 shows the simulated voltage stress waveform with an RC snubber circuit implemented using a 10Ω resistor and 3nF capacitor. The simulation results demonstrate a reduction in peak voltage stress from 125.8V to 113.1V. Comparative efficiency analysis reveals that the RC snubber introduces an additional power loss of 19W, corresponding to a 0.54% reduction in overall system efficiency.

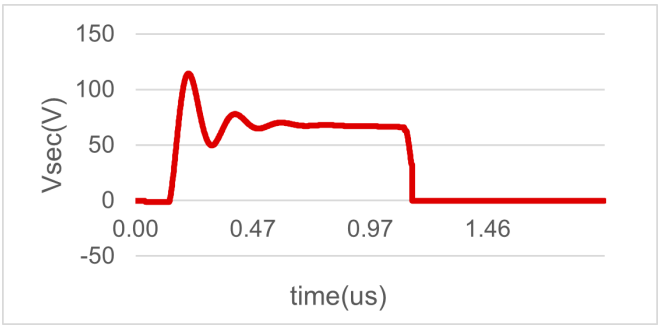

Figure 1-6. Simulation Waveform of Voltage Stress with RC Snubber Circuit

1.2.2 RCD Snubber

The RCD snubber circuit represents an extension of the RC configuration with the addition of a series diode, as depicted in Figure 1-7. The diode anode is connected to the drain terminal of the synchronous rectifier device, while the cathode is connected to the capacitor; a resistor is bridged across the capacitor and the output side. Upon turn-off of Q6, when the voltage stress across Q6 exceeds the capacitor voltage, the capacitor charges through the diode, effectively clamping the voltage stress to the capacitor voltage level. The capacitor discharges through the resistor to the DC-DC converter output, thereby maintaining charge balance and establishing a steady-state capacitor voltage.

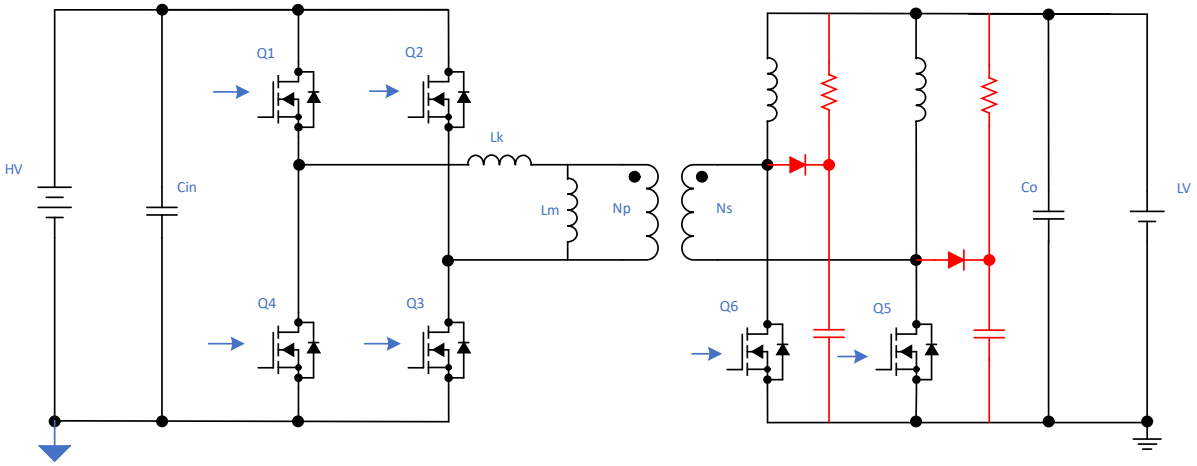

Figure 1-7. Block Diagram of the RCD Snubber Circuit

Compared to the RC snubber circuit, the RCD snubber configuration offers two significant advantages. First, the capacitor charging process is facilitated through a diode, resulting in a clamping voltage equal to the capacitor voltage plus the forward voltage drop of the diode. In contrast, the RC snubber exhibits a clamping voltage equal to the capacitor voltage plus the resistive voltage drop, which is typically higher. Consequently, the RCD snubber achieves a lower effective clamping voltage. Second, the capacitor discharges through the resistor to the converter output rather than through the synchronous rectifier. This enables partial energy recovery to

the output, thereby reducing resistive losses and improving overall efficiency compared to the complete energy dissipation characteristic of the RC snubber.

In the RCD snubber circuit, since no series resistor limits the charging current, the diode must possess adequate current handling capability, and the capacitor requires sufficient capacitance to prevent overvoltage conditions induced by transient current spikes. Figure 1-8 presents the simulated voltage stress waveform with an RCD snubber circuit employing a 510Ω resistor and 100nF capacitor. The simulation results indicate a reduction in peak voltage stress from 125.8V to 101.2V. Comparative efficiency analysis reveals that the RCD snubber introduces an additional power loss of 15W, corresponding to a 0.42% degradation in overall system efficiency.

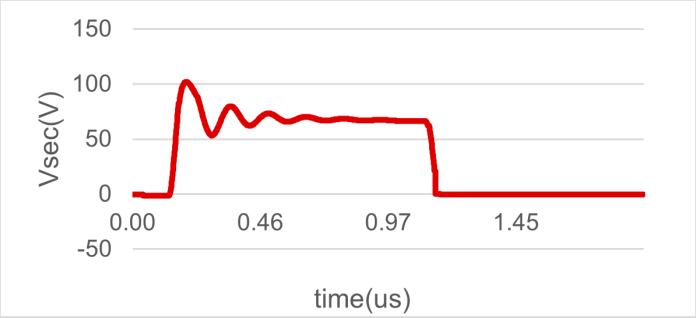

Figure 1-8. Waveform of Voltage Stress With RCD Snubber Circuit

1.2.3 Diode Clamping

Diode clamping techniques are generally classified into two categories: secondary-side Zener diode clamping and primary-side Schottky diode clamping. Secondary-side Zener diode clamping represents a straightforward implementation approach, as illustrated in Figure 1-9. A Zener diode is connected in parallel with the synchronous rectifier device. When the voltage stress exceeds the Zener breakdown voltage, the diode enters avalanche conduction, effectively clamping the voltage stress to the characteristic breakdown voltage level.

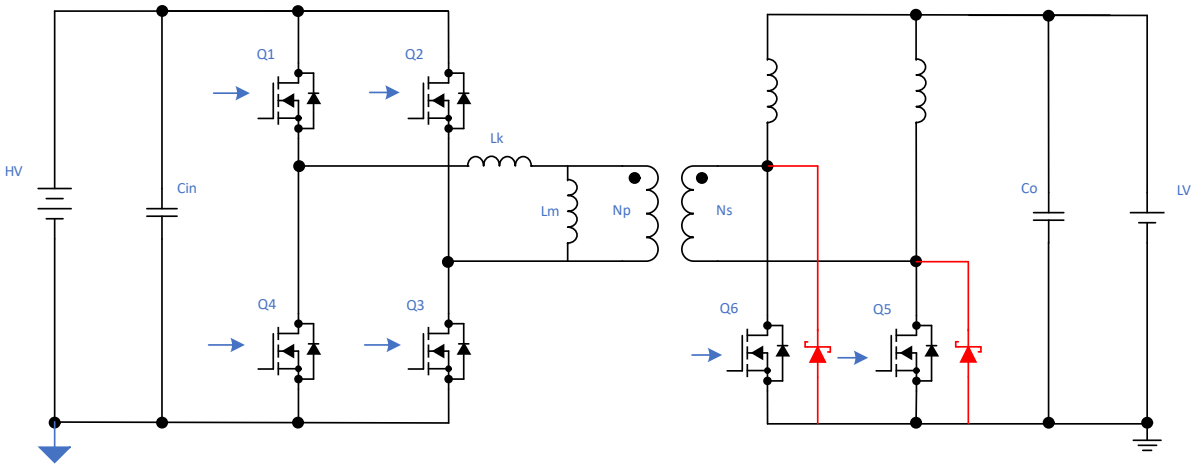

Figure 1-9. Block Diagram of the Zener Diode Clamping Circuit

While this circuit topology exhibits simplicity, the limitations are substantial. The entire absorbed energy is dissipated within the Zener diode, resulting in reduced system efficiency and significant thermal stress on the device. Consequently, this approach is typically employed in conjunction with complementary clamping circuits rather than as a standalone design. Figure 1-10 shows the simulated voltage stress waveform with Zener diode clamping implemented. The simulation demonstrates a reduction in peak voltage stress from 125.8V to 101.2V. Comparative efficiency analysis reveals that the Zener diode clamping circuit introduces an additional power loss of 27W, corresponding to a 0.78% degradation in overall system efficiency.

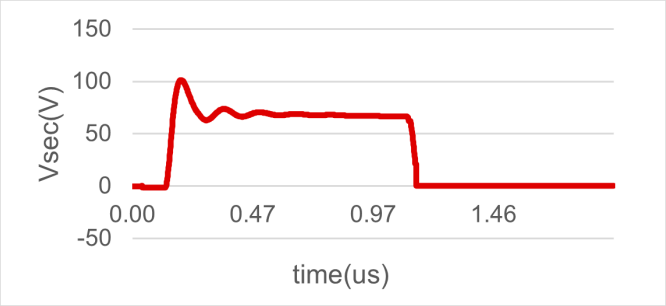

Figure 1-10. Simulation Waveform of Voltage Stress with Zener Diode Clamping Circuit

Primary-side Schottky diode clamping represents a more widely adopted implementation, as depicted in Figure 1-11. The clamping network consists of two Schottky diodes configured as follows: one diode has the anode connected to the primary winding of the transformer and the cathode connected to the positive high-voltage bus (HV BUS+); the other diode has its cathode connected to the primary winding and its anode connected to the negative high-voltage bus (HV BUS-). When excessive transient voltage appears on the secondary side, the reflected voltage on the primary side (scaled by the transformer turns ratio) is clamped by the diodes, thereby limiting the maximum voltage stress experienced on the secondary side through the transformer coupling.

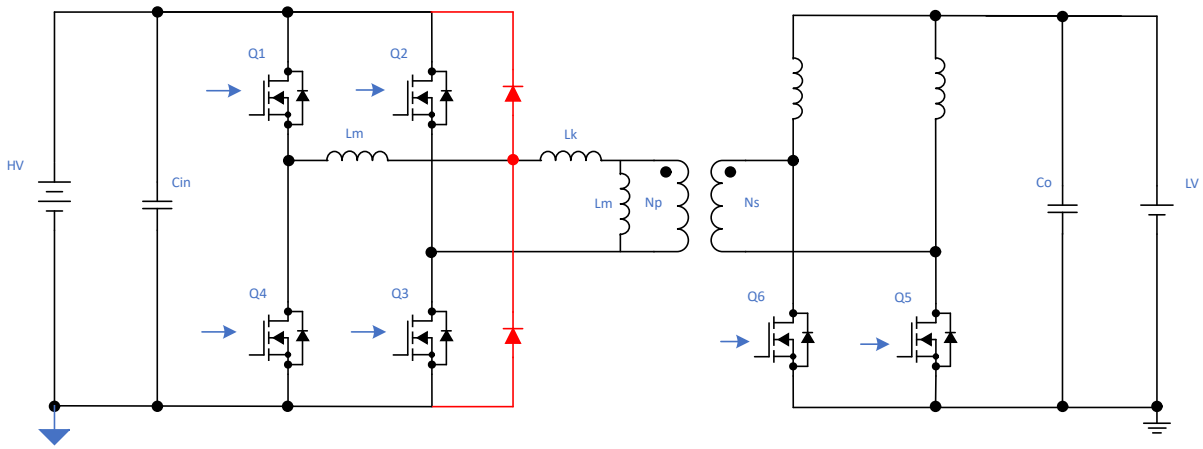

Figure 1-11. Block Diagram of the Schottky Diode Clamping Circuit

While this solution demonstrates effective voltage stress suppression, it exhibits two significant limitations. First, in conventional designs, the external inductor Lr and the transformer leakage inductance Lk collectively provide the inductance required for PSFB operation. However, the primary-side Schottky diodes can only clamp voltage stress resulting from resonance between the external inductor Lr and the output capacitance Coss; they are ineffective against voltage stress generated by resonance between the transformer leakage inductance Lk and Coss. As contemporary DC-DC converter designs increasingly emphasize power density optimization, designers frequently eliminate the external inductor Lr and rely solely on the transformer leakage inductance Lk. Under such conditions, this clamping approach becomes ineffective.

Second, the Schottky diodes must be rated to withstand the full input voltage of the DC-DC converter and possess ultrafast reverse recovery characteristics. For DC-DC systems with 800V input, 1200V SiC Schottky diodes are typically required, significantly increasing the BOM cost.

Figure 1-12 presents the simulated voltage stress waveform with primary-side Schottky diode clamping implemented. To accurately evaluate the effectiveness of this clamping technique, the primary-side inductance was explicitly partitioned into the external inductor Lr and the transformer leakage inductance Lk in the simulation model. The results demonstrate a reduction in peak voltage stress from 125.8V to 86.9V.

Comparative efficiency analysis indicates that the additional power loss attributable to the Schottky diode clamping circuit is negligible and does not measurably degrade overall system efficiency.

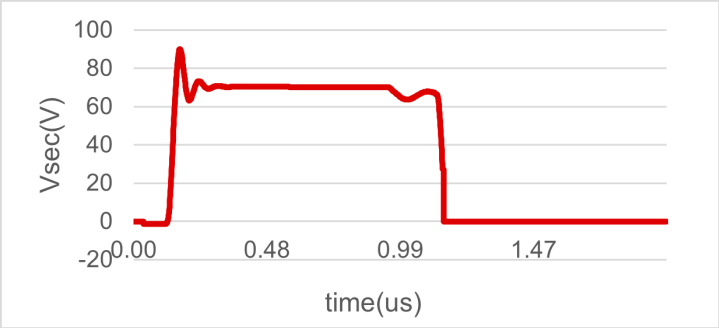

Figure 1-12. Simulation Waveform of Voltage Stress with Schottky Diode Clamping Circuit

1.2.4 Active Clamping

ACL circuits currently represent the most prevalent clamping topology employed in DC-DC converters. Numerous variants of active clamping architectures exist, which is comprehensively examined in Section 2. This section focuses on the representative configuration illustrated in Figure 1-13. The active clamp power switch is connected in series with the clamping capacitor, and this combination is placed in parallel with the synchronous rectifier. Upon turn-off of Q6, when the voltage stress across Q6 exceeds the capacitor voltage, the capacitor charges through the antiparallel body diode of the active clamp switch, thereby clamping the voltage stress to the capacitor voltage level. Through precise control of the active clamp switch turn-on timing and conduction duration, the energy stored in the clamping capacitor can be completely transferred to the output side, enabling energy recovery rather than dissipation.

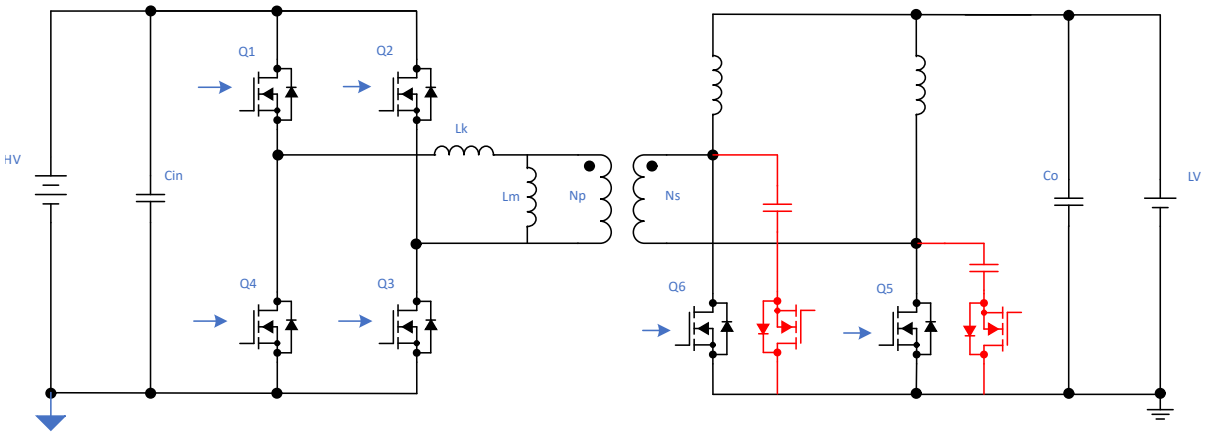

Figure 1-13. Block diagram of the Active Clamping Circuit

In active clamping circuits, the charging path is analogous to that of the RCD snubber configuration, while the discharging path is actively controlled and bypasses the current-limiting resistor. Consequently, this topology achieves highly effective voltage stress suppression. Figure 1-14 presents the simulated voltage stress waveform with active clamping implemented. The simulation results demonstrate a reduction in peak voltage stress from 125.8V to 80.5V. Comparative efficiency analysis indicates that the additional power loss attributable to the active clamping circuit is negligible and does not measurably degrade overall system efficiency.

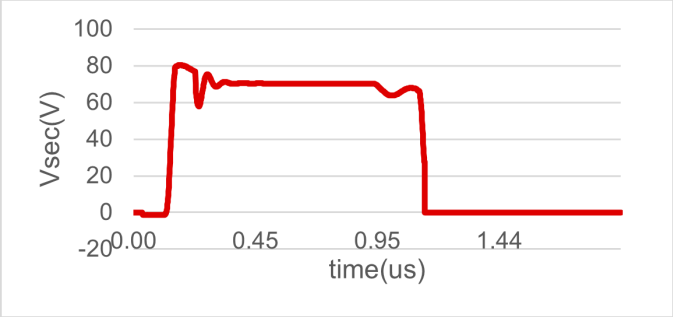

Figure 1-14. Simulation Waveform of Voltage Stress with Active Clamping Circuit

Table 1-1 presents a comprehensive comparison of all clamping circuit topologies discussed. As evident from the comparative analysis, ACL circuits exhibit significant advantages in terms of voltage stress suppression effectiveness and efficiency, which accounts for the widespread adoption in contemporary DC-DC converter designs. Section 2 provides a detailed exposition of ACL circuit design methodologies and implementation considerations.

Table 1-1. Summary of All Clamping Circuits

Clamping Circuit	No Clamping	RC Snubber	RCD Snubber	Zener Clamping	Schottky Clamping	Active Clamping
Voltage stress	125.8V	113.1V	101.2V	101.2V	86.9V	80.5V
Power switch voltage rating	150V	120V	120V	120V	100V	100V
Additional power loss	0W	19W	15W	27W	Negligible	Negligible
Benefits	/	Lowest cost	Low cost, Partial energy recycles	Simple circuit	Good clamping performance	Good clamping performance
Limitation	/	High power loss	High power loss	Highest power loss	High cost,Limited by TF	Complex control

2 Active Clamping Circuit

2.1 Different Types of ACL Circuits

2.1.1 Difference Placement of ACL

The PSFB topology illustrated in Figure 2-1 is extensively employed in high-to-low voltage DC-DC conversion applications. As discussed in Section 1, the synchronous rectifier remains susceptible to substantial voltage stress arising from resonance between the parasitic output capacitance and the transformer leakage inductance. The peak voltage stress imposed on the rectifier can theoretically reach the magnitude expressed in Equation 1.

$$V_{ds\_max} = 2 \times V_{in} \times Ns/Np \quad (1)$$

where Np and Ns are the transformer's primary and secondary windings, respectively.

As discussed in Section 1, designers predominantly favor ACL circuits over RCD snubbers for SR MOSFETs, primarily due to power level requirements and the substantial power dissipation inherent in passive snubber topologies. Figure 2-1 depicts representative ACL circuit configurations commonly implemented in full-bridge SR applications.

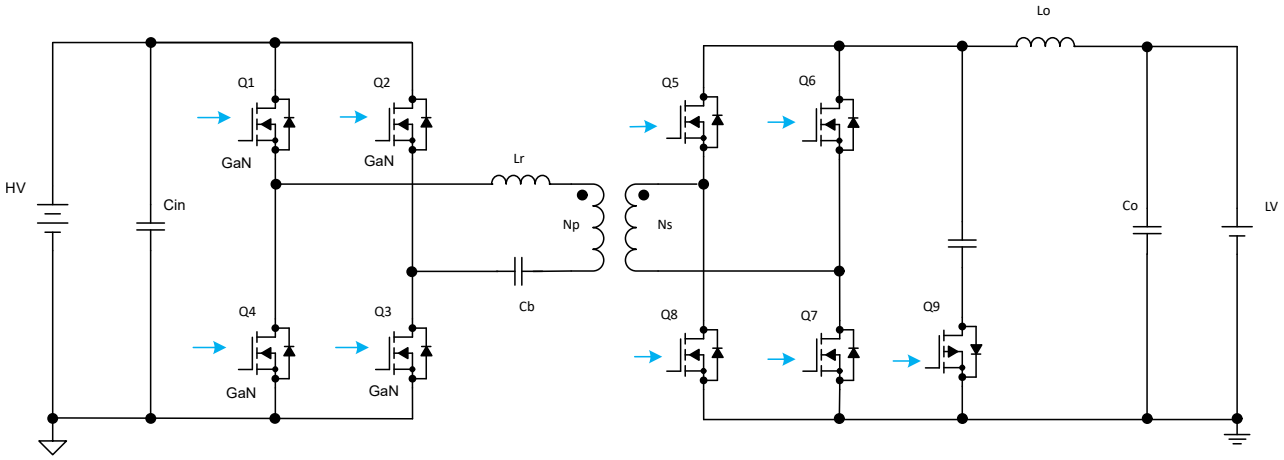

Figure 2-1. Traditional active clamp circuit for PSFB synchronous rectifier MOSFETs

Figure 2-1 delineates the principal components of the ACL circuit: the P-channel metal-oxide-semiconductor field-effect transistor (PMOS) Q9 and the snubber capacitor. The snubber capacitor is connected to the output inductor at one terminal, while the PMOS source terminal is connected to ground. In the conventional PSFB active clamp configuration, SR MOSFETs Q5 and Q7 employ identical circuit arrangements, as do Q6 and Q8. The PMOS is activated with an appropriate delay following the turn-off transition of the SR MOSFET.

Figure 2-2 illustrates the control timing scheme for the PSFB topology with ACL circuits. As shown in Figure 2-2, the PMOS switching frequency operates at twice the primary-side switching frequency (f_{sw}).

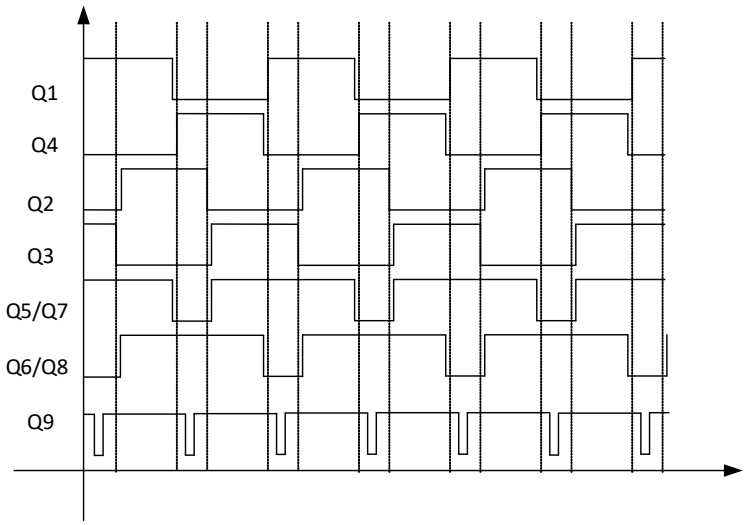

Figure 2-2. Control scheme of active clamp PMOS Q9.

Equation 2 through Equation 6 can be employed to calculate the power losses in the ACL PMOS. With the exception of conduction losses (P_{on_state}), all other loss components scale proportionally with switching frequency. Given that the PMOS switching frequency operates at twice the primary-side frequency, the associated losses are correspondingly doubled, presenting substantial thermal management challenges. These thermal considerations become increasingly critical when the switching frequency is elevated to meet miniaturization and power density requirements.

$$\mathrm{P_{on\_state}} = \mathrm{Irms}^2 \times \mathrm{Rdson} \tag{2}$$

$$\mathrm{P_{turn\_on}} = 0.5 \times \mathrm{Vds} \times \mathrm{Ion} \times \mathrm{ton} \times \mathrm{fsw} \tag{3}$$

$$\mathrm{Pturn_{off}} = 0.5 \times \mathrm{Vds} \times \mathrm{Ioff} \times \mathrm{toff} \times \mathrm{fsw} \tag{4}$$

$$\mathrm{Pdrive} = \mathrm{Vdrv} \times \mathrm{Qg} \times \mathrm{fsw} \tag{5}$$

$$\mathrm{Pdiode} = \mathrm{Isnubber} \times \mathrm{Vsd} \times \mathrm{td} \times \mathrm{fsw} \tag{6}$$

Selecting PMOS devices with figure of merit (FOM) or employing thermal interface materials with enhanced thermal conductivity represent viable approaches. However, the fundamental limitation persists that thermal stress remains concentrated within a single component, rendering effective thermal management inherently difficult.

A more effective strategy involves distributing the thermal load across multiple components through the implementation of dual active clamp circuits. As depicted in Figure 2-3, this configuration is realized by connecting the snubber capacitor terminals to the switching nodes of the secondary-side legs. In this topology, Q11 is activated exclusively following the turn-off transitions of Q5 and Q7, while Q10 is activated exclusively following the turn-off transitions of Q6 and Q8. Figure 2-4 illustrates the control timing scheme for the PSFB topology with this dual active clamp configuration.

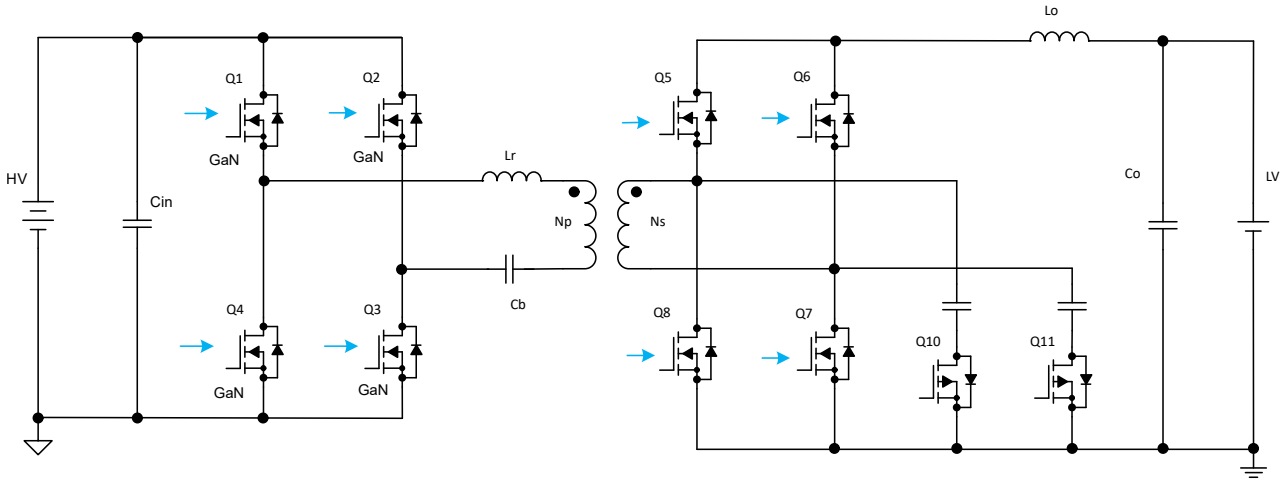

Figure 2-3. New Active Clamp Circuit for PSFB Synchronous Rectifier MOSFETs

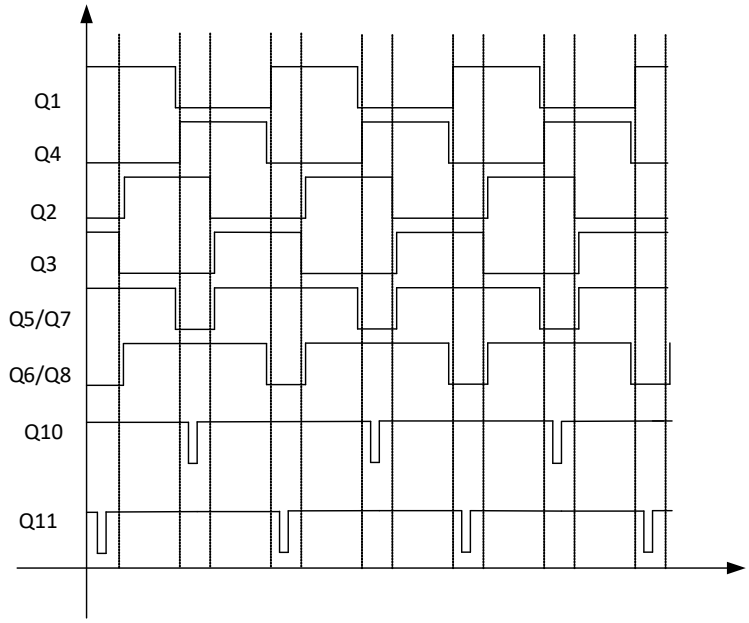

Figure 2-4. Control Scheme of the PSFB and New Active Clamp

2.1.2 PMOS Type and NMOS Type

In addition to PMOS devices, N-channel MOSFETs (NMOS) also represent a viable option for ACL circuit implementation. When selecting the appropriate ACL MOSFET type, designers should consider two fundamental design principles.

Principle One: Driver Circuit Complexity

PMOS devices are generally preferred due to the simplified driver circuit topology and reduced BOM cost. Compared to conventional NMOS driver circuits, PMOS implementations require only one additional diode and ceramic capacitor. Conversely, employing NMOS as the clamping MOSFET necessitates isolated gate driver circuits, as the NMOS source terminal is connected to the switching node rather than a fixed potential. This requirement results in substantially greater circuit complexity and elevated BOM costs. Section 2.2.2 provides comprehensive details regarding these driver circuit configurations.

Principle Two: Pulse Current Capability

NMOS transistors typically exhibit superior current-carrying capacity and faster switching characteristics compared to PMOS devices, primarily attributable to the higher electron mobility in NMOS (approximately 2-3 times greater than hole mobility in PMOS). For converters with output currents below 100A, PMOS clamping MOSFETs represent a suitable choice. However, for high-current applications—such as high-voltage to low-voltage (HV-LV) DC-DC converters with output currents approaching 200A—NMOS clamping MOSFETs are recommended due to their enhanced performance characteristics. Figure 2-5 illustrates the conventional ACL circuit topology for PSFB converters utilizing NMOS devices.

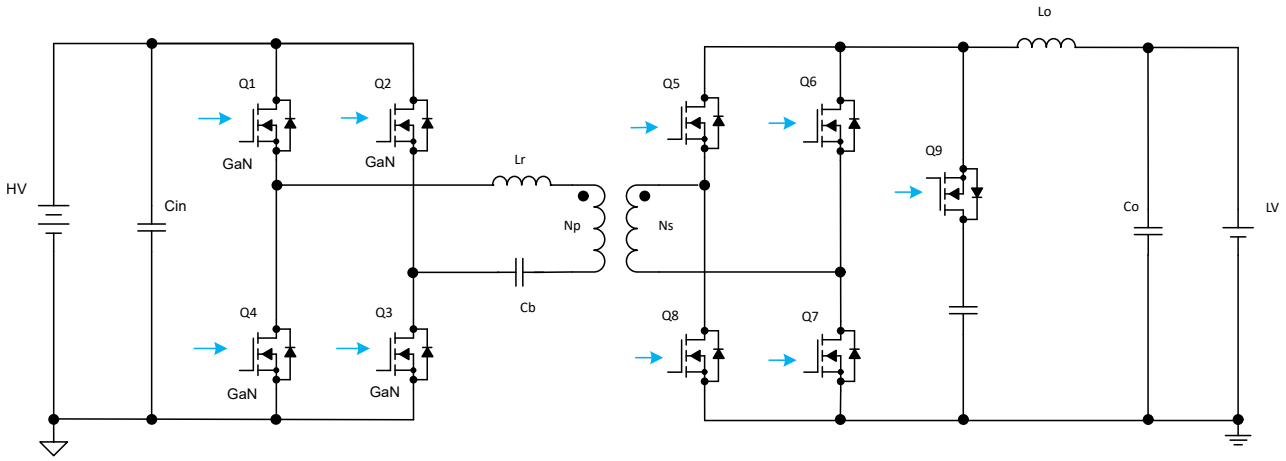

Figure 2-5. Traditional Active Clamp Circuit for PSFB using NMOS as Clamp FET

2.2 Hardware Design of ACL Circuit

2.2.1 Clamping Capacitor

The selection of an active clamp capacitor requires careful consideration of multiple design trade-offs involving voltage ripple, transient response characteristics, and overall efficiency. Key design parameters include the capacitance value (C_{clamp}) and voltage rating. The designer must evaluate the resonant frequency relative to the switching frequency, ensuring the capacitance is sufficiently large to minimize voltage ripple while remaining small enough to facilitate rapid transient response. Additionally, low equivalent series resistance (ESR) capacitor types, such as ceramic capacitors, should be selected to effectively handle resonant currents without generating excessive heat dissipation or voltage overshoot during switching transitions.

1. Determine Operating Voltages:

   When using ACL, the Vds of secondary SR FETs is clamped to

   $$\mathrm{V_{ds\_sr}} = \mathrm{K} \times \mathrm{Vin_{max}} \times \mathrm{Ns/Np} \tag{7}$$

   in which K is less than 1.5

   Given that the clamping capacitors are connected in parallel with the SR FETs, the voltage across the clamping capacitors is equivalent to the drain-to-source voltage (Vds) of the SR FETs. It is important to note that the clamping capacitors are also subjected to a DC bias voltage equal to:

   $$\mathrm{V_{dc\_bias}} = 2 \times \mathrm{D} \times \mathrm{Vin_{max}} \times \mathrm{Ns/Np} \tag{8}$$

   in which D is effective duty on transformer primary winding,

   $$0 \leq D < 0.5 \tag{9}$$

2. Select Resonant Frequency (f_r): Set f_r significantly lower than resonant frequency without ACL f_R (for example, $f_r \approx 0.1 \times f_R$ or less).

$$f_R = \frac{1}{2 \times \pi \times \sqrt{\left(\frac{\mathrm{Ns}}{\mathrm{Np}}\right)^2 \times \mathrm{L_r} \times 2 \times \mathrm{C_{oss}}}} \quad (10)$$

$$f_r = \frac{1}{2 \times \pi \times \sqrt{\left(\frac{\mathrm{Ns}}{\mathrm{Np}}\right)^2 \times \mathrm{L_r} \times \left(\mathrm{C_{clamp}} + 2 \times \mathrm{C_{oss}}\right)}} \quad (11)$$

3. Calculate C_{clamp} :

   Using the PSFB topology as an example, $C_{clamp} = 1/\left((Ns/Np)^2 \times L_r \times \left(2\pi f_r\right)^2\right)$, where L_r represents the resonant inductor on the primary side. For other topologies without a discrete resonant inductor, Lr is equivalent to the leakage inductance of the transformer secondary winding. A larger C_{clamp} results in a lower resonant frequency f_r , which corresponds to reduced voltage ripple across the capacitors. This reduction in capacitor voltage ripple decreases the Vds stress on the SR FETs; however, this also degrades the transient response performance of the converter.
4. Check I_{clamp} :

   Suppose the designed K is 1.1, voltage ripples on capacitors is $0.1 \times Vin \times Ns/Np$. Then I_{clamp} can be derived from:

$$\mathrm{I_{clamp}} = \mathrm{C_{clamp}} \times \left(0.1 \times \mathrm{Vin} \times \mathrm{Ns/Np}\right) \times T_{delay} \times \mathrm{fr} \quad (12)$$

   Based on I_{clamp} and temperature rise data of capacitors, you can decide the number of capacitors. Notice, I_{clamp} is the rms current in clamping time . Find more details about T_{delay} in Section 2.3.1.
5. Select Capacitor Type:

Use low-ESR ceramic capacitors (such as X7R or C0G etc.) for high-frequency AC performance.

Table 2-1. Summary Checklist for clamping capacitors

Parameter	Selection Criteria
V_c	Must safely handle the peak voltage, typically around $V_{in} + V_{out}$ or $2V_{in}$ (depending on topology), plus margin.
C_{clamp}	Larger C_{clamp} : Reduces drain voltage ripple (better for efficiency) but slows transient response. Smaller C_{clamp} : Improves transient response but increases ripple. Trade-off: Find the sweet spot where ripple is acceptable and transients are fast enough (for example, use design tools or datasheet recommendations).
ESR	Crucial for managing energy dissipated in the capacitor, especially during fast switching. A low ESR (ceramic caps are great) is preferred to minimize heating and voltage spikes, as the clamp circuit handles resonant currents.

2.2.2 Power Switches

The selection of a MOSFET for an ACL circuit—commonly employed to reset transformer cores in forward/ flyback converter topologies or provide protection against inductive voltage spikes—necessitates careful optimization of voltage stress ratings, switching speed characteristics, and gate drive requirements.

1. Breakdown Voltage (V_{DSS})

The MOSFET must withstand the maximum clamping voltage without entering avalanche breakdown. A V_{DSS} should be selected at least 30% higher than the expected peak clamping voltage, as calculated in Equation 7, to provide adequate margin for input voltage variations and transient voltage spikes.

2. Body Diode Characteristics

The ACL MOSFET relies on its internal body diode to conduct current during the initial reset phase. The body diode must possess adequate current-handling capability to withstand the peak reflected current. Since

current conduction occurs through the internal body diode of the MOSFET, gallium nitride (GaN) devices are not preferred for this application due to the lack of an intrinsic body diode.

Based on the I_{clamp} calculated in Section 2.2.1, an initial current rating for the FET can be determined; however, this represents only an RMS value. To obtain the peak current (I_{clamp_peak}), circuit simulation is necessary, or it can be analytically calculated by referring to methodologies outlined in "Achieving high converter efficiency with an active clamp in a PSFB converter". The "Source-Drain Pulsed Current" rating specified in the device datasheet should be verified against the calculated peak current. If the pulsed drain current $I_{D,pulse}$ of the PMOS approaches or exceeds this rating, a series power resistor can be incorporated to limit the current magnitude.

Table 2-2. Summary Checklist for clamping FETs

Parameter	Selection Criteria
V_{DSS}	Max clamp voltage + 20-30% margin.
$I_{D,pulse}$	Must exceed peak current pulse.
olarity	High-side clamps typically use N-channel; low-side can use N- or P-channel depending on the controller

2.2.3 Gate Driver

Typically, a low-side gate driver can be employed to drive a PMOS device, as illustrated in Figure 2-6. Capacitor C1 is used to generate the negative gate voltage for the PMOS, with an initial value of 10nF serving as a starting point. Diode D1 clamps the maximum positive voltage to its forward voltage drop (VF); consequently, the effective negative gate-to-source voltage applied to the PMOS is (VDD - VF).

Note that if the capacitance of C1 is excessively large, the gate signal of the PMOS will exhibit a slow fall time. Particular attention must be paid to this phenomenon when troubleshooting drain-to-source voltage (Vds) overvoltage issues during converter soft-start operation.

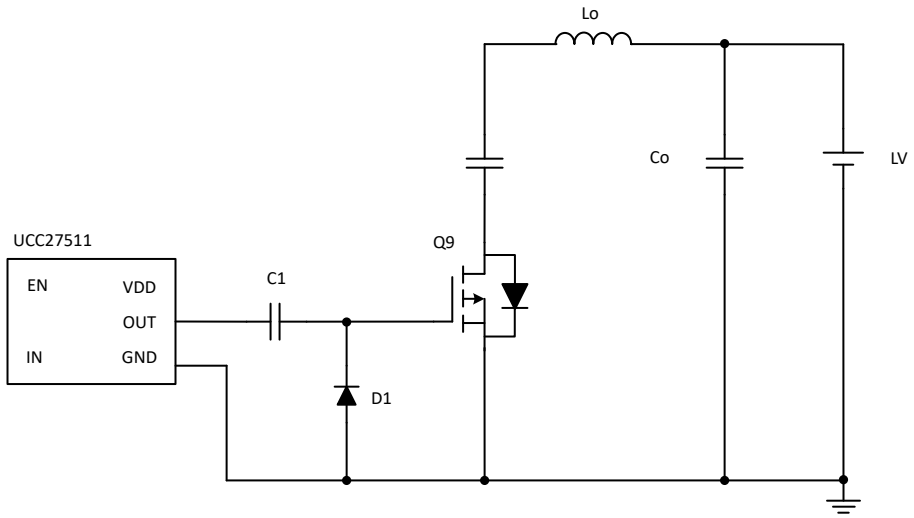

Figure 2-6. Low Side Driver for PMOS

When an NMOS device is employed as the clamping MOSFET in an ACL circuit, an isolated gate driver is required, as depicted in Figure 2-7. Alternatively, a digital isolator combined with a low-side driver can be utilized, as shown in Figure 2-8. A bootstrap circuit is implemented to provide power to the isolated components. Table 2-3 presents a selection of gate driver integrated circuits from TI that are preferred for implementation in ACL circuit applications.

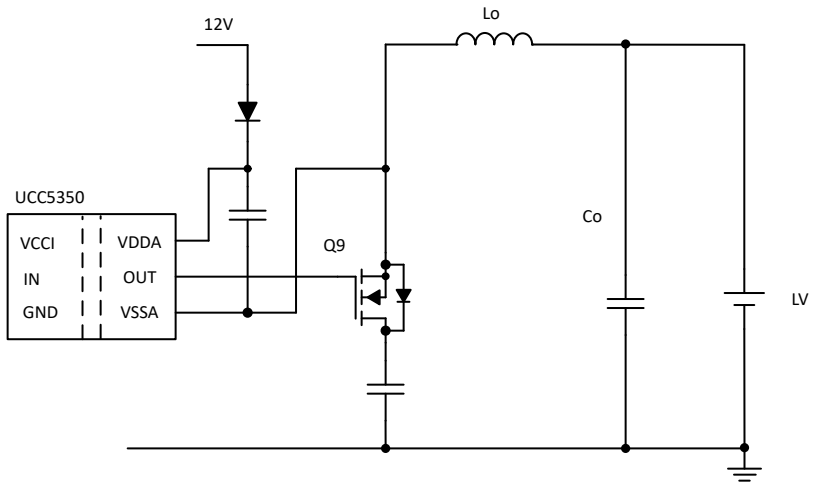

Figure 2-7. Isolated Driver for NMOS

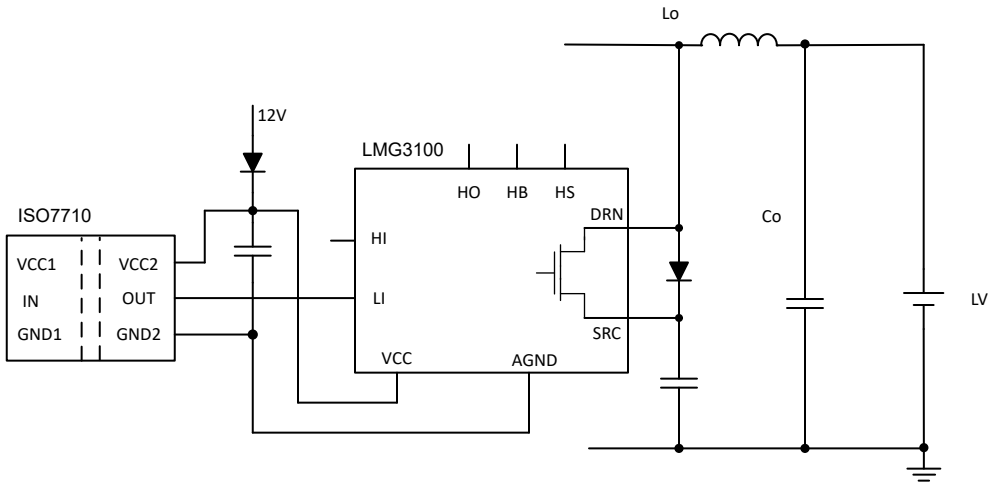

Figure 2-8. Digital Isolator and Low Side Driver for NMOS

Table 2-3. TI Components in ACL

Type	Part Number	Specification
Low side driver	UCC27511A	Single-Channel High-Speed Low-Side Gate Driver With 4A Peak Source and 8A Peak Sink
	UCC27524A1	Dual 5A, High-Speed, Low-Side Gate Driver With Negative Input Voltage Capability
Isolated driver	UCC5350	Single-Channel Isolated Gate Drivers
	UCC21331	4A, 6A, 3.0kVRMS Isolated Dual-Channel Gate Driver
Digital isolator	ISO7710	High Speed, Robust EMC Reinforced Single-Channel Digital Isolator
	ISO6420	General-Purpose, Basic and Reinforced, Dual-Channel Digital Isolators

2.3 Software Design of ACL Circuit

Following the completion of the hardware circuit design, the control strategy for the ACL power switches must be implemented. The performance of the active clamping circuit is significantly influenced by two critical parameters: the turn-on delay time and the turn-on duration of the active clamp switch. Prior to analyzing

the impact of these parameters, it is essential to establish a comprehensive understanding of the ACL circuit operating principles. The analysis is conducted using the circuit schematic illustrated in Figure 2-9, with the corresponding timing diagram shown in Figure 2-10.

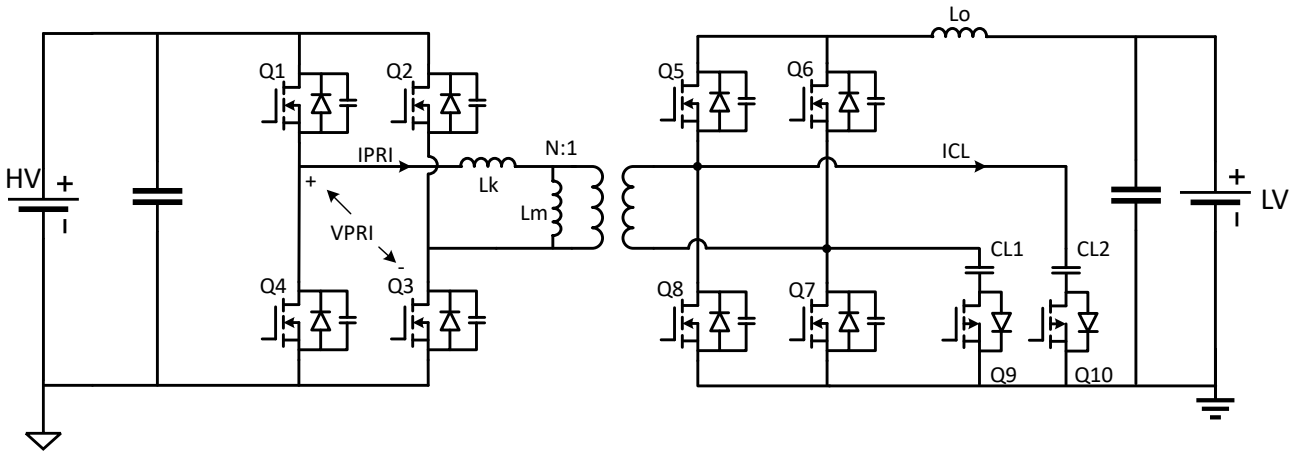

Figure 2-9. Block Diagram of Full Bridge Synchronous Rectifier with Active Clamping Circuit

[t0-t1]: Prior to t0, switches Q1 and Q2 are conducting, with the primary current IPRI flowing in the direction opposite to the reference polarity defined in Fig. 15. At t0, Q2 undergoes turn-off, causing IPRI to charge the Coss of Q2 while simultaneously discharging the Coss of Q3. Consequently, the primary voltage VPRI rises from 0V to 400V. During this interval, synchronous rectifiers Q5 through Q8 remain in conduction to maintain the load current. The transformer secondary winding is effectively short-circuited, resulting in zero drain-to-source voltage (VDS = 0V) across Q8.

[t1-t2]: At t1, Q3 is turned on. Since the Coss of Q3 has been fully discharged during the dead time, Q3 achieves zero-voltage switching (ZVS) turn-on. Due to the short-circuit condition of the transformer secondary, the primary voltage VPRI is applied entirely across the leakage inductance Lk, causing IPRI to decrease rapidly, reverse direction, and then increase rapidly in the opposite polarity. During this interval, the secondary-side operation remains identical to that of [t0-t1]. Because the input voltage is applied to VPRI while the transformer remains short-circuited, energy cannot be transferred to the secondary side. Consequently, this interval represents the duty cycle loss period.

[t2-t3]: At t2, as IPRI increases sufficiently to support the load current, synchronous rectifiers Q6 and Q8 cease freewheeling conduction, enabling zero-current switching (ZCS) turn-off shortly after t2. Following the turn-off of Q6 and Q8, the drain-to-source voltage VDS of Q8 begins to rise gradually. When VDS exceeds the active clamp capacitor voltage VCL2, the voltage stress is clamped at VCL2.

As illustrated in Figure 1-3, voltage stress arises from resonance between the leakage inductance Lk and the output capacitance Coss. With the active clamp (ACL) circuit implemented, during interval [t2-t3], the equivalent capacitance comprises Coss in parallel with the clamp capacitor CL2. Since CL2 is significantly larger than Coss (CL2 >> Coss), the voltage fluctuation is substantially reduced, and the oscillation frequency is considerably lower. The resonant period can be expressed as:

$$T = 2\pi\sqrt{\left(\frac{1}{N}\right)^2 \times L_k \times \left(2C_{oss} + C_{CL2}\right)} \quad (13)$$

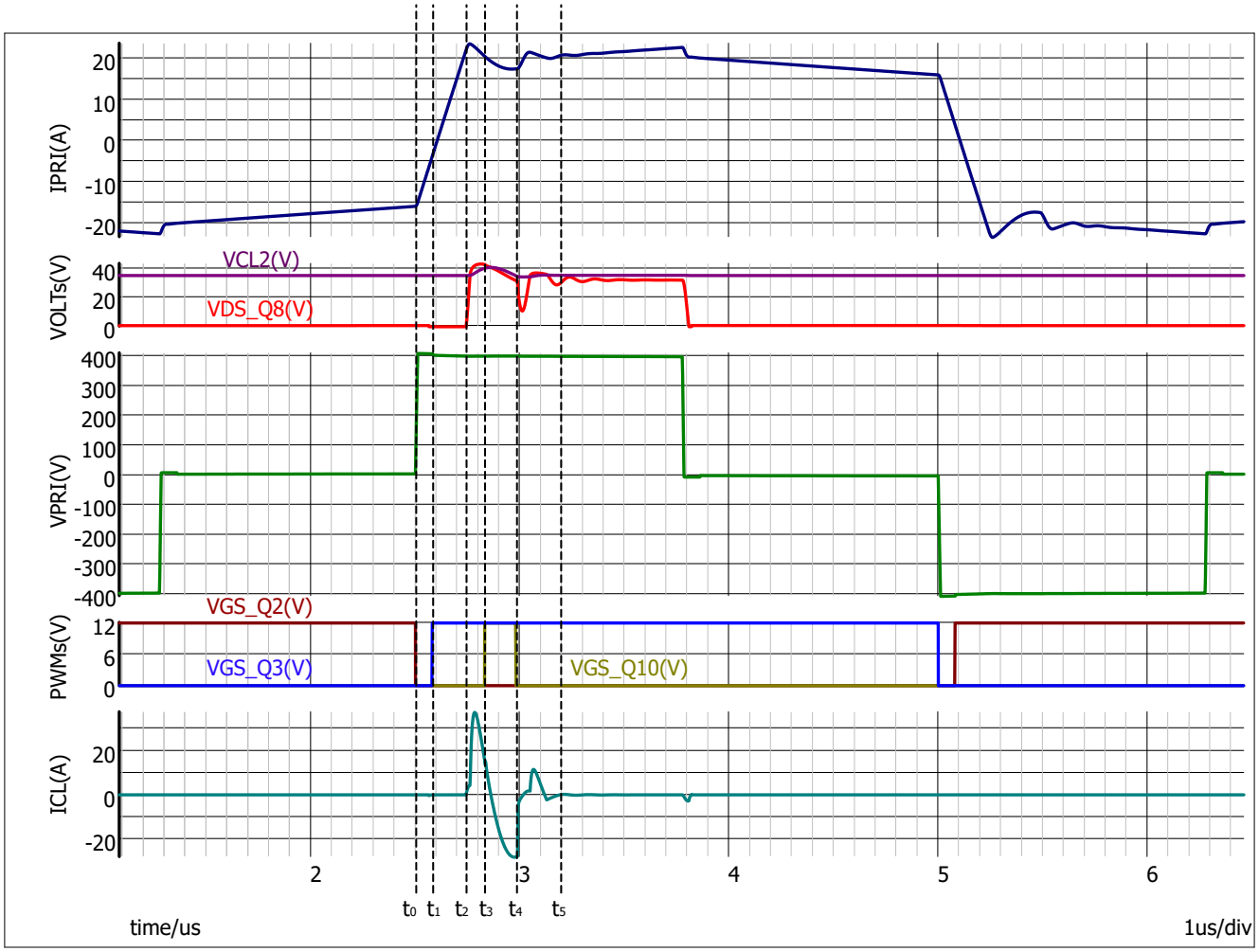

Figure 2-10. Sequence of Phase-Shifted Full Bridge with Active Clamping Circuit

[t3-t4]: At t3, the active clamping switch Q10 is turned on. Since the clamp current ICL remains in the forward direction at this instant, the body diode of Q10 is conducting in freewheeling mode, thereby enabling zero-voltage switching (ZVS) turn-on of Q10. The conduction of Q10 establishes a discharge path for the clamp capacitor CL2. Consequently, after half a resonant cycle, the direction of ICL reverses, and CL2 begins discharging, transferring stored energy to the output side.

When ICL reverses direction, this supplies load current in conjunction with the primary-reflected current IPRI. Since the load current remains essentially constant during this interval, a corresponding dip in IPRI is observed to maintain current balance.

[t4-t5]: At t4, the active clamping switch Q10 is turned off. The turn-off of Q10 eliminates the discharge path for CL2, causing ICL to decay rapidly to zero. Since the load current remains constant, the output capacitance Coss of Q8 supplies load current together with IPRI, resulting in a significant reduction in the drain-to-source voltage VDS of Q8. Subsequently, as IPRI increases, the VDS of Q8 is recharged back to the clamping voltage level.

After VDS of Q8 reaches the clamping voltage, the circuit enters a subsequent resonant cycle, causing ICL to rise and charge CL2. However, the energy content of this resonant cycle is substantially lower than that of the previous cycle; consequently, the clamp voltage VCL2 remains nearly constant. Since Q10 is no longer conducting and no discharge path exists, the resonance terminates after half a cycle.

2.3.1 Turn-on Delay

From the preceding analysis, the interval [t1-t2] constitutes the duty cycle loss phase of the phase-shifted full-bridge topology. During this phase, the primary current IPRI continues to increase, while all secondary-side power switches remain in freewheeling mode. If the active clamping switch conducts during this stage, the clamp

capacitor CL2 discharges rapidly, generating a large reverse clamp current ICL. This results in undesirable energy backflow from the active clamping capacitor to the primary side. Therefore, the minimum turn-on delay, measured relative to the turn-off instant of Q2, must equal or exceed the duration of the duty cycle loss period, corresponding to interval [t0-t2] in Figure 2-10.

Assuming the output inductor current is I_{Lo} , during interval [t0-t2] the primary current IPRI transitions from $-I_{Lo}/N$ to $-I_{Lo}/N$. Consequently, the minimum turn-on delay can be expressed as:

$$\mathrm{T_{dmin}} = 2 \times \mathrm{L_k} \times \mathrm{I_{Lo}}/\mathrm{N} \times \mathrm{V_{in}} \tag{14}$$

From this equation, the minimum turn-on delay depends on several factors: it decreases with higher input voltage, lighter load current, and smaller resonant inductance. For the specific DC-DC converter, the worst case of the minimum turn-on delay is in the scenario where the input voltage is the minimum value, and the load current is in the full load.

At instant t3 within interval [t3-t4], the clamp current ICL crosses zero and reverses direction. If the ACL switch is turned on prior to this zero-crossing, the body diode conducts in freewheeling mode, enabling ZVS turn-on. Therefore, the maximum turn-on delay, measured relative to the turn-off of Q2, is constrained by the zero-crossing instant of the ICL current. The maximum turn-on delay can be expressed as:

$$T_{dmax} = T_{dmin} + \frac{T}{2} \tag{15}$$

In reference design PMP41078, the switching frequency is 200kHz, the input voltage range is 200V to 450V, the output voltage range is 9V to 16V, and the maximum output power is 3.5kW. Based on the equations derived above, the calculated minimum turn-on delay is 265ns, and the calculated maximum turn-on delay is 557.5ns; therefore, a design value of 400 ns is selected to provide adequate margin.

2.3.2 Turn-on Duration

Following the turn-off of the active clamping switch, the active clamping capacitor loses its discharge path. Consequently, the minimum turn-on duration of the active clamping switch should be designed to achieve volt-second balance for the desired clamping voltage. As illustrated in Figure 2-10, if Q10 is turned off at the instant when ICL crosses zero, ZCS turn-off can be achieved. The turn-on duration can be configured according to this principle to optimize switching performance. This time interval can be obtained through simulation.

Under varying operating conditions, the worst-case scenario occurs when the phase shift angle reaches its maximum value, which is typically determined by the voltage regulation range requirements. At this operating point, the equivalent duty cycle of the primary voltage VPRI reaches its minimum value. The turn-on transition of synchronous rectifier Q8 is aligned with the falling edge of VPRI; therefore, the maximum conduction duration of the active clamp switch Q10 must verify turn-off prior to the turn-on of Q8, which is the minimum effective duty cycle minus the time interval of duty-cycle loss. Failure to satisfy this constraint results in Q8 short-circuiting the clamp capacitor CL2, generating excessive transient current.

In reference design PMP41078, the minimum primary-side equivalent duty cycle is 20%. Consequently, in the worst-case scenario, the sum of the turn-on delay and turn-on duration must not exceed 500ns. Since the turn-on delay is selected as 400ns, the turn-on duration is configured as 100ns in PMP41078.

From Figure 2-11to Figure 2-12 are waveforms in reference design PMP41078. Figure 2-11 shows the waveforms without any clamping circuit, and Figure 2-12 and Figure 2-13 are the waveforms with active clamping. CH1 is the VGS of one synchronous rectifier power switch, CH2 is the VDS of this power switch, CH3 is the waveform of the transformer primary side voltage, CH4 is the waveform of the transformer primary side voltage.

Figure 2-11and Figure 2-12 are measured at 200V input voltage (Minimum input voltage). The voltage stress is 32V without active clamping, while the voltage stress can be reduced to 22V with active clamping. The voltage overshoot is suppressed from 92% to 30%.

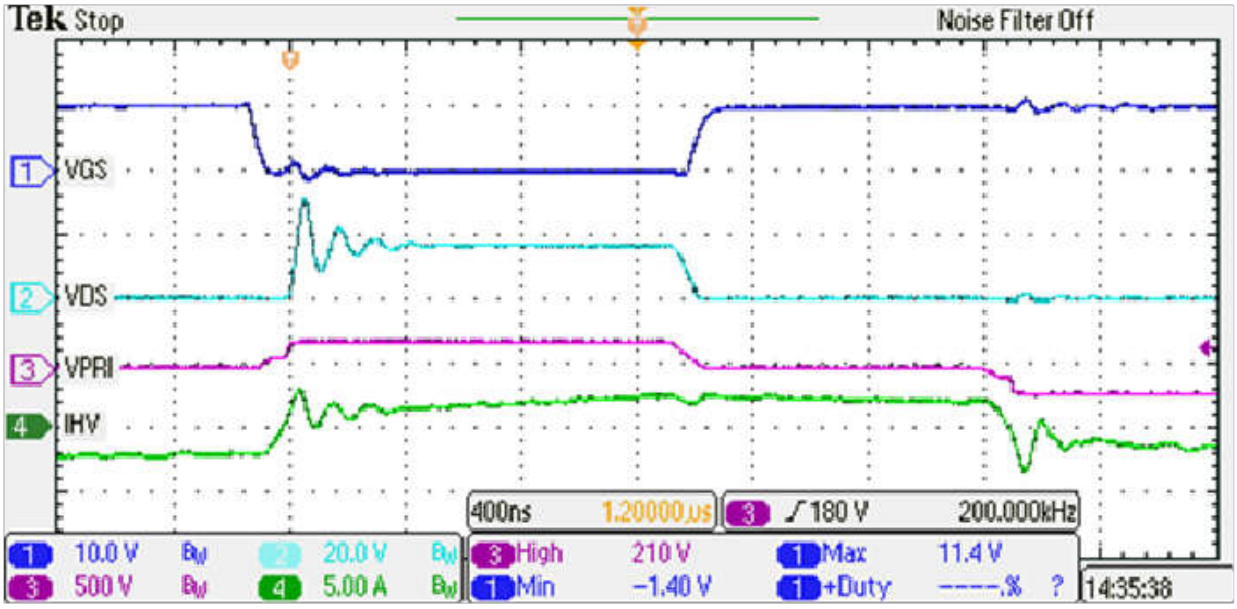

Figure 2-11. No Clamping at Vin = 200V, Iout = 20A

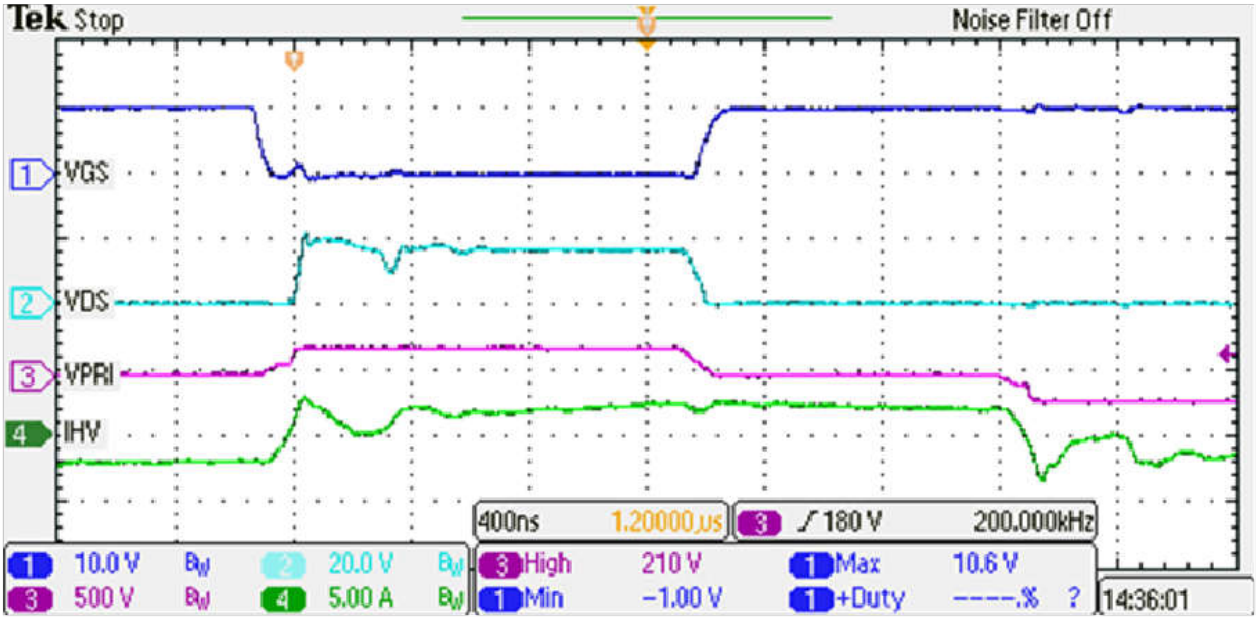

Figure 2-12. Active Clamping at Vin = 200V, Iout = 20A

Figure 2-13 is measured at 450V input voltage (Maximum input voltage). The voltage stress is 45.6V with active clamping. Therefore, 60V power switch is sufficient in this DC-DC converter.

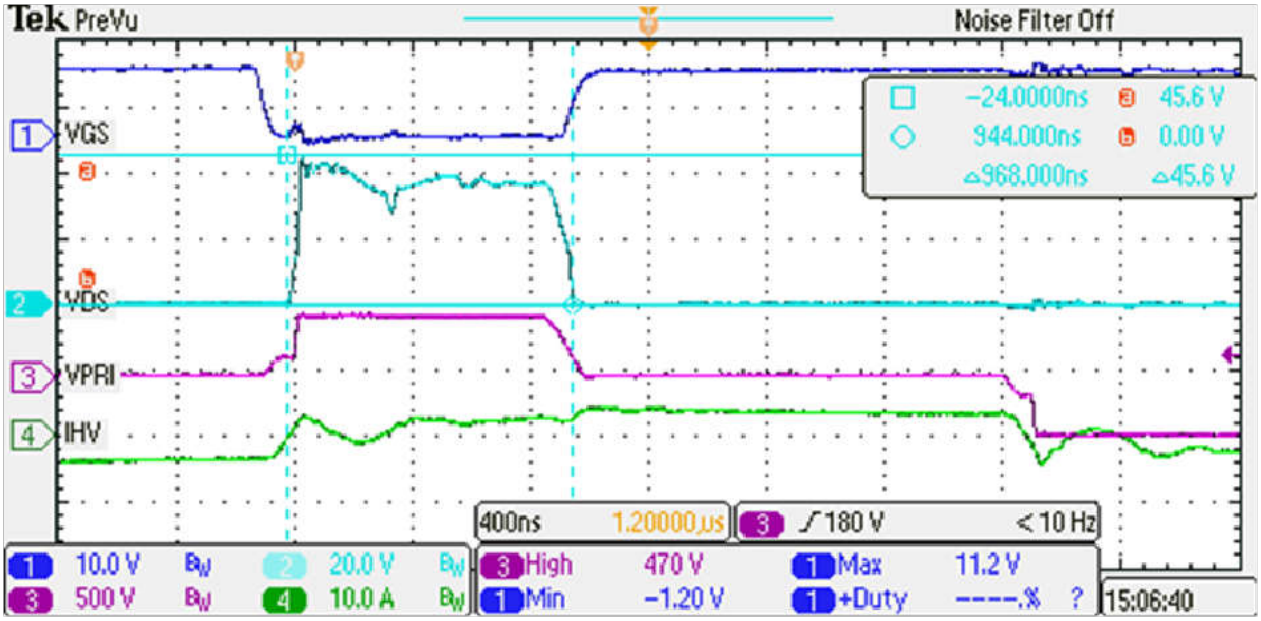

Figure 2-13. Active Clamping at Vin = 450V, Iout = 20A

Figure 2-14 is measured at 320V input voltage. The CH1 is the voltage on the active clamping capacitor. In each cycle, the voltage on the capcitor is stabilized in 28V, and this is charged to 32.8V to absorb the resonant energy.

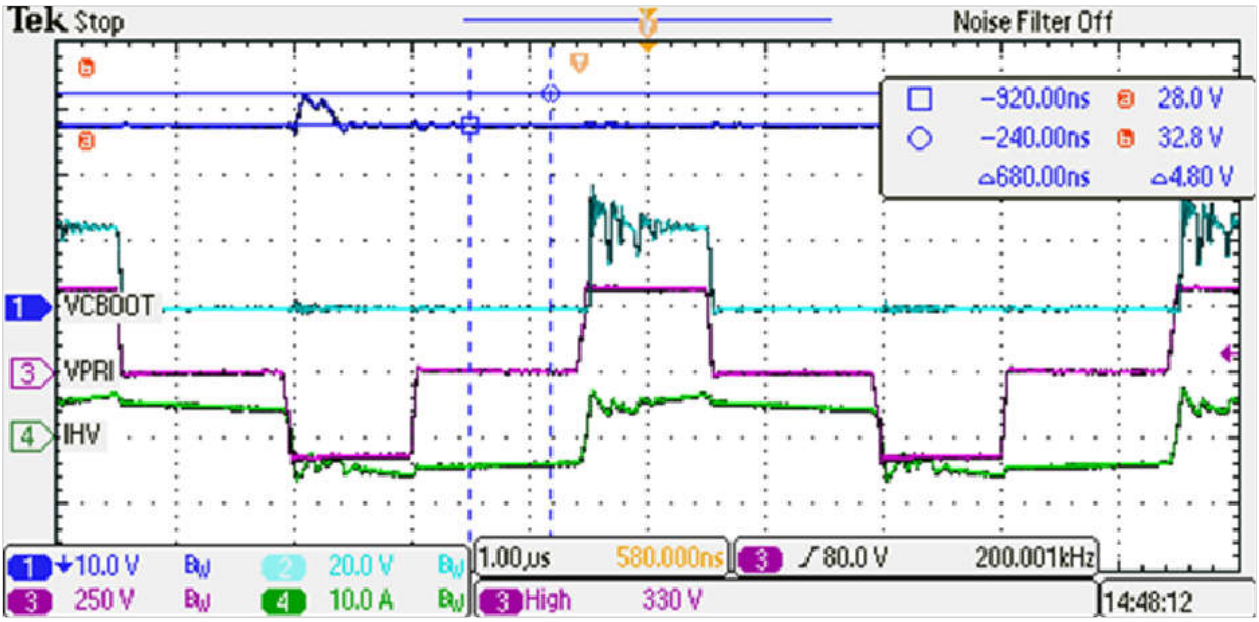

Figure 2-14. Voltage on the Active Clamping Capacitor

PMP41078 and PMP41139 are reference designs used in automotive application. The PMP41078 is used in 400V high-voltage battery applications, while the PMP41139 is used in 800V high-voltage battery applications. PMP23126 and PMP22951 are reference designs used in industry application, which has different specs compared to automotive applications. The PMP23126 is used in 12V output applications, while the PMP22951

is used in 54V output applications. The acitve clamping circuit illustrated in the paper had been verified in these reference designs.

3 Summary

This application note primarily examines the mechanisms underlying voltage stress generation in full-bridge converter topologies and presents an overview of principal clamping strategies. For the widely adopted active clamping approach, comprehensive design methodologies encompassing both hardware circuit implementation and software control algorithms are presented. These design principles have been validated through practical reference design implementations.

4 References

1. Texas Instruments, PMP41078 High-voltage to low-voltage DC-DC converter reference design with GaN HEMT, product page.
2. Texas Instruments, PMP41139 3.5kW, 800V to 14V DC/DC converter reference design, product page.
3. Texas Instruments, PMP23126 3-kW phase-shifted full bridge with active clamp reference design with > 270-W/in3 power density, product page.
4. Texas Instruments, PMP22951 54-V, 3-kW phase-shifted full-bridge with active clamp reference design, product page.
5. Texas Instruments, *Achieving high converter efficiency with an active clamp in a PSFB converter*, analog design journal.
6. Texas Instruments, *Phase-shifted full-bridge converter fundamentals*, seminar.

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