Application Note

How to Avoid False HDCP-Triggered AV MUTE Mode in FPD-LINK III DS90UB94x and DS90UB92x Devices

Violet Lei, Shelly Xie

ABSTRACT

FPDLINK III DS90UH94x deserializers implement a mode called AV MUTE which deserializers enter when the value 0x666666 is received during the blanking period (when DE=LOW). When deserializers enter AV MUTE mode, the device mutes the output video signal and audio signal, resulting in a black screen. In very rare circumstances, DS90UB94x deserializers can inadvertently enter the AV MUTE when the SoC in the systems sends signal (0x666666) during the blanking period or when a module of the system is not designed in such a way that it causes a large amount of noise interference.

This application note analyzes the causes of devices inadvertently entering AV MUTE at both the system and chip levels and provides a comprehensive design to prevent this AV MUTE mode from occurring, thus preventing systems from experiencing a black screen due to accidental AV MUTE mode entry.

1 Introduction

In HDCP-capable DS90UH94x devices, the AV MUTE feature enables users to block the transmission of both audio and video signals from the deserializer. This functionality was not intended for use in non-HDCP DS90UB94x devices; however, under specific conditions, DS90UB94x deserializers can inadvertently enter AV MUTE mode. The device triggers AV MUTE state upon detection of the defined data pattern 0x666666 during the blanking period. Analysis has confirmed that in rare instances, the DS90UB94x deserializers can receive random data matching the AV MUTE command pattern, leading to unintended activation of AV MUTE mode.

To prevent FPDLINK from entering AV MUTE mode incorrectly and causing a black screen, TI has applied multiple solutions from a system and chip perspective to limit FPDLINK to incorrectly trigger AV MUTE. This application note details the causes and designs that caused FPDLINK to enter AV MUTE mode.

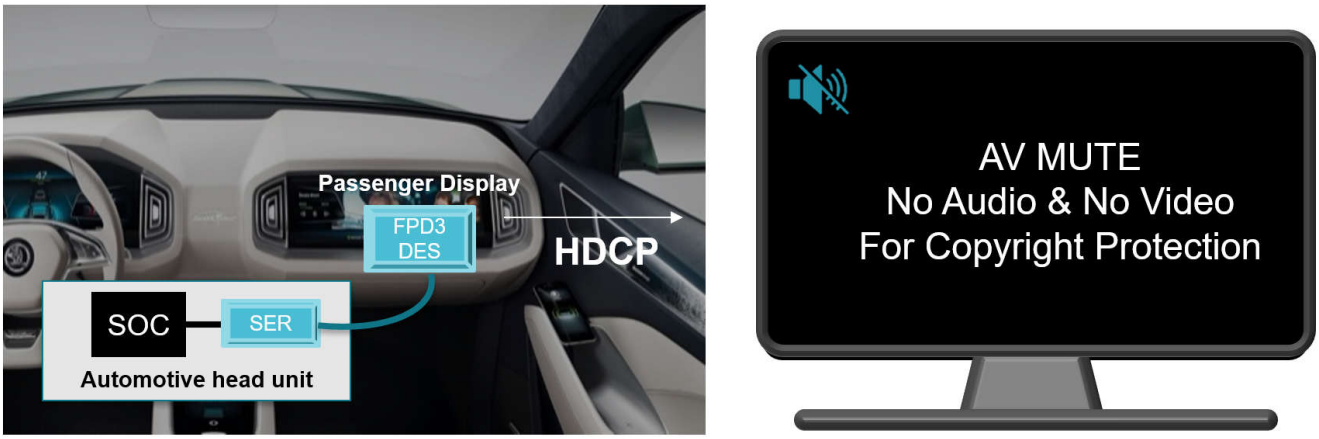

Figure 1-1. HDCP Copyright Protection

2 AV MUTE Mode

2.1 AV MUTE Mode in HDCP

HDCP (High-bandwidth Digital Content Protection) was developed by Intel Corporation as a form of digital copy protection. The purpose is to safeguard copyrighted content from being illegally intercepted as it travels from a source device to a display device. The core of HDCP is a process known as the *handshake*. This is a rapid, continuous dialogue between the source and receiver.

1. Authentication: The source and receiver device exchange public keys (KSVs) to verify that both are licensed and authorized devices. The source and receiver check these keys against a revocation list of known-compromised hardware.
2. Encryption: Once authenticated, they create a shared secret key. The source device uses this key to encrypt, or *scramble* the video data, making it unintelligible to any unauthorized device.
3. Decryption and Monitoring: The receiver uses the same key to decrypt the data in real-time. The devices then continuously monitor the connection every few seconds.

This process is highly sensitive. If the handshake is interrupted (by turning devices on in the wrong order or a loose cable) the transmission stops, resulting in a blank screen. This fragility is why a simple power-cycle of all devices often resolves the problem, as this forces a clean renegotiation of the entire handshake.

AV MUTE is a feature to temporarily blank the video and pause the audio, and it is also manages HDCP. In the context of HDCP, using AV MUTE can help maintain the HDCP link during changes in video resolution, and this can pause encryption while keeping the authentication active. When a source device changes video resolutions, this can cause a temporary loss of signal. Using AV MUTE pauses the video and audio and pauses HDCP encryption at the same time, which allows the system to maintain the HDCP link and re-authenticate the new resolution without interruption.

Figure 2-1 shows the encryption and decryption process for HDCP, which typically transmits encrypted information during DE=LOW.

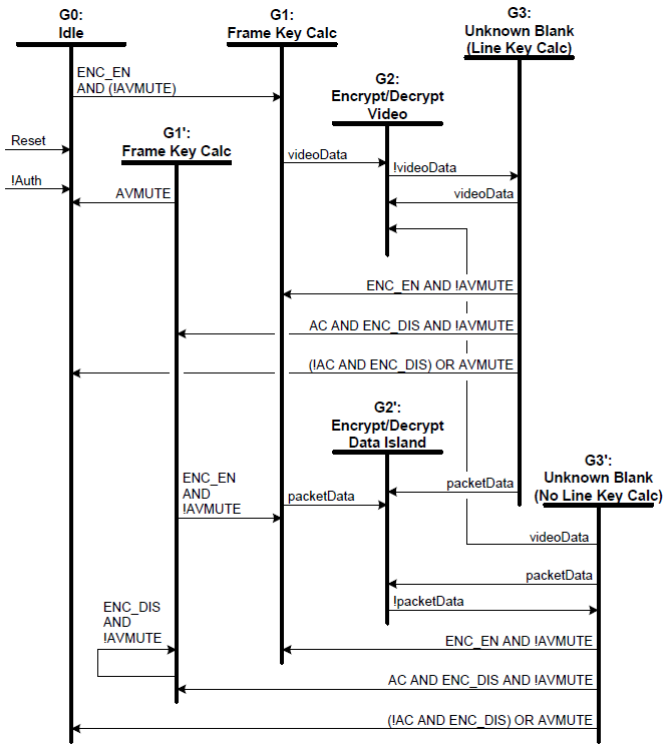

Figure 2-1. HDCP Encryption and Decryption State Diagram (EESS)

2.2 FPD-Link HDCP Device Family-UB and UH

FPD-Link III and IV devices are named according to the following rules; see Figure 2-2. In this paper, UB and UH is used to distinguish whether a device supports HDCP.

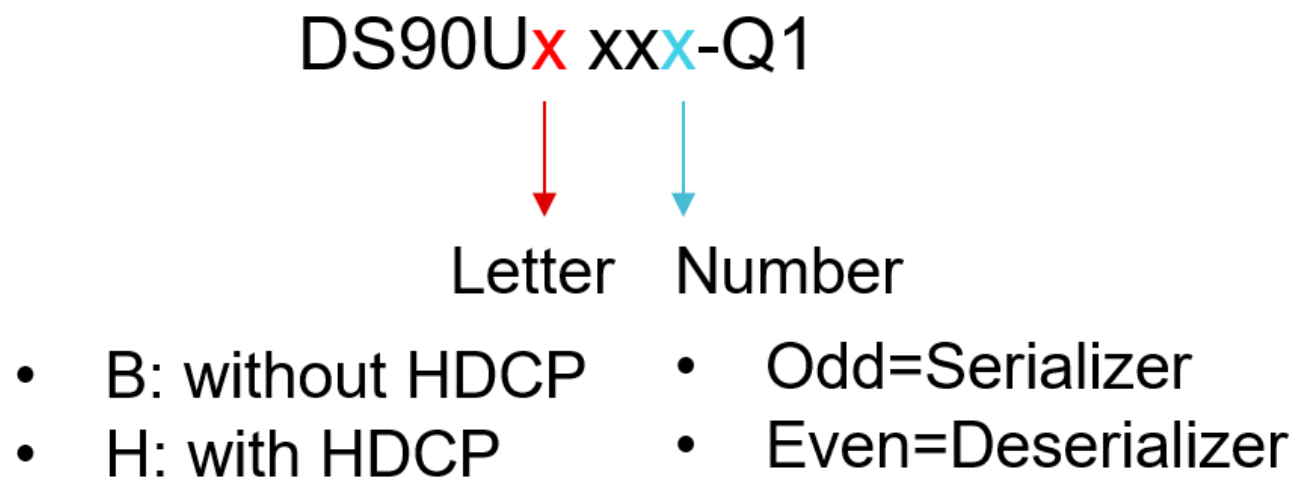

Figure 2-2. FPD-Link Nomenclature

The HDCP Cipher function is implemented in the serializer per HDCP v1.4 specification. The serializer provides HDCP encryption of audiovisual content when connected to an HDCP capable source. HDCP authentication and shared key generation is performed using the HDCP Control Channel, which is embedded in the forward and backward channels of the serial link. On-chip Non-Volatile Memory (NVM) is used to store the HDCP keys. The confidential HDCP keys are loaded by TI during the manufacturing process and are not accessible externally to the device.

Table 2-1. FPD-Link III and IV Devices

SerDes	Without HDCP FPD-Link III IV	With HDCP FPD-Link III IV
Serializer	DS90UB925Q-Q1	DS90UH925Q-Q1
	DS90UB927Q-Q1	DS90UH927Q-Q1
	DS90UB929Q-Q1	DS90UH929Q-Q1
	DS90UB941AS-Q1	DS90UH941AS-Q1
	DS90UB947Q-Q1	DS90UH947Q-Q1
	DS90UB949Q-Q1	DS90UH949Q-Q1
	DS90UB949A-Q1	DS90UH949A-Q1
	DS90UB981-Q1	DS90UH981-Q1
	DS90UB983-Q1	DS90UH983-Q1
	DS90HB983-Q1	DS90HH983-Q1
Deserializer	DS90UB926Q-Q1	DS90UH926Q-Q1
	DS90UB928Q-Q1	DS90UH928Q-Q1
	DS90UB948-Q1	DS90UH948-Q1
	DS90UB940-Q1	DS90UH940-Q1
	DS90UB940N-Q1	DS90UH940N-Q1
	DS90UB988-Q1	DS90UH988-Q1
	DS90UB984-Q1	DS90UH984-Q1
	DS90HB984-Q1	DS90HH984-Q1

The UH device supports the AV MUTE functionality of the HDCP when receiving the specifically defined data pattern *666666* during the blanking period (DE = LOW). When there are *555555* patterns during the blanking period, the UH device exits from AV MUTE status

Once the device enters the AV MUTE state, the device mutes both audio and video outputs, resulting in a black display screen.

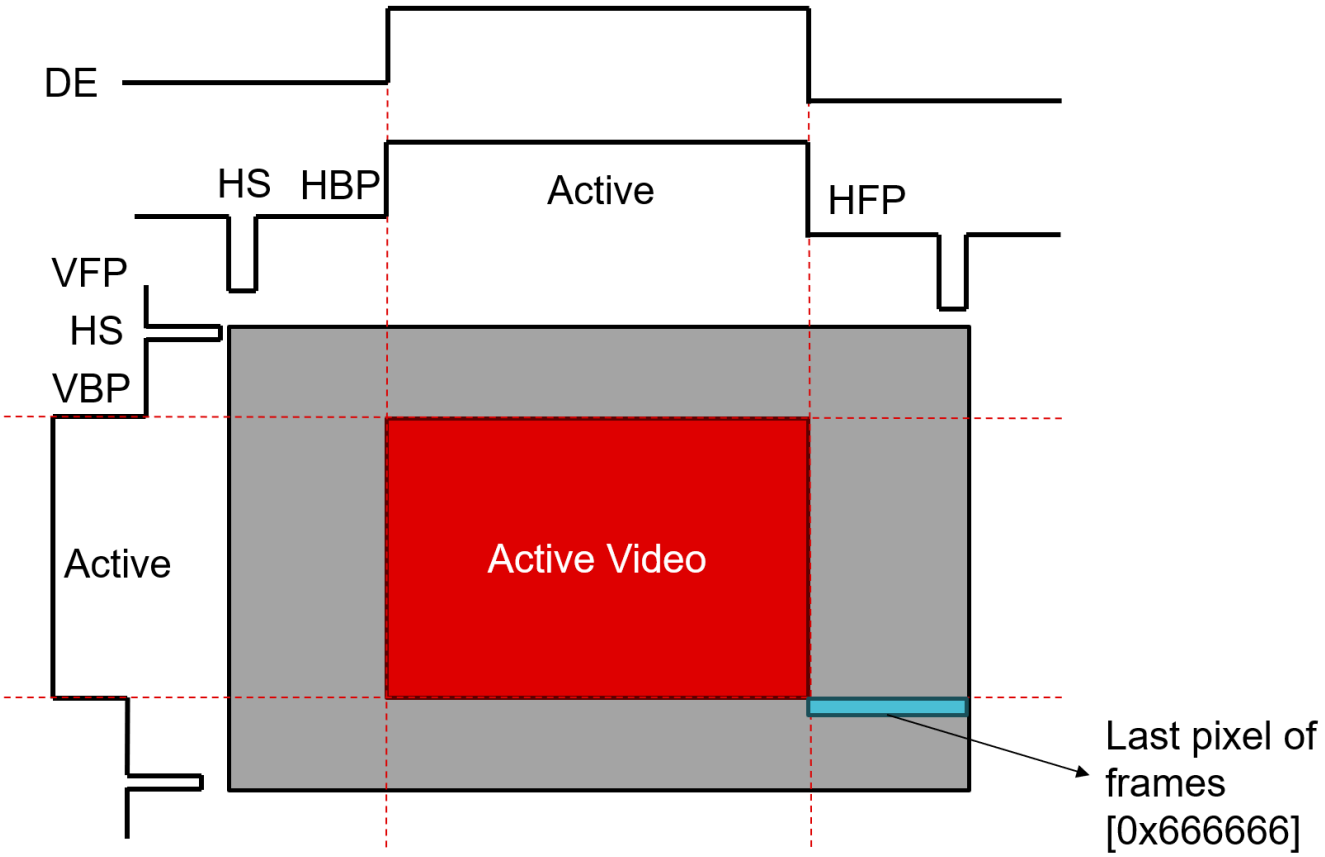

Figure 2-3. How to Enter AV MUTE Mode in UH Device

3 UB Device Can Incorrectly Enter AV MUTE State

By default, UB Serializers send all video data, including that which occurs during blanking intervals (when DE = LOW). UB Serializers can be made to function like HDCP (UH) Serializers, and block video data during blanking intervals.

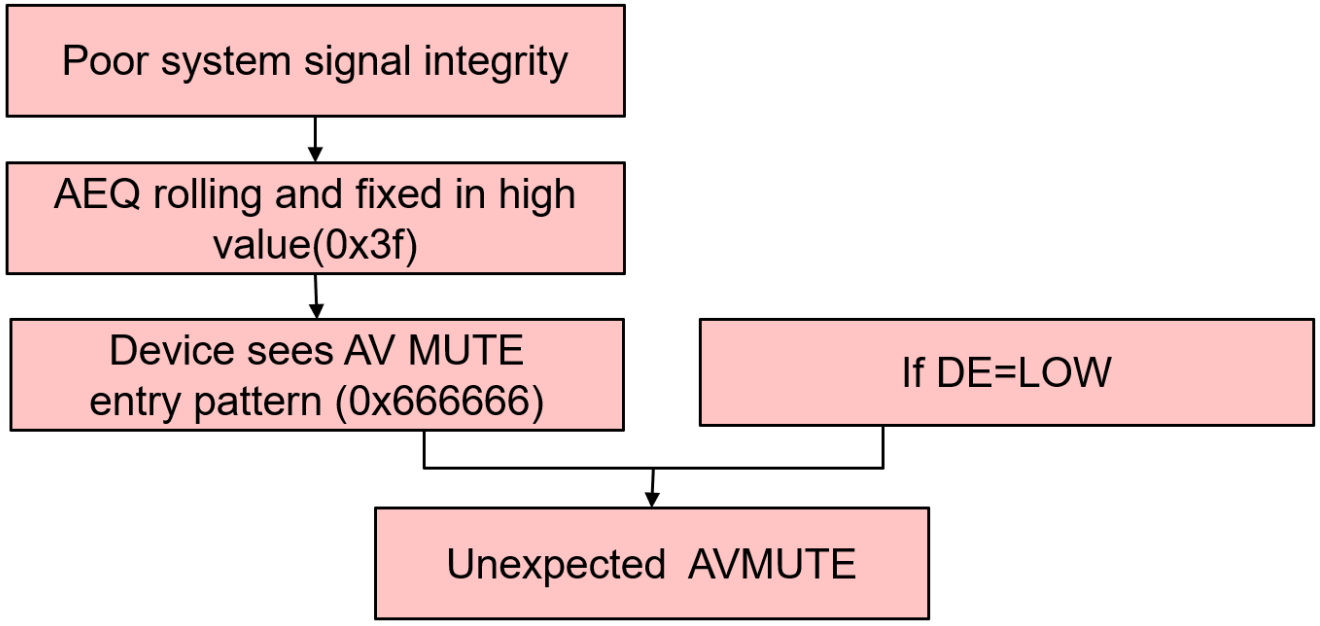

Figure 3-1. Two Ways to Enter AVMUTE

When using FPD-Link III for IVI *UB* Serializers, it is possible to send video data during the blanking period (DE = LOW). If a specific pattern (0x666666) is sent during the blanking period, the companion deserializer enters AV MUTE mode. When entering AV Mute mode, messages such as device diagnostics such as LOCK, Link, PLL, and BIST of the FPD-Link device are all normal, but the screen is black.

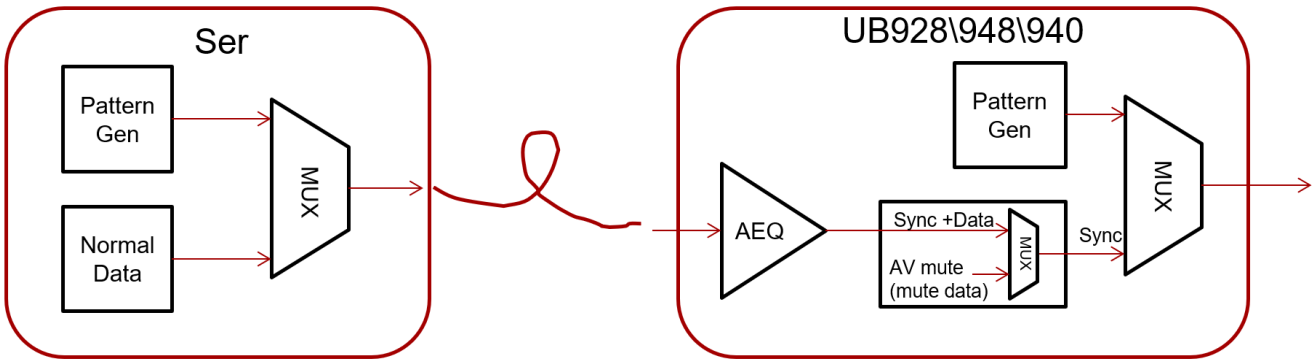

Figure 3-2. Affected Deserializers

Note

When any of the serializer and the DS90UB928\948\940-Q1 deserializer pair, it is possible to enter AV MUTE incorrectly; the DS90UB940N-Q1 is not affected by this issue.

The FPD-Link receiver inputs incorporate an adaptive equalizer (AEQ) to compensate for signal degradation from the communications channel and interconnect components. Each RX port signal path continuously monitors cable characteristics for long-term cable aging and temperature changes. The AEQ is primarily intended to adapt and compensate for channel losses over the lifetime of a cable installed in an automobile.

The AEQ attempts to optimize the equalization setting of the RX receiver. This adaption includes compensating insertion loss from temperature effects and aging degradation due to bending and flexion. To determine the maximum cable reach, factors that affect signal integrity such as jitter, skew, inter-symbol interference (ISI), crosstalk, and so forth, must also be considered. The FPD-Link III receiver inputs incorporate an adaptive equalizer (AEQ) to compensate for signal degradation from the communications channel and interconnect components. Each RX port signal path continuously monitors cable characteristics for long-term cable aging and temperature changes. The AEQ is primarily intended to adapt and compensate for channel losses over the lifetime of a cable installed in an automobile. The AEQ attempts to optimize the equalization setting of the RX receiver. This adaption includes compensating insertion loss from temperature effects and aging degradation due to bending and flexion. To determine the maximum cable reach, factors that affect signal integrity such as jitter, skew, inter-symbol interference (ISI), crosstalk, and so forth, must also be considered.

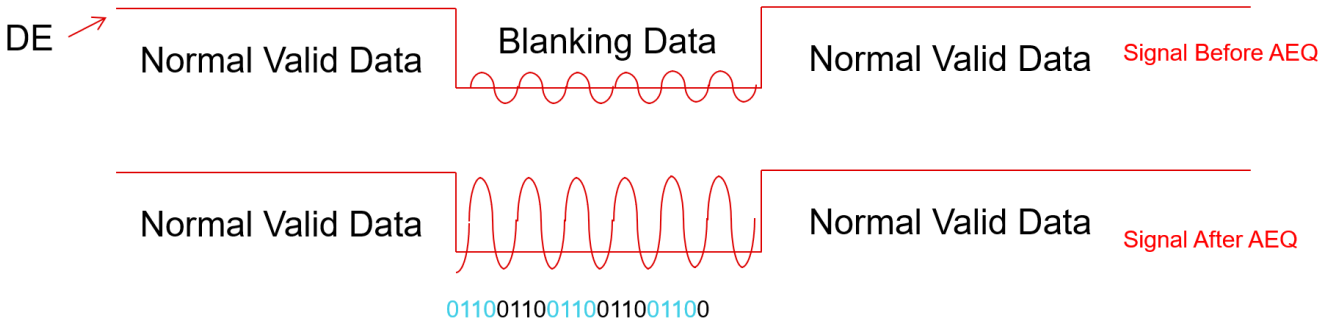

Figure 3-3. AEQ Incorrectly Identifies Blanking Data as 0x666666

If an FPD3 deserializer has already locked to a serializer and lock drops, the AEQ algorithm with increment the EQ value and try to relock to the serializer. The deserializer repeats this process until it is able to successfully re-lock to the serializer. If the EQ reaches the max EQ value, this process restarts at the minimum EQ value. If the system work environment is not stable, it is possible that UB928\948\940 enter and exit of lock status several times and when it relocks at a stable state, the final EQ value can end up at a very high value, such as 0x3F.

When the AEQ is higher value, such as 0x3F; if there is some periodic noise present in the system within the blanking period, the AEQ will boost this noise and the DS90UB94x deserializer may interpret it as a special pattern *666666* and enter AV MUTE mode. Figure 3-3 shows this situation.

4 How to Prevent Entering AV MUTE Mode

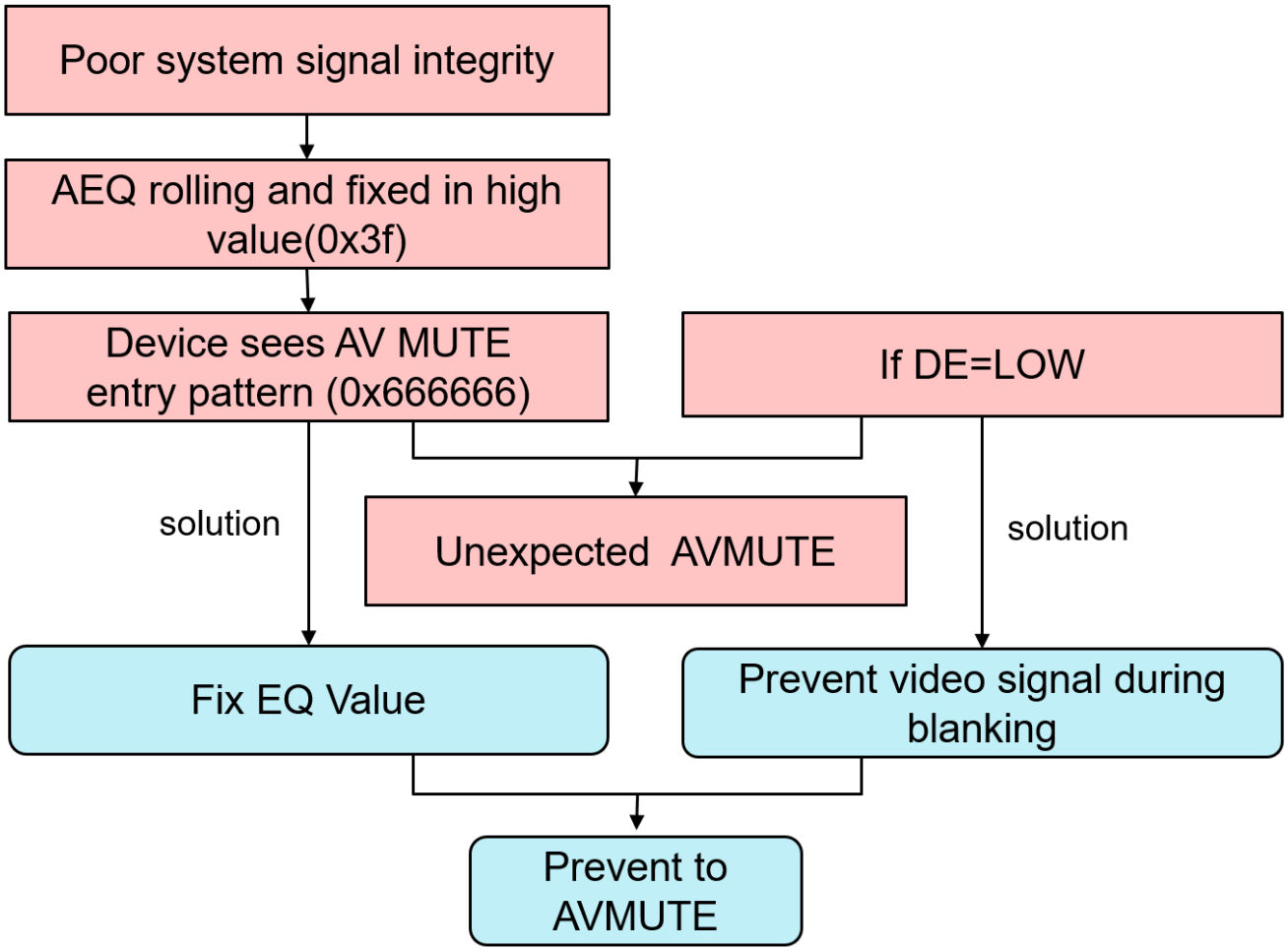

Figure 4-1. How to Prevent Entering AV MUTE Mode

Note

If an unexpected AV MUTE state is seen, TI recommends verifying the data path control setting of the paired serializer. This prevent setting is not accessible from deserializers

4.1 Prevent Video Signals During the Blanking Interval

When paired with a UB version FPD-Link compatible serializer, setting the DE_GATE Register (check table4-x) prevents video signals from being sent during the blanking interval. This verifies that AV MUTE mode is not entered during normal operation. By default, the Data Enable (DE) signal is assumed to be active high. If DE is active low, then setting DE_POLARITY register is also required.

With the DE permanently LOW, deserializers do not check for the AV Mute conditions, so the AV Mute is not an issue when operating with HSYNC/VSYNC only mode displays.

DE_GATE Register:

Gate RGB data with DE signal. When this bit is set, the DS90UB947-Q1 will use the DE signal to gate the RGB video data.

1: Gate RGB data with DE.

0: Pass RGB data independent of DE.

Table 4-1. Set DE_GATE Register in Pairing Serializers

Set Device	Set DE_GATE Register
DS90UB925Q-Q1	0x04 [4] =0
DS90UB927Q-Q1	0x04 [4] =0
DS90UB929Q-Q1	0x04 [4] =0
DS90UB941AS-Q1	0x04 [4] =0
DS90UB947Q-Q1	0x04 [4] =0
DS90UB949A-Q1	0x04 [4] =0
DS90UB981-Q1/ DS90UB681-Q1	0x5A [6] =1
DS90UB983-Q1 / DS90UB943A-Q1	0x5A [6] =1
DS90HB983-Q1	0x5A [6] =1

4.2 Fix EQ Value

As Figure 4-1 shown, be advised if the video source continues sending random data during blanking interval, the UB928\948\940 can inadvertently enter the AV MUTE state upon receiving random data matching the AV MUTE command pattern.

To force the AEQ and fix the EQ Value, use the following registers setting applied to the deserializer during initialization:

```
Des_ID=0x58
## ********************************************
## Fix EQ Value
## ********************************************
board.WriteI2C(Des_ID,0x34,0x03) #Select Port0&1, change it if you use port0
board.WriteI2C(Des_ID,0x44,0x21) #Force AEQ to level 1
board.WriteI2C(Des_ID,0x01,0x05) #softreset
board.ReadI2C(Des_ID,0x3B) #readback for double check. 0x3B=0x01, EQ=1
## select the appropriate one gear in the code below
# board.WriteI2C(Des_ID,0x44,0x41) #Force AEQ to level 2
# board.ReadI2C(Des_ID,0x3B) #readback reg 0x3B=0x02, EQ=2
# board.WriteI2C(Des_ID,0x44,0x61) #Force AEQ to level 3
# board.ReadI2C(Des_ID,0x3B) #readback reg 0x3B=0x03, EQ=3
# board.WriteI2C(Des_ID,0x44,0x81) #Force AEQ to level 4
# board.ReadI2C(Des_ID,0x3B) #readback reg 0x3B=0x04, EQ=4
# board.WriteI2C(Des_ID,0x44,0xA1) #Force AEQ to level 5
# board.ReadI2C(Des_ID,0x3B) #readback reg 0x3B=0x05, EQ=5
# board.WriteI2C(Des_ID,0x44,0xC1) #Force AEQ to level 6
# board.ReadI2C(Des_ID,0x3B) #readback reg 0x3B=0x01, EQ=6
# board.WriteI2C(Des_ID,0x44,0xE1) #Force AEQ to level 7
# board.ReadI2C(Des_ID,0x3B) #readback reg 0x3B=0x01, EQ=7
# board.WriteI2C(Des_ID,0x44,0xE3) #Force AEQ to level 8
# board.ReadI2C(Des_ID,0x3B) #readback reg 0x3B=0x01, EQ=8
# board.WriteI2C(Des_ID,0x44,0xE5) #Force AEQ to level 9
# board.ReadI2C(Des_ID,0x3B) #readback reg 0x3B=0x01, EQ=9
# board.WriteI2C(Des_ID,0x44,0xE7) #Force AEQ to level 10
# board.ReadI2C(Des_ID,0x3B) #readback reg 0x3B=0x01, EQ=10
# board.WriteI2C(Des_ID,0x44,0xE9) #Force AEQ to level 11
# board.ReadI2C(Des_ID,0x3B) #readback reg 0x3B=0x01, EQ=11
# board.WriteI2C(Des_ID,0x44,0xEB) #Force AEQ to level 12
# board.ReadI2C(Des_ID,0x3B) #readback reg 0x3B=0x01, EQ=12
# board.WriteI2C(Des_ID,0x44,0xED) #Force AEQ to level 13
# board.ReadI2C(Des_ID,0x3B) #readback reg 0x3B=0x01, EQ=13
# board.WriteI2C(Des_ID,0x44,0xEF) #Force AEQ to level 14\15
# board.ReadI2C(Des_ID,0x3B) #readback reg 0x3B=0x3F, EQ=14\15
```

4.3 How to Find EQ Value

Method 1: Test the S parameter of system link

As can be seen from Example of S Parameter Test Results (10m Coax), the cable loss of 10m at 1GHz is approximately 13dB, corresponding to the cable loss of 1m and connector loss of approximately 2dB. The host-to-display loss must not exceed a maximum of 5dB, considering the different cables and the effects of temperature changes, aging, and so on.

The UB948 can see EQ=0x02 compensation at 5dB at 1GHz according to Table 4-1 which can fully compensate for loss in a system. So in this situation, set EQ=0x2.

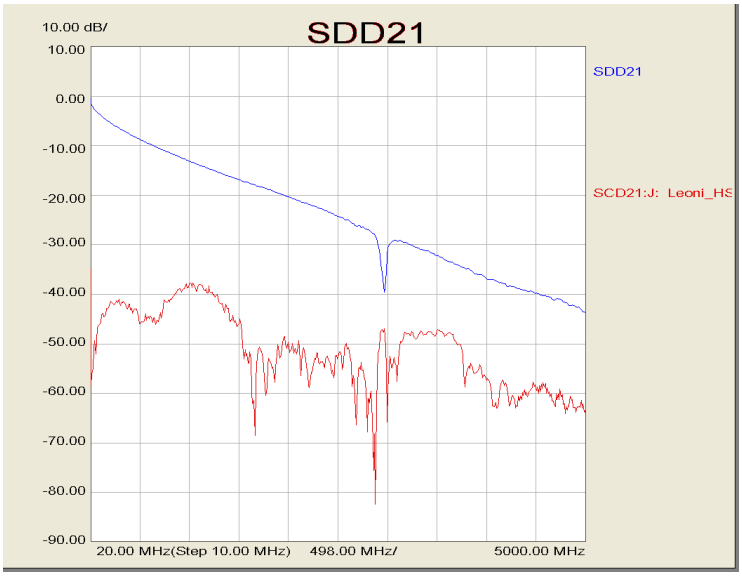

Figure 4-2. Example of S Parameter Test Results (10m Coax)

Table 4-2. Recommended Fixed AEQ Setting Range for a Cable Loss Range

Acceptable Equalizer Range	Loss Range(dB)
0-1	0-3
1-2	3-4
2-3	4-6
3-4	6-9.5
4-5	9.5-10.5
5-9	10.5-13.5
10-15	13.5-16
15	>16

Method 2: Test MAP (Margin Analysis Program)

The MAP included in Analog LaunchPad (ALP) development kit creates diagrams showing which EQ level and strobe position combinations show no errors or loss of lock. These diagrams can be used to diagnose the condition of the eye, with a larger number of passing (green) squares to show a larger eye opening. See FPD-Link Margin Analysis Program (MAP) user's guide for the specific test procedure.

Based on the analysis of the MAP (Figure 4-3), it is also shown that with EQ = 0x01, the perimeter is green, indicating a large headroom. So, TI recommends setting EQ = 0x01 in this situation.

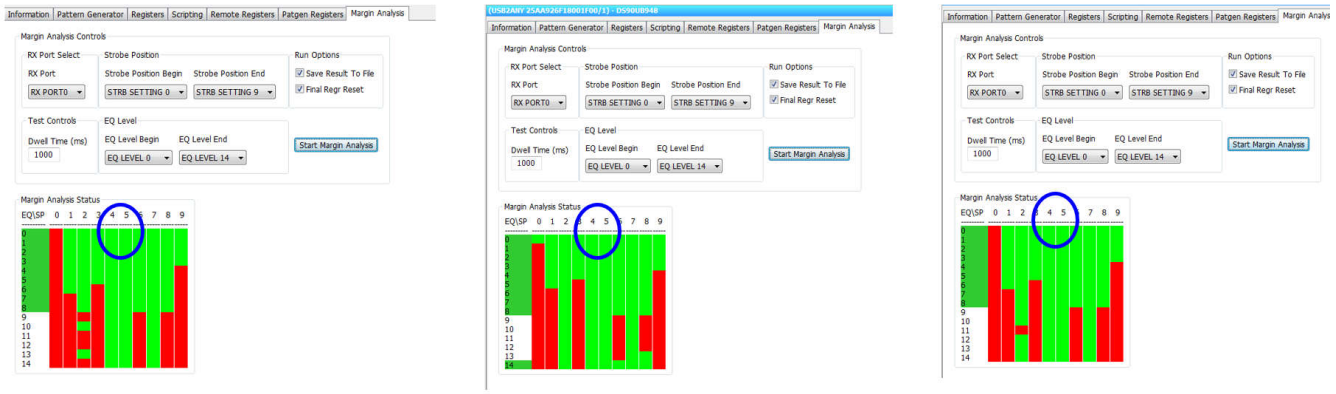

Figure 4-3. Example of MAP Test Results in Different Temperature

5 Summary

In unstable link environments, it is possible for the FPDLINK deserializers to experience repeated lock drops and potentially entering a state where the EQ value is operating outside of the normal range of a given system. In this extreme environment, the EQ may boost noise in such a way that the deserializer interprets this noise as the signal to enter AV MUTE mode even on a non-HDCP enabled device. The designs proposed in this document are intended to solve the inadvertent entry into AV MUTE mode by preventing this signal from being recognized but also by helping stabilize the EQ range in this type of environment.

6 References

Digital Content Protection, *HDCP Specifications*, webpage.

Texas Instruments, *DS90UH94X Adaptive Equalizer and Startup*, white paper.

Texas Instruments, *DS90UH948-Q1 Automotive 2K FPD-Link III to OpenLDI Deserializer With HDC*, datasheet.

Texas Instruments, *DS90UB948-Q1 Automotive 2K FPD-Link III to OpenLDI Deserializer*, datasheet.

Texas Instruments, *FPD-Link Margin Analysis Program (MAP) user's guide*, user's guide.

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