Application Note

Remote Wake-up, Sleep, and Surveillance Modes for FPD-Link III and FPD-Link

Johannes Kargl, Harry Shin

ABSTRACT

The requirement to maximize power saving has increased in various automotive electronic systems in the past years. Particularly, surveillance systems which utilize camera and radar sensors are required to minimize power consumption to maximize operational time when the vehicle is parked. This requires most system components to be in a low power sleep mode configuration while the vehicle is parked. This application note will explain how to implement low power mode operation of cameras with FPD-Link III and IV to minimize power consumption in surveillance mode operation including how to enable remote wake-up capabilities.

Table of Contents

Trademarks

1 Introduction of FPD-Link

FPD-Link is a multi-protocol physical layer technology that aggregates data from various industry standard video protocols and transfers it over coax or twisted pair cables. Its most common use is for digital video and audio transfer in automotive applications, such as video screens or driver assistance cameras as shown in Figure 1-1.

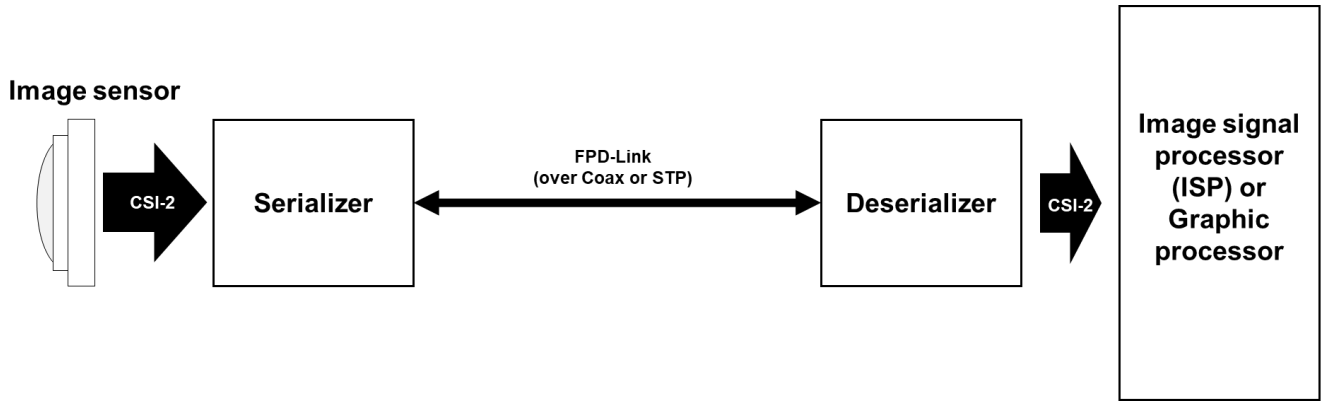

Figure 1-1. Typical application of FPD-Link

The FPD-Link forward channel is used to send video, audio or other control data such as I2C and GPIOs to endpoint devices with low latency. Low-speed data is transmitted from deserializer to serializer through the back channel simultaneously with frequency division duplexing.

2 Power-over-Coax Concept

A Power-over-Coax (PoC) network separates the high-speed data signal from the DC power signal on a coaxial cable. Figure 2-1 shows a high-level overview of how FPD-Link and DC power share a single coax cable. The inner conductor of the coax cable is used as the supply line for the DC power and the shield of the coax cable is connected to ground and is used as return path for the DC power. The PoC Network acts as a low pass filter with high impedance at the FPD-Link operational frequency band to minimize interference from the DC power with the high-speed signals.

For more information on PoC with FPD-Link see FPD-Link ADAS Power-Over-Coax Design Guidelines.

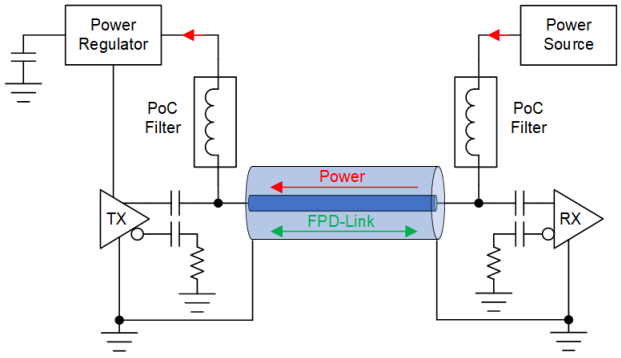

Figure 2-1. Power-over-Coax Application

3 System consideration for sleep mode and remote wake-up with FPD-Link III and FPD-Link IV

FPD-Link III and IV devices do not have a built-in sleep mode feature with bidirectional wake-up capabilities. Therefore, a sleep mode function with bidirectional wake-up needs to be implemented on system level. The following Figure 3-1 shows a proposal on how to cost-effectively add a robust sleep and bidirectional wake functionality for remote sensor systems which use FPD-Link III or IV devices. The additional system components and considerations compared to a traditional automotive camera system implementation are depicted in red.

The system level proposal is based on two functions. Entering and exiting sleep mode is based on adjusting the PoC voltage. A higher PoC voltage is used for normal mode operation and a lower PoC voltage is used for sleep mode operation. The PoC voltage adjustment is controlled on the deserializer side (e.g. ADAS or central ECU). During sleep mode operation, the deserializer can be fully powered off to minimize system power consumption. A voltage detection circuit on the serializer side (e.g. remote camera) enables and disables the serializer through the power down pin (PDB) to minimize power consumption and achieves the wake-up functionality from the ECU to the remote sensor.

The PoC voltage levels for normal mode and sleep mode should be carefully selected to account for the voltage drop due to the DC resistance of the power path and accuracy of voltage sensing and PoC voltage regulation. Depending on the system requirements, the PoC voltage in sleep mode should be selected high enough to avoid undervoltage lockout (UVLO) of the PMIC on serializer side which supplies other devices, e.g. image sensor which runs in a low-power movement/human detection mode. As an example, the PoC voltage in normal mode can be selected with 12V and for sleep mode operation with 7 - 8V.

For advanced system features, e.g. cameras with movement or human detection, a wake-up from serializer to deserializer side needs to be implemented. This can be realized by monitoring the PoC current of the individual camera channels during sleep mode. If one of the remotely connected sensors is switching to active state, an increase in power consumption is detected on the ECU side and the wake-up of the system can be initiated. Other remote sensors which remained in sleep mode are enabled by increasing the PoC voltage to normal mode level.

The following sections present possible implementations of the detection circuits for bidirectional wake-up functionality. The first three options show how to implement the voltage detection circuit on the camera side for wake-up initiated by the ECU side. The fourth option shows how the current sensing on ECU side is implemented for reverse wake-up scenarios initiated by a remote sensor (camera).

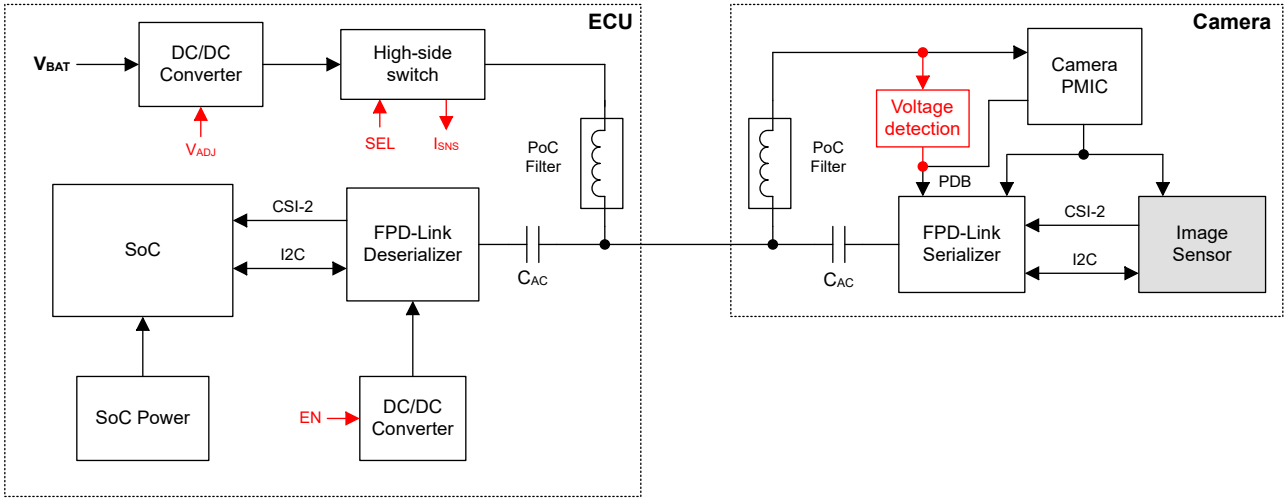

Figure 3-1. System level block diagram

3.1 Voltage detection with Comparator circuit

The first option to implement PoC voltage detection on the serializer side is using a comparator circuit with a resistor divider as shown in Figure 3-2. This option represents the easiest and most cost-effective approach but requires more consideration at the system level due to component tolerances. An external resistor divider

is used to set the threshold voltage to switch between sleep and normal mode. The output rail of the voltage regulator (e.g. 1.8V) is used as reference voltage for the comparator. If the PoC voltage is below the threshold the output of the comparator is low and powers down the serializer for system sleep mode. For this option, resistors with a tolerance of 1% are recommended for the external resistor divider.

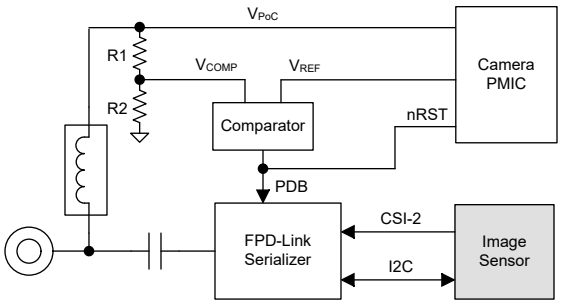

Figure 3-2. Voltage detection with comparator

The following example shows how to estimate the voltage levels at the comparator input for sleep and normal mode for a given configuration as shown in Table 3-1.

Depending on the tolerance of resistors, PoC voltage, reference voltage and IR drop of the PoC filter networks and coax cable the system designer needs to ensure correct detection of sleep and normal mode based on worst case conditions.

Table 3-1. Comparator Example Design Parameters

Parameter		Condition	Min	Typ	Max	Unit
$V_{PoC(norm)}$	PoC voltage normal mode	Tolerance: +/- 5%	8.55	9	9.45	V
$V_{PoC(sleep)}$	PoC voltage sleep mode	Tolerance: +/- 5%	4.75	5	5.25	V
R1	Resistor high side	Tolerance: +/- 1%	68.31	69	69.69	kΩ
R2	Resistor low side	Tolerance: +/- 1%	26.73	27	27.27	kΩ
V_{REF}	Reference voltage	Tolerance: +/- 5%	1.71	1.8	1.89	V
$V_{IR(norm)}$	IR drop over coax path	$I_{PoC(norm)}$ x $R_{DC(max)}$		500		mV
$V_{IR(sleep)}$	IR drop over coax path	$I_{PoC(sleep)}$ x $R_{DC(max)}$		40		mV

The comparator input voltage can be calculated with the following equation.

$$V_{comp} = \frac{(V_{PoC} - V_{IR}) \times R2}{(R1 + R2)} \quad (1)$$

For the above example, the comparator input voltage at normal mode in worst case condition equates as:

$$V_{comp(norm,min)} = \frac{\left(V_{PoC(norm,min)} - V_{IR(norm)}\right) \times R2(min)}{R1(max) + R2(min)} = \frac{(8.55V - 0.5V) \times 26.73k\Omega}{69.69k\Omega + 26.73k\Omega} = 2.231V \quad (2)$$

For sleep mode the worst case condition can be calculated with Equation 3.

$$V_{comp(sleep,max)} = \frac{\left(V_{PoC(sleep,max)} - V_{IR(sleep)}\right) \times R2(max)}{R1(min) + R2(max)} = \frac{(5.25V - 0.04V) \times 27.27K}{(68.31K + 27.27K)} = 1.486V \quad (3)$$

The calculated values show sufficient margin of at least 200mV to the reference voltage range.

Other system parameters which should be considered are the offset voltage and offset voltage drift of the comparator. However, these values are typically in the low mV range and therefore are negligible.

For robustness against voltage transients, a small capacitor can be added at the input of the comparator.

TI offers a variety of comparators like LM393LV-Q1 with low quiescent current and input offset voltage which are suitable for the presented solution.

3.2 Voltage detection with Supervisor

A different option to implement the voltage detection circuit is with a voltage supervisor. Compared to the previously presented option this approach requires no external resistor divider and provides therefore better accuracy. As shown in Figure 3-3, the voltage supervisor directly connects to the PoC voltage rail.

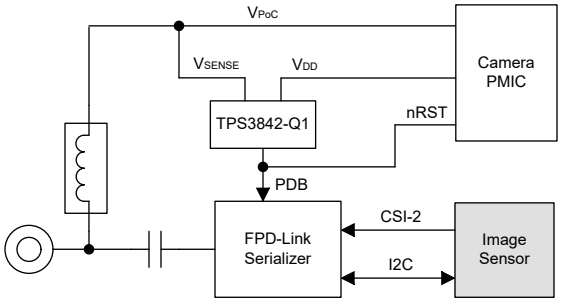

Figure 3-3. Voltage detection with Supervisor

The voltage supervisor uses an internal voltage reference and selectable internal threshold voltage.

Below example shows the expected voltage range at the input of the supervisor for normal mode and sleep mode for a given configuration according to Table 3-2.

Table 3-2. Supervisor Example Design Parameters

Parameter		Condition	Min	Typ	Max	Unit
$V_{PoC(norm)}$	PoC voltage normal mode	Tolerance: +/- 5%	8.55	9	9.45	V
$V_{PoC(sleep)}$	PoC voltage sleep mode	Tolerance: +/- 5%	4.75	5	5.25	V
V_{THR}	Threshold voltage	Tolerance: +/- 1.5%	6.40	6.5	6.60	V
$V_{IR(norm)}$	IR drop over coax path	$I_{PoC(norm)}$ x $R_{DC(max)}$		500		mV
$V_{IR(sleep)}$	IR drop over coax path	$I_{PoC(sleep)}$ x $R_{DC(max)}$		40		mV

The input voltage at the supervisor can be calculated with the following Equation 4.

$$V_{SVS} = V_{PoC} - V_{IR} \quad (4)$$

For the above example, the supervisor input voltage at normal mode in worst case condition equates as:

$$V_{SVS(norm,\,min)} = V_{PoC(norm,\,min)} - V_{IR(norm)} = 8.55V - 0.5V = 8.05V \quad (5)$$

For sleep mode the worst case condition can be calculated with Equation 6.

$$V_{SVS(sleep,\,max)} = V_{PoC(sleep,\,max)} - V_{IR(sleep)} = 5.25V - 0.04V = 5.21V \quad (6)$$

Considering the threshold voltage range of 6.4 – 6.6V, the supervisor option provides significantly more margin compared to the comparator option with external resistor divider.

A suitable supervisor device for this option is TPS3842-Q1, which offers high accuracy, built-in hysteresis and a programmable sense delay which makes it robust against voltage transients and allows for more PoC voltage variation.

3.3 Voltage detection with Programmable Logic Device

The two previously presented options are not robust against conditions when the PoC voltage is lower than the threshold voltage for an extended time period during normal mode. This leads to a power down of the serializer through the PDB pin as shown in the diagram in Figure 3-4.

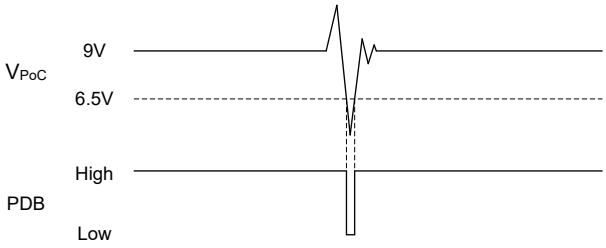

Figure 3-4. PDB output during transient event

A third option to implement the voltage detection circuit on the serializer side is by using a programmable logic device which allows designers to choose a custom configuration to avoid unwanted activation of the sleep mode condition during normal mode. Table 3-3 shows the function table for an example configuration of the voltage detection function with a programmable logic device.

Table 3-3. Function Table of Programmable Logic Device

Input		Output
IN_1	**IN_2**	**PDB**
Low	$V_{IN\_2} < V_{THR}$	Low
High	$V_{IN\_2} < V_{THR}$	High
Low	$V_{IN\_2} > V_{THR}$	High
High	$V_{IN\_2} > V_{THR}$	High

In this example, the IN_1 pin acts as an enable input for sleep mode control. If the input on the IN_1 pin is logic low and the voltage on the IN_2 pin is below the configured threshold, the output pin which is connected to the PDB pin of the serializer is set to low and powers down the serializer. This avoids unintended sleep mode activation when the PoC voltage falls below the configured voltage threshold in normal mode operation. Figure 3-5 shows the implementation with the programmable logic device for the above example configuration. The IN_1 input is connected to a GPIO of the PMIC, which is controlled over I2C from a remote host ECU. Depending on the system architecture this can be also a GPIO pin from the image sensor.

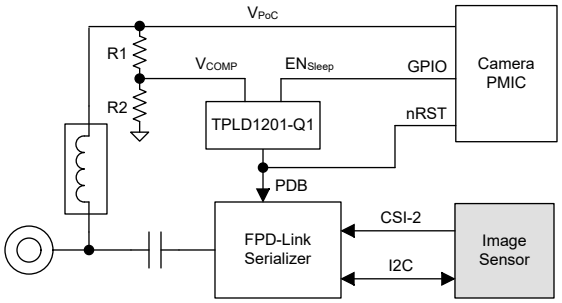

Figure 3-5. Voltage detection with Programmable Logic Device

TI offers a variety of programmable logic devices suitable for the voltage detection function like TPLD1201-Q1 with integrated comparators, LUTs, counters and oscillators.

3.4 Power-over-Coax Current Sensing for Reverse Wake-up

For advanced systems where wake-up from sensor to ECU side is required, additional system level considerations are required. Figure 3-6 shows how to cost-effectively implement the wake-up function from sensor to ECU side.

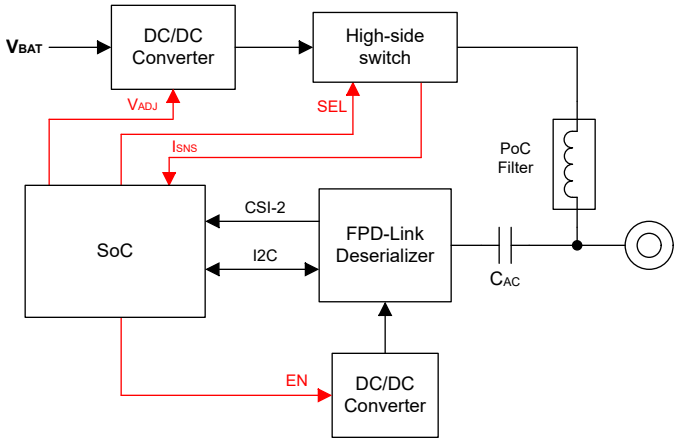

Figure 3-6. Current sensing for reverse wake-up

During sleep mode, the MCU/SoC is monitoring the supply current on the individual camera channels through the high-side switch or camera protector switch. The current monitoring can be accomplished by either using an ADC channel in the SoC if the high-side switch provides an analog current sense output or through I2C if the high-side switch already integrates an ADC for the current monitoring. When sleep mode is active and the SoC detects one of the channel supply currents is increasing above a defined threshold, the SoC interprets this as a wake-up request from a remote sensor. The rest of the system then transitions to normal mode and increases the PoC voltage to wake up the remaining remote sensors (Serializers), which are still in sleep mode. Together with the lower PoC voltage used in sleep mode, the current sense accuracy for wake-up detection can be also lower. To increase the current draw for wake-up purposes, there are different options on the sensor side: a dummy load which is only temporarily activated or by enabling other devices which increase the power consumption, e.g. serializer. The presented approach for reverse wake-up utilizes devices that are already present in most camera systems and therefore provides a cost-effective implementation.

4 Summary

The increasing demand for camera surveillance functionality in the automotive segment requires solutions to reduce the system power consumption when the vehicle is parked and maximize the operation time of surveillance mode. This application note presents concepts and different options for how to implement low power mode on a system level for FPD-Link camera systems. This includes system level considerations like voltage variations, transients and component tolerances as well as suitable devices to implement lowest power operation in surveillance mode for automotive camera systems.

5 References

- Texas Instruments TL331LV, TL391LV, LM393LV and LM339LV Low Voltage Rail to Rail Input Comparators datasheet (Rev. D)
- Texas Instruments TPS3842-Q1 Automotive 42V Small Size, 850nA Undervoltage or Overvoltage Supervisor With Programmable Delay and De-Glitch datasheet (Rev. B)
- Texas Instruments TPLD1201-Q1 Automotive Programmable Logic Device with 8-GPIO datasheet (Rev. B)
- FPD-Link ADAS Power-Over-Coax Design Guidelines
- Texas instruments DS90UB9702 -Q1 Automotive FPD-Link IV Deserializer Hub With D-PHY CSI-2 Output Ports for 8MP+ Cameras & Other Sensors datasheet
- Texas instruments DS90UB960-Q1 Quad 4.16-Gbps FPD-Link III Deserializer Hub With Dual MIPI CSI-2 Ports datasheet (Rev. D)
- Texas instruments DS90UB971 -Q1 FPD-Link IV 7.55-Gbps Serializer With CSI-2 Interface for 8MP+ Cameras, RADAR & Other Sensors datasheet (Rev. A)
- Texas instruments DS90UB953-Q1 FPD-Link III 4.16Gbps Serializer With CSI-2 Interface for 2.3MP/60fps Cameras, RADAR, and Other Sensors datasheet (Rev. E)

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Last updated 10/2025