Application Note

Design Consideration of 3-Level Flying Capacitor Converters for Three-Phase AC/DC Applications

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ABSTRACT

The adoption of three-level flying capacitor conversion structures permits the use of 650V rated transistors in three-phase DC/AC applications where the DC voltages are higher than 650V. In this paper, an introduction to the three-level flying capacitor topology is given. Design tips and experimental results are provided to prove the benefits of this topology when using TI GaN transistors.

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Trademarks

1 Introduction

Nowadays, power conversion systems having high-efficiency and power density in renewable energy are becoming a must. Adoption of GaN technology becomes a state-of-the-art design when targeting single-phase applications as 400V DC link rated [1, 2]. When targeting 800V systems, GaN in two-level topologies require breaking down voltage higher than 1000V, thus making it hard to find GaN transistors being able to withstand this high voltage. In traditional half bridges cell, each switching device needs to withstand the full DC bus voltage. To reduce the voltage stress presents in three-phase applications, alternative multilevel topologies need to be taken into consideration. By adding additional power components, the overall voltage stress on the device can be significantly reduced when adopting multilevel converters. As can be seen from 3, multiple topologies can be found in the literature but flying capacitor results is the most cost-effective design. The three-level flying capacitor topology is discussed in this document. A special focus is given on the implementation with Texas Instruments GaN FETs.

2 Operating Principles in a Flying Capacitor Switching Cell

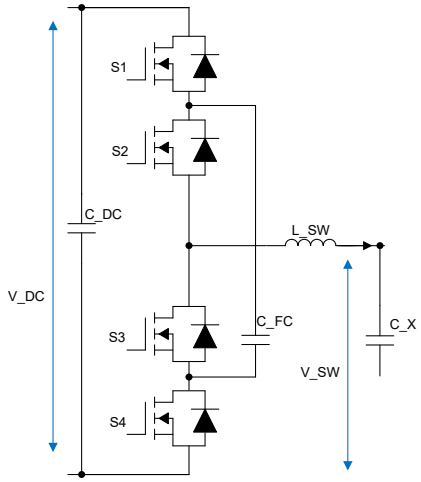

Figure 2-1. Three-Level Flying Capacitor Switching Cell

In a three-level switching cell, the following components can be found as shown in Figure 2-1:

- S1, S2, S3 and S4 are four power switches.
- C_{FC} is the flying capacitor.
- L_{SW} is the switching node inductance.
- C_{DC} is the DC link voltage capacitor.

Note that this topology is considered a boost converter topology, where the V_{SW} voltage is always lower than the DC link voltage (V_{DC}).

In this topology, the three voltage levels on the switching node output are achieved by turning the transistors on with the right combination:

1. Output equal to Vdc: S1 and S2 are ON.
2. Output equal to 0 V: S3 and S4 are ON.
3. Output equal to V_DC-V_FC: S1 and S3 ON.
4. Output equal to V_FC: S2 and S4 ON.

As can be seen from the third and fourth switching states, it is important to control the voltages of the two capacitors constant (Vfc and Vdc). This condition makes sure that the switching node voltage is half the DC link voltage, if the flying capacitor voltage is control to half the DC link voltage.

2.1 Switching Pattern of a 3-Level Flying Capacitor Switching Cell

As can be seen from Figure 2-1, there are four switches implemented for each phase (S1, S2, S3 and S4). In this topology, each of the FET is rated for half the DC link voltage. Though there are various switching schemes to control this power stage, a simpler scheme has been selected to reduce complexity. In this design, all the transistors are switching at the nominal frequency of f_{SW}. Dead-time, carrier and duty cycle needs to be defined for each FET:

- Switch pairs S1+S4, and S2+S3 are switching complementary to each other's. Two pairs of dead times are required per switching cell. If S1 and S4 are not complementary to each there is risk of shorting C_{DC}, thus causing a severe overcurrent plus overvoltage across S2 and S3. If S2 and S3 are not switching complementary to each other there is risk of shorting C_{FC}, thus causing a severe overcurrent plus overvoltage across S1 and S4.
- S1+ S4 and S2+ S3 signals are 180 degrees phase-shifted to each other. Because of this phase shifting, the switching node inductor sees double the switching frequency, thus making the required inductance value smaller.
- At first approximation the duty cycle applied to the two PWM pairs is going to be the same. The duty-cycle is as a ratio between V_{SW} and V_{DC}.

Three different operating points of the switching cell are investigated. The duty cycle is defined as the on time of S1 and S2:

- When the duty cycle is higher than 50 %, S1 and S2 are more time in the on-state than S3 and S4. When there is a 1000V DC link, the output switching voltage is switching between the levels 500V and 1000V.
- When the duty cycle is lower than 50 %, S3 and S4 are more time in the on-state than S1 and S2. When there is 1000V DC link, the output switching voltage is switching between the levels 0V and 500V.
- When the requested duty is equal to 50 %, the four switches are going to be ON 50 % of the switching time. At first approximation, output switching node voltage is going to be fixed at 500V.

The switching pattern graphs of 3-level flying capacitor converter can be seen from section 2.2.1 of the TIDA-010957 design guide.

3 Design Considerations of a Flying Capacitor Switching Cell

3.1 Conduction and Switching Losses

3.1.1 AC Conduction Losses

Conduction loss is determined by the $R_{DS,ON}$ of the FETs. At any moment, there are always two devices conducting the switching node current at the same time. The total conduction loss of the single FET can be calculated as Equation 1.

$$P_{COND} = \frac{R_{DS,ON} \times I_{SW}^2}{\sqrt{2}} \quad (1)$$

Where I_{SW} represents the RMS current of the inductor.

3.1.2 AC Switching Losses

Switching loss is in function of the switching frequency and switching energy associated for each transistor. The switching energy is related to the device current and voltage at the switching transient. Using the switching energy curve in the datasheet, as for example the one in LMG3522R030 datasheet, the total switching loss can be estimated.

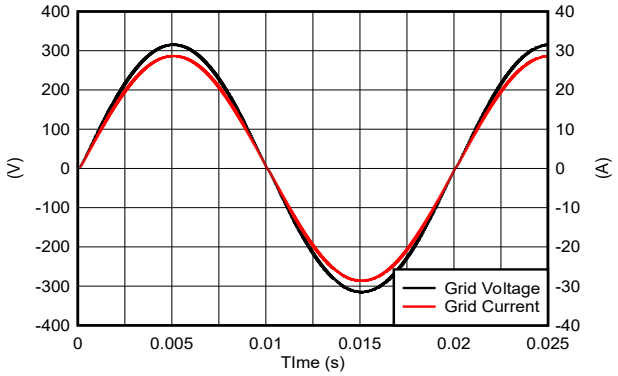

Figure 3-1. Grid Voltage and Grid Current

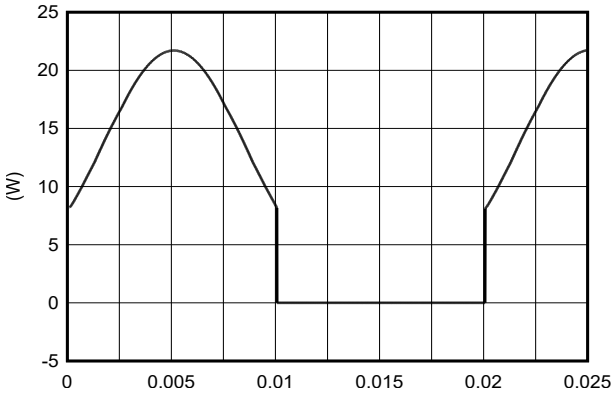

Figure 3-2. Switching Losses: S1 and S2

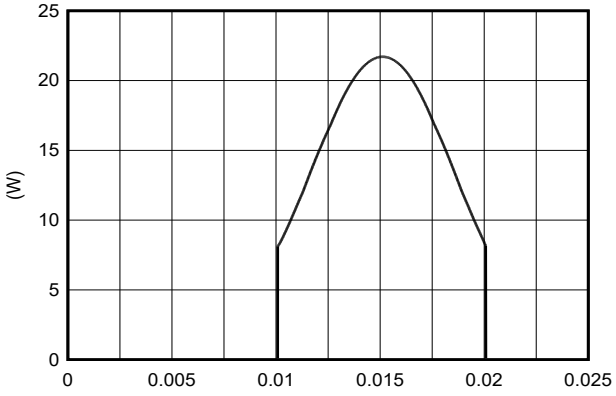

Figure 3-3. Switching Losses: S3 and S4

In Figure 3-1, current and voltages on the switching node of the switching cell shown previously are shown. Note that both the current and the voltage are in phase, and as a result, involving an inverter operation of the switching cell. The switching losses of the four transistors are shown in Figure 3-2 and Figure 3-3. Note that switching losses are only present for half-electrical period. This means that half-period the switches are hard-switching and the other half-period the FETs are soft-switching. In average over full AC period AC losses are equal for all FETs. Additional investigations have been conducted and the switching losses in all the operational modes mentioned below are always the same, where with operating mode this is mean:

- Power Factor Corrector (PFC) power from the AC to the DC
- Inverter power from the DC to the grid.
- Capacitive and inductive compensators, when only reactive power is pushed or drained to the grid.

3.2 Passive Components Design

3.2.1 Boost Inductor Design

The boost inductor or the switching node inductor is used to filter out the voltage pulses generated by the switching cell. When selecting the right inductor three important parameters need to be considered:

- Peak to peak ripple current which drives losses of the inductor
- Application peak current which drives the saturation current of the core
- RMS current of the applications itself.

In a three-level flying capacitor converter the peak-to-peak ripple current flowing through the boost inductor (L_{SW}) is calculated as follows:

$$D_{eff} = 2 \times D - \text{floor}(2 \times D) \quad (2)$$

$$\Delta I_L = \frac{V_{DC} \times (D_{eff}(1 - D_{eff}))}{4 \times L_{sw} \times f_{sw}} \quad (3)$$

Where:

- V_{DC} is the DC link voltage
- D_{eff} is the effective duty ratio applied to the inductor
- L_{SW} is the boost inductance
- f_{SW} is the switching frequency

The formula in function of the duty cycle is as shown in Figure 3-4.

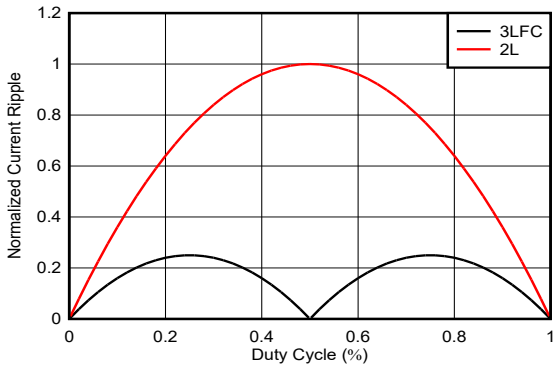

Figure 3-4. Normalized Ripple Current vs. Duty-cycle When Having 3-Level and 2-Level Converters

Note that when compared to a 2-level converter, the 3-level converter achieve a peak to peak current reduction of 75%. The peak to peak current is reduced 75% because the frequency seen by the inductor is double and the applied voltage is half. Figure 3-4 shows that the ripple is maximum when the duty cycles are equal to 25% and 75%. In sinusoidal applications, TI recommends considering 25% and the 75% duty cycle as the worst-case.

3.2.2 DC Link High Frequency Ripple

The DC link voltage ripple and RMS current can be calculated as in:

$$\Delta V_{DC} = \frac{D(1-D) \times I_{boost}}{C_{out} \times f_{sw}} \quad (4)$$

$$I_{out,RMS} = \sqrt{D \times {I_L}^2 \times (1-D) + \frac{{\Delta I_L}^2}{12}} \quad (5)$$

Where:

- ΔV_{DC} is the DC link voltage ripple visible at the C_DC terminals.
- D is the ratio between the average switching node voltage and the DC link voltage. This value corresponds to the duty-cycle.
- I_L is the switching node current.
- f_{SW} is the switching frequency of the four FETs.

These two formula are plotted with respect to the duty-cycle as shown in Figure 3-5 and Figure 3-6.

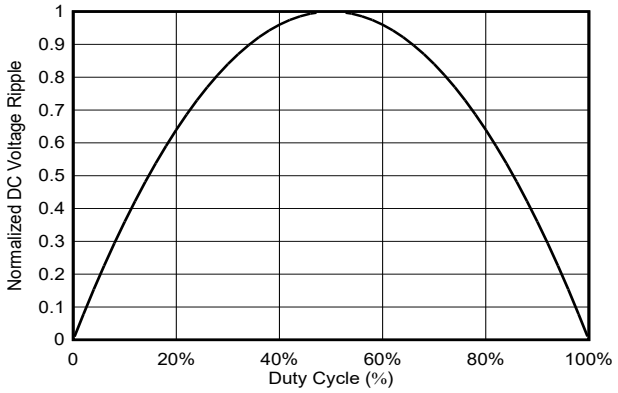

Figure 3-5. DC Voltage Ripple as a Function of the Duty Cycle

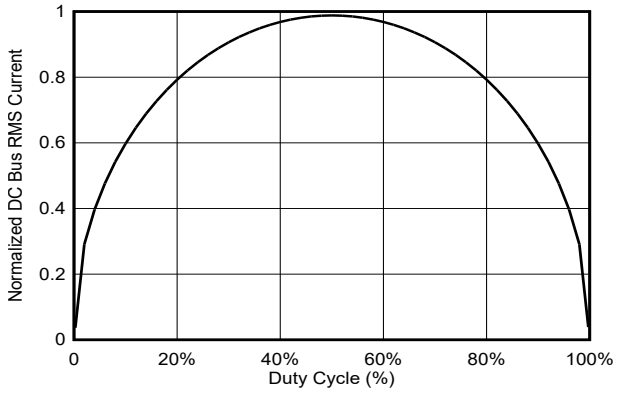

Figure 3-6. DC Bus RMS Current as a Function of the Duty Cycle

Figure 3-6 shows that the worst-case scenario is always happening when the duty cycle is equal to 50%. When selecting the capacitor, the average ripple over the AC cycle must be considered. The switching frequency seen by the capacitor is equal to fsw and this time is not double as on the inductor case.

3.2.3 Flying Capacitor Design

In this topology, the flying capacitor is a critical component. This component must be selected with a voltage rating greater than half the DC link voltage. Since when the complete inductor current flows into the flying capacitor a large voltage ripple is present. The peak-to-peak voltage ripple across the flying capacitor can be calculated as in:

$$\Delta V_{FC} = \frac{(0.5 - ABS(D - 0.5)) \times I_L}{C_{FC} \times f_{sw}} \quad (6)$$

Where C_{FC} is the capacitance value of the flying capacitor.

Note that from this formula that when increasing the switching frequency, the ripple voltage can be decreased quite significantly, thus making GaN transistors more appealing in this topology.

Furthermore, the RMS current can be calculated as follows.

$$I_{FC,\,RMS} = \sqrt{2(0.5 - ABS(D - 0.5)) \times \left({I_L}^2 + \frac{\Delta {I_L}^2}{12} \right)} \quad (7)$$

The flying capacitor ripple voltage and the RMS current in function of the duty-cycle are plotted in Figure 3-7 and Figure 3-8.

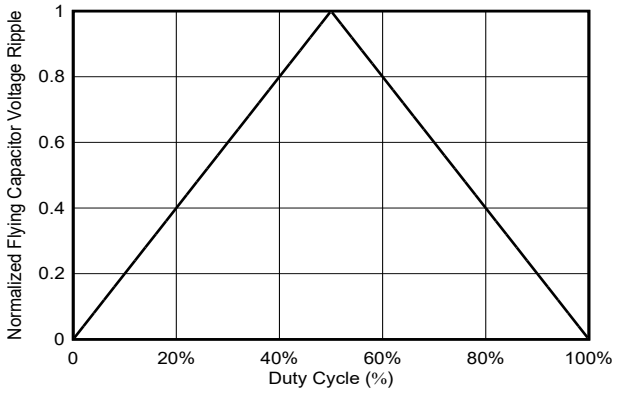

Figure 3-7. Flying Capacitor Peak-to-Peak Voltage in Function of the Duty Cycle

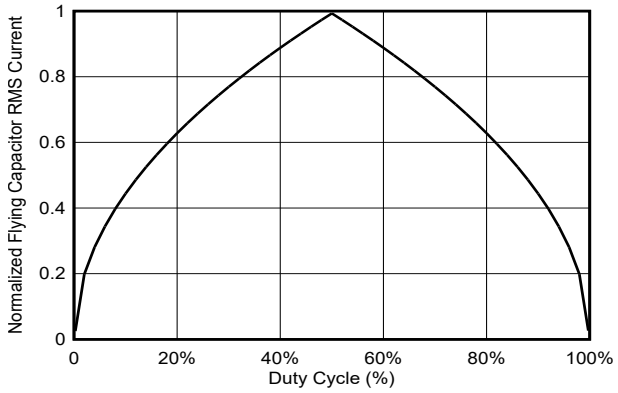

Figure 3-8. RMS Current of the Flying Capacitor in Function of the Duty Cycle

Note that from Figure 3-7 and Figure 3-8 that the worst-case scenario is happening when the duty cycle is equal to 50%. The fundamental ripple frequency flowing in the flying capacitor is equal to the switching frequency. To achieve a good cost structure of the designed converter, TI recommends using film capacitor because it provides high capacitance while also being able to handle large ripple currents in a low-cost design.

3.3 Layout Considerations

As demonstrated in Section 3.2, it can be observed from the formula that by switching at a higher switching frequency the flying capacitor and the boost inductor values can be decreased significantly. To achieve a higher switching frequency, GaN transistors can be adopted. These transistors switch faster than standard Si FETs, thus decreasing the switching losses. Switching faster leads to high di/dt which together with the loop parasitic inductance can lead to important device overvoltage. The overvoltage causes EMI issues or even the device destruction. In this topology, two commutation loops can be identified as in Figure 3-9.

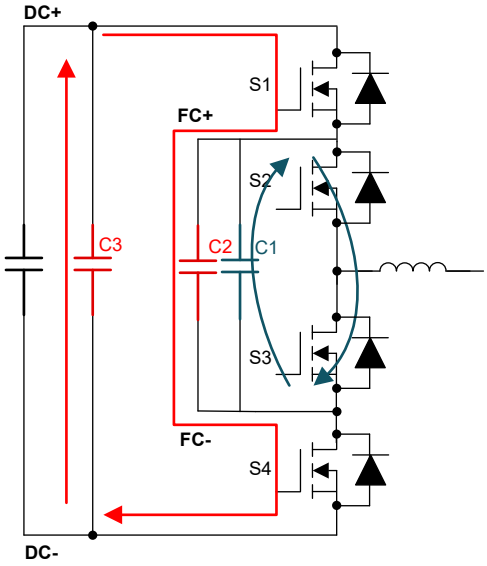

Figure 3-9. Commutation Loops of a 3-Level Flying Capacitor Switching Leg

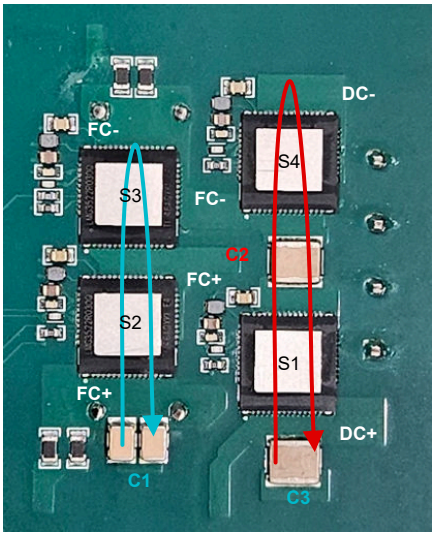

Figure 3-10. Layout of a 3-Level Flying Capacitor Switching Cell based on LMG3522R030

Note the flying capacitors are not shown in Figure 3-10. Only the decoupling ceramic capacitors are shown. The blue arrows represent the inner loop, which is composed of the parasitic inductance of S2, S3, and C1. This layout can be optimized by following the layout recommendation as shown in the datasheet of LMG3522R030. The red circle represents the external loop, which is composed of S1, S4, and C3. To decouple out the parasitic inductances of S2 and S3, the capacitor C2 can be placed in parallel to C1. Having this additional capacitor allows to improve the local layout and the FETs are spread out without impacting the power performance. A recommendation layout for a three-level flying capacitor switching cell is shown in Figure 3-10.

Note that from this picture that by adding the capacitor C2 the parasitic inductance of the switching loop is decreased. When adding additional components, as a result it becomes complicated handle gate driver signals due to a larger mechanical dimension of the board. This can cause the need of derating the switching speed of the FETs, thus increasing the total losses. This can be solved by using GaN transistors with integrated gate driver as LMG3522R030. Driving the GaN transistor quickly is possible because of the internal gate driver design.

3.4 Pre-Charging Network

A critical subject in flying capacitor converter is the precharging method of the flying capacitor itself.

During the nominal operation of the converter, the flying capacitor voltage level is set up to a nominal voltage of Vdc/2 by a voltage control loop. By having the flying capacitor voltage controlled to half the DC bus voltage, the voltage stress across the FETs can be specified to be half the DC bus voltage.

When connecting for the first time the converter to the grid, the MCU and AUX power supplies are off. During the precharging sequence of the converter, DC link voltage starts to rise but the flying capacitor voltage is still equal to zero. If the grid voltage is high and the DC bus voltage reaches value higher than the breakdown voltage of the transistor, the FETs risk damage. This problem is solved by using Zener diodes and resistors in parallel to the S1 and S4 as shown in Figure 3-11.

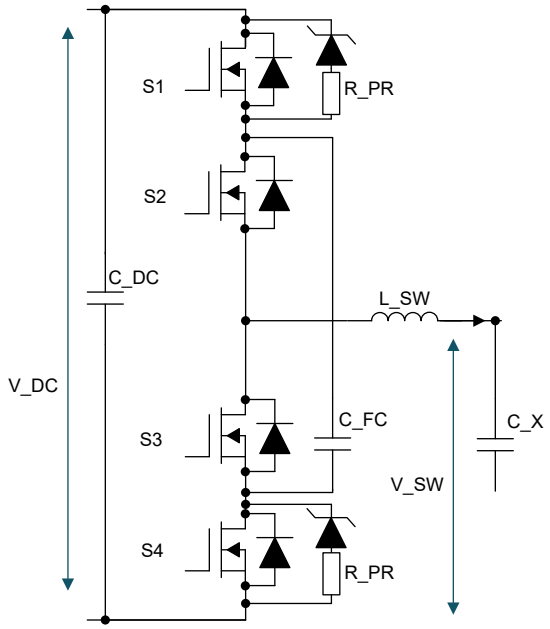

Figure 3-11. Precharging Network of the Three-Level Flying Capacitor Converter

Having Zener diodes in parallel to the FETS help to clamp the voltage across them. By doing this, once the Zener voltage is reached the flying capacitor starts to charge. To control the charging the current, a resistor of few ohms can be placed in series, thus limiting the charging current. A trade-off between the charging the current and the charging time can be found by changing the value of the resistor based on the capacitance value. The constant time of the circuit can be calculated in Equation 8.

$$\tau = 2R_{PR}C_{FC} \tag{8}$$

4 Experimental Results

In this chapter, experimental results of the reference design called TIDA-010957 are given [5]. This is a TI reference design rated for 15kVA based on TI GaN FETs (LMG3522R030) targeting three-phase plus neutral applications. This reference design can be connected to 900V DC link while still using 650V GaN transistors. Thanks to the integrated gate driver of the GaN FETs a switching speed of 70 kV/us is achieved. A schematic representation of the reference design can be found in Figure 4-1.

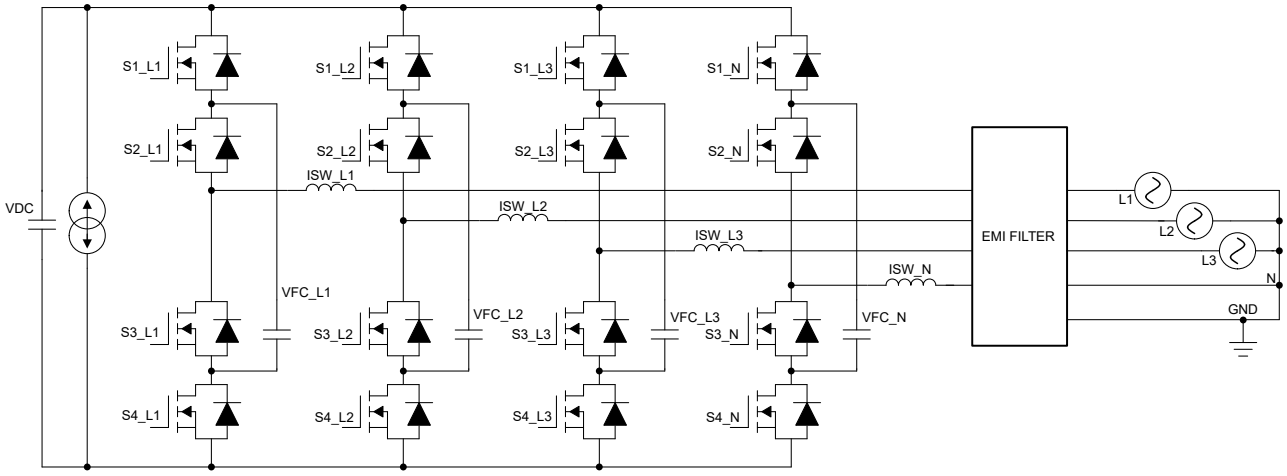

Figure 4-1. Schematic Representation of TIDA-010957 Reference Design

It can be noticed that in this topology, four clone branches are implemented by having for all of them flying capacitor topology. Each switching cell of the converter is capable of handling 21A_{rms}.

4.1 Pre-charging of the Flying Capacitor of TIDA-010957

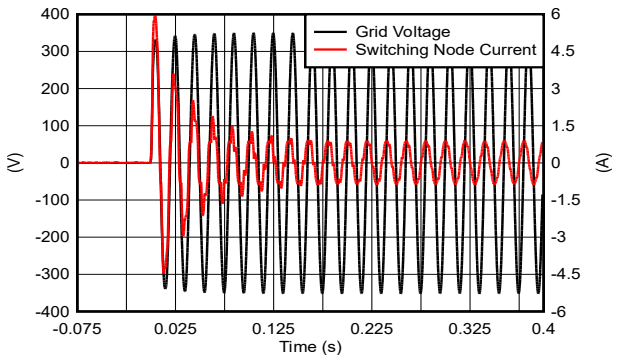

Figure 4-2. Precharging Sequence of the Flying Capacitor-Grid Voltage and Grid Current

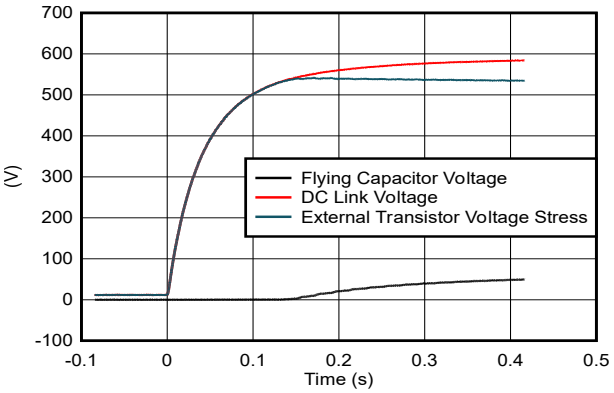

Figure 4-3. Precharging Sequence of the Flying Capacitor-DC link Voltage, Flying Capacitor Voltage and Voltage Stress of the External Transistor

In Figure 4-2 and Figure 4-3, waveforms associated with the precharging sequence are provided. The following waveforms are shown:

- Current on phase L1
- Voltage on phase L1
- DC link voltage
- Flying capacitor voltage
- Voltage stress of external transistors

In this test, the converter under test has been connected to the grid. Note that a grid voltage is present immediately on the terminal of the converter. Once the grid voltage is established a grid inrush current is generated. Voltages across the FETs are effectively clamped to 520V by the zener diodes.

4.2 Steady State Operation

This reference design was tested in four different operating modes:

- Inverter operation: power converted from the DC to the grid.
- PFC operation: power converter from the grid to the DC.
- Inverter plus Capacitive Power Compensator: active power is injected together with reactive power into the grid.
- Inverter plus Inductive Power Compensator: active power is injected and reactive power is drained from the grid.

The data collected during the experiments were collected and are shown in Figure 4-4 through Figure 4-11. In these pictures, switching node voltage, grid current and grid voltage for all the four operating points are shown.

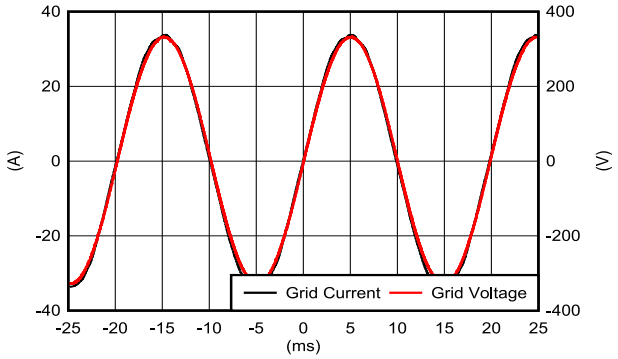

Figure 4-4. Experimental PFC Operation: Line Current, Line Voltage, and Switching Node Voltage (Figure A)

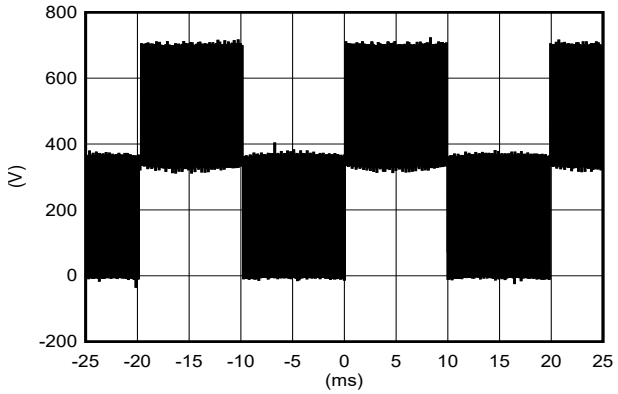

Figure 4-5. Experimental PFC Operation: Line Current, Line Voltage, and Switching Node Voltage (Figure B)

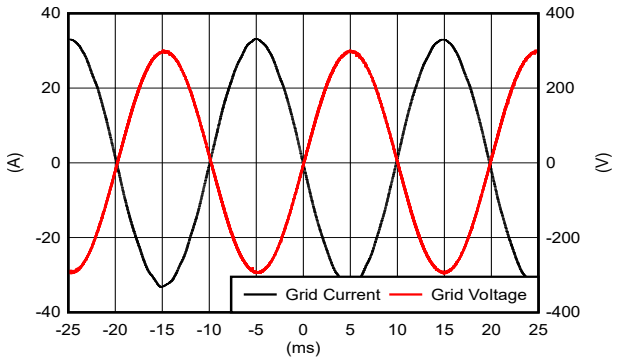

Figure 4-6. Experimental Inverter Operation: Line Current, Line Voltage, and Switching Node Voltage (Figure A)

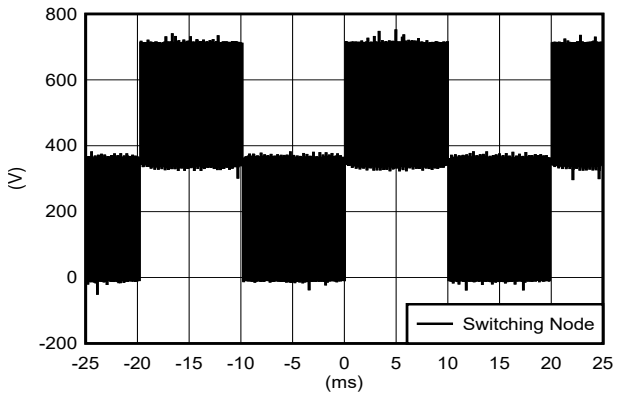

Figure 4-7. Experimental Inverter Operation: Line Current, Line Voltage, and Switching Node Voltage (Figure B)

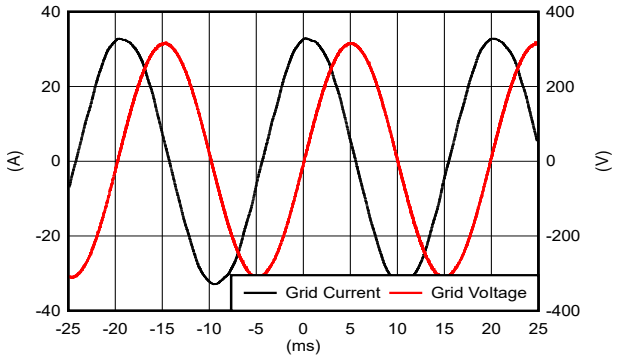

Figure 4-8. Experimental Inverter Plus Capacitive Compensation: Line Current, Line Voltage, and Switching Node Voltage (Figure A)

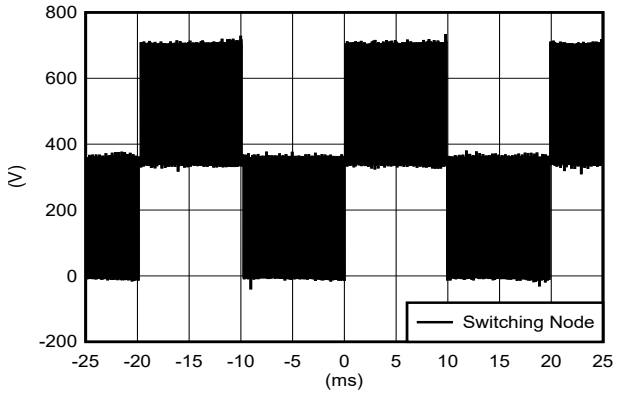

Figure 4-9. Experimental Inverter Plus Capacitive Compensation: Line Current, Line Voltage, and Switching Node Voltage (Figure B)

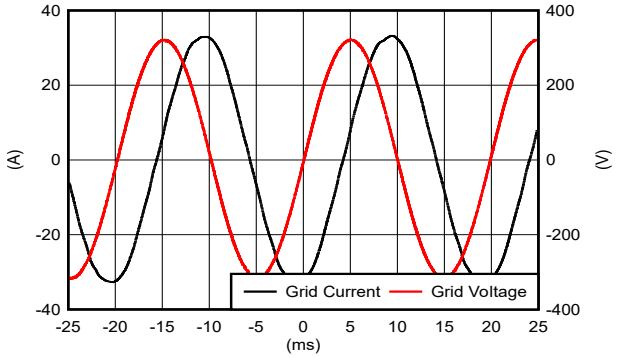

Figure 4-10. Experimental Inverter Plus Inductive Compensation: Line Current, Line Voltage, and Switching Node Voltage (Figure A)

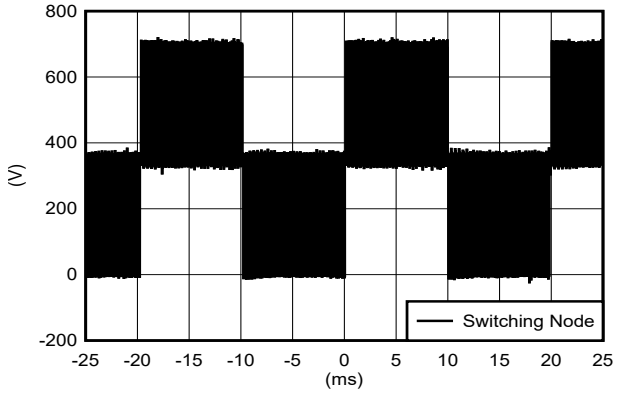

Figure 4-11. Experimental Inverter Plus Inductive Compensation: Line Current, Line Voltage, and Switching Node Voltage (Figure B)

At first, it can be observed that the switching node voltage shows three distinguished levels when considering the electrical frequency grid period. This is because half of the period a duty cycle lower than 50% is required and the other half of the period a duty cycle higher than 50% is required. Having three voltage levels plus doubling of the equivalent switching frequency permits the grid current to have a low ripple current as can be seen from the previous figures. Secondly, note that from these results that this topology can operate on all the operating points by keeping still the same performances because no worsening in the ripple current or efficiency were observed. In this reference design, by using LMG3522R030 a peak efficiency of 98.9% at 18kW was measured when having a mean junction temperature of 105°C. The junction temperature was derived from the device using the integrated temperature sensing feature.

5 Summary

Flying capacitor topologies are a preferred design when trying to decrease the converter size and increase efficiency. When adopting GaN transistors, switching frequency can be significantly increased, as a result, making this topology even more appealing. By using TI GaN FETs with integrated gate driver, it has been demonstrated that power layout can be optimized at its best. A switching speed of 70kV/µs has been achieved without no significant voltage overshoot.

A three-phase plus neutral reference designed rated 15kW has been taken as a reference in this work. This topology can operate in inverter, PFC and reactive power compensation. A peak efficiency close to 99% has been achieved.

6 References

1. Texas Instruments, *Design considerations of a 10kW single-phase string inverter based on TI GaN FETs,*, technical article.
2. How2Power, *Assessing Performance of A 10kW String Inverter Based on GaN FETs*, article.
3. Texas Instruments, *Comparison of AC/DC Power-Conversion Topologies for Three-Phase Industrial Systems*, seminar.
4. IEEE, *Inverter Side RL Filter Precise Design for Motor Overvoltage Mitigation in SiC-Based Drives*, article.
5. Texas Instruments, *15kW, Bidirectional, Three-Phase plus Neutral Flying Capacitor based on GaN Reference Design*, design guide.

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