Application Note

Designing EMC-Compliant, High-Accuracy Voltage (±10V) and Current (4-20mA) Input Measurement Systems With ADS125H18

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ABSTRACT

This application note provides practical guidelines for designing electromagnetic compatibility (EMC)-optimized voltage (±10V) and current (4-20mA) measurement systems for industrial settings. This application note delves into important design aspects to help designers pass standard EMC tests, including effective circuit design and printed circuit board (PCB) layout techniques. Additionally, this application note covers test setup considerations and the interpretation of IEC 61000-4-x standard EMC test results using an ADS125H18 EMC test board, aiding in the development of reliable industrial analog input modules.

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1 Design Overview and Measurement Performance (Normal Operation)

This section briefly introduces the ADS125H18 EMC test board and then demonstrates the voltage and current input measurement performance during normal operation.

1.1 Design Overview

Modern industrial control systems often use process-level voltage (±10V) or current (4-20mA) signaling to monitor and operate a factory or plant. An analog input module receives these signals and converts them to digital so the control system can make efficient and precise decisions. Therefore, designing high-accuracy voltage and current measurement systems that are also protected against electromagnetic interference (EMI), overvoltages, and other interference signals is critical.

The EMC test board discussed in this application note uses the ADS125H18, a precision, 24-bit, 1MSPS delta-sigma (ΔΣ) analog-to-digital converter (ADC) designed for use in analog input modules. The ADS125H18 can measure up to eight fully differential analog inputs or up to 16 single-ended high voltage input signals. Each input comprises a high-impedance voltage divider with integrated precision matched resistors to scale down the input voltage to the input range of the ADC. The ADS125H18 is equipped with a channel autosequencer and a FIFO (first-in, first-out) buffer. The power-scalable architecture provides four speed modes to optimize data rate, resolution, and power consumption. Figure 1-1 shows the ADS125H18 functional block diagram:

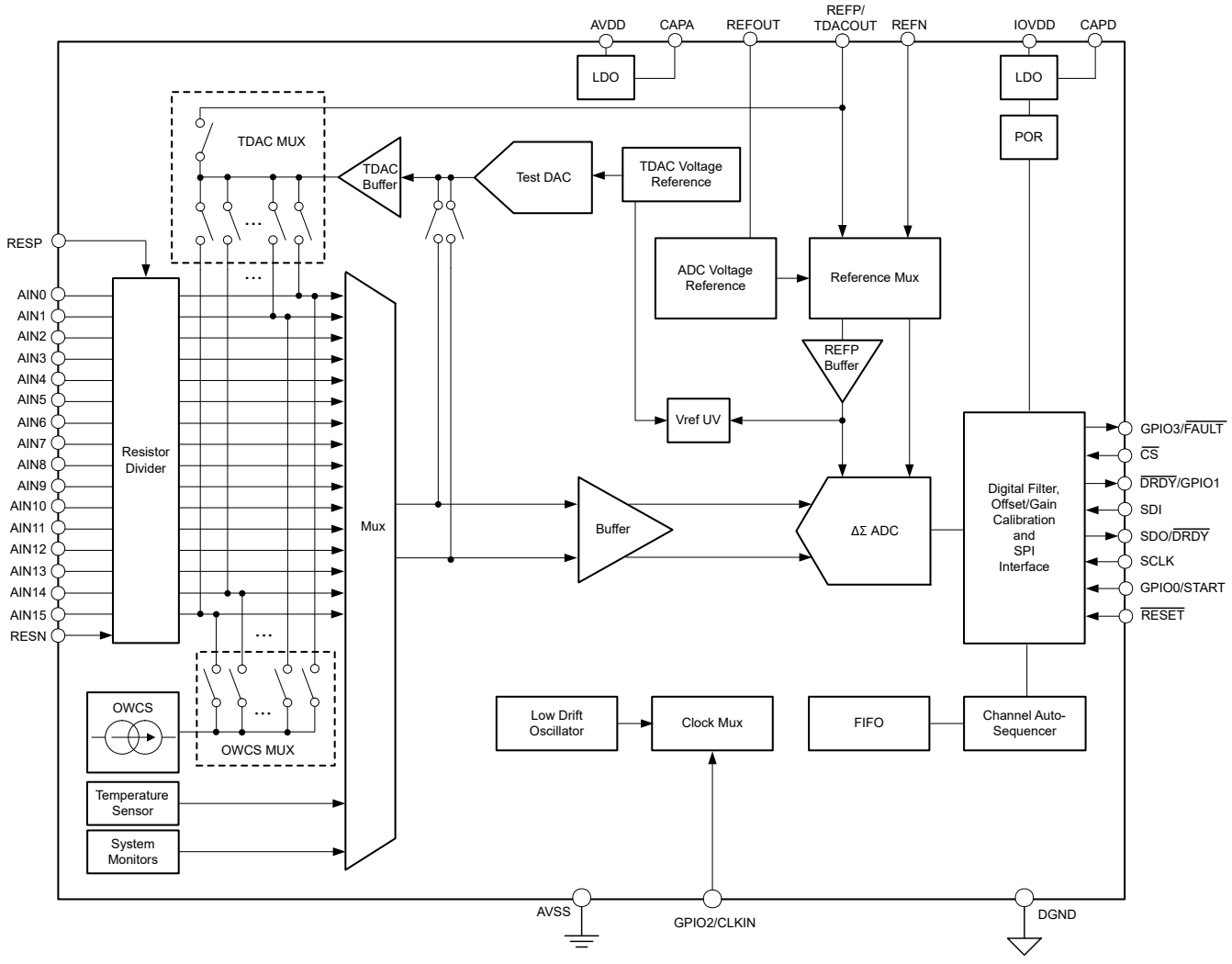

Figure 1-1. ADS125H18 Functional Block Diagram

The ADS125H18 EMC test board includes external isolated power supplies and a digital isolator. The digital isolator provides galvanic isolation between the ADC serial peripheral interface (SPI) and the precision host

interface (PHI) controller card that monitors conversion data from the ADS125H18. The PCB is designed to satisfy the IEC 61000-4-x standards for systems operating in a harsh electromagnetic environment.

Figure 1-2 shows an overall view of the EMC test board layout:

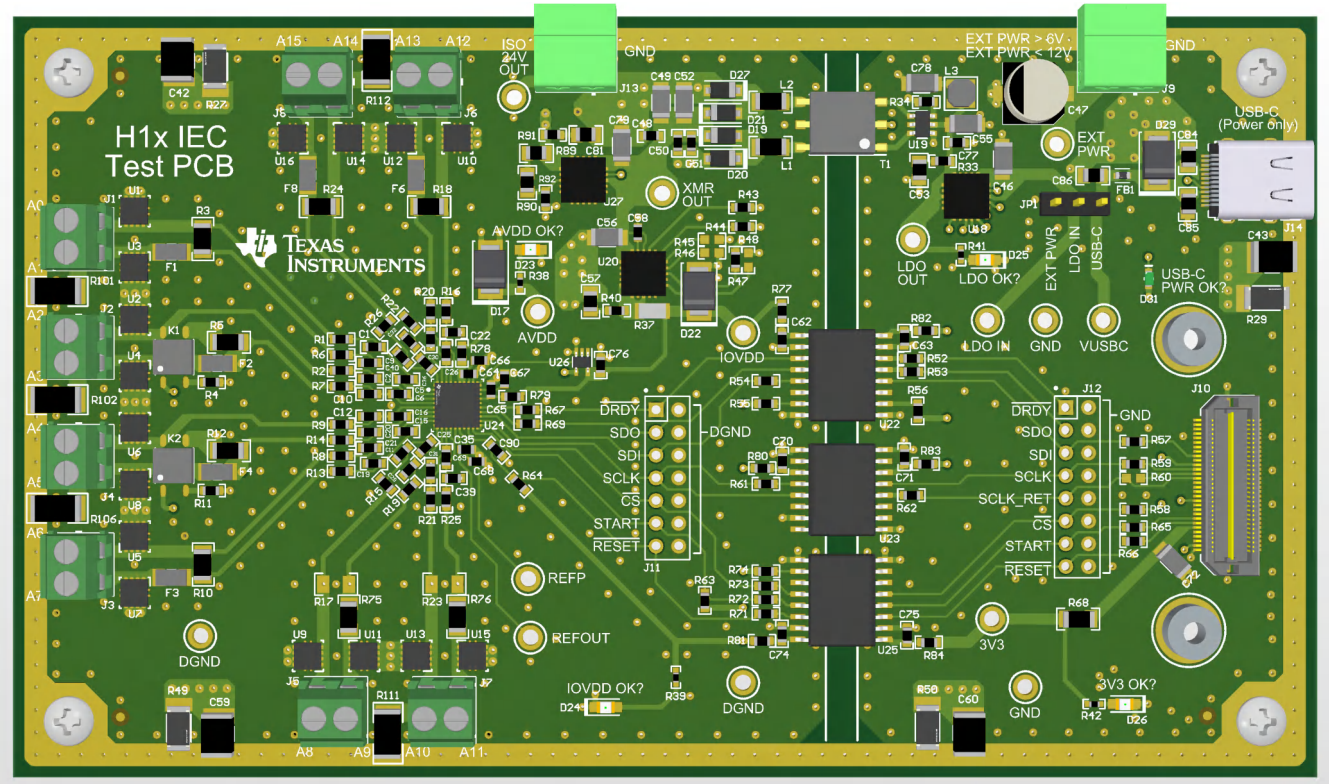

Figure 1-2. ADS125H18 EMC Test Board

1.2 EMC Test Board Voltage Measurement Performance During Normal Operation

Figure 1-3 shows a block diagram of the ADS125H18 measuring a 10V input signal. Note that no external components are required in this case because the ADS125H18 integrates a high-voltage resistor divider per channel such that the 10V signal can be measured directly by the ADC.

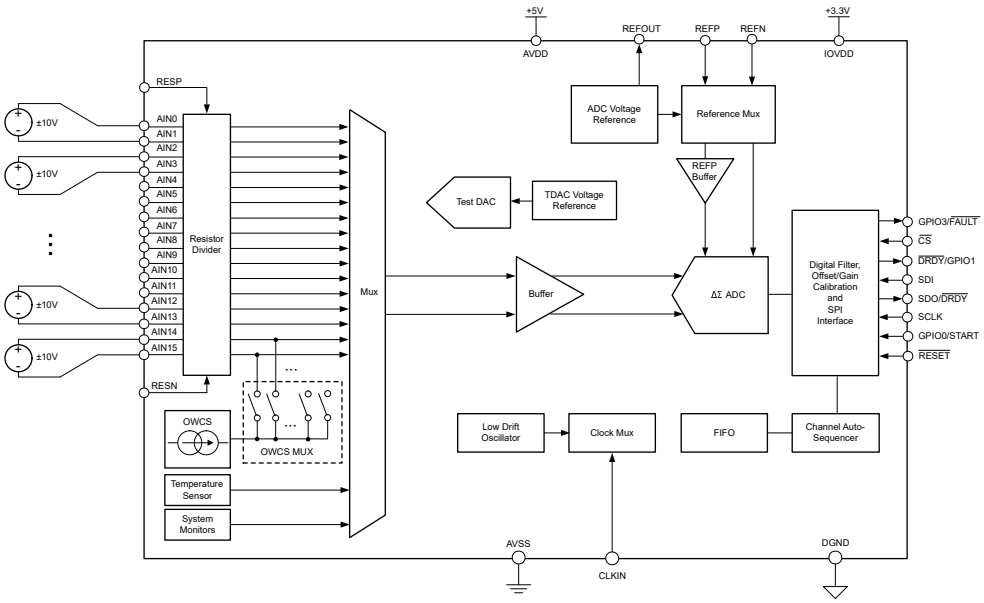

Figure 1-3. Voltage Input (±10V) Measurements Using the ADS125H18

The ADS125H18 on the EMC test board was programmed with the following settings to measure the circuit shown in Figure 1-3:

- 12.5kSPS data rate
- Sinc4 digital filter
- AIN8/AIN9 differential analog inputs
- Internal 2.5V reference
- Internal 25.6MHz oscillator
- Speed mode 3 (f_{MOD} = 12.8MHz)

Figure 1-4 shows the actual ADS125H18 EMC test board with a 9V battery connected to the inputs to mimic a 10V process signal:

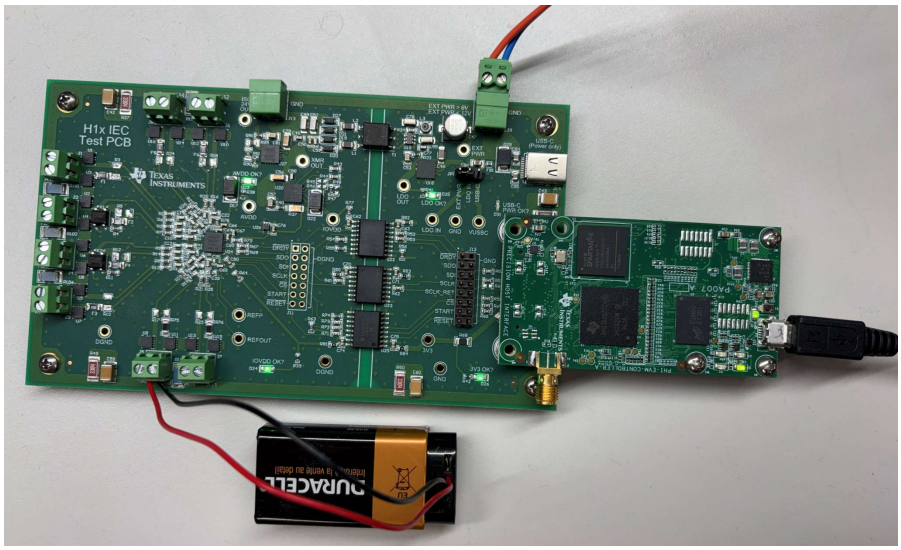

Figure 1-4. ADS125H18 EMC Test Board Measuring a 9V Battery

Calculate the ADS125H18 EMC test board performance by first measuring the actual input signal and reference voltage using a digital multimeter (DMM). These values were measured as follows:

- V_{IN} = 9.300V
- V_{REF} = 2.508V

Figure 1-5 shows the output from the ADS125H18 EVM graphical user interface (GUI) during the voltage measurement test:

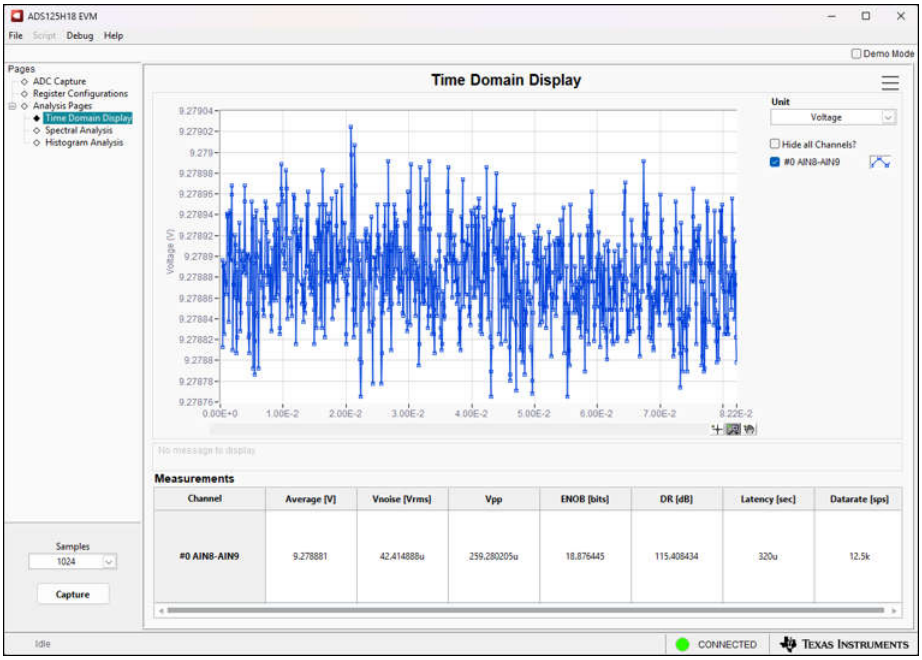

Figure 1-5. Voltage Measurement Results from the ADS125H18 EMC Test Board GUI

Use this information to determine the total unadjusted error (TUE) of these measurements using Equation 1:

$$\text{TUE} = \frac{(V_{ADC} - V_{DMM})}{V_{DMM}} \times 100 \quad (1)$$

where:

- V_{ADC} = Voltage measured by the ADC
- V_{DMM} = Voltage measured at the terminal block with a DMM

Equation 2 calculates the voltage measurement error using the average value of 9.278881V from Figure 1-5

$$\text{TUE} = \frac{(9.278881\text{V} - 9.300\text{V})}{9.300\text{V}} \times 100 = -0.228\,\% \quad (2)$$

Use the actual measured VREF voltage to determine the TUE with the VREF error removed. Equation 3 calculates the scaling value assuming $VREF_{Ideal}$ = 2.5V and $VREF_{Measured}$ = 2.508V:

$$\text{Scaling Factor} = \frac{\text{VREF}_{\text{Measured}}}{\text{VREF}_{\text{Ideal}}} = \frac{2.508\text{V}}{2.5\text{V}} = 1.0032 \quad (3)$$

Equation 4 calculates the voltage measurement error with the VREF error removed:

$$\text{TUE}_{\text{No\_VREF\_Error}} = \frac{(9.278881\text{V} - 9.300\text{V})}{9.300\text{V}} \times 100 = 0.04\,\% \quad (4)$$

Ultimately, these results indicate that the ADS125H18 EMC test board is a high-performance system for process-level voltage measurements such as ±10V.

1.3 EMC Test Board Current Measurement Performance During Normal Operation

Figure 1-6 shows a block diagram of the ADS125H18 measuring a 20mA input signal. These measurements require an external shunt to convert current to a voltage that can be measured by the ADC. The ADS125H18 EMC test board includes current-measurement shunts on certain channels for this purpose.

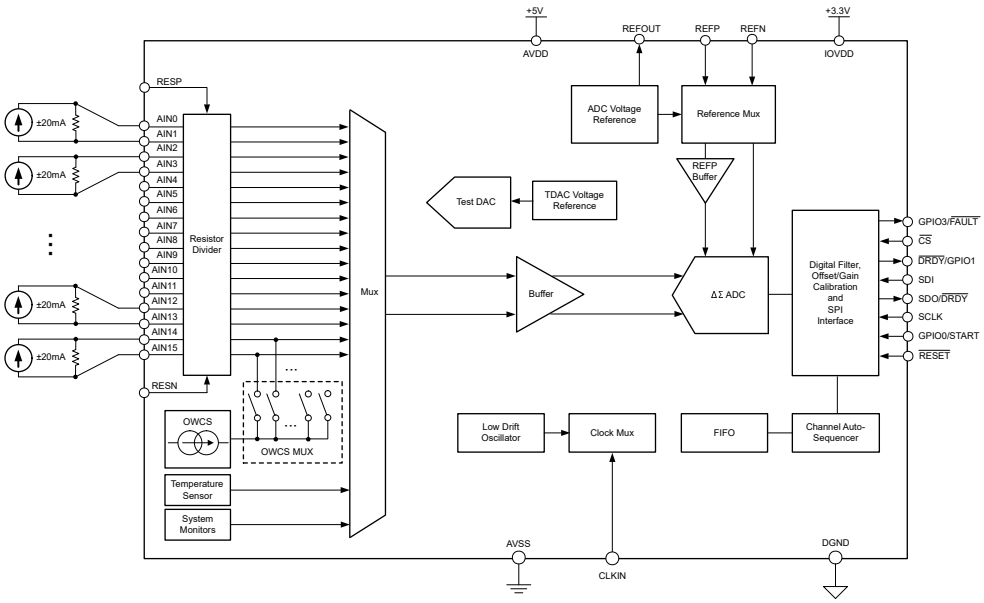

Figure 1-6. Current Input (±20mA) Measurements Using the ADS125H18

The ADS125H18 on the EMC test board was programmed with the following settings to measure the circuit shown in Figure 1-6:

- 12.5kSPS data rate
- Sinc4 digital filter
- AIN0/AIN1 differential analog inputs
- Internal 2.5V reference
- Internal 25.6MHz oscillator
- Speed mode 3 (f_{MOD} = 12.8MHz)

Figure 1-7 shows the actual ADS125H18 EMC test board connected to an XTR111EVM that generates the current output signal. The EMC test board isolated 24V output powers the XTR111EVM. The XTR111EVM generate a 10mA output using the 2.5V ADC REFOUT voltage as its input. The ADS125H18 measures this 10mA output across an external 100Ω shunt placed between the AIN0 and AIN1 inputs.

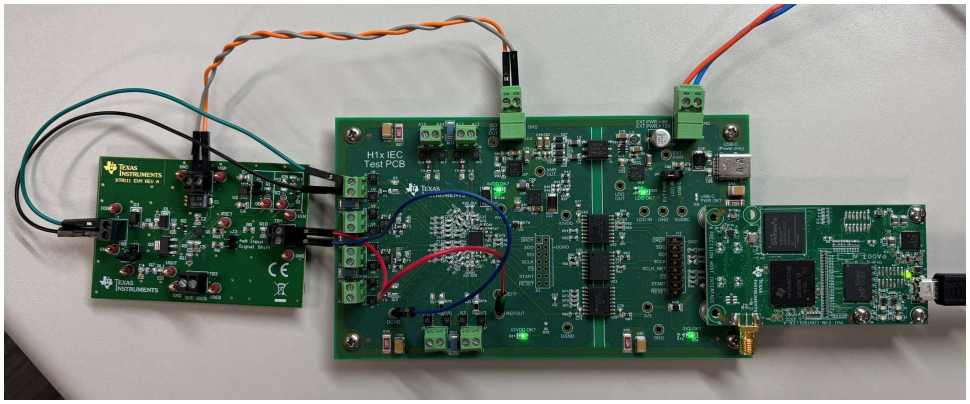

Figure 1-7. ADS125H18 EMC Test Board Measuring the Current Output from XTR111EVM

Calculate the ADS125H18 EMC test board peformance by first measuring the actual input current, shunt resistance, and reference voltage using a multimeter. These values were measured as follows:

- R_{Shunt} = 100Ω
- I_{IN} = 10.06mA
- V_{IN} = 100Ω ×10.06mA = 1.006V
- V_{REF} = 2.508V

Figure 1-8 shows the output from the ADS125H18 EVM GUI during the current measurement test:

Figure 1-8. Current Measurement Results from the ADS125H18 EMC Test Board GUI

Use this information to determine the total unadjusted error (TUE) of these measurements using Equation 5:

$$\text{TUE} = \frac{(V_{ADC} - V_{DMM})}{V_{DMM}} \times 100 \quad (5)$$

Equation 6 calculates the current measurement error using the average value of 1.003111V from Figure 1-8

$$\text{TUE} = \frac{(1.003111\text{V} - 1.006\text{V})}{1.006\text{V}} \times 100 = -0.287\,\% \quad (6)$$

Use the actual measured VREF voltage to determine the TUE with the VREF error removed. Equation 7 calculates the scaling value assuming $VREF_{Ideal}$ = 2.5V and $VREF_{Measured}$ = 2.508V:

$$\text{Scaling Factor} = \frac{VREF_{Measured}}{VREF_{Ideal}} = \frac{2.508\text{V}}{2.5\text{V}} = 1.0032 \quad (7)$$

Equation 8 calculates the current measurement error with the VREF error removed:

$$\text{TUE}_{No\_VREF\_Error} = \frac{(1.00632\text{V} - 1.006\text{V})}{1.006\text{V}} \times 100 = 0.032\,\% \quad (8)$$

Ultimately, these results indicate that the ADS125H18 EMC test board is a high-performance system for process-level current measurements such as 4-20mA or ±20mA.

2 EMC Test Board Circuit and PCB Layout Considerations

This section discusses the circuit and PCB layout considerations that enable an EMC-compliant, process-level voltage and current measurement system.

2.1 Circuit Design Considerations for EMC Compliance

This section describes the EMC test board circuit design that protects the ADS125H18, improves system EMC performance, and maintains measurement accuracy. Figure 2-1 shows a block diagram of the ADS125H18 EMC test board:

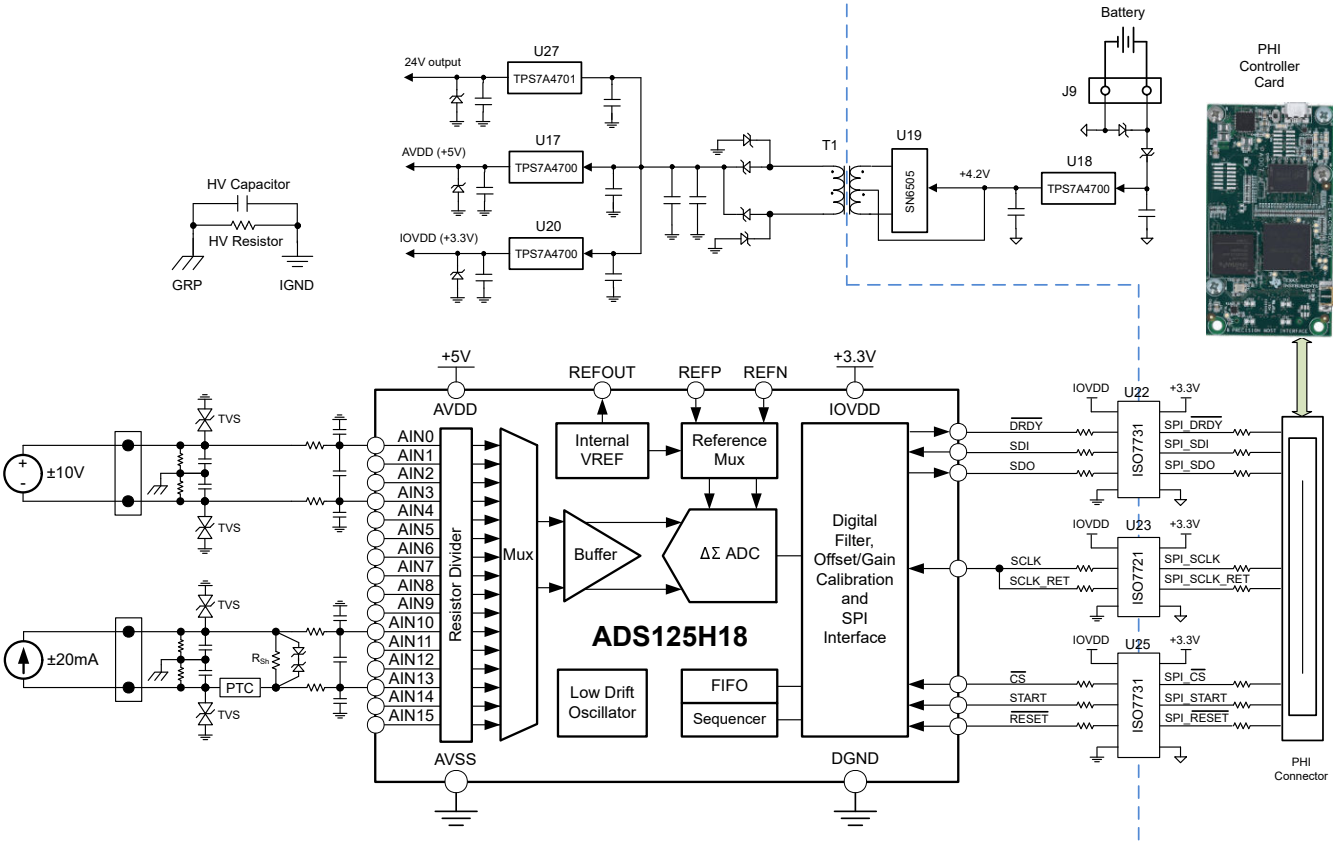

Figure 2-1. ADS125H18 EMC Test Circuit Board with 10V Input Signal and PHI Connection

Considerations for the EMC test board include:

- High-Voltage Capacitors and Resistors on Every Input Connector Pin
- TVS Diodes
- Protecting the Current Shunt: PTC and Zener Diodes
- Series Resistors on Digital Signals
- Digital Isolation
- Power Supply and Protection
- High-Voltage Capacitors and Resistors for Discharging Path

2.1.1 High-Voltage Capacitors and Resistors on Every Input Connector Pin

Filtering signals directly at the input connector helps increase electrostatic discharge immunity, reduce radiated emissions, and increase immunity to coupled burst signals on the input. Every input signal that enters the PCB needs a filter element such as a ceramic capacitor. Connect the capacitor between the input connector and earth ground with a wide trace. Place this capacitor as close as possible to the connector pin.

Figure 2-2 shows the high-voltage capacitor circuit on the EMC test boards.

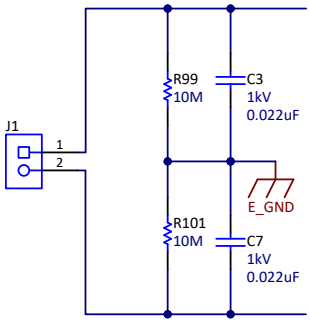

Figure 2-2. High-Voltage Capacitors on Input Connector

Use a high-voltage rated capacitor because this component is exposed to high-energy transient signals including electrostatic discharge, electrical fast transients, or surge signals during the EMC test.

Use the input signal frequency to determine the capacitor value. This design measures low-frequency voltage and current signals such that larger value capacitors can be used. Therefore, this design uses a 1kV high voltage, X7R type, 0.022µF ceramic capacitor on each ADC channel as close as possible to the input terminal blocks so that the transient energy is discharged to earth ground through the shortest path.

Figure 2-2 also shows a 10MΩ resistor in parallel with the capacitor. These resistors help discharge the capacitor to avoid charge build up during repeated transients. Otherwise, this charge accumulates and reduces the effectiveness of the capacitor. Use a high-voltage rated resistor in the range of 1-10MΩ for these components.

2.1.2 TVS Diodes

Each analog input includes a bidirectional TVS diode to ground. The TVS3301 flat clamp TVS diode has a reverse stand-off voltage of ±33V and a typical breakdown voltage of ±37.5V. These TVS diodes also have low leakage across temperature for high-accuracy applications. These diode characteristics shunt transient energy away from the signal path while:

- Enabling measurement of bidirectional signals (±10V) without interference
- Supporting up to 30V input voltages including a common-mode offset
- Remaining inactive during a sustained overvoltage fault condition where the 24V power supply is shorted to the inputs for example

Select an alternative TVS diode with similar characteristics for best performance. Figure 2-3 shows a TVS3301 installed on both the A0 and A1 pins for one of the ADS125H18 EMC test board current input channels.

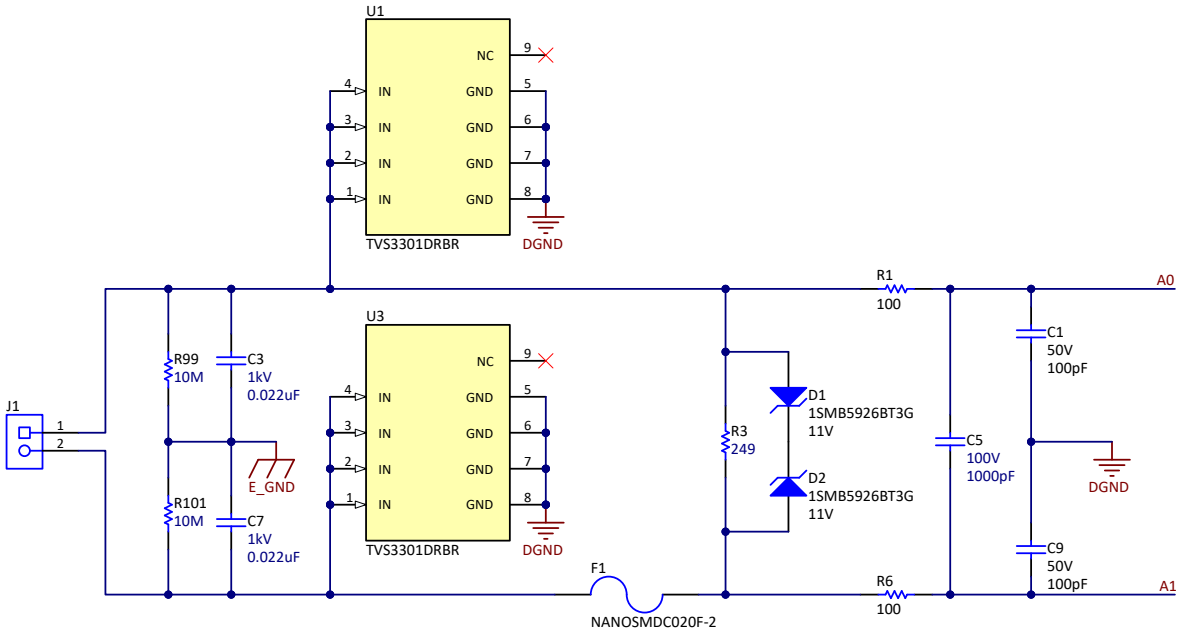

Figure 2-3. Bidirectional TVS Diodes on each Analog Input

2.1.3 Protecting the Current Shunt: PTC and Zener Diodes

Figure 2-3 shows that the EMC test board includes 249Ω shunts (R3) on certain analog inputs. These shunts convert the current output from a field transmitter to a voltage that the ADC measures during normal operation. However, fault conditions can occur that apply a sustained overvoltage to the shunt and potentially cause its destruction. For example, the most common overvoltage event occurs when the nominally 24V power supply gets accidentally shorted to the inputs. Equation 9 and Equation 10 calculate the current through and the power dissipated by a 249Ω shunt that has 24V applied, respectively:

$$I_{Shunt} = \frac{V_{Supply}}{R_{Shunt}} = \frac{24V}{249\Omega} = 96.4mA \quad (9)$$

$$P_{Shunt} = I_{Shunt}^{2} \times R_{Shunt} = 96.4mA^{2} \times 249\Omega = 2.31W \quad (10)$$

Equation 10 shows that a typical 0.1W or 0.25W shunt would be destroyed under these fault conditions. Therefore, the ADS125H18 EMC test board uses back-to-back Zener diodes and a PTC fuse to help protect the shunt as follows:

- The back-to-back Zener diodes — D1 and D2 in Figure 2-3 — protect the shunt by clamping to a specific voltage during both positive and negative overvoltages. This clamping voltage limits the current through the shunt such that any remaining fault current flows through the diodes
- The PTC fuse — F1 in Figure 2-3 — protects the Zener diodes by increasing its resistance due to increasing temperature. The temperature increase results from excessive power dissipation because of the large fault current flowing through the diodes. The elevated PTC fuse resistance then reduces the total fault current sourced from the supply and stabilizes the system

Figure 2-4 shows a current input channel on the ADS125H18 EMC test board with the back-to-back Zener diodes and the PTC fuse highlighted in yellow:

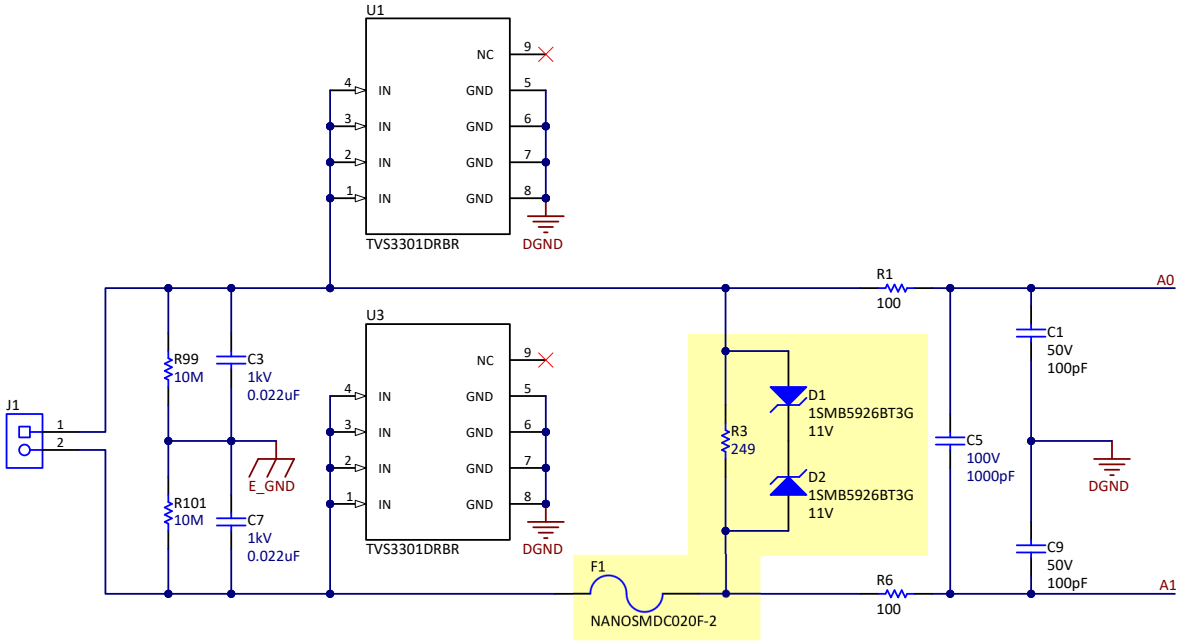

Figure 2-4. Shunt Protection Circuitry on the ADS125H18 EMC Test Board

Table 2-1 describes important Zener diode parameters, their definitions, and example values:

Table 2-1. Important Zener Diode Parameters, Definitions, and Values

Parameter	Definition	Value (@25°C)
Zener voltage (V_Z)	Amount of current that can pass through the PTC without tripping	11V
Surge power (P_S)	Amount of time the diode can sustain a given input current	90W for 1.5ms
Forward voltage (V_F)	Diode voltage drop when it is forward biased	0.7V
Leakage current (I_R)	Residual device current in the off state that flows through the shunt and creates a measurement error	1µA
DC Zener current (I_Z)	Current at which the Zener diode clamps	136mA

Table 2-2 describes important PTC fuse parameters, their definitions, and example values:

Table 2-2. Important PTC Fuse Parameters, Definitions, and Values

Parameter	Definition	Value (at 25°C)
Hold current (I_H)	Amount of current that can pass through the PTC without tripping at 25°C	200mA
Trip current (I_T)	The current at which the PTC begins to trip at 25°C	600mA
Max current (I_{MAX})	Maximum current that can flow through the PTC without damaging the device	30A
Power dissipation (P_D)	The power dissipated by the PTC in the tripped state	0.9W
Time to trip (t_{Trip})	Amount of time for the PTC to trip for a given input current	1.5ms at 8A

It helps to walk through an example to understand how these components protect the shunt. Assume a 24V power supply with an 8A current limit accidentally shorts across the shunt. The Zener diodes instantaneously clamp the voltage across the shunt while the fault current passes through the Zener diodes instead of the shunt. Equation 11 calculates the total clamped voltage across the shunt using the values from Table 2-1:

$$V_{Clamp} = V_Z + V_F = 11V + 0.7V = 11.7V \quad (11)$$

The Zener diodes clamp the voltage across the shunt at 11.7V. Equation 12 and Equation 13 calculate the current through the shunt as well as the power dissipated by the shunt under these conditions, respectively:

$$I_{Shunt} = \frac{V_{Clamp}}{R_{Shunt}} = \frac{11.7V}{249\Omega} = 47mA \quad (12)$$

$$P_{Shunt} = \frac{V_{Clamp}^2}{R_{Shunt}} = \frac{11.7V^2}{249\Omega} = 0.55W \quad (13)$$

The remaining power supply current passes through the Zener diodes. Equation 14 and Equation 15 calculate the current through the diodes as well as the power dissipated by the diode under these conditions, respectively:

$$I_{Zener} = I_{Supply} - I_{Shunt} = 8A - 47mA = 7.953A \quad (14)$$

$$P_{Zener} = V_{Zener} \times I_{Zener} = 11V \times 7.953A = 87.48W \quad (15)$$

The diode surge power (P_S) specification indicates how long the diodes can survive during the overcurrent event. The diode datasheet often provides a plot showing pulse duration on the x-axis and peak power on the y-axis because the diode can support higher current as the pulse duration decreases. In this example, the Zener diode supports P_S = 90W for 1.5ms. Therefore, the diode can support the overcurrent conditions for approximately 1.5ms given the result in Equation 15. Figure 2-5 shows the circuit behavior at the instant the power supply shorts to the input. Note that some components have been removed for simplicity.

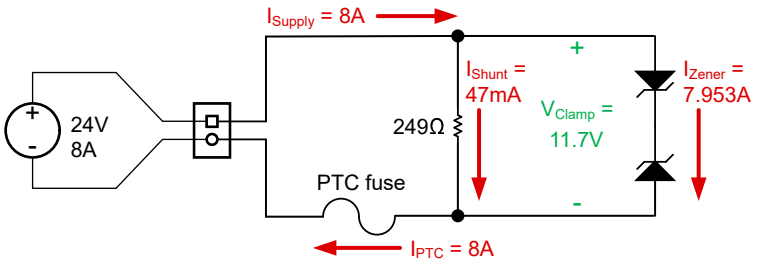

Figure 2-5. Shunt Protection Circuit Immediately After the Power Supply Shorts

Select a PTC fuse such that the component trip time versus current is less than P_S so the diode does not get damaged. The PTC fuse protects the diode in this example because t_{Trip} = 1.5ms (at 8A) according to the specifications in Table 2-2. The PTC fuse resistance increases significantly in the tripped state, reducing the current sourced by the power supply and dropping the remaining supply voltage across the fuse as shown in Equation 16:

$$V_{PTC} = V_{Supply} - V_{Shunt} = 24V - 11.7V = 12.3V \quad (16)$$

The PTC fuse also maintains the power dissipation specification (P_D) in the tripped state. Equation 17 calculates the PTC fuse current given the P_D specification from Table 2-2:

$$I_{PTC} = \frac{P_D}{V_{PTC}} = \frac{0.9W}{12.3V} = 73mA \quad (17)$$

The remaining current passes through the Zener diode as shown in Equation 18:

$$I_{Zener} = I_{PTC} - I_{Shunt} = 73mA - 47mA = 26mA \quad (18)$$

Confirm that I_{Zener} is less than the Zener maximum DC current specification (I_Z) when the PTC fuse trips. Equation 18 shows that I_{Zener} = 26mA, which is well within the limit of I_Z = 136mA specified in Table 2-1. Figure 2-6 shows the circuit behavior when the PTC fuse trips after 1.5ms.

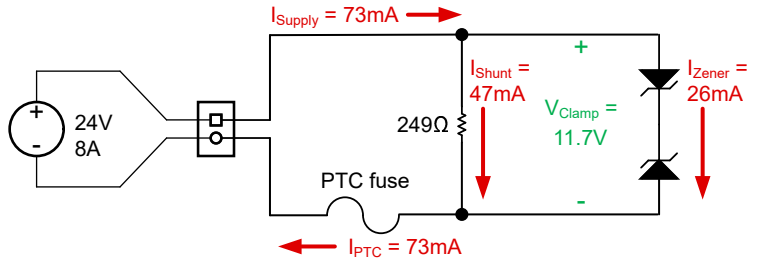

Figure 2-6. Shunt Protection Circuit 1.5ms After the Power Supply Shorts

The circuit remains in the state shown in Figure 2-6 until the fault condition is removed. Therefore, design the system to ensure all components can support the required voltages and currents indefinitely. Also consider the following factors to select shunt protection components in an industrial application:

- The PTC fuse behavior changes with temperature. Take care at low temperatures because the trip current and power dissipation are much higher. This behavior requires the Zener diodes to support much larger DC currents after the PTC fuse trips. Comparatively, the PTC fuse trips at a much lower current at higher temperatures. This behavior might cause the PTC fuse to trip while the system is measuring a valid current
- Two shunts in parallel can help reduce the total power dissipation across each device because the current reduces by a factor of two while the resistance increases by a factor of two. However, the power equation squares the current ($P = I^2R$) such that the power dissipated by each shunt reduces by a factor of two compared to single shunt.
- The Zener diode leakage current adds to the measured input current and creates an error. Choose a low leakage component to maintain a high-accuracy system

2.1.4 Series Resistors on Digital Signals

Fast transitions on high-speed digital signals can lead to radiated emissions or reflections in the case of a long transmission line. Adding a series resistor can help increase the rise- and fall-time of any digital signal — especially high-speed clock signals — and improve EMC performance by:

- Slowing down transition edges: A series termination resistor effectively increases the time constant of the digital line by adding a resistance in series with the trace capacitance and inductance.
- Reducing reflections and emissions: A series termination resistor can minimize the reflections that can cause ringing, overshoot, and undershoot by matching the source impedance to the characteristic impedance of the transmission line.
- Reducing high-frequency harmonics: longer transition times can result in lower bandwidth and high-frequency harmonics that are often responsible for radiating emissions.
- Improving signal integrity: A series termination resistor helps improve the integrity of the digital signal, leading to more reliable data transmission.

Select the value of the series resistor to match the characteristic impedance of the transmission line for optimal impedance matching and minimal reflections. Figure 2-7 shows the 49.9Ω resistors on the digital lines between the ADS125H18, digital isolator, and the PHI controller board. Place the series resistor as close to the driver as possible for effective series termination.

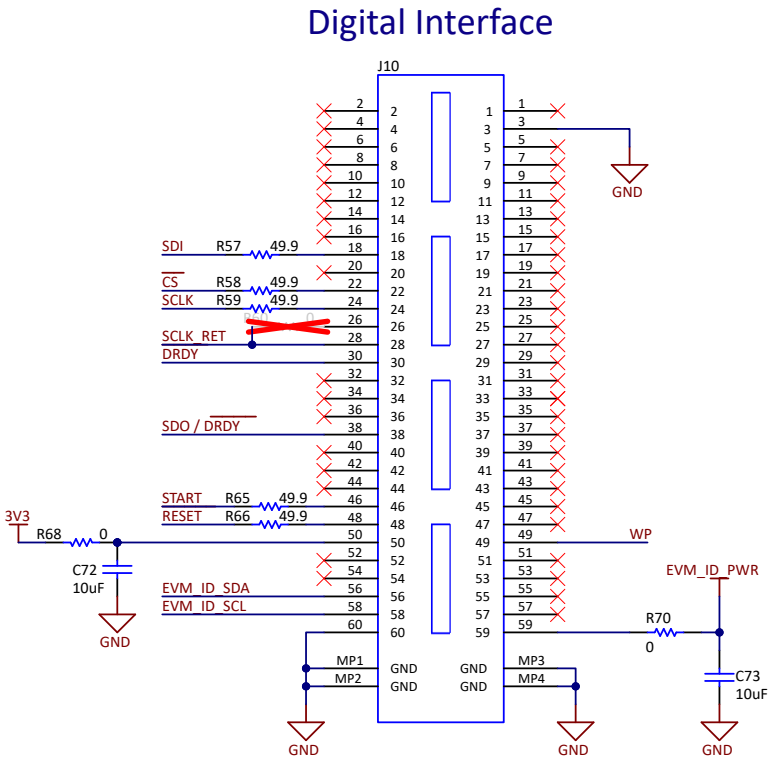

Figure 2-7. Inserting Series Resistors on Digital Signals

2.1.5 Digital Isolation

This EMC test board uses the ISO7721, ISO7730, and ISO7731 digital isolators to isolate data communication. These reinforced isolators have high immunity, a 5kVrms (DW package) isolation rating, 8kVpk maximum transient isolation voltage, and 12.8kVpk maximum surge isolation voltage. These isolators support signal rates up to 100Mbps with a low propagation delay (11ns) and a wide supply range (2.25V to 5.5V).

Each digital isolator also includes a 0Ω resistor on the supply pin that can be used to filter high frequency noise. Replace these resistors with 1-3Ω components or install a ferrite bead to remove specific frequencies.

Figure 2-8 shows the digital isolation circuit on the EMC test boards:

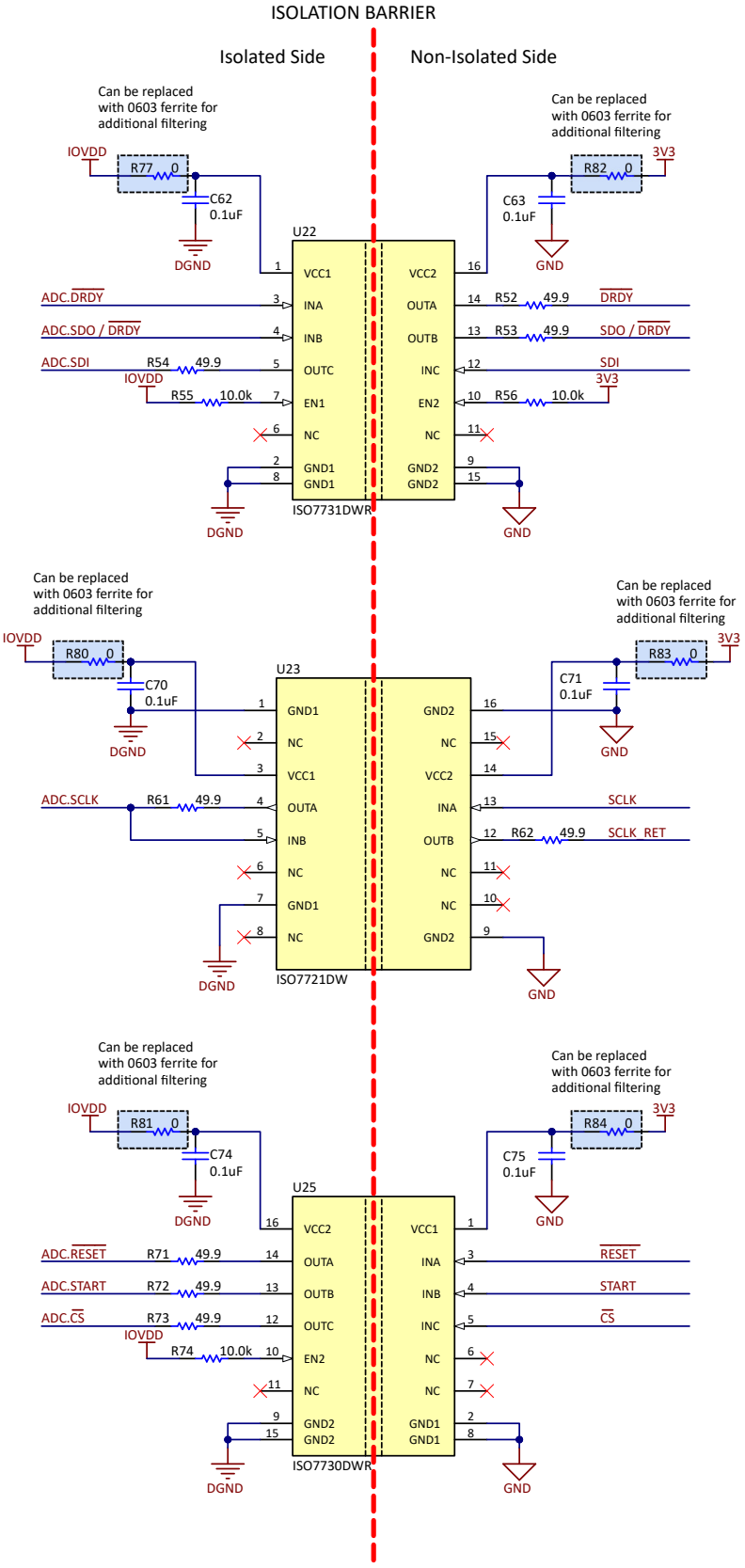

Figure 2-8. Digital Isolation

2.1.6 Power Supply and Protection

The EMC test board power supply circuits are intentionally designed to mimic typical industrial systems. By default, only one power supply between +6V and +12V on J9 is required to power the entire circuit board.

Non-Isolated Side

The TPS7A4700 (U18) low-dropout regulator (LDO) converts an externally-provided power supply (6V to 12V) to a steady 4.2V. This 4.2V output powers a low-noise, low-EMI push-pull transformer driver, SN6505 (U19). The PHI controller card directly provides the 3.3V supply for the ISO7721, ISO7730, and ISO7731 digital isolators on the non-isolated side of the test board.

The ADS125H18 EMC test board can also be powered by an external USB-C power supply using connector J14. This connection is intended to power the board during any non-EMC testing. The input LDO (U18) outputs 4.2V specifically to account for any losses in the USB voltage.

Isolated Side

Transformer T1 has a turns ratio of 1:3.45 and uses a bipolar configuration to produce a voltage gain of approximately 6.9 from the non-isolated to the isolated side of the board. Therefore, the 4.2V input voltage is approximately 29V at the transformer output. This voltage mimics the standard 24V isolated supply voltage in analog input module systems.

TPS7A4701 (U27) regulates the output of the transformer to generate a 24V output signal at connector J13. The unregulated transformer output voltage is also provided to two TPS7A4700 (U17 and U20) LDOs that generate the ADS125H18 AVDD (5V) and DVDD (3.3V) supplies, respectively. TVS diodes protect the outputs of each regulated supply

Figure 2-9 shows the power supply schematic.

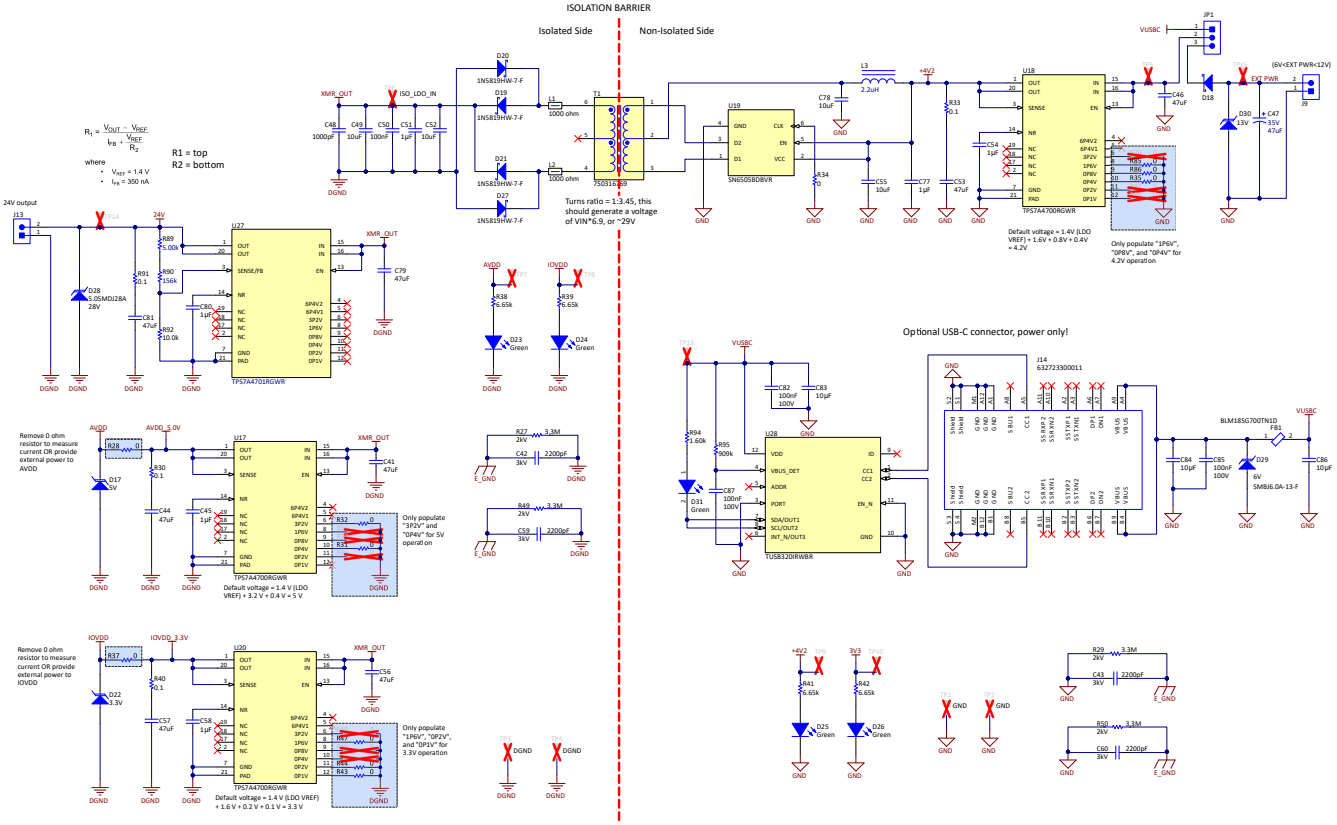

Figure 2-9. ADS125H18 EMC Test Board Power Supply Schematic

2.1.7 High-Voltage Capacitors and Resistors for Discharging Path

A high voltage 3kV, 2.2nF capacitor and a 2.2kV, 3.3MΩ resistor are placed in parallel between the local ground and earth ground. These components provide a path to discharge transient energy to the earth ground and protect the components on the circuit board. Two discharge paths including R27 || C42 and R49 || C59 are designed on the isolated side of the circuit board. The same components in parallel are installed on the non-isolated side of the EMC test board: R29 || C43 and R50 || C60.

Figure 2-10 shows the high-voltage capacitor and resistor schematic and PCB layout example on the EMC test boards:

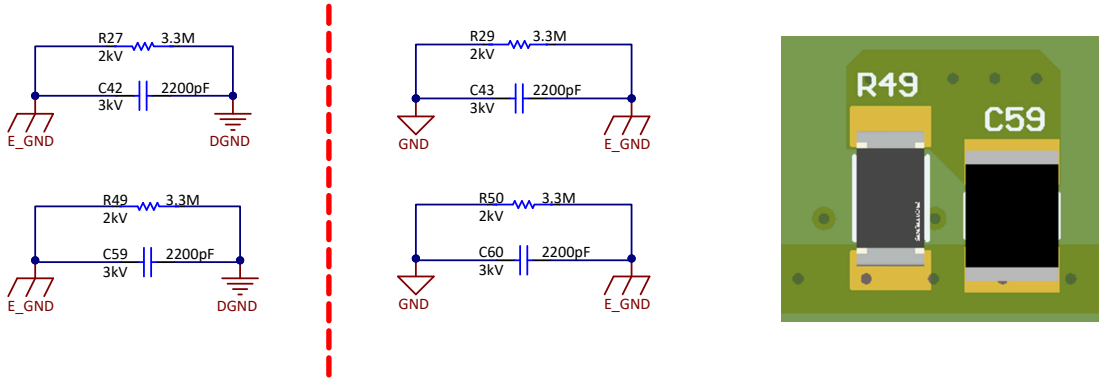

Figure 2-10. Adding High-Voltage Capacitors and Resistors

2.2 PCB Layout Considerations for EMC Compliance

Designing a PCB board that measures voltage and current process signals requires special attention to pass EMC testing because these signals are highly susceptible to both radiated and conducted interference. The following layout practices help verify the PCB design is robust against EMC phenomena while maintaining signal integrity and measurement accuracy:

- PCB Layer Stack-up and Ground Plane
- Avoiding a Long Return Path
- Avoiding 90-Degree Bends in PCB Traces
- Using a Guard Ring to Isolate Interference Signals
- Decoupling Capacitors
- Differential Routing
- Stitching Vias
- Layout for Isolation Barrier
- Component Placement

2.2.1 PCB Layer Stack-up and Ground Plane

A continuous and uninterrupted ground plane is fundamental to achieve EMC compliance. An uninterrupted ground plane provides a low impedance return path for signal currents and acts as a shield against external interference.

Additionally, proper PCB layer stack-up is critical for EMC performance and signal integrity. Place higher-speed and critical signals, such as the SPI SCLK signal, on the layer that is adjacent to the ground plane, while non-critical signals can be placed near the power plane if applicable. Figure 2-11 shows a typical multi-layer circuit board stack-up. Power and ground planes are adjacent to each other as they provide additional interplane capacitance, which helps with high frequency decoupling of the power supply.

A good configuration is:

- Top layer: mixed analog/digital signal routing
- Layer 2 (inner layer): solid ground plane
- Layer 3 (inner layer):
  - Power plane with isolated analog and digital sections (if necessary)

  - Solid ground plane (if no power plane is required)
- Bottom layer: additional signal routing or shielding if needed.

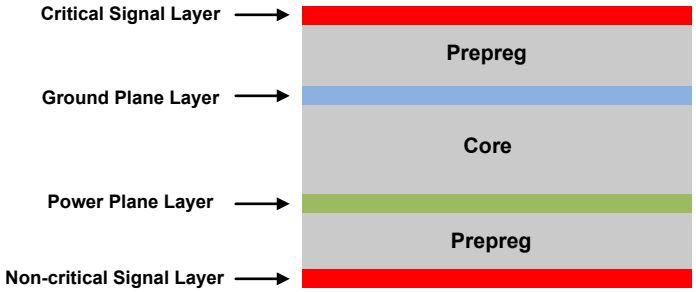

Figure 2-11. Example 4-Layer PCB Stack-Up

A typical 4-layer PCB should have at least one dedicated layer as the ground plane to ensure a low impedance path for the return signals. The stack-up design places a solid ground layer directly adjacent to the signal layers providing consistent return paths and minimizing the loop area and electromagnetic radiation. The ADS125H18 EMC test board uses two solid ground planes as shown in Figure 4-6 and Figure 4-7.

2.2.2 Avoiding a Long Return Path

A long or disrupted current return path can act as a radiating antenna, increasing susceptibility to EMI and violating EMC requirements. Every signal trace must be routed such that its return current flows directly beneath it through the ground plane. This practice is important for high accuracy process signal measurement such as ±10V or 4-20mA.

2.2.3 Avoiding 90-Degree Bends in PCB Traces

Trace geometry can significantly affect signal integrity and emissions. Sharp 90-degree bends in PCB traces should be avoided because they create impedance discontinuities that may result in signal reflections and increase high frequency radiation. Instead, route traces with two 45-degree bends or smooth arcs when making turns to preserve controlled impedance and minimize emissions. Adhering to such guidance helps maintain signal integrity in analog signal routing, but is more critical in high-speed digital circuits.

Figure 2-12 shows an example for avoiding 90-degree bends on the EMC test boards.

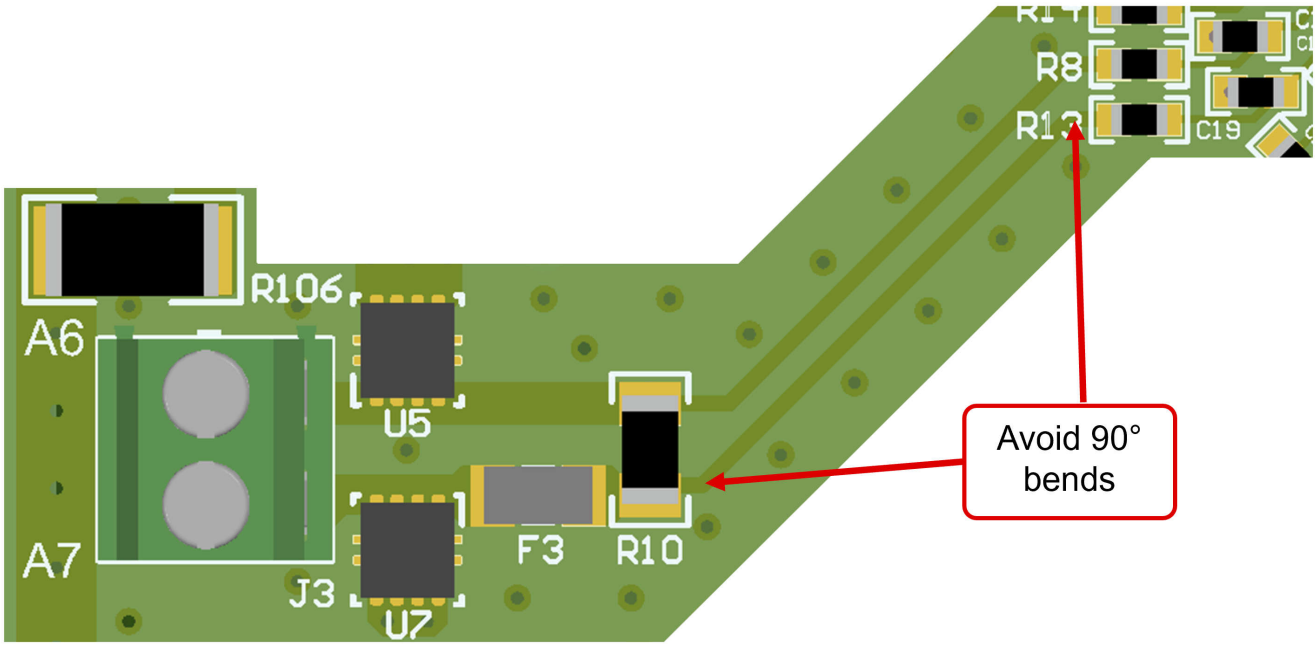

Figure 2-12. Avoiding 90-degree bends in PCB Traces

2.2.4 Using a Guard Ring to Isolate Interference Signals

A guard ring is a continuous conductive trace that encircles the perimeter of a PCB or a specific circuit zone. Connecting the guard ring to the system chassis ground or earth ground acts as a Faraday cage on the PCB level, reducing electromagnetic interference signals both emitted from and received by the circuit board. Adding a guard ring is an effective technique for shielding highly sensitive analog signals or ADCs from nearby noise sources or interference signals. Figure 2-13 shows the side view of guard rings on a typical 4-layer circuit board that are connected together by equally-spaced vias.

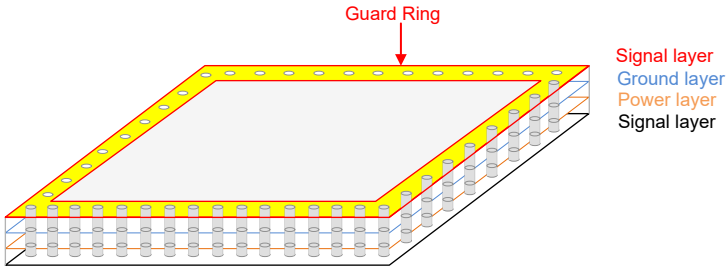

Figure 2-13. Side View of Guard Ring on 4-Layer Circuit Board

The purpose and benefits of using a guard ring include:

- Reducing radiated emissions: The guard ring provides a current return path and confines high-frequency signal currents, reducing unintentional radiation from the board edges.
- Improving immunity for electrostatic discharge, fast transients and surge: Transient signals can enter a circuit through both air and coupling (direct contact, conduction and electromagnetic fields) and affect the function of the circuit. A grounded guard ring helps dissipate the energy away from sensitive circuitry.
- Acting as a ground reference shield: The guard ring on the outer layer of a multi-layer board helps maintain signal integrity and reduce coupling between high-speed and analog sections.

The guidelines to implement a guard ring include:

- Layer placement: Place the guard ring on the top and bottom layer on a 2-layer board or on the outer layers of a 4-layer board. Ensure the ring forms a closed loop for maximum effectiveness. Connect all guard rings together with vias.
- Hole-to-hole spacing between vias: Use vias to tie the guard rings on the top and bottom layer together. Determine the proper hole-to-hole spacing between vias to ensure an effective guard ring by generally following the wavelength limit in Equation 19, where S is the spacing between the vias on the guard ring trace. All signal wavelengths longer than this limit can be effectively shielded.

$$Wavelength\ (L) > \left(\frac{S}{4}\right) \tag{19}$$

- Guard ring trace width: Determine the appropriate trace width of the guard ring. Wider traces enhance guarding effect but consume more space. As a general rule of thumb, the trace width of the guard ring should be equal to 2~3x width of the protected signal trace. Set the trace width of the guard ring to ~5x width of the protected signal trace for low impedance guarding. This guidance provides a robust shielding for critical high-speed or RF traces.
- Guard ring clearance : The 3W rule specifies a space clearance between signal lines, guard traces, and solid ground planes. Maintain the clearance to reduce crosstalk and coupling by a distance equal to 3x width of a single signal trace.
- Chassis ground tie: For enhanced protection, tie the guard ring to chassis ground, protective earth or shield ground to isolate DC ground but still allow high-frequency discharge. This guidance is implemented by high voltage resistors and capacitors on the EMC test board.

Both inner layers on the ADS125H18 EMC test board are designated as ground layers (GND and DGND) for good decoupling and ground current return. The ADS125H18 EMC test board guard ring is included on all layers, and the edge guard on these layers are linked together with vias every 100mil to attenuate emissions of high frequency signals up to 472GHz. Figure 2-14 shows a portion of the EMC test board guard ring:

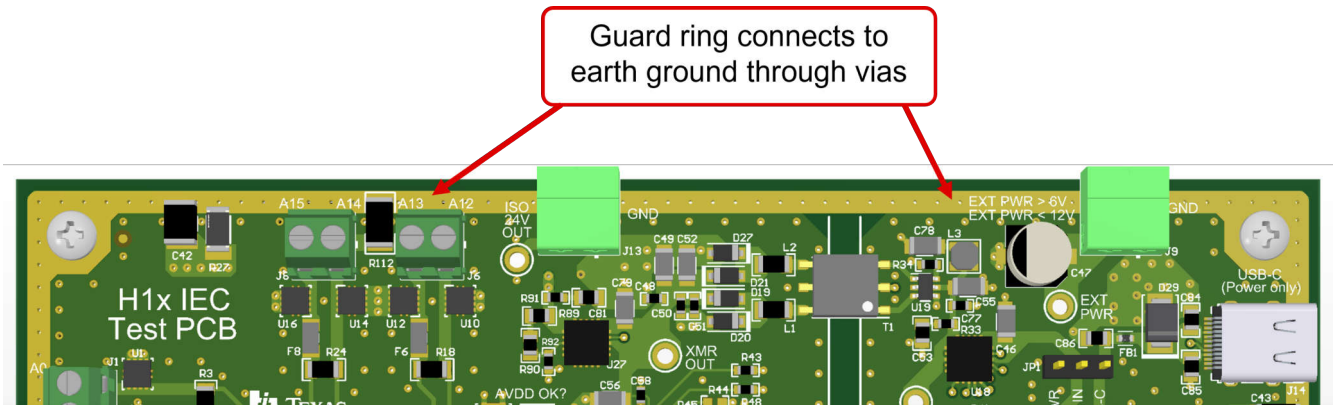

Figure 2-14. EMC Test Board Guard Ring

2.2.5 Decoupling Capacitors

Decoupling capacitors are essential for stabilizing power supplies and reducing high-frequency noise. Place a local decoupling capacitor - typically 0.1µF - as close as possible to each power pin with a short and direct return path to the ground plane. Larger bulk capacitors such as 1µF or 10µF can also be placed in parallel to reduce low-frequency power fluctuations. Place the decoupling capacitors between the power supply and the power pin of the device for the best decoupling effect. Process-level voltage and current signals benefit greatly from clean, locally regulated analog supplies and careful decoupling. The circuit on the left in Figure 2-15 shows an appropriate PCB layout example implemented on the EMC test board for decoupling capacitors on AVDD, while the circuit on the right is an inappropriate PCB layout example that is not designed on the EMC test board.

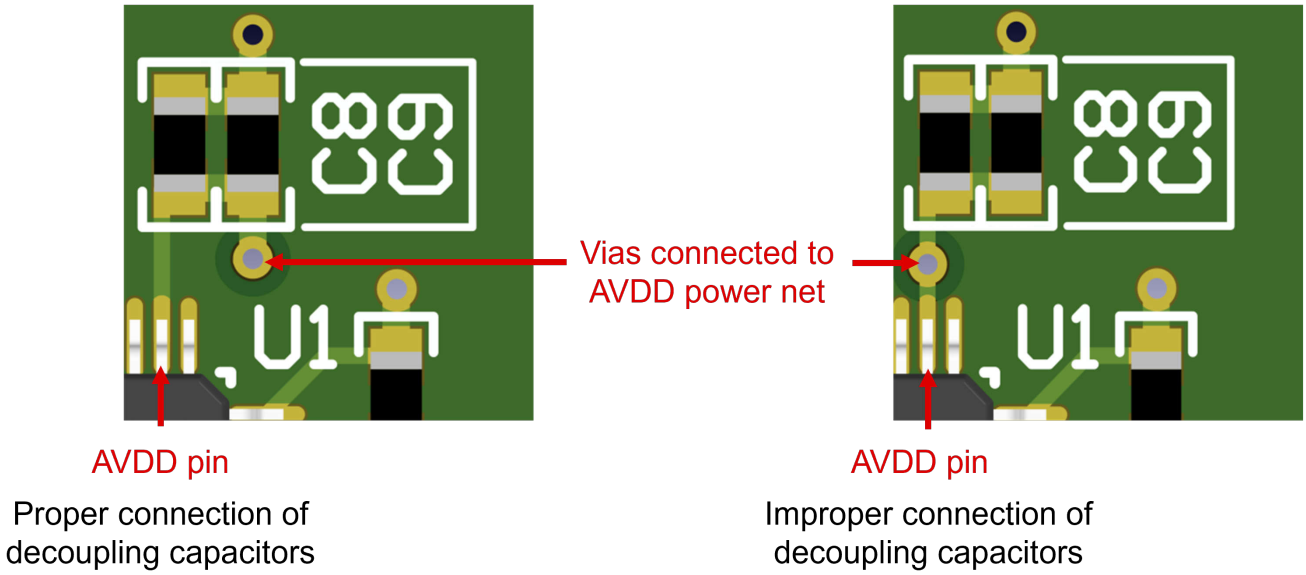

Figure 2-15. Proper (left) and Improper (right) Decoupling Capacitors

2.2.6 Differential Signal Routing

Voltage and current process signals can be differential or single-ended. The EMC test board routes the traces for differential signals closely and symmetrically so that any external interference or noise couples equally into both traces. Therefore, the induced noise signal is a common-mode signal that the ADC rejects within the common-mode rejection ratio (CMRR) specification limits. Avoid placing components and vias between differential traces. Placing components or vias between differential pairs could lead to EMC problems and impedance discontinuities.

Figure 2-16 shows a differential routing example on the EMC test boards:

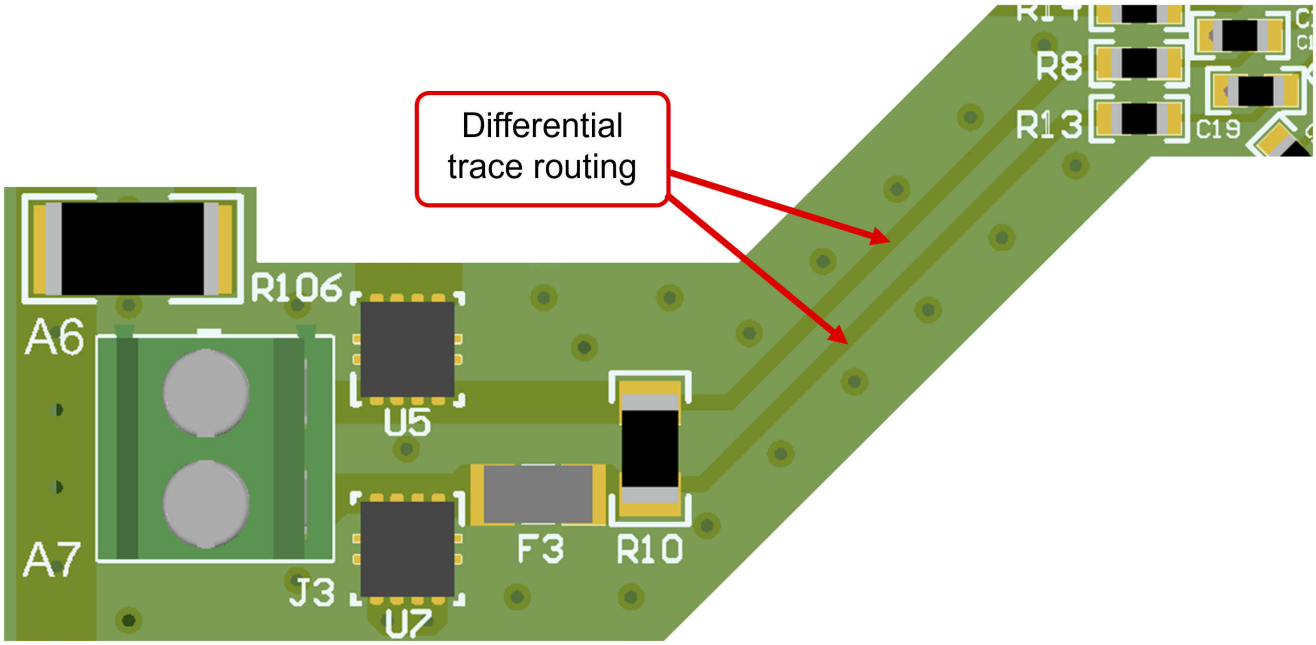

Figure 2-16. Differential Signal Routing

2.2.7 Stitching Vias

Stitching vias can improve signal integrity, reduce impedance and inductance, minimize noise and crosstalk, and also enhance EMI shielding. The ADS125H18 EMC test board employs stitching vias to enhance high speed signal integrity and reliability. The serial clock signal required by many ADCs can be as high as 50MHz. Stitching vias can significantly enhance signal integrity and reliability for high-speed signals by providing a low impedance ground return path, reducing ground ringing and crosstalk. Keep high-speed signals on the same layer as the ADC if possible. Use a single stitching via or stitching via array if a high-speed signal must be routed between different layers. Figure 2-17 shows the side view of a stitching via on a 4-layer circuit board.

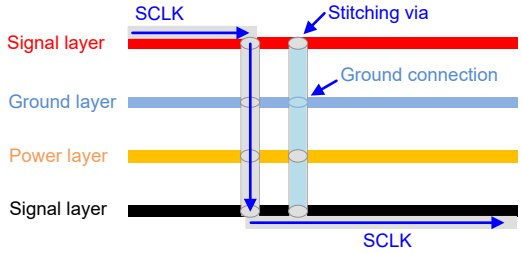

Figure 2-17. Side View of Stitching Via for High-Speed Signal

2.2.8 Layout for Isolation Barrier

Two important isolation barrier considerations in high voltage PCB design are clearance and creepage. Keep the space across the isolation barrier as wide as possible to meet the shortest clearance and creepage requirements and prevent electrical failure. Use rounded or smoothed corners at the edge of PCB board to avoid capacitive coupling between pours and electric charge accumulation. This guideline is important for passing high voltage and high frequency signal tests, such as electrical fast transients and radiated immunity test. Figure 2-18 shows

the isolation barrier design between the ADS125H18 and the PHI controller card, as well as the PCB corner design on the EMC test board.

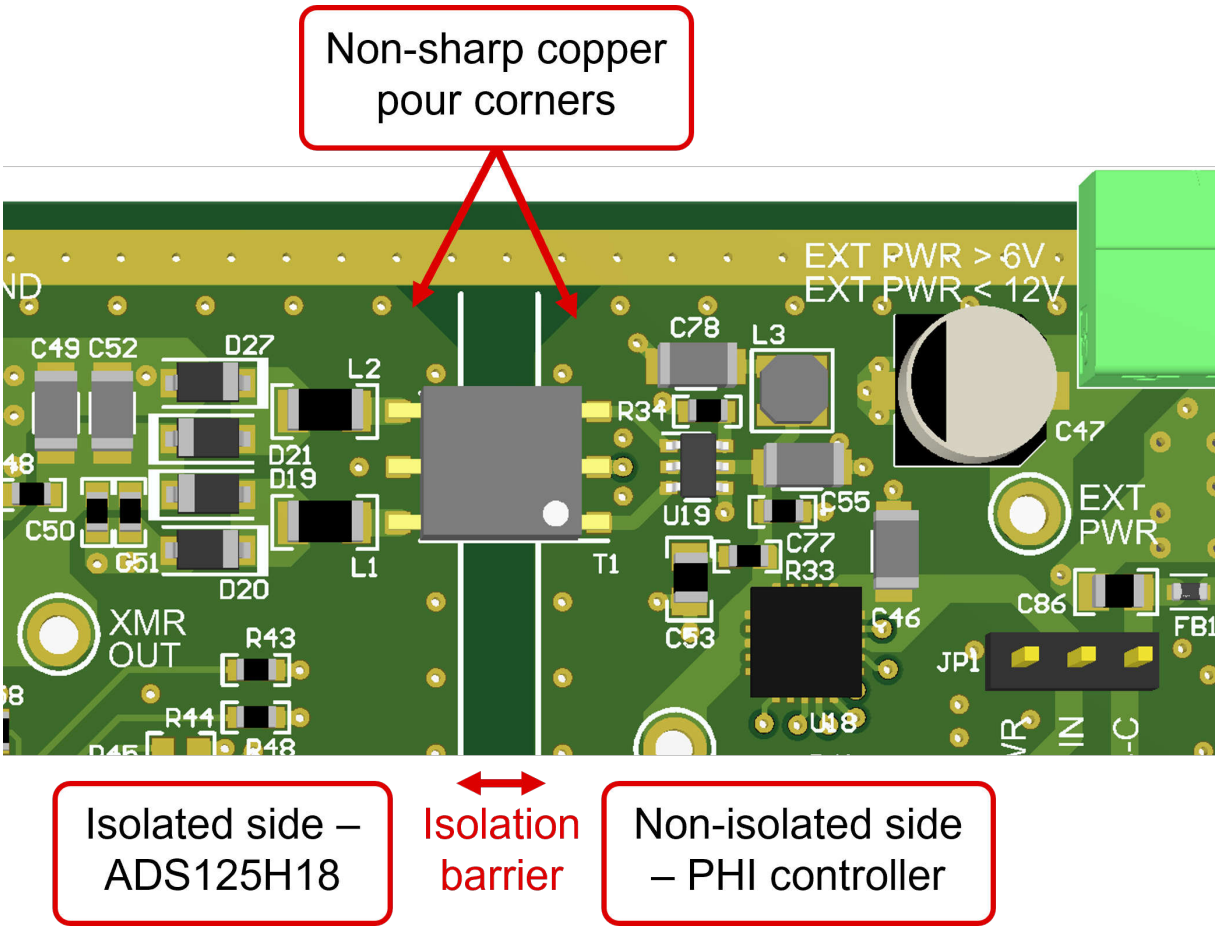

Figure 2-18. Isolation Barrier Layout

2.2.9 Component Placement

Proper component placement is important for precision signal measurement and electromagnetic compatibility design in mixed-signal circuits. Designers must analyze function blocks, signal paths, and connections to optimize each component location. For example, place connectors at the PCB edges, place decoupling capacitors close to the power supply and reference pin of the ADC, and place input differential capacitors as close as possible to the ADC. Separating analog and digital components can help minimize interference or noise from the shared return paths, ensuring signal integrity.

3 EMC Test System, Standards, and Results

This section covers test standard and criteria, test setup and result for each test.

3.1 EMC Test System

Figure 3-1 shows the general setup of the ADS125H18 EMC test board. A software script configures the system parameters including the SPI interface, clock frequency configuration, ADC mode selection, data capture and analysis, data monitoring, and exporting for post-processing. The software and the PHI controller verify the operation of the test system and the equipment under test (EUT) before the EMC test. The system continuously captures and monitors the data during the EMC event and also checks the EUT functionality after the EMC test.

The PHI controller card provides a communication interface between the ADS125H18 EMC test board and the laptop over a USB 2.0 (or higher) interface for digital input and output. The test system uses a battery powered optical transceiver pair between the laptop and the PHI controller card. The optical transceiver pair isolates harsh transient signals from the test environment and provides an additional layer of protection for the user equipment.

Test Hardware

- ADS125H18 EMC test board
- PHI controller card from Texas Instruments
- Optical transceivers with fiber optic cables
- Twisted-pair wire with a 9V battery for voltage measurements or a precision signal for current measurements
- Specific equipment for individual EMC test
- Laptop running Windows® 10 or 11, 64-bit version
- Lab supply or 9V lead battery for floating system power supply

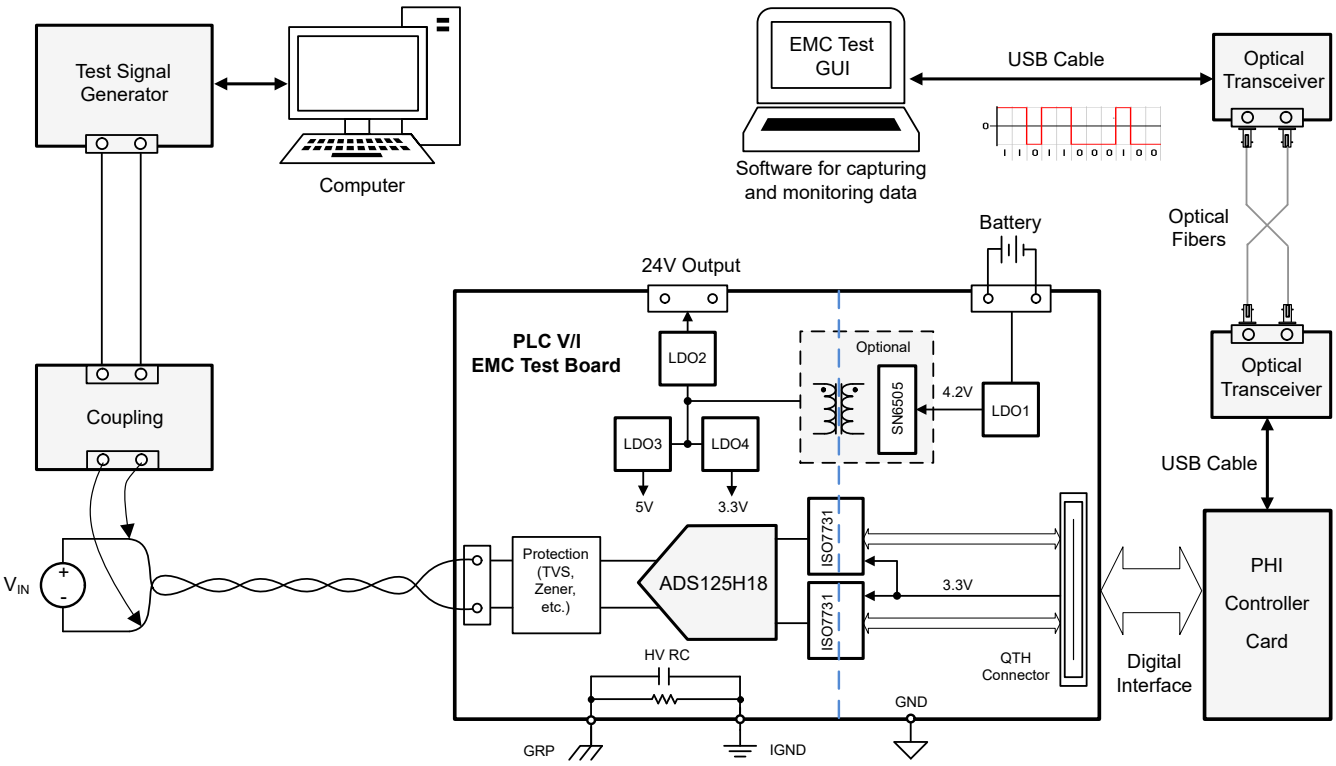

Figure 3-1. General EMC Test Setup

3.2 EMC Test Standards

The ADS125H18 EMC test boards are designed to meet EMC and EMI test standards and criteria for industrial applications. EMC test criteria define the limits and conditions under which an electronic device is tested to verify the device functions properly in its intended environment without causing or being affected by interferences. Table 3-1 shows essential test criteria for product reliability and compliance with regulatory standards. Defining EMC test criteria involves specifying the types of tests (emissions and immunity), the test methods (radiated and conducted), the frequency ranges, and the acceptable performance levels.

Table 3-1. IEC 61000-4-x Test Criteria

Criteria	Description
A	Normal performance within specified limits
B	Temporary performance loss that can recover after disturbance ends
C	Temporary function or performance loss which can recover with user's intervention
D	Permanent function or performance loss due to damage or loss of data

3.3 EMC Test Results

This document describes five IEC 61000-4-x tests. Review detailed information about how the ADS125H18 EMC test board perfomed by clicking on the links in the following list:

- IEC 61000-4-2: Electrostatic Discharge (ESD)
- IEC 61000-4-3: Radiated Immunity (RI)
- IEC 61000-4-4: Electrical Fast Transients (EFT)
- IEC 61000-4-5: Surge Immunity (SI)
- IEC 61000-4-6: Conducted Immunity (CI)

Table 3-2 summarizes the results from all tests for quick reference:

Table 3-2. Summary of ADS125H18 EMC Test Board Results

Test	IEC Standard	Description	Test Conditions	Criterion	Test Result
ESD	IEC 61000-4-2	Contact Discharge (HCP/VCP)	±8kV	A	Pass
			±15kV	A	Pass
		Contact Discharge (shield guard screws)	±4kV	A	Pass
			±6kV	C	USB communication failed
RI	IEC 61000-4-3	20V/m	80MHz -1GHz (Horizontal & Vertical)	A	Pass
				A	Pass
			1GHz -2.7GHz (Horizontal & Vertical)	A	Pass
				A	Pass
EFT	IEC 61000-4-4	Voltage Input	±4kV | 5kHz	A	Pass
			±4kV | 100kHz	A	Pass
		Current Input	±4kV | 5kHz	A	Pass
			±4kV | 100kHz	A	Pass
		DC Port	±4kV | 5kHz	C	USB communication failed
			±4kV | 100kHz	C	USB communication failed
		DC Port	±3kV | 5kHz	A	Pass
			±3kV | 100kHz	A	Pass
SI[(1)]	IEC 61000-4-5	Voltage Input	500V	B	Pass
			1000V	B	Pass
		Current Input	500V	B	Pass
			1000V	B	Pass
		DC input	500V	B	Pass
			1000V	B	Pass

Table 3-2. Summary of ADS125H18 EMC Test Board Results (continued)

Test	IEC Standard	Description	Test Conditions	Criterion	Test Result
CI	IEC 61000-4-6	Voltage Input	20V/m (Level >3) from 150kHz-80MHz	A	Pass
		Current Input		A	Pass
		DC Port		A	Pass
		Earth Line		A	Pass

(1) Line-to-ground (2Ω source impedance + 40Ω from coupling network) and line-to-line (2Ω source impedance on DC input)

3.3.1 Electrostatic Discharge (ESD)

The IEC 61000-4-2 standard specifies the details for the ESD test including the test criteria and setup requirements. The IEC 61000-4-2 test determines the EUT immunity to external ESD events during operation. Figure 3-2 shows a diagram of the setup and connection for the ESD test. A 0.8m high wood table stands on the GRP. A 1.6m × 0.8m horizontal coupling plane (HCP) is placed on the table. The EUT is tested and isolated on a 0.5mm thick insulating mat that is placed on top of the HCP. The EUT is placed on the insulating mat 0.1m away from a 0.5m × 0.5m vertical coupling plane (VCP).

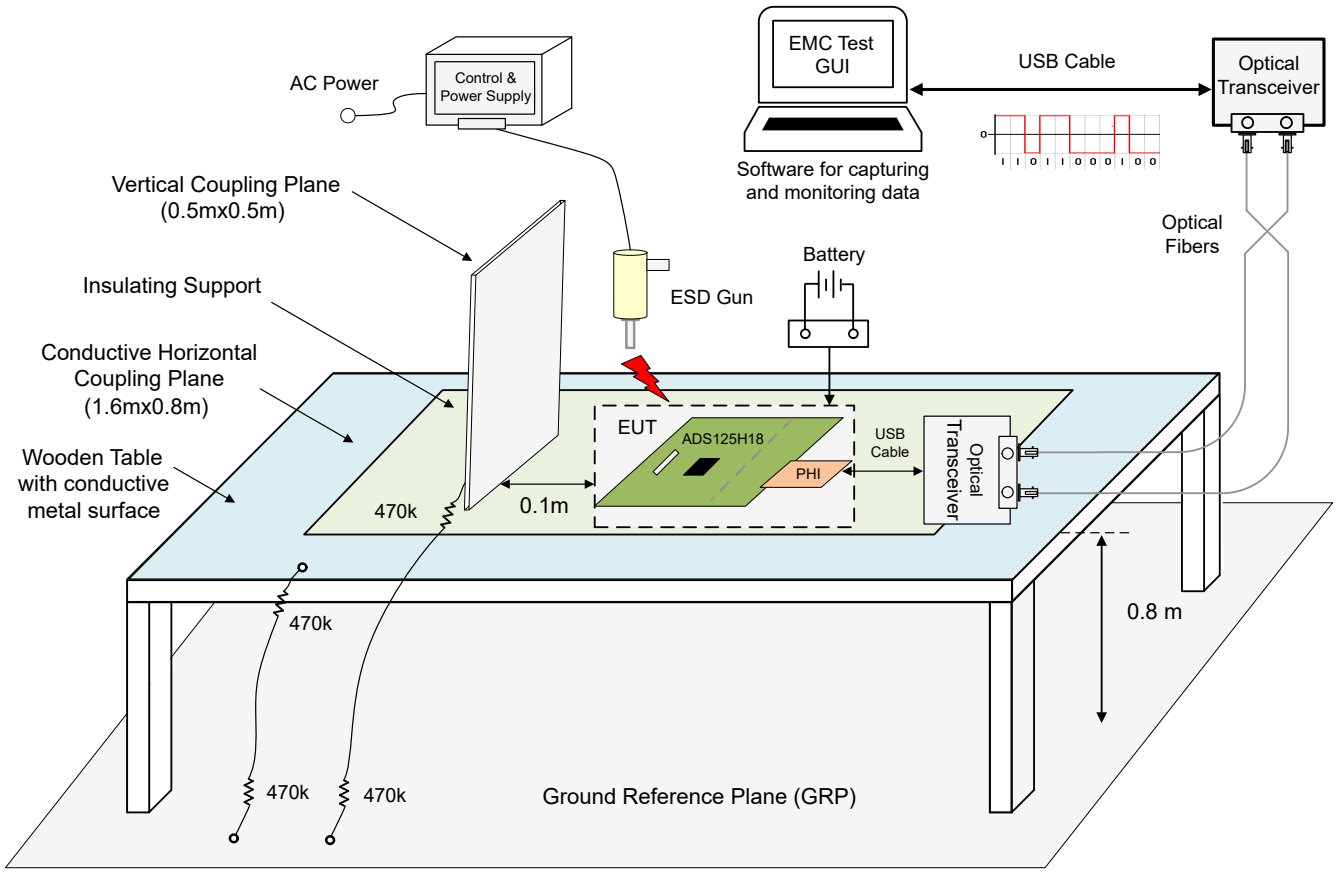

Figure 3-2. Diagram of Laboratory Setup for ESD Test

There are two types of ESD tests: contact discharge and air discharge. The contact discharge test is the most aggressive direct discharge test where the tip of the ESD gun directly contacts conductive screws of the input terminal block or shield guard screws on the ADS125H18 test board. Air discharge tests are executed three different ways: direct air gap discharge, indirect discharge to the horizontal coupling plane (HCP), and indirect discharge to the vertical coupling plane (VCP). The air gap discharge test places the ESD gun tip near the input terminal block insulating surface on the EMC test board. The indirect discharge tests applies the ESD signal into the HCP or VCP, which represents an ESD strike onto the equipment rack where the design is mounted.

Table 3-3 specifies the IEC 61000-4-2 test levels:

Table 3-3. ESD Test Levels

Contact Discharge		Air Discharge	
Level	**Test Voltage (kV)**	**Level**	**Test Voltage (kV)**
1	2	1	2
2	4	2	4
3	6	3	8
4	8	4	15
x	Special	x	Special

Figure 3-3 shows a photograph of the actual setup for the ESD test on the ADS125H18 EMC test board shield guard screws.

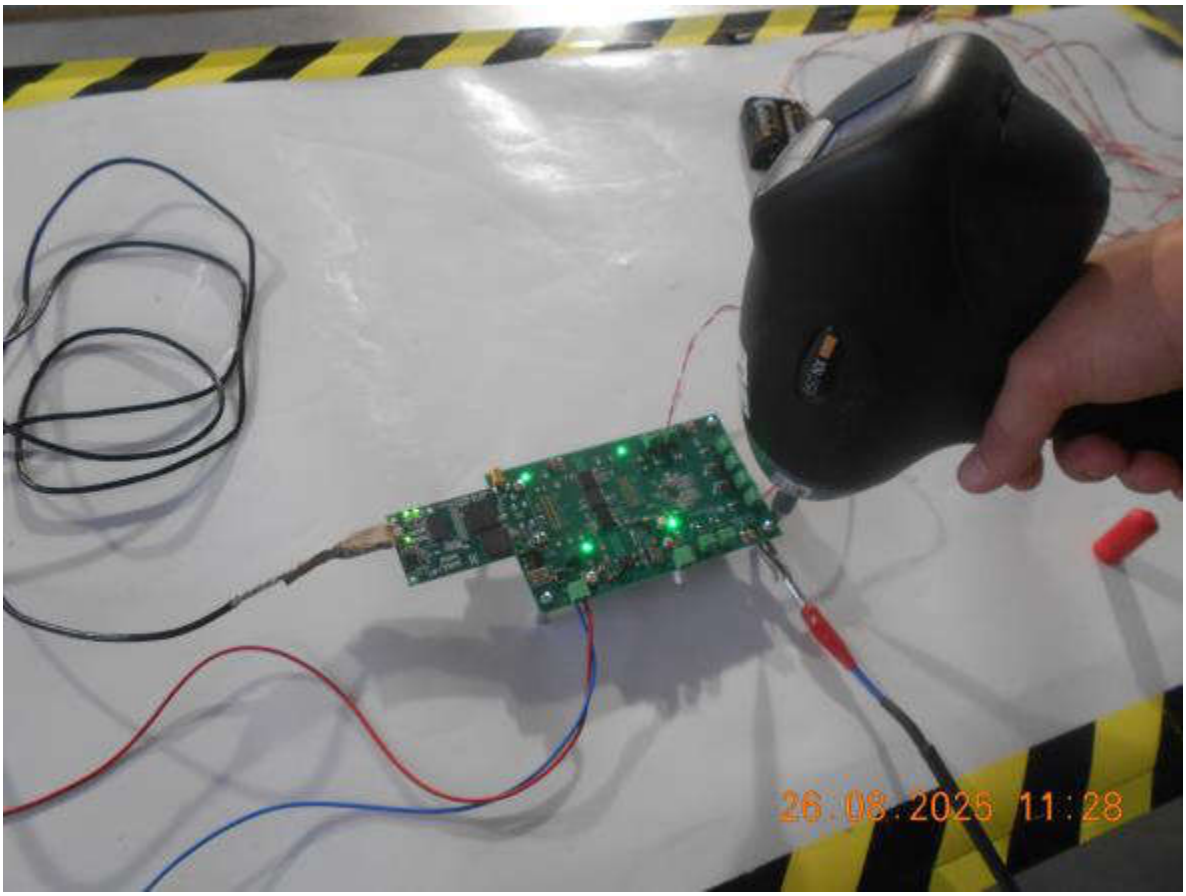

Figure 3-3. Laboratory Setup for ESD Test

For the ESD test, the EUT is tested with at least 100 discharges at each rating into the screws and 10 discharges into the coupling plane. Figure 3-4 shows the ADS125H18 EMC test board output data during the ESD test when the ADC measures the voltage input (left) and the current input (right). Both graphs show that the ADS125H18 was not significantly affected by the ESD test signals. Therefore, the ADS125H18 EMC test board passed the ESD test with criteria A.

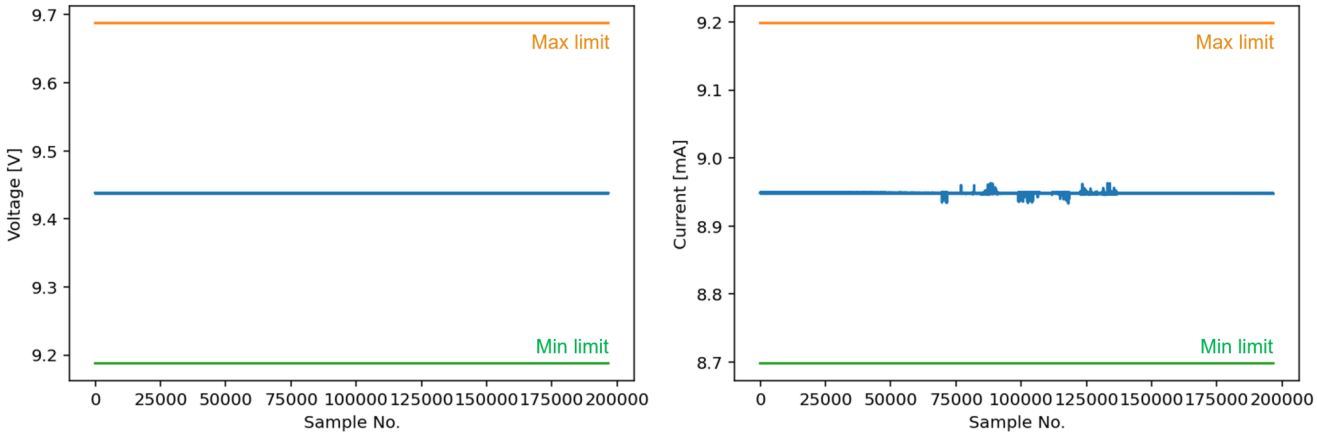

Figure 3-4. Voltage (Left) and Current (Right) Measurements Captured During ESD Test

Table 3-4 lists the results of the ESD tests. The test result is the same for both the voltage and current channels on the EMC test board.

Table 3-4. ESD Test Results using ADS125H18 EMC Test Board

Test	IEC Standard	Type	Test Voltage	Criterion	Test Result
ESD	IEC 61000-4-2	Contact Discharge (HCP/VCP)	±8kV	A	Pass
			±15kV	A	Pass
		Contact Discharge (shield guard screws)	±4kV	A	Pass
			±6kV	C	USB communication failed

3.3.2 Radiated Immunity (RI)

The IEC 61000-4-3 standard specifies the details for the RI test including test criteria and setup requirements. The IEC61000-4-3 test determines the EUT immunity to external electromagnetic radiation during operation. The test is performed in an anechoic chamber and the EUT is placed on a nonconductive table that is 0.8m tall. The test distance between the EUT and the antenna is 3m. The EUT is exposed to both horizontal and vertical field polarities at each rating. The RF test signal is swept from 80MHz to 1GHz, and from 1GHz to 2.7GHz with a disturbance signal of 80% amplitude modulated with a 1kHz sinusoidal signal. The field strength is 10V/m and 20V/m for each frequency range. The conversion data is captured from the EUT by the PHI controller card and sent to the laptop running the software script outside the chamber through the fully isolated optical fiber cables.

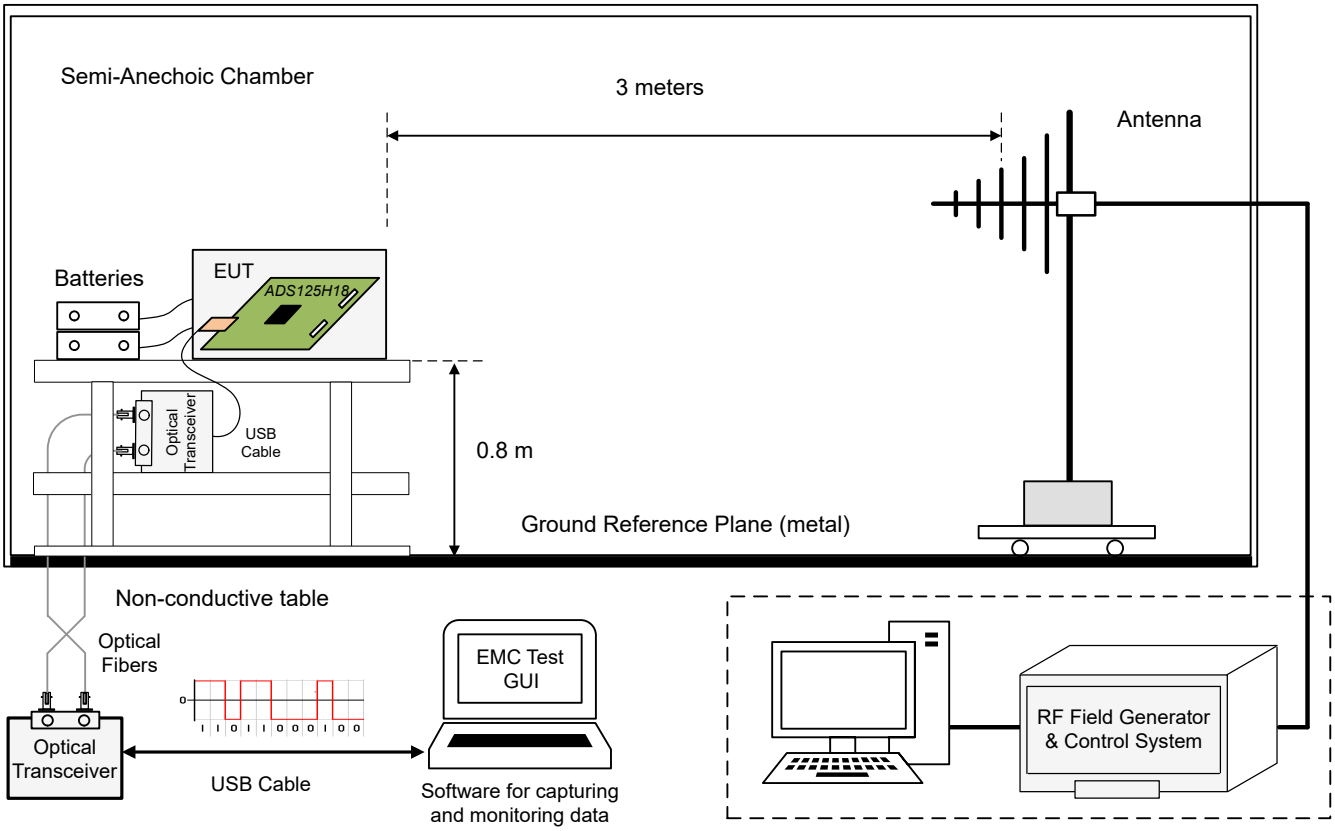

Figure 3-5. Diagram of Laboratory Setup for RI Test

Table 3-5 specifies the IEC 61000-4-3 test levels.

Table 3-5. RI Test Levels

Level	Field Strength of Test Signal (V/m)
1	1
2	3
3	10
4	30
x	Special level that can be above, below or between the other levels. This level can be specified in product standard.

Figure 3-6 shows the actual setup for the RI test on the ADS124S08 EMC test board.

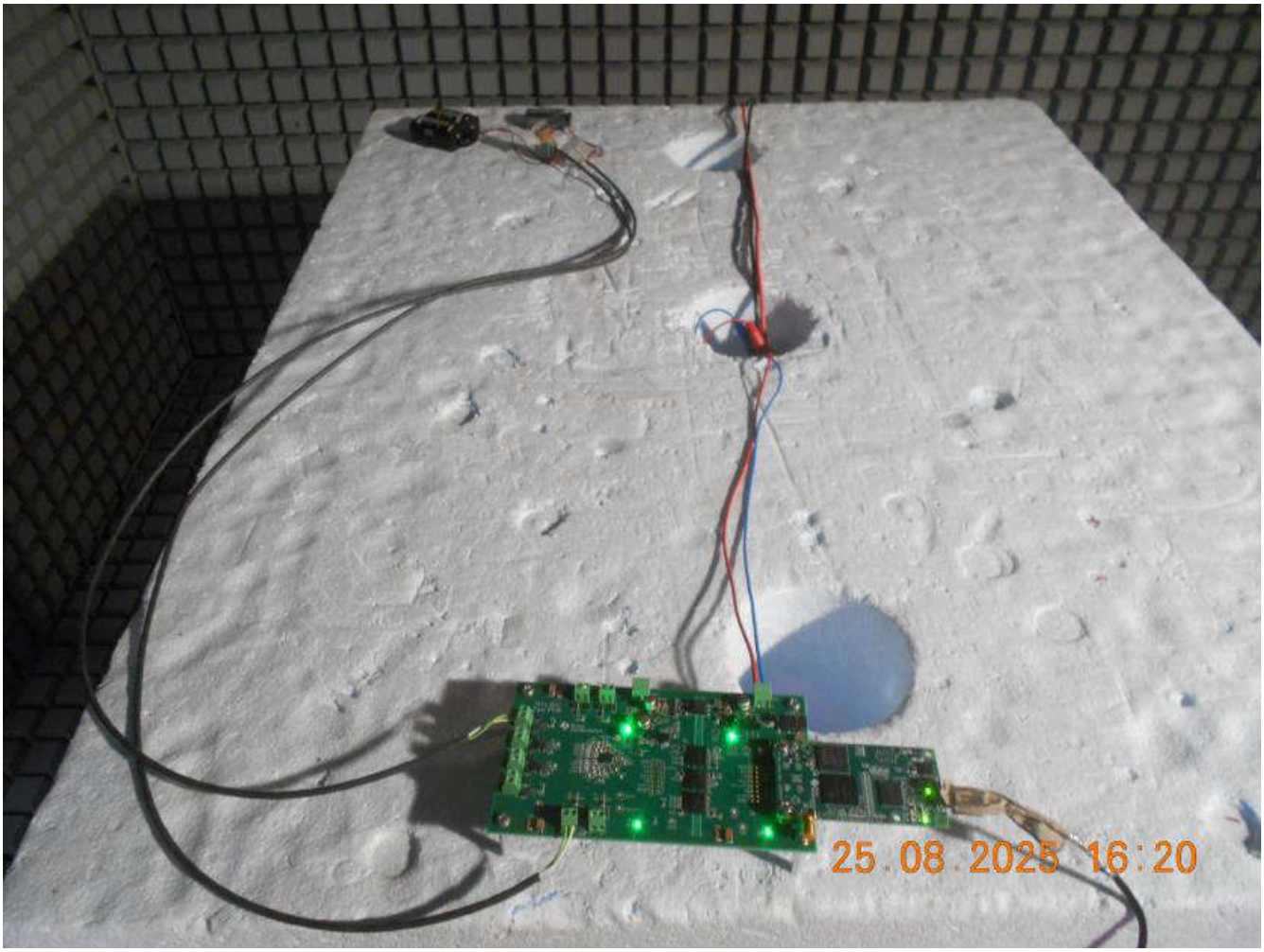

Figure 3-6. Laboratory Setup for RI Test

Figure 3-7 shows the ADS125H18 EMC test board output data during the RI test when the ADC measures the voltage input (left) and the current input (right). These graphs reveal that the interference signals did not affect the ADS125H18. Therefore, the ADS125H18 EMC test board passed the RI test with criteria A.

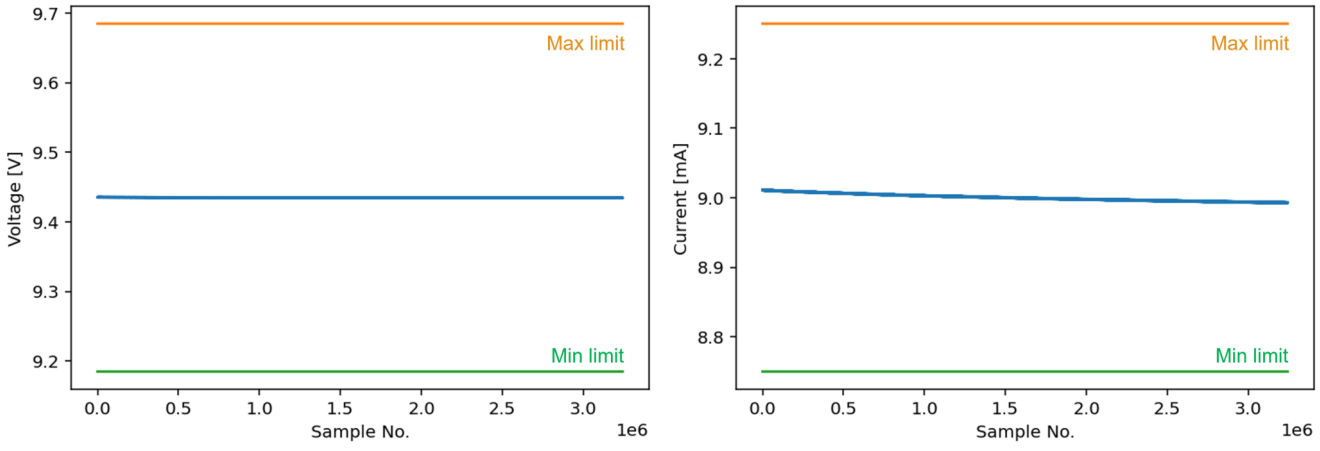

Figure 3-7. Voltage (Left) and Current (Right) Measurements Captured during RI Test

Table 3-6 shows the results of the RI test. The test result is the same for both the voltage and current channels on the EMC test board.

Table 3-6. RI Test Results using ADS125H18 EMC Test Board

Test	IEC Standard	Test Signal			Criterion	Test Result
		Field Strength	Frequency	Antenna Polarization		
RI	IEC 61000-4-3	20V/m	80MHz -1GHz	Horizontal	A	Pass
				Vertical	A	Pass
			1GHz -2.7GHz	Horizontal	A	Pass
				Vertical	A	Pass

3.3.3 Electrical Fast Transients (EFT)

The IEC 61000-4-4 standard specifies the details for the EFT test including test criteria and setup requirements. The IEC61000-4-4 test determines EUT immunity to an external burst of transient signals with short duration and fast rise time during operation. The standard defines four test voltage levels with two repetition frequencies for signal and control ports: 0.25kV, 0.5kV, 1kV and 2kV at 5kHz and 100kHz repetition frequency. Each test also requires positive and negative polarity discharge. The ADS125H18 EMC test board was tested at the standard 1kV and 2kV levels, as well as a more extreme 4kV level. The ADS125H18 EMC test board was tested at both 5kHz and 100kHz frequencies. The EFT transient burst consists of 75 fast pulses followed by a break interval. One pulse occurs every 15ms for 5kHz and 0.75ms for 100 kHz, with bursts repeated every 300ms. Each individual burst pulse is a double exponential waveform with a rise time of 5ns and a total pulse duration of 50ns. The total test time for each test is approximately one minute.

Figure 3-8 shows a setup and connection diagram for the EFT immunity test. In this setup, the EFT signal is applied to the analog input of the ADS125H18 EMC test board by running 2m of twisted pair input wires through a 1m length standard capacitive EFT clamp. All the cables in the test are placed on insulation support materials to keep them isolated from the GRP. The EUT is placed on top of the GRP and isolated from the GRP by a 0.1m insulated platform.

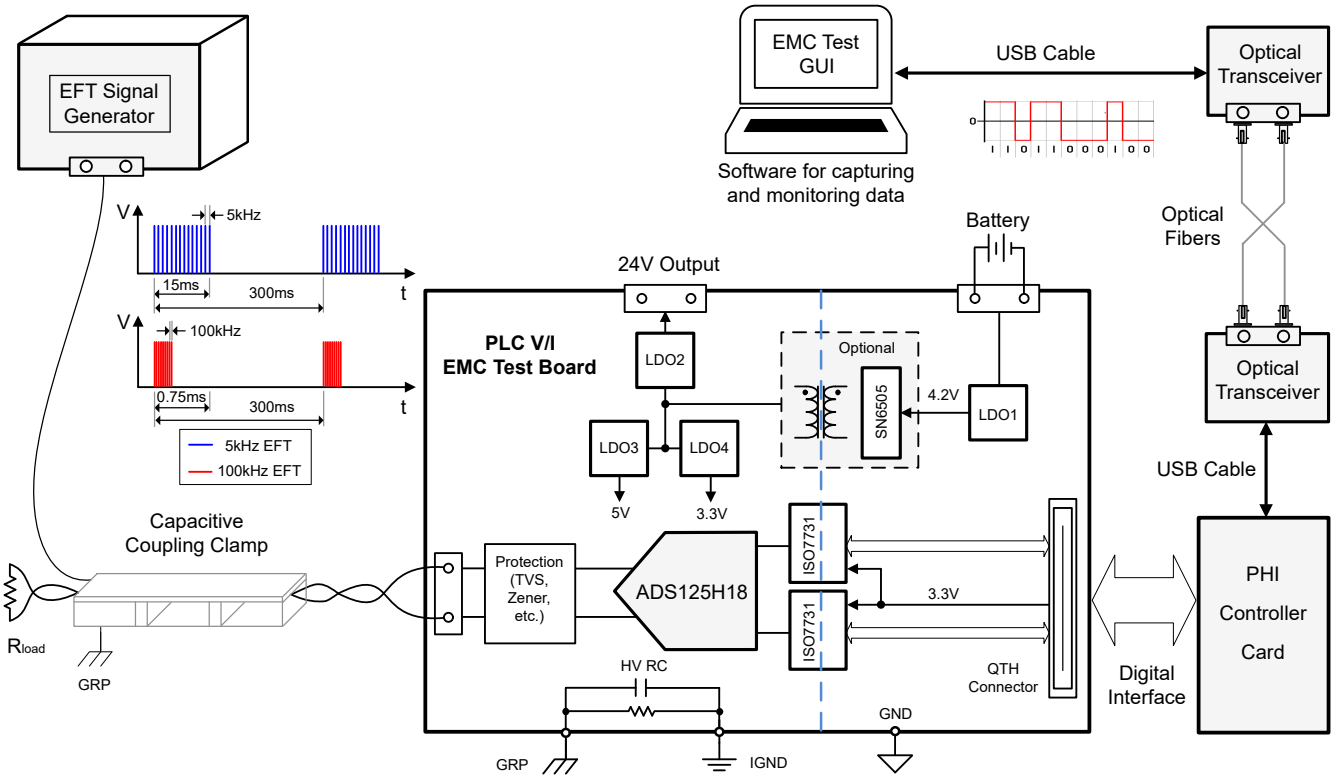

Figure 3-8. Diagram of Laboratory Setup for EFT Test

Table 3-7 specifies the IEC 61000-4-4 test levels:

Table 3-7. EFT Test Levels

Level	On Power Supply Port			On I/O, Signal, Data, and Control Lines		
	Open-Circuit Voltage (kV)	Short-Circuit Current (A)	Repetition Rate (kHz)	Open-Circuit Voltage (kV)	Short-Circuit Current (A)	Repetition Rate (kHz)
1	0.5	10	5 or 100	0.25	5	5 or 100
2	1	20	5 or 100	0.5	10	5 or 100
3	2	40	5 or 100	1	20	5 or 100
4	4	80	5 or 100	2	40	5 or 100
x	Special level that can be above, below or between the other levels. This level can be specified in product standard.					

Figure 3-9 shows the actual setup for the EFT test on the ADS125H18 EMC test board.

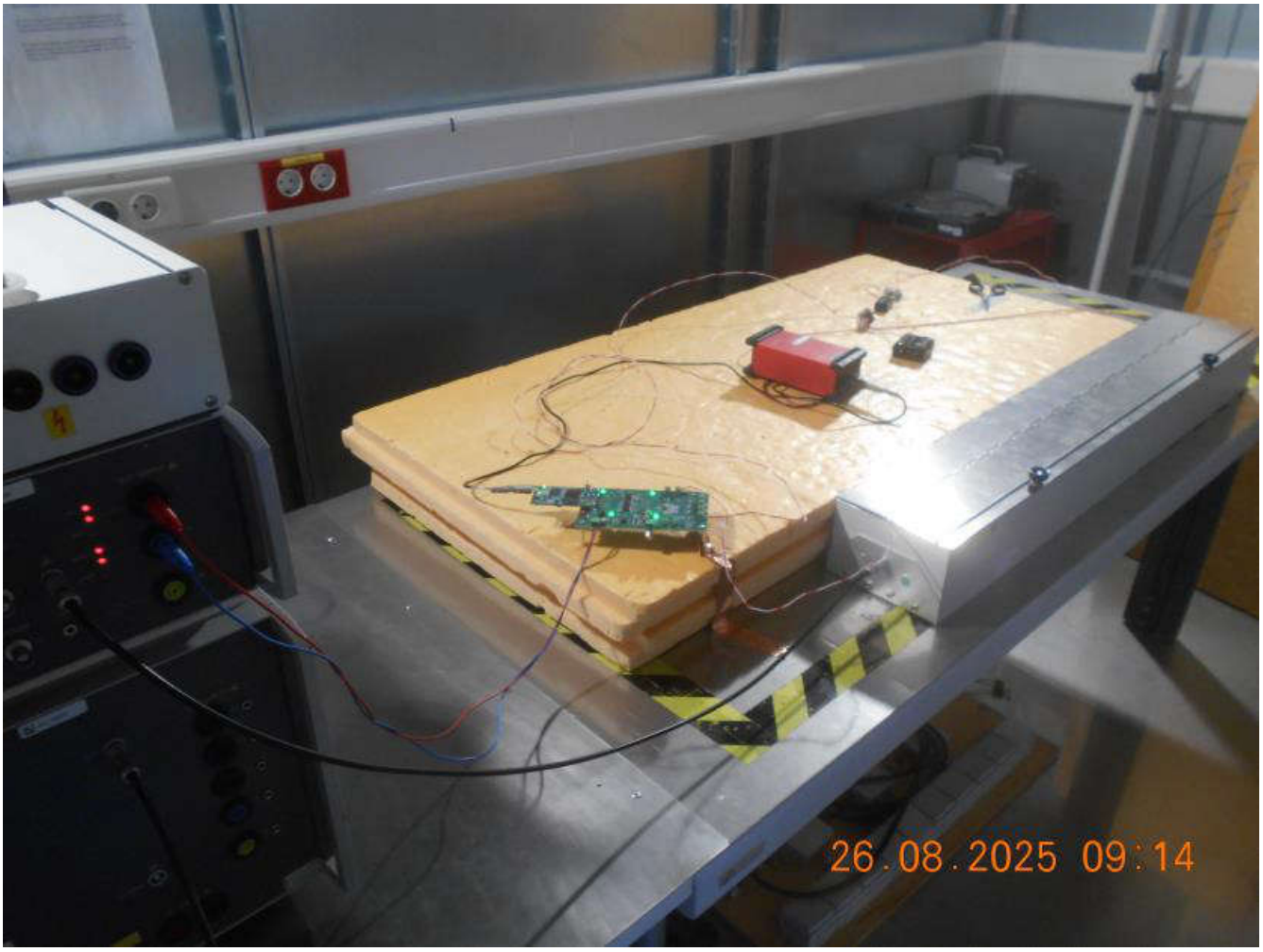

Figure 3-9. Laboratory Setup for EFT Test

Figure 3-10 shows the ADS125H18 EMC test board output data during the EFT test when the ADC measures the voltage input (left) and the current input (right). The plots show the ADS125H18 is affected by the EFT signals leading to a small temporary performance loss. However, this performance loss is within the specified limits. Therefore, the ADS125H18 EMC test board passed the EFT test with criteria A.

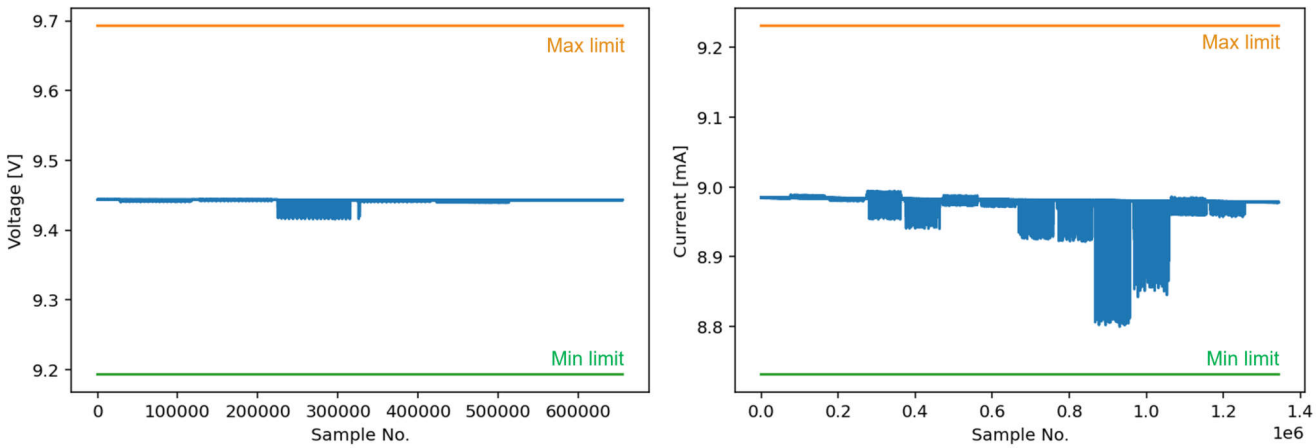

Figure 3-10. Voltage (Left) and Current (Right) Measurements Captured During EFT Test

Table 3-8 shows the results of the EFT test. The test result is the same for both the voltage and current channels on the EMC test board.

Table 3-8. EFT Test Results using ADS125H18 EMC Test Board

Test	IEC Standard	Configuration	Test Signal		Criterion	Test Result
			Voltage	Frequency		
EFT	IEC 61000-4-4	Voltage Input	±4kV	5kHz	A	Pass
			±4kV	100kHz	A	Pass
		Current Input	±4kV	5kHz	A	Pass
			±4kV	100kHz	A	Pass
		DC Port	±4kV	5kHz	C	USB communication failed
			±4kV	100kHz	C	USB communication failed
		DC Port	±3kV	5kHz	A	Pass
			±3kV	100kHz	A	Pass

3.3.4 Surge Immunity (SI)

The IEC 61000-4-5 standard specifies the details for the SI test including test criteria and setup requirements. The setup includes the test equipment and procedures for performing surge testing at a specific source impedance and coupling mode (line-to-line or line-to-ground). The IEC61000-4-5 test determines the EUT immunity to external high energy surges on both power and data lines. These energy surges can be caused by power system switching, load changes and short circuit faults, or direct or indirect lighting strikes. The IEC 61000-4-5 specifies two types of combination wave generators (CWGs). The 10µs / 700µs CWG is specifically used to test the ports of symmetrical telecommunication lines. The 1.2µs / 50µs CWG is used for all other cases. The surge for all other cases combines a 1.2µs / 50µs (1.2µs rising time with 50µs pulse width) open-circuit voltage waveform and 8µs / 20µs (8µs rising time with 20µs pulse width) short-circuit current waveform. The EUT is subject to two positive and two negative surges at each rating. The surge is repeated at least once per minute. A coupling/decoupling network (CDN) is required by the surge test. The IEC 61000-4-5 defines the impedance and capacitance used in the coupling network in different cases. The EUT is tested with the surge through a CDN with a 0.5µF capacitor and a twisted cable.

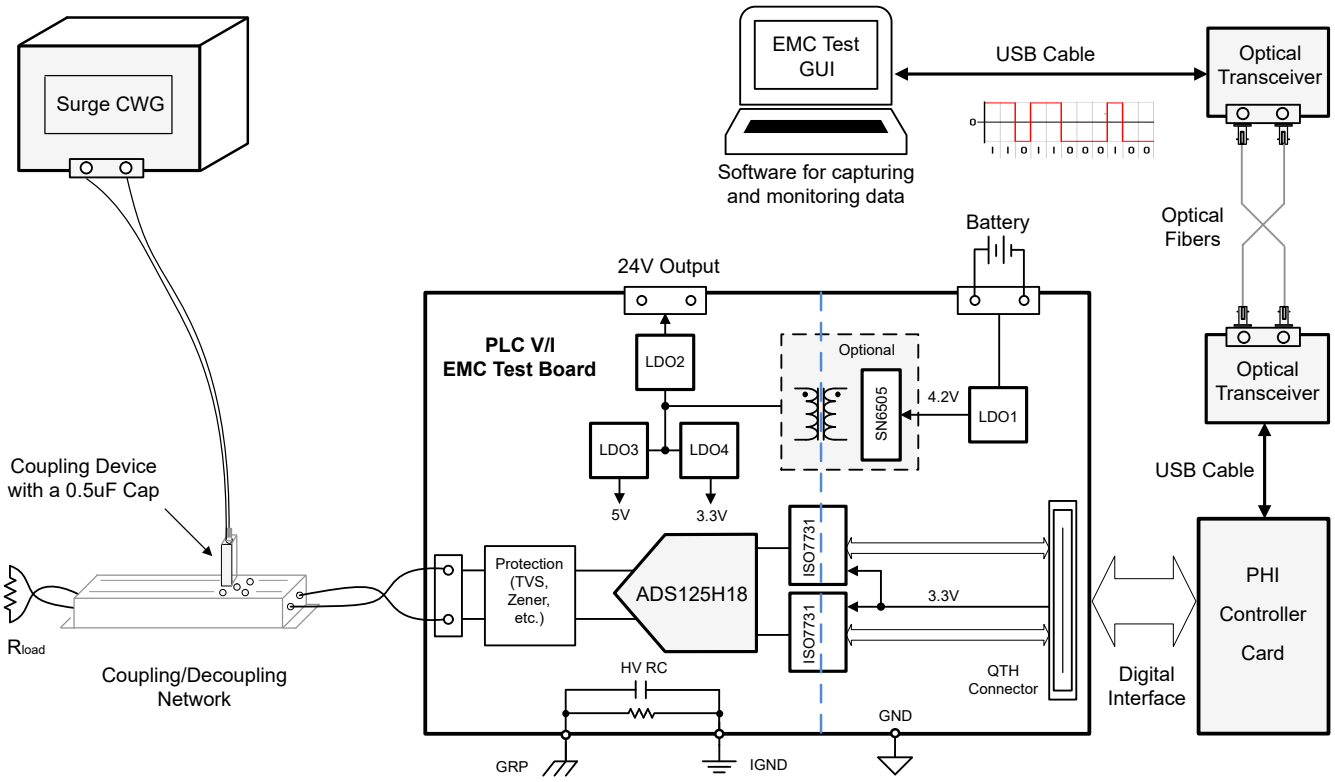

Figure 3-11. Diagram of Laboratory Setup for SI Test

Table 3-9 specifies the IEC 61000-4-5 test levels:

Table 3-9. SI Test Levels

Level	Open-Circuit Test Voltage ±10% (kV)
1	0.5
2	1.0
3	2.0
4	4.0
X	Special level that can be above, below or between the other levels. This level can be specified in product standard.

The surge generator uses a 2Ω output impedance to model the source impedance of a low voltage power supply and the inherent source impedance of the waveform generator. An additional series resistance may be needed between the EUT and the surge generator based on the power and data line test requirements. The surge

current is determined by the surge voltage level and the total impedance (Req), where Req is the combination of the surge generator output impedance and the additional series resistance. The selection of the impedance depends on the equipment type and test requirements.

Table 3-10 shows the surge current levels for different surge voltages and impedances:

Table 3-10. Current Levels for each Surge Test Voltage and Impedance

Level	1	2	3	4
Voltage (V)	**500**	**1000**	**2000**	**4000**
Req = 42Ω	12A	24A	48A	96A
Req = 12Ω	42A	84A	167A	334A
Req = 2Ω	250A	500A	1000A	2000A

Figure 3-12 shows the actual setup for the SI test on the ADS125H18 EMC test board.

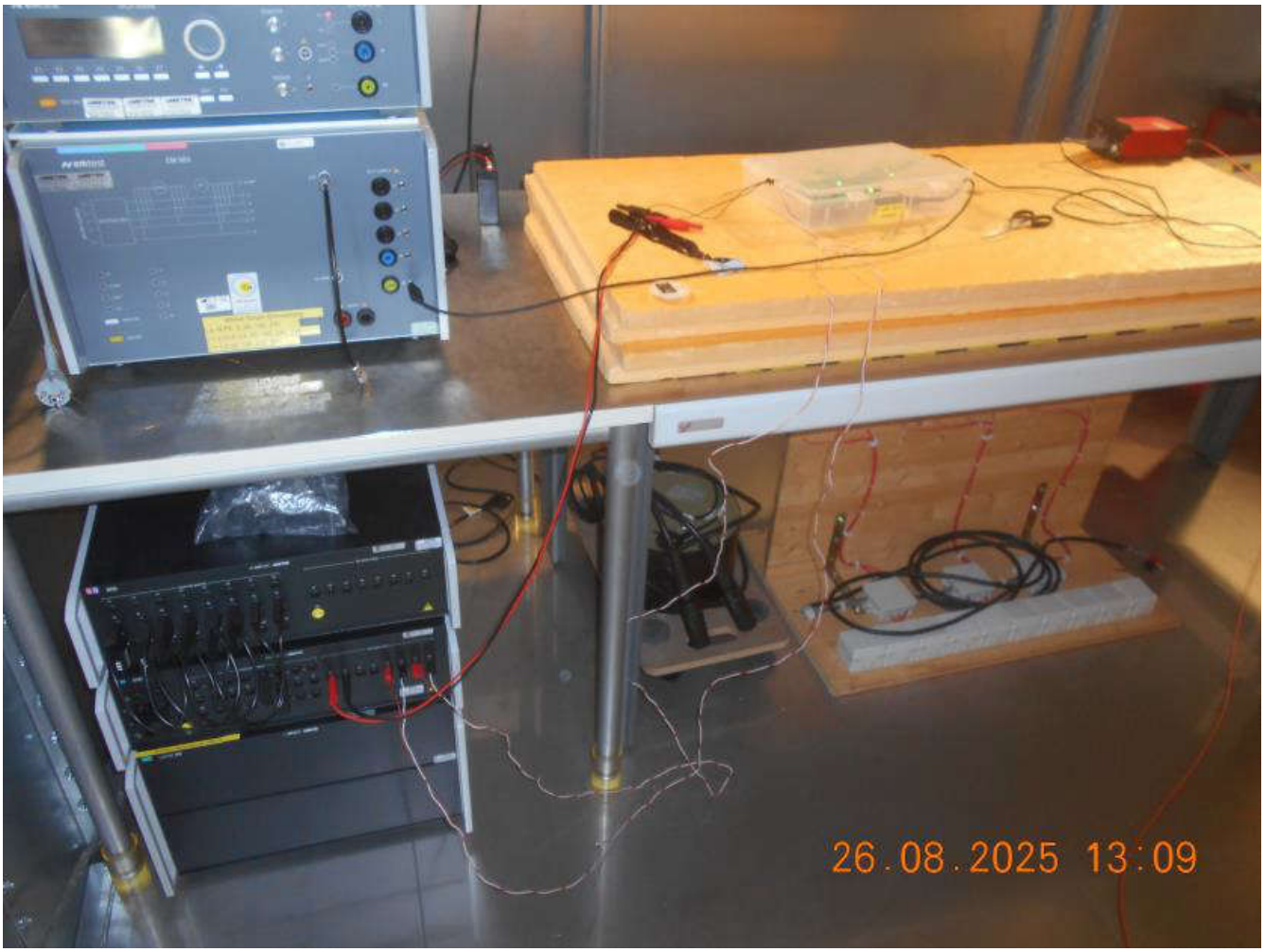

Figure 3-12. Laboratory Setup for SI Test

Figure 3-13 shows the ADS125H18 EMC test board output data during the SI test (±1kV, line-to-line, 42Ω) when the ADC measures the voltage input (left) and the current input (right). The plots show that the surge signals affected the ADS125H18 output resulting in large spikes and a temporary performance loss during the test. However, the device recovered without any intervention after the disturbance stopped. Therefore, the ADS125H18 EMC test board passed the SI test with criteria B.

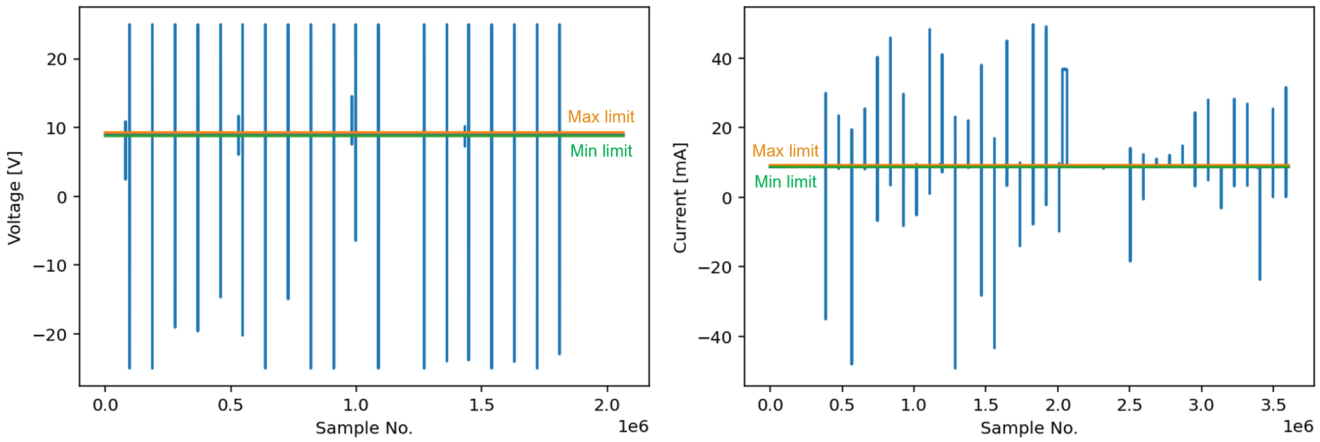

Figure 3-13. Voltage (Left) and Current (Right) Measurements Captured During SI Test

Table 3-11 shows the results of the SI test. The test result is the same for both the voltage and current channels on the EMC test board.

Table 3-11. SI Test Results using ADS125H18 EMC Test Board

Test	Standard	Type and Impedance	Configuration	Test Voltage	Criterion	Test Result
SI	IEC 61000-4-5	Line-to-ground (2Ω source impedance + 40Ω from coupling network) and line-to-line (2Ω source impedance on DC input)	Voltage Input	500V	B	Pass
				1000V	B	Pass
			Current Input	500V	B	Pass
				1000V	B	Pass
			DC Input	500V	B	Pass
				1000V	B	Pass

3.3.5 Conducted Immunity (CI)

The IEC 61000-4-6 standard specifies the details for the CI test including test criteria and setup requirements. The IEC61000-4-6 test determines the EUT immunity to external conducted electromagnetic disturbances during operation. Figure 3-14 shows that the test signal is generated from an RF signal generator and an RF power amplifier that is used to amplify the test signal to a specified level. The test signal is injected to the EMC test board input with an injection probe. Spectrum analyzer 1 is used to monitor the output of the power amplifier, while spectrum analyzer 2 is used to monitor and verify the injected signal. The signal frequency is swept from 150kHz to 80MHz with a disturbance signal of 80% amplitude that is modulated with a 1kHz sinusoidal signal. The EUT should be placed at a specified height (10cm) above the ground plane

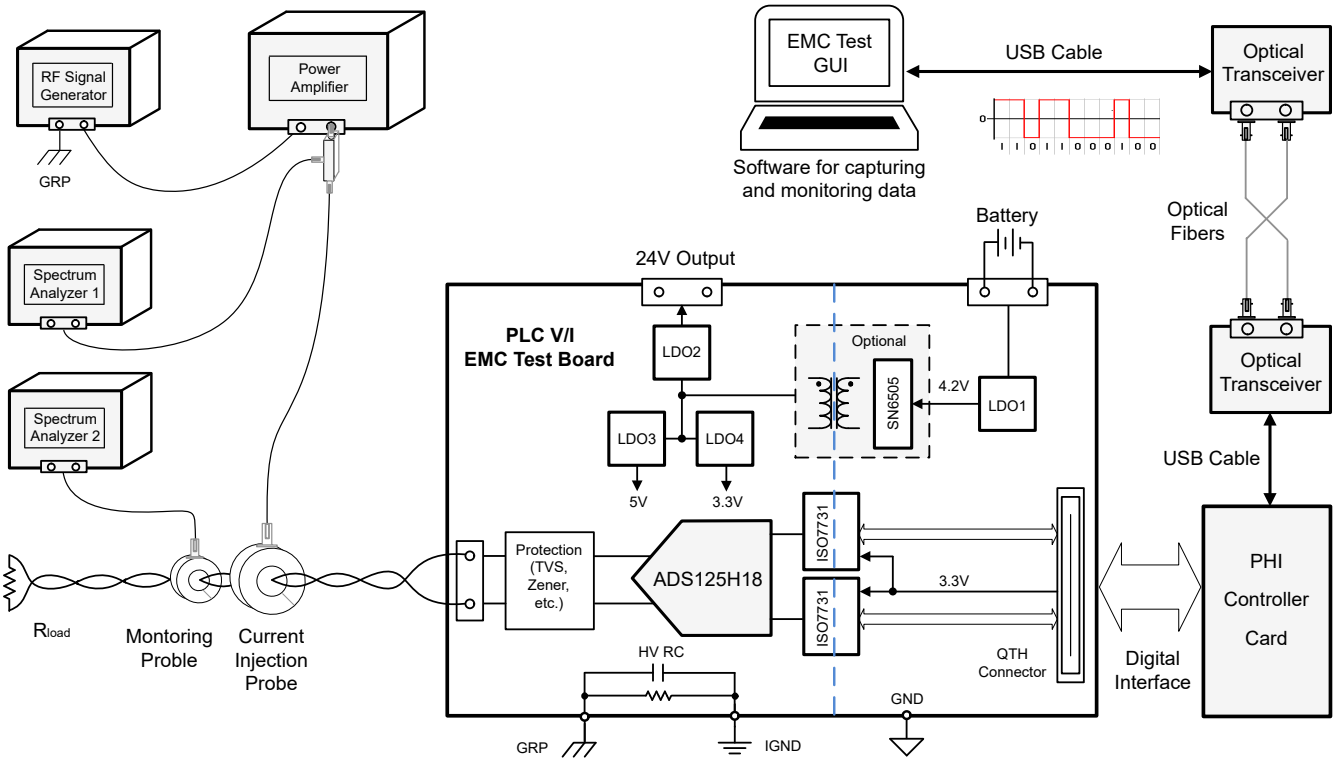

Figure 3-14. Diagram of Laboratory Setup for CI Test

Table 3-12 specifies the IEC 61000-4-6 test levels.

Table 3-12. CI Test Levels

Level	Field Strength of Test Signal	
	V0 (10V/m)	V0 (dBµV)
1	1	120
2	3	129.5
3	10	140
x	Special level that can be above, below or between the other levels. This level can be specified in product standard.	

Figure 3-15 shows the actual setup for the CI test on the ADS125H18 EMC test board.

Figure 3-15. Laboratory Setup for CI Test

Figure 3-16 shows the ADS125H18 EMC test board output data during the CI test when the ADC measures the voltage input (left) and the current input (right). The plots show that the test signals do not affect the ADS125H18 ADC when the test signal frequency sweeps from 150kHz to 80MHz. This test was also repeated coupling the interference signals into the DC port and the earth line. In all cases, the ADS125H18 EMC test board passed the CI test with criteria A.

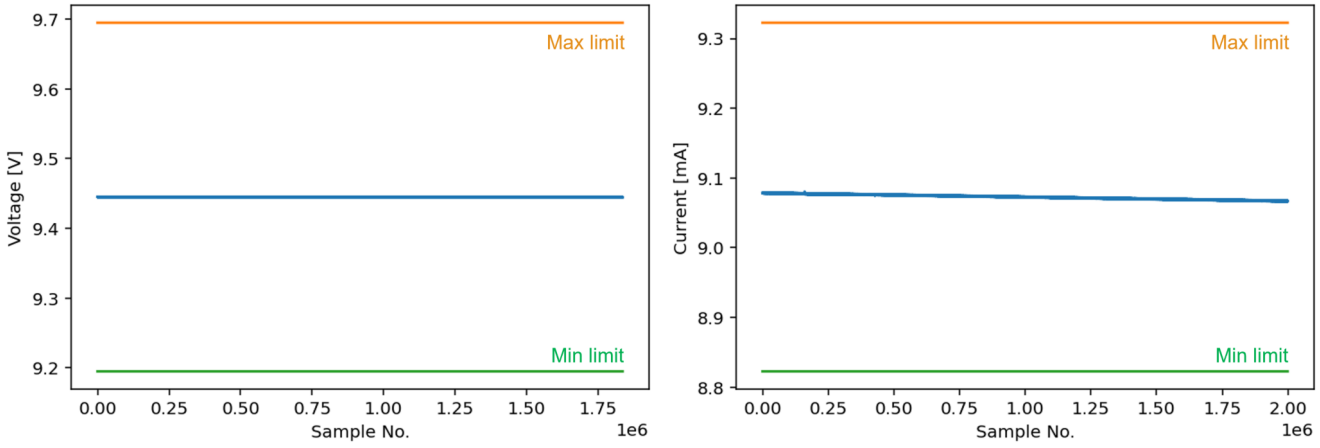

Figure 3-16. Voltage (Left) and Current (Right) Measurements Captured during CI Test

Table 3-13 shows the results of the CI test. The test result is the same for both the voltage and current channels on the EMC test board.

Table 3-13. CI Test Results using ADS125H18 EMC Test Board

Test	IEC Standard	Test Signal		Configuration	Criterion	Test Results
		Field Strength	Frequency			
CI	IEC 61000-4-6	20V/m (Level >3)	150kHz-80MHz	Voltage Input	A	Pass
				Current Input	A	Pass
				DC Port	A	Pass
				Earth Line	A	Pass

4 Schematic, PCB Layout and Bill of Materials

Section 4.1, Section 4.2, and Section 4.3 show the ADS125H18 EMC test board schematic, PCB layout, and bill of materials, respectively

4.1 Schematic

Figure 4-1 to Figure 4-4 show the ADS125H18 EMC test board schematic:

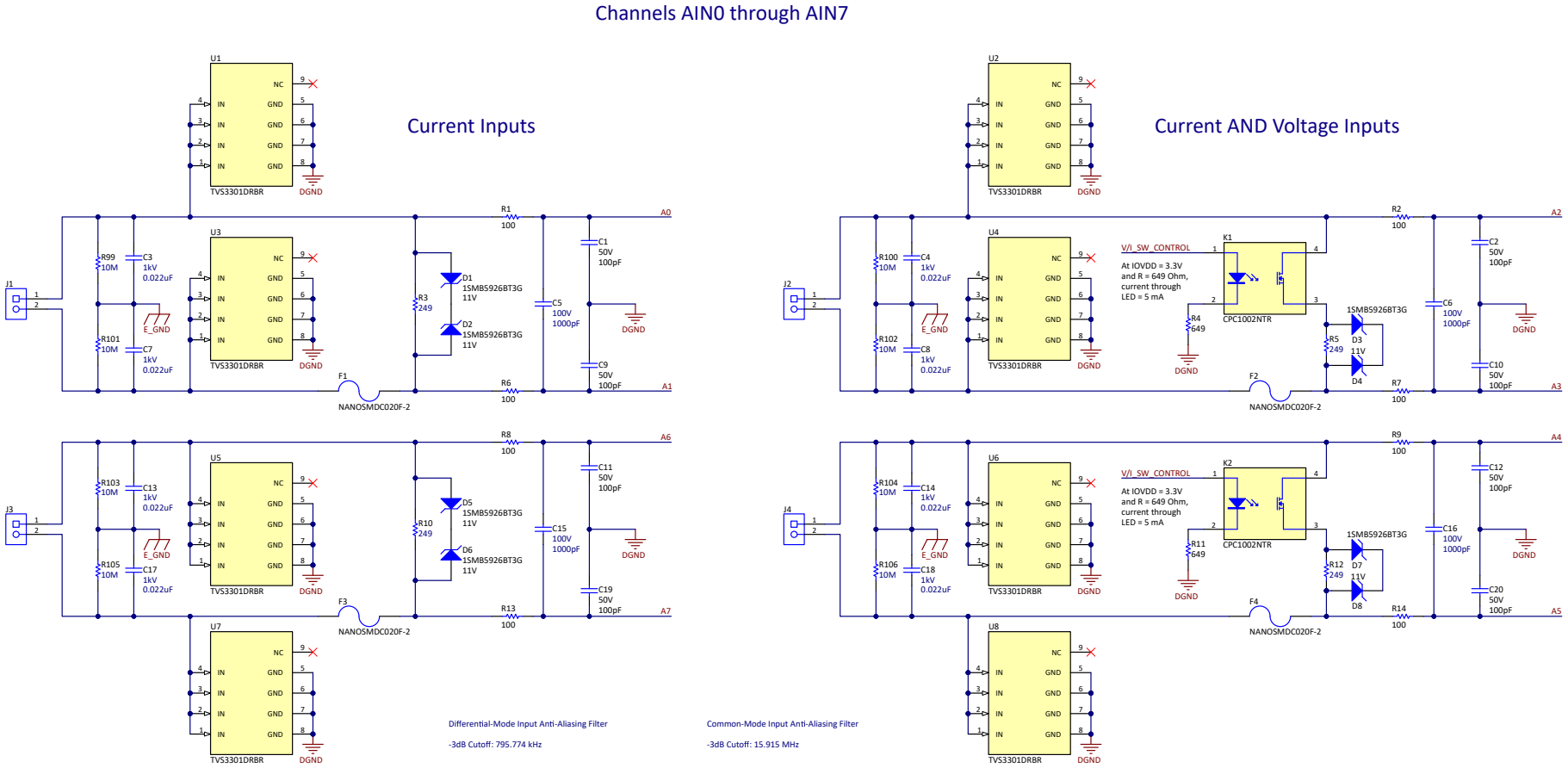

Figure 4-1. ADS125H18 EMC Test Board Analog Inputs AIN0 to AIN7 Schematic

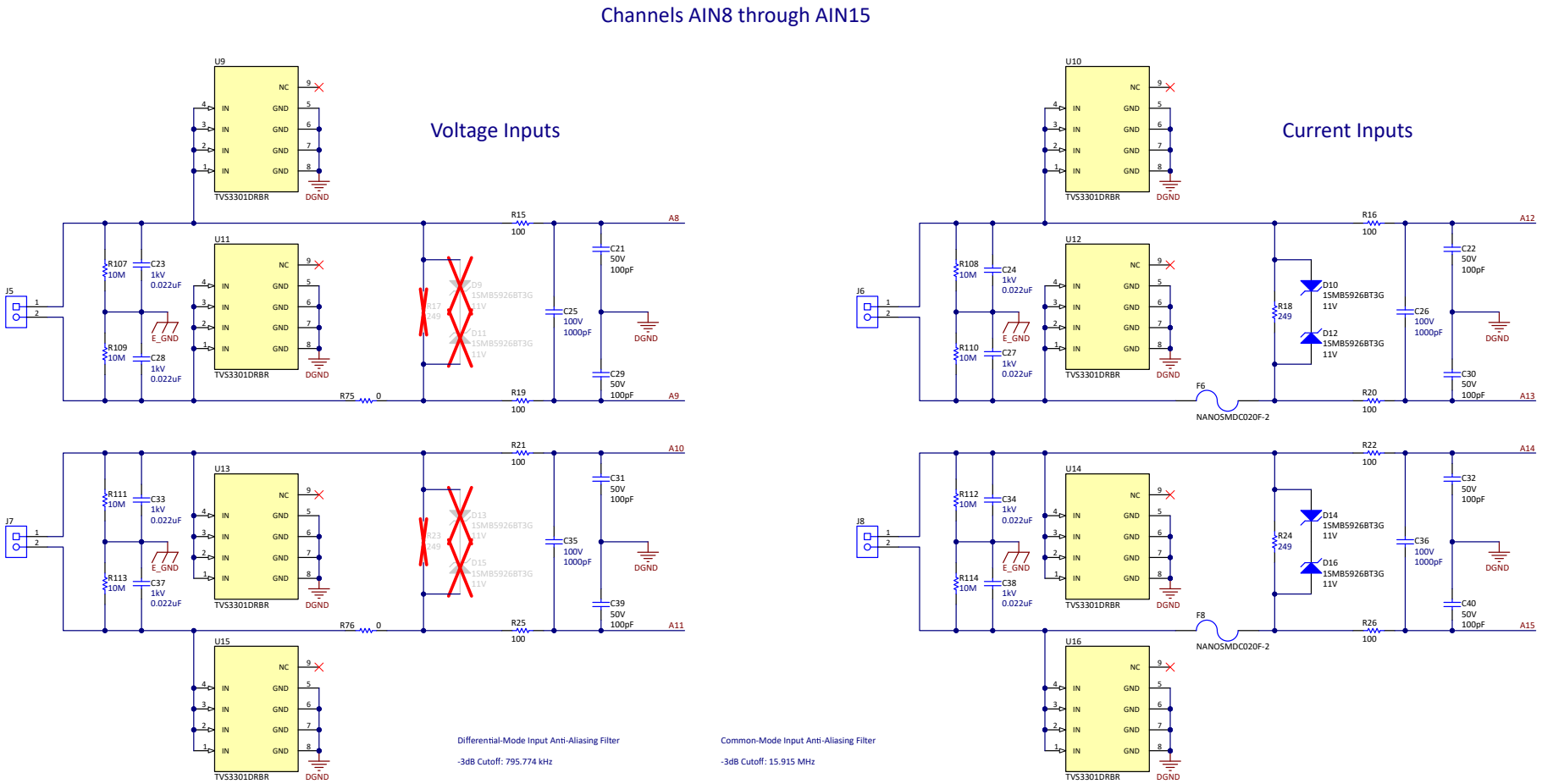

Figure 4-2. ADS125H18 EMC Test Board Analog Inputs AIN8 to AIN15 Schematic

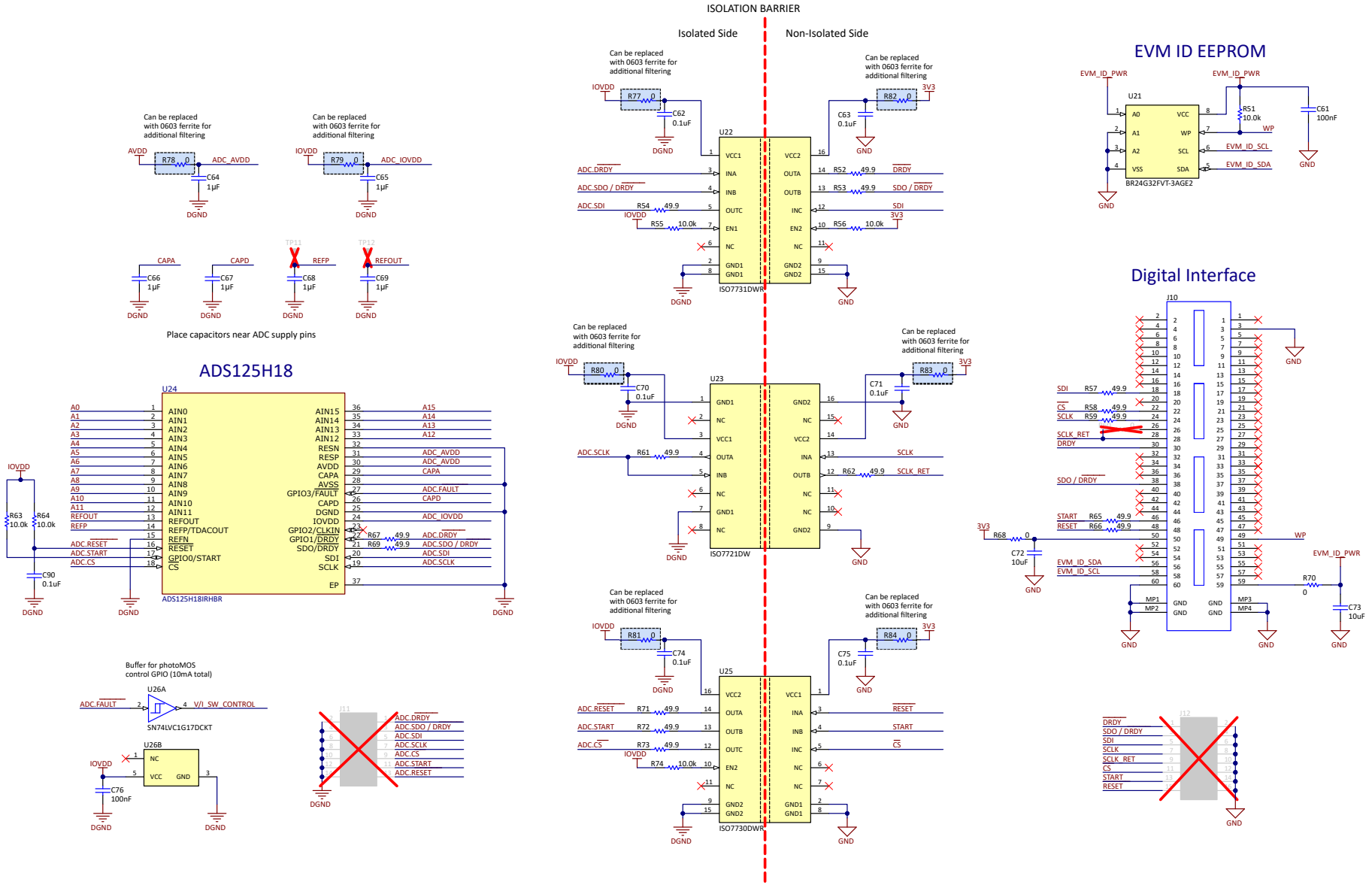

Figure 4-3. ADS125H18 EMC Test Board ADC and Digital Communication Schematic

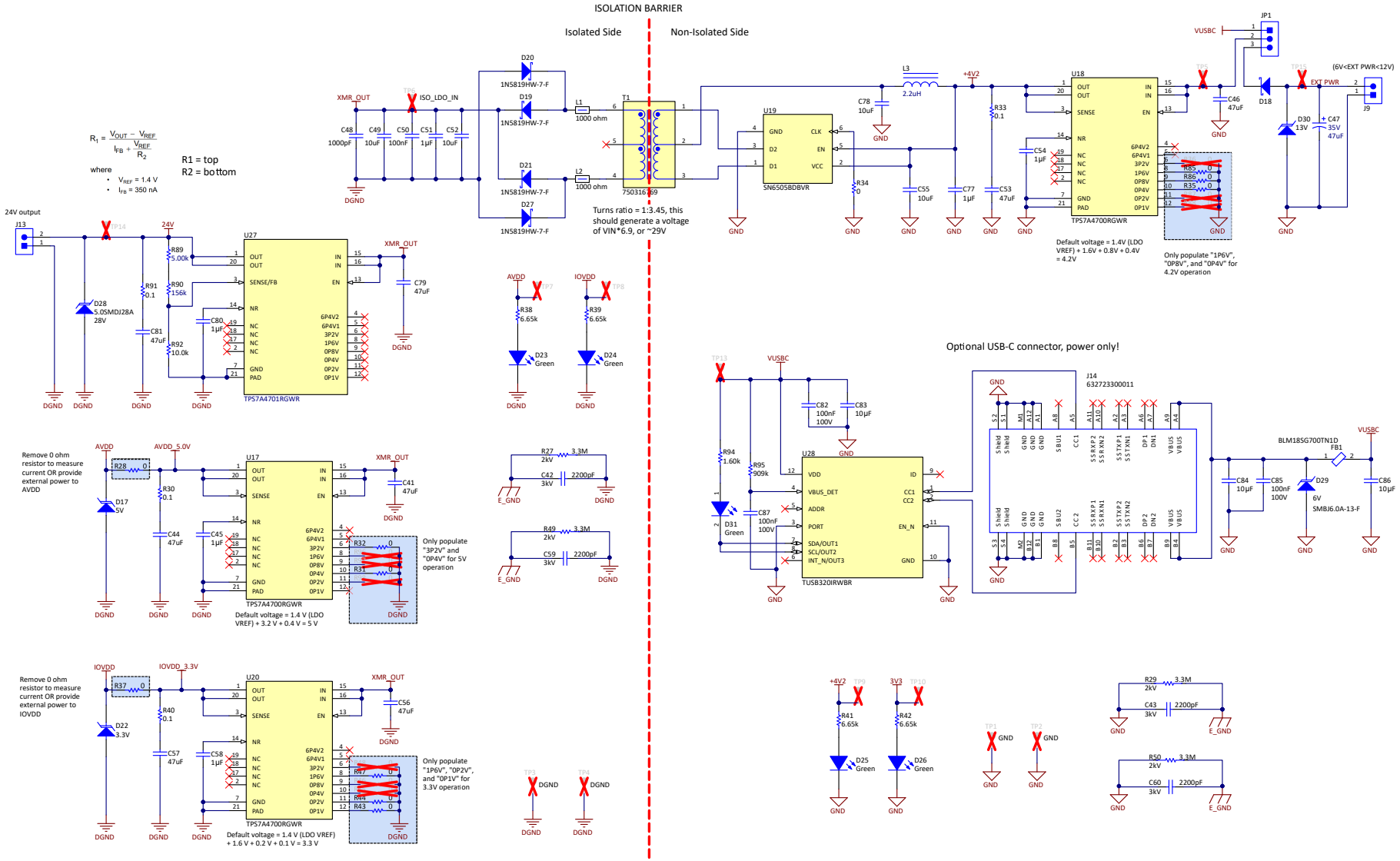

Figure 4-4. ADS125H18 EMC Test Board Isolated and Non-Isolated Power Tree Schematic

4.2 PCB Layout

Figure 4-5 through Figure 4-8 show the ADS125H18 EMC test board PCB layout:

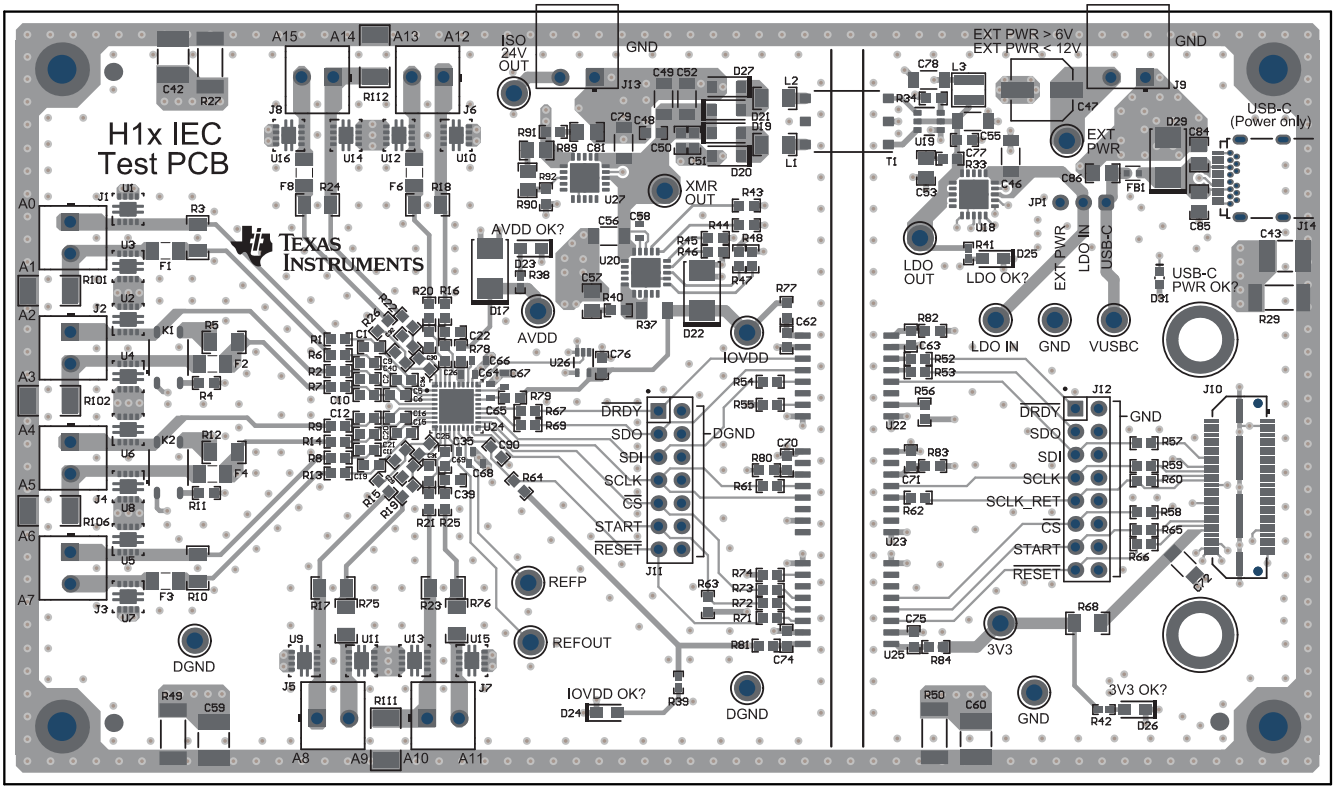

Figure 4-5. ADS125H18 EMC Test Board Top Layer with Silkscreen

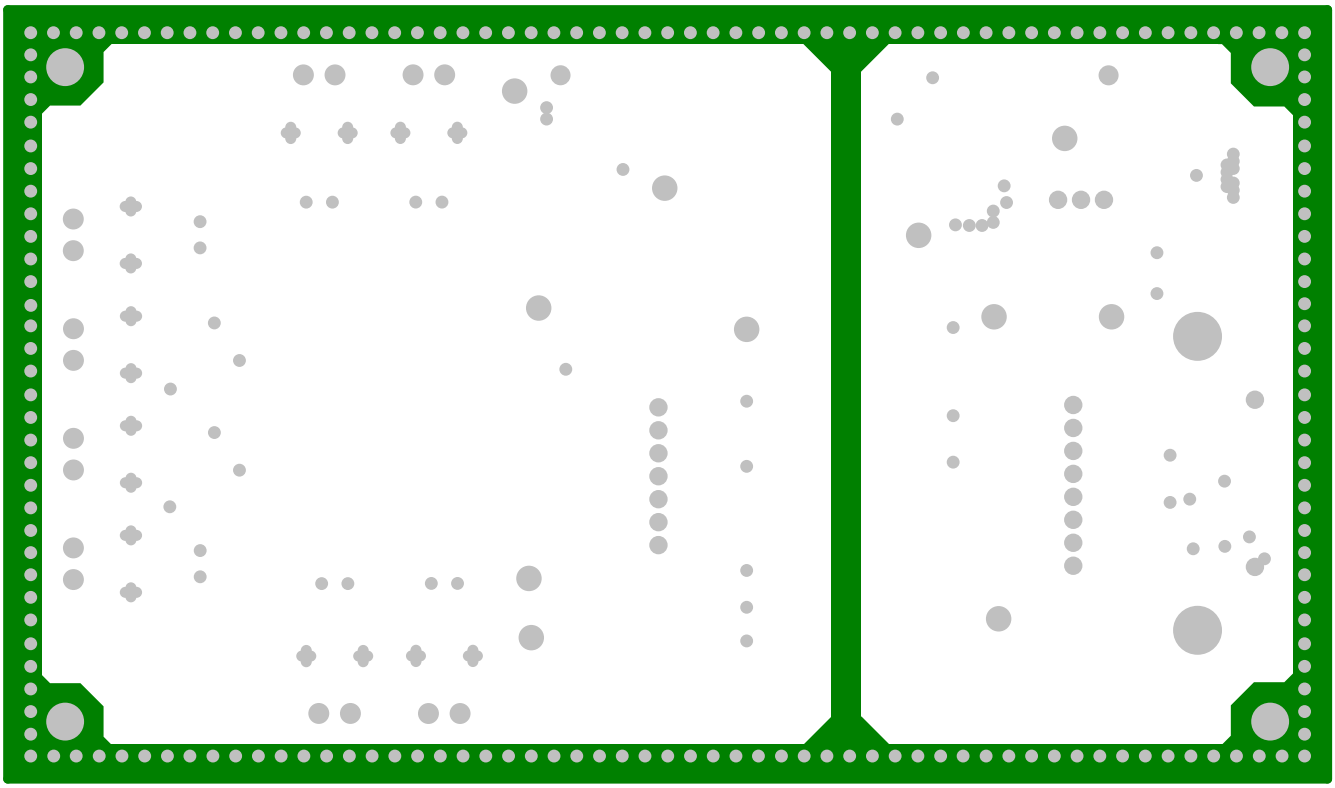

Figure 4-6. ADS125H18 EMC Test Board Inner Ground Layer 1

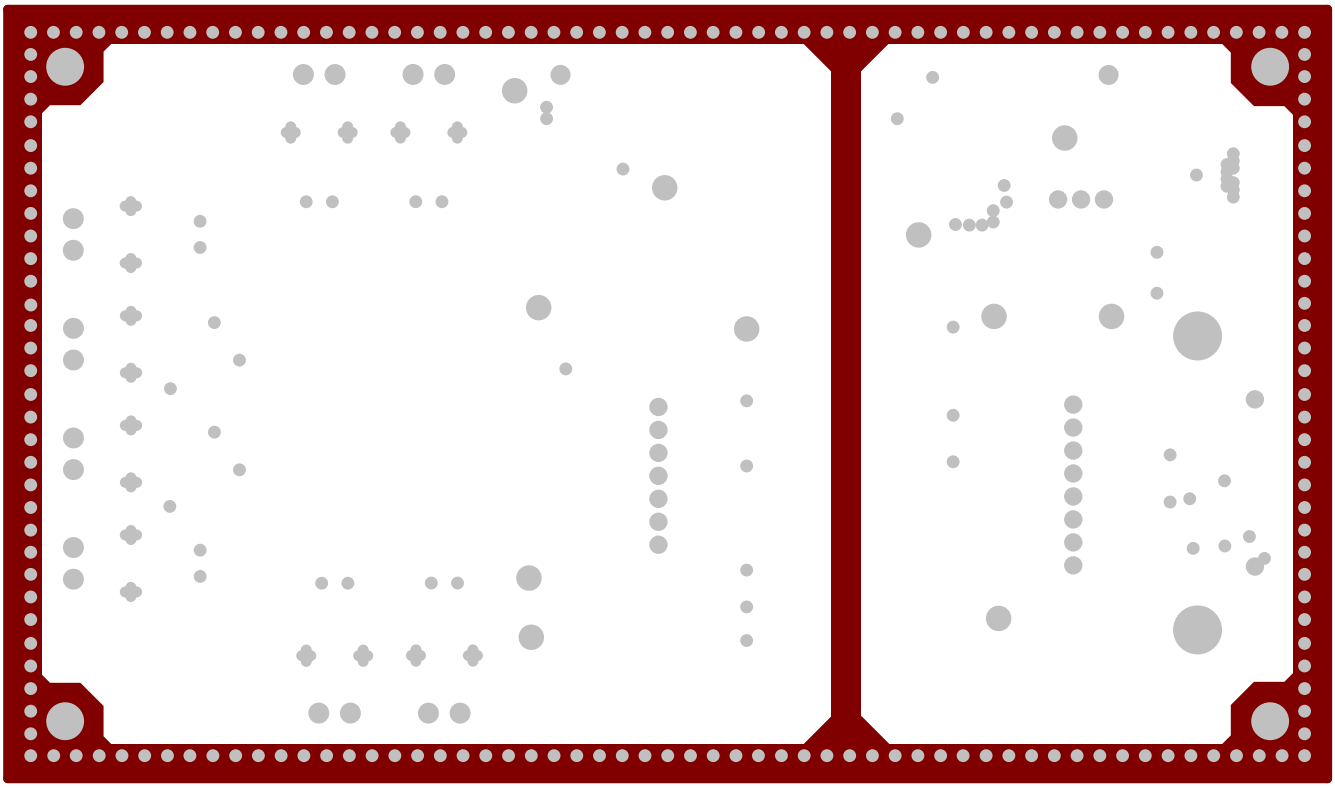

Figure 4-7. ADS125H18 EMC Test Board Inner Ground Layer 2

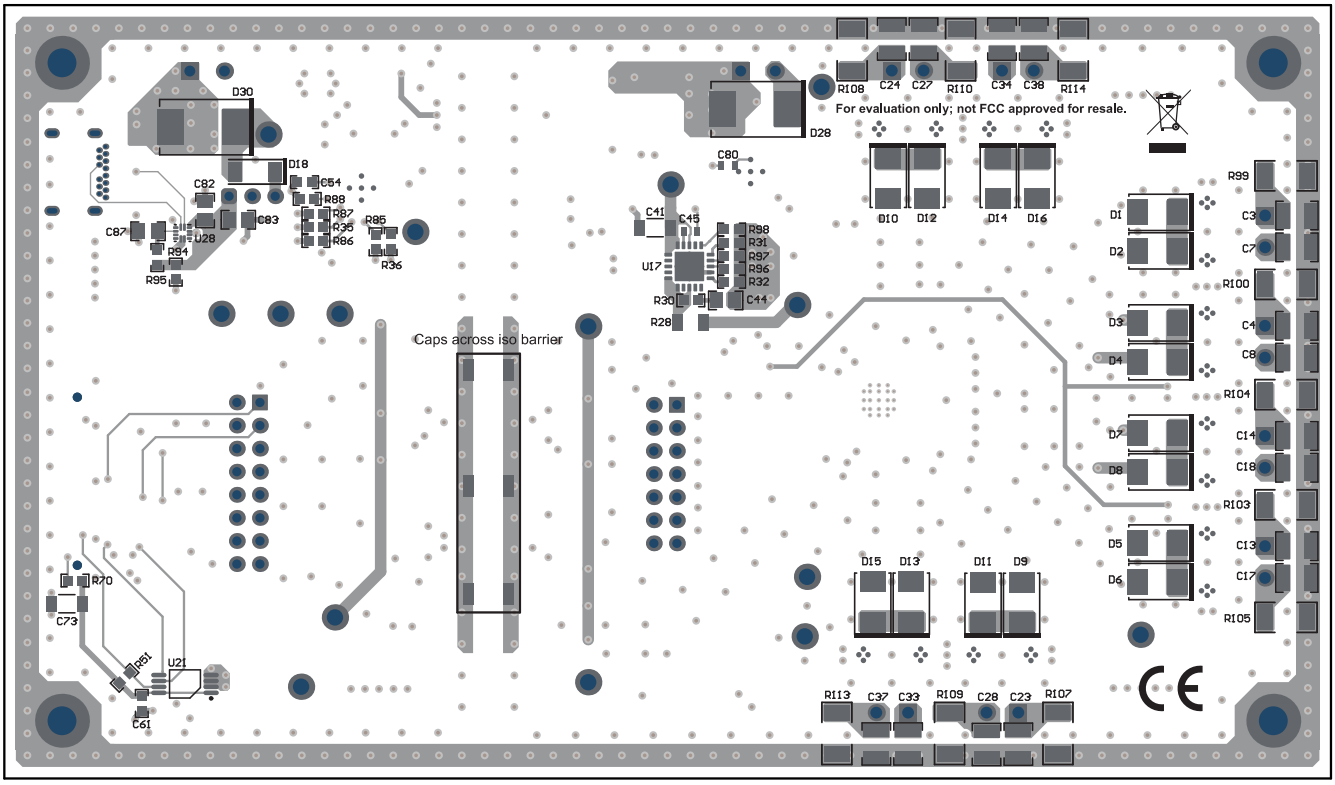

Figure 4-8. ADS125H18 EMC Test Board Bottom Layer with Silkscreen

4.3 Bill of Materials (BOM)

Table 4-1 lists the bill of materials (BOM) for the ADS125H18 EMC test board.

Table 4-1. Bill of Materials

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
C1, C2, C9, C10, C11, C12, C19, C20, C21, C22, C29, C30, C31, C32, C39, C40	16	100pF	CAP, CERM, 100 pF, 50 V, +/- 5%, C0G/NP0, 0603	603	C0603C101J5GAC	Kemet
C3, C4, C7, C8, C13, C14, C17, C18, C23, C24, C27, C28, C33, C34, C37, C38	16	0.022uF	CAP, CERM, 0.022 uF, 1000 V, +/- 10%, X7R, 1210	1210	GRM32DR73A223KW01L	MuRata
C5, C6, C15, C16, C25, C26, C35, C36	8	1000pF	CAP, CERM, 1000 pF, 100 V, +/- 5%, C0G/NP0, 0603	603	GRM1885C2A102JA01D	MuRata
C41, C46, C56, C79	4	47uF	CAP, CERM, 47 uF, 25 V, +/- 20%, X5R, 1206_190	1206_190	C3216X5R1E476M160AC	TDK
C42, C43, C59, C60	4	2200pF	CAP, CERM, 2200 pF, 3000 V, +/- 10%, X7R, 1812	1812	1812HC222KAT1A	AVX
C44, C53, C57, C81	4	47uF	CAP, CERM, 47 uF, 10 V, +/- 20%, X5R, 0805	805	C2012X5R1A476M125AC	TDK
C45, C58, C64, C65, C66, C67, C68, C69, C80	9	1uF	CAP, CERM, 1 µF, 25 V,+/- 10%, X7R, AEC-Q200 Grade 1, 0603	603	CGA3E1X7R1E105K080AC	TDK
C47	1	47uF	CAP, AL, 47 uF, 35 V, +/- 20%, 1 ohm, SMD	F55	EMVY350ADA470MF55G	Chemi-Con
C48	1	1000pF	CAP, CERM, 1000 pF, 50 V, +/- 1%, C0G/NP0, 0603	603	GRM1885C1H102FA01J	MuRata
C49, C52, C55, C78	4	10uF	CAP, CERM, 10 uF, 50 V, +/- 10%, X5R, 1206_190	1206_190	CL31A106KBHNNNE	Samsung Electro-Mechanics
C50, C62, C63, C70, C71, C74, C75, C90	8	0.1uF	CAP, CERM, 0.1 uF, 50 V, +/- 10%, X7R, 0603	603	C0603C104K5RACTU	Kemet
C51, C54, C77	3	1uF	CAP, CERM, 1 uF, 25 V, +/- 10%, X7R, 0603	603	06033C105KAT2A	AVX
C61, C76	2	0.1uF	CAP, CERM, 0.1 uF, 25 V, +/- 5%, X7R, 0603	603	C0603C104J3RACTU	Kemet
C72, C73	2	10uF	CAP, CERM, 10 uF, 25 V, +/- 10%, X7R, 1206_190	1206_190	C1206C106K3RACTU	Kemet
C82, C85, C87	3	0.1uF	CAP, CERM, 0.1 uF, 100 V, +/- 10%, X7R, 0805	805	CL21B104KCFSFNE	Samsung Electro-Mechanics
C83, C84, C86	3	10uF	CAP, CERM, 10 uF, 25 V, +/- 10%, X7R, 0805	805	GRM21BZ71E106KE15L	MuRata
D1, D2, D3, D4, D5, D6, D7, D8, D10, D12, D14, D16	12	11V	Diode, Zener, 11 V, 550 mW, SMB	SMB	1SMB5926BT3G	ON Semiconductor

Table 4-1. Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
D17	1	5V	Diode, TVS, Uni, 5 V, 9.2 Vc, SMB	SMB	SMBJ5.0A-13-F	Diodes Inc.
D18	1	30V	Diode, Schottky, 30 V, 5 A, SOD-128	SOD-128	PMEG3050EP,115	Nexperia
D19, D20, D21, D27	4	40V	Diode, Schottky, 40 V, 1 A, SOD-123	SOD-123	1N5819HW-7-F	Diodes Inc.
D22	1	3.3V	Diode, TVS, Uni, 3.3 V, 7.3 Vc, AEC-Q101, SMB	SMB	SMBJ3V3-E3/52	Vishay-Semiconductor
D23, D24, D25, D26	4	Green	LED, Green, SMD	LED_0805	APT2012LZGCK	Kingbright
D28	1	28V	Diode, TVS, Uni, 28 V, 45.4 Vc, SMC	SMC	5.0SMDJ28A	Littelfuse
D29	1	6V	Diode, TVS, Uni, 6 V, 10.3 Vc, SMB	SMB	SMBJ6.0A-13-F	Diodes Inc.
D30	1	13V	Diode, TVS, Uni, 13 V, 21.5 Vc, SMC	SMC	5.0SMDJ13A	Littelfuse
D31	1	Green	LED, Green, SMD	1.7x0.65x0.8mm	LG L29K-G2J1-24-Z	OSRAM
F1, F2, F3, F4, F6, F8	6		Fuse, Resettable, 0.2 A, 24 VDC, SMD	1206	NANOASMDCH020F-2	Littelfuse
FB1	1		70 Ohms @ 100MHz 1 Power Line Ferrite Bead 0603 (1608 Metric) 4A 20mOhm	603	BLM18SG700TN1D	Murata
H1, H5, H9, H11	4		MACHINE SCREW PAN PHILLIPS 4-40	Machine Screw, 4-40, 1/4 inch	PMSSS 440 0025 PH	B&F Fastener Supply
H2, H7, H10, H12	4		Hex Standoff, #4-40, Aluminum, 1/4"	1/4 inch Aluminum Hex Standoff	1891	Keystone
H3, H6	2		Machine Screw Pan PHILLIPS M3		RM3X4MM 2701	APM HEXSEAL
H4, H8	2		ROUND STANDOFF M3 STEEL 5MM	ROUND STANDOFF M3 STEEL 5MM	9774050360R	Wurth Elektronik
J1, J2, J3, J4, J5, J6, J7, J8	8		Terminal Block, 3.5mm, 2x1, Tin, TH	Receptacle, 3.5mm, 2x1, TH	6.91214E+11	Wurth Elektronik
J9, J13	2		Terminal Block, 2x1, 3.81mm, R/A, TH	Connector, 2 pos. 3.8mm RA	1803277	Phoenix Contact
J10	1		Header(Shrouded), 19.7mil, 30x2, Gold, SMT	Header (Shrouded), 19.7mil, 30x2, SMT	QTH-030-01-L-D-A	Samtec
J14	1		Connector, Receptacle, USB Type C, R/A	Connector, Receptacle, USB Type C, R/A, THT/SMT	6.32723E+11	Wurth Elektronik
JP1	1		Header, 100mil, 3x1, Gold, TH	3x1 Header	TSW-103-07-G-S	Samtec
K1, K2	2		Relay, SPST-NO (1 Form A), 0.7 A, SMD	4.089x3.81mm	CPC1002NTR	IXYS
L1, L2	2	1000 ohm	Ferrite Bead, 1000 ohm @ 100 MHz, 0.4 A, 1206	1206	HZ1206D102R-10	Laird-Signal Integrity Products
L3	1	2.2uH	Inductor, Shielded Drum Core, Ferrite, 2.2 uH, 1.15 A, 0.088 ohm, SMD	2.8 x 1.35 x 2.8mm	744029002	Wurth Elektronik
R1, R2, R6, R7, R8, R9, R13, R14, R15, R16, R19, R20, R21, R22, R25, R26	16	100	RES, 100, 0.1%, 0.1 W, 0603	603	RG1608P-101-B-T5	Susumu Co Ltd

Table 4-1. Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
R3, R5, R10, R12, R18, R24	6	249	RES, 249, 0.1%, 0.25 W, 1206	1206	TNPW1206249RBEEA	Vishay-Dale
R4, R11	2	649	RES, 649, 0.1%, 0.1 W, 0603	603	RT0603BRD07649RL	Yageo America
R27, R29, R49, R50	4		RES SMD 3.3M OHM 1% 1/2W 2010	2010	CHV2010-FX-3304ELF	Bourns
R28, R37	2	0	RES, 0, 1%, 0.5 W, 1206	1206	5108	Keystone
R30, R33, R40, R91	4	0.1	RES, 0.1, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	603	ERJ-3RSFR10V	Panasonic
R31, R32, R34, R35, R43, R44, R47, R77, R78, R79, R80, R81, R82, R83, R84, R85, R86	17	0	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	603	CRCW06030000Z0EA	Vishay-Dale
R38, R39, R41, R42	4	6.65k	RES, 6.65 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	402	CRCW04026K65FKED	Vishay-Dale
R51, R55, R56, R63, R64, R74, R92	7	10.0k	RES, 10.0 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	603	CRCW060310K0FKEA	Vishay-Dale
R52, R53, R54, R57, R58, R59, R61, R62, R65, R66, R67, R69, R71, R72, R73	15	49.9	RES, 49.9, 0.5%, 0.1 W, 0603	603	RT0603DRE0749R9L	Yageo America
R68	1	0	RES, 0, 0.75 W, AEC-Q200 Grade 0, 1206	1206	CRCW12060000Z0EAHP	Vishay-Dale
R70	1	0	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	603	ERJ-3GEY0R00V	Panasonic
R75, R76	2	0	RES, 0, 5%, 0.25 W, AEC-Q200 Grade 0, 1206	1206	ERJ-8GEY0R00V	Panasonic
R89	1	5.00k	RES, 5.00 k, 0.1%, 0.2 W, 0805	805	PNM0805E5001BST5	Vishay Thin Film
R90	1	156k	RES, 156 k, 0.1%, 0.125 W, 0805	805	RT0805BRD07156KL	Yageo America
R94	1	1.60k	RES, 1.60 k, 0.1%, 0.1 W, 0603	603	RG1608P-162-B-T5	Susumu Co Ltd
R95	1	909k	RES, 909 k, 1%, 0.1 W, 0603	603	RC0603FR-07909KL	Yageo
R99, R100, R101, R102, R103, R104, R105, R106, R107, R108, R109, R110, R111, R112, R113, R114	16	10Meg	RES, 10 M, 5%, 0.5 W, 2010	2010	HVC2010-10MJT3	TT Electronics/IRC
T1	1	350uH	Transformer, 350 uH, SMT	7.14x6.73mm	750316769	Wurth Elektronik
U1, U2, U3, U4, U5, U6, U7, U8, U9, U10, U11, U12, U13, U14, U15, U16	16		33 V Bidirectional Flat-Clamp Surge Protection Device, DRB0008A (VSON-8)	DRB0008A	TVS3301DRBR	Texas Instruments
U17, U18, U20	3		36V, 1A, 4.17μVRMS, RF Low-Dropout (LDO) Voltage Regulator, RGW0020A (VQFN-20)	RGW0020A	TPS7A4700RGWR	Texas Instruments
U19	1		Low-Noise 1 A, 420 kHz Transformer Driver, DBV0006A (SOT-23-6)	DBV0006A	SN6505BDBVR	Texas Instruments

Table 4-1. Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
U21	1		I2C BUS EEPROM (2-Wire), TSSOP-B8	TSSOP-8	BR24G32FVT-3AGE2	Rohm
U22	1		High Speed, Robust EMC Triple-Channel Digital Isolators, DW0016B (SOIC-16)	DW0016B	ISO7731DWR	Texas Instruments
U23	1		High Speed, Robust EMC Reinforced Dual-Channel Digital Isolator, DW0016B (SOIC-16)	DW0016B	ISO7721DW	Texas Instruments
U24	1		ADS125H18IRHBR	VQFN36	ADS125H18IRHBR	Texas Instruments
U25	1		High Speed, Robust EMC Triple-Channel Digital Isolators, DW0016B (SOIC-16)	DW0016B	ISO7730DWR	Texas Instruments
U26	1		Single Schmitt-Trigger Buffer, DCK0005A, SMALL T&R	DCK0005A	SN74LVC1G17DCKT	Texas Instruments
U27	1		36V, 1A, 4.17μVRMS, RF Low-Dropout (LDO) Voltage Regulator, RGW0020A (VQFN-20)	RGW0020A	TPS7A4701RGWR	Texas Instruments
U28	1		USB Type-C for USB 2.0 CC Port Controller, RWB0012A (X2QFN-12)	RWB0012A	TUSB320IRWBR	Texas Instruments
D9, D11, D13, D15	0	11V	Diode, Zener, 11 V, 550 mW, SMB	SMB	1SMB5926BT3G	ON Semiconductor
FID1, FID2, FID3	0		Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A
J11	0		Header, 100mil, 7x2, Gold, TH	7x2 Header	TSW-107-07-G-D	Samtec
J12	0		Header, 100mil, 8x2, Gold, TH	8x2 Header	TSW-108-07-G-D	Samtec
R17, R23	0	249	RES, 249, 0.1%, 0.25 W, 1206	1206	TNPW1206249RBEEA	Vishay-Dale
R36, R45, R46, R48, R60, R87, R88, R96, R97, R98	0	0	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	603	CRCW06030000Z0EA	Vishay-Dale
TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP15	0		Terminal, Turret, TH, Double	Keystone1593-2	1593-2	Keystone

5 Summary

Designing a high performance temperature measurement system that can also pass rigorous EMC testing presents a significant challenge for many designers. This application note provides practical, in-depth guidance for developing high-accuracy voltage (±10V) and current (4-20mA) input measurement systems using the ADS125H18 while ensuring robust EMC performance. Key topics covered in the application note include:

1. Design for EMC compliance: Practical guidelines for protective circuit design and optimized PCB layout for 4-layer boards that meet EMC standards.
2. Measurement fundamentals: Detailed explanations of input connections, sensor configurations, code conversion, and error calculation methods for voltage and current measurement systems.
3. Achieved precision: Specific configurations using an EMC-compliant measurement system result in exceptionally high accuracy at room temperature:
   a. Voltage Inputs: 0.04%
   b. Current inputs: 0.032%
4. Validated performance: Test setups and measured results confirm that each design successfully passes all relevant IEC-61000-4 testing requirements.

Follow the practical guidelines and use the validated designs presented in this application note to achieve high-accuracy, reliable, and EMC-compliant voltage and current measurement systems using the ADS125H18. Additionally, this information can be generally applied to any measurement system that must also be EMC compliant.

6 References

1. Texas Instruments, *ADS125H18EVM-PDK*, product page for the ADS125H18 evaluation module.
2. Texas Instruments, *TIDA-010988*, product page for an 8-ch voltage and current combined analog input module with single supply reference design.
3. Texas Instruments, *TI Precision Labs - ADCs*, on-demand training videos for Precision ADCs.

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