User's Guide
SBOU133–September 2013

TINA Simulation Schematic of a Two-Node, Power-Line Communication System

This user's guide describes the primary blocks and use of a simulation schematic of the analog signal chain in a two-node, power-line communication (PLC) system. With TINA-TI, the schematic can be used to simulate the operating conditions of a PLC system based on the AFE031; TI's integrated analog front-end device designed for PLC applications.

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1 Block Description

The two-node TINA-TI simulation schematic consists of two modems, one line-coupling circuit per modem, and a transmission line connecting the two transceivers. Each modem has a transmitter path and a receiver path.

1.1 Transmitter Path

The transmitter path consists of an orthogonal frequency division multiplexing (OFDM) signal source, a signal-conditioning block to provide gain and offset to the OFDM signal, a power amplifier (PA) stage, a power amplifier output disable block, and a PA-side line-coupling circuit.

1.1.1 OFDM Signal Source and Signal-Conditioning Block

Figure 1 shows the OFDM signal source and signal-conditioning blocks.

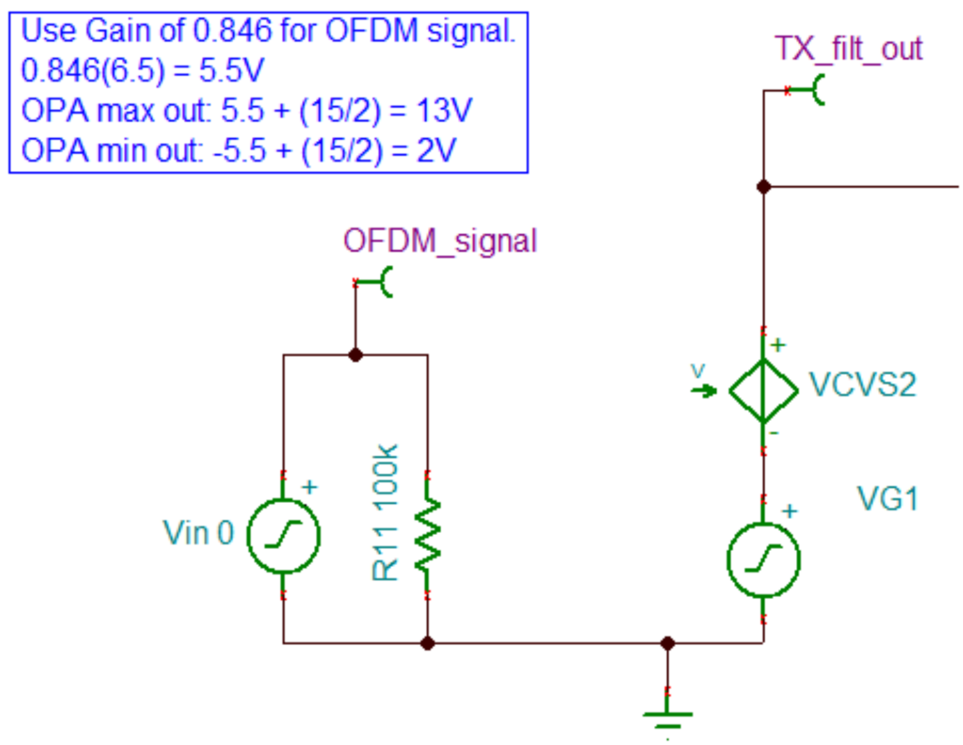

Figure 1. OFDM Signal Source and Signal Conditioning Block

The input to each modem consists of a unique OFDM signal generated by a piecewise linear voltage source (that is, the component labeled *Vin* in Figure 1). Each signal starts with a constant 0 volts period for 300-µs followed by six consecutive OFDM symbols (1.28 ms per symbol) synthesized with 36 equidistant and equipotential tones modulated using DQPSK, starting at 35.9 kHz and ending at 90.6 kHz.

The signal-conditioning block consists of an offset term (the component labeled *VG1* in Figure 1) used to simulate the point in time when the AFE031 Tx_PGA and its voltage reference are enabled. In addition, a gain block (the component labeled *VCVS2* in Figure 1) allows to tailor the amplitude of the signal fed into the PA input; this component models the gain of the AFE031 Tx_PGA.

Each OFDM sequence is normalized to have a peak absolute value of 1 V. The fact that the OFDM signal has a maximum absolute value of 1 volt permits the user to easily scale the signal source to a desired absolute peak PA output. For example, applying a gain of 0.846 V/V to the OFDM signal source allows the alternating current (AC) portion of the PA input to be bounded between –0.846 V and +0.846 V; this signal is then amplified with a gain of –6.5 V/V by the power amplifier (see Section 1.1.2), thus yielding a PA output bounded between 2 V and 13 V. In a real system based on the AFE031, the PA output is ensured to have a voltage swing no smaller than [2 V, 13 V], provided the PA supply is 15 V and the PA output current does not exceed 1.5 A (for complete AFE031 specifications, refer to the AFE031 datasheet available for download at www.ti.com).

1.1.2 Power Amplifier Stage

Figure 2 shows the device component used to model the AFE031 power amplifier. An ideal operational amplifier (op amp) is used in the TINA schematic included for this two-node project. Using an ideal op amp significantly reduces the simulation time; however, the user can substitute this component with the OPA564 TINA model (available at http://www.ti.com/litv/zip/sbom402a) to obtain results that more closely resemble those for the AFE031.

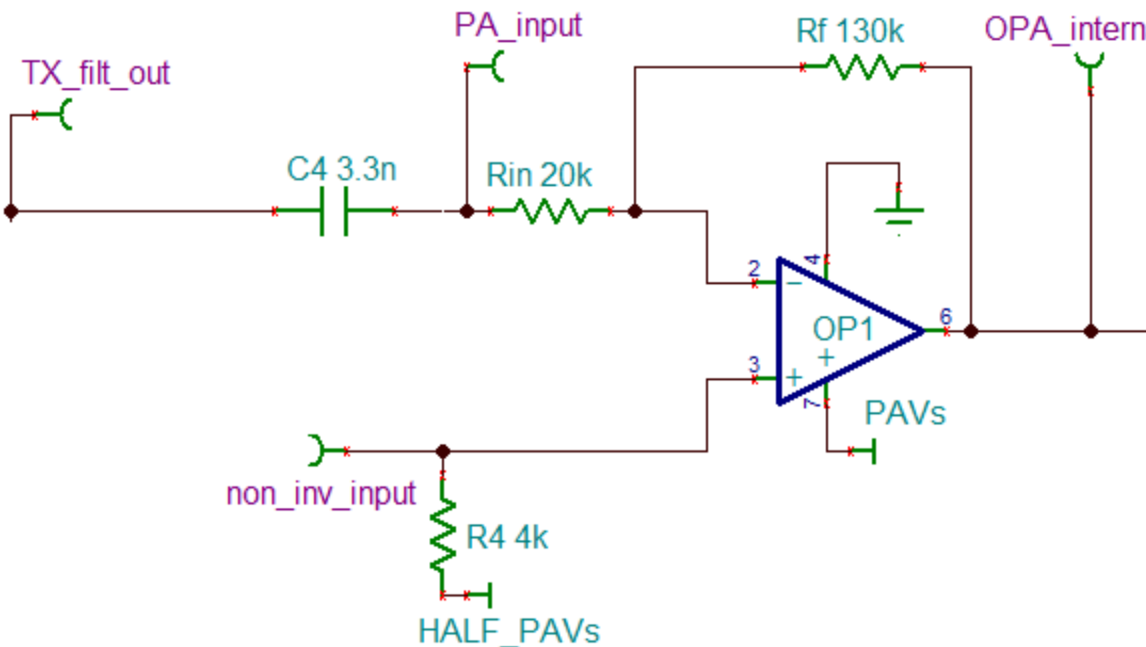

Figure 2. Power Amplifier (PA) Stage

The power amplifier input is capacitively coupled with C4 because the AFE031 Tx_PGA and Tx_Filter operate from a 3.3-V supply, whereas the PA operates from a 15-V supply. Both Rin and Rf set the inverting gain of the power amplifier to –6.5 V/V, the nominal gain of the AFE031 PA block.

1.1.3 Power Amplifier Output Disable Block

This block is used to simulate different methods of connecting the PA internal output to the corresponding pin in the AFE031. In its most basic form, the PA output disable block introduces a time-invariant resistor between the PA output and the network formed by R2 and R3. The most basic implementation is used in the right-hand side modem of the TINA schematic included for this two-node project.

A more sophisticated implementation of the PA output disable block (shown in Figure 3) provides a time-dependent resistance that can be used to model the fact that some time is required for the user to write register 01 of the AFE031 in order to enable the TX and PA block, and then write register 03 of the AFE031 in order to enable the voltage references and PA output stage. This implementation is used in the left-hand side modem of the TINA schematic included for this two-node project.

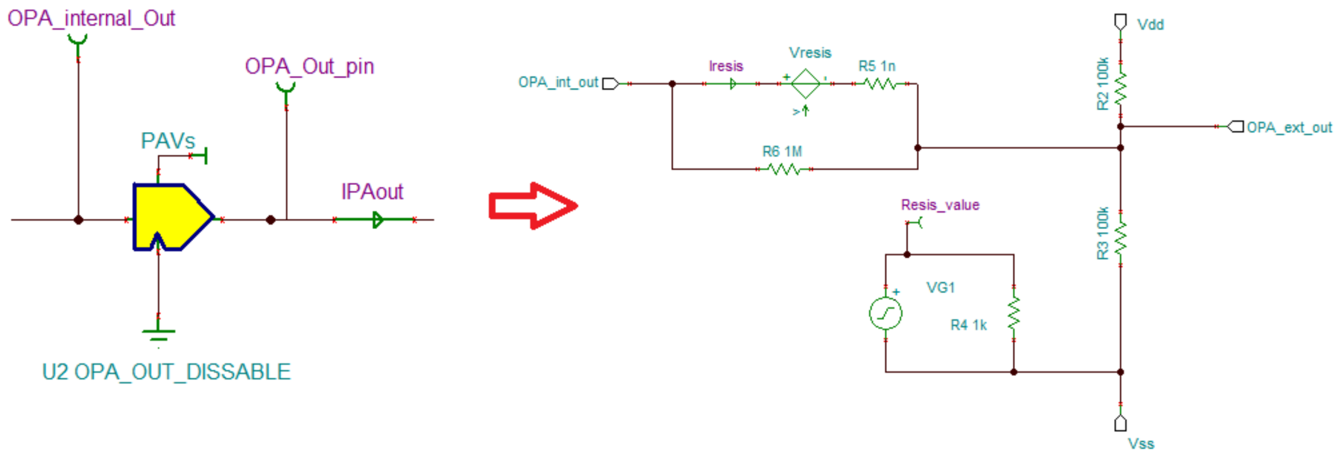

Figure 3. PA Output Disable Block

1.1.4 PA-Side Line-Coupling Circuit

Figure 4 shows the PA-side line-coupling circuit.

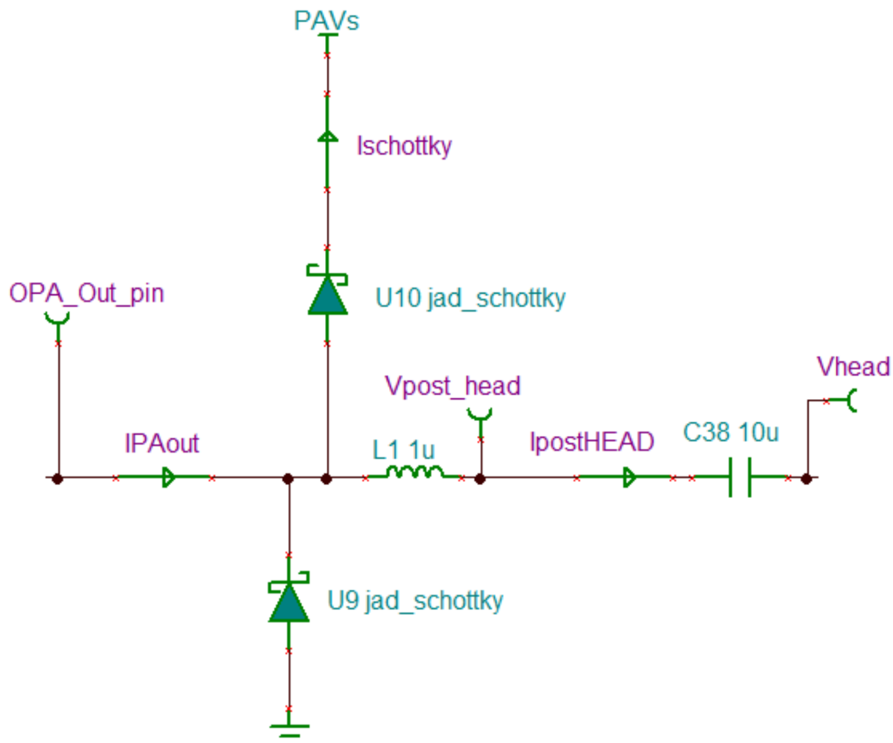

Figure 4. PA-Side Line-Coupling Circuit

This line-coupling circuit protects the output of the AFE031 PA from rising above PAVs or dropping below PA_GND when a voltage surge in the power line is injected into the modem. In particular, the schottky diodes U9 and U10 shunt current and prevent such rises or drops from occurring. Another element used to prevent damage to the AFE031 PA is L1. This inductor slows down abrupt currents injected into the modem caused by voltage surges in the power line.

When the transmitter reaches a steady state, C38 is charged to one-half the PA power-supply level, thus allowing the *Vhead* node to swing at approximately ground potential with a 0-VDC offset.

Note that L1 and C38 also provide a small level of band-pass filtering in the frequency range of interest.

1.2 Receiver Path

The receiver path consists of a passive band-pass filter and a programmable gain amplifier (PGA).

Figure 5 shows the receiver path's band-pass filter; although optional, this filter is recommended for applications where high performance is required.

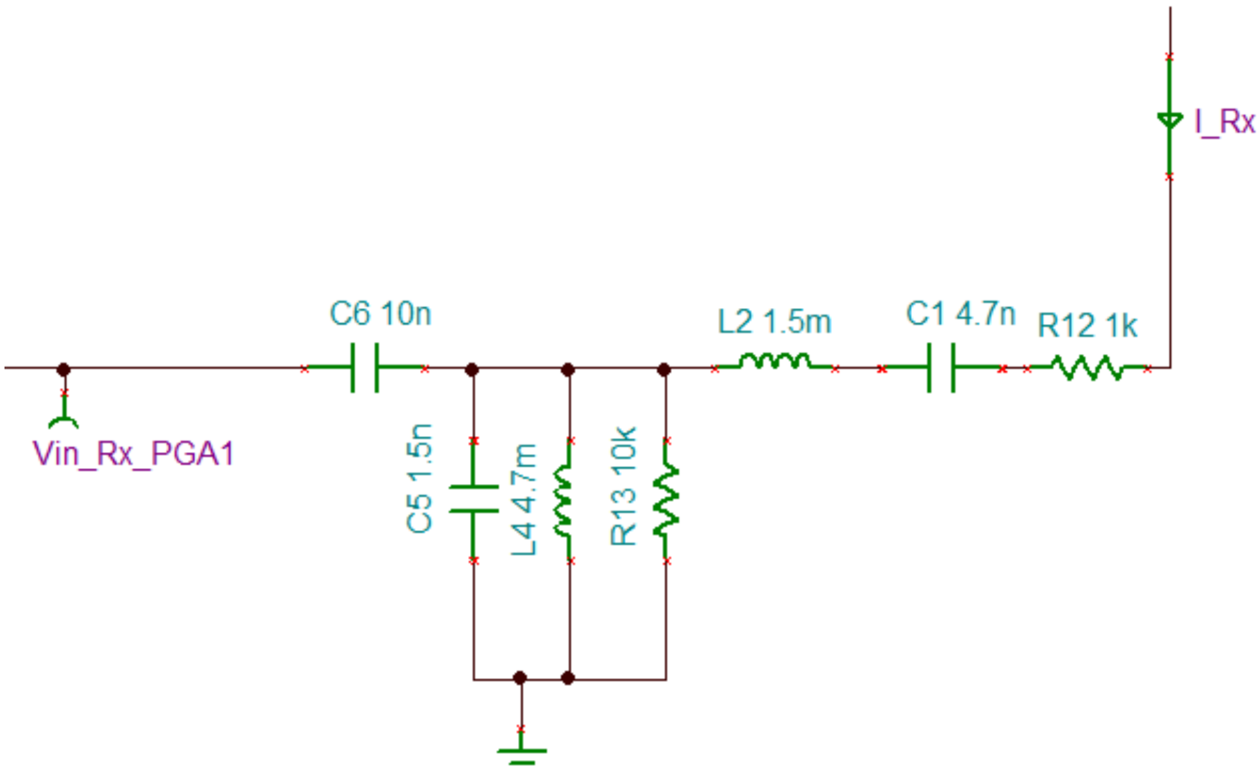

Figure 5. Passive Band-Pass Filter on the Receiver Path

Figure 6 shows the PGA for the receiver path. The specific resistor values used in the AFE031 Rx_PGA are provided in the table included in Figure 6. Note that for this table, R16 = Rin and R17 = Rf .

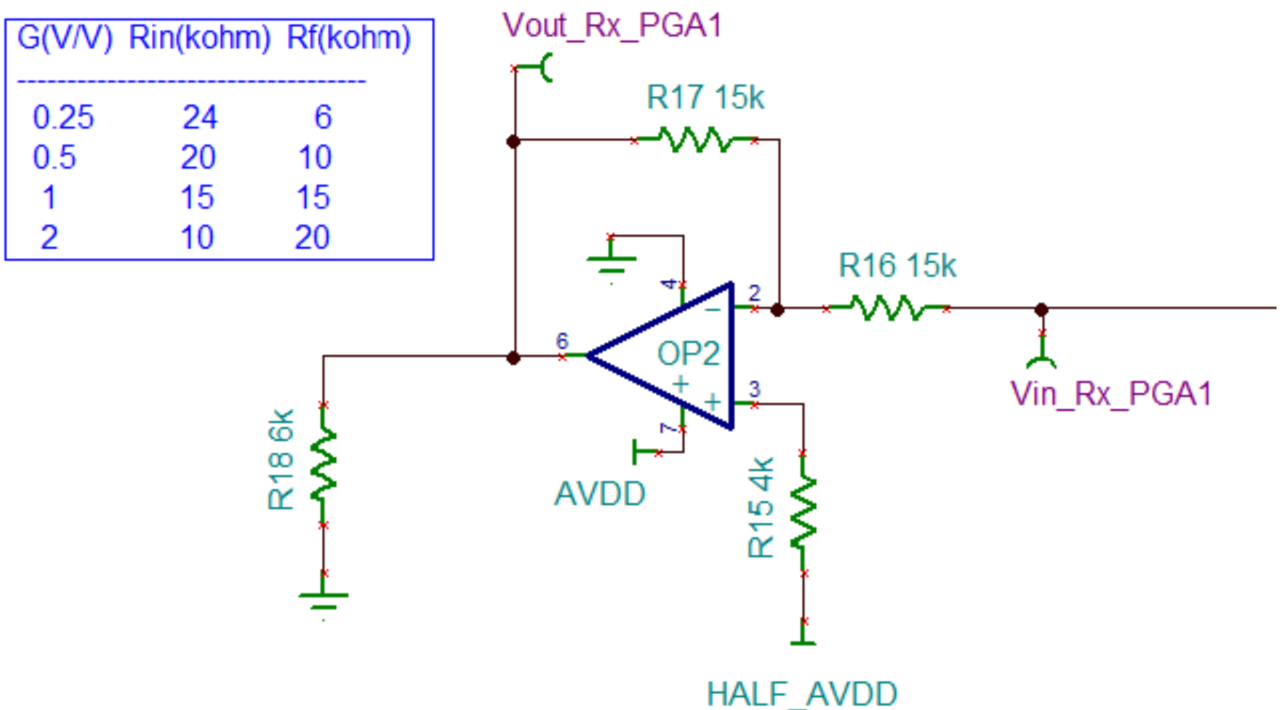

Figure 6. Programmable Gain Amplifier on the Receiver Path

1.3 Line-Coupling Circuit

Figure 7 shows the modem line-coupling circuit that consists of a passive shunt filter (C3 and R1), protection transient voltage suppressors (TVSs), line-coupling transformer, and power-line (PL)-side band-pass filter.

The shunt filter dampens high-frequency components that arise during circuit startup and remain until steady state is reached. U5 is an optional filter used to decrease lower-frequency components that also arise during circuit startup.

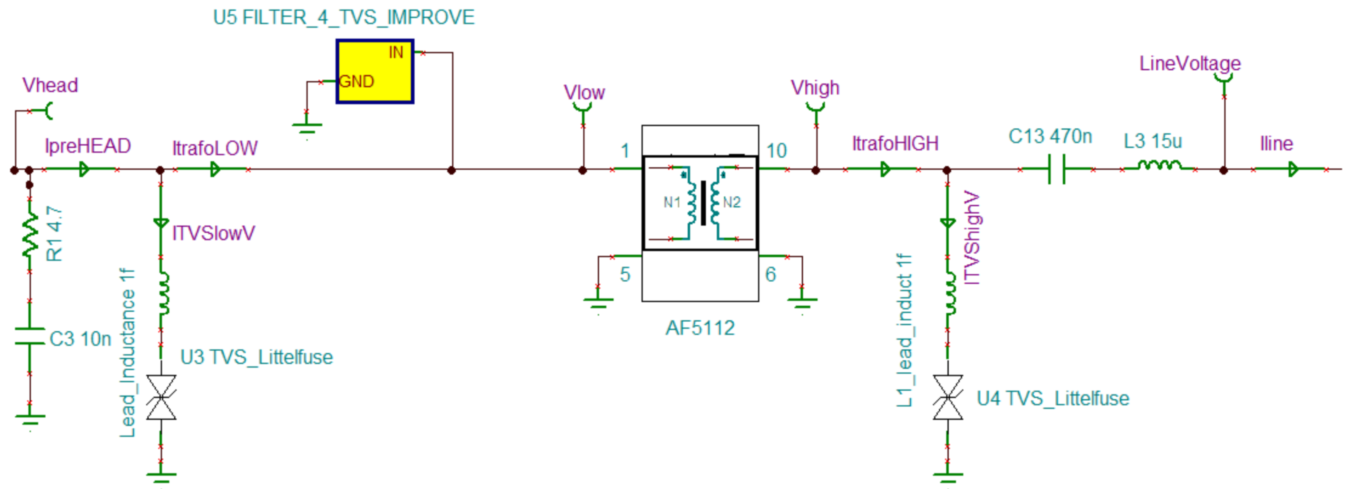

Figure 7. Modem Line-Coupling Circuit

Figure 7 includes inductors in series to the TVSs to account for printed circuit board (PCB) parasitics. For more information on the purpose and selection of the line-coupling circuit elements, refer to the AFE031 and application report Analog Front-End Design for a Narrowband Power-Line Communications Modem Using the AFE031 (SBOA130).

2 Typical Simulation

To run a typical simulation of the two-node PLC system using TINA version 9.3, click on Analysis > Transient. A dialog box allows the user to define the simulation time and initial conditions. Selecting zero initial conditions provides results with all capacitors starting at zero volts. Figure 8 and Figure 9 show these steps.

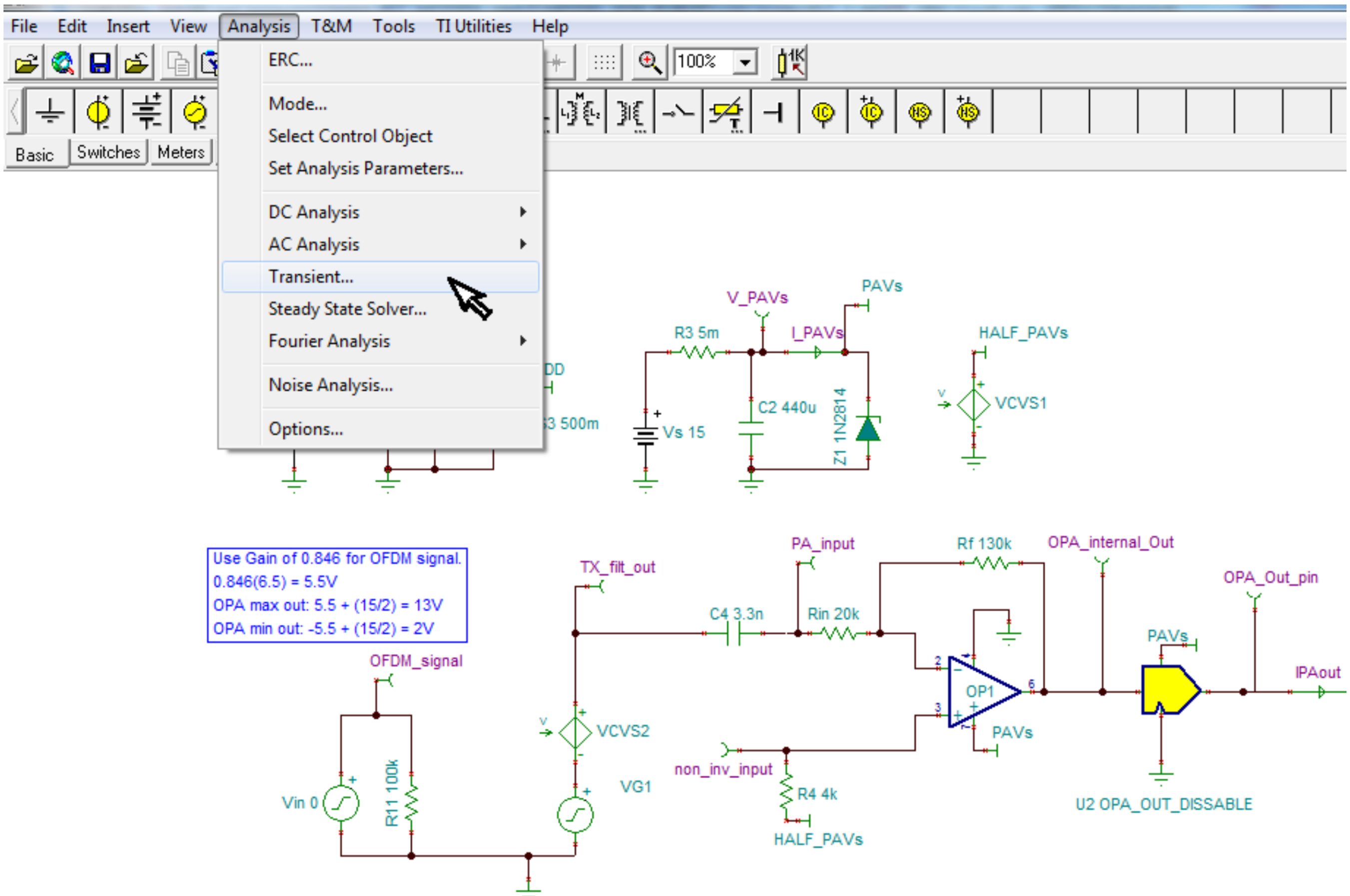

Figure 8. Transient Analysis Menu in TINA Version 9.3

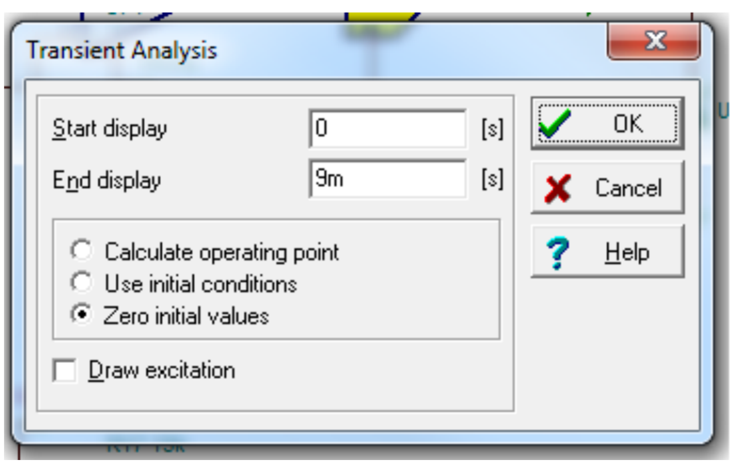

Figure 9. Dialog Box

After running a typical simulation, the user can probe various nodes and observe circuit behavior. Figure 10 shows the waveforms corresponding to a typical simulation where the left-hand side modem is transmitting and the right-hand side modem is receiving. The raw OFDM signal, the power amplifier output of the transmitting modem, and the signal at the output of the Rx_PGA in the receiving modem are shown in Figure 10.

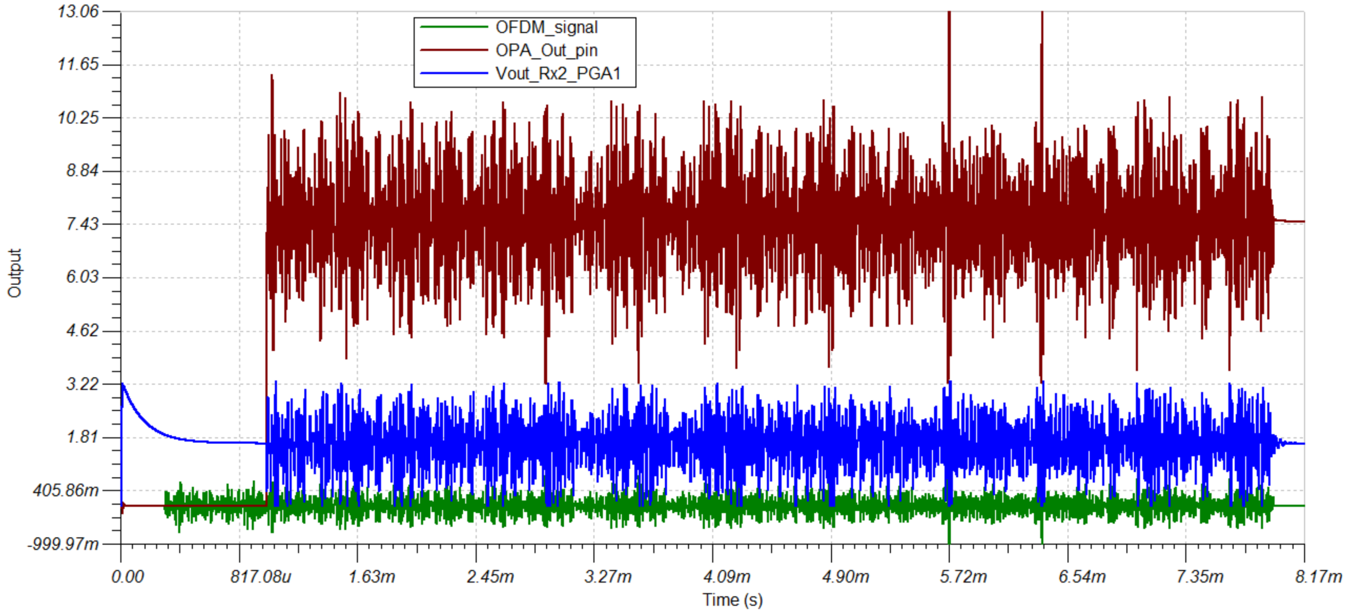

Figure 10. Results From a Typical Simulation

Table 1 provides a summary of signals in the simulation schematic. Note that all signals present in modem 1 have a counterpart signal in modem 2.

Table 1. Signals in Modem 1

Signal Label	Description
OFDM_signal	Six consecutive OFDM symbols (1.28 ms per symbol) synthesized with 36 equidistant and equipotential tones
TX_filt_out	Signal modeling the output of the transmitter filter; this signal can be measured on terminal 2, jumper 4 of the AFE031 module in the TMDSPLCKIT-V3
non_inv_input	Signal present on the noninverting input of the power amplifier
PA_input	Input to the power amplifier (pin 18 of the AFE031)
OPA_internal_Out	Signal corresponding to the ideal output of the power amplifier, regardless of the PA output disable block state
OPA_Out_pin	Signal on pins 42 and 43 of the AFE031; this signal depends on whether the PA output is enabled or not
IPAout	Current flowing out of the power amplifier (pins 42 and 43 of the AFE031)
Vpost_head	Signal in the middle point of the PA-side line-coupling circuit
IpostHEAD	Current flowing through the LC combination in the PA-side line-coupling circuit
Vhead	Signal in the PA-side winding of the line-coupling transformer; this signal can is on TP2 and TP4 of the AFE031 module in the TMDSPLCKIT-V3
ItrafoLOW	Current flowing through the PA-side winding of the line-coupling transformer
Vhigh	Signal on the power-line side of the line-coupling transformer
ItrafoHIGH	Current flowing through the winding in the power-line side of the line-coupling transformer
LineVoltage	Signal at the point of connection to the power line
I_Rx	Current flowing into the receiver portion of the modem
Vin_Rx_PGA1	Input to the receiver PGA1
Vout_Rx_PGA1	Output of the receiver PGA1
AVDD	Analog supply (3.3 V, typical)
HALF_AVDD	Analog supply level divided by two
V_PAVs	Power amplifier supply
HALF_PAVs	Power amplifier level divided by two

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