Analog Engineer's Circuit

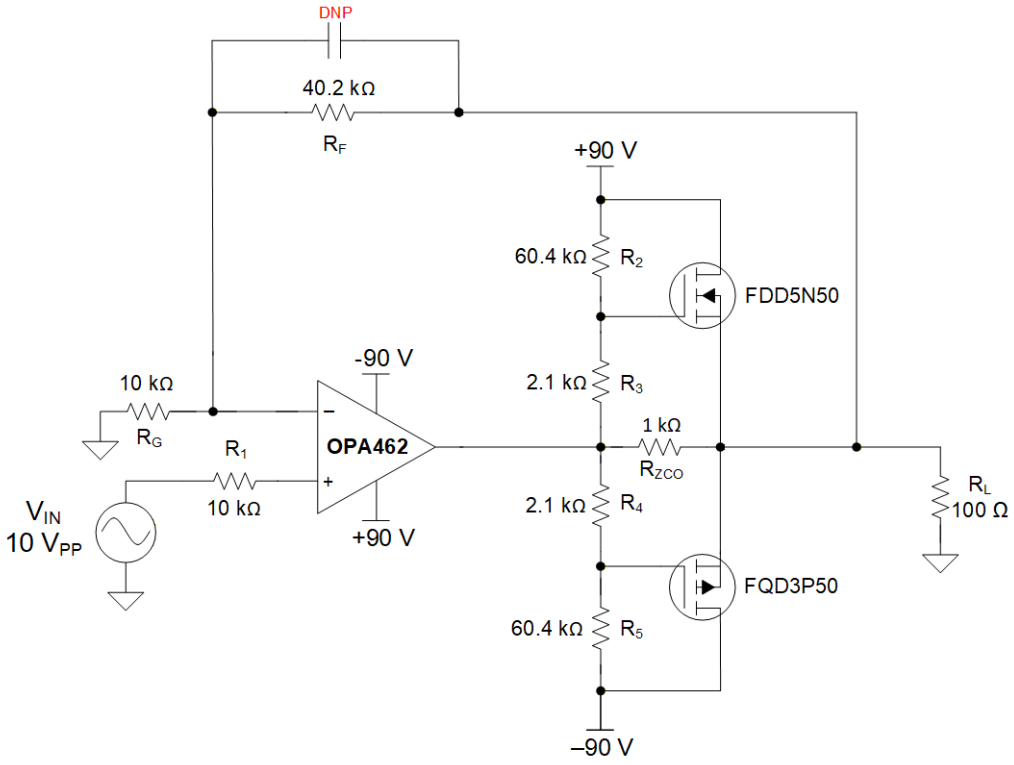
High Voltage Amplifier with Discrete Output Current Boost

Design Goals

Input			Output	
V_{IN}	Bandwidth	Gain	V_{OUT}	I_{OUT}
$10V_{PP}$	20kHz	5V/V	$50V_{PP}$	500mA

Design Description

This circuit implements a non-inverting amplifier with a gain of 5 to drive discrete complementary output transistors. This circuit is capable of delivering 500mA at 20kHz with negligible distortion. This circuit is designed to be operated at ±90V.



OPA462 Discrete Output Current Boost Circuit

Design Notes

1. A voltage divider network (R_2, R_3, R_4, and R_5) provides nominal voltage to bias V_{GS}. It is essential to choose a voltage bias network that minimizes crossover distortion, but does not cause cross conduction, as this can damage the metal-oxide-semiconductor field-effect transistors (MOSFETs) and surrounding circuit. Cross conduction occurs when both MOSFETs are on at the same time. This can cause large current surges and thermal runaway which can damage the circuit.
2. Select a high voltage op amp to maximize the output swing of the circuit.
3. Bandwidth is a function of the closed loop gain, as seen from the equation below. Selecting an amplifier with a large gain bandwidth allows for wider frequency response.

$$Closed\ \ Loop\ \ Bandwidth = \frac{Gain\ \ Bandwidth\ \ Product}{A_{CL}} \quad (1)$$

4. Verify input voltage is within the full power bandwidth and output voltage specifications for the given op amp. For a ±90 V supply, slew induced distortion will become significant above 50kHz (see Figure 28 from OPA462 datasheet). This can also be calculated using the equation:

$$V_{pk} = \frac{Slew\ \ Rate}{2 \times \pi \times f} \quad (2)$$

   Distortion becomes more significant the closer the output voltage is to the power supply rails. However, distortion in the output crossover region, resulting from the switching characteristics of the discrete transistors, differs from slew-rate-induced distortion. This crossover distortion is also dependent on the input and output capacitance of the transistors, and difficult to calculate empirically. Therefore, the best approach to determine if the desired input frequency is feasible is to simulate the circuit.
5. When designing the voltage divider, use smaller resistor values to lessen the transition time between the push-pull pair. The gate resistor and input capacitance of the MOSFET (FET) determines the RC time constant. Therefore, the smaller the resistor, the faster theFET will switch on. However, smaller resistor values increase the current consumption through the bias path, so it is important to be aware of this trade-off. In this example design, R_2 and R_5 were chosen to be 60.4kΩ for best results.
6. Careful consideration of the characteristics and trade-offs between bipolar junction transistors (BJTs) and MOSFETs is essential when choosing a discrete complementary output stage (see Table 3-1 from the application note Optimizing Dual Feedback Compensation in the OPA593 With a Current Booster for further detail).
7. Including a footprint for a compensation capacitor C_F is recommended to provide flexibility for stability optimization. Instability can result from capacitive loading at the output node, large feedback resistors, or capacitance on the inverting input. Refer to the Operational Amplifier Stability Theory and Compensation Methods technical paper for a detailed discussion of op amp stability and compensation methods.
8. Components in output path of the transistors, such as the load resistor, R_L, must have adequate power ratings. High voltage and high-power PCB layout guidelines should also be followed (see the TIPL training on Power and Temperature). Consider using a fan to help reduce the heat that the circuit can generate.

Design Steps

1. Calculate maximum output current for given Gain and R_L.

$$Given: V_{IN} = 10V_{PP}, \quad R_G = 10k\Omega, \quad R_F = 40.2k\Omega, \quad R_L = 100\Omega \tag{3}$$

$$I_{OUT} = \frac{V_{OUT}}{R_L} = \frac{V_{IN}\left(\frac{R_F}{R_G} + 1\right)}{R_L} = \frac{10\left(\frac{40.2k\Omega}{10k\Omega} + 1\right)}{100\Omega} = 500.2mA \tag{4}$$

2. Calculate the output power of the circuit and select MOSFETs with appropriate power dissipation capabilities. The output FET power will be a function of the load, output voltage and supply voltage. For resistive loads, with the load ground-referenced, the power will peak when the output voltage is halfway between ground and the supply voltage. The peak current the FET will consume is 500mA, with the TINA-TI simulation results showing a maximum output power of approximately 16.2W. Note that the output of the amplifier is significantly lower, consuming less than 300mW of power, demonstrating the benefits of this circuit configuration. Select MOSFETs that have greater than 30W of power dissipation capability, such as FDD5N50 and FQD3P50, which have a power dissipation of at least 50W. The maximum power dissipation at the output stage with a resistive load can be calculated using the following equation. Note that power consumption will vary with the load type (resistive vs. current). Refer to the TIPL on Power and Temperature for further details.

$$P_{AC\_MAX\_AVG} = \frac{2 \times {V_{CC}}^2}{\pi^2 \times R_L} \tag{5}$$

$$P_{AC\_MAX\_AVG} = \frac{2 \times (90V)^2}{\pi^2 \times 100\Omega} \tag{6}$$

$$P_{AC\_MAX\_VG} = 16.414W \tag{7}$$

3. Select a zero-crossover resistor (R_{ZCO}) that provides sufficient current to drive the circuit while the MOSFETs are off. During this period, the R_{ZCO} is driving the load. Consider the trade-offs when selecting the R_{ZCO}. R_{ZCO} must be high enough to avoid current limit of the amplifier, but low enough to minimize noise and crossover distortion. A large R_{ZCO}, when paired with a capacitive load, can result in slower transients. However, a larger R_{ZCO} results in lower power dissipation.

   The value of R_{ZCO} can be iteratively determined through simulation. The results shown below demonstrate that resistor values below 100 Ω cannot drive the loop when the MOSFETs are off. The 499 Ω resistor value drives 10.1 mA of current, while the 1kΩ drives 5.05mA of current. The 1kΩ resistor has a thermal noise of approximately 4 nV/√Hz, which is smaller than the op amp voltage noise of 23nV/√Hz . Therefore, 1kΩ is a good choice for the R_{ZCO}, optimizing for both voltage noise and low power dissipation.
4. Calculate the voltage divider resistor values based on the V_{TH} of the selected MOSFET or BJT. To minimize power dissipation from VCC and VEE, use relatively large resistance for R_2 and R_5.

Given: R_2 = R_5 = 60.4 kΩ.

From the FDD5N50 datasheet, 3 V < $V_{GS(th)}$ < 5 V.

Optimize the resistor divider network by selecting R_3 and R_4 such that $V_{GS(th)}$ = 3 V.

Set V_{GS} to nominal value 3V to optimize for crossover distortion without cross conduction.

$$V_{GS} = \frac{R_3}{R_2 + R_3} \times VCC \tag{8}$$

$$3V = \frac{R_3}{60.4k\Omega + R_3} \times 90V \tag{9}$$

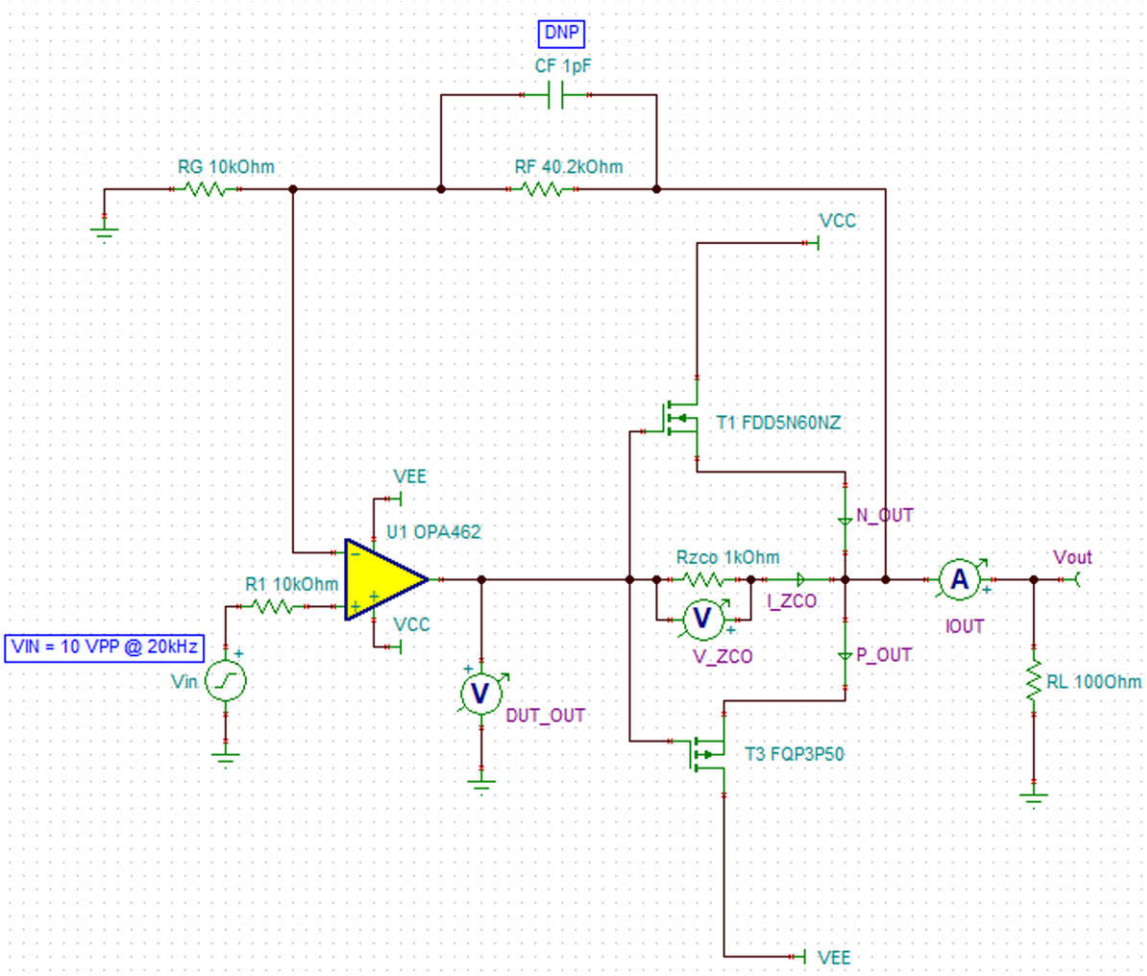
$$R_3 = 2082.76\Omega \tag{10}$$

Choose standard resistor value such that $R_3 = 2.1k\Omega$.

$$\therefore R_3 = R_4 = 2.1k\Omega \quad (11)$$

R_3 and R_4 can be further optimized for crossover distortion empirically, as individual $V_{GS(th)}$ values for the chosen MOSFETs will vary due to process variation. However, caution should be used, as there is a possibility for cross conduction if V_{GS} is too high.

Design Simulation Results

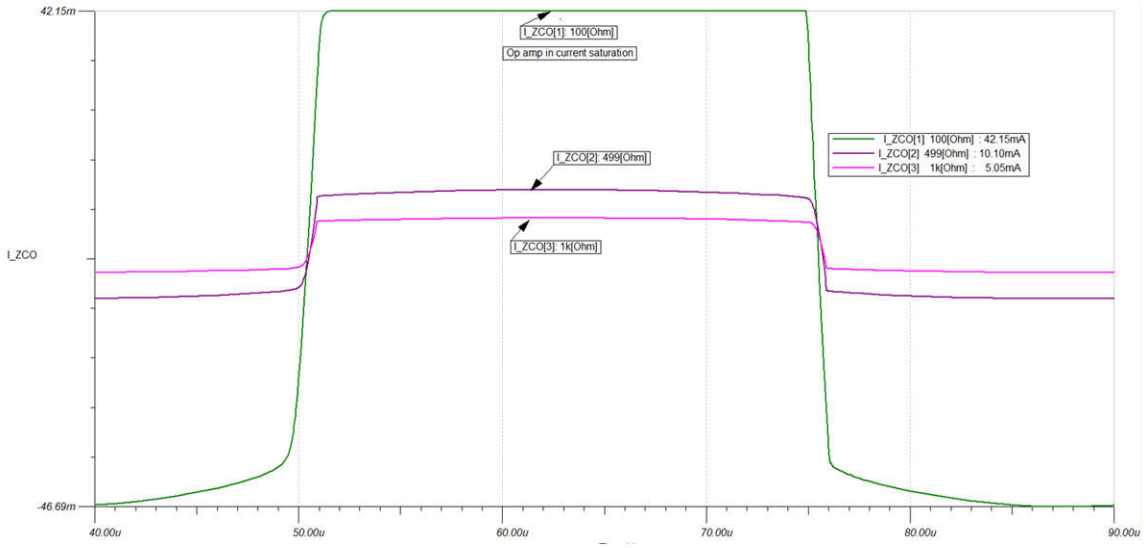


OPA462 Discrete Output Current Boost R_{ZCO} TINA Circuit

Note

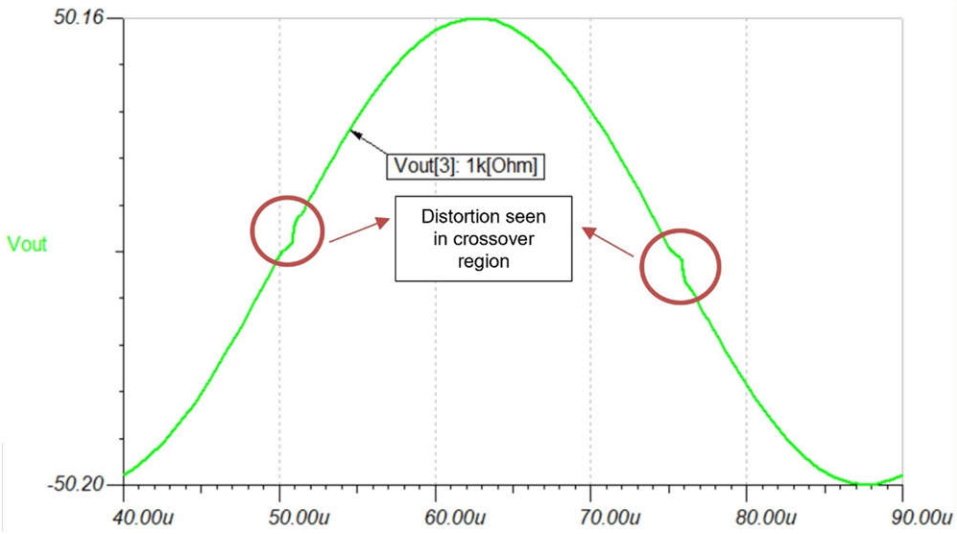
The SPICE model FDD5N60NZ was used for modeling as there is no model available for the 500V version of the NMOS. The characteristics are similar enough to provide a close approximation for simulation results.

TINA simulations are run originally without the voltage divider as part of the circuit. This allows for insight into the optimized value of R_{ZCO}. Later we will add a voltage divider to the circuit to further optimize crossover distortion.



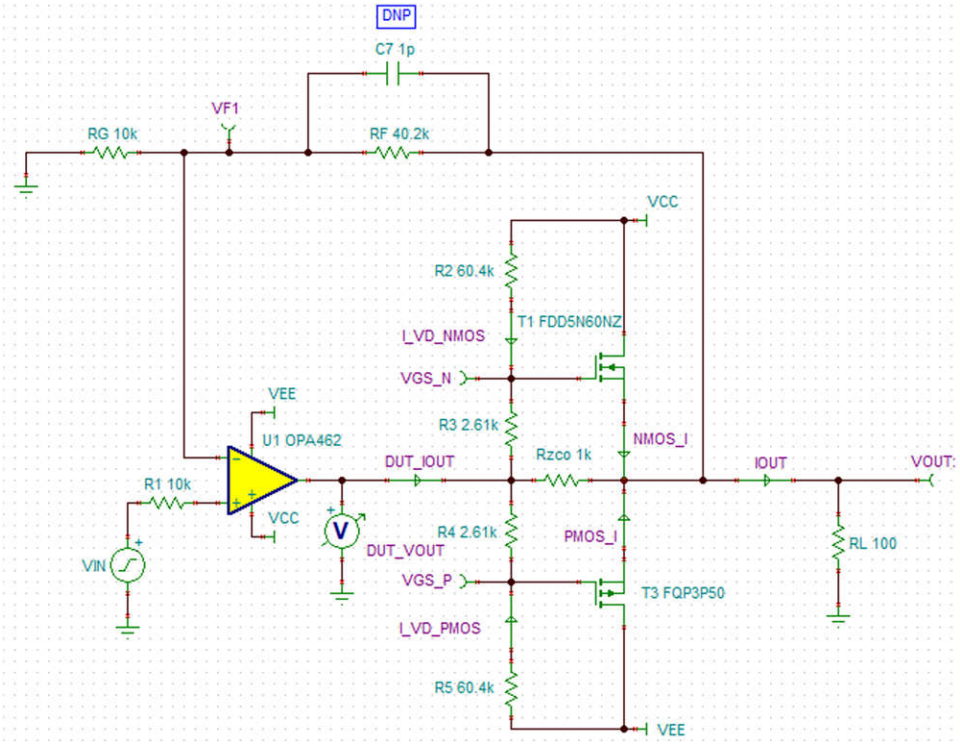
Simulation Results for R_{ZCO} and Corresponding I_{ZCO} Values

A $10V_{PP}$ square wave is applied to the input of the circuit. The output response provides insight into the current driving the load when the MOSFETs are turned off. Selecting R_{ZCO} resistors that are too low (100 Ω, 499 Ω) result in excessive current flow (labelled I_ZCO) from the output of the amplifier. Here, 1kΩ was chosen for R_{ZCO} as it adds 5 mA of current to the circuit, as opposed to the 10 mA of current consumption with the 499Ω resistor (see Simulation Results for R_{ZCO} and Corresponding I_{ZCO} Values). Furthermore, the noise difference between the 499Ω resistor and the 1kΩ resistor is minimal, making 1kΩ a preferred choice for R_{ZCO}. A larger resistor can be used but adds additional noise to the circuit.

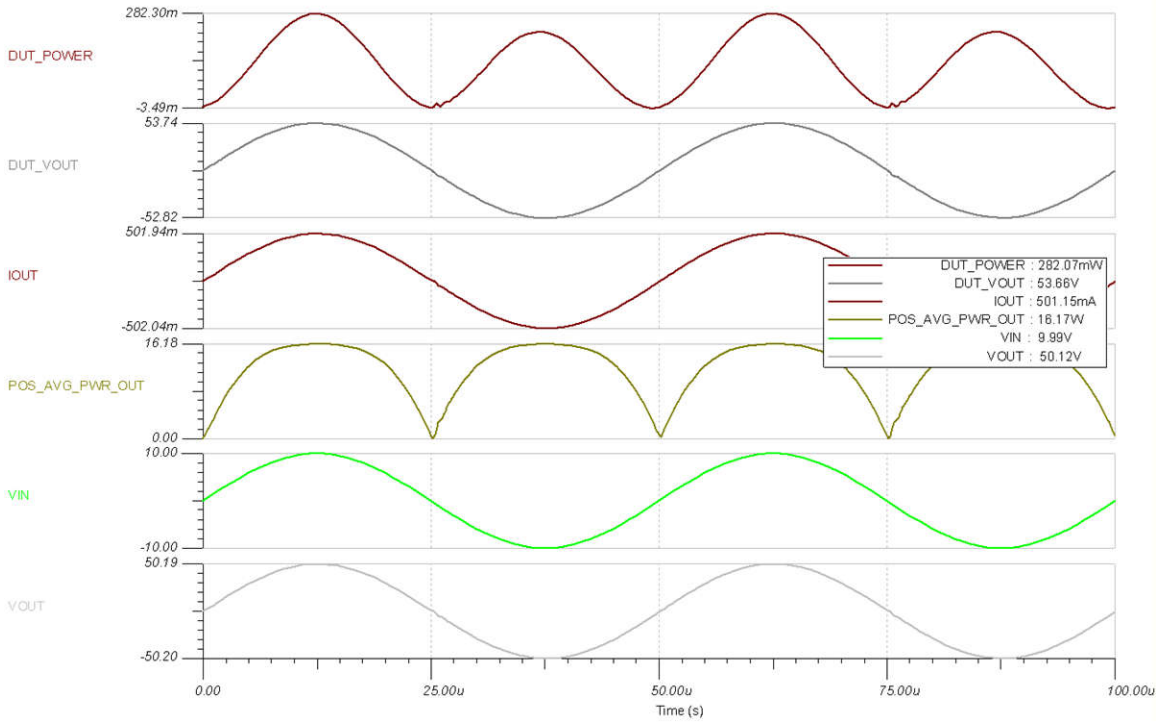


Simulation Results for V_{OUT} Distribution for R_{ZCO} = 1 kΩ

The distortion is minimized with R_{ZCO} = 1kΩ, but there is still crossover distortion in the circuit. Adding a voltage divider to the circuit allows for further optimization, as seen in the OPA462 Discrete Output Boost TINA Circuit figure.



OPA462 Discrete Output Current Boost TINA Circuit



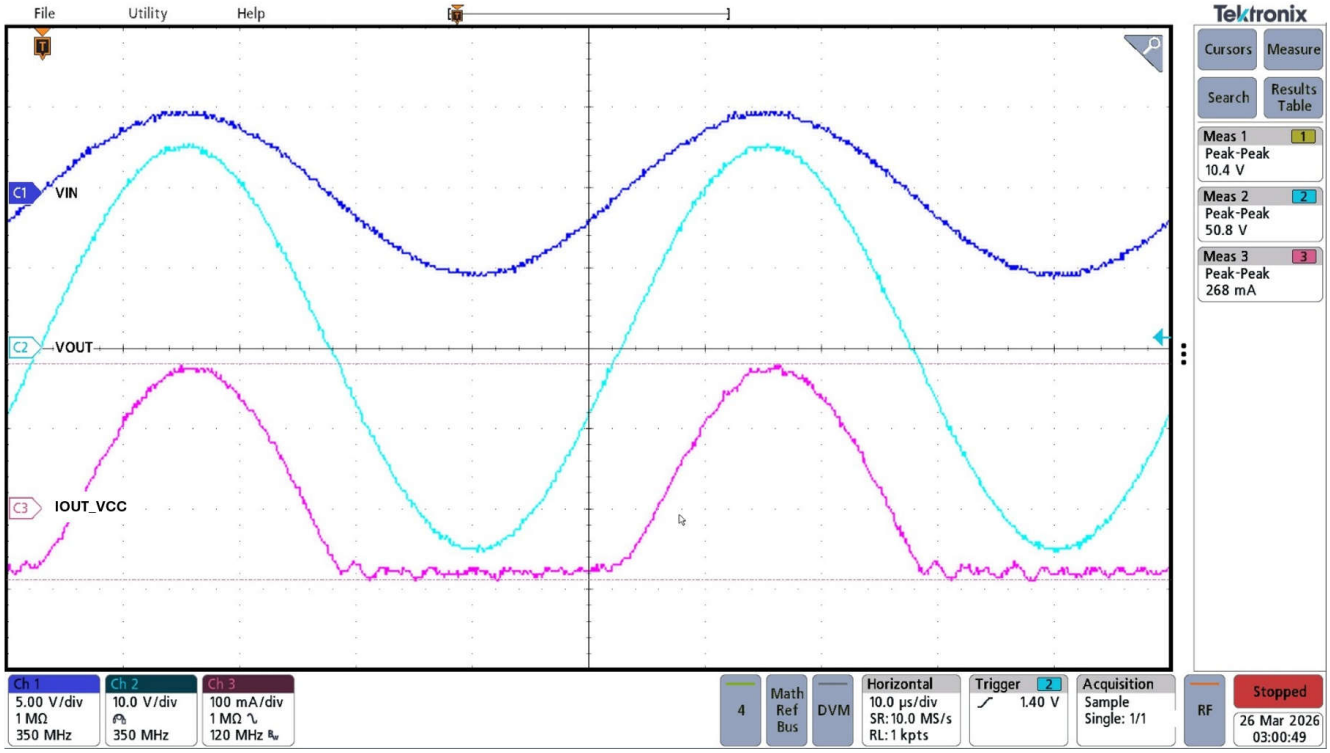
OPA462 Discrete Output Current Boost Circuit Simulation Results

The voltage divider was added to the circuit and further minimizes cross over distortion on the output of the circuit. The post processor in TINA is used to calculate the average output power of the circuit. Additionally, the post processor is used to show the output power of the OPA462 is minimal, approximately 300mW (labeled DUT_POWER).

Design Measured Results

R_3 was iteratively increased to find the optimal value for minimal crossover. A value of $R_3 = R_4 = 2.67k\Omega$ was found to optimize the circuit while allowing for minimal distortion. See below for oscilloscope results for the circuit.

Input			Output	
V_{IN}	Bandwidth	Gain	V_{OUT}	I_{OUT}
10 V_{PP}	20kHz	5V/V	50V_{PP}	500mA

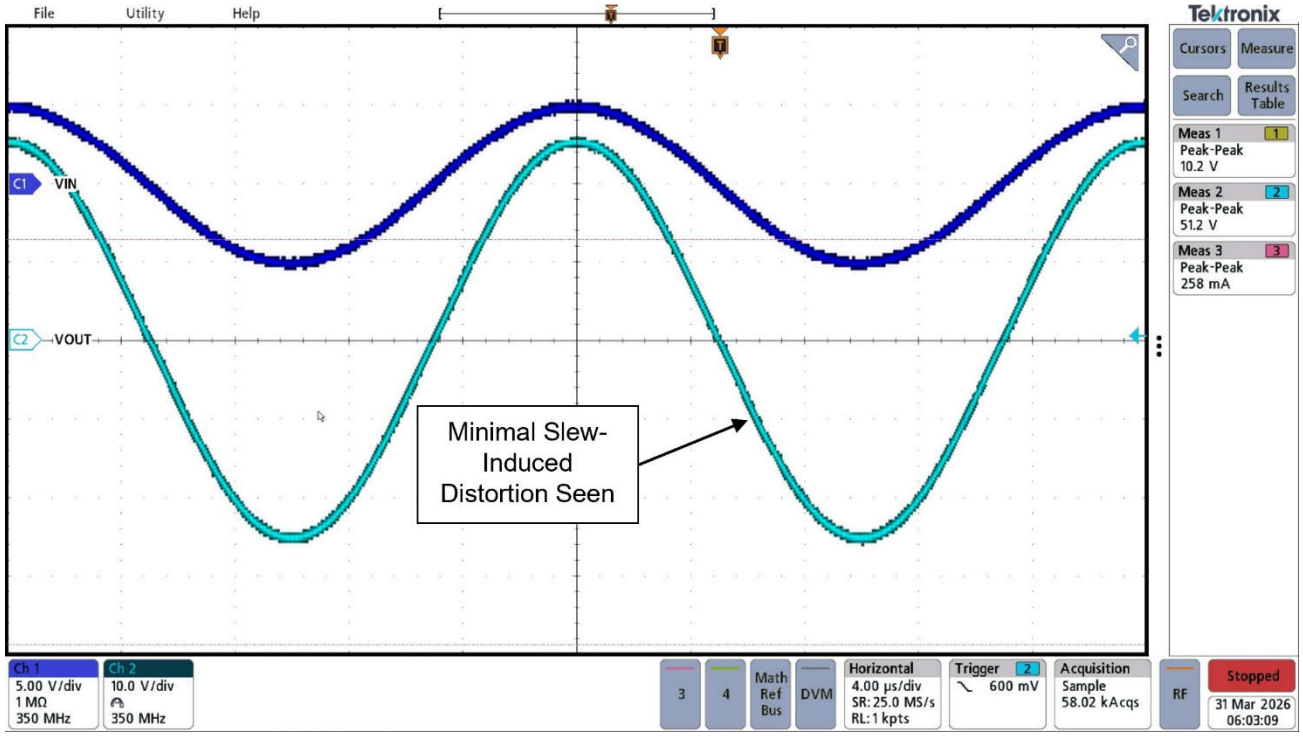


OPA462 Discrete Output Current Boost Circuit Measured Results (V_{IN} = 10V_{PP} @ 20 kHz)

Note

The IOUT_VCC measurement is measured from VCC. No visible distortion is seen at VOUT.

Input			Output	
V_{IN}	Bandwidth	Gain	V_{OUT}	I_{OUT}
10V_{PP}	50kHz	5V/V	50V_{PP}	500mA



OPA462 Discrete Output Current Boost Circuit Measured Results (V_{IN} = 10V_{PP} @ 50 kHz)

Note

Minimal slew-induced distortion is seen at VOUT, but the amplitude of the sine wave is not affected.

Target Applications

- High Voltage/High Signal Generator
- Parametric Measurement Unit
- Source Measurement Unit

Design Featured Devices

OPA462	
V_{SS}	12V to 180V
V_{OUT}	(V-) + 3 to (V+) -1.5 (with R_L = 10kΩ)
V_{OS}	3.4mV
I_Q	3.2mA
Unity Gain Bandwidth	6.5MHz
Slew Rate	32V/µs
OPA462	

Design Alternative Devices

OPA455	
V_{SS}	12V to 150V
V_{OUT}	(V-) + 3 to (V+) -1.5 (with R_L = 10kΩ)
V_{OS}	3.4mV
I_Q	3.2mA
Unity Gain Bandwidth	6.5MHz
Slew Rate	32V/µs
OPA455	

Design References

1. Texas Instruments, OPA462 Discrete Output Current Boost Circuit, TINA-TI simulation files SBOMCU1
2. Texas Instruments, OPA462 TINA-TI Spice Model

Additional Resources

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