Application Note

Create Automated SPICE Designs Using PSpice-for-TI

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ABSTRACT

Texas Instruments offers two SPICE simulation tools to help evaluate the functionality of analog circuits, TINA-TI and PSPICE-FOR-TI. TINA-TI is a nimble program that allows the user to quickly assemble a schematic and analyze the response of the circuit. PSpice®-for-TI is designed for larger-scale circuit analysis as the ecosystem remembers all post-processor settings (several complex traces and equations).

This document provides information to teach a new user; all terms covered in this abstract are defined later.

Once a procedure for a simulation problem is established, PSpice®-for-TI only has to be setup once. The circuits, simulation profiles, output window setup of plots and traces, and key measurements are saved to the project. The upfront investment is fruitful the more the project is opened and reused.

This application note discusses the creation of an automated SPICE design for stability regarding an operational amplifier (op amp). This process can be replicated for any evaluation that is SPICE-dependent and requires repeat circuit analysis.

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Trademarks

1 Introduction

The two input nodes of an op amp must be equal to one another and the output changes accordingly to make this happen. When there are components that introduce delay (or phase lag) between the output response and the inverting feedback node (IN-), the output shows an unstable oscillating response trying repeatedly to settle to the correct value.

In Figure 1-1, the expected response is 100mV but the output of the op amp initially overshoots and then over/under corrects - resulting in oscillation in the output.

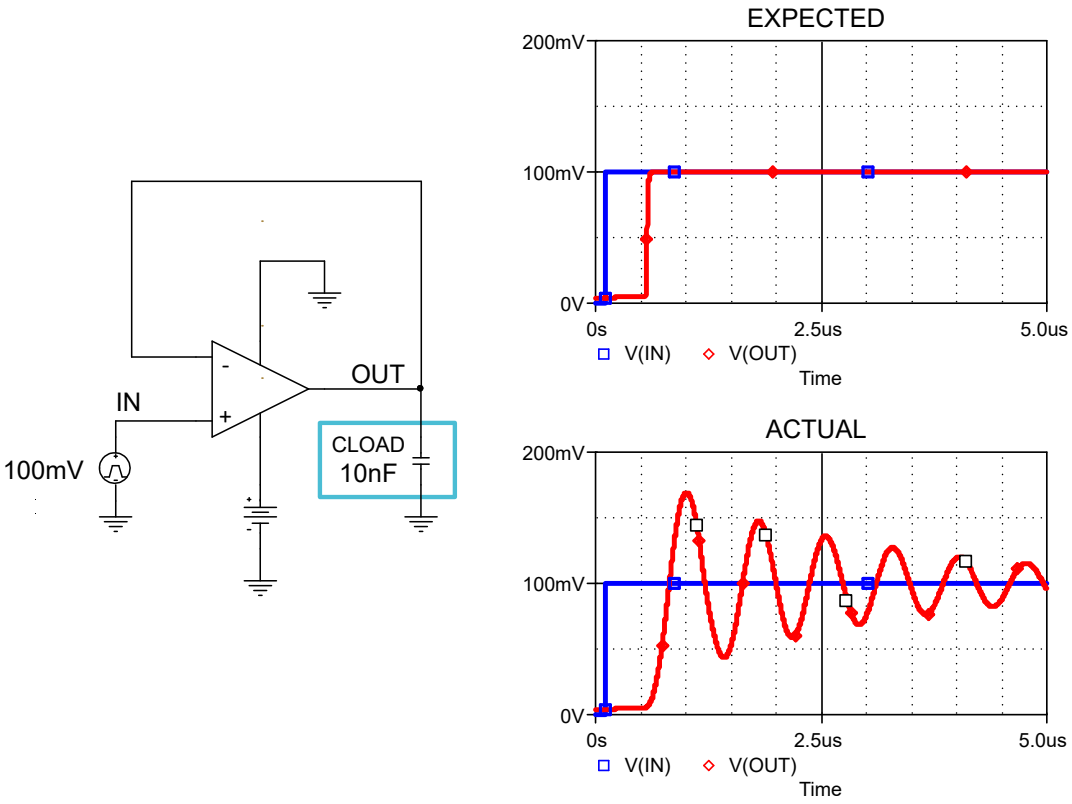

Figure 1-1. An Unstable Op Amp Circuit Response

Some ways that phase lag is commonly introduced in the feedback network are the output impedance of the op amp and a capacitive load or the input capacitance of the op amp and a large feedback resistor. Figure 1-1 shows an example of a large capacitive load causing instability. For additional information of stability compensation theory, see TI's Precision Labs training: TIPL Stability video series.

Stability compensation components are introduced to the circuit to achieve a stable output response (between 45˚ to 90˚ of phase margin). To find the appropriate stability compensation values, the following must be done for each op amp and circuit configuration:

1. Build a simulation schematic in pseudo open-loop configuration.
2. Run an AC sweep.
3. Plot the open loop gain and phase of the circuit and measure phase margin.
4. Calculate compensation values using parameters from the frequency response.
5. Implement the compensation value and rerun the AC sweep to see if the desired phase margin (45° to 90°) is achieved.

This procedure requires a significant amount of post-processing calculations and rerunning of AC sweeps. PSpice®-for-TI simplifies this procedure by remembering the setup of output window plots, key measurements such as phase margin, and equations for determining compensation values using the frequency response and a parameter from the schematic. This document shows how to solve this repeatable problem with an automated design built in PSpice®-for-TI.

2 A Reusable Schematic

Once a repeatable procedure is identified, the next step is to find a schematic configuration that works for a majority of circuit configurations.

In this example, the most robust open loop configuration for op amps is the *double-break* shown in Method 3 which accounts for interaction between output impedance of the op amp to the feedback network (disadvantage of Method 1); and interaction between the feedback network and the parasitic impedance of the inputs (disadvantage of Method 2).

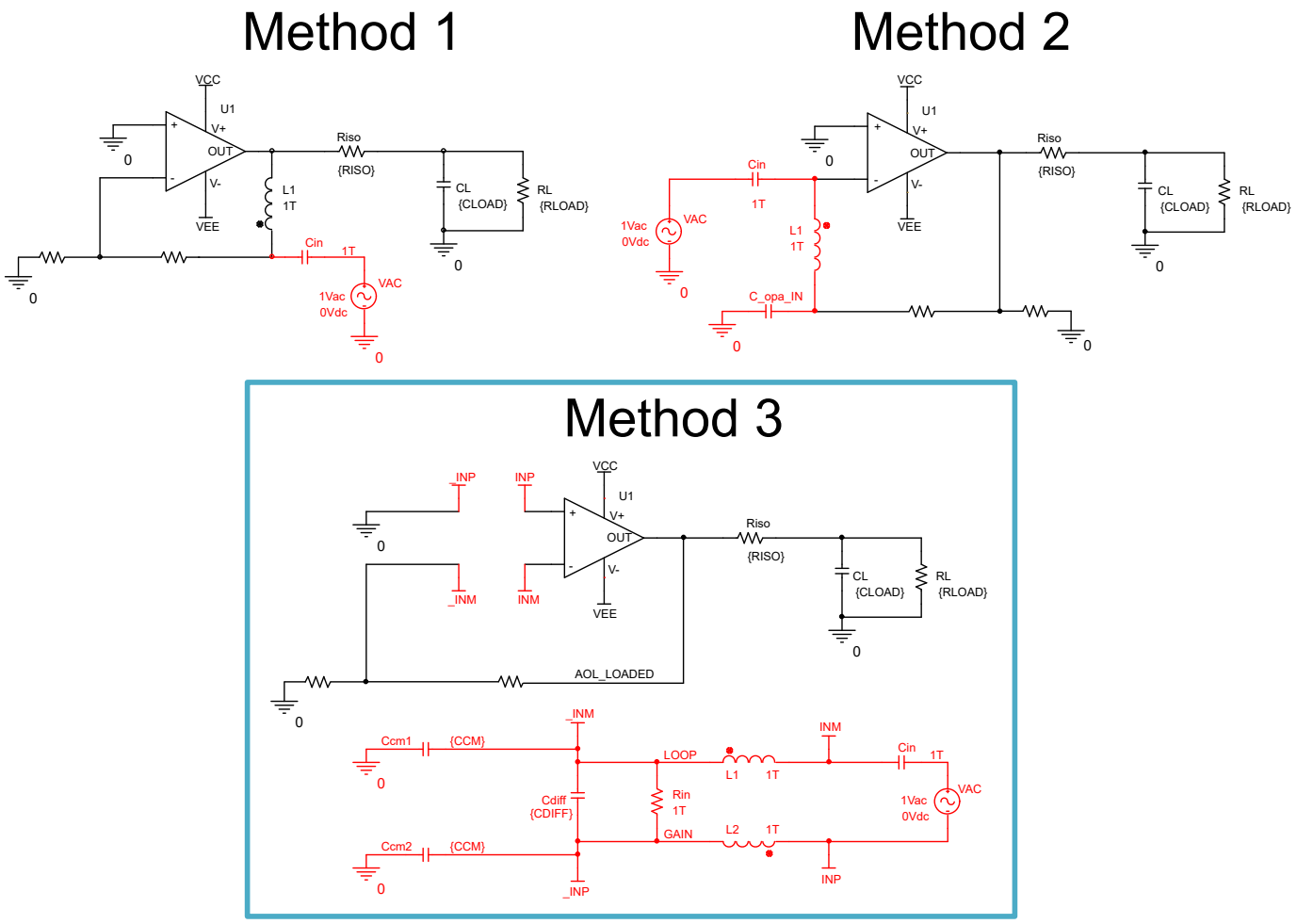

Figure 2-1. Methods for Pseudo Open-Loop Configuration for Op Amp Circuits

Method 3 is a preferred choice for PSpice®-for-TI's re-usability as the main drawback is the complexity in the schematic in setup. For additional information on this method, see "Breaking loop on differential amplifier" video on ti.com.

3 Create a Project

The instructions in this document assume the user is new to the Cadence environment and walk through the creation of an automated project from the beginning.

If the user has created a project and schematic in PSpice®-for-TI before, there is an option to skip forward to Section 4.5.

A new project can be created through *File* > *New* > *Project*.

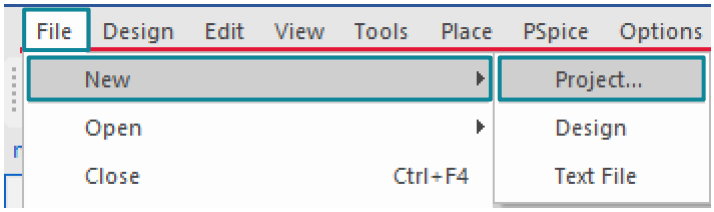

Figure 3-1. New Project Selection

Select a location and a name for the new project, and *OK* to continue. For best practice, each PSpice®-for-TI project is placed in a new folder.

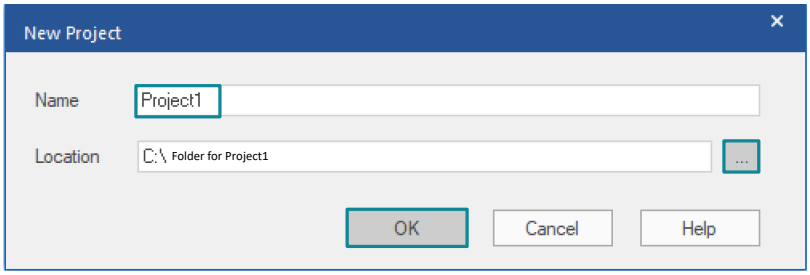

Figure 3-2. New Project Creation

When prompted, select *Create a blank project* and *OK* to continue. Note that the *Create based upon an existing project* can be helpful in the development of multiple automated projects; however, this is beyond the scope of this application note.

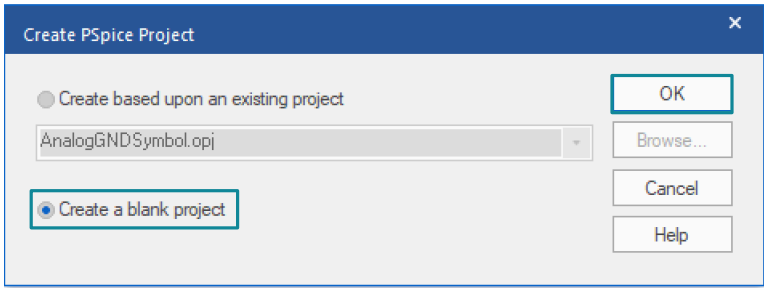

Figure 3-3. Project Template Selection

3.1 Project Hierarchy

The Cadence environment includes a project (.opj) that contains a design (.dsn) which can have multiple schematics. Each schematic can contain multiple pages and can have multiple simulation profiles associated.

In the example shown in Figure 3-4, the *non-inverting. opj* is a project that includes the design file, *non-inverting.dsn*. This design file includes six schematics, of which, *RISO_DF* contains two schematic pages and has one AC simulation profile labeled *RISO_DF_ac*.

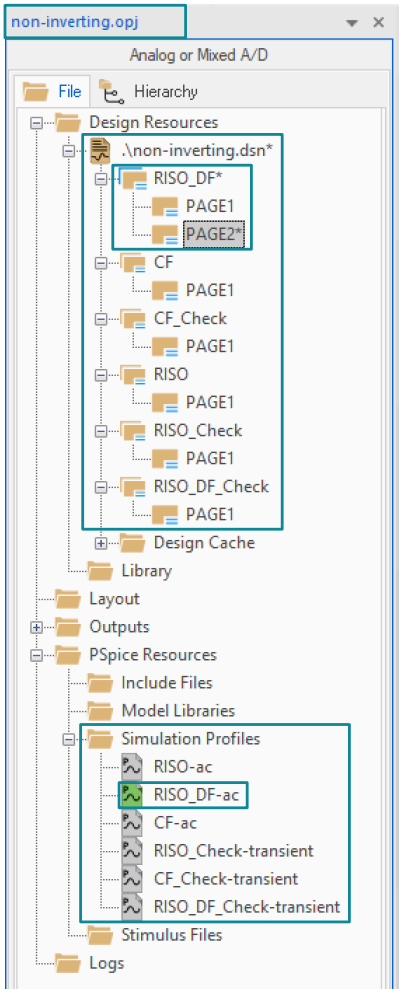

Figure 3-4. Project Hierarchy

4 Schematic Drawing for Increased Readability

There are best practices within PSpice®-for-TI's schematic editor that allow for simplicity of use for a larger audience. The following steps discuss how to assemble a schematic that is read by multiple users and as a result, must be intuitive.

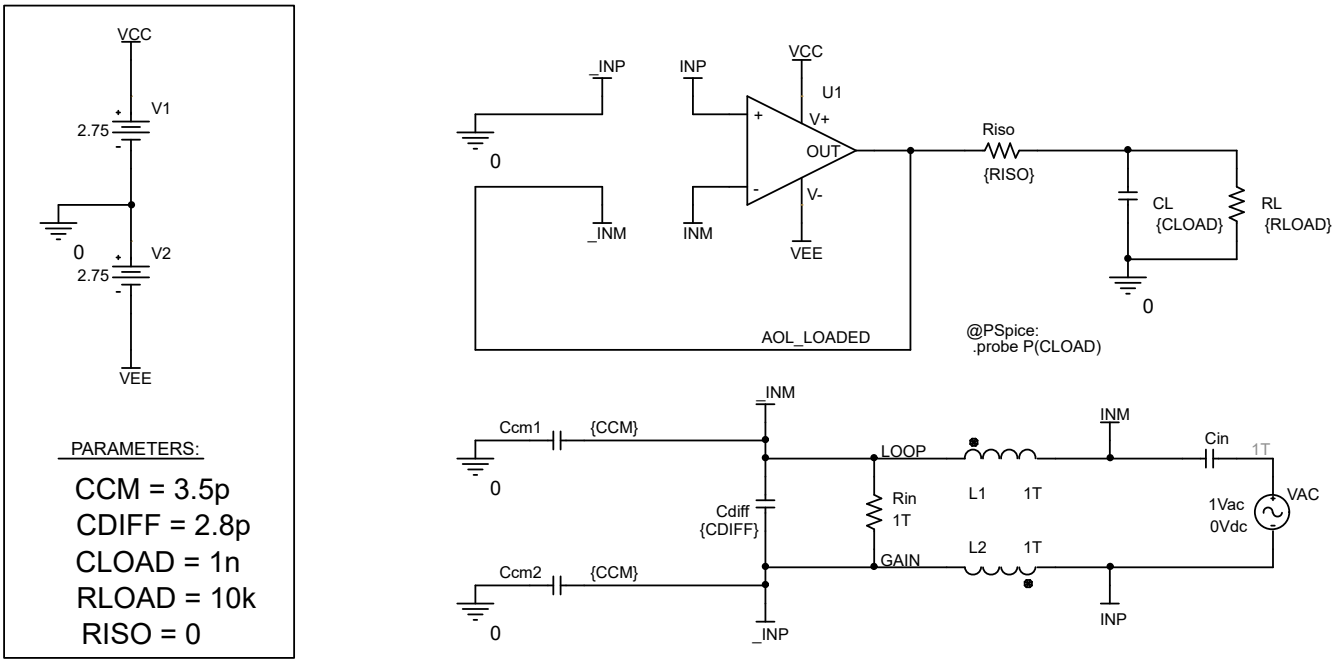

Figure 4-1. Final Schematic

4.1 Placing Passive Components

A passive component can be placed by navigating through *Place* > *PSpice Component* and selecting the relevant component. In the example shown in Figure 4-2, a resistor is placed in the schematic.

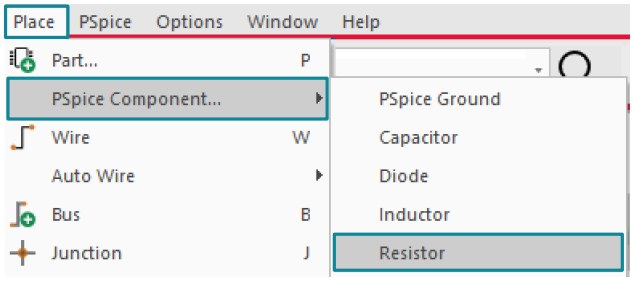

Figure 4-2. Placing a Resistor

Figure 4-3 shows R1 (a previously placed component), R2 (highlighted in pink as the last placed component), and a hovering unnamed component where the mouse is. Press *ESC* to stop placing multiple components.

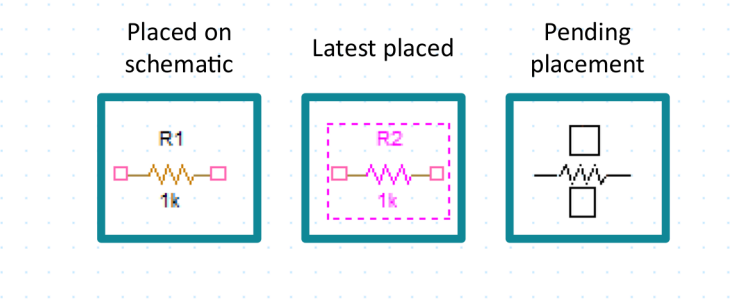

Figure 4-3. Multiple Placements

Once placed, a component value can be edited by double clicking on the value.

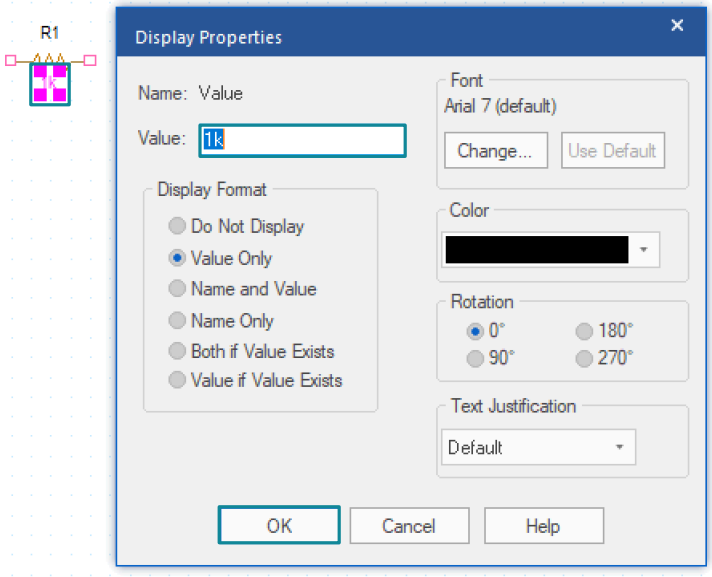

Figure 4-4. Changing a Single Value

Type the new value and select *OK* to implement.

4.2 Parameters

If a variable is used in many locations, the variable can be implemented in the schematic as a parameter. Through the PSpice® Part Search (built in library), which can be accessed through *Place* > *PSpice Component…* > *Search…*, search for PARAM and double-click to place on schematic.

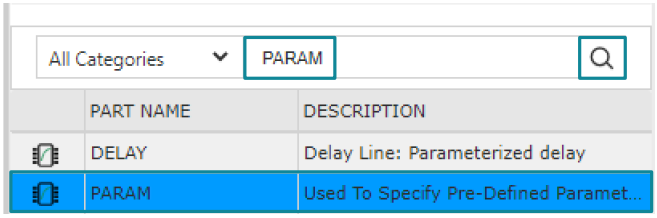

Figure 4-5. "PARAM" for variables

Press “ESC” to stop multiple placements. Figure 4-6 shows the *PARAM* component placed on the schematic.

Figure 4-6. *PARAM* Component on Schematic

Once placed, double-click on the *PARAMETERS* component to open the *Property Editor* in another tab. Optionally, to display properties in a vertical fashion, as seen in Figure 4-7, select *Pivot*.

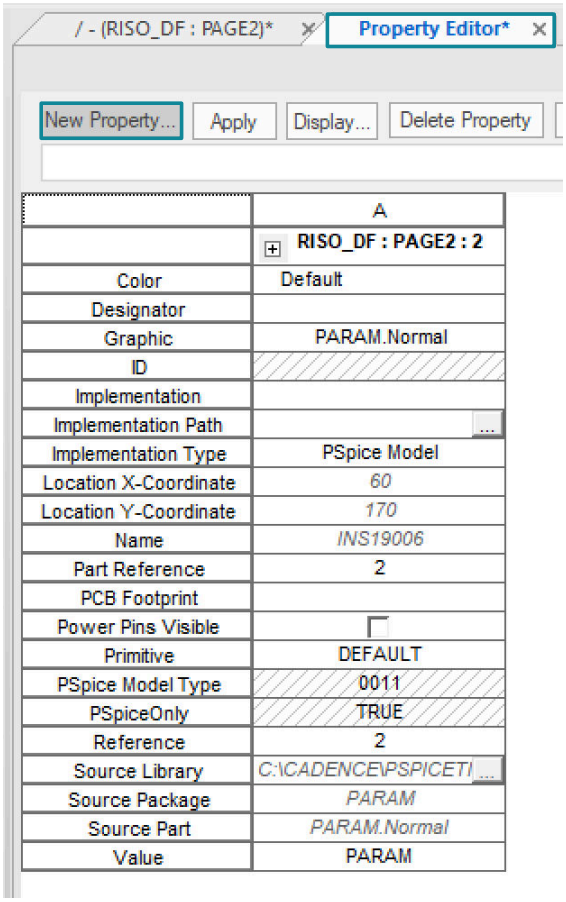

Figure 4-7. Property Editor for *PARAM*

Select *New Property…* and select a name and a default value for the parameter as seen in Figure 4-8. Select the checkbox *Display [ON/OFF]* to show the new parameter in the schematic. Select *Apply* to continue to add multiple parameters. Alternatively, select *OK* to add only one parameter.

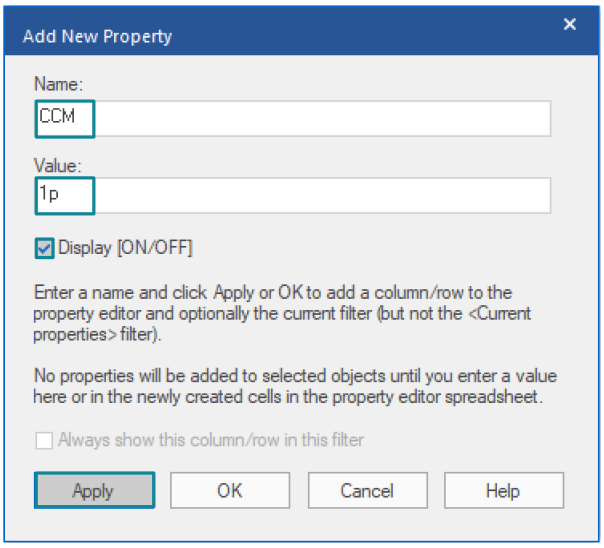

Figure 4-8. Add New Property to *PARAM*

The selection of *Display [ON/OFF]*, allows the user to choose display settings. Select the *Display Format* to be *Name and Value*. The default font and size, Arial 7, is small when presenting on a projector. For an automated project, commonly used parameters can be simple to find in a schematic if implemented with a larger font size. In the example shown in Figure 4-9, font size of 12 was selected.

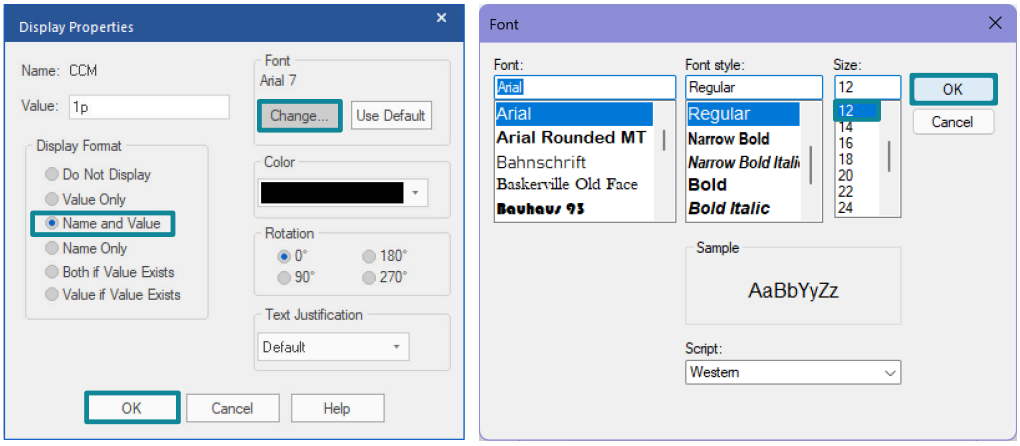

Figure 4-9. Display and Sizing of Parameters

As previously mentioned, if adding multiple parameters, select *Apply* and create as many new parameters as the project requires. Figure 4-10 shows different parameters that were added and the default value of each parameter.

PARAMETERS:
CCM = 1p
CDIFF = 3p
CLOAD = 1u
RLOAD = 10k
RISO = 0

Figure 4-10. Multiple Parameters

Once a parameter is declared in the schematic, the user can *call* the parameter by placing curly brackets around the name in the *Value* of a component. In Figure 4-11, the value of R1 is changed from 1kΩ to the variable value corresponding to the parameter RISO.

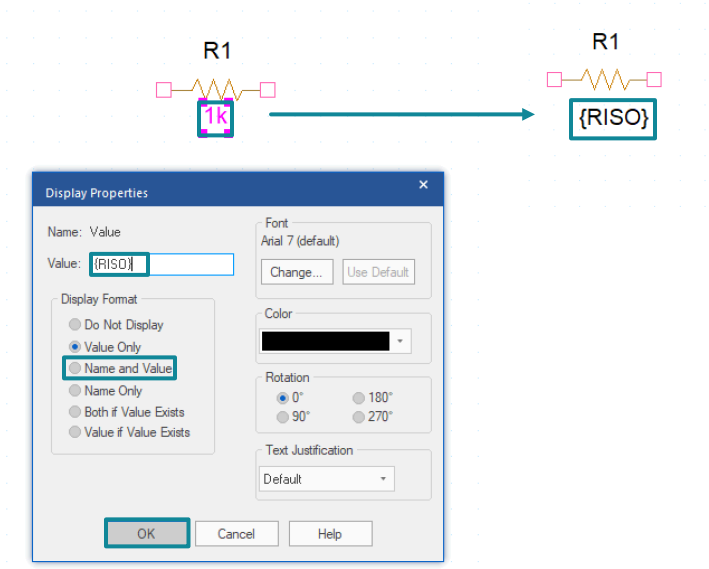

Figure 4-11. Add a Parameter as a Part Value

If there are commonly used names for the components in a circuit, change the *Part Reference* to reflect that.

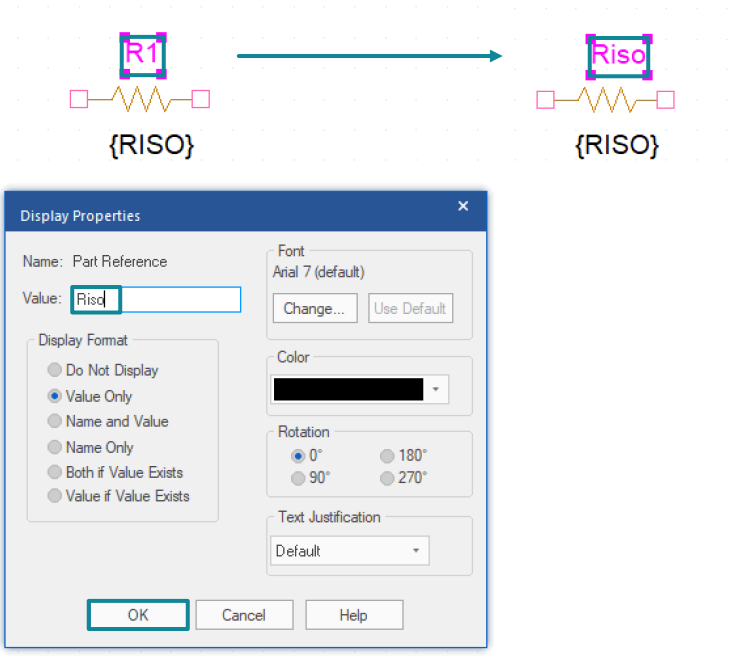

Figure 4-12. Rename a Part Reference

A probe is added for the parameter to be *called* in the output simulator window. To add a probe to a parameter, the following text must be added in the schematic through *Place* > *Text* or keyboard shortcut T, *@PSpice: .probe P(parameter name*). The use-case for this implementation is when a parameter is needed in post-processing equations, discussed in detail in Section 5.2. In Figure 4-13, the parameter used in calculations was *CLOAD*, this procedure can be repeated for multiple parameters as needed. The font size was increased to 12.

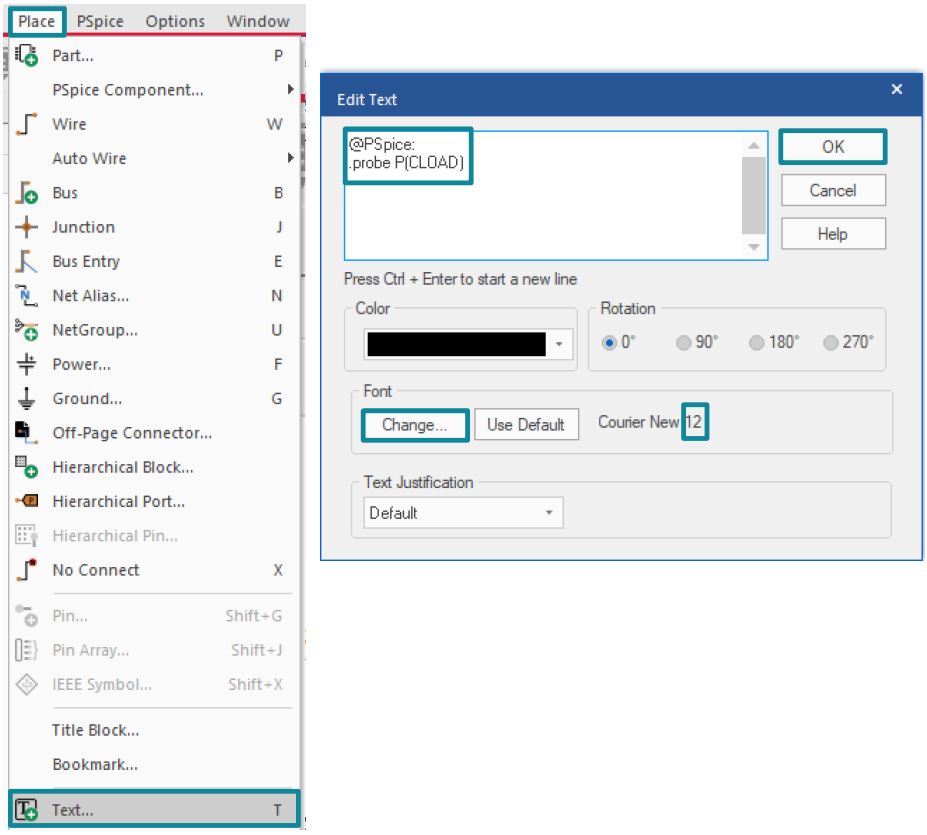

Figure 4-13. Parameters Used in the Output Simulation Window

4.3 Place Power Supplies

DC power supplies can be placed through, *Place* > *PSpice Component…* > *Source* > *Voltage Sources* > *DC*.

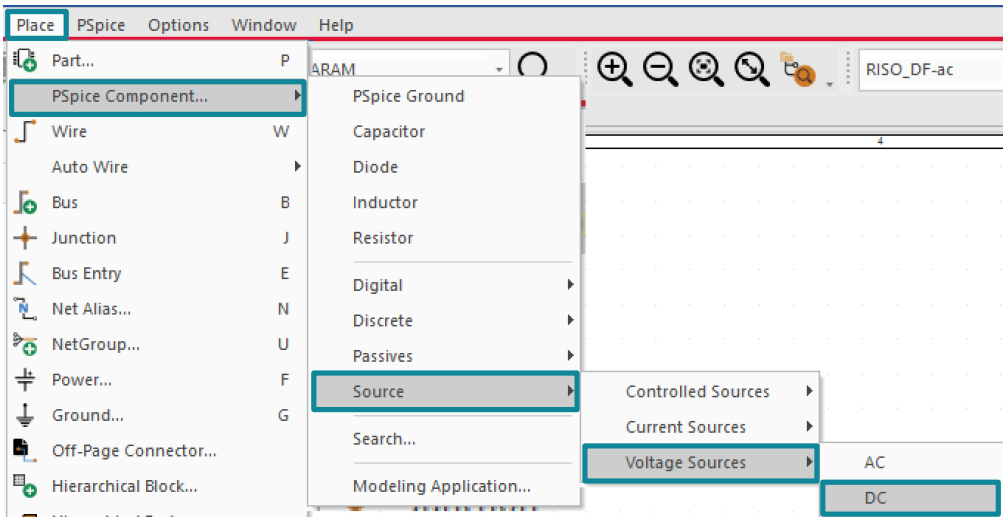

Figure 4-14. Placing DC voltages

Once power supplies are placed, the power net can be placed in multiple places in the schematic to use that power supply. The power components are located in *Place* > *Power…* or keyboard shortcut F. Multiple symbols are available, the example in Figure 4-15 uses *VCC_BAR*.

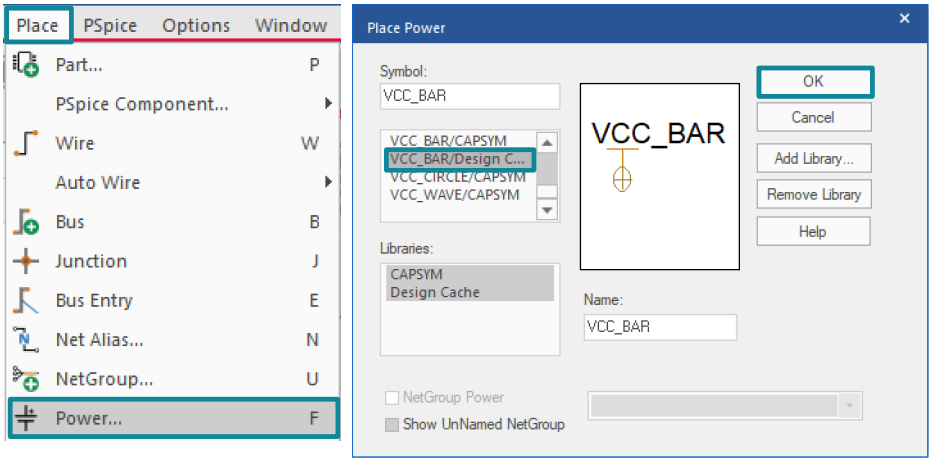

Figure 4-15. VCC_BAR

4.4 Wiring

A wire is placed through *Place* > *Wire* or keyboard shortcut W. Click on the schematic to begin placing a wire, every click allows for a change of direction. To connect two components together, simply click on the square connectors.

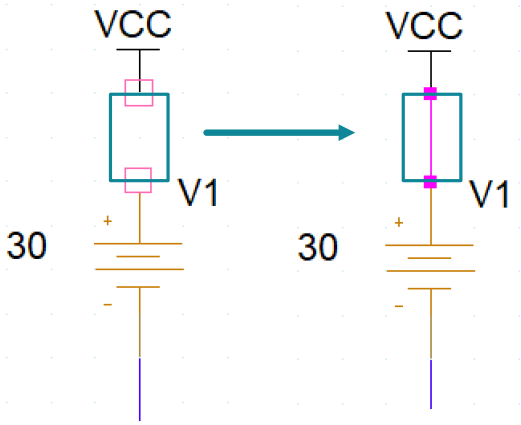

Figure 4-16. Wire Placement

Once wires have been placed, PSpice®-for-TI assigns an alphanumeric net alias to each wire. For important wires, rename the net alias to a recognizable name. A net alias is placed through *Place* > *Net Alias* or keyboard shortcut N. Type an alias and select *OK* to place. Net aliases only place on pre-existing wires and can also be used to connect two wires together without physically connecting them.

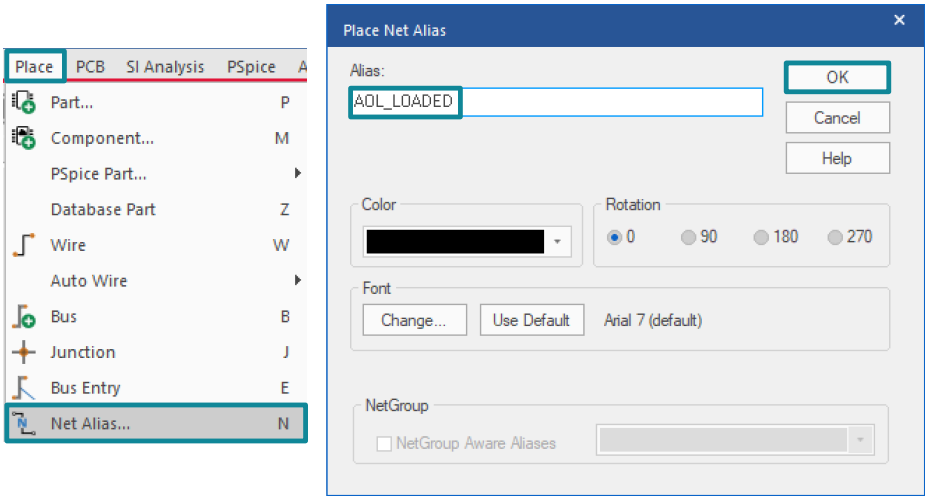

Figure 4-17. Labeling nets

4.5 Organizing for the User Experience

Once all the components have been placed, named intuitively, and wired together, the user experience must be considered. What is obvious to the author is often subtler to a brand-new user; therefore, labeling and isolating portions of the project allows direction for a new user.

In the example, the only variables that need to be changed by the user are located inside the box on the left of Figure 4-18. The schematic connections on the right interact with the user-dependent variables (parameters) but have less chance of being overwritten in the actual schematic.

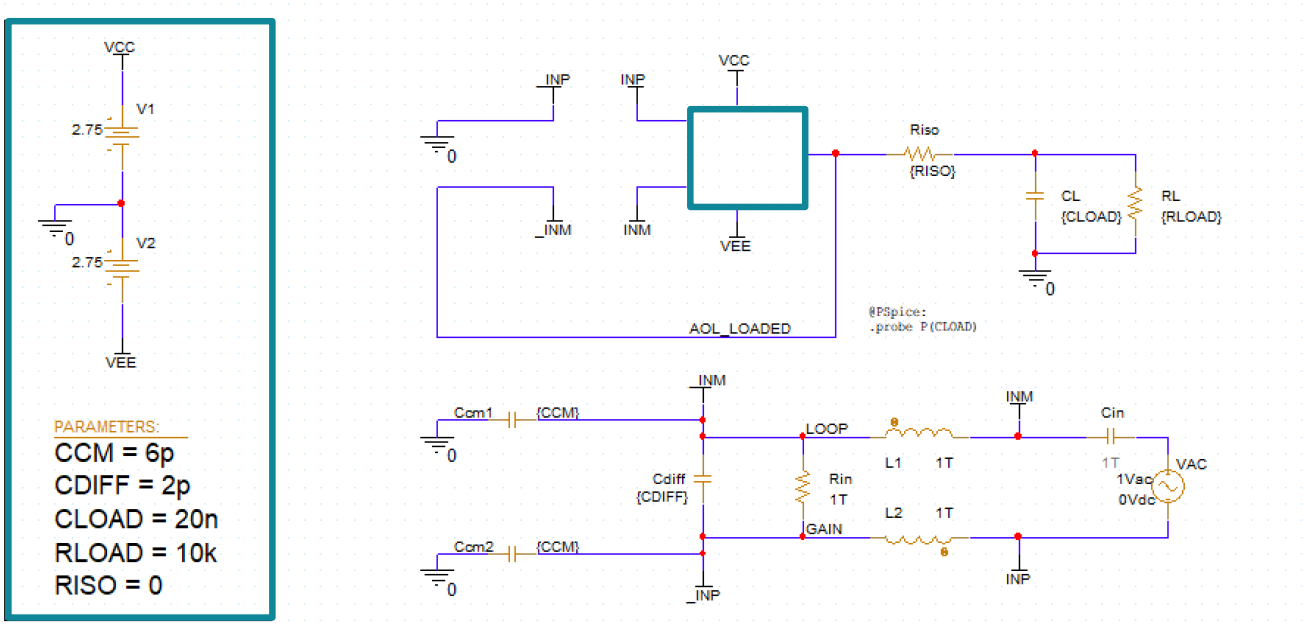

Figure 4-18. Minimize User Interaction

The last user interaction to the circuit is op amp placement in the middle of the schematic of Figure 4-18. A part can be placed from the PSpice® Part search (similar to a parameter), by navigating through the *Texas Instruments* > *Amplifiers* > *Operational amplifiers (op amps)* or through the search (located next to the *All Categories* drop-down menu with the magnifying glass). A wildcard can be used in the search as an asterisk (*). Double-click to place.

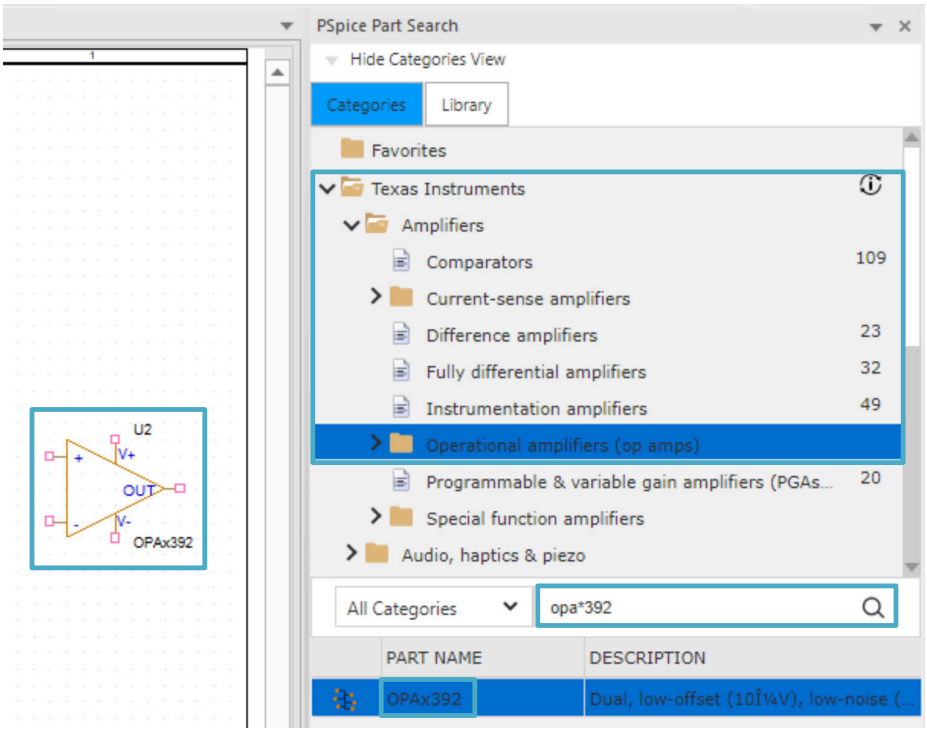

Figure 4-19. Place a TI Component through the Integrated Library

Over 90% of the TI's op amp portfolio place with the same pin-orientation seen in Figure 4-19, non-inverting input (IN+) and positive power supply (V+) oriented at the top. The schematic was drawn in a way that allows the user to simply drop-in,as seen in Figure 4-20, without having to rotate or mirror.

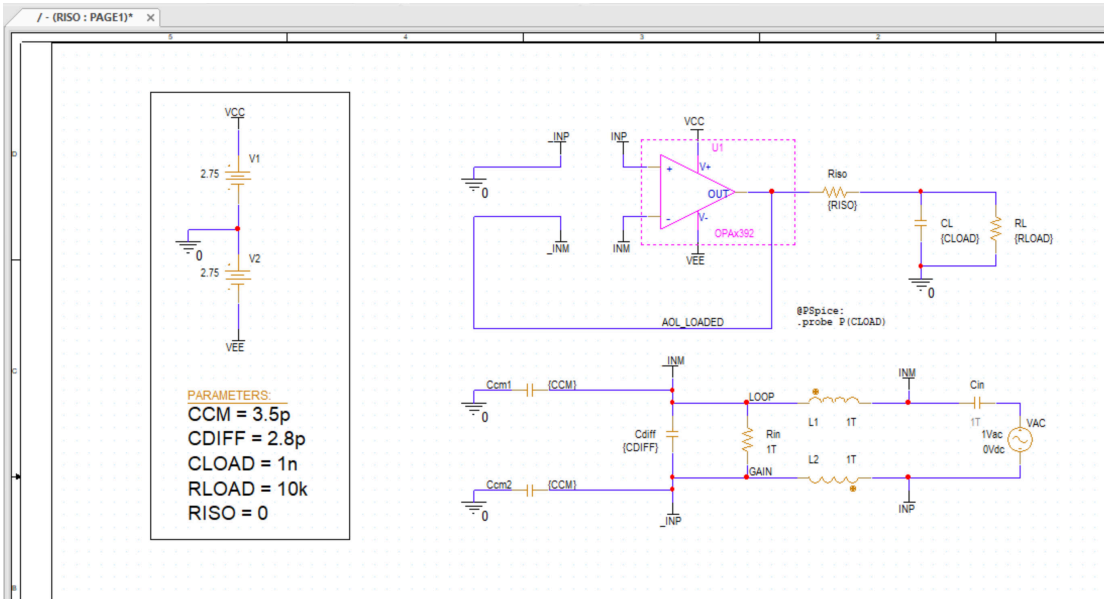

Figure 4-20. User Placement Without Modification

5 Simulation Profile Setup

Once the schematic is complete, the next step is to create a simulation profile.

If the user has created a simulation profile in PSpice®-for-TI before skip forward to Section 5.1.

To create a new simulation profile, navigate to *PSpice* > *New Simulation Profile* or through the new simulation profile icon in the taskbar shown in Figure 5-1.

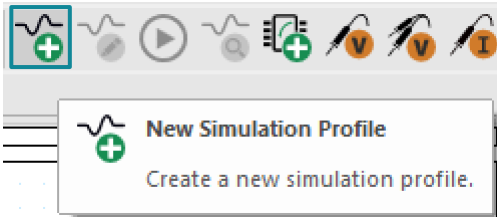

Figure 5-1. New Simulation Profile Icon

Name the simulation profile a representative name for ease of recognition. In Figure 5-2, the simulation is named *ac* to stand for an AC sweep. Select *Create* to continue.

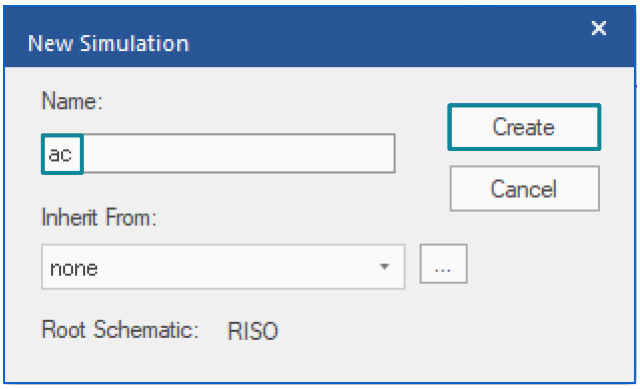

Figure 5-2. Name the New Simulation Profile

In the example, the analysis is done in the frequency domain; as a result, an *AC Sweep/Noise* is selected as the Analysis Type in the Analysis tab. The frequencies of interest depend on the bandwidth of the amplifier, in the example a frequency sweep from 10Hz to 100MHz is run with 10 points per decade. PSpice®-for-TI requires the declaration of *MEG* for mega (10^6), *M* is recognized as milli (10^{-3}). Select *Apply* to save the settings on this tab.

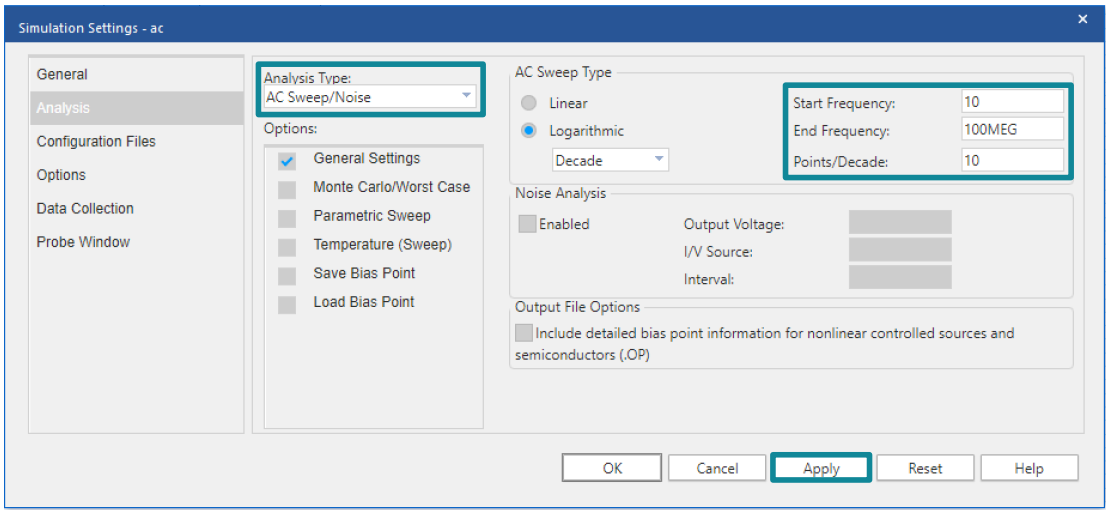

Figure 5-3. AC Sweep Setup

In the *Probe Window* tab, select to show *Last Plot* every time the simulation is run. The resulting factor is that the simulation profile saves the setup (plots and equations) in the probe window and is applied on every run. Select *Apply* and *OK* to exit simulation profile settings.

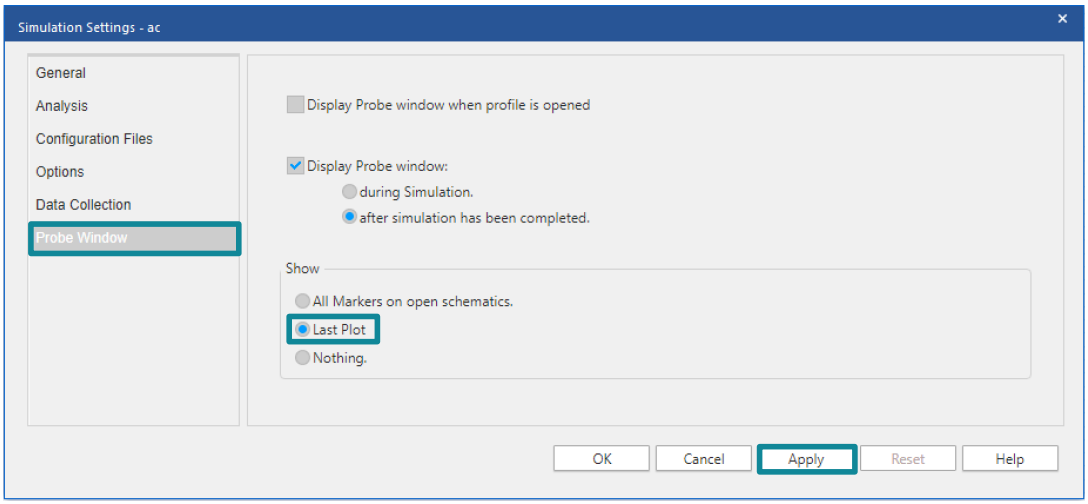

Figure 5-4. Last Plot

5.1 Aiding in Convergence

By default, PSpice®-for-TI does not have *AutoConverge* turned on. If there are convergence issues, check the datasheet of the device to verify setup and operation within the linear operating conditions of the device.

When working with complex projects the simulation takes a while (a couple of minutes) even within linear operating conditions of the device. *AutoConverge* can be turned on in the simulation profile settings to reduce the simulation time. Under the *Options tab* > *Analog Simulation* > *Auto Converge*, selecting the top *AutoConverge* text box selects all options below.

AutoConverge can reduce the accuracy of simulation or increase the amount of iterations as the program tries to reach convergence.

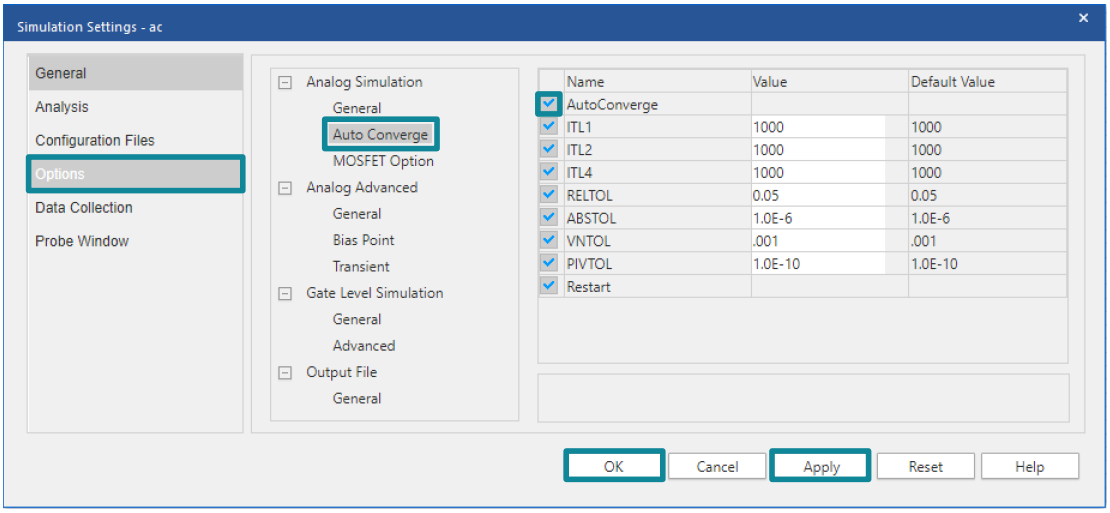

Figure 5-5. Auto Converge

Select *Apply* to save settings on a tab and *OK* to finish editing the entire simulation profile.

5.1.1 Modeling Application

Dependent on each project, the simulator can run into numerical limitations when calculating node voltages and currents.

For this example, the large (1T) capacitor next to the AC input must have a parasitic series resistance added to aid in convergence. This small series resistance provides a minimum capacitor impedance to avoid the simulator calculating very large currents through the capacitor.

There are two ways to implement this, (1) a resistor can be placed in series with the capacitor; or (2) a more elegant option is available in the *Modeling Application* through *Place* > *PSpice Component…* > *Modeling Application*. Under *Passives* in *Capacitor* set the *Capacitance* to *1T* and the *Series resistance (ESR)* to *1m*. This allows the AC simulation response to be smooth across all frequencies. The resulting placed capacitor is gray instead of black to highlight the modification.

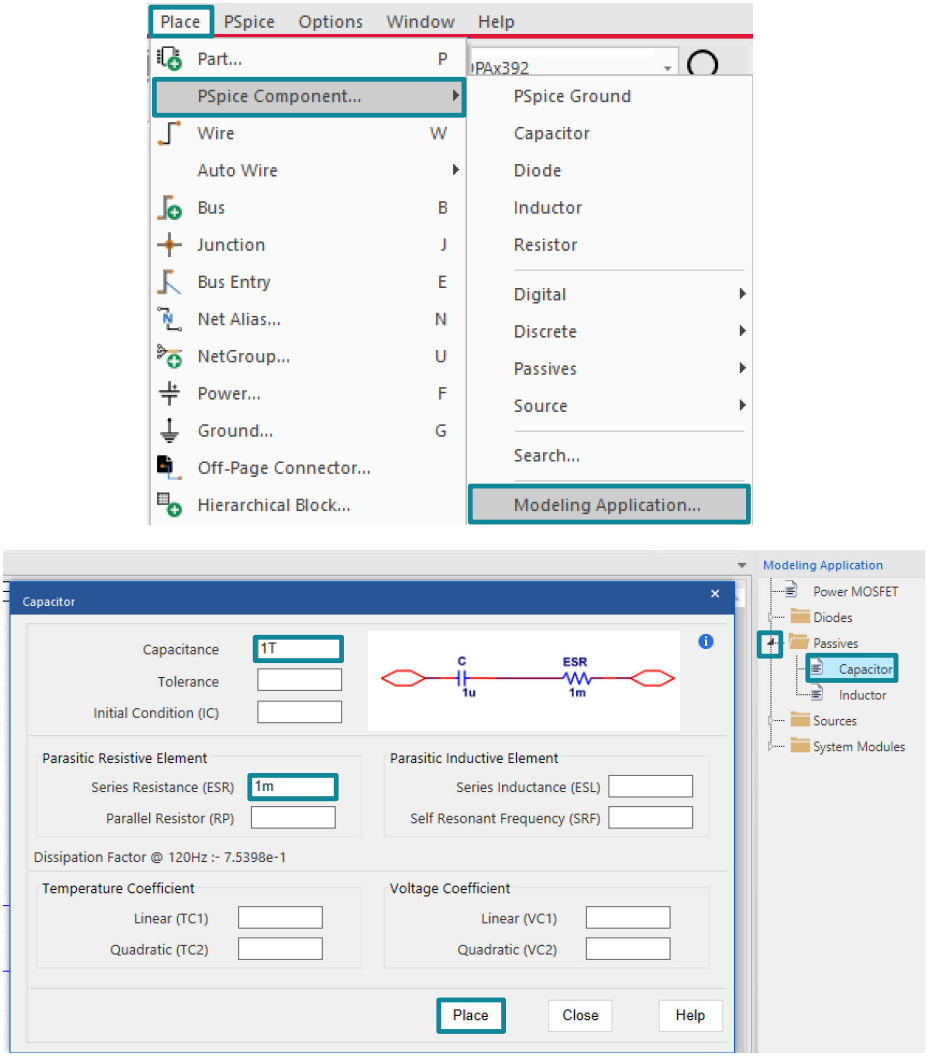

Figure 5-6. Modeling application

5.2 Powerful Post-Processing

Once the simulation profile has been created, by default the simulation profile is at the *top* of the hierarchy and shown as active. The active simulation profile is evaluated through *PSpice* > *Run* or keyboard shortcut F11.

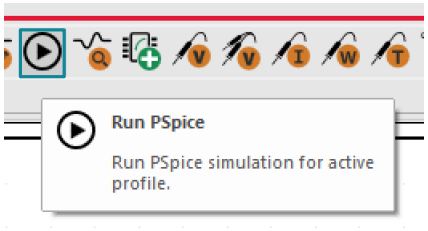

Figure 5-7. Run PSpice® Simulation Icon

The first time the simulation is run a longer wait time is expected than the subsequent runs as PSpice®-for-TI is updating the latest libraries from ti.com. A new window opens up and displays an empty plot as seen in Figure 5-8.

Figure 5-8. First Output is an Empty Plot

Multiple plots can be added by right-clicking on the plot and selecting *Add Plot* as seen in Figure 5-9.

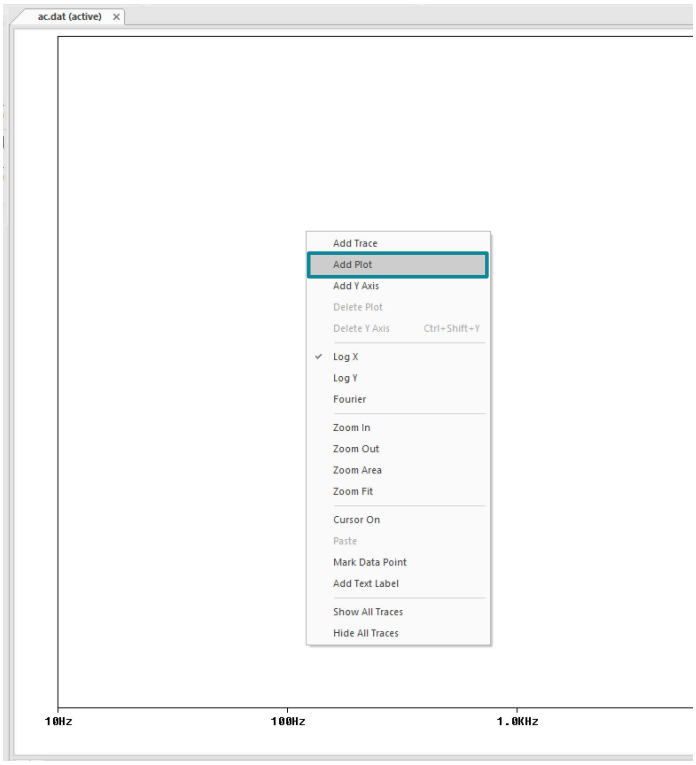

Figure 5-9. Add a Plot

In this example, the frequency sweep was performed to observe the open loop response of the circuit, seen in Magnitude (dB) and Phase (˚); therefore, two plots are added in the output window of the simulator.

Typically for the AC response of op amps, the top plot is Magnitude (dB) and the bottom plot is Phase (˚). To add the Magnitude (dB) and Phase (˚) of the relevant nets, a trace must be placed. This can be done by right-clicking on the desired plot and selecting *Add Trace* as seen in Figure 5-10.

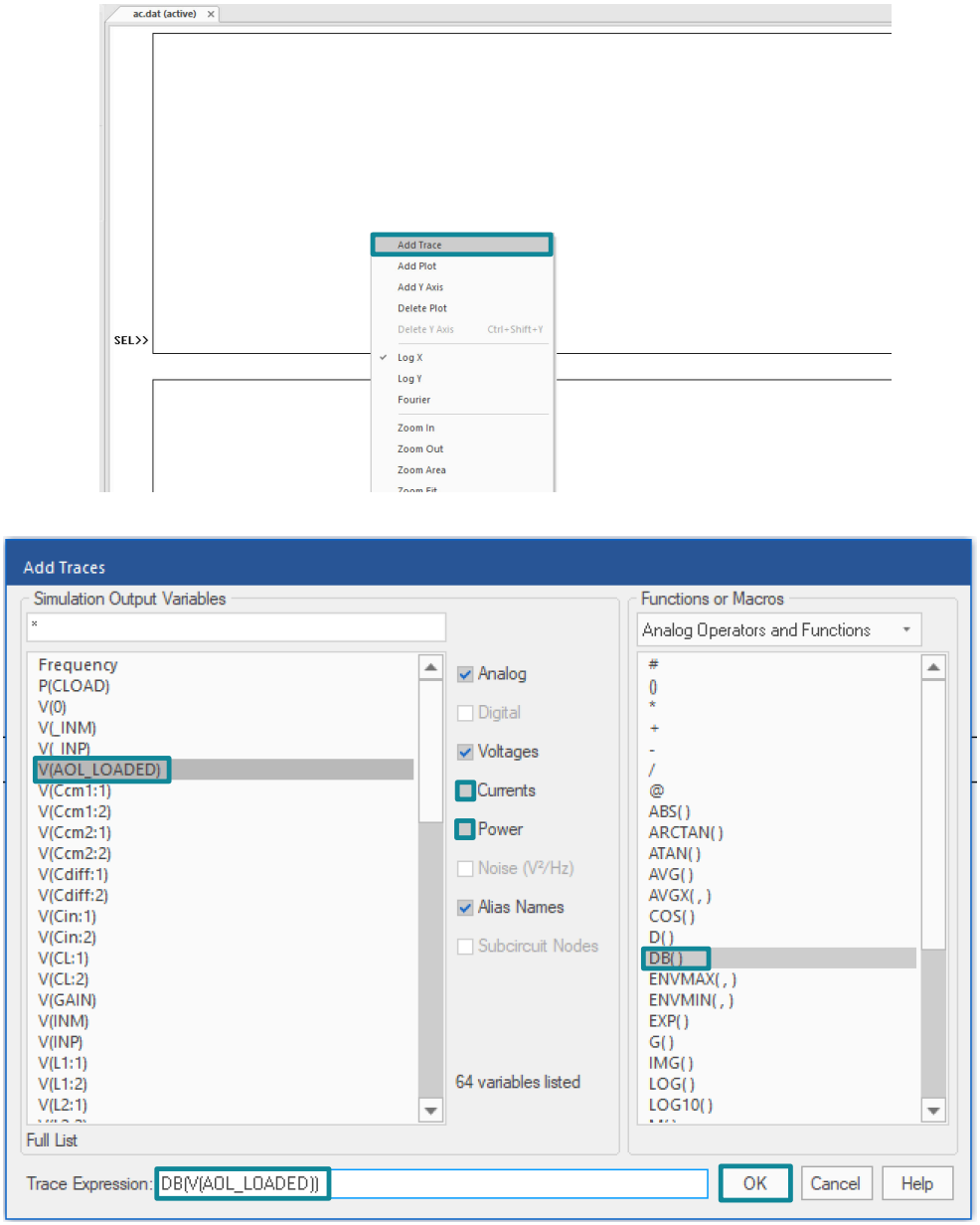

Figure 5-10. Add Trace

A dialog window appears in which *Simulation Output Variables* can be selected along with “Functions or Macros.”

In this example, the required Magnitude (dB) and Phase (˚) traces are listed in Table 5-1.

Table 5-1. Trace Syntax

	Trace	Expression Syntax
Open loop response with load	Voltage at op amp output with load (in dB)	DB(V(AOL_LOADED))
Loop Gain	Voltage across nets labeled "LOOP" and "GAIN" (in dB and degrees)	DB(V(LOOP,GAIN))
		P(V(LOOP,GAIN))
1/β	Ratio of open loop response with load and loop gain	DB(V(AOL_LOADED)/V(LOOP,GAIN))

The *Trace Expression* can be typed in or selected from the available options as seen in Figure 5-10. Alternatively, the traces can be copied and pasted fromTable 5-1 into the program directly if the nets have been labeled as described earlier in the document, Figure 4-17.

The output simulation window including all trace expressions are shown in Figure 5-11, the top plot is the Magnitude (dB) response and the bottom plot is Phase (˚).

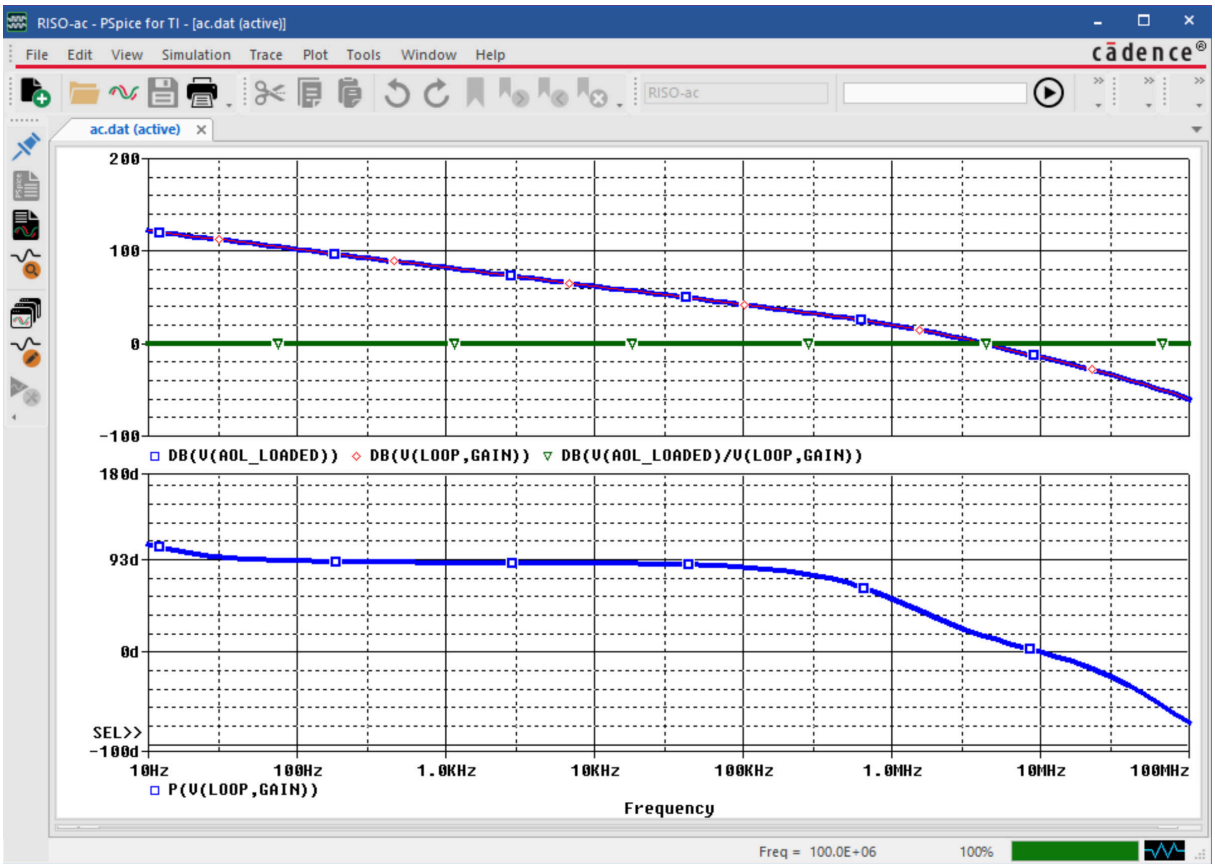

Figure 5-11. Output Simulation Window

In this example, the goal is to improve the phase margin. This is done by evaluating the phase margin of the open loop response and calculating compensation component from the AC response of the circuit.

PSpice®-for-TI has built in formulas, the syntax can be found in the *Measurements* option in the *Trace* sub menu, as seen in Figure 5-12.In this example, three measurements are used, *PhaseMargin*, *XatNthY*, and *Max*.

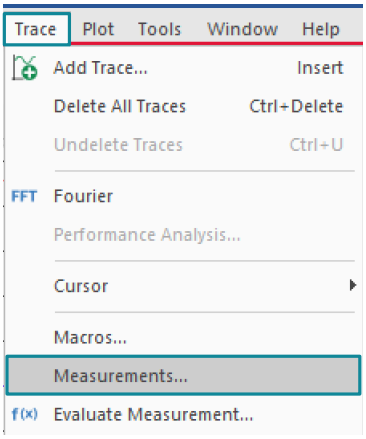

Figure 5-12. Syntax Definition for Measurements

Select the relevant option in the *Measurements* window, in this example *PhaseMargin* is highlighted and *View* is selected.

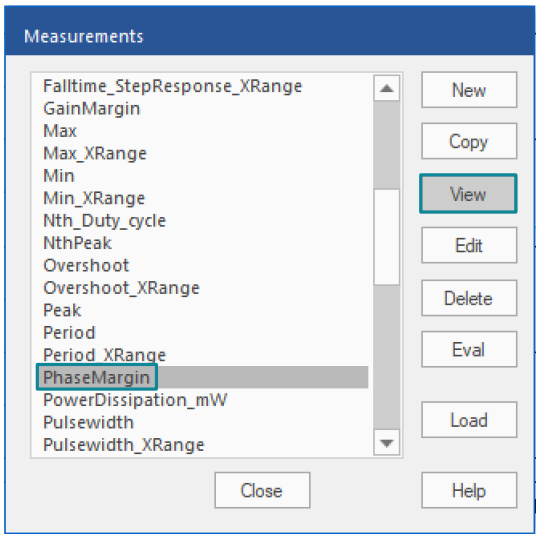

Figure 5-13. PhaseMargin Measurement

The selected measurement, the description, syntax for the measurement argument, and file path are displayed in the dialogue box.

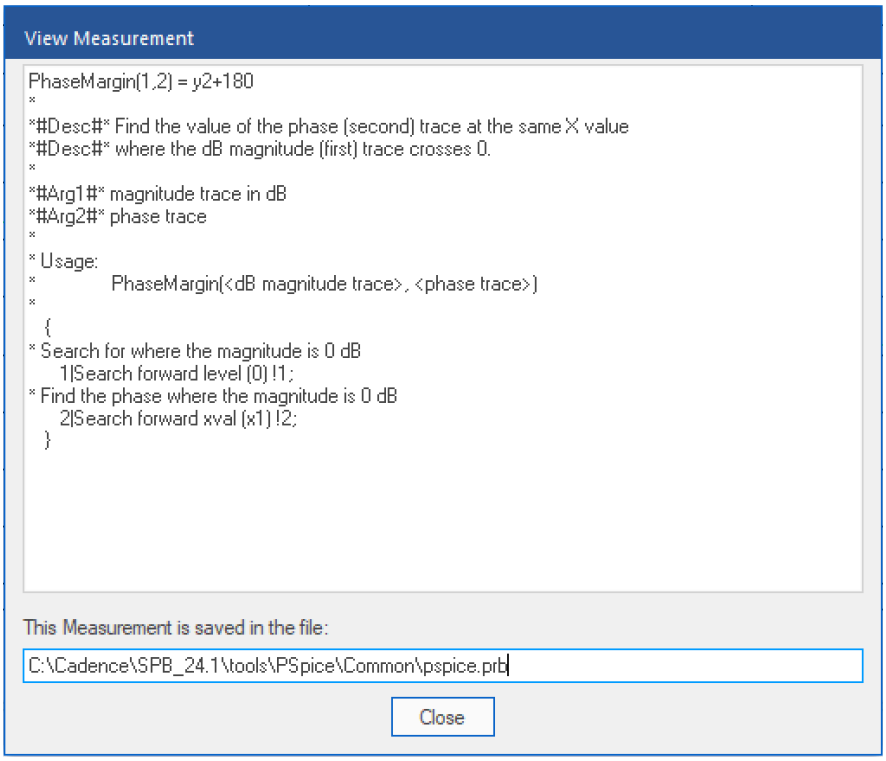

Figure 5-14. PhaseMargin Measurement Defined

The phase margin measurement is the phase at the frequency in which the magnitude is 0dB. In PSpice®-for-TI, this is accomplished by searching a magnitude of the trace in dB, until the value level is 0, the x value (frequency) is recorded. Then the y value of the phase plot is read at that frequency.

In the defined measurement in Figure 5-14, the phase margin provided by *y2* is offset by +180 degrees, this is not relevant for op amps so the measurement evaluated is offset by -180 degrees resulting in the written equation of *PhaseMargin(DB(Trace), P(Trace)) -180*.

Next, to find the frequency where the output of the magnitude of the op amp is 0dB and 20dB, the *XatNthY* measurement is used. XatNthY measurement is defined, in Figure 5-15, as the x corresponding to the given y value at an occurrence - where x is the frequency (Hz) and y is the magnitude (dB). For both of these scenarios, there are not multiple occurrences, therefore just the first occurrence is considered.

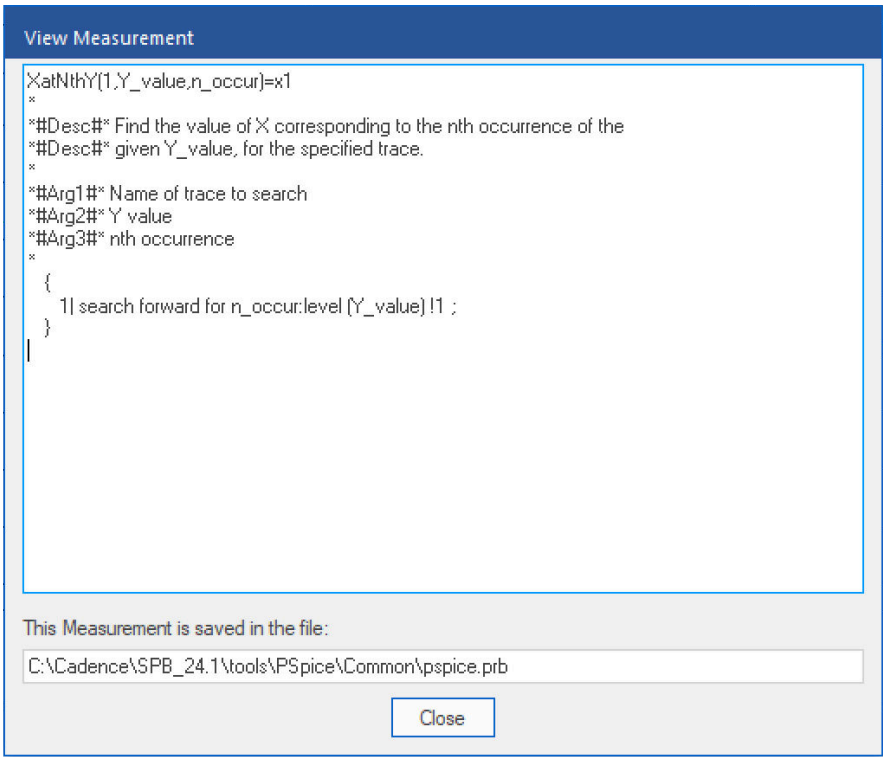

Figure 5-15. XatNthY Measurement Defined

To calculate *RISO* compensation, the value of the capacitive load must be transferred from the schematic to the output simulation window, the implementation of this was described Figure 4-13. To include this probe at CLOAD, P(CLOAD), into an equation to be evaluated, a measurement must be applied to the probe at the parameter *CLOAD*. Considering the capacitive value does not change with frequency, the *max* measurement, defined in Figure 5-16, is used.

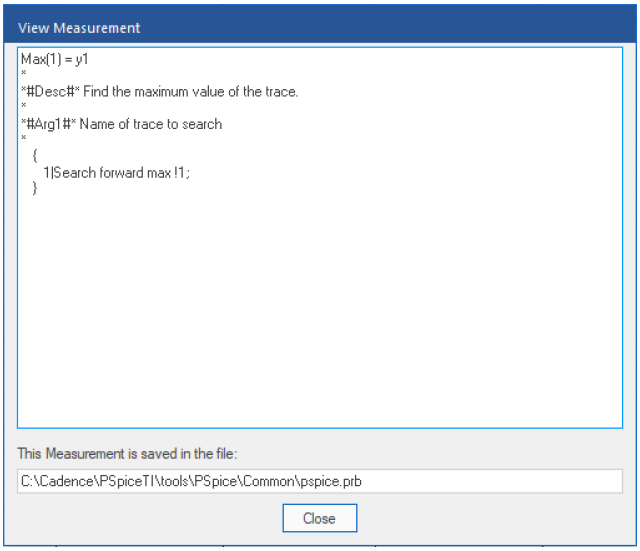

Figure 5-16. Max Measurement Defined

Table 5-2 shows a summary of the equation syntax needed for “Phase Margin,” typical "RISO," and a conservative “RISO” value. The typical "RISO" provides a phase margin close to 45° and the conservative "RISO" provides a phase margin close to 90°. The tradeoff for a larger isolation resistor is voltage inaccuracies at the output with higher current demand (smaller resistive loads).

$$R_{ISO}\left(typical\right) = \frac{1}{2\pi \times f_{AOL\_LOADED\ =\ 0dB} \times C_{LOAD}} \quad (1)$$

$$R_{ISO}\left(conservative\right) = \frac{1}{2\pi \times f_{AOL\_LOADED\ =\ 20dB} \times C_{LOAD}} \quad (2)$$

Table 5-2. Measurement equations and syntax

Measurement	Expression Syntax
Phase Margin	PhaseMargin(DB(V(LOOP,GAIN)),P(V(LOOP,GAIN)))-180
RISO (typical)	1/(2*pi* Max(P(CLOAD))* XatNthY(DB(V(AOL_LOADED)),0,1))
RISO (conservative)	1/(2*pi* Max(P(CLOAD))* XatNthY(DB(V(AOL_LOADED)),20,1))

To add these measurements to the output simulation window, select *Evaluate Measurement* through the *Trace* sub menu.

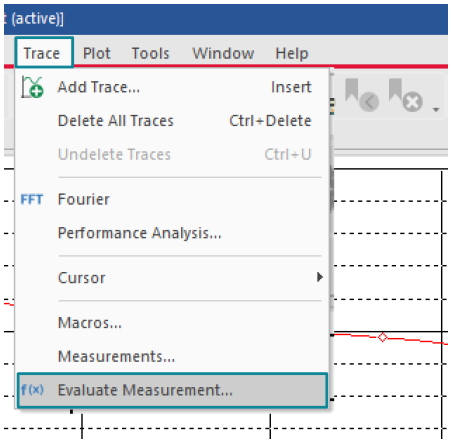

Figure 5-17. Evaluate Measurement

The *Trace Expression* can be typed in, selected from the available options, or copied and pasted from Table 5-2.

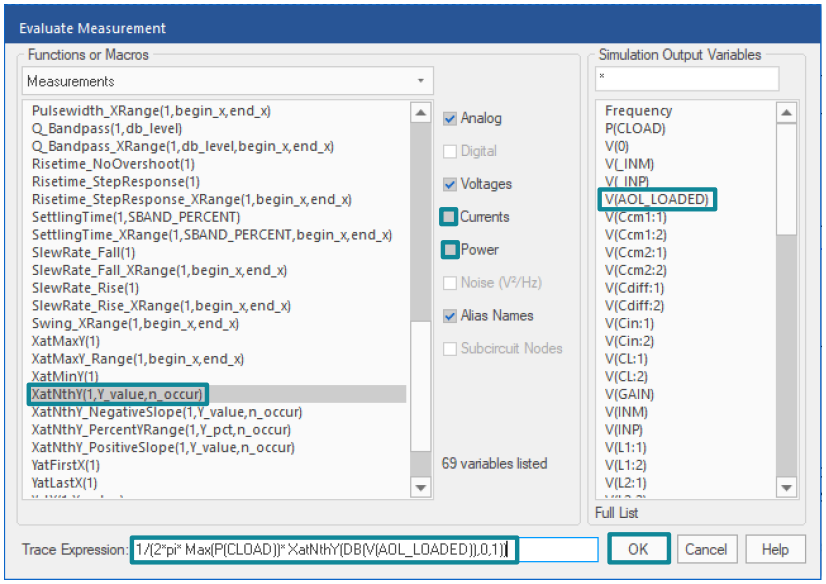

Figure 5-18. Trace Expression for Measurement Evaluation

The *Measurement Results* window displays the measurements described in Figure 5-19. The output window, which includes the plots and measurements, is displayed every time an iteration is run.

Evaluate	Measurement	
☑	PhaseMargin(DB(V(LOOP,GAIN)),P(V(LOOP,GAIN)))-180	Phase Margin
☑	1/(2*pi* Max(P(CLOAD))* XatNthY(DB(V(AOL_LOADED)),0,1))	RISO (typical)
☑	1/(2*pi* Max(P(CLOAD))* XatNthY(DB(V(AOL_LOADED)),20,1))	RISO (conservative)

Figure 5-19. Equations in PSpice®-for-TI syntax

6 Summary

All the ingredients of the automated design have been discussed to great detail, including but not limited to:

- A problem to solve
- A reusable solution
- How to create a PSpice®-for-TI project
- Schematic drawing for increased readability
  - Placing passive components
  - Leveraging parameters
  - Placing power supplies
  - How to wire and label
  - Organizing for the user experience
- Simulation profile setup
  - Aiding in convergence
  - Powerful post processing

Once assembled, the design can be used to quickly solve the problem across multiple devices and conditions. Here is the example discussed throughout the document in action.

The OPAx392 is placed into the schematic driving a 1nF capacitive load.

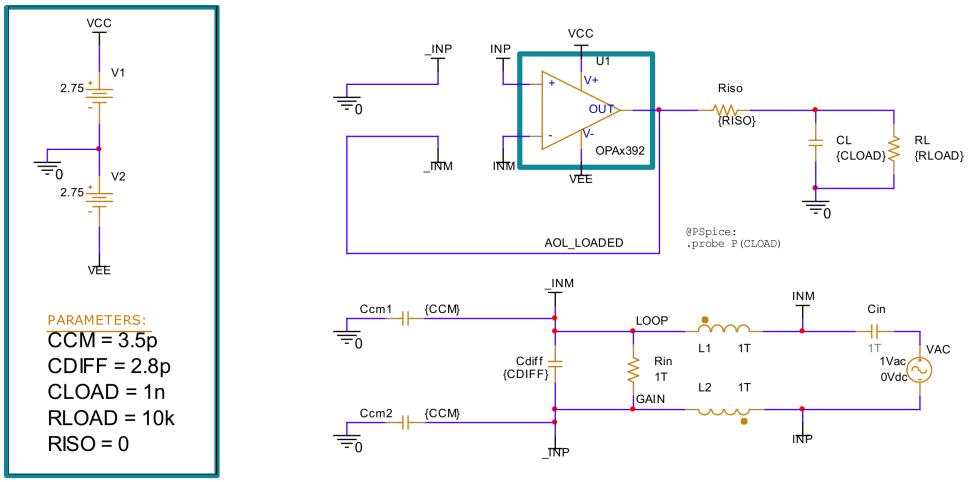

Figure 6-1. OPA392 Driving 1nF Capacitive Load: No Compensation

The resulting phase margin is 16 degrees, which is outside of the stable definition of between 45° and 90°.

	Evaluate	Measurement	Value
	☑	PhaseMargin(DB(V(LOOP,GAIN)),P(V(LOOP,GAIN)))-180	16.35200
	☑	1/(2*pi* Max(P(CLOAD))* XatNthY(DB(V(AOL_LOADED)),0,1))	37.92552
▶	☑	1/(2*pi* Max(P(CLOAD))* XatNthY(DB(V(AOL_LOADED)),20,1))	153.34276

Figure 6-2. Unstable Phase Margin with Suggestions for RISO (Typical and Conservative)

The minimum RISO suggestion is 37.9Ω and conservative RISO suggestion is 153.3Ω, the 1% common resistor value of 38.3Ω is used for the RISO in the next iteration of the simulation.

The resulting output has a phase margin of 57 degrees, which implies the output capacitive load is properly compensated by an isolation resistor of 38.3Ω.

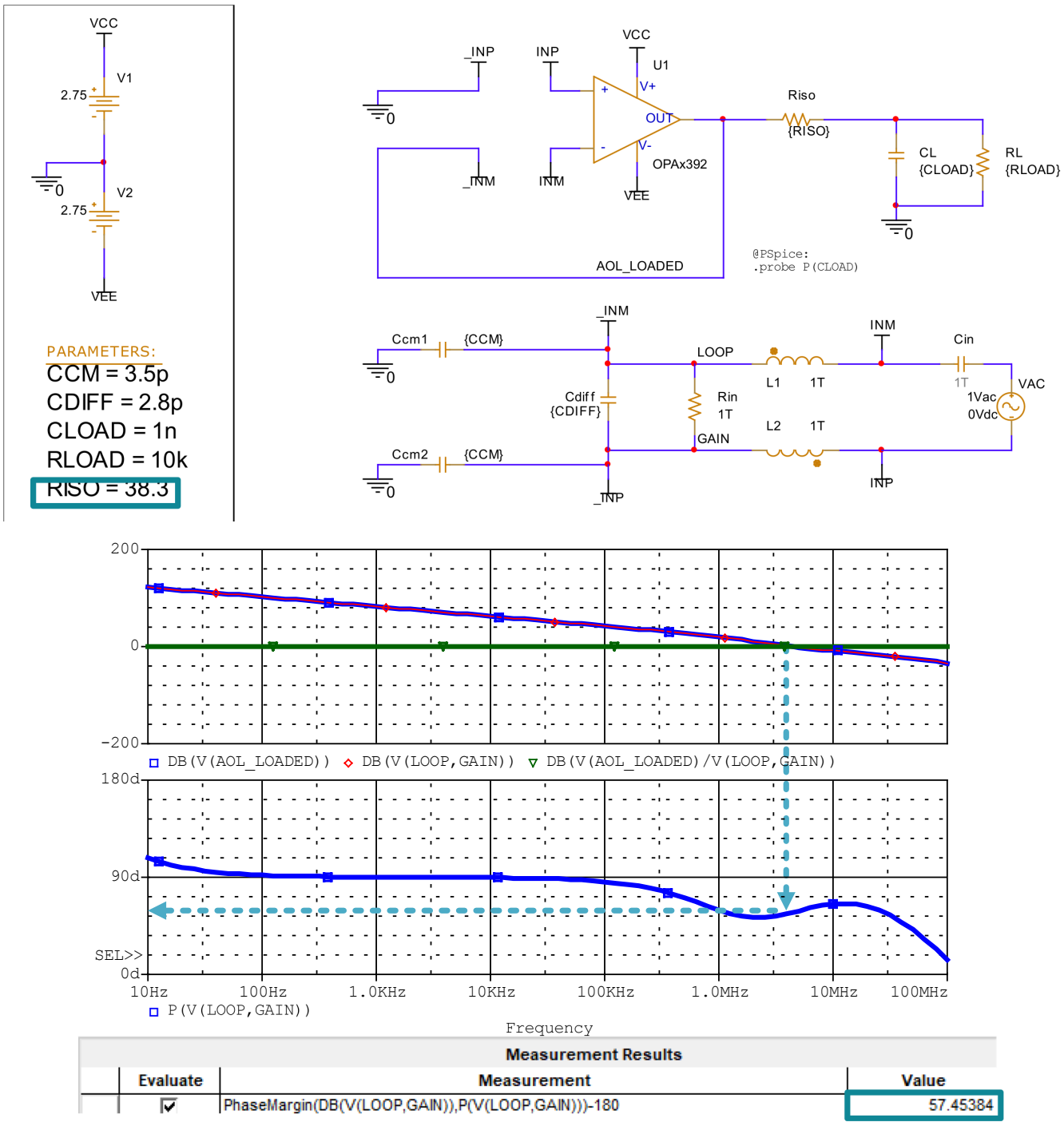

Figure 6-3. OPA392 Driving 1nF Capacitive Load with RISO Compensation

This automated design can be repeated for different op amps, different capacitive loads, and different circuit configurations to help achieve a quick resolution. The automated design example discussed in this application note is available for download here:

- 0° to 60° Stability Automated: Gain of 1 (Buffer)
- 0° to 60° Stability Automated: Non-Inverting Gain
- 0° to 60° Stability Automated: Inverting Gain
- 0° to 60° Stability Automated: Difference Amplifier Gain

7 References

- Texas Instruments, TINA-TI Simulation tool, SPICE-based analog simulation program.
- PSPICE-FOR-TI Simulation tool, simulation tool.
- Precision labs series: Op amps, video series.
- Breaking loop on differential amplifier, video series.

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