Analog Engineer's Circuit

Three-Wire PT100 RTD Measurement Circuit With High-Side Reference and Two IDAC Current Sources

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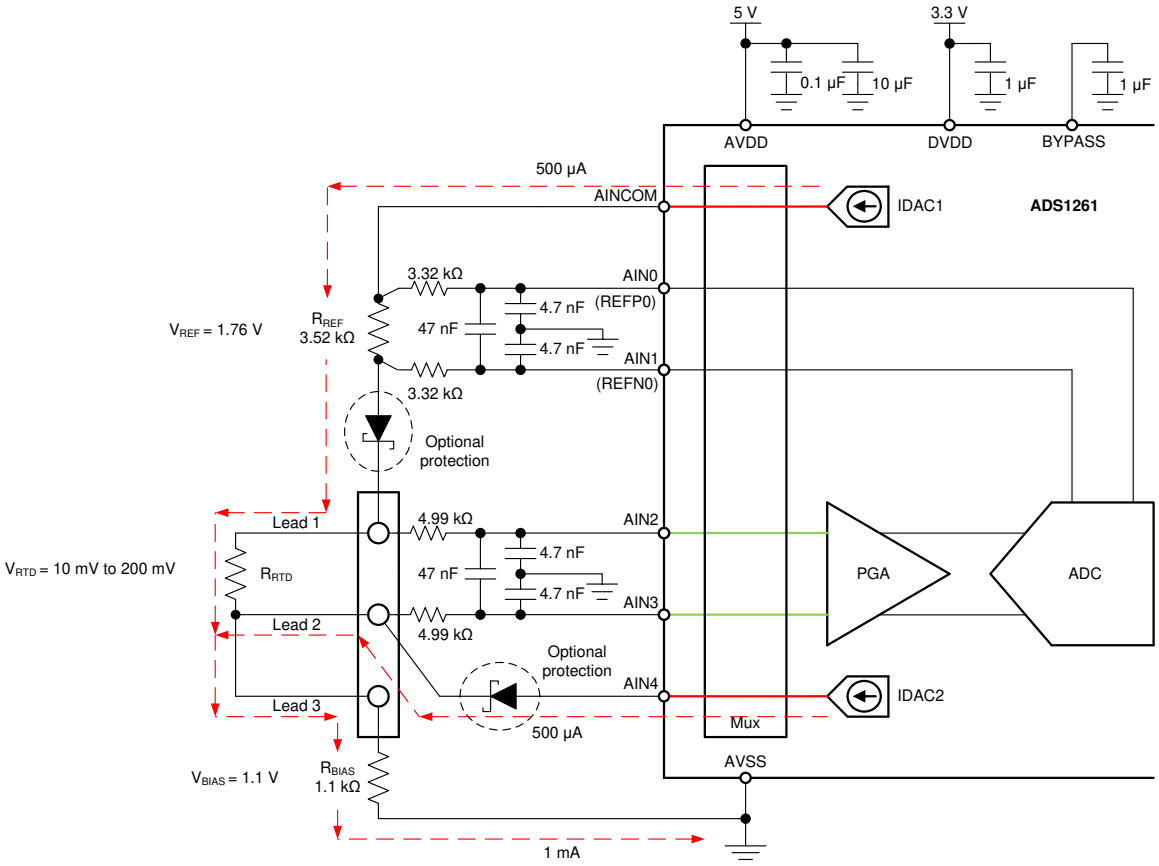
Power Supplies

AVDD	AVSS, DGND	DVDD
5V	0V	3.3V

Design Description

This cookbook design describes a temperature measurement for a three-wire RTD using the ADS1261. This design uses a ratiometric measurement with a high-side reference using two matched excitation current sources for a PT100 type RTD with a temperature measurement range from –200°C to 850°C. Included in this design are ADC configuration register settings and pseudo code to configure and read from the device. This circuit can be used in applications such as *analog input modules* for PLCs, *lab and field instrumentation,* and *factory automation and control.* For more information about making precision ADC measurements with a variety of RTD wiring configurations, see *A Basic Guide to RTD Measurements.*



Design Notes

1. Use supply decoupling capacitors for both the analog and digital supplies. Place 0.1-µF and 10-µF capacitors between AVDD and AVSS (ground). Connect a 1-µF capacitor from DVDD to the ground plane. Connect a 1-µF capacitor from BYPASS to the ground plane. See the *ADS126x Precision, 5-Channel and 10-Channel, 40-kSPS, 24-Bit, Delta-Sigma ADCs With PGA and Monitors* data sheet for details on power-supply recommendations.
2. Do not route the excitation currents through input filter resistors, using the same pin as an ADC input and as the output for an IDAC current source. Excitation currents reacting with series resistance adds error to the measurement.
3. A 10-µF capacitor is required between REFOUT and REFCOM to enable the internal reference for the IDAC current.
4. Use a precision reference resistor with high accuracy and low drift. Because the measurement is ratiometric, accuracy is dependent on the error of this reference resistor. A 0.01% resistor contributes a gain error similar to that as the ADC.
5. When possible, use C0G (NPO) ceramic capacitors for input filtering. The dielectric used in these capacitors provides the most stable electrical properties over voltage, frequency, and temperature changes.
6. Input filtering for the ADC inputs and the reference inputs are selected using standard capacitor values and 1% resistor values. An example design and analysis of these filters is found in *RTD Ratiometric Measurements and Filtering Using the ADS1148 and ADS1248 Family of Devices.*
7. This design shows connections to six input pins of the ADC multiplexer. Use the remaining analog inputs for other measurements, such as bridge measurements with AC excitation.
8. Because of lead-resistance cancellation, the three-wire measurement offers more accuracy than comparable *two-wire RTD measurements.* Using a high-side reference for this design significantly reduces the error from IDAC current mismatch seen in *three-wire RTD measurements using a low-side reference.* For measurements with other RTD wiring configurations, see *A Basic Guide to RTD Measurements.*

Component Selection

1. Identify the range of operation for the RTD.

   As an example, a PT100 RTD has a range of approximately 20Ω to 400Ω if the temperature measurement range is from −200°C to 850°C. The reference resistor must be larger than the maximum RTD value. The reference resistance and PGA gain determines the positive full scale range of the measurement.
2. Use two matched IDAC current sources to cancel the lead-resistance error.

   Two matched IDAC current sources are used for lead-resistance cancellation. Assuming the resistances of lead 1 and lead 2 are the same, and the currents of IDAC1 and IDAC2 are the same, then the lead-resistance error is canceled. Cancellation can be shown through the measured voltages at AIN2 and AIN3.

   IDAC1 drives current into the reference resistor R_{REF} and the RTD through lead 1. IDAC2 drives current into lead 2. First, assume that the input protection shown in the circuit has no voltage drop. The voltages at AIN2 and AIN3 are calculated with the following equations.

   $$V_{AIN2} = I_{IDAC1} \times (R_{LEAD1} + R_{RTD}) + (I_{IDAC1} + I_{IDAC2}) \times (R_{LEAD3} + R_{BIAS})$$

   $$V_{AIN3} = I_{IDAC2} \times R_{LEAD2} + (I_{IDAC1} + I_{IDAC2}) \times (R_{LEAD3} + R_{BIAS})$$

   The measurement of the ADC is the difference between AIN2 and AIN3, which is the subtraction of the previous equations.

   $$V_{AIN2} - V_{AIN3} = [I_{IDAC1} \times (R_{LEAD1} + R_{RTD} + R_{BIAS}) + (I_{IDAC1} + I_{IDAC2}) \times (R_{LEAD3} + R_{BIAS})] - [I_{IDAC2} \times R_{LEAD2} + (I_{IDAC1} + I_{IDAC2}) \times (R_{LEAD3} + R_{BIAS})]$$

   Then, the R_{LEAD3} and R_{BIAS} terms drop out.

   $$V_{AIN2} - V_{AIN3} = I_{IDAC1} \times (R_{LEAD1} + R_{RTD}) - I_{IDAC2} \times R_{LEAD2}$$

If R_{LEAD1} and R_{LEAD2} are equal and I_{IDAC1} and I_{IDAC2} are equal (to become I_{IDAC}), then the lead resistance errors cancel to leave the following equation:

$$V_{AIN2} – V_{AIN3} = I_{IDAC} × R_{RTD}$$

3. Determine values for the IDAC excitation currents and reference resistor.

   The excitation current source in this design is selected to be 500µA. This maximizes the value of the RTD voltage while keeping the self-heating of the RTD low. The typical range of RTD self-heating coefficients is 2.5mW/°C for small, thin-film elements and 65mW/°C for larger, wire wound elements. With 500µA excitation at the maximum RTD resistance value, the power dissipation in the RTD is less than 0.4mW and keeps the measurement errors from self-heating to less than 0.005°C.

   After selecting the IDAC current magnitude, set R_{REF} = 3.52kΩ. Using a 500µA excitation current sets the reference at 1.76V and the maximum RTD voltage is 200mV. With these values, the PGA gain can be set to eight so that the maximum RTD voltage is near, but not exceeding, the positive full scale range without exceeding.

   The reference resistor, R_{REF} must be a precision resistor with high accuracy and low drift. Any error in R_{REF} reflects the same error in the RTD measurement. The REFP and REFN pins (AIN0 and AIN1) are shown connecting to the R_{REF} resistor as a Kelvin connection to get the best measurement of the reference voltage. This eliminates any series resistance as an error from the reference resistance measurement.

   Note that for a high-side reference, the current flowing through the reference resistor and the RTD are the same. For a *three-wire RTD measurement with a low-side reference*, the IDAC current mismatch is a large contributor to the error. In this design, the mismatch only leads to a smaller error in the lead-resistor cancellation, rather than a larger gain error in the RTD measurement.

4. Set R_{BIAS} and verify that the design is within the range of operation of the ADC.

   Once the reference resistance, IDAC current magnitudes, and ADC gain are set, select the R_{BIAS} resistance to set the bias voltage of the input measurement. Normally, R_{BIAS} is selected to set the input to the mid-supply voltage. However, there is a large total sum of the voltage drop across the reference resistor, the RTD resistance, the bias resistor, and any optional input protection used in the circuit. It is important that the R_{BIAS} input offset is high enough to keep the RTD measurement voltage in the PGA input range, but not too high so that the excitation current output pin is within the compliance voltage of the IDAC.

   Setting R_{BIAS} of 1.1kΩ meets this requirement. Using the maximum RTD resistance of 400Ω, the ADC input voltages are calculated in the following equations. The small lead resistances can be ignored for this calculation.

   $$V_{AIN2} = (I_{IDAC1} × R_{RTD}) + [(I_{IDAC1} + I_{IDAC2}) × R_{BIAS}] = 1.3V$$

   $$V_{AIN3} = (I_{IDAC1} + I_{IDAC2}) × R_{BIAS} = 1mA × 1.1kΩ = 1.1V$$

   $$V_{INMAX} = 500µA × 400Ω = 200mV$$

   First, verify that the voltage at AIN2 and AIN3 are within the input range of the PGA given that the gain is 8 and that AVDD is 5V and AVSS is 0V. As shown in the *ADS126x Precision, 5-Channel and 10-Channel, 40-kSPS, 24-Bit, Delta-Sigma ADCs With PGA and Monitors* data sheet, the absolute input voltage must satisfy the following:

   $$AVSS + 0.3V + [|V_{INMAX}| × (Gain – 1) ÷ 2] < V_{AIN2}, V_{AIN3} < V_{AVDD} – 0.3V – [|V_{INMAX}| × (Gain – 1) ÷ 2]$$

   $$0.3V + [|0.2V| × (8 – 1) ÷ 2] < V_{AIN2}, V_{AIN3} < 5V– 0.3V – [|0.2V| × (8 – 1) ÷ 2]$$

   $$1V < V_{AIN2}, V_{AIN3} < 4V$$

   Because the maximum and minimum input voltage seen at AIN2 and AIN2 (1.1V and 1.3V) are between 1V and 4V, the inputs are in the PGA operating range.

Second, verify that the IDAC output pin voltages are within the compliance voltage. The IDAC current output voltage is highest and most limited by output compliance when the RTD voltage is at a maximum as the following equation shows. As before, we can ignore the low voltage contribution of the lead resistance.

$V_{IDAC1} = V_{BIAS} + V_{RTD} + V_D + V_{REF}$

$V_{IDAC1} = 1V + 0.2V + 0.3V + 1.76V = 3.26V$

The maximum RTD voltage is 200mV and a drop of 300mV is assumed for an input protection Schottky diode (V_D).

The IDAC current compliance range is listed in the *Electrical Characteristics* table under the *Current Sources* section of the *ADS126x Precision, 5-Channel and 10-Channel, 40-kSPS, 24-Bit, Delta-Sigma ADCs With PGA and Monitors* data sheet. The IDAC current compliance range is given by the following equation.

$AVSS < V_{IDAC1} < AVDD – 1.1V$

In this example design, AVDD is 5V and reduces the following:

$0V < V_{IDAC1} < 3.9V$

With the previous equation, the output compliance of the IDAC1 pin is satisfied. Because the IDAC2 pin is always at a lower voltage than IDAC1 voltage, both current sources are in the compliance range.

The schematic is shown with two optional input protection diodes. These low V_F diodes provide input fault protection for the IDAC current sources, and may be replaced with series resistances. If series resistance is used, then the added diode voltage of 0.3V is replaced with the voltage from I_{IDAC} across the new series resistance for equations verifying the IDAC output pin compliance voltage.

Third, verify that the reference voltage is within the reference voltage input range for the ADC. For the ADS1261, the differential reference input voltage range is shown in the *Recommended Operating Conditions* of the *ADS126x Precision, 5-Channel and 10-Channel, 40-kSPS, 24-Bit, Delta-Sigma ADCs With PGA and Monitors* data sheet as the following equation.

$0.9V < V_{REFP} – V_{REFN} < AVDD – AVSS$

$0.9V < 1.76V < 5V$

Also verify the absolute negative reference input voltage and verify the absolute positive reference input voltage with the following equations. Calculations show that the reference voltages are within the input range of the ADC reference.

$AVSS – 0.05V < V_{REFN} = V_{BIAS} + V_{RTD} + V_D < V_{REFP} – 0.9V$

$–0.05V < 1.5V < 4.1V$

$V_{REFN} < V_{REFP} = V_{BIAS} + V_{RTD} + V_D + V_{REF} < AVDD + 0.05V$

$1.5V < 3.26V < 5.05V$

5. Select values for the differential and common-mode input filtering for the ADC inputs and reference inputs.

   This design includes differential and common-mode input RC filtering. The bandwidth of the differential input filtering is set to be at least 10 × higher than the data rate of the ADC. The common-mode capacitors are selected to be 1/10 of the value the differential capacitor. Because of capacitor selection, the bandwidth of common-mode input filtering is approximately 20 × higher than the differential input filtering. While series filter resistors offer some amount of input protection, keep the input resistors lower than 10kΩ, to allow for proper input sampling for the ADC.

With input filtering, differential signals are attenuated at a lower frequency than the common-mode signals, which are significantly rejected by the PGA of the device. Mismatches in common-mode capacitors cause an asymmetric noise attenuation, appearing as a differential input noise. With a lower bandwidth for differential signals, the effects from the mismatch of input common-mode capacitors be reduced. Input filtering for the ADC inputs and reference inputs are designed for the same bandwidth.

In this design, the data rate is chosen to be 20SPS using the low-latency filter of the ADS1261. This filtering provides a low noise measurement with single-cycle settling and the ability to reject 50-Hz and 60-Hz line noise. For the ADC input filtering, the bandwidth frequency for the differential and common-mode filtering is approximated in the following equations.

$$f_{IN\_DIFF} = 1 \div [2 \times \pi \times C_{IN\_DIFF} (R_{RTD} + 2 \times R_{IN})]$$

$$f_{IN\_CM} = 1 \div [2 \times \pi \times C_{IN\_CM} (R_{RTD} + R_{IN} + R_{BIAS})]$$

For the ADC input filtering, R_{IN} = 4.99kΩ, C_{IN_DIFF} = 47nF, and C_{IN_CM} = 4.7nF. This sets the differential filter bandwidth to 330Hz and the common-mode filter bandwidth to 5.4kHz.

Similarly, the bandwidth for the reference input filtering is approximated in the following equations.

$$f_{REF\_DIFF} = 1 \div [2 \times \pi \times C_{REF\_DIFF} \times (R_{REF} + 2 \times R_{IN\_REF})]$$

$$f_{REF\_CM} = 1 / \{2 \times \pi \times C_{REF\_CM} \times [R_{IN\_REF} + (½ \times R_{REF}) + R_{RTD} + R_{BIAS}]\}$$

For the reference input filtering, R_{IN_REF} = 3.32kΩ, C_{REF_DIFF} = 47nF, and C_{REF_CM} = 4.7nF. This sets the differential filter bandwidth to 330Hz and the common-mode filter bandwidth to 5.3kHz. Matching the ADC input and reference input filtering is not always possible in a design. However, keeping the bandwidths close may reduce noise in the measurement.

For an in-depth analysis of component selection for input filtering, see *RTD Ratiometric Measurements and Filtering Using the ADS1148 and ADS1248 Family of Devices*.

Measurement Conversion

RTD measurements are typically ratiometric measurements. Using a ratiometric measurement, the ADC output code does not need to be converted to a voltage. This means that the output code gives a measurement only as a ratio of the value of the reference resistor and does not require a precise value for the excitation current. The only requirement is that the current through the RTD and reference resistor are the same.

Equations for the measurement conversion are shown for a 24-bit ADC:

$$\text{Output Code} = 2^{23} \times \text{Gain} \times (V_{RTD} \div V_{REF}) = 2^{23} \times \text{Gain} \times (I_{IDAC1} \times R_{RTD}) \div (I_{IDAC1} \times R_{REF}) = 2^{23} \times \text{Gain} \times (R_{RTD} \div R_{REF})$$

$$R_{RTD} = R_{REF} \times [\text{Output Code} \div (\text{Gain} \times 2^{23})]$$

The ADC converts the measurement to the RTD equivalent resistance. Because of non-linearity in the RTD response, the conversion of the resistance to temperature requires an calculation from equation or lookup table. For more information about the conversion of RTD resistance to temperature, see *A Basic Guide to RTD Measurements*.

Register Settings

Configuration Register Settings for a 3-Wire RTD Measurement with High-Side Reference and Two IDAC Current Sources Using the ADS1261

Register Address	Register Name	Setting	Description
02h	MODE0	24h	20SPS, FIR digital filter
03h	MODE1	01h	Normal mode, Continuous conversion, 50 µs delay between conversions
04h	MODE2	00h	GPIOs disabled
05h	MODE3	00h	No power-down, no STATUS or CRC byte, timeout disabled
06h	REF	1Ah	Internal reference enabled, REFP = AIN0, REFN = AIN1
0Dh	IMUX	4Ah	IDAC2 = AIN4, IDAC1 = AINCOM
0Eh	IMAG	44h	IMAG2 = IMAG1 = 500µA
0Fh	RESERVED	00h	Reserved
10h	PGA	03h	PGA enabled, Gain = 8
11h	INPMUX	34h	Select AIN_P = AIN2 and AIN_N = AIN3
12h	INPBIAS	00h	VBIAS voltages and burnout current sources disabled

Pseudo Code Example

The following shows a pseudo code sequence with the required steps to set up the device and the microcontroller that interfaces to the ADC to take subsequent readings from the ADS1261 in continuous conversion mode. The dedicated $\overline{DRDY}$ pin indicates availability of new conversion data. Pseudo code is shown without the use of the STATUS byte and CRC data verification. ADS1261 example code is available from the ADS1261 product folder.

```
Configure microcontroller for SPI mode 1 (CPOL = 0, CPHA = 1)
Configure microcontroller GPIO for /DRDY as a falling edge triggered interrupt input
Set CS low;
Send 06;//RESET command to make sure the device is properly reset after power-up
Set CS high;
Set CS low;// Configure the device
Send 42// WREG starting at 02h address
04// Write to 5 registers
24// 20SPS, FIR digital filter
01// Normal mode, Continuous conversion, 50µs delay between conversions
00// GPIOs disabled
00// No power-down, no STATUS or CRC byte, timeout disabled
1A;// Internal reference enabled, REFP = AIN0, REFN = AIN1
Set CS high;
Set CS low;// Configure the device, IDACs
Send 4D// WREG starting at 0Dh address
05// Write to 6 registers
4A// IMUX2 = AIN4, IMUX1 = AINCOM
44// IMAG2 = IMAG1 = 500µA
00// RESERVED
03// PGA enabled, Gain = 8
34// Select AINP = AIN2 and AINN = AIN3
00;// VBIAS voltages and burn-out current sources disabled
Set CS high;
Set CS low;// For verification, read back configuration registers
Send 22// RREG starting at 02h address
10// Read from 17 registers
00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00;// Send 17 NOPs for the read
Set CS high;
Set CS low;
Send 08;// Send START command to start converting in continuous conversion mode;
Set CS high;
Loop
{
Wait for DRDY to transition low;
Set CS low;
Send 12// Send RDATA command
00 00 00;// Send 3 NOPs (24 SCLKs) to clock out data
Set CS high;
}
Set CS low;
Send 0A;//STOP command stops conversions and puts the device in standby mode;
Set CS to high;
```

RTD Circuit Comparison Table

RTD Circuit Topology	Advantages	Disadvantages
Two-wire RTD, low-side reference	Least expensive	Least accurate, no lead-resistance cancellation
Three-wire RTD, low-side reference, two IDAC current sources	Allows for lead-resistance cancellation	Sensitive to IDAC current mismatch, mismatch can be removed by swapping IDAC currents and averaging two measurements
Three-wire RTD, low-side reference, one IDAC current source	Allows for lead-resistance cancellation	Requires two measurements, first for RTD measurement, second for lead-resistance cancellation
Three-wire RTD, high-side reference, two IDAC current sources	Allows for lead-resistance cancellation, less sensitive to IDAC mismatch than using low side reference	Requires extra resistor for biasing, added voltage may not be compatible with low supply operation
Four-wire RTD, low-side reference	Most accurate, no lead-resistance error	Most expensive

Design Featured Devices

Device	Key Features	Link	Other Possible Devices
ADS1261	24-bit 40kSPS 10-ch delta-sigma ADC with PGA, Vref, 2 × IDACs, and AC excitation for factory automation	24-bit, 40-kSPS, 10-ch delta-sigma ADC with PGA, VREF, IDACs & AC excitation for factory automation	Precision ADCs

Additional Resources

- Texas Instruments, ADS1261 Evaluation Module, product overview
- Texas Instruments, *ADS1261 and ADS1235 Evaluation Module*, user's guide
- Texas Instruments, *24-bit, 40-kSPS, 10-ch delta-sigma ADC with PGA, VREF, IDACs & AC excitation for factory automation*, product overview
- Texas Instruments, *A Basic Guide to RTD Measurements*, application note
- Texas Instruments, *RTD Ratiometric Measurements and Filtering Using the ADS1148 and ADS1248 Family of Devices*, application note

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