Analog Engineer's Circuit

Low-Power Sensor Measurements: 3.3V, 1Ksps, 12-Bit, Single-Ended, Dual-Supply Circuit

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Design Goals

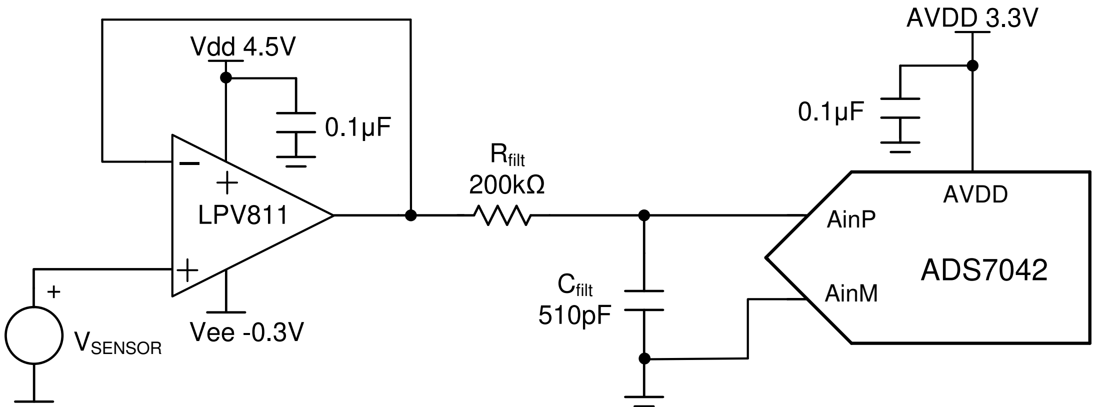
Input	ADC Input	Digital Output ADS7042
V_{inMin} = 0V	AIN_P = 0V, AIN_M = 0V	000_H or 0_{10}
V_{inMax} = 3.3V	AIN_P = 3.3V, AIN_M = 0V	FFF_H or 4096_{10}

Power Supply

AVDD	V_{ee}	V_{dd}
3.3V	–0.3V	4.5V

Design Description

This design shows an low-power amplifier being used to drive a SAR ADC that consumes only nW of power during operation. This design is intended for systems collecting sensor data and require a low-power signal chain which only burns single-digit µW of power. *PIR sensors*, *gas sensors*, and *blood glucose monitors* are a few examples of power-sensitive systems that benefit from this SAR ADC design. The values in the component selection section can be adjusted to allow for different data throughput rates and different bandwidth amplifiers. *Low-Power Sensor Measurements: 3.3V, 1ksps, 12-bit Single-Ended, Single Supply* shows a simplified version of this circuit where the negative supply is grounded. The –0.3-V negative supply in this example is used to achieve the best possible linear input signal range. See *SAR ADC Power Scaling* for a detailed description of trade-offs in low-power SAR design.



Specifications

Specification	Calculated	Simulated	Measured
Transient ADC Input Settling (1ksps)	< 0.5 × LSB = 402μV	41.6μV	N/A
AVDD Supply Current (1ksps)	230nA	N/A	214.8nA
AVDD Supply Power (1ksps)	759nW	N/A	709nW
VDD OPAMP Supply Current	450nA	N/A	431.6nA
VDD OPAMP Supply Power	2.025μW	N/A	1.942μW
AVDD + VDD System Power (1ksps)	2.784μW	N/A	2.651μW

Design Notes

1. Determine the linear range of the op amp based on common mode, output swing, and linear open loop gain specification. This is covered in the component selection section.
2. Select a COG (NPO) capacitor for Cfilt to minimize distortion.
3. The *TI Precision Labs – ADCs* training video series covers methods for selecting the charge bucket circuit Rfilt and Cfilt (see *Introduction to SAR ADC Front-End Component Selection*). These component values are dependent on the amplifier bandwidth, data converter sampling rate, and data converter design. The values shown here provide good settling and AC performance for the amplifier and data converter in this example. Modifying the design requires selection of a different RC filter.

Component Selection

1. Select a low-power op amp:
   - Supply current < 0.5μA
   - Gain bandwidth product > 5kHz (five times the sampling rate)
   - Unity gain stable
   - LPV811 – 450-nA supply current, 8-kHz gain bandwidth product, unity gain stable
2. Find op amp maximum and minimum output for linear operation:

$$V_{ee} + 0\ V < V_{out} < V_{dd} - 0.9\ V \quad \text{from} \quad \text{LPV811} \quad V_{cm} \quad \text{specification}$$

$$V_{ee} + 10\ mV < V_{out} < V_{dd} - 10\ mV \quad \text{from} \quad \text{LPV811} \quad \text{Vout} \quad \text{swing} \quad \text{specification}$$

$$V_{ee} + 0.3\ V < V_{out} < V_{dd} - 0.3\ V \quad \text{from} \quad \text{LPV811} \quad \text{Aol} \quad \text{linear} \quad \text{region} \quad \text{specification}$$

3. Typical power calculations (at 1ksps) with expected values. See *SAR ADC Power Scaling* for a detailed description of trade-offs in low-power SAR design:

$$P_{AVDD} = I_{AVDD\_AVG} \times AVDD = 230\ nA \times 3.3\ V = 759\ nW$$

$$P_{LPV811} = I_{LPV811} \times (V_{dd} - V_{ee}) = 450\ nA \times [4.5\ V - (-0.3\ V)] = 2.16\ \mu W$$

$$P_{total} = P_{AVDD} + P_{LPV811} = 759\ nW + 2.16\ \mu W = 2.919\ \mu W$$

4. Typical power calculations (at 1ksps) with measured values:

$$P_{AVDD} = I_{AVDD\_AVG} \times AVDD = 214.8\ nA \times 3.3\ V = 708.8\ nW$$

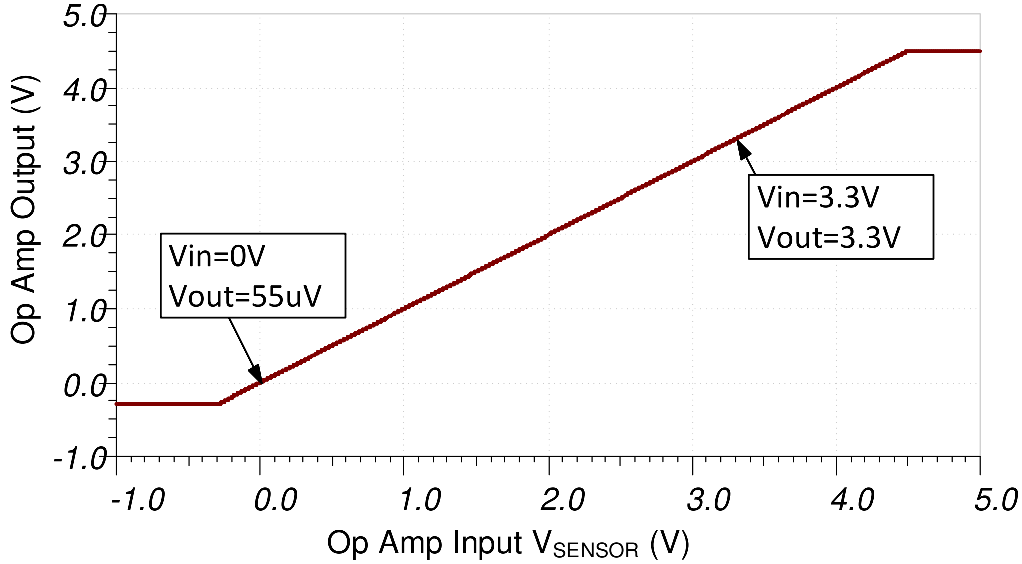
$$P_{LPV811} = I_{LPV811} \times (V_{dd} - V_{ee}) = 431.6\ nA \times [4.5\ V - (-0.3\ V)] = 2.071\ \mu W$$

$$P_{total} = P_{AVDD} + P_{LPV811} = 708.8\ nW + 2.071\ \mu W = 2.780\ \mu W$$

5. Find Rfilt and Cfilt to allow for settling at 1ksps. Refer to *Refine the Rfilt and Cfilt Values* (a *Precision Labs* video) for the algorithm to select Rfilt and Cfilt. The final value of 200kΩ and 510pF proved to settle to well below ½ of a least significant bit (LSB).

DC Transfer Characteristics

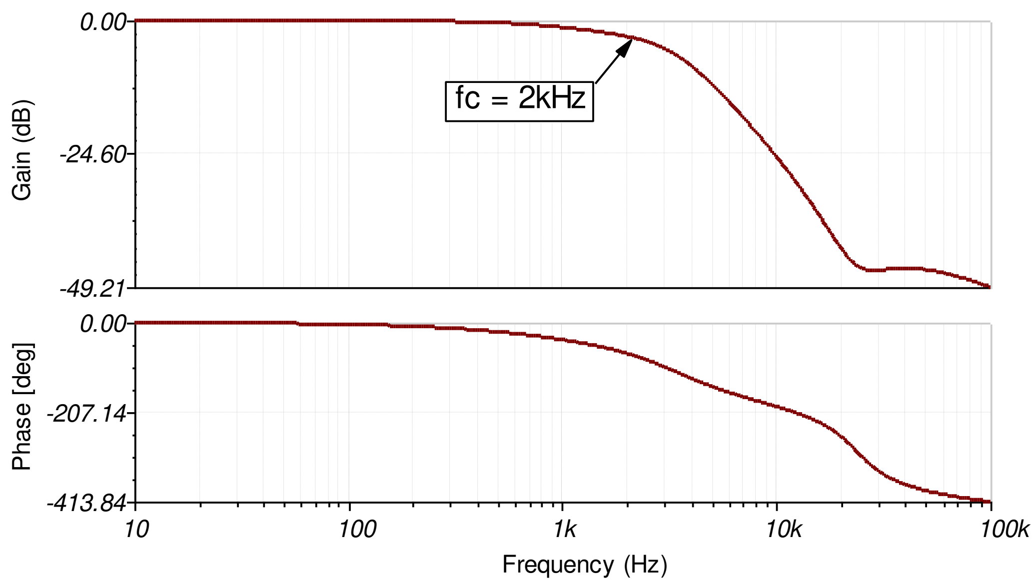
The following graph shows a linear output response for inputs from 0 to 3.3V. The full-scale range (FSR) of the ADC falls within the linear range of the op amp. Refer to *Determining a SAR ADC's Linear Range when using Operational Amplifiers* for detailed theory on this subject.



AC Transfer Characteristics

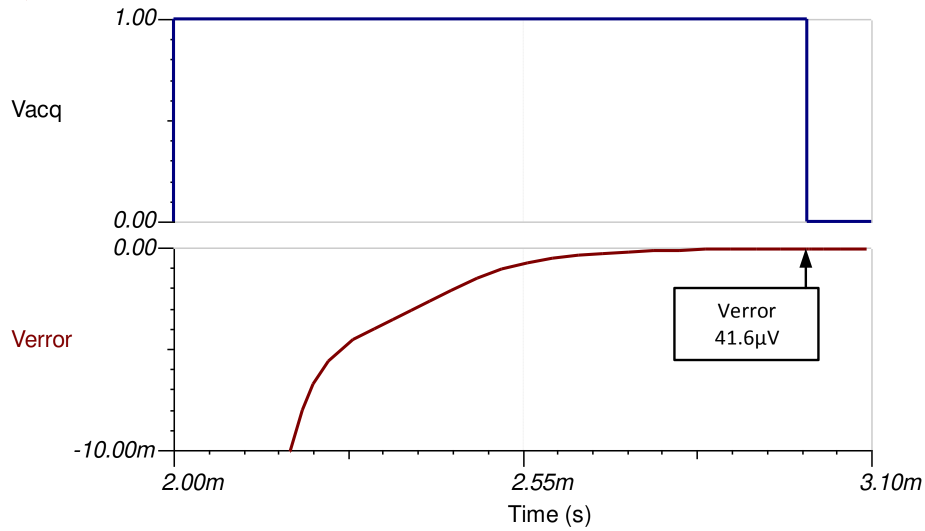
The bandwidth simulation includes the effects of the amplifier output impedance and the RC charge bucket circuit (R_{filt} and C_{filt}).The bandwidth of the RC circuit is shown in the following equation as 1.56kHz. The simulated bandwidth of 2 kHz includes effects from the output impedance interacting with the impedance of the load. See *TI Precision Labs - Op Amps: Bandwidth 1* for more details on this subject.

$$f_c = \frac{1}{2 \times \pi \times R_{filt} \times C_{filt}} = \frac{1}{2 \times \pi \times (200\ k\Omega) \times (510\ pF)} = 1.56\ kHz$$



Transient ADC Input Settling Simulation

The following simulation shows settling to a 3-V DC input signal. This type of simulation shows that the sample and hold kickback circuit is properly selected to within ½ of an LSB (402µV). Refer to *Introduction to SAR ADC Front-End Component Selection* for detailed theory on this subject.



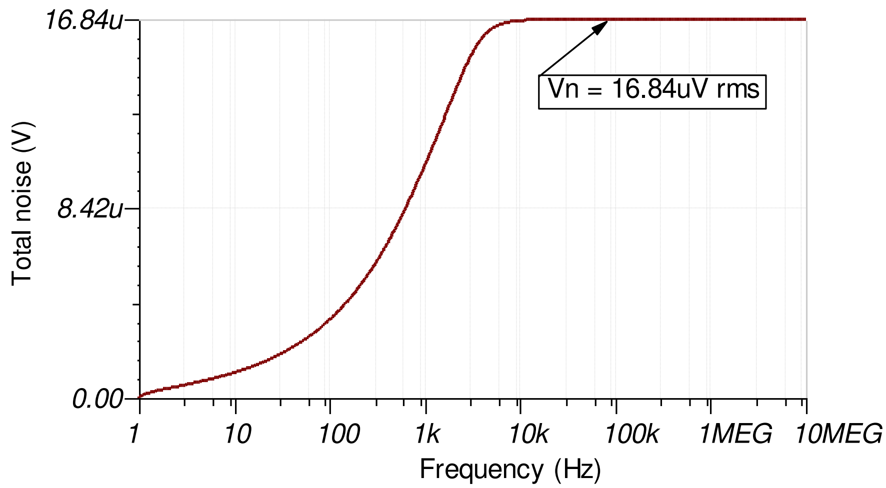
Noise Simulation

This section walks through a simplified noise calculation for a rough estimate. The resistor noise in this calculation is neglected because it is attenuated for frequencies greater than 10 kHz.

$$f_c = \frac{1}{2 \times \pi \times R_{filt} \times C_{filt}} = \frac{1}{2 \times \pi \times 200\ k\Omega \times 510\ pF} = 1560\ Hz$$

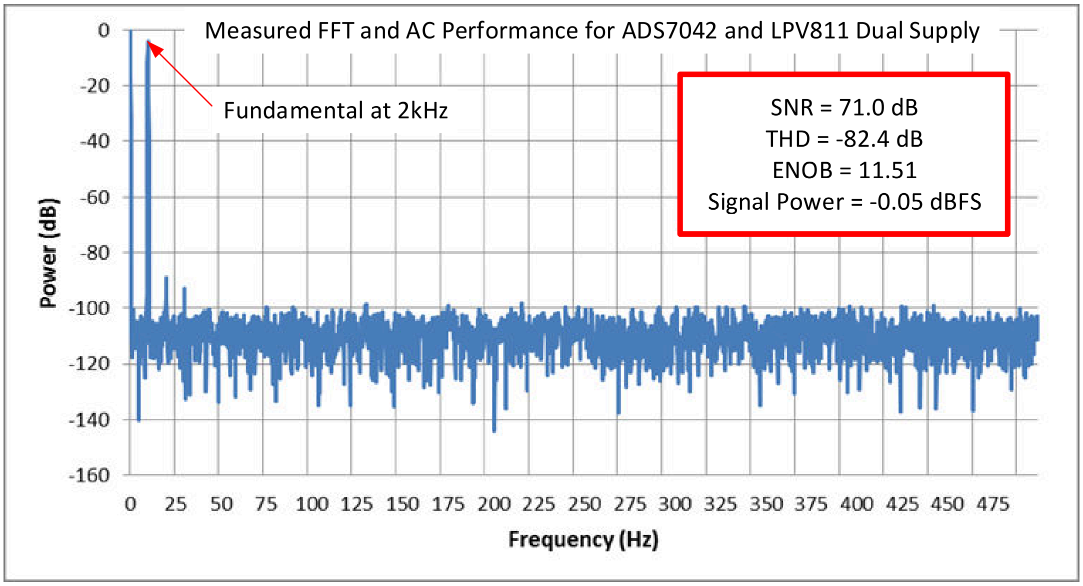
$$E_n = e_{n811} \times \sqrt{K_n \times f_c} = \frac{340\ nV}{\sqrt{Hz}} \times \sqrt{1.57 \times 1560\ Hz} = 16.8\ \mu V$$

Note that the calculated and simulated values match well. Refer to *Calculating the Total Noise for ADC Systems* for detailed theory on this subject.



Measure FFT

This performance was measured on a modified version of the ADS7042EVM with a 10-Hz input sine wave. The AC performance indicates SNR = 71.0dB, THD = –82.4dB, and ENOB (effective number of bits) = 11.51, which matches well with the specified performance of the ADC, SNR = 70dB and THD = –80dB. This test was performed at room temperature. See *Introduction to Frequency Domain* for more details on this subject.



Design Featured Devices

Device	Key Features	Link	Similar Devices
ADS7042 (1)	12-bit resolution, SPI, 1-Msps sample rate, single-ended input, AVDD reference input range 1.6V to 3.6V.	12-Bit 1MSPS Ultra-Low-Power Ultra-Small-Size SAR ADC With SPI Interface	Analog-to-digital converters (ADCs)
LPV811 (2)	8-kHz bandwidth, rail-to-rail output, 450-nA supply current, unity gain stable	Single Channel 450nA Precision Nanopower Operational Amplifier	Operational amplifiers (op amps)

(1) The ADS7042 uses the AVDD as the reference input. Use a high-PSRR LDO, such as the TPS7A47, as the power supply.
(2) The LPV811 is also commonly used in low-speed applications for sensors. Furthermore, the rail-to-rail output allows for linear swing across the entire ADC input range.

Link to Key Files (TINA)

Texas Instruments, SBAM342 circuit, design files

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (March 2019) to Revision B (September 2024) **Page**

- Updated the format for tables, figures, and cross-references throughout the document.................................. 1

Changes from Revision * (November 2017) to Revision A (March 2019) **Page**

- Downstyle the title and changed title role to 'Data Converters'.. 1
- Added link to circuit cookbook landing page.. 1

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