TVS0500 5-V Flat-Clamp Surge Protection Device

1 Features

- Protection Against 2 kV, 42 Ω IEC 61000-4-5 Surge Test for Industrial Signal Lines
- Max Clamping Voltage of 9.2 V at 43 A of 8/20 µs Surge Current
- Standoff Voltage: 5 V
- Tiny 4 mm^2 Footprint
- Survives over 5,000 Repetitive Strikes of 35 A 8/20 µs Surge Current at 125°C
- Robust Surge Protection:
  - IEC61000-4-5 (8/20 µs): 43 A
  - IEC61643-321 (10/1000 µs): 22 A
- Low Leakage Current
  - 70 pA typical at 27°C
  - 6.5 nA typical at 85°C
- Low Capacitance: 155 pF
- Integrated Level 4 IEC 61000-4-2 ESD Protection

2 Applications

- Industrial Sensors
- PLC I/O Modules
- 5 V Power Lines
- Appliances
- Medical Equipment
- Smart Meters

3 Description

The TVS0500 robustly shunts up to 43 A of IEC 61000-4-5 fault current to protect systems from high power transients or lightning strikes. The device offers a solution to the common industrial signal line EMC requirement to survive up to 2 kV IEC 61000-4-5 open circuit voltage coupled through a 42 Ω impedance. The TVS0500 uses a unique feedback mechanism to ensure precise flat clamping during a fault, assuring system exposure below 10 V. The tight voltage regulation allows designers to confidently select system components with a lower voltage tolerance, lowering system costs and complexity without sacrificing robustness.

In addition, the TVS0500 is available in a small 2 mm × 2 mm SON footprint which is ideal for space constrained applications, offering a 70 percent reduction in size compared to industry standard SMA and SMB packages. The extremely low device leakage and capacitance ensure a minimal effect on the protected line. To ensure robust protection over the lifetime of the product, TI tests the TVS0500 against 5000 repetitive surge strikes at high temperature with no shift in device performance.

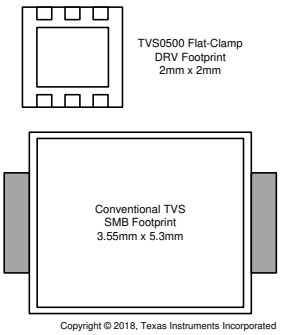
The TVS0500 is part of TI's Flat-Clamp family of surge devices. For more information on the other devices in the family, see the *Device Comparison Table*

Device Information(1)

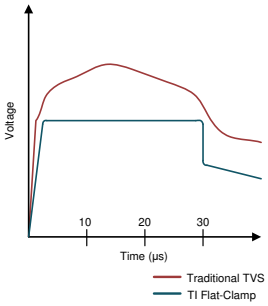
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TVS0500	SON (6)	2.00 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Footprint Comparison



Voltage Clamp Response to 8/20 µs Surge Event



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4 Revision History

Changes from Revision B (February 2018) to Revision C **Page**

- Fixed grammar error in the *Reliability Testing* section ... 9

Changes from Revision A (February 2018) to Revision B **Page**

- Changed DC Breakdown Current MAX from 100 to 50 in the Specifications *Absolute Maximum Ratings* table ... 5
- Changed Break-down Voltage MIN from 7.6 to 7.5 and MAX from 8.2 to 8.4 in the Specifications *Electrical Characteristics* table ... 5

Changes from Original (December 2017) to Revision A **Page**

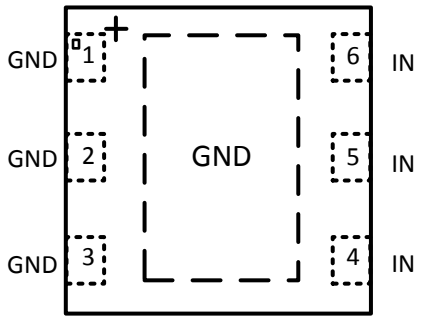
- Changed device document status from Advance Information to Production Data ... 1

5 Device Comparison Table

Device	V_{rwm}	V_{clamp} at I_{pp}	I_{pp} (8/20 µs)	V_{rwm} leakage (nA)	Package Options	Polarity
TVS0500	5	9.2	43	0.07	SON	Unidirectional
TVS1400	14	18.4	43	2	SON	Unidirectional
TVS1800	18	22.8	40	0.5	SON	Unidirectional
TVS2200	22	27.7	40	3.2	SON	Unidirectional
TVS2700	27	32.5	40	1.7	SON	Unidirectional
TVS3300	33	38	35	19	WCSP, SON	Unidirectional

6 Pin Configuration and Functions

DRV Package
6-Pin SON
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	No.		
IN	4, 5, 6	I	ESD and surge protected channel
GND	1, 2, 3, exposed thermal pad	GND	Ground

7 Specifications

7.1 Absolute Maximum Ratings

T_A = 27°C (unless otherwise noted)(1)

		MIN	MAX	UNIT
Maximum Surge	IEC 61000-4-5 Current (8/20 µs)		43	A
	IEC 61000-4-5 Power (8/20 µs)		400	W
	IEC 61643-321 Current (10/1000 µs)		20	A
	IEC 61643-321 Power (10/1000 µs)		180	W
Maximum Forward Surge	IEC 61000-4-5 Current (8/20 µs)		50	A
	IEC 61000-4-5 Power (8/20 µs)		80	W
	IEC 61643-321 Current (10/1000 µs)		23	A
	IEC 61643-321 Power (10/1000 µs)		60	W
EFT	IEC 61000-4-4 EFT Protection		80	A
I_{BR}	DC Breakdown Current		50	mA
I_F	DC Forward Current		500	mA
T_A	Ambient Operating Temperature	-40	125	°C
T_{stg}	Storage Temperature	-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings - JEDEC

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 ESD Ratings - IEC

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 contact discharge	±24	kV
		IEC 61000-4-2 air-gap discharge	±30	

7.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	NOM	MAX	UNIT
V_{RWM}	Reverse Stand-off Voltage		5		V

7.5 Thermal Information

THERMAL METRIC(1)		TVS0500 DRV (SON) 6 PINS	UNIT
R_{qJA}	Junction-to-ambient thermal resistance	70.4	°C/W
$R_{qJC(top)}$	Junction-to-case (top) thermal resistance	73.7	°C/W
R_{qJB}	Junction-to-board thermal resistance	40	°C/W
Y_{JT}	Junction-to-top characterization parameter	2.2	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

Thermal Information (continued)

THERMAL METRIC(1)		TVS0500 DRV (SON) 6 PINS	UNIT
Y_{JB}	Junction-to-board characterization parameter	40.3	°C/W
$R_{qJC(bot)}$	Junction-to-case (bottom) thermal resistance	11	°C/W

7.6 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{LEAK}	Leakage Current	Measured at $V_{IN} = V_{RWM}$, T_A = 27°C		0.07	5.5	nA
		Measured at $V_{IN} = V_{RWM}$, T_A = 85°C		6.5	220	nA
		Measured at $V_{IN} = V_{RWM}$, T_A = 105°C		38	755	nA
V_F	Forward Voltage	I_{IN} = 1 mA from GND to IO	0.25	0.5	0.65	V
V_{BR}	Break-down Voltage	I_{IN} = 1 mA from IO to GND	7.5	7.9	8.4	V
V_{FCLAMP}	Forward Clamp Voltage	35 A IEC 61000-4-5 Surge (8/20 µs) from GND to IO, 27°C		2	5	V
V_{CLAMP}	Clamp Voltage	24 A IEC 61000-4-5 Surge (8/20 µs) from IO to GND, V_{IN} = 0 V before surge, 27°C		8.6	8.8	V
		43 A IEC 61000-4-5 Surge (8/20 µs) from IO to GND, V_{IN} = 0 V before surge, 27°C		9.2	9.5	V
		35 A IEC 61000-4-5 Surge (8/20 µs) from IO to GND, $V_{IN} = V_{RWM}$ before surge, T_A = 125°C		9.2	9.5	V
R_{DYN}	8/20 µs surge dynamic resistance	Calculated from V_{CLAMP} at .5*I_{pp} and I_{pp} surge current levels, 27°C		30	50	mΩ
C_{IN}	Input pin capacitance	V_{IN} = 5 V, f = 1 MHz, 30 mV_{pp}, IO to GND		155		pF
SR	Maximum Slew Rate	0-V_{RWM} rising edge, sweep rise time and measure slew rate when I_{PEAK} = 1 mA, 27°C		2.5		V/µs
		0-V_{RWM} rising edge, sweep rise time and measure slew rate when I_{PEAK} = 1 mA, 105°C		0.7		V/µs

7.7 Typical Characteristics

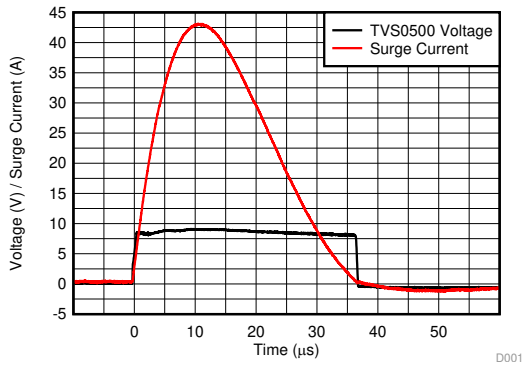


Figure 1. 8/20 µs Surge Response at 43 A

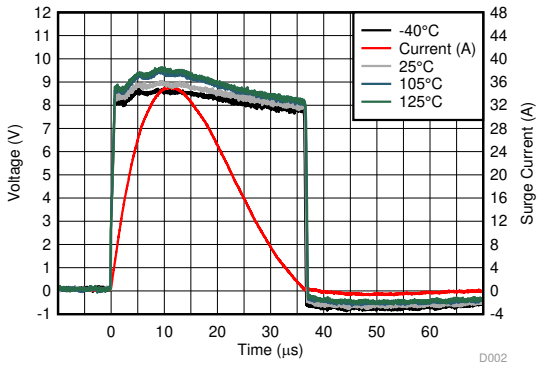
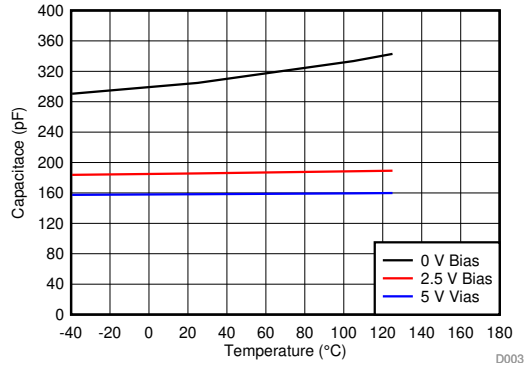


Figure 2. 8/20 µs Surge Response at 35 A Across Temperature



f = 1 MHz, 30 mVpp, IO to GND

Figure 3. Capacitance vs Temperature Across Bias

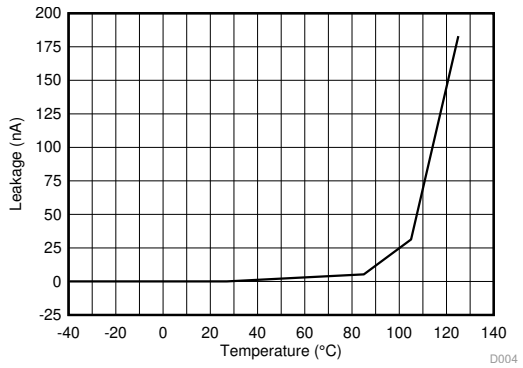


Figure 4. Leakage Current vs Temperature at 5 V

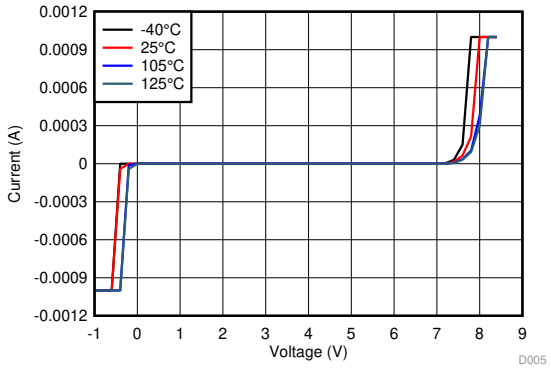


Figure 5. I/V Curve Across Temperature

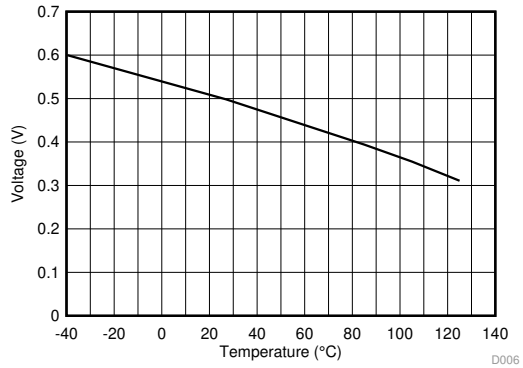


Figure 6. Forward Voltage vs Temperature

Typical Characteristics (continued)

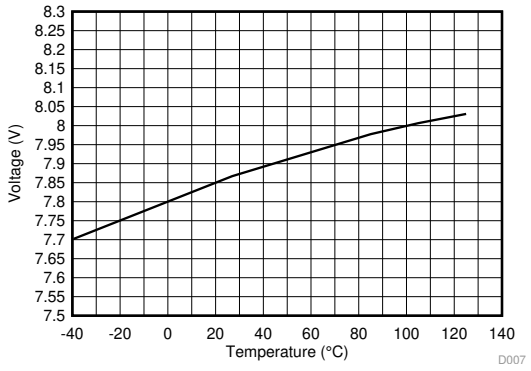


Figure 7. Breakdown Voltage (1 mA) vs Temperature

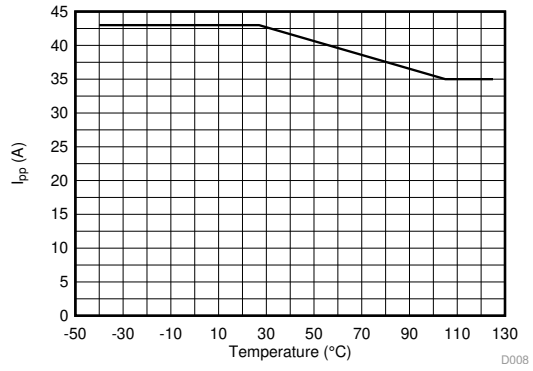


Figure 8. Max Surge Current (8/20 µs) vs Temperature

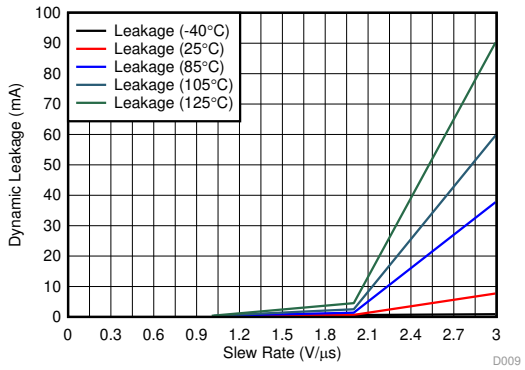


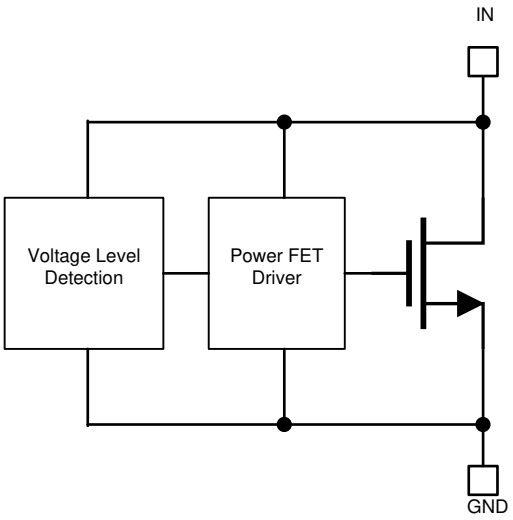
Figure 9. Dynamic Leakage vs Signal Slew Rate across Temperature

8 Detailed Description

8.1 Overview

The TVS0500 is a precision clamp with a low, flat clamping voltage during transient overvoltage events like surge and protecting the system with zero voltage overshoot.

8.2 Functional Block Diagram



8.3 Feature Description

The TVS0500 is a precision clamp that handles 43 A of IEC 61000-4-5 8/20 µs surge pulse. The flat clamping feature helps keep the clamping voltage very low to keep the downstream circuits from being stressed. The flat clamping feature can also help end-equipment designers save cost by opening up the possibility to use lower-cost, lower voltage tolerant downstream ICs. The TVS0500 has minimal leakage under the standoff voltage of 5 V, making it an ideal candidate for applications where low leakage and power dissipation is a necessity. IEC 61000-4-2 and IEC 61000-4-4 ratings make it a robust protection solution for ESD and EFT events. Wide ambient temperature range of –40°C to +125°C a good candidate for most applications. Compact packages enable it to be used in small devices and save board area.

8.4 Reliability Testing

To ensure device reliability, the TVS0500 is characterized against 5000 repetitive pulses of 35 A IEC 61000-4-5 8/20 µs surge pulses at 125°C. The test is performed with less than 10 seconds between each pulse at high temperature to simulate worst case scenarios for fault regulation. After each surge pulse, the TVS0500 clamping voltage, breakdown voltage, and leakage are recorded to ensure that there is no variation or performance degradation. By ensuring robust, reliable, high temperature protection, the TVS0500 enables fault protection in applications that must withstand years of continuous operation with no performance change.

8.5 Device Functional Modes

8.5.1 Protection Specifications

The TVS0500 is specified according to both the IEC 61000-4-5 and IEC 61643-321 standards. This enables usage in systems regardless of which standard is required in relevant product standards or best matches measured fault conditions. The IEC 61000-4-5 standards requires protection against a pulse with a rise time of 8 µs and a half length of 20 µs, while the IEC 61643-321 standard requires protection against a much longer pulse with a rise time of 10 µs and a half length of 1000 µs.

Device Functional Modes (continued)

The positive and negative surges are imposed to the TVS0500 by a combinational waveform generator (CWG) with a 2-Ω coupling resistor at different peak voltage levels. For powered on transient tests that need power supply bias, inductances are usually used to decouple the transient stress and protect the power supply. The TVS0500 is post tested by assuring that there is no shift in device breakdown or leakage at V_{rwm}.

In addition, the TVS0500 has been tested according to IEC 61000-4-5 to pass a ±2 kV surge test through a 42-Ω coupling resistor and a 0.5 µF capacitor. This test is a common test requirement for industrial signal I/O lines and the TVS0500 will serve an ideal protection solution for applications with that requirement.

The TVS0500 allow integrates IEC 61000-4-2 level 4 ESD Protection and 80 A of IEC 61000-4-4 EFT Protection. These combine to ensure that the device can protect against most transient conditions regardless of length or type.

For more information on TI's test methods for Surge, ESD, and EFT testing, reference TI's IEC 61000-4-x Testing Application Note

8.5.2 Minimal Derating

Unlike traditional diodes the TVS0500 has very little derating of max power dissipation and ensures robust performance up to 125°C, shown in Figure 8. Traditional TVS diodes lose up to 50% of their current carrying capability when at high temperatures, so a surge pulse above 85°C ambient can cause failures that are not seen at room temperature. The TVS0500 prevents this and ensures that you will see the same level of protection regardless of temperature.

8.5.3 Transient Performance

During large transient swings, the TVS0500 will begin clamping the input signal to protect downstream conditions. While this prevents damage during fault conditions, it can cause leakage when the intended input signal has a fast slew rate. In order to keep power dissipation low and remove the chance of signal distortion, it is recommended to keep the slew rate of any input signal on the TVS0500 below 2.5 V/µs at room temperature and below 0.7 V/µs at 125°C shown in Figure 9. Faster slew rates will cause the device to clamp the input signal and draw current through the device for a few microseconds, increasing the rise time of the signal. This will not cause any harm to the system or to the device, however if the fast input voltage swings occur regularly it can cause device overheating.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TVS0500 can be used to protect any power, analog, or digital signal from transient fault conditions caused by the environment or other electrical components.

9.2 Typical Application

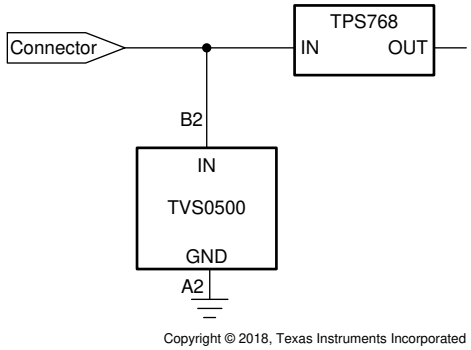


Figure 10. TVS0500 Application Schematic

9.2.1 Design Requirements

A typical operation for the TVS0500 would be protecting a nominal 5 V input to an LDO similar to Figure 10. In this example, the TVS0500 is protecting the input to a TPS768, a standard 1 A LDO with an input voltage range of 2.7 V to 10 V. Without any input protection, if a surge event is caused by lightning, coupling, ringing, or any other fault condition this input voltage will rise to hundreds of volts for multiple microseconds, violating the absolute maximum input voltage and harming the device. An ideal surge protection diode will maximize the useable voltage range while still clamping at a safe level for the system, TI's Flat-Clamp technology provides the best protection solution.

9.2.2 Detailed Design Procedure

If the TVS0500 is in place to protect the device, during a surge event the voltage will rise to the breakdown of the diode at 7.9 V, and then the TVS0500 will turn on, shunting the surge current to ground. With the low dynamic resistance of the TVS0500, large amounts of surge current will have minimal impact on the clamping voltage. The dynamic resistance of the TVS0500 is around 30 mΩ, which means 30 A of surge current will cause a voltage raise of 30 A × 30 mΩ = 0.9 V. Because the device turns on at 7.9 V, this means the LDO input will be exposed to a maximum of 7.9 V + 0.9 V = 8.8 V during surge pulses, well within the absolute maximum input voltage. This ensures robust protection of your circuit.

The small size of the device also improves fault protection by lowering the effect of fault current coupling onto neighboring traces. The small form factor of the TVS0500 allows the device to be placed extremely close to the input connector, lowering the length of the path fault current will take through the system compared to larger protection solutions.

Finally, the low leakage of the TVS0500 will have low input power losses. At 5 V, the device will see typical 70 pA leakage for a constant power dissipation of less than 1 nW, a negligible quantity that will not effect overall efficiency metrics or add heating concerns.

Typical Application (continued)

9.2.3 Configuration Options

The TVS0500 can be used in either unidirectional or bidirectional configuration. Figure 10 shows unidirectional usage to protect an input. By placing two TVS0500's in series with reverse orientation, bidirectional operation can be used, allowing a working voltage of ±5 V. TVS0500 operation in bidirectional will be similar to unidirectional operation, with a minor increase in breakdown voltage and clamping voltage. The TVS3300 bidirectional performance has been characterized in the TVS3300 Configurations Characterization. While the TVS0500 in bidirectional configuration has not specifically been characterized, it will have similar relative changes to the TVS3300 in bidirectional configuration.

10 Power Supply Recommendations

The TVS0500 is a clamping device so there is no need to power it. To ensure the device functions properly do not violate the recommended V_{IN} voltage range (0 V to 5 V) .

11 Layout

11.1 Layout Guidelines

The optimum placement is close to the connector. EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures. The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.

Route the protected traces straight.

Eliminate any sharp corners on the protected traces between the TVS0500 and the connector by using rounded corners with the largest radii possible. Electric fields tend to build up on corners, increasing EMI coupling.

11.2 Layout Example

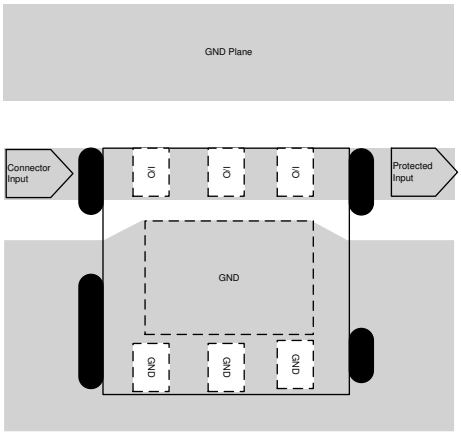


Figure 11. TVS0500 Layout

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Community Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.3 Trademarks

E2E is a trademark of Texas Instruments.

12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TVS0500DRVR	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1HRH
TVS0500DRVR.A	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1HRH
TVS0500DRVRG4	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1HRH
TVS0500DRVRG4.A	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1HRH

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

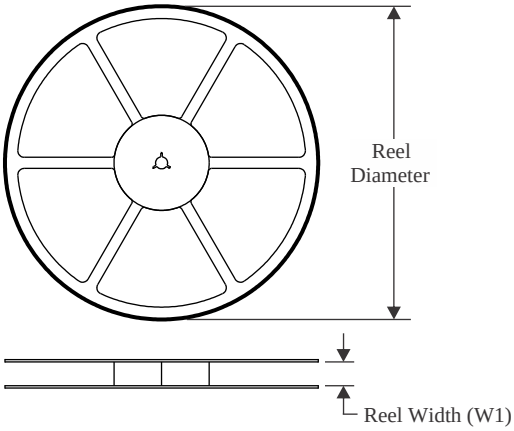
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

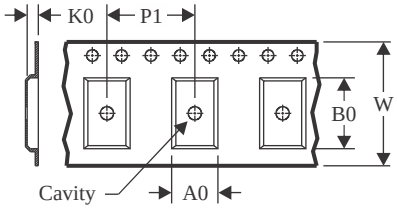
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

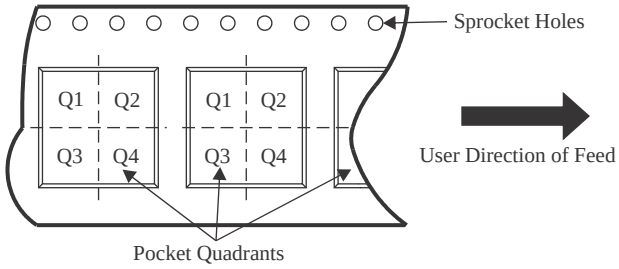


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

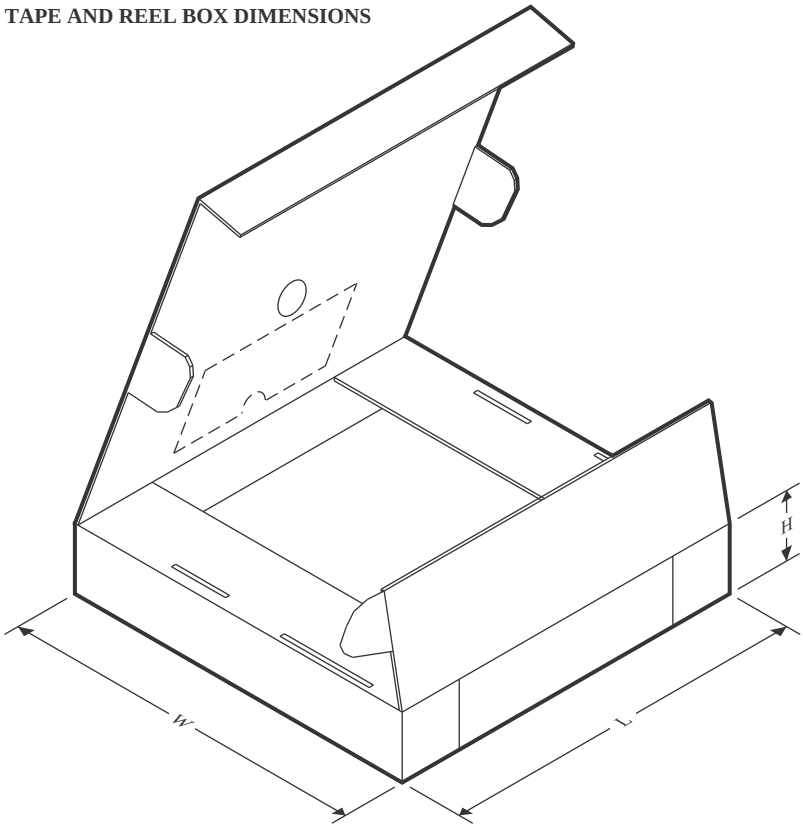
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TVS0500DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TVS0500DRVRG4	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS

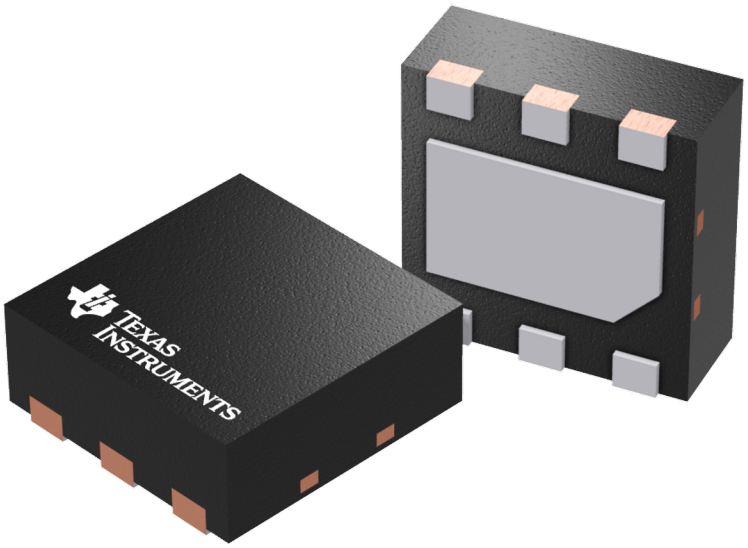


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TVS0500DRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TVS0500DRVRG4	WSON	DRV	6	3000	210.0	185.0	35.0

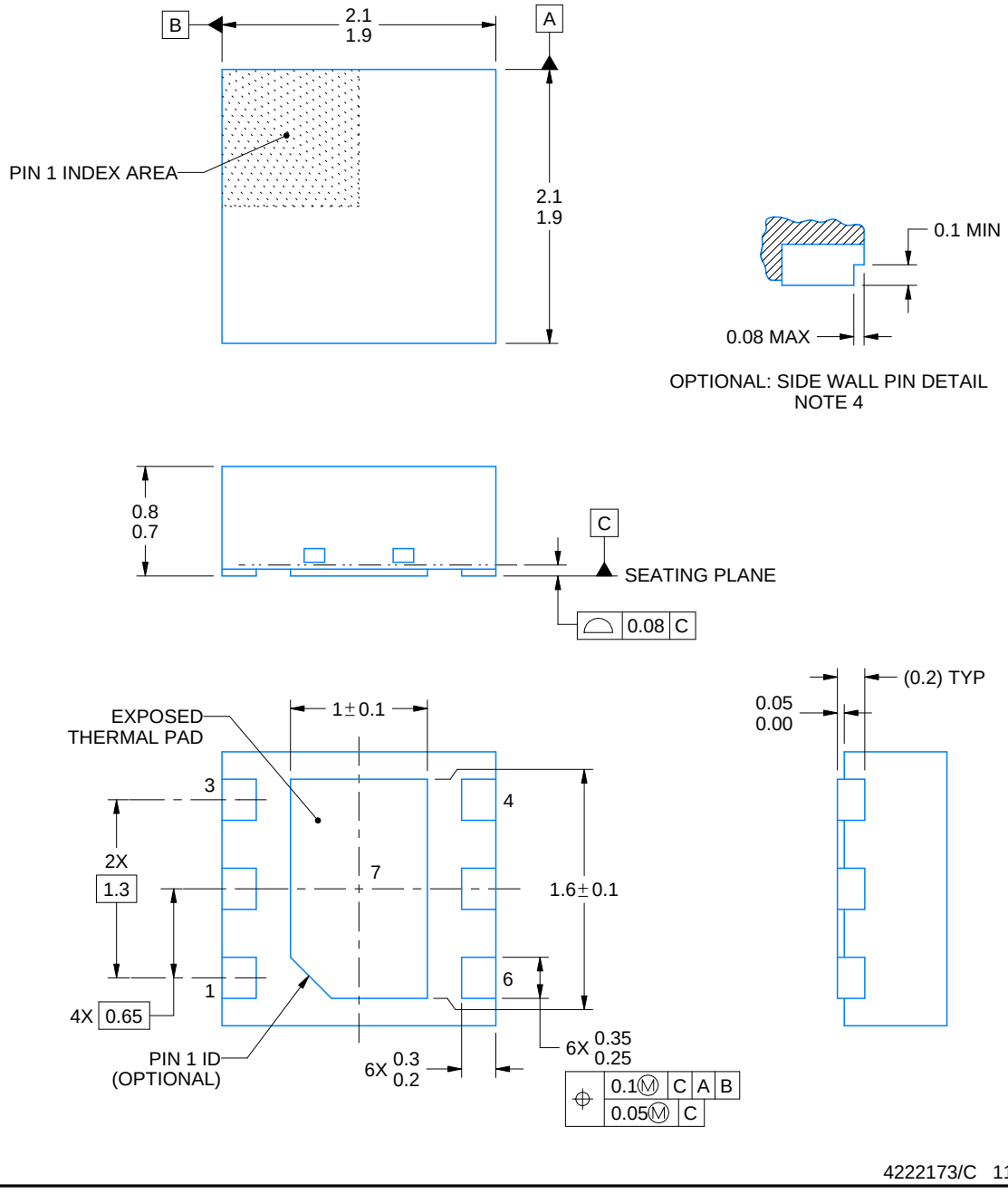
DRV 6 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



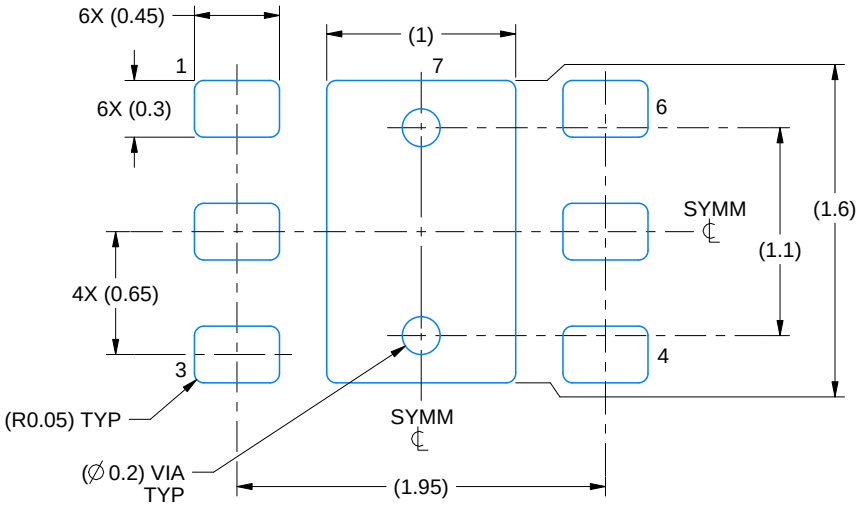
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PLASTIC SMALL OUTLINE - NO LEAD

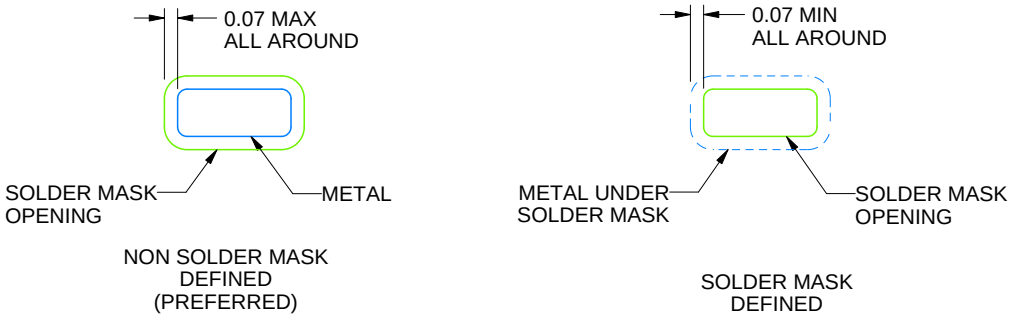


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Minimum 0.1 mm solder wetting on pin side wall. Available for wettable flank version only.



LAND PATTERN EXAMPLE
SCALE:25X



SOLDER MASK DETAILS

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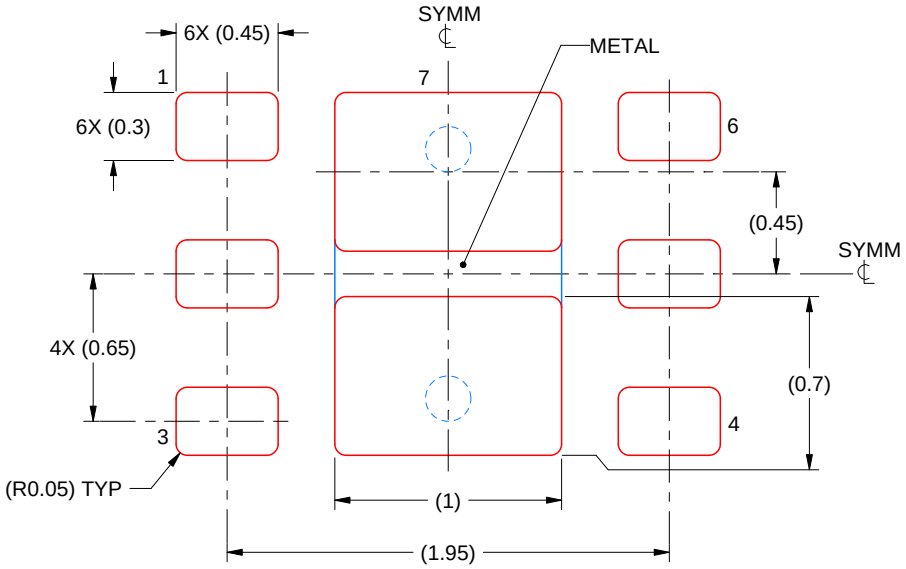
NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
6. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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Last updated 10/2025