TPS796 Ultra-Low-Noise, High PSRR, Fast, RF, 1A Low-Dropout Linear Regulator

1 Features

- 1A low-dropout regulator with enable
- Available in fixed and adjustable (1.2V to 5.5V)
- Low output noise:
  - 54μV_{RMS} (legacy chip)
  - 78μV_{RMS} (new chip)
- Stable with a 1µF ceramic capacitor
- Excellent load and line transient response
- Very low dropout voltage: 220mV (typ) at 1A
- Packages:
  - 3mm × 3mm VSON (DRB)
  - SOT223-6 (DCQ)
  - TO-263 (KTT)

2 Applications

- TV applications
- Building automation
- Connected peripherals and printers
- Home theater and entertainment applications

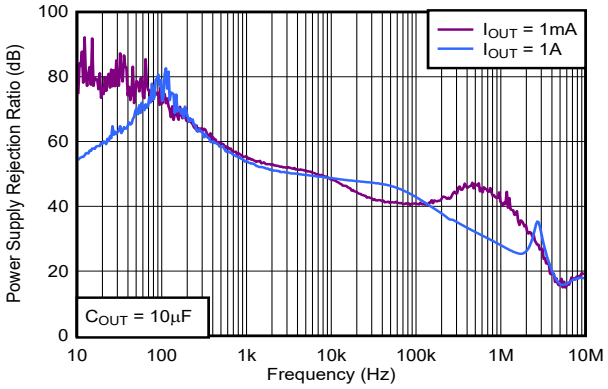
3 Description

The TPS796 low-dropout (LDO) low-power linear voltage regulator features high power-supply rejection ratio (PSRR), low-noise, fast start-up, and excellent line and load transient responses in small outline, 3mm × 3mm VSON, SOT223-6, and TO-263 packages. Tis device is stable with a small, 1µF ceramic capacitor on the output. The TPS796 offers low dropout voltages (for example, 220mV at 1A). Applications with analog components that are noise sensitive (such as portable RF electronics) benefit from the high-PSRR, low-noise features, and need fast response time.

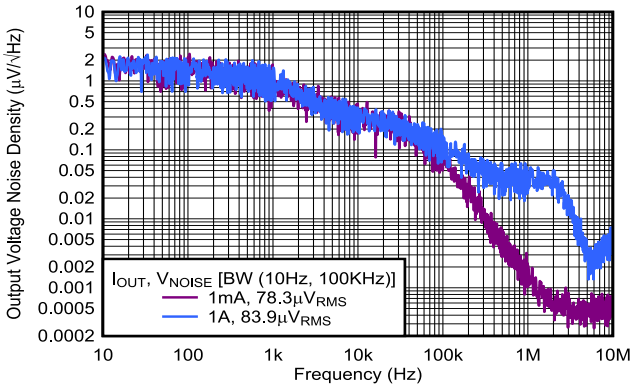
Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TPS796	DRB (VSON, 8)	3mm × 3mm
	DCQ (SOT-223, 6)	6.5mm × 7.06mm
	KTT (TO-263, 5)	10.16mm × 15.24mm

(1) For more information, see the *Mechanical, Packaging, and Orderable Information*.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Ripple Rejection vs Frequency



Output Spectral Noise Density vs Frequency

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4 Pin Configuration and Functions

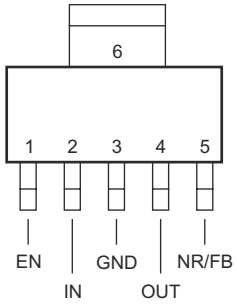


Figure 4-1. DCQ Package, 6-Pin SOT-223 (Top View, Legacy Chip)

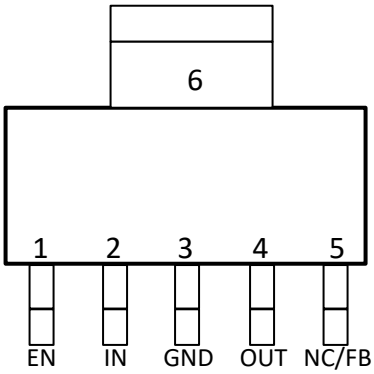


Figure 4-2. DCQ Package, 6-Pin SOT-223 (Top View, New Chip)

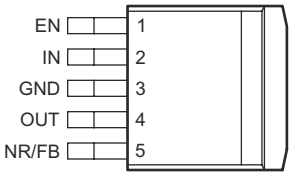


Figure 4-3. KTT Package, 5-Pin TO-263 (Top View, Legacy Chip)

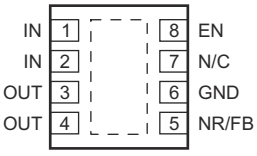


Figure 4-4. DRB Package, 8-Pin VSON (Top View, Legacy Chip)

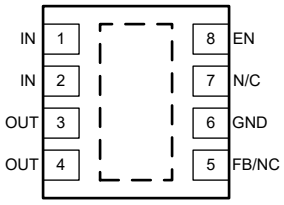


Figure 4-5. DRB Package, 8-Pin VSON (Top View, New Chip)

Table 4-1. Pin Functions

PIN			TYPE[1]	DESCRIPTION
NAME	SOT-223 TO-263	VSON		
EN	1	8	I	Enable pin. Driving the enable pin (EN) high turns on the regulator. Driving this pin low puts the regulator into shutdown mode. EN can be connected to IN if not used.
FB	5	5	I	Feedback pin. This terminal is the feedback input voltage for the adjustable device.
GND	3, Tab	6, PowerPAD	—	Regulator ground
IN	2	1, 2	I	Input to the device.
N/C	5	7	—	Not internally connected. This pin must either be left open, or tied to GND.
NR	5	5	—	Noise-reduction pin (legacy chip). Connecting an external capacitor to this pin bypasses noise generated by the internal band gap. This bypass improves power-supply rejection and reduces output noise. For a lower noise performance device, consider the TPS7A91.
OUT	4	3, 4	O	Output of the regulator.

(1) I=Input; O=Output

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	Supply, V_{IN} (New chip)	–0.3	6.5	V
	Supply, V_{IN} (Legacy chip)	–0.3	6	
	Enable, V_{EN}	–0.3	V_{IN} + 0.3	
	Output, V_{OUT}	–0.3	6	
Current	Output, I_{OUT}	Internally limited		
Temperature	Operating junction, T_J	–40	150	°C
	Storage, T_{stg}	–65	150	

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
$V_{(ESD)}$	Electrostatic discharge	Charged device model (CDM), per JEDEC specification JESD22C101, V all pins(2)	±500	V

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{IN}	Input supply voltage (legacy chip)		2.7		5.5	V
	Input supply voltage (new chip)		2.7		6.0	
C_{IN}	Input capacitor		2.2			µF
C_{OUT}	Output capacitor		1[1]		200	
C_{FF}	Feed-forward capacitor (new chip)		0	10	100	nF
I_{OUT}	Output current		0		1	A
V_{EN}	Enable voltage (legacy chip)		0		5.5	V
	Enable voltage (new chip)		0		6.0	
F_{EN}	Enable toggle frequency (new chip)				10	kHz
Tj	Junction Temperature		–40		125	°C

(1) The minimum effective capacitance is 0.47 µF.

5.4 Thermal Information

THERMAL METRIC[1]		TPS796					UNIT
		DRB (VSON)		DCQ (SOT223-6)		KTT (TO-263)	
		8 PINS [2]	8 PINS [3]	6 PINS [2]	6 PINS [3]	5 PINS [2]	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	47.8	54.7	70.4	71.1	25	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	83	76.1	70	41.6	35	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	N/A	30.1	N/A	8.8	N/A	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.1	6.6	6.8	3.5	1.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	17.8	30.2	30.1	8.5	8.52	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	12.1	16.7	6.3	6	0.4	°C/W

(1) For more information about traditional and new thermal metrics, see the "Semiconductor and IC Package Thermal Metrics" application note.
(2) Legacy chip.
(3) New chip.

5.5 Electrical Characteristics

at operating temperature range (T_J = –40°C to +125°C), $V_{EN} = V_{IN}$, $V_{IN} = V_{OUT(nom)}$ + 1V (1), I_{OUT} = 1mA, and C_{OUT} = 10µF and C_{NR} = 0.01µF(Legacy Chip only), unless otherwise noted. All typical values at T_J = 25°C.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN}	Input Voltage	Legacy chip		2.7		5.5	V
		New chip		2.7		6.0	
V_{FB}	Internal reference (TPS79601)			1.2	1.225	1.25	V
I_{OUT}	Continuous output current			0		1	A
V_{OUT}	Output voltage range (TPS79601)			1.225		$5.5V_{DO}$	V
V_{OUT}	Output accuracy	TPS79601 (legacy chip)	0 µA ≤ I_{OUT} ≤ 1A, $V_{OUT(nom)}$ + 1V ≤ V_{IN} ≤ 5.5V (1)	$0.98V_{OUT(nom)}$		$1.02V_{OUT(nom)}$	%
		TPS79601 (new chip)	0 µA ≤ I_{OUT} ≤ 1A, $V_{OUT(nom)}$ + 1V ≤ V_{IN} ≤ 5.5V (1)	$0.975V_{OUT(nom)}$		$1.025V_{OUT(nom)}$	
V_{OUT}	Output accuracy	Fixed V_{OUT} < 5V	0 µA ≤ I_{OUT} ≤ 1A, $V_{OUT(nom)}$ + 1V ≤ V_{IN} ≤ 5.5V (1)	-2.0		2.0	%
V_{OUT}	Output accuracy	Fixed V_{OUT} = 5V	0 µA ≤ I_{OUT} ≤ 1A, $V_{OUT(nom)}$ + 1V ≤ V_{IN} ≤ 5.5V (1)	-3.0		3.0	%
$\Delta V_{OUT}/\Delta VIN$	Line regulation	V_{OUT} + 1V ≤ V_{IN} ≤ 5.5V			0.05	0.12	%/V
$\Delta V_{OUT}/\Delta I_{OUT}$	Load regulation	0 µA ≤ I_{OUT} ≤ 1A			5		mV
V_{DO}	Dropout voltage TPS79628	V_{IN}= V_{OUT} - 0.1V	I_{OUT} = 1A		270	365	mV
	Dropout voltage TPS79628DRB		I_{OUT} = 250mA		52	90	
	Dropout voltage TPS79630		I_{OUT} = 1A		250	345	
	Dropout voltage TPS79633		I_{OUT} = 1A		220	325	
	Dropout voltage TPS79650		I_{OUT} = 1A		220	300	
I_{CL}	Output current limit	V_{OUT} = 0 (legacy chip)		2.4		4.2	A
I_{CL}	Output current limit	$V_{IN} = V_{OUT(nom)}$ + 1.25V or 2.0V (whichever is greater), V_{OUT} = 0.9x $V_{OUT(nom)}$ (new chip only) (2)		1.04		1.65	A
I_{SC}	Short-circuit current limit	V_{OUT} = 0 (new chip only)			550		mA
I_{GND}	Ground current	0µA ≤ I_{OUT} ≤ 1A (legacy chip)			265	385	µA
I_{GND}	Ground current	0µA ≤ I_{OUT} ≤ 1A (new chip)			700	1100	µA
I_{SHDN}	Shutdown current	V_{EN} = 0V, 2.7 V ≤ V_{IN} ≤ 5.5V			0.07	1	µA
I_{FB}	Feedback pin current	V_{FB} = 1.225V				1	µA
PSRR	Power-supply rejection ratio	f = 100Hz, I_{OUT} = 10mA (legacy chip)			59		dB
		f = 100Hz, I_{OUT} = 10mA (new chip)			64		
		f = 100Hz, I_{OUT} = 1A (legacy chip)			54		
		f = 100Hz, I_{OUT} = 1A (new chip)			74		
		f = 10kHz, I_{OUT} = 1A (legacy chip)			53		
		f = 10kHz, I_{OUT} = 1A (new chip)			49		
		f = 100kHz, I_{OUT} = 1A (legacy chip)			42		
		f = 100kHz, I_{OUT} = 1A (new chip)			42		
V_n	Output noise voltage	BW = 100Hz to 100kHz, I_{OUT} = 1A	C_{NR} = 0.001 µF		54		μV_{RMS}
			C_{NR} = 0.0047 µF		46		
			C_{NR} = 0.01 µF		41		
			C_{NR} = 0.1 µF		40		
		BW = 10Hz to 100kHz, I_{OUT} = 1A	new chip (10		78		μV_{RMS}

5.5 Electrical Characteristics (continued)

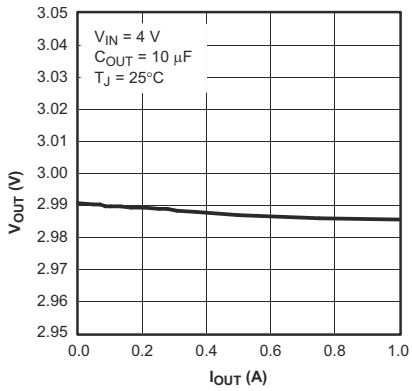
at operating temperature range (T_J = –40°C to +125°C), $V_{EN} = V_{IN}$, $V_{IN} = V_{OUT(nom)}$ + 1V (1), I_{OUT} = 1mA, and C_{OUT} = 10µF and C_{NR} = 0.01µF(Legacy Chip only), unless otherwise noted. All typical values at T_J = 25°C.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{str}	Time, start-up	R_L = 3Ω, C_{OUT} = 1 µF	C_{NR} = 0.001 µF		50		µs
		R_L = 3Ω, C_{OUT} = 1 µF	C_{NR} = 0.0047 µF		75		
		R_L = 3Ω, C_{OUT} = 1 µF	C_{NR} = 0.01 µF		110		
t_{str}	Time, start-up	R_L = 3Ω, C_{OUT} = 1 µF	new chip		550		µs
I_{EN}	Enable pin current	V_{EN} = 0V		-1		1	µA
$R_{PULLDOWN}$	Pulldown resistance	V_{IN} = 3.3V (new chip only)			100		Ω
V_{UVLO}	UVLO threshold	V_{IN} rising (legacy chip)		2.25		2.65	V
		V_{IN} rising (new chip)		1.28		1.62	
$V_{UVLO(HYST)}$	UVLO hysteresis	V_{IN} hysteresis (legacy chip)			100		mV
		V_{IN} hysteresis (new Chip)			130		
$V_{EN(HI)}$	High-level enable input voltage	2.7V(1) ≤ V_{IN} ≤ 5.5V (legacy chip)		1.7		V_{IN}	V
		2.7V(1) ≤ V_{IN} ≤ 5.5V (new chip)		0.85		V_{IN}	
$V_{EN(LOW)}$	Low-level enable input voltage	2.7V(1) ≤ V_{IN} ≤ 5.5V (legacy chip)				0.7	
		2.7V(1) ≤ V_{IN} ≤ 5.5V (new chip)				0.425	
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing	legacy chip		165		℃
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing	new chip		170		℃
T_{SD}	Thermal shutdown temperature	Reset, temperature decreasing	legacy chip		140		℃
T_{SD}	Thermal shutdown temperature	Reset, temperature decreasing	new chip		155		℃

(1) Minimum $V_{IN} = V_{OUT}$ +1V or 2.7V, whichever is greater. $V_{OUT(NOM)}$ =5V is tested at $V_{IN\ (NOM)}$ = 5.5V
(2) $V_{OUT(NOM)}$ =5V is tested at $V_{IN\ (NOM)} = V_{OUT(NOM)}$ +1V

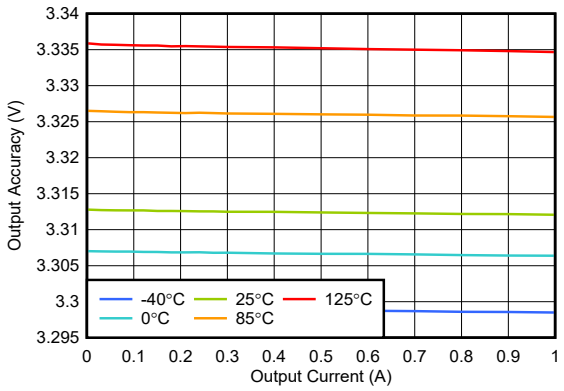
5.6 Typical Characteristics

at $V_{EN} = V_{IN}$, $V_{IN} = V_{OUT(nom)} + 1V$, $I_{OUT} = 1mA$, $C_{OUT} = 10\mu F$, $C_{NR} = 0.01\mu F$, $C_{IN} = 2.2\mu F$, and $T_J = 25°C$ (unless otherwise noted)



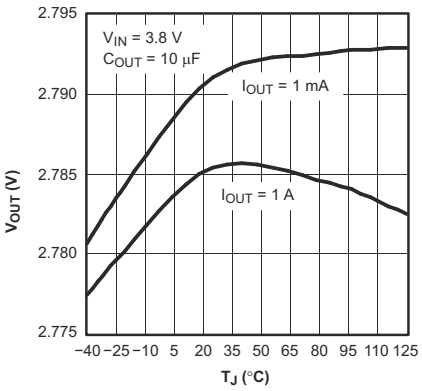
Legacy chip

Figure 5-1. TPS79630 Output Voltage vs Output Current



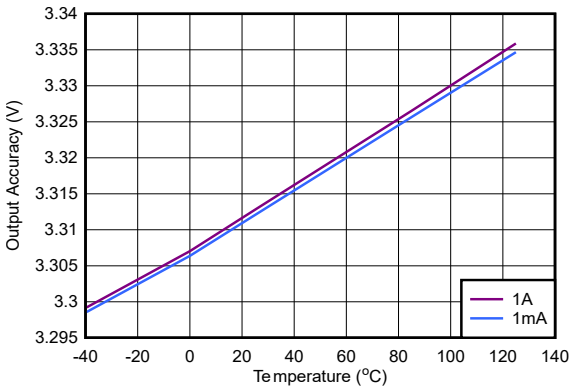
New chip

Figure 5-2. TPS79633 Output Voltage vs Output Current



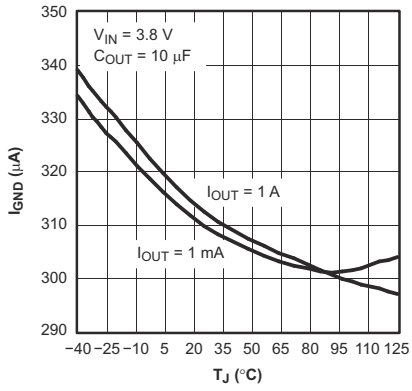
Legacy chip

Figure 5-3. TPS79628 Output Voltage vs Junction Temperature



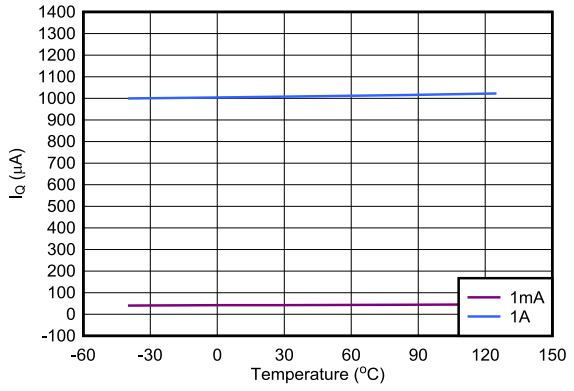
New chip

Figure 5-4. TPS79633 Output Voltage vs Junction Temperature



Legacy chip

Figure 5-5. TPS79628 Ground Current vs Junction Temperature

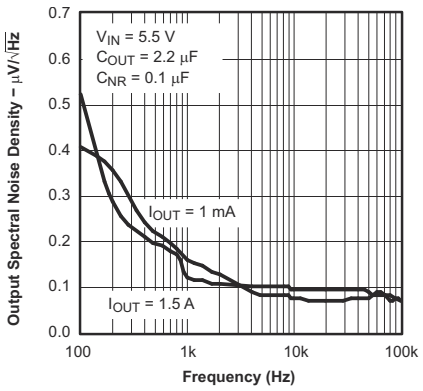


New chip

Figure 5-6. TPS79633 Ground Current vs Junction Temperature

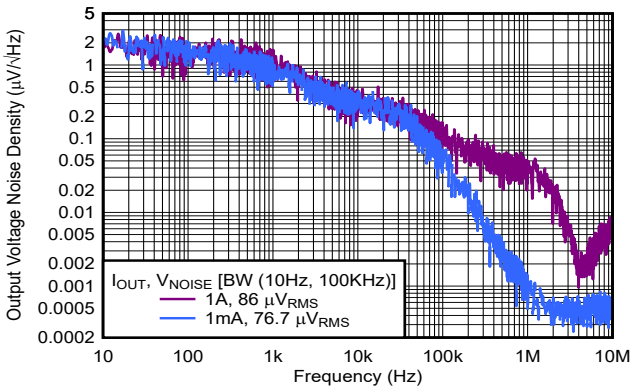
5.6 Typical Characteristics (continued)

at $V_{EN} = V_{IN}$, $V_{IN} = V_{OUT(nom)} + 1V$, $I_{OUT} = 1mA$, $C_{OUT} = 10\mu F$, $C_{NR} = 0.01\mu F$, $C_{IN} = 2.2\mu F$, and $T_J = 25°C$ (unless otherwise noted)



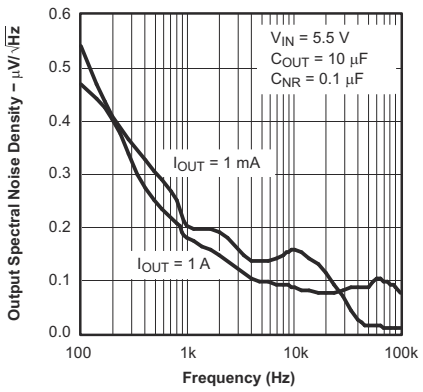
Legacy chip

Figure 5-7. TPS79630 Output Spectral Noise Density vs Frequency



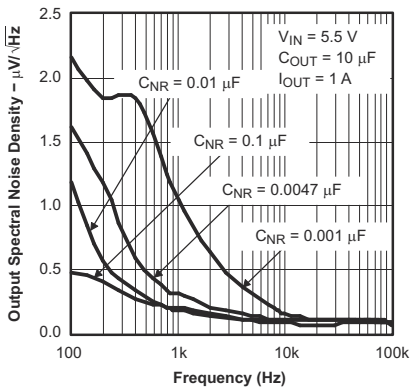
COUT = 2.2uF (new chip)

Figure 5-8. TPS79633 Output Spectral Noise Density vs Frequency



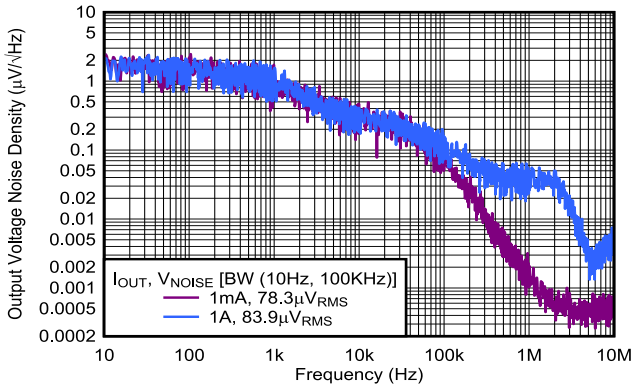
Legacy chip

Figure 5-9. TPS79630 Output Spectral Noise Density vs Frequency



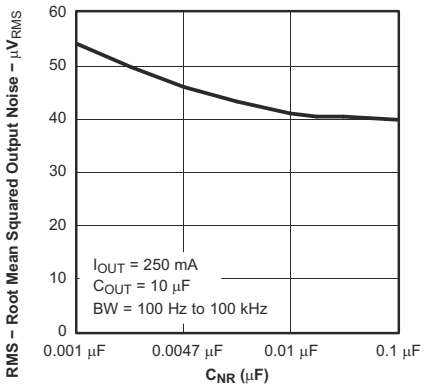
Legacy chip

Figure 5-10. TPS79630 Output Spectral Noise Density vs Frequency



COUT = 10uF (new chip)

Figure 5-11. TPS79633 Output Spectral Noise Density vs Frequency

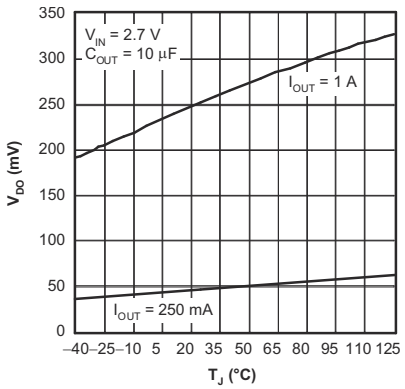


Legacy chip

Figure 5-12. TPS79630 Root Mean Squared Output Noise vs Bypass Capacitance

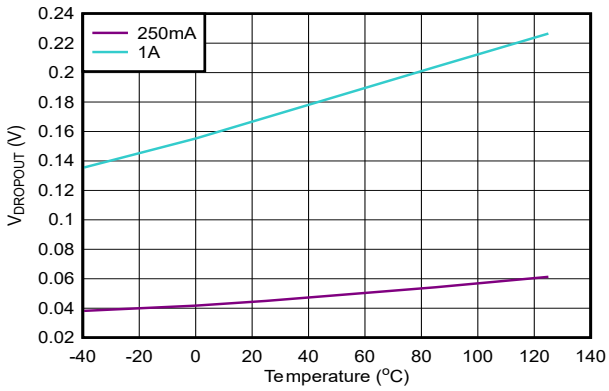
5.6 Typical Characteristics (continued)

at $V_{EN} = V_{IN}$, $V_{IN} = V_{OUT(nom)} + 1V$, $I_{OUT} = 1mA$, $C_{OUT} = 10\mu F$, $C_{NR} = 0.01\mu F$, $C_{IN} = 2.2\mu F$, and $T_J = 25°C$ (unless otherwise noted)



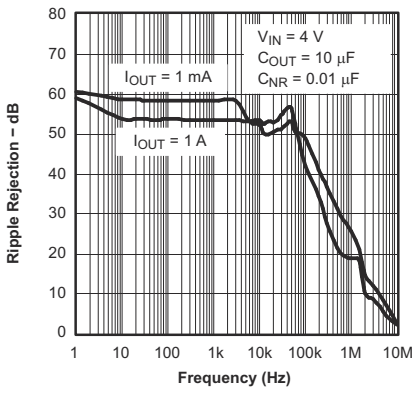
Legacy chip

Figure 5-13. TPS79628 Dropout Voltage vs Junction Temperature



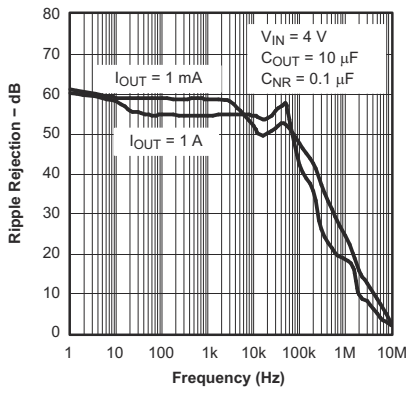
New chip

Figure 5-14. TPS79633 Dropout Voltage vs Junction Temperature



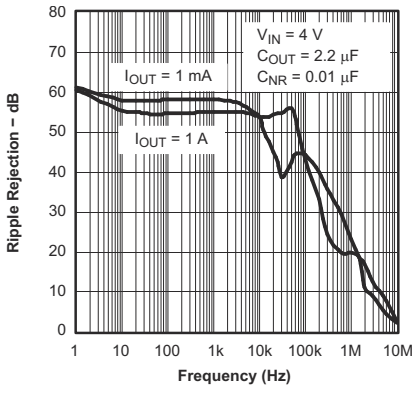
Legacy chip

Figure 5-15. TPS79630 Ripple Rejection vs Frequency



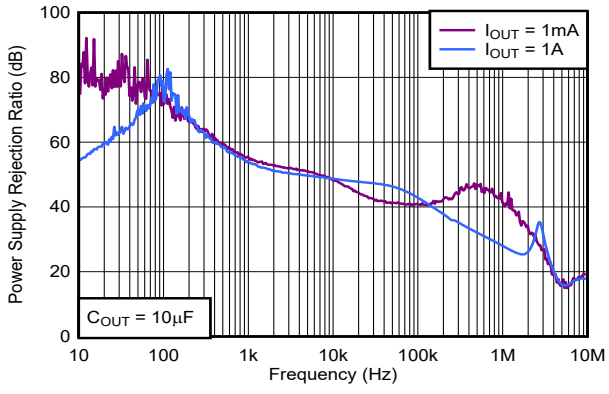
Legacy chip

Figure 5-16. TPS79630 Ripple Rejection vs Frequency



Legacy chip

Figure 5-17. TPS79630 Ripple Rejection vs Frequency

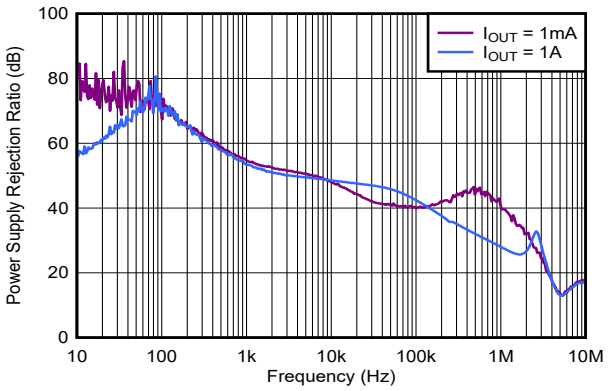


New chip

Figure 5-18. TPS79633 Ripple Rejection vs Frequency

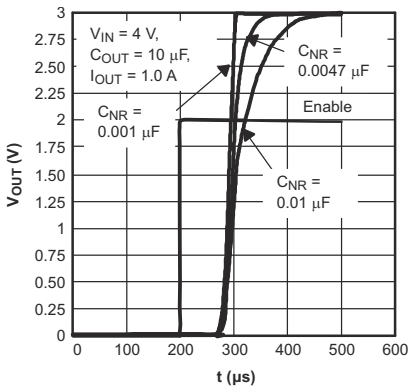
5.6 Typical Characteristics (continued)

at V_{EN} = V_{IN}, V_{IN} = $V_{OUT(nom)}$ + 1V, I_{OUT} = 1mA, C_{OUT} = 10µF, C_{NR} = 0.01µF, C_{IN} = 2.2µF, and T_J = 25°C (unless otherwise noted)



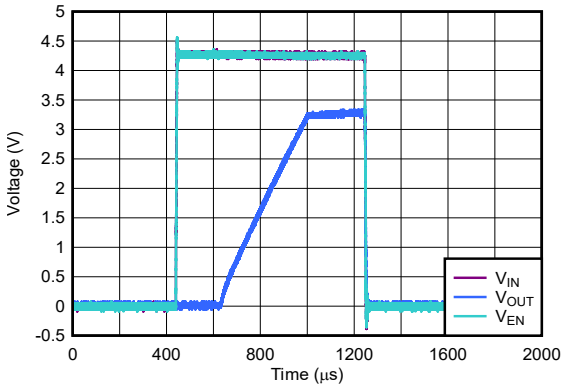
C_{OUT} = 1uF (new chip)

Figure 5-19. TPS79633 Ripple Rejection vs Frequency



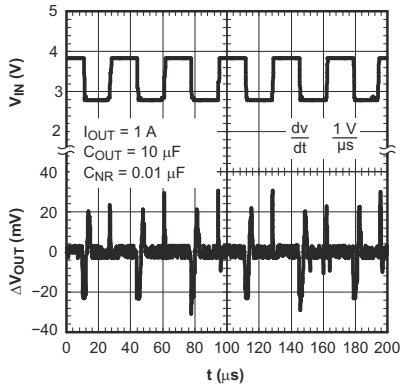
Legacy chip

Figure 5-20. Start-Up Time



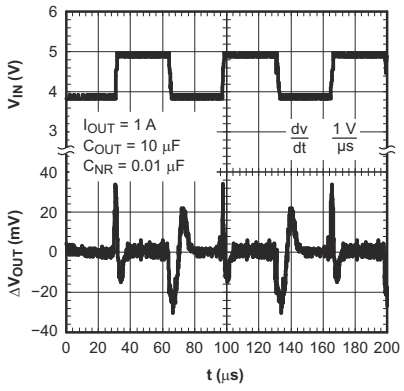
New chip

Figure 5-21. Start-Up Time



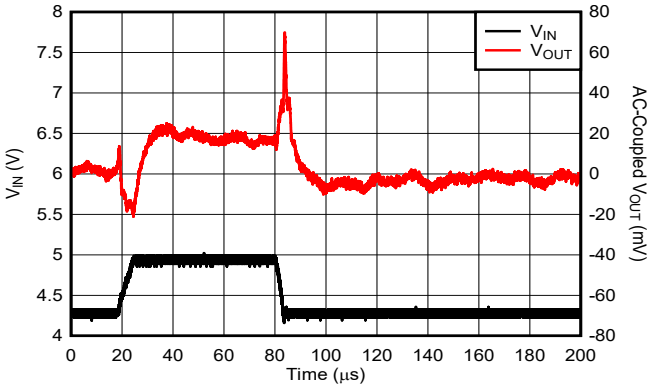
Legacy chip

Figure 5-22. TPS79618 Line Transient Response



Legacy chip

Figure 5-23. TPS79630 Line Transient Response

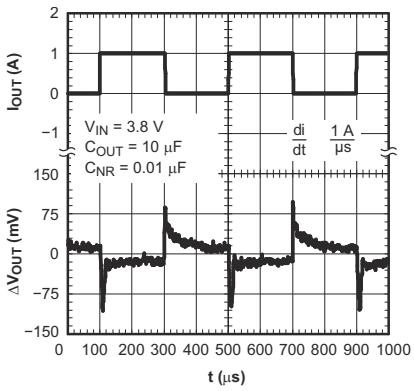


New chip

Figure 5-24. TPS79633 Line Transient Response

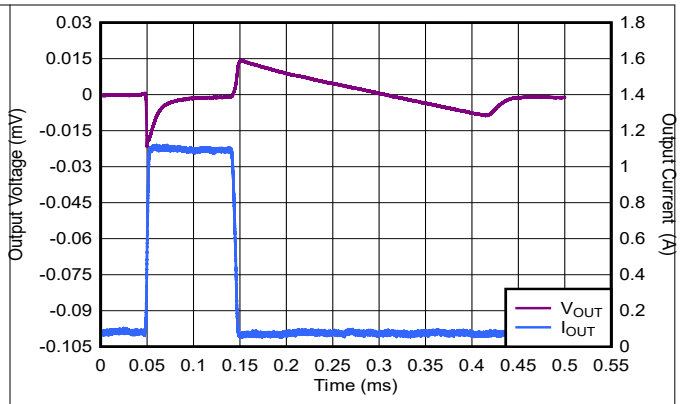
5.6 Typical Characteristics (continued)

at $V_{EN} = V_{IN}$, $V_{IN} = V_{OUT(nom)} + 1V$, $I_{OUT} = 1mA$, $C_{OUT} = 10\mu F$, $C_{NR} = 0.01\mu F$, $C_{IN} = 2.2\mu F$, and $T_J = 25°C$ (unless otherwise noted)



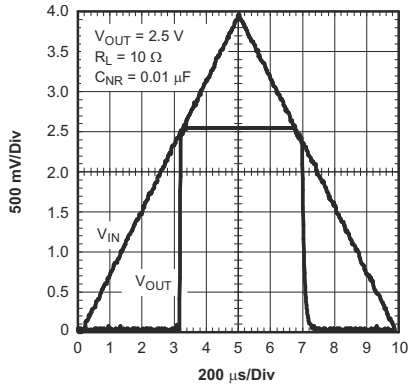
Legacy chip

Figure 5-25. TPS79628 Load Transient Response



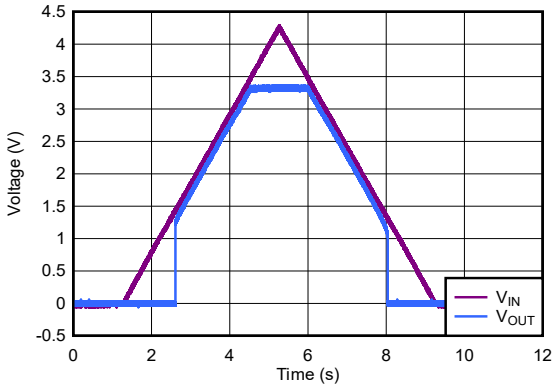
New chip

Figure 5-26. TPS79633 Load Transient Response



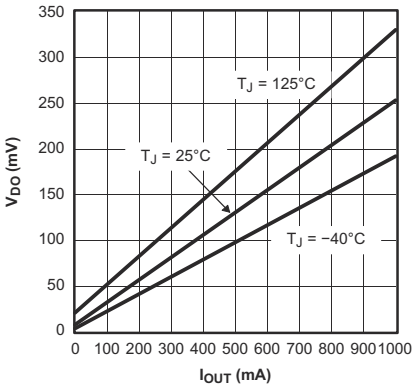
Legacy chip

Figure 5-27. TPS79625 Power-Up, Power-Down



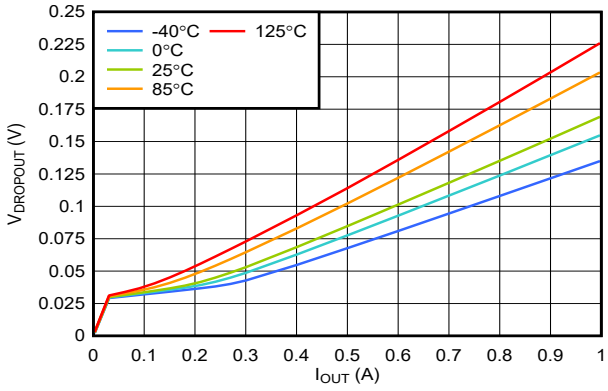
New chip

Figure 5-28. TPS79633 Power-Up, Power-Down



Legacy chip

Figure 5-29. TPS79630 Dropout Voltage vs Output Current



New chip

Figure 5-30. TPS79633 Dropout Voltage vs Output Current

5.6 Typical Characteristics (continued)

at $V_{EN} = V_{IN}$, $V_{IN} = V_{OUT(nom)} + 1V$, $I_{OUT} = 1mA$, $C_{OUT} = 10\mu F$, $C_{NR} = 0.01\mu F$, $C_{IN} = 2.2\mu F$, and $T_J = 25°C$ (unless otherwise noted)

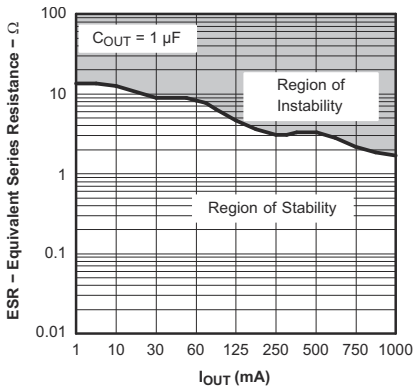


Figure 5-31. TPS79630 Typical Regions of Stability Equivalent Series Resistance (ESR) vs Output Current

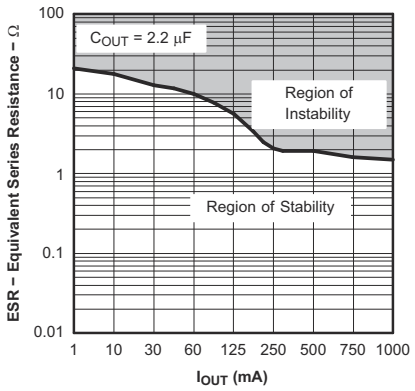


Figure 5-32. TPS79630 Typical Regions of Stability Equivalent Series Resistance (ESR) vs Output Current

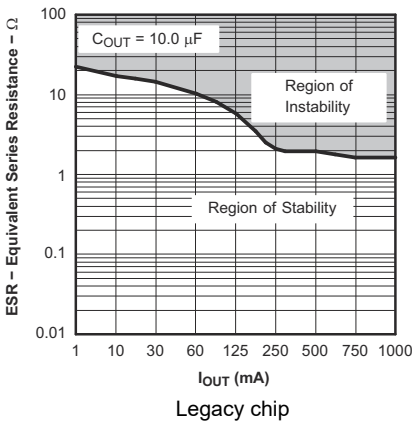


Figure 5-33. TPS79630 Typical Regions of Stability Equivalent Series Resistance (ESR) vs Output Current

6 Detailed Description

6.1 Overview

The TPS796 low-dropout (LDO) regulator combines the high performance required of many RF and precision analog applications with low current consumption. High PSRR is provided by a high-gain, high-bandwidth error loop with good supply rejection at very low headroom (V_{IN} – V_{OUT}). A noise-reduction pin is provided to bypass noise generated by the band-gap reference and to improve PSRR, while a quick-start circuit quickly charges this capacitor at start-up. This device features thermal and overcurrent protection, and is fully specified from –40°C to 125°C.

6.2 Functional Block Diagrams

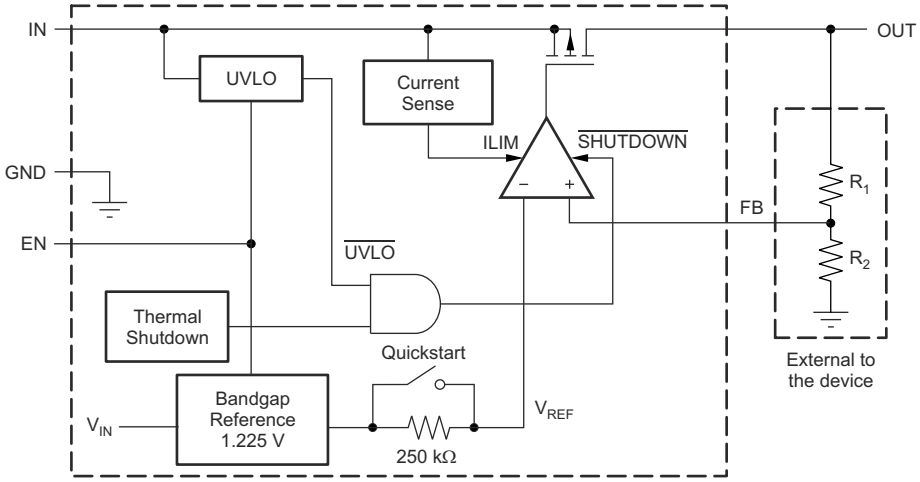


Figure 6-1. Functional Block Diagram: Adjustable Version (Legacy Chip)

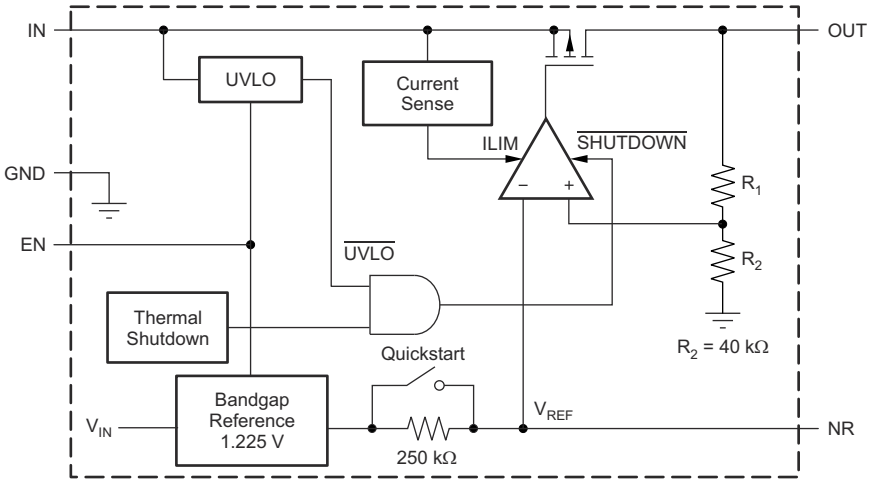


Figure 6-2. Functional Block Diagram: Fixed Version (Legacy Chip)

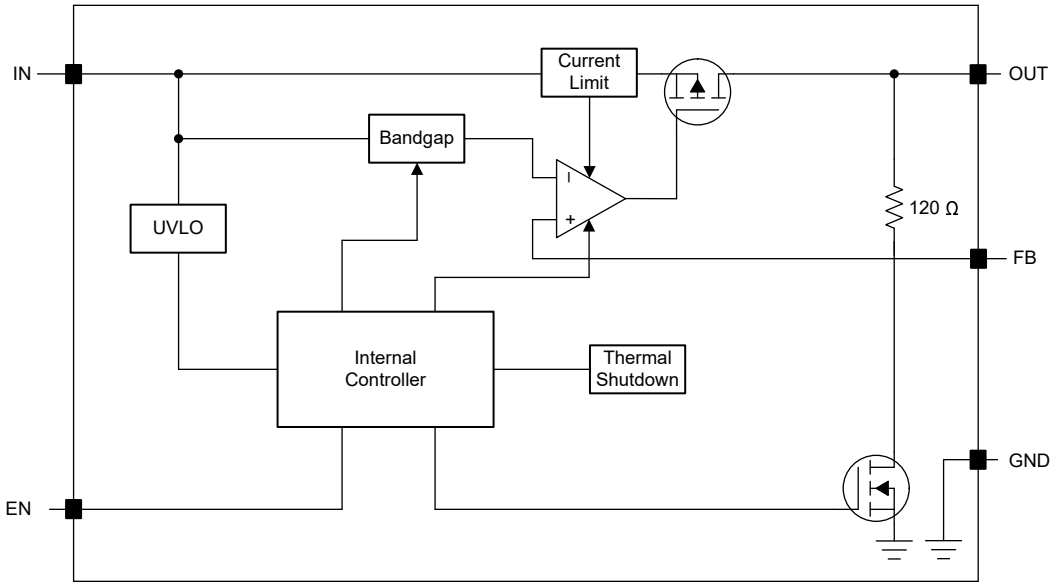


Figure 6-3. Functional Block Diagram: Adjustable Version (New Chip)

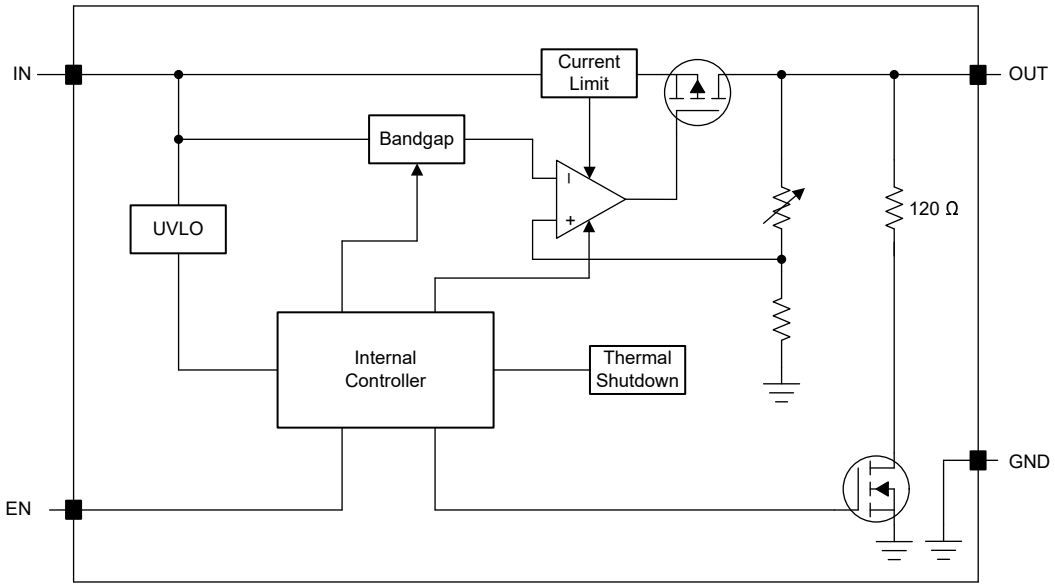


Figure 6-4. Functional Block Diagram: Fixed Version (New Chip)

6.3 Feature Description

6.3.1 Active Discharge (New Chip)

The device has an internal pulldown MOSFET that connects an $R_{PULLDOWN}$ resistor to ground when the device is disabled to actively discharge the output voltage. The active discharge circuit is activated by the enable pin.

Do not rely on the active discharge circuit to discharge the output voltage after the input supply has collapsed because reverse current can possibly flow from the output to the input. This reverse current flow can cause damage to the device, especially when a large output capacitor is used. Limit reverse current to no more than 5% of the device rated current for a short period of time.

6.3.2 Shutdown

The enable pin (EN) is active high. Enable the device by forcing the EN pin to exceed $V_{EN(high)}$. Turn off the device by forcing the EN pin to drop below the maximum EN pin low-level input voltage (see the *Electrical Characteristics* table). If shutdown capability is not required, connect EN to IN.

6.3.3 Start-Up

The TPS796 (legacy chip) uses a start-up circuit to quickly charge the noise reduction capacitor, C_{NR}, if present (see the *Functional Block Diagrams*). This circuit allows for the combination of very low output noise and fast start-up times. The NR pin is high impedance so a low leakage C_{NR} capacitor must be used; most ceramic capacitors are appropriate for this configuration.

For the fastest start-up, apply V_{IN} first, and then drive the enable pin (EN) high. If EN is tied to IN, start-up is somewhat slower. To make sure that C_{NR} is fully charged during start-up, use a 0.1µF or smaller capacitor.

The TPS796 (new chip) uses an internal soft-start time to reduce inrush current.

6.3.4 Undervoltage Lockout (UVLO)

The TPS796 uses an undervoltage lockout circuit to keep the output shut off until internal circuitry is operating properly. The UVLO circuit has hysteresis to help reject input voltage drops when the regulator first turns on (see the *Electrical Characteristics* table).

The UVLO circuit makes sure that the device stays disabled before the input supply reaches the minimum operational voltage range, and makes sure that the device shuts down when the input supply collapses. Figure 6-5 shows the UVLO circuit response to various input voltage events. The diagram can be separated into the following parts:

- Region A: The device does not start until the input reaches the UVLO rising threshold.
- Region B: Normal operation, regulating device.
- Region C: Brownout event above the UVLO falling threshold (UVLO rising threshold – UVLO hysteresis). The output can fall out of regulation but the device remains enabled.
- Region D: Normal operation, regulating device.
- Region E: Brownout event below the UVLO falling threshold. The device is disabled in most cases and the output falls because of the load and active discharge circuit. The device is re-enabled when the UVLO rising threshold is reached by the input voltage and a normal start-up follows.
- Region F: Normal operation followed by the input falling to the UVLO falling threshold.
- Region G: The device is disabled when the input voltage falls below the UVLO falling threshold to 0V. The output falls because of the load and active discharge circuit.

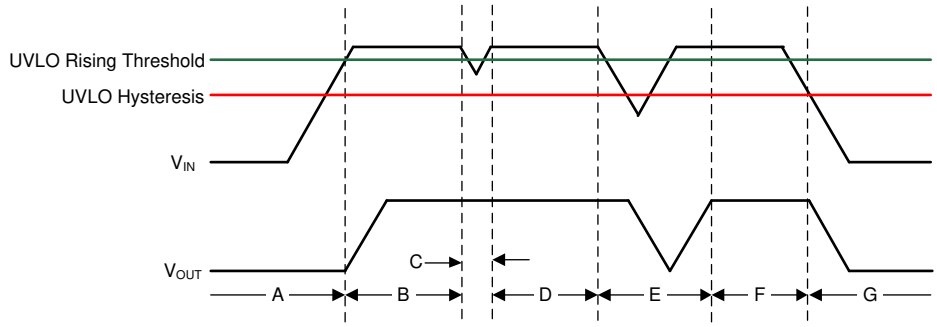


Figure 6-5. Typical UVLO Operation

6.3.5 Regulator Protection

The TPS796 (legacy chip) PMOS-pass transistor has a built-in back diode that conducts reverse current when the input voltage drops below the output voltage (for example, during power-down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage operation is anticipated, external limiting can be appropriate.

6.3.5.1 Current Limit

During normal operation, the TPS796 (legacy chip) limits output current to approximately 2.8A. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, take care not to exceed the power dissipation ratings of the package

For the new chip, the device has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a hybrid brick-wall-foldback scheme. The current limit transitions from a brick-wall scheme to a foldback scheme at the foldback voltage ($V_{FOLDBACK}$). In a high-load current fault with the output voltage above $V_{FOLDBACK}$, the brick-wall scheme limits the output current to the current limit (I_{CL}). When the voltage drops below $V_{FOLDBACK}$, a foldback current limit activates that scales back the current as the output voltage approaches GND. When the output is shorted, the device supplies a typical current called the short-circuit current limit (I_{SC}). I_{CL} and I_{SC} are listed in the *Electrical Characteristics* table.

For this device, $V_{FOLDBACK} = 0.4 \times V_{OUT(NOM)}$.

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in brick-wall current limit, the pass transistor dissipates power [$(V_{IN} – V_{OUT}) \times I_{CL}$]. When the device output is shorted and the output is below $V_{FOLDBACK}$, the pass transistor dissipates power [$(V_{IN} – V_{OUT}) \times I_{SC}$]. If thermal shutdown is triggered, the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition continues, the device cycles between current limit and thermal shutdown. For more information on current limits, see the *Know Your Limits* application note.

Figure 6-6 shows a diagram of the foldback current limit.

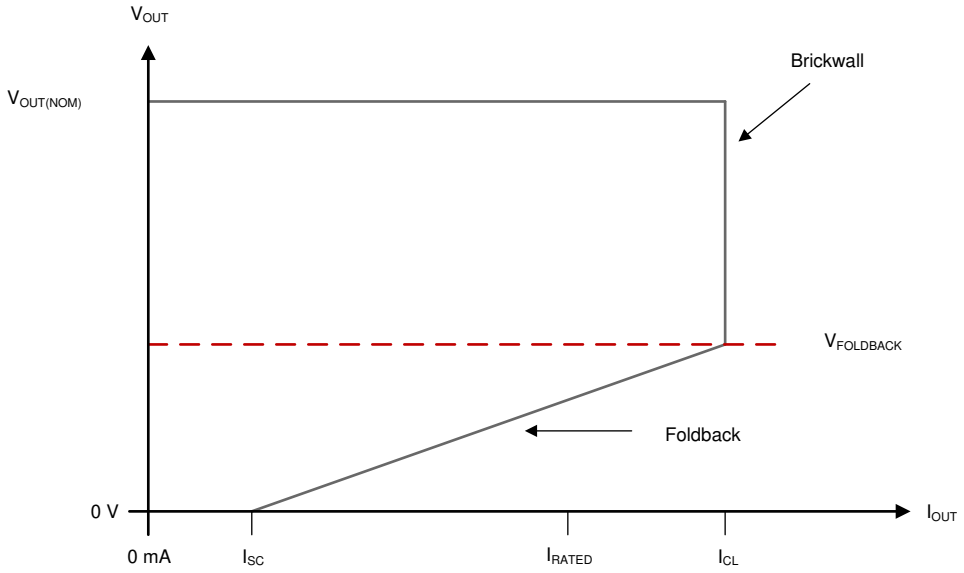


Figure 6-6. Foldback Current Limit

6.3.5.2 Thermal Shutdown

The device contains a thermal shutdown protection circuit to disable the device when the junction temperature (T_J) of the pass transistor rises to $T_{SD(shutdown)}$ (typical). Thermal shutdown hysteresis verifies that the device resets (turns on) when the temperature falls to $T_{SD(reset)}$ (typical).

The thermal time-constant of the semiconductor die is fairly short, thus the device can cycle on and off when thermal shutdown is reached until power dissipation is reduced. Power dissipation during startup can be high from large $V_{IN} – V_{OUT}$ voltage drops across the device or from high inrush currents charging large output capacitors. Under some conditions, the thermal shutdown protection disables the device before startup completes.

For reliable operation, limit the junction temperature to the maximum listed in the *Recommended Operating Conditions* table. Operation above this maximum temperature causes the device to exceed the operational specifications. Although the internal protection circuitry of the device is designed to protect against thermal overall conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown or above the maximum recommended junction temperature reduces long-term reliability.

6.4 Device Functional Modes

Table 6-1 provides a quick comparison between the normal, dropout, and disabled modes of operation.

Table 6-1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	EN	I_{OUT}	T_J
Normal	$V_{IN} > V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{CL}$	$T_J < T_{SD}$
Dropout	$V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{CL}$	$T_J < T_{SD}$
Disabled	$V_{IN} < V_{UVLO}$	$V_{EN} < V_{EN(LO)}$	—	$T_J > T_{SD}$

6.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$).
- The enable voltage has previously exceeded the enable rising threshold voltage and not yet decreased below the enable falling threshold.
- The output current is less than the current limit ($I_{OUT} < I_{CL}$).
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD}$).

6.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass device is in a triode state and no longer controls the current through the LDO. Line or load transients in dropout can result in large output-voltage deviations.

When the device is in a steady dropout state (defined as when the device is in dropout, $V_{IN} < V_{OUT(NOM)} + V_{DO}$, directly after being in a normal regulation state, but not during start-up), the pass transistor is driven into the ohmic or triode region. When the input voltage returns to a value greater than or equal to the nominal output voltage plus the dropout voltage ($V_{OUT(NOM)} + V_{DO}$), the output voltage can overshoot for a short period of time while the device pulls the pass transistor back into the linear region.

6.4.3 Disabled

The device is disabled under the following conditions:

- The enable voltage is less than the enable falling threshold voltage or has not yet exceeded the enable rising threshold.
- The device junction temperature is greater than the thermal shutdown temperature ($T_J > T_{SD}$).

The TPS796 (new chip), when disabled, the output voltage is actively discharged to ground by an internal discharge circuit from the output to ground.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The TPS796 low-dropout (LDO) regulator is optimized for use in noise-sensitive equipment. The device features extremely low dropout voltages, high PSRR, ultra-low output noise, low quiescent current, and enable input to reduce supply currents to less than 1µA when the regulator is turned off.

7.1.1 Recommended Capacitor Types

The device is designed to be stable using low equivalent series resistance (ESR) ceramic capacitors at the input and output. Multilayer ceramic capacitors have become the industry standard for these types of applications and are recommended, but must be used with good judgment. Ceramic capacitors that employ X7R-, X5R-, and C0G-rated dielectric materials provide relatively good capacitive stability across temperature, whereas the use of Y5V-rated capacitors is discouraged because of large variations in capacitance.

Regardless of the ceramic capacitor type selected, the effective capacitance varies with operating voltage and temperature. Generally, expect the effective capacitance to decrease by as much as 50%. The input and output capacitors recommended in the *Recommended Operating Conditions* table account for an effective capacitance of approximately 50% of the nominal value.

7.1.2 Input and Output Capacitor Requirements

A 2.2µF or larger ceramic input bypass capacitor, connected between IN and GND and located close to the TPS796, is required for stability and improves transient response, noise rejection, and ripple rejection. A higher-value input capacitor can be necessary if large, fast-rise-time load transients are anticipated and the device is located several inches from the power source.

Like most low dropout regulators, the TPS796 requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitor is 1µF. Any 1µF or larger ceramic capacitor is suitable.

7.1.3 Feed-forward Capacitor (C_{FF})

For the adjustable-voltage version device, a feed-forward capacitor (C_{FF}) can be connected from the OUT pin to the FB pin. C_{FF} improves transient, noise, and PSRR performance, but is not required for regulator stability. Recommended C_{FF} values are listed in the *Recommended Operating Conditions* table. A higher capacitance C_{FF} can be used; however, the start-up time increases. For a detailed description of C_{FF} tradeoffs, see the *Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator* application note.

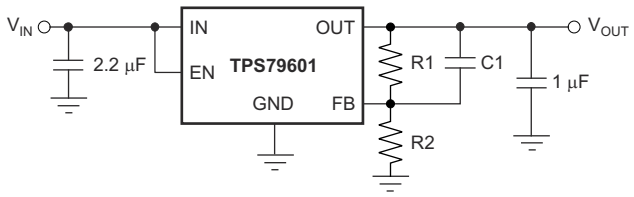
For the legacy chip, the C_{FF} can be estimated by Equation 1:

$$C1 = \frac{\left(3 \times 10^{-7}\right) \times (R1 + R2)}{(R1 \times R2)} \quad (1)$$

The suggested value of this capacitor for several resistor ratios is shown in the table in Figure 7-1. If this capacitor is not used (such as in a unity-gain configuration) then the minimum recommended output capacitor is 2.2µF instead of 1µF.

7.1.4 Adjustable Configuration

The output voltage of the TPS79601 adjustable regulator is programmed using an external resistor divider, as Figure 7-1 shows.



OUTPUT VOLTAGE PROGRAMMING GUIDE

OUTPUT VOLTAGE	R1	R2	C1
1.8 V	14.0 kΩ	30.1 kΩ	33 pF
3.6 V	57.9 kΩ	30.1 kΩ	15 pF

Figure 7-1. Typical Application, Adjustable Output

The output voltage is calculated using Equation 2:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right) \quad (2)$$

where:

- V_{REF} = 1.2246V typical (the internal reference voltage)

For the TPS796 (legacy chip), resistors R_1 and R_2 must be selected for approximately 40µA divider current. Lower value resistors can be used for improved noise performance, but the device wastes more power. Avoid higher values, as leakage current at FB increases the output voltage error.

The recommended design procedure is to choose R_2 = 30.1kΩ to set the divider current at 40µA, C_1 = 15pF for stability, and then calculate R_1 using Equation 3:

$$R1 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \times R2 \quad (3)$$

Similarly, for the TPS796 (new chip), to disregard the effect of the FB pin current error term and to achieve best accuracy, choose R_2 to be equal to or smaller than 550kΩ so that the current flowing through R_1 and R_2 is at least five times larger than the I_{FB} current listed in the *Electrical Characteristics* table. Lowering the value of R_2 increases the immunity against noise injection. Increasing the value of R_2 reduces the quiescent current for achieving higher efficiency at low load currents. Equation 4 calculates the setting that provides the maximum feedback divider series resistance.

$$(R_1 + R_2) \leq V_{OUT} / (I_{FB} \times 5) \quad (4)$$

7.1.5 Load Transient Response

The load-step transient response is the output voltage response by the LDO to a step in load current, whereby output voltage regulation is maintained. There are two key transitions during a load transient response: the transition from a light to a heavy load and the transition from a heavy to a light load. The regions shown in Figure 7-2 are broken down as follows. Regions A, E, and H are where the output voltage is in steady-state.

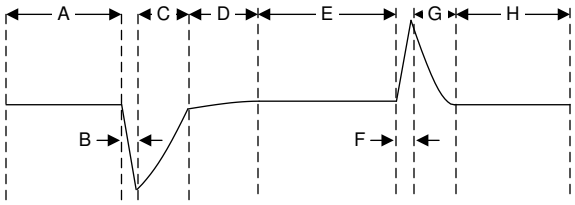


Figure 7-2. Load Transient Waveform

During transitions from a light load to a heavy load, the:

- Initial voltage dip is a result of the depletion of the output capacitor charge and parasitic impedance to the output capacitor (region B)
- Recovery from the dip results from the LDO increasing the sourcing current, and leads to output voltage regulation (region C)
- Initial voltage rise results from the LDO sourcing a large current, and leads to the output capacitor charge to increase (region F)
- Recovery from the rise results from the LDO decreasing the sourcing current in combination with the load discharging the output capacitor (region G)

A larger output capacitance reduces the peaks during a load transient but slows down the response time of the device. A larger DC load also reduces the peaks because the amplitude of the transition is lowered and a higher current discharge path is provided for the output capacitor.

7.1.6 Dropout Voltage

The TPS796 uses a PMOS-pass transistor to achieve a low dropout voltage. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the PMOS-pass transistor is in the linear region of operation and $r_{DS(on)}$ of the PMOS-pass transistor is the input-to-output resistance. Because the PMOS transistor behaves like a resistor in dropout, V_{DO} approximately scales with the output current.

7.1.6.1 Exiting Dropout

Some applications have transients that place the LDO into dropout, such as slower ramps on V_{IN} during start-up. As with other LDOs, the output can overshoot on recovery from these conditions. A ramping input supply causes an LDO to overshoot on start-up, as shown in Figure 7-3, when the slew rate and voltage levels are in the correct range. Use an enable signal to avoid this condition.

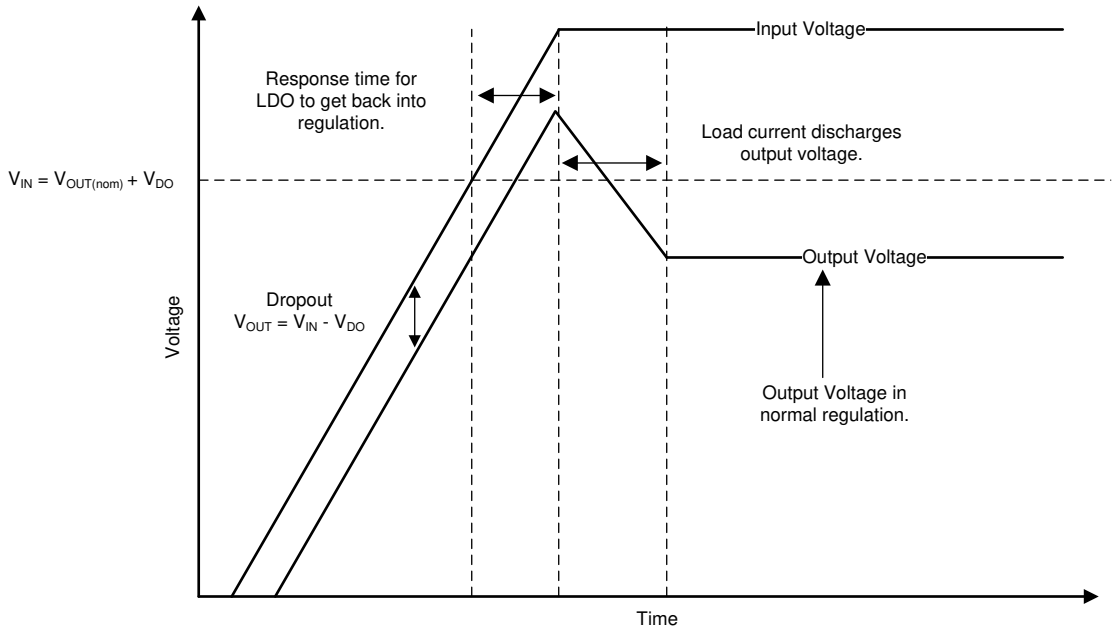


Figure 7-3. Start-Up Into Dropout

Line transients out of dropout can also cause overshoot on the output of the regulator. These overshoots are caused by the error amplifier having to drive the gate capacitance of the pass element and bring the gate back to the correct voltage for proper regulation. Figure 7-4 illustrates what is happening internally with the gate voltage and how overshoot can be caused during operation. When the LDO is placed in dropout, the gate voltage (V_{GS}) is pulled all the way down to ground to give the pass device the lowest on-resistance as possible. However, if a line transient occurs when the device is in dropout, the loop is not in regulation and can cause the output to overshoot until the loop responds and the output current pulls the output voltage back down into regulation. If these transients are not acceptable, then continue to add input capacitance in the system until the transient is slow enough to reduce the overshoot.

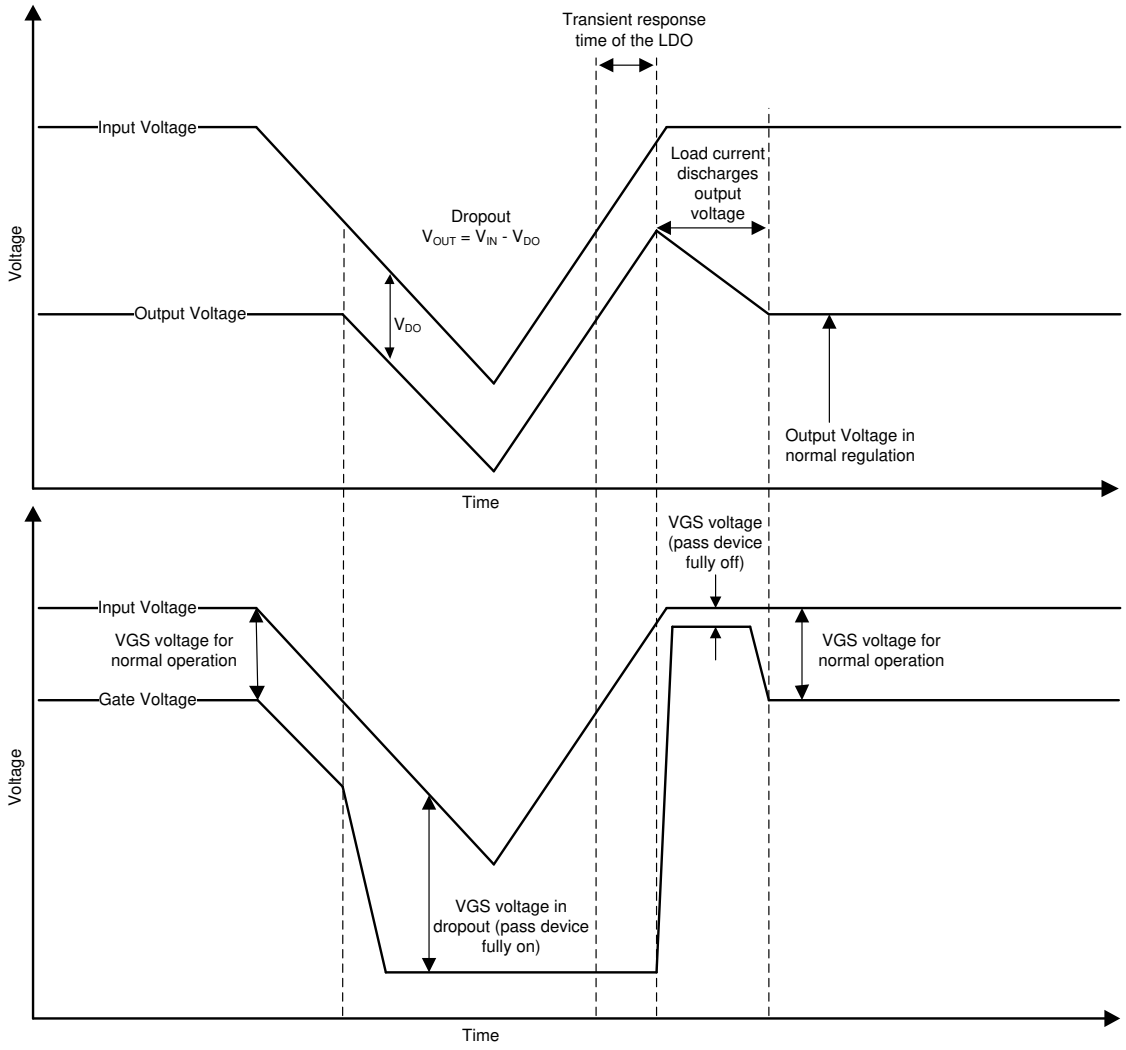


Figure 7-4. Line Transients From Dropout

7.1.7 Noise Reduction Pin (Legacy Chip)

The internal voltage reference is a key source of noise in an LDO regulator. The TPS796 (legacy chip) has a noise-reduction (NR) pin that is connected to the voltage reference through a 250kΩ internal resistor. The 250kΩ internal resistor, in conjunction with an external bypass capacitor connected to the NR pin, creates a low-pass filter to reduce the voltage reference noise and, therefore, the noise at the regulator output. For the regulator to operate properly, the current flow out of the NR pin must be at a minimum, because any leakage current creates an IR drop across the internal resistor, thus creating an output error. Therefore, the bypass capacitor must have minimal leakage current. The bypass capacitor must be no more than 0.1µF to make sure the capacitor is fully charged during the quick-start time provided by the internal switch shown in the functional block diagram of the legacy chip Figure 6-2. The output starts up slower as the bypass capacitance increases due to the RC time constant at the bypass pin that is created by the internal 250kΩ resistor and external capacitor.

7.1.8 Power Dissipation (P_D)

Knowing the device power dissipation and proper sizing of the thermal plane that is connected to the tab or pad is critical to avoiding thermal shutdown and providing reliable operation.

As a first-order approximation, power dissipation of the device depends on input voltage and load conditions. Use Equation 5 to approximate P_D:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (5)$$

Power dissipation can be minimized and greater efficiency can be achieved by using the lowest possible input voltage necessary to achieve the required output voltage regulation.

The main heat conduction path for the device is through the thermal pad on the package or the GND pad for the SOT-223 (DCQ) and TO-263 (KTT) packages. As such, the thermal pad and GND pad must be soldered to a copper pad area under the device. This pad area contains an array of plated vias that conduct heat to any inner plane areas or to a bottom-side copper plane. That tab must be connected to ground.

The maximum power dissipation determines the maximum allowable junction temperature (T_J) for the device. According to Equation 6, power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air (T_A). Equation 7 rearranges Equation 6 for output current.

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad (6)$$

$$I_{OUT} = (T_J - T_A) / [R_{\theta JA} \times (V_{IN} - V_{OUT})] \quad (7)$$

Unfortunately, this thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The $R_{\theta JA}$ recorded in the *Recommended Operating Conditions* table is determined by the JEDEC standard, PCB, and copper-spreading area, and is only used as a relative measure of package thermal performance.

7.2 Typical Application

A typical application circuit is shown in Figure 7-5.

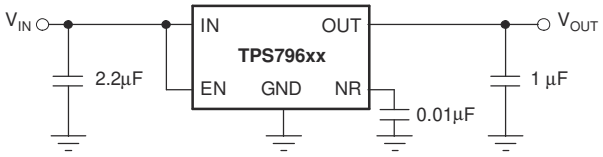


Figure 7-5. Typical Application Circuit

7.2.1 Design Requirements

Table 7-1 lists the design parameters.

Table 7-1. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Input voltage	4.3V
Output voltage	3.3V
Maximum output current	700mA
Output capacitor	10µF

7.2.2 Detailed Design Procedure

For this design example, a fixed 3.3V device is selected. The device is powered with a 4.3V rail, to maintain a 1V headroom between V_{IN} and V_{OUT} to make sure the device stays in regulation under all load and temperature conditions for the design. The load requires a minimum of 600mA up to 1A with a PSRR of 40dB at 100kHz.

7.2.3 Application Curves

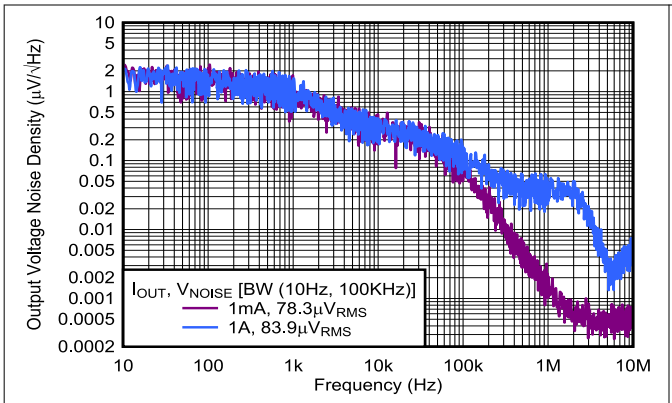


Figure 7-6. TPS796 Output Spectral Noise Density vs Frequency

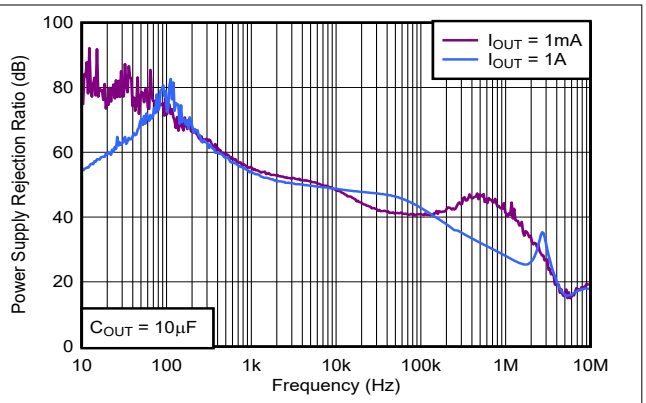


Figure 7-7. TPS796 PSRR vs Frequency

7.2.4 Best Design Practices

Place at least one 1µF ceramic capacitor as close as possible to the OUT pin of the regulator.

Do not place the output capacitor more than 10mm away from the regulator.

Connect a 2.2µF low equivalent series resistance (ESR) capacitor across the IN pin and GND input of the regulator.

Do not exceed the absolute maximum ratings.

7.3 Power Supply Recommendations

These devices are designed to operate from an input voltage supply range between 2.7V and 5.5V. The input voltage range provides adequate headroom for the device to have a regulated output. This input supply is well-regulated and stable. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

7.4 Layout

7.4.1 Layout Guidelines

7.4.1.1 Board Layout Recommendation to Improve PSRR and Noise Performance

To improve AC measurements like PSRR, output noise, and transient response, design the board with separate ground planes for V_{IN} and V_{OUT}, with each ground plane connected only at the ground pin of the device. In addition, the ground connection for the bypass capacitor must connect directly to the ground pin of the device.

7.4.1.2 Regulator Mounting

The tab of the SOT223-6 package is electrically connected to ground. For best thermal performance, the tab of the surface-mount version must be soldered directly to a circuit-board copper area. Increasing the copper area improves heat dissipation.

Solder pad footprint recommendations for the devices are presented in the *Solder Pad Recommendations for Surface-Mount Devices* application note, available from the TI web site (www.ti.com).

7.4.1.3 Estimating Junction Temperature

Using the thermal metrics Ψ_{JT} and Ψ_{JB}, as shown in the *Thermal Information* table, the junction temperature can be estimated with corresponding formulas (given in Equation 8). For backwards compatibility, an older $R_{\theta JC,Top}$ parameter is listed as well.

$$\Psi_{JT}: \quad T_J = T_T + \Psi_{JT} \bullet P_D$$
$$\Psi_{JB}: \quad T_J = T_B + \Psi_{JB} \bullet P_D \tag{8}$$

where:

- P_D is the power dissipation shown by Equation 8.
- T_T is the temperature at the center-top of the device package
- T_B is the PCB temperature measured 1mm away from the device package *on the PCB surface* (as Figure 7-9 shows).

Note

Both T_T and T_B can be measured on actual application boards using a thermo-gun (an infrared thermometer).

For more information about measuring T_T and T_B, see the *Using New Thermal Metrics* application note, available at www.ti.com.

By referring to Figure 7-8, the new thermal metrics (Ψ_{JT} and Ψ_{JB}) have very little dependency on board size. That is, using Ψ_{JT} or Ψ_{JB} with Equation 8 is a good way to estimate T_J by simply measuring T_T or T_B, regardless of the application board size.

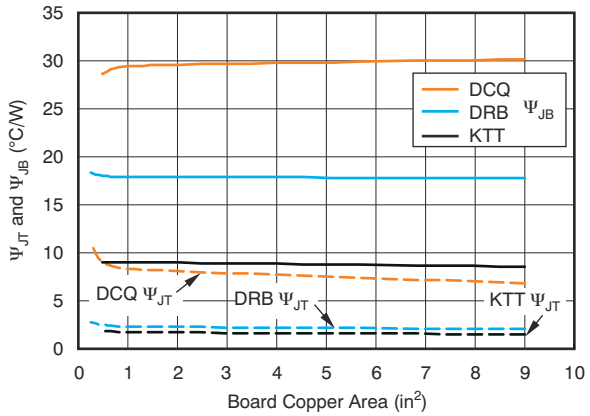
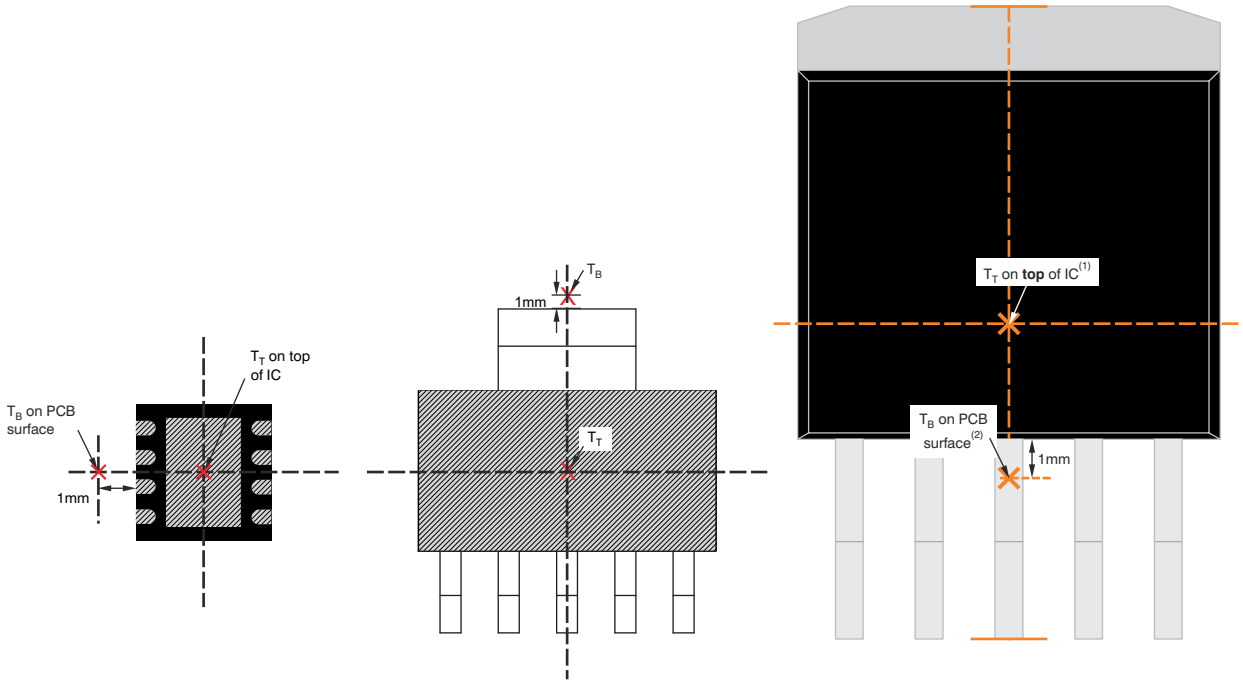


Figure 7-8. Ψ_{JT} And Ψ_{JB} vs Board Size

For a more detailed discussion of why TI does not recommend using $\theta_{JC(top)}$ to determine thermal characteristics, see the *Using New Thermal Metrics* application report, available for download at www.ti.com. For further information, see the *Semiconductor and IC Package Thermal Metrics* application note, also available on the TI website.



(a) Example DRB (VSON) Package Measurement (b) Example DCQ (SOT-223) Package Measurement (c) Example KTT (TO-263) Package Measurement

A. T_T is measured at the center of both the X- and Y-dimensional axes.
B. T_B is measured ***below*** the package lead on the PCB surface.

Figure 7-9. Measuring Points For T_T and T_B

7.4.2 Layout Examples

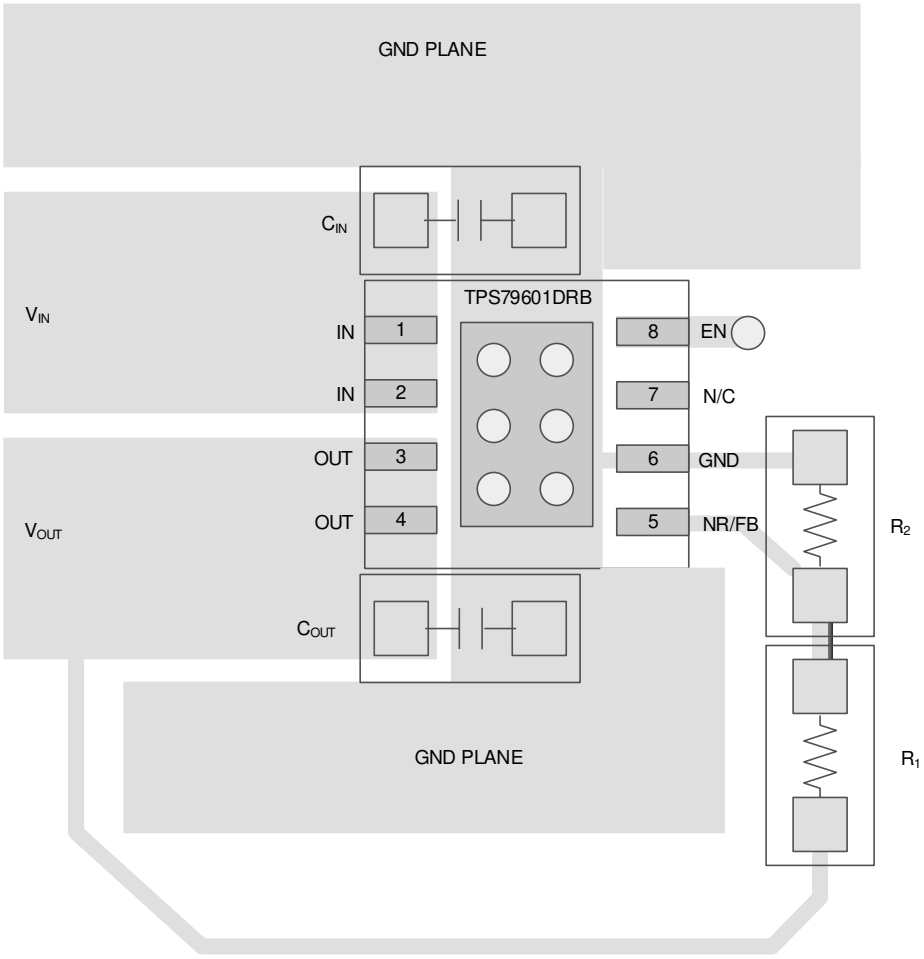


Figure 7-10. TPS79601 (Adjustable-Voltage Version): DRB Layout Example

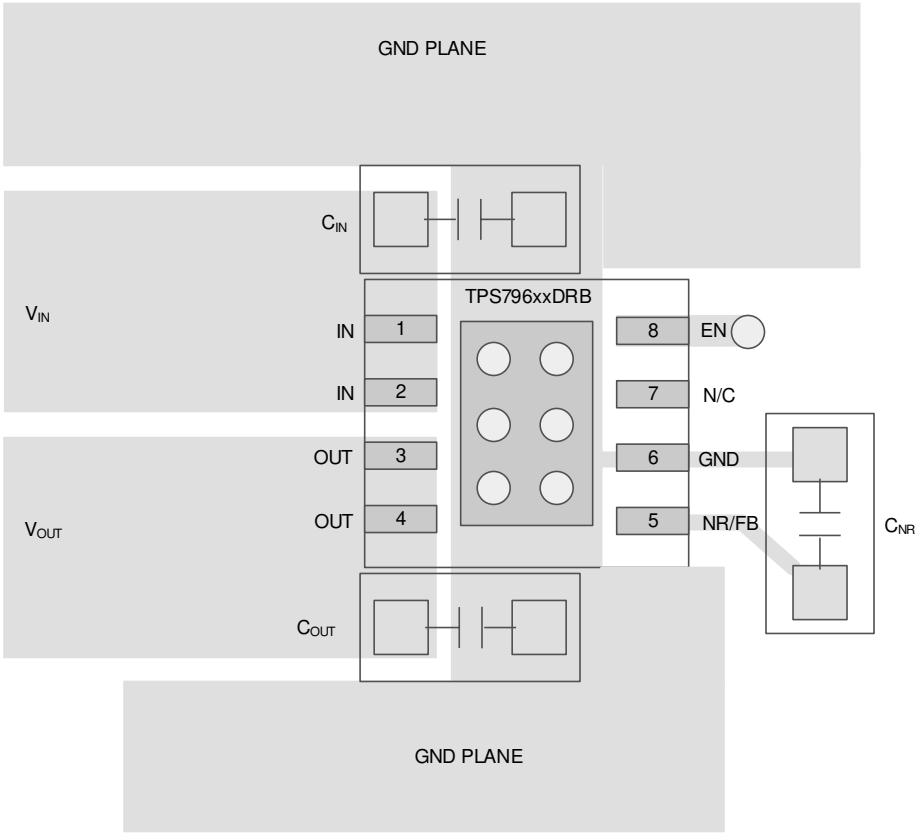


Figure 7-11. TPS796xx (Fixed-Voltage Versions): DRB Layout Example

8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

8.1.1.1 Evaluation Modules

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TPS796. The TPS79601DRBEVM evaluation module can be requested at the TI website through the product folders or purchased directly from the TI eStore.

8.1.1.2 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TPS796 is available through the product folders under simulation models.

8.1.2 Device Nomenclature

Table 8-1. Available Options

PRODUCT(1)	DESCRIPTION
TPS796**xx(x)***yyy z M3*	**xx(x)** is the nominal output voltage (for example, 28 = 2.8V, 285 = 2.85V, 01 = Adjustable). **yyy** is the package designator. **z** is the package quantity. ***M3*** is a suffix designator for devices that only use the latest manufacturing flow (CSO: RFB). Devices without this suffix ship with the legacy chip (CSO: DLN) or the new chip (CSO: RFB). The reel packaging label provides CSO information to distinguish which chip is being used. The device performance for new and legacy chips is denoted throughout the document.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Using New Thermal Metrics* application note
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics* application note
- Texas Instruments, *TPS799xxEVM-105* user's guide
- Texas Instruments, *Solder Pad Recommendations for Surface-Mount Devices* application note

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision Q (June 2025) to Revision R (January 2026)	Page
• added DRB thermal information for "new chip"	5

Changes from Revision P (January 2015) to Revision Q (June 2025)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Changed device name to condensed *TPS796* to consolidate all voltage option devices under one device name	1
• Changed entire document to align with current family format	1
• Added new silicon (M3) devices to document	1
• Added nomenclature distinguishing between new chip and legacy chip information throughout document	1
• Changed *Features*, *Applications*, and *Description* sections	1
• Changed *Pin Configuration and Functions* section	3
• Added new silicon curves to *Typical Characteristics* section	8
• Added new chip block diagrams to *Functional Block Diagrams* section	14
• Added *Active Discharge (New Chip)* section	16
• Changed *Shutdown* section	16
• Changed *Undervoltage Lockout (UVLO)* section	16
• Changed *Regulator Protection* section and added subsections	17
• Added steady dropout state discussion in second paragraph to *Dropout Operation* section	19
• Added subsections to *Application Information*	20
• Changed *Design Parameters* table	25
• Changed *Detailed Design Procedure* section	25
• Changed *Application Curves* section	26
• Changed title from *Do's and Don'ts* to *Best Design Practices*	26
• Added *Estimating Junction Temperature* section	26
• Added M3 information to *Available Options* table	31

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS79601DCQ	Active	Production	SOT-223 (DCQ) | 6	78 | TUBE	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	PS79601
TPS79601DCQ.A	Active	Production	SOT-223 (DCQ) | 6	78 | TUBE	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	PS79601
TPS79601DCQG4	Obsolete	Production	SOT-223 (DCQ) | 6	-	-	Call TI	Call TI	-40 to 125	PS79601
TPS79601DCQR	Active	Production	SOT-223 (DCQ) | 6	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	PS79601
TPS79601DCQR.A	Active	Production	SOT-223 (DCQ) | 6	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	PS79601
TPS79601DCQRM3	Active	Production	SOT-223 (DCQ) | 6	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS79601
TPS79601DRBR	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CES
TPS79601DRBR.A	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CES
TPS79601DRBRG4	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CES
TPS79601DRBRM3	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CES
TPS79601DRBT	Active	Production	SON (DRB) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CES
TPS79601DRBT.A	Active	Production	SON (DRB) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CES
TPS79601DRBTG4	Active	Production	SON (DRB) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CES
TPS79601KTTR	NRND	Production	DDPAK/ TO-263 (KTT) | 5	500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	TPS 79601
TPS79601KTTR.A	NRND	Production	DDPAK/ TO-263 (KTT) | 5	500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	TPS 79601
TPS79601KTTRG3	NRND	Production	DDPAK/ TO-263 (KTT) | 5	500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	TPS 79601
TPS79613DRBR	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CCT
TPS79613DRBR.A	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CCT
TPS79618DCQ	Obsolete	Production	SOT-223 (DCQ) | 6	-	-	Call TI	Call TI	-40 to 125	PS79618
TPS79618DCQR	Active	Production	SOT-223 (DCQ) | 6	2500 | LARGE T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	PS79618
TPS79618DCQR.A	Active	Production	SOT-223 (DCQ) | 6	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	PS79618
TPS79618DCQRM3	Active	Production	SOT-223 (DCQ) | 6	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS79618
TPS79618KTTR	Active	Production	DDPAK/ TO-263 (KTT) | 5	500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-	TPS 79618
TPS79618KTTR.A	Active	Production	DDPAK/ TO-263 (KTT) | 5	500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	TPS 79618
TPS79625DCQ	Obsolete	Production	SOT-223 (DCQ) | 6	-	-	Call TI	Call TI	-40 to 125	PS79625

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS79625DCQR	Active	Production	SOT-223 (DCQ) | 6	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	PS79625
TPS79625DCQR.A	Active	Production	SOT-223 (DCQ) | 6	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	PS79625
TPS79625DCQRM3	Active	Production	SOT-223 (DCQ) | 6	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS79625
TPS79625KTTR	Active	Production	DDPAK/ TO-263 (KTT) | 5	500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-	TPS 79625
TPS79625KTTR.A	Active	Production	DDPAK/ TO-263 (KTT) | 5	500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	TPS 79625
TPS79628DCQ	Obsolete	Production	SOT-223 (DCQ) | 6	-	-	Call TI	Call TI	-40 to 125	PS79628
TPS79628DCQR	Active	Production	SOT-223 (DCQ) | 6	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS79628
TPS79628DCQR.A	Active	Production	SOT-223 (DCQ) | 6	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS79628
TPS79630DCQ	Obsolete	Production	SOT-223 (DCQ) | 6	-	-	Call TI	Call TI	-40 to 125	PS79630
TPS79630DCQR	Active	Production	SOT-223 (DCQ) | 6	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS79630
TPS79630DCQR.A	Active	Production	SOT-223 (DCQ) | 6	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS79630
TPS79630KTTR	Active	Production	DDPAK/ TO-263 (KTT) | 5	500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-	TPS 79630
TPS79630KTTR.A	Active	Production	DDPAK/ TO-263 (KTT) | 5	500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	TPS 79630
TPS79633DCQR	Active	Production	SOT-223 (DCQ) | 6	2500 | LARGE T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	PS79633
TPS79633DCQR.A	Active	Production	SOT-223 (DCQ) | 6	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	PS79633
TPS79633DCQRG4	Obsolete	Production	SOT-223 (DCQ) | 6	-	-	Call TI	Call TI	-40 to 125	PS79633
TPS79633DCQRM3	Active	Production	SOT-223 (DCQ) | 6	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS79633
TPS79633KTTR	NRND	Production	DDPAK/ TO-263 (KTT) | 5	500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-	TPS 79633
TPS79633KTTR.A	NRND	Production	DDPAK/ TO-263 (KTT) | 5	500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	TPS 79633
TPS79633KTTRG3	NRND	Production	DDPAK/ TO-263 (KTT) | 5	500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	TPS 79633
TPS79650DCQ	Obsolete	Production	SOT-223 (DCQ) | 6	-	-	Call TI	Call TI	-40 to 125	PS79650
TPS79650DCQR	Active	Production	SOT-223 (DCQ) | 6	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS79650
TPS79650DCQR.A	Active	Production	SOT-223 (DCQ) | 6	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS79650
TPS79650DRBR	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BYZ
TPS79650DRBR.A	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BYZ

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS79650DRBT	Active	Production	SON (DRB) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BYZ
TPS79650DRBT.A	Active	Production	SON (DRB) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BYZ
TPS79650DRBTG4	Active	Production	SON (DRB) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BYZ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

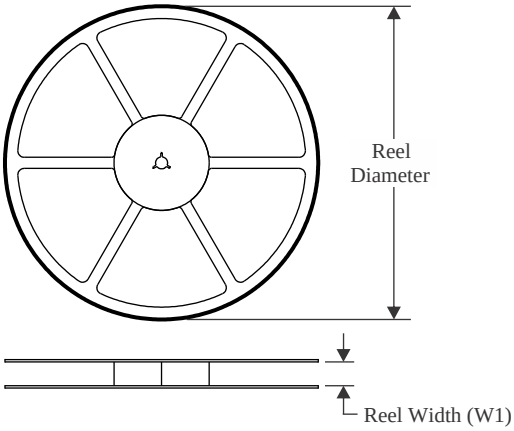
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

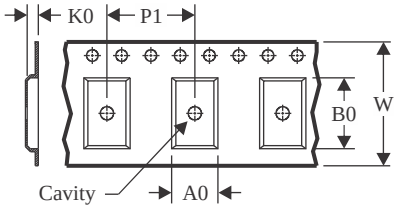
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

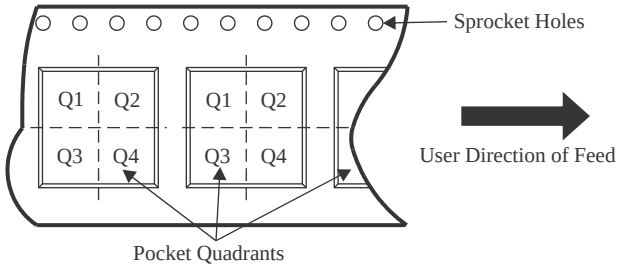


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

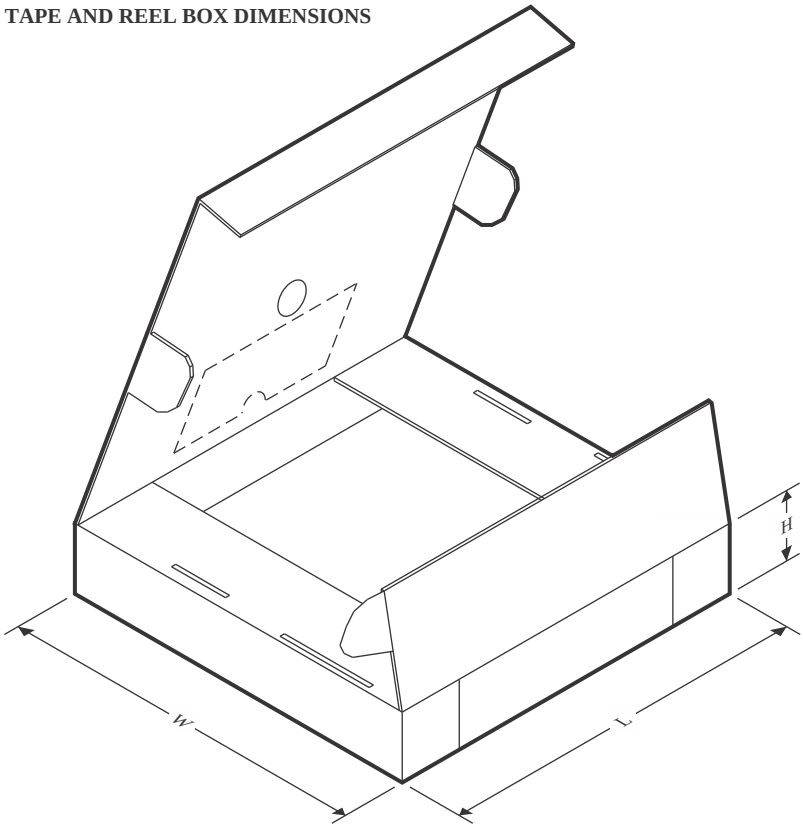


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS79601DCQR	SOT-223	DCQ	6	2500	330.0	12.4	6.85	7.3	1.88	8.0	12.0	Q3
TPS79601DCQRM3	SOT-223	DCQ	6	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TPS79601DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS79601DRBRM3	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS79601DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS79601KTTR	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.9	16.1	4.9	16.0	24.0	Q2
TPS79613DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS79618DCQR	SOT-223	DCQ	6	2500	330.0	12.4	6.85	7.3	1.88	8.0	12.0	Q3
TPS79618DCQRM3	SOT-223	DCQ	6	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TPS79618KTTR	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.9	16.1	4.9	16.0	24.0	Q2
TPS79625DCQR	SOT-223	DCQ	6	2500	330.0	12.4	6.85	7.3	1.88	8.0	12.0	Q3
TPS79625DCQRM3	SOT-223	DCQ	6	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TPS79625KTTR	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.9	16.1	4.9	16.0	24.0	Q2
TPS79628DCQR	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS79630DCQR	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TPS79630KTTR	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.9	16.1	4.9	16.0	24.0	Q2
TPS79633DCQR	SOT-223	DCQ	6	2500	330.0	12.4	6.85	7.3	1.88	8.0	12.0	Q3
TPS79633DCQRM3	SOT-223	DCQ	6	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TPS79633KTTR	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.9	16.1	4.9	16.0	24.0	Q2
TPS79650DCQR	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TPS79650DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS79650DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

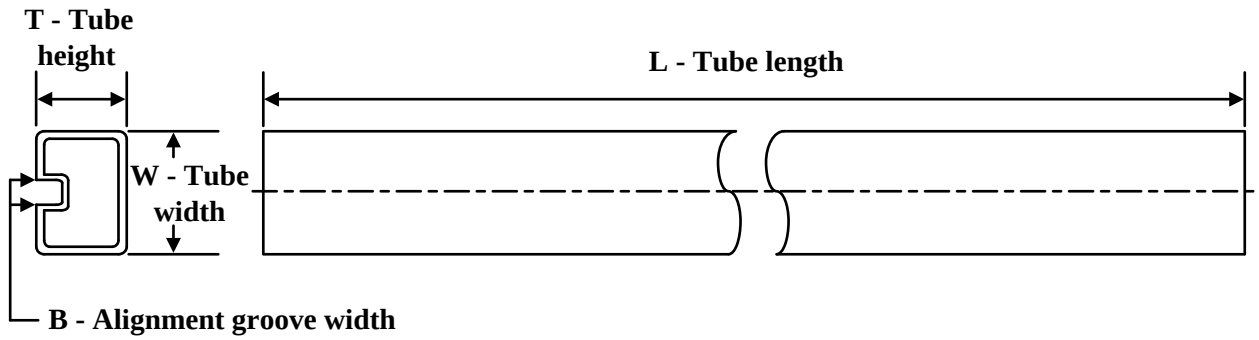


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS79601DCQR	SOT-223	DCQ	6	2500	356.0	356.0	36.0
TPS79601DCQRM3	SOT-223	DCQ	6	2500	366.0	364.0	50.0
TPS79601DRBR	SON	DRB	8	3000	353.0	353.0	32.0
TPS79601DRBRM3	SON	DRB	8	3000	367.0	367.0	35.0
TPS79601DRBT	SON	DRB	8	250	213.0	191.0	35.0
TPS79601KTTR	DDPAK/TO-263	KTT	5	500	356.0	356.0	45.0
TPS79613DRBR	SON	DRB	8	3000	353.0	353.0	32.0
TPS79618DCQR	SOT-223	DCQ	6	2500	356.0	356.0	36.0
TPS79618DCQRM3	SOT-223	DCQ	6	2500	340.0	340.0	38.0
TPS79618KTTR	DDPAK/TO-263	KTT	5	500	356.0	356.0	45.0
TPS79625DCQR	SOT-223	DCQ	6	2500	356.0	356.0	36.0
TPS79625DCQRM3	SOT-223	DCQ	6	2500	340.0	340.0	38.0
TPS79625KTTR	DDPAK/TO-263	KTT	5	500	356.0	356.0	45.0
TPS79628DCQR	SOT-223	DCQ	6	2500	346.0	346.0	29.0
TPS79630DCQR	SOT-223	DCQ	6	2500	346.0	346.0	29.0
TPS79630KTTR	DDPAK/TO-263	KTT	5	500	356.0	356.0	45.0
TPS79633DCQR	SOT-223	DCQ	6	2500	356.0	356.0	36.0
TPS79633DCQRM3	SOT-223	DCQ	6	2500	340.0	340.0	38.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS79633KTTR	DDPAK/TO-263	KTT	5	500	356.0	356.0	45.0
TPS79650DCQR	SOT-223	DCQ	6	2500	346.0	346.0	29.0
TPS79650DRBR	SON	DRB	8	3000	353.0	353.0	32.0
TPS79650DRBT	SON	DRB	8	250	213.0	191.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS79601DCQ	DCQ	SOT-223	6	78	543	8.6	3606.8	2.67
TPS79601DCQ.A	DCQ	SOT-223	6	78	543	8.6	3606.8	2.67

GENERIC PACKAGE VIEW

DRB 8

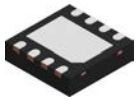
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4203482/L

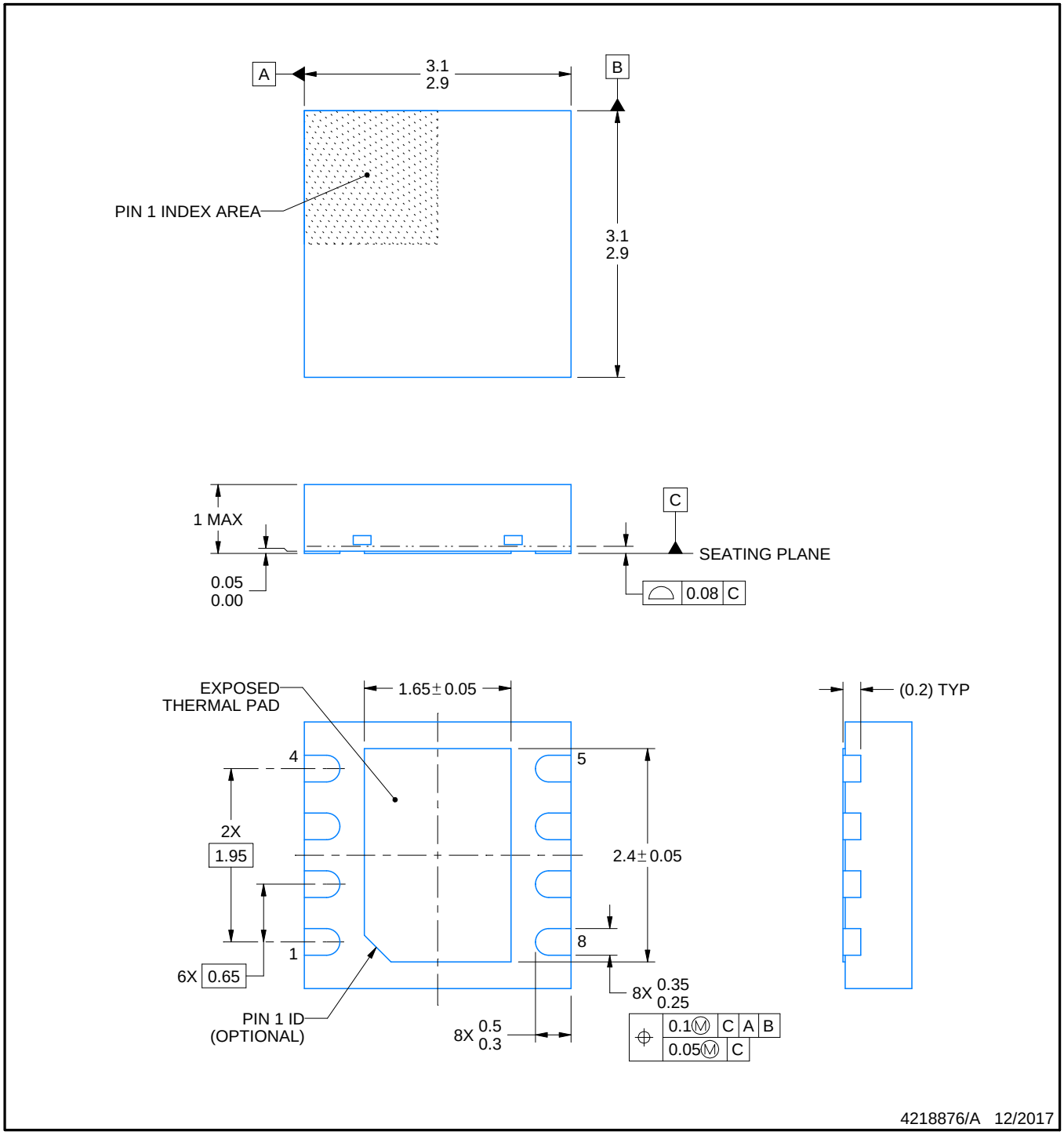
DRB0008B



PACKAGE OUTLINE

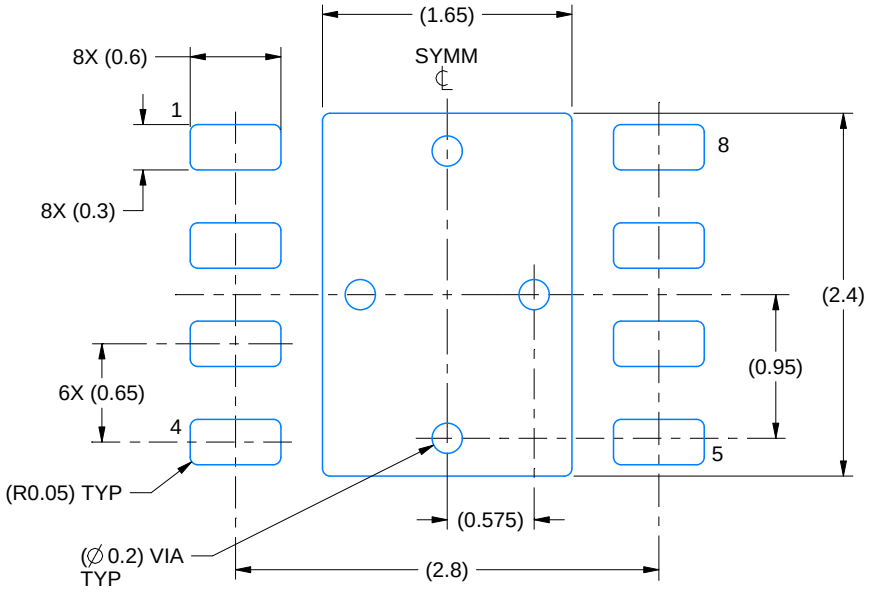
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

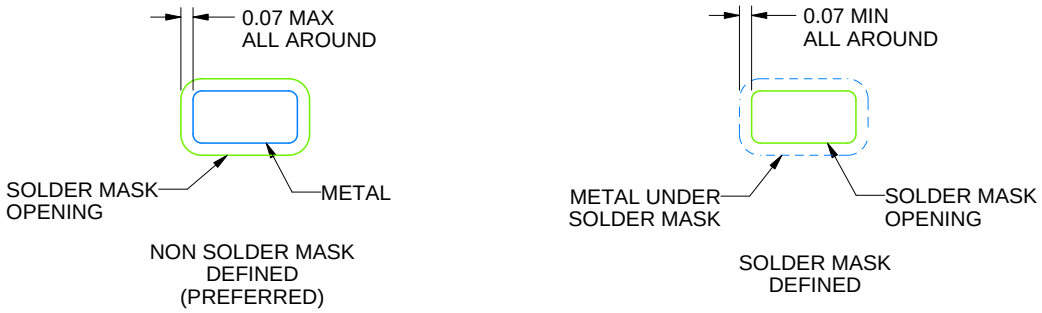


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

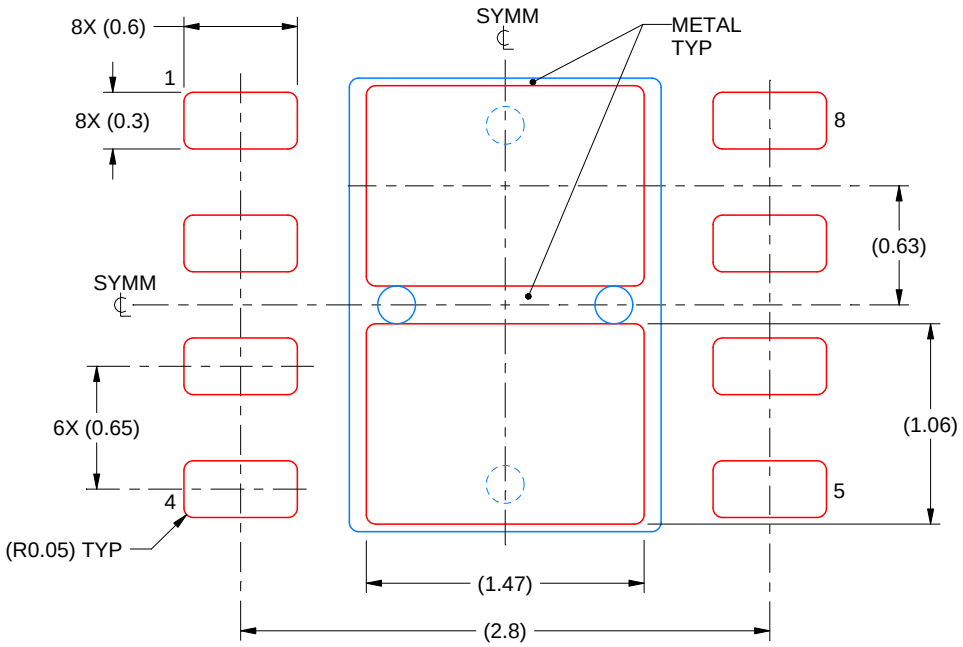


SOLDER MASK DETAILS

4218876/A 12/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

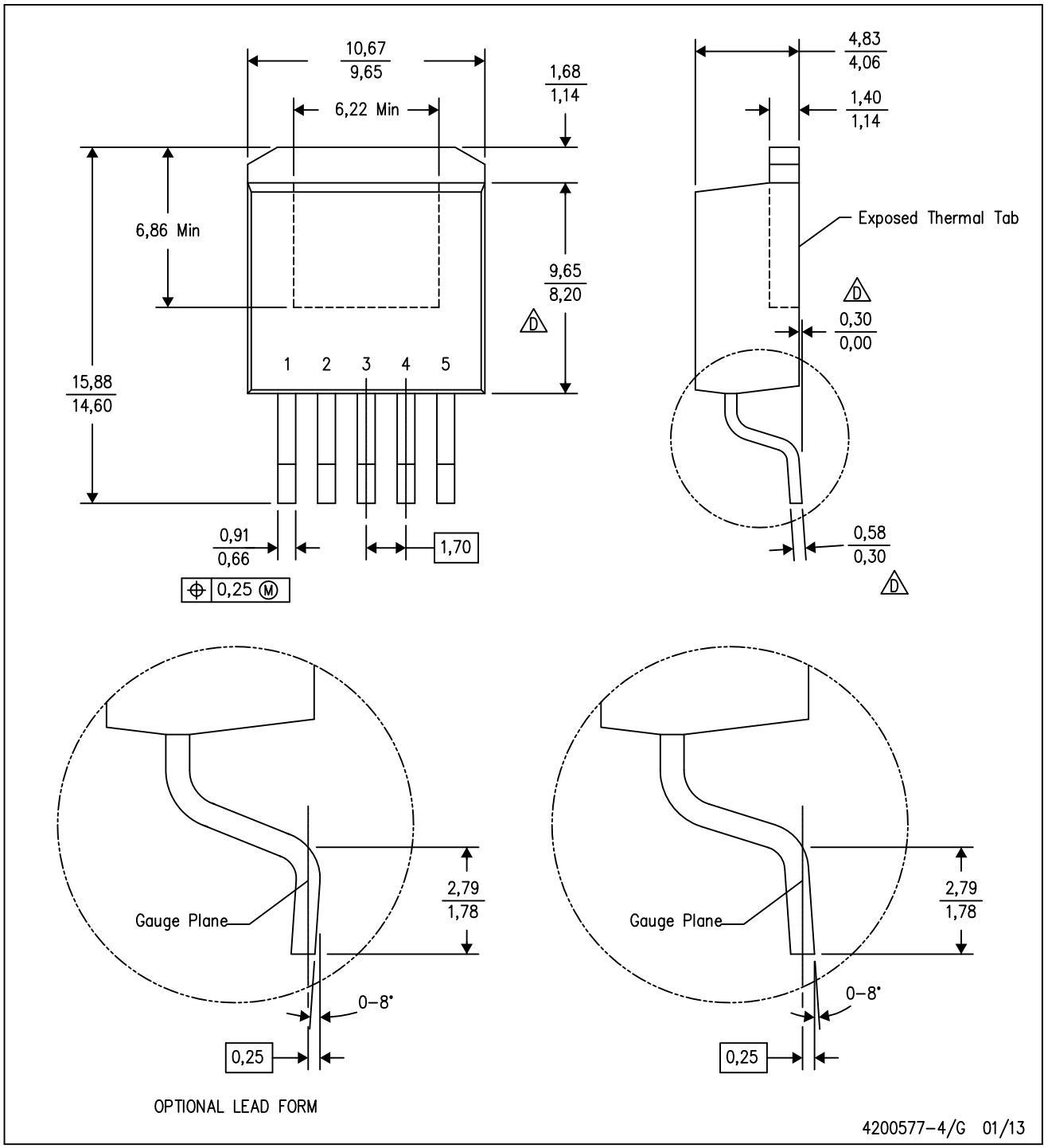
EXPOSED PAD
81% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218876/A 12/2017

NOTES: (continued)

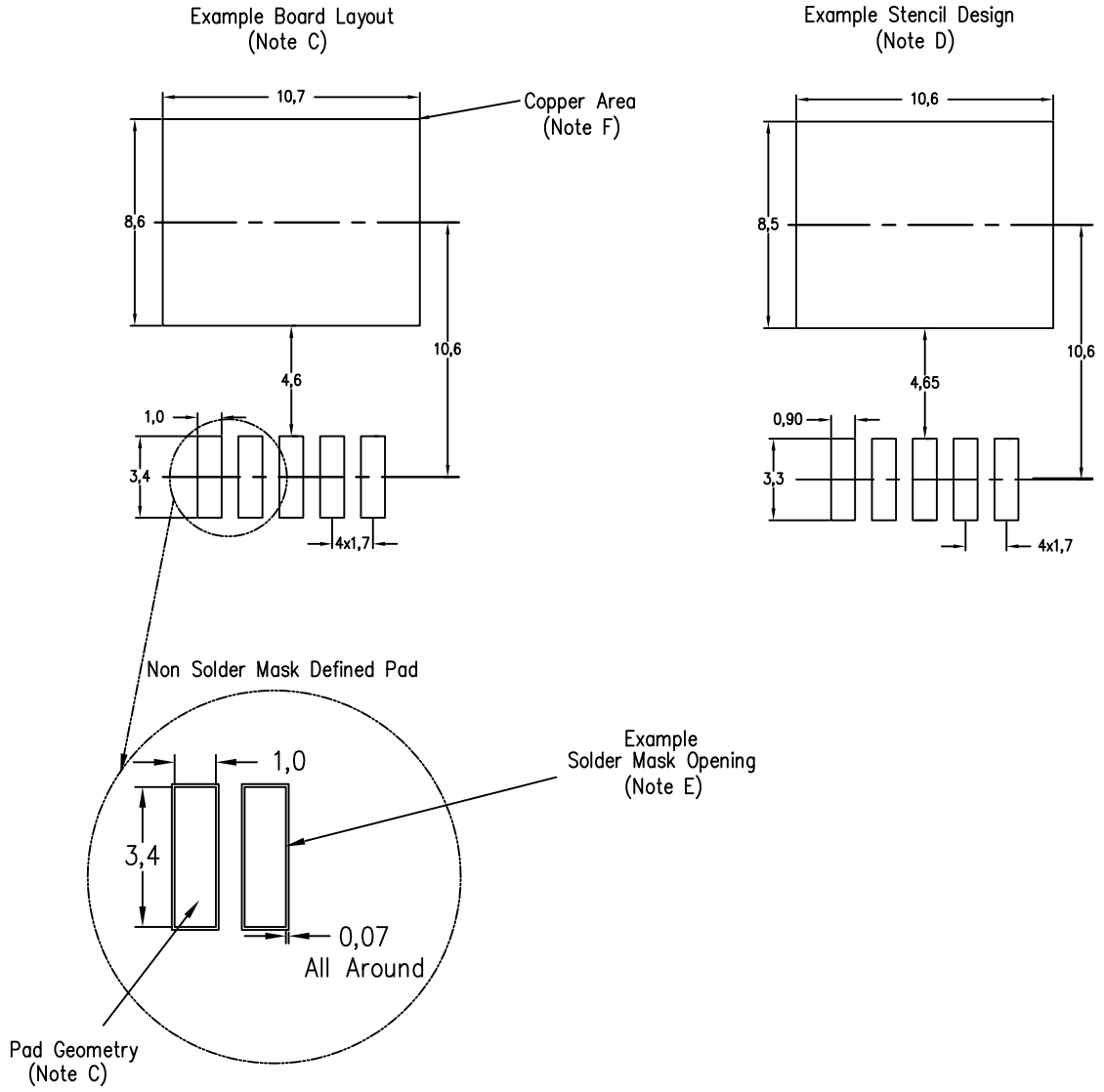
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

KTT (R–PSFM–G5) PLASTIC FLANGE–MOUNT PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash or protrusion not to exceed 0.005 (0,13) per side.
D. Falls within JEDEC TO–263 variation BA, except minimum lead thickness, maximum seating height, and minimum body length.

KTT (R–PSFM–G5) PLASTIC FLANGE–MOUNT PACKAGE



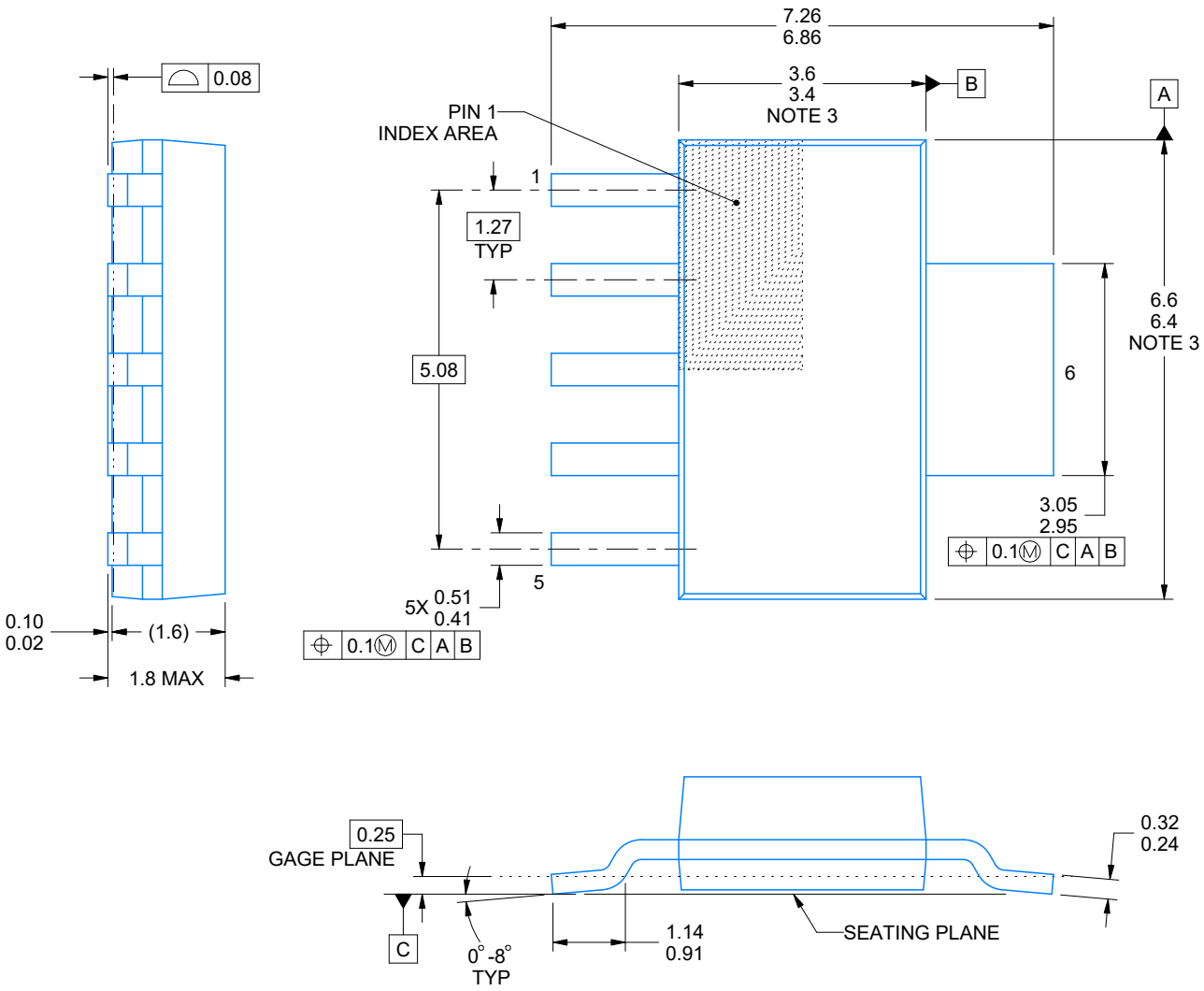
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–SM–782 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
F. This package is designed to be soldered to a thermal pad on the board. Refer to the Product Datasheet for specific thermal information, via requirements, and recommended thermal pad size. For thermal pad sizes larger than shown a solder mask defined pad is recommended in order to maintain the solderable pad geometry while increasing copper area.

PACKAGE OUTLINE

DCQ0006A

SOT - 1.8 mm max height

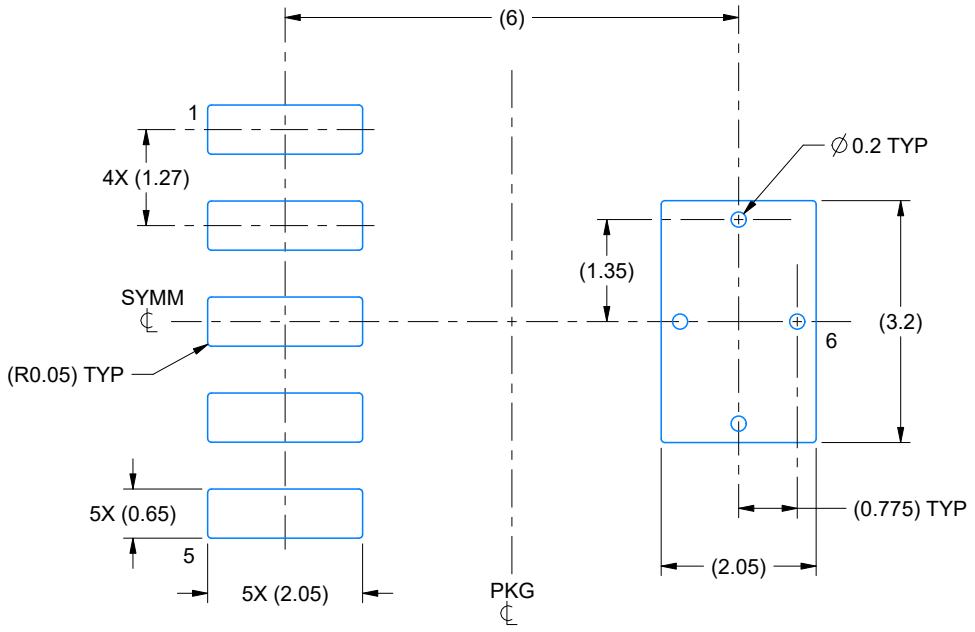
PLASTIC SMALL OUTLINE



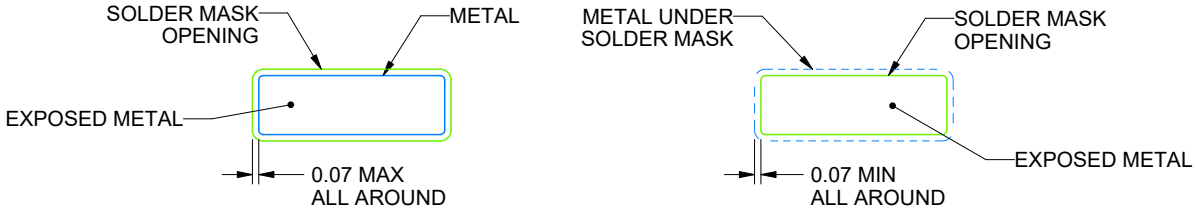
4214845/C 11/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

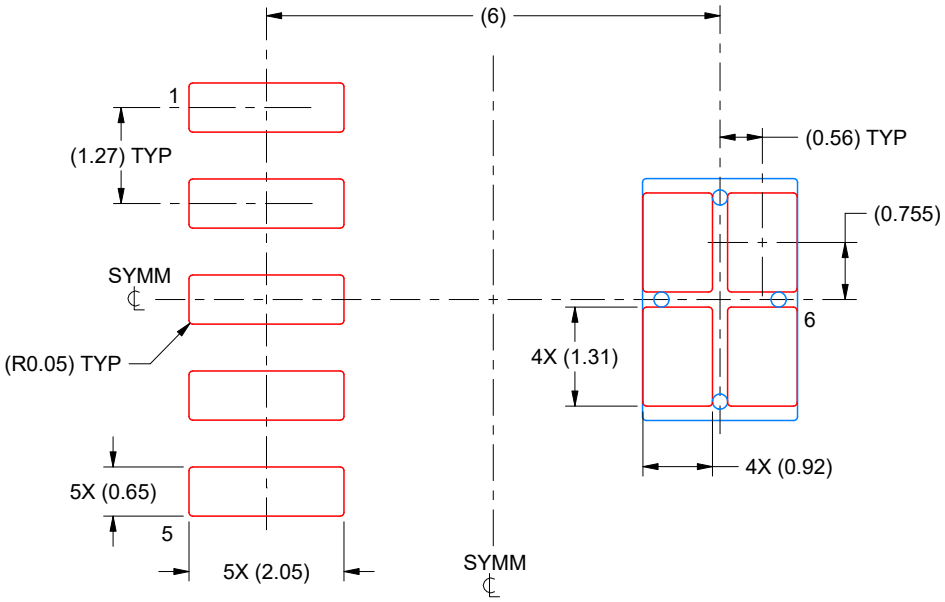


SOLDER MASK DETAILS

4214845/C 11/2021

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214845/C 11/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025