TLVx886 Zero-Drift, Low-Power, Low-Noise, Op Amp with Mux-Friendly Inputs

1 Features

- High dc precision:
  - Zero drift: 0.01µV/°C
  - Low offset voltage: 3µV
  - High PSRR: 160dB
  - High CMRR: 160dB
- Excellent ac performance:
  - Gain bandwidth: 5.4MHz
  - Slew rate: 14V/µs
  - Low noise: 9.2nV/√Hz
- Input to the negative rail, rail-to-rail output
- Low quiescent current: 570µA
- Supply range: 4.5V to 36V
- Temperature: –40°C to +125°C
- Protection features:
  - Thermal shutdown
  - Phase reversal protection
  - Latch-up protection

2 Applications

- Common redundant power supply (CRPS)
- Analog input module
- Flow transmitter
- Pressure transmitter
- Merchant battery charger
- Weigh Scale

3 Description

The TLV886, TLV2886, and TLV4886 (TLVx886) are a family of low noise, wide-bandwidth, zero-drift operational amplifiers (op amps). These op amps feature only 3µV of offset voltage (max) and 0.01µV/°C of offset voltage drift (max) over a wide temperature range.

The TLVx886 feature wide bandwidth and a low power for a wide range of applications. This family of devices are equipped with a proprietary MUX-friendly input architecture to enhance performance in multichannel, multiplexed applications.

The outstanding dc and ac performance of the TLVx886 makes these devices an excellent choice for applications requiring high precision and low noise including analog input modules, battery test, and precision instrumentation.

The TLVx886 are available in industry standard packages as well as micro-size packages to fit in the most space-constrained applications. The devices are specified for operation from –40°C to +125°C.

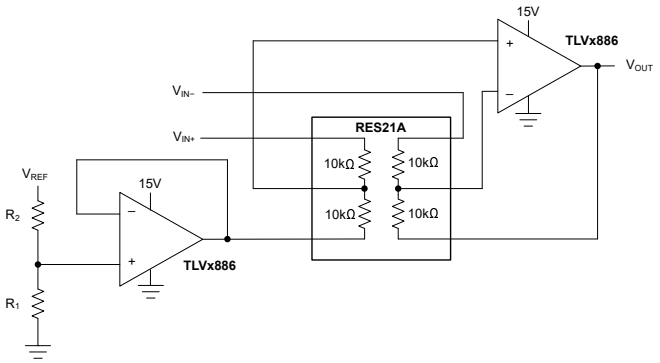
Package Information

PART NUMBER	CHANNEL COUNT	PACKAGE(2)	PACKAGE SIZE(3)
TLV886	Single	D (SOIC, 8)(1)	4.90mm × 6.00mm
		DBV (SOT-23, 5) (1)	2.90mm × 2.80mm
TLV2886	Dual	D (SOIC, 8)	4.90mm × 6.00mm
		DGK (VSSOP-8)	3.00mm × 4.90mm
TLV4886	Quad	D (SOIC, 14)(1)	8.65mm × 6.00mm
		PW (TSSOP-14) (1)	5.00mm × 6.40mm

(1) Preview information (not Production Data).
(2) For more information, see Section 10.
(3) The package size (length × width) is a nominal value and includes pins, where applicable.

Related Products

PART NUMBER	OFFSET DRIFT	GAIN BANDWIDTH	NOISE	SUPPLY CURRENT
TLVx888	0.01µV/°C	14MHz	7.5nV/√Hz	1.5mA



Difference Amplifier

Table of Contents

4 Pin Configuration and Functions

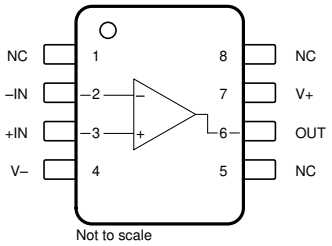


Figure 4-1. TLV886: D Package, 8-Pin SOIC (Top View)

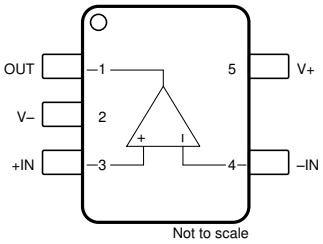


Figure 4-2. TLV886: DBV Package, 5-Pin SOT-23 (Top View)

Table 4-1. Pin Functions: TLV886

PIN			TYPE	DESCRIPTION
NAME	NO.			
	D	DBV		
–IN	2	4	Input	Inverting input
+IN	3	3	Input	Noninverting input
NC	1, 8, 5	–	_	No connection (can be left floating)
OUT	6	1	Output	Output
V–	4	2	Power	Negative (lowest) power supply
V+	7	5	Power	Positive (highest) power supply

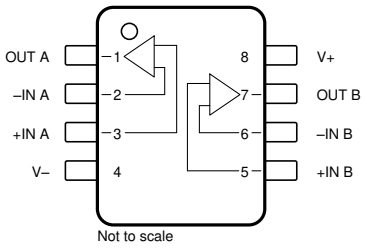


Figure 4-3. TLV2886: D Package, 8-Pin SOIC and DGK Package, 8-Pin VSSOP (Top View)

Table 4-2. Pin Functions: TLV2886

PIN		TYPE	DESCRIPTION
NAME	NO.		
–IN A	2	Input	Inverting input channel A
–IN B	6	Input	Inverting input channel B
+IN A	3	Input	Noninverting input channel A
+IN B	5	Input	Noninverting input channel B
OUT A	1	Output	Output channel A
OUT B	7	Output	Output channel B
V–	4	Power	Negative supply
V+	8	Power	Positive supply
Thermal Pad(1)	-	-	Connect thermal pad to the negative supply (V–). See also *Packages with an Exposed Thermal Pad* for more information.

(1) For DSG package only

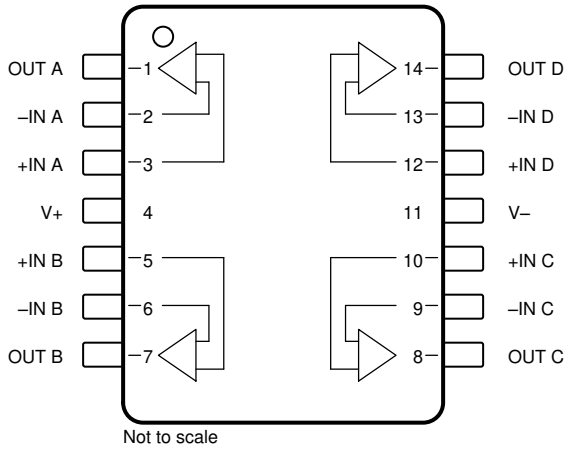


Figure 4-4. TLV4886: D Package, 14-Pin SOIC and PW Package, 14-Pin TSSOP (Top View)

Table 4-3. Pin Functions: TLV4886

PIN		TYPE	DESCRIPTION
NAME	NO.		
–IN A	2	Input	Inverting input channel A
–IN B	6	Input	Inverting input channel B
–IN C	9	Input	Inverting input channel C
–IN D	13	Input	Inverting input channel D
+IN A	3	Input	Noninverting input channel A
+IN B	5	Input	Noninverting input channel B
+IN C	10	Input	Noninverting input channel C
+IN D	12	Input	Noninverting input channel D
OUT A	1	Output	Output channel A
OUT B	7	Output	Output channel B
OUT C	8	Output	Output channel C
OUT D	14	Output	Output channel D
V–	11	Power	Negative supply
V+	4	Power	Positive supply

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_S	Supply voltage			40	V
	Signal input pins	Common-mode voltage	(V–) – 0.5	(V+) + 0.5	V
		Differential voltage		(V+) – (V–)	
		Current		±10	mA
	Output short circuit(2)		Continuous		
T_A	Operating temperature		–55	150	°C
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Short-circuit to ground, one amplifier per package. This device has been designed to limit electrical damage due to excessive output current, but extended short-circuit current, especially with higher supply voltage, can cause excessive heating and eventual thermal destruction.

5.2 ESD Ratings

			VALUE	UNIT
DBV package				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±3000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±500	
All other packages				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±3000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±250	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_S	Supply voltage, (V+) – (V–)	Single supply	4.5		36	V
		Dual supply	±2.25		±18	
T_A	Operating temperature		–40		125	°C

5.4 Thermal Information: TLV886

THERMAL METRIC[1]		TLV886		UNIT
		D (SOIC)	DBV (SOT-23)	
		8 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	149.8	197.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	88.3	110.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	93.6	62.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	36.3	36.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	92.9	62.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Thermal Information: TLV2886

THERMAL METRIC[1]		TLV2886		UNIT
		D (SOIC)	DGK (VSSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	138.4	159	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	77.7	53	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	82.3	93	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	27.7	3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	81.7	92	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.6 Thermal Information: TLV4886

THERMAL METRIC[1]		TLV4888		UNIT
		D (SOIC)	PW (TSSOP)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	95	103	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56	37	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	54	61	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	18	9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	54	60	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.7 Electrical Characteristics

at T_A = 25°C, V_S = 4.5V (±2.25V) to 36V (±18V), V_{CM} = V_{OUT} = V_S / 2, and R_{LOAD} = 10kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage(1)				±3	±15	µV
		T_A = –40°C to +125°C				±20	
dV_{OS}/dT	Input offset voltage drift(1)	T_A = –40°C to +125°C			±0.01	±0.05	µV/°C
PSRR	Power-supply rejection ratio(1)	T_A = –40°C to +125°C			±0.01	±0.5	µV/V
INPUT BIAS CURRENT							
I_B	Input bias current(1)				±50	±250	pA
		T_A = –40°C to +125°C				±3	nA
I_{OS}	Input offset current(1)				±100	±500	pA
		T_A = –40°C to +125°C				±6	nA
NOISE							
E_n	Input voltage noise	f = 0.1Hz to 10Hz			0.3		$µV_{PP}$
e_n	Input voltage noise density	f = 10Hz			9.2		$nV/\sqrt{Hz}$
		f = 100Hz			9.2		
		f = 1kHz			9.2		
i_n	Input current noise density	f = 1kHz			200		$fA/\sqrt{Hz}$
INPUT VOLTAGE							
V_{CM}	Common-mode voltage			(V–) – 0.1		(V+) – 2	V
CMRR	Common-mode rejection ratio	(V–) – 0.1V ≤ V_{CM} ≤ (V+) – 2V	V_S = ±2.25V	120	140		dB
			V_S = ±18V	140	160		
		(V–) – 0.1V ≤ V_{CM} ≤ (V+) – 2V, T_A = –40°C to +125°C(1)	V_S = ±2.25V	120	140		
			V_S = ±18V	140	160		
INPUT IMPEDANCE							
z_{id}	Differential input impedance				100 || 2.2		MΩ || pF
z_{ic}	Common-mode input impedance				1 || 1.2		TΩ || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	V_S = ±15V, (V–) + 0.6V < V_O < (V+) – 0.6V, R_{LOAD} = 10kΩ		130	148		dB
			T_A = –40°C to +125°C(1)	130			
		V_S = ±15V, (V–) + 1V < V_O < (V+) – 1V, R_{LOAD} = 2kΩ		130	144		
			T_A = –40°C to +125°C(1)	130			

5.7 Electrical Characteristics (continued)

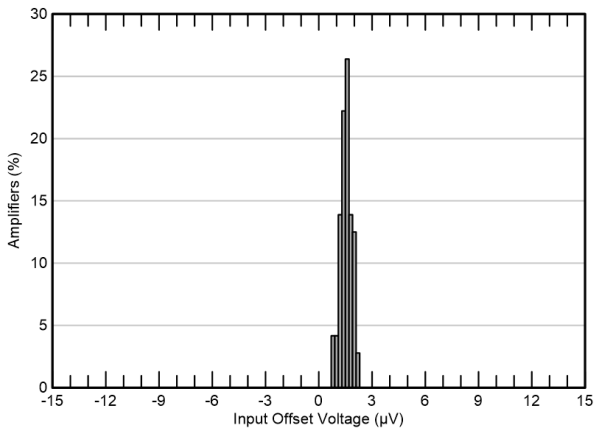
at T_A = 25°C, V_S = 4.5V (±2.25V) to 36V (±18V), V_{CM} = V_{OUT} = V_S / 2, and R_{LOAD} = 10kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product				5.4		MHz
SR	Slew rate	Gain = 1, 10V step			14		V/µs
THD+N	Total harmonic distortion + noise	Gain = 1, f = 1kHz, V_{OUT} = 4V_{RMS}			0.00012%		
	Crosstalk	f = 100kHz			110		dB
t_S	Settling time	Gain = 1, 10V step	To 0.1%		1.25		µs
			To 0.01%		12		
t_{OR}	Overload recovery time	V_{IN} × gain = V_S = ±18V			950		ns
OUTPUT							
V_O	Voltage output swing from rail	Positive rail, V_S = 30V	No load(1)		6	20	mV
			R_{LOAD} = 10kΩ		115	150	
			R_{LOAD} = 2kΩ		500	575	
		Negative rail, V_S = 30V	No load(1)		6	20	
			R_{LOAD} = 10kΩ		112	135	
			R_{LOAD} = 2kΩ		515	575	
		R_{LOAD} = 10kΩ, T_A = –40°C to +125°C, both rails(1)				250	
I_{SC}	Short-circuit current	Sourcing			35		mA
		Sinking			–54		
C_{LOAD}	Capacitive load drive				See *Typical Characteristics*		pF
Z_O	Open-loop output impedance	f = 1MHz			460		Ω
POWER SUPPLY							
I_Q	Quiescent current per amplifier	TLV886, I_O = 0A			670	795	µA
			T_A = –40°C to +125°C(1)		670	800	
		TLV2886 and TLV4886, I_O = 0A			570	650	
			T_A = –40°C to +125°C(1)		570	655	

(1) Specification established from device population bench system measurements.

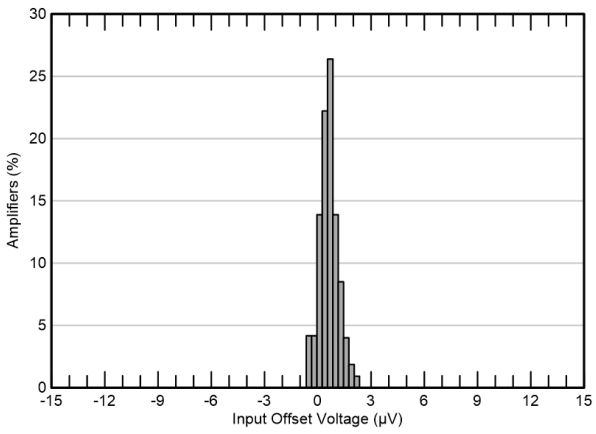
5.8 Typical Characteristics

at T_A = 25°C, V_S = ±18V, V_{CM} = V_S / 2, and R_L = 10kΩ (unless otherwise noted)



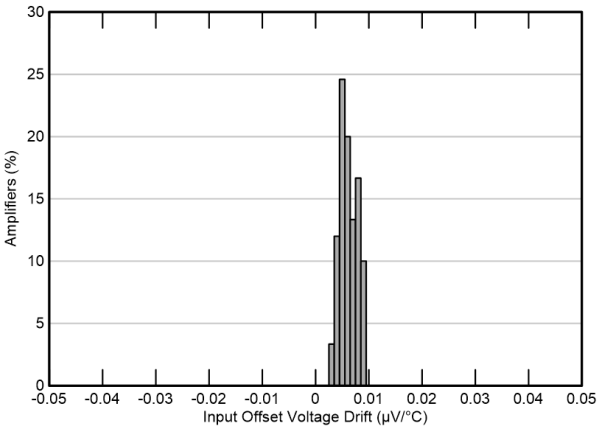
60 units

Figure 5-1. Offset Voltage Distribution



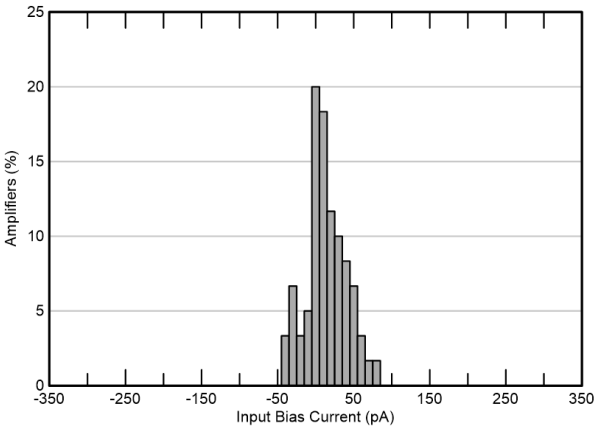
T_A = 125°C, 60 units

Figure 5-2. Offset Voltage Distribution



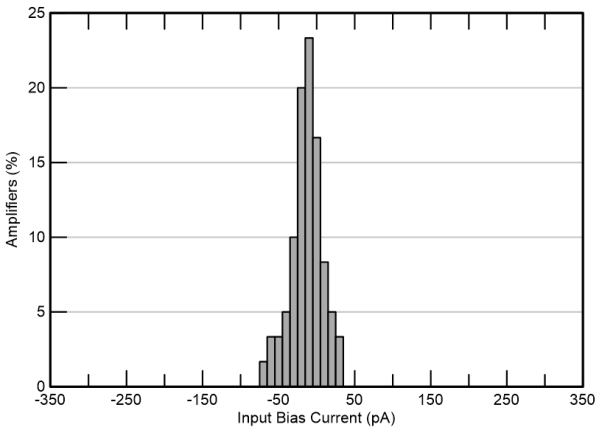
T_A = –40°C to +125°C, 60 units

Figure 5-3. Offset Voltage Drift



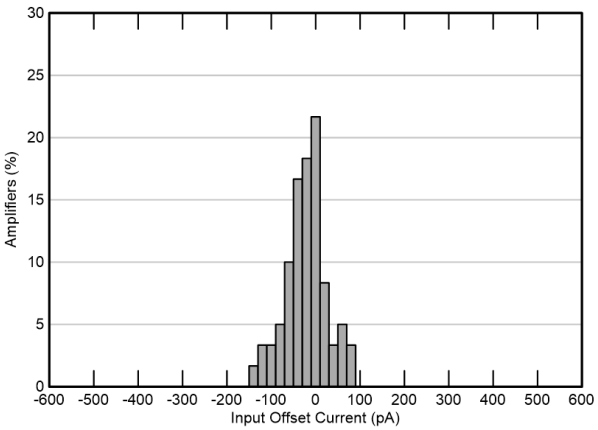
60 units

Figure 5-4. Input Bias Current Distribution, I_{BN}



60 units

Figure 5-5. Input Bias Current Distribution, I_{BP}

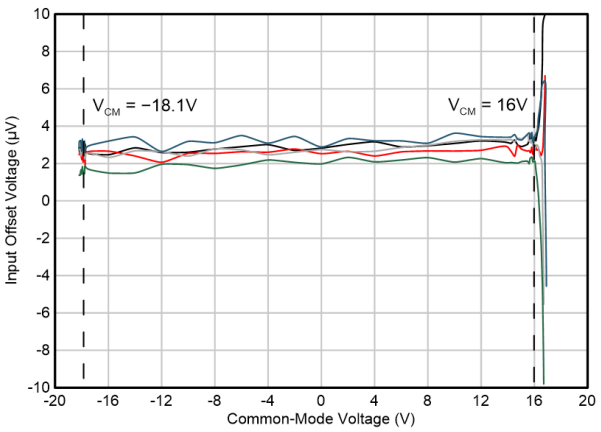


60 units

Figure 5-6. Input Offset Current Distribution

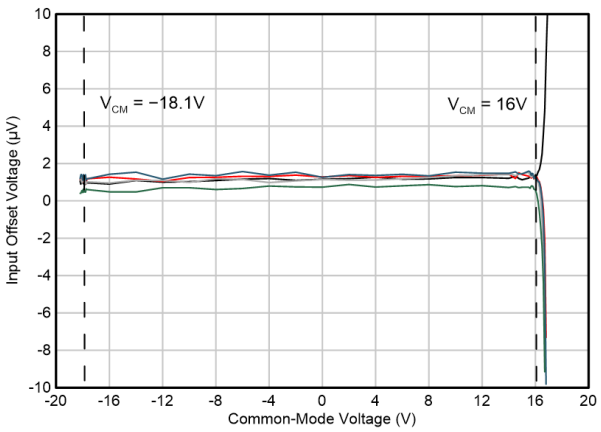
5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18V, V_{CM} = V_S / 2, and R_L = 10kΩ (unless otherwise noted)



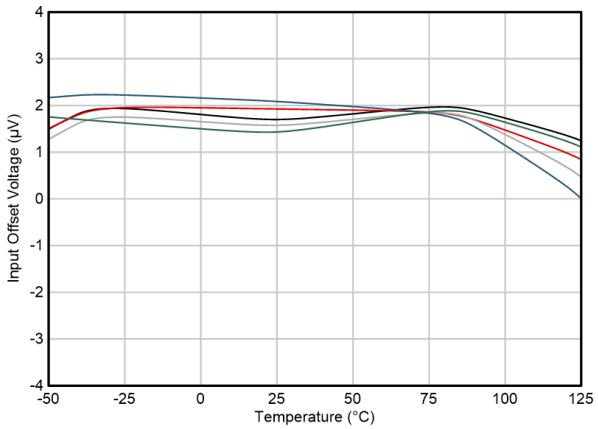
5 typical units

Figure 5-7. Offset Voltage vs Common-Mode Voltage



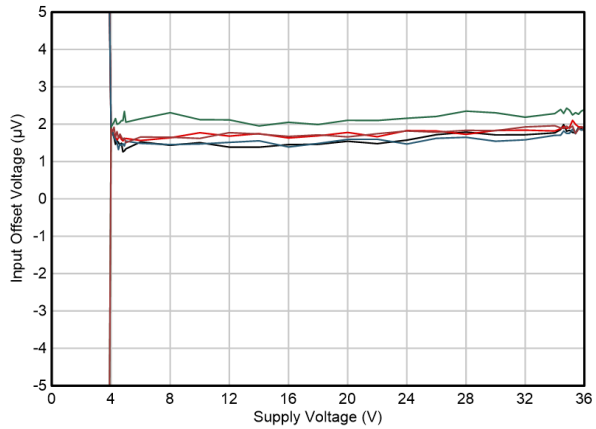
T_A = 125°C, 5 typical units

Figure 5-8. Offset Voltage vs Common-Mode Voltage



5 typical units

Figure 5-9. Offset Voltage vs Temperature



5 typical units

Figure 5-10. Offset Voltage vs Supply Voltage

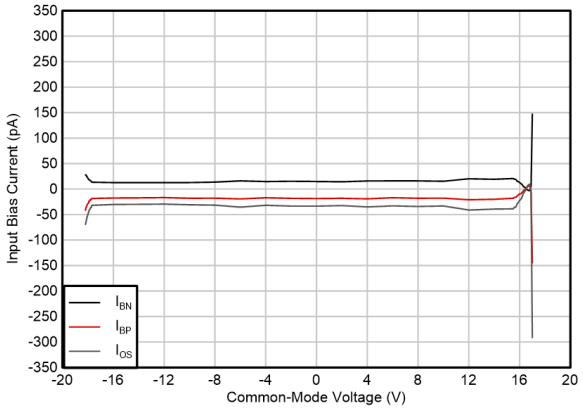


Figure 5-11. Input Bias Current vs Common-Mode Voltage

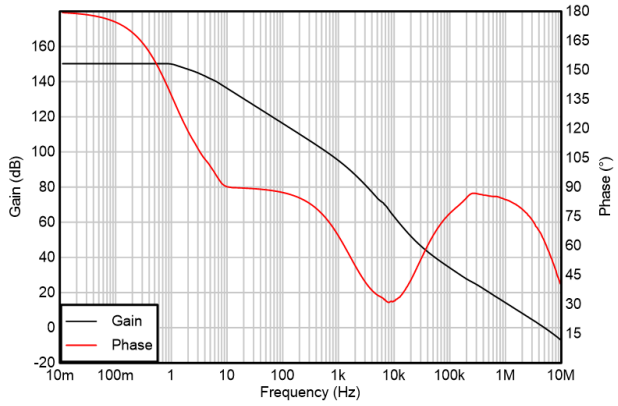


Figure 5-12. Open-Loop Gain and Phase vs Frequency

5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18V, V_{CM} = V_S / 2, and R_L = 10kΩ (unless otherwise noted)

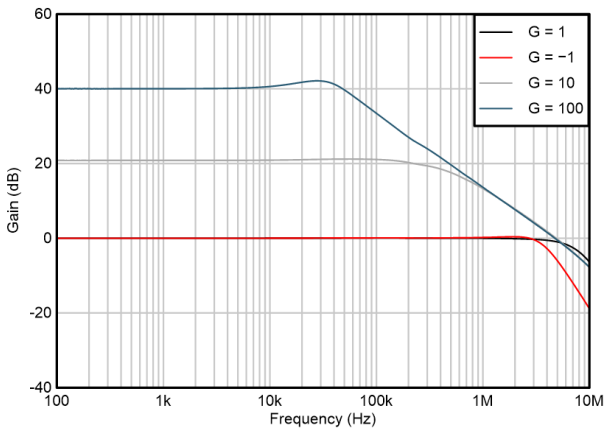


Figure 5-13. Closed-Loop Gain vs Frequency

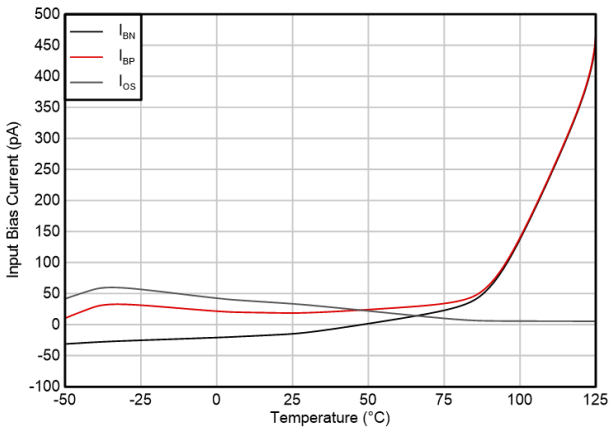


Figure 5-14. Input Bias Current and Offset Current vs Temperature

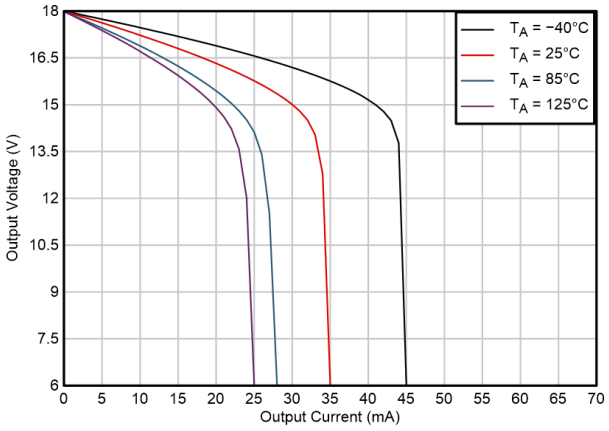


Figure 5-15. Output Voltage Swing vs Output Current (Sourcing)

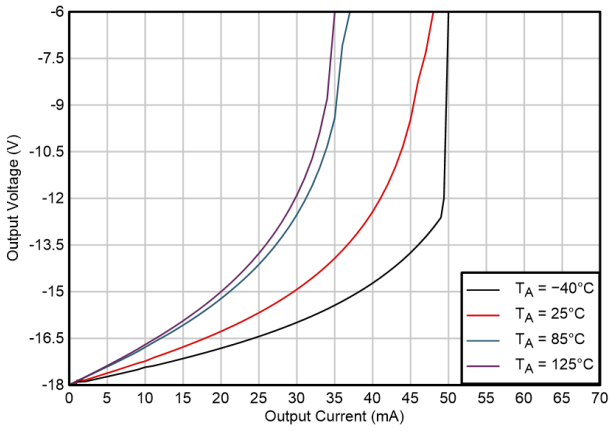


Figure 5-16. Output Voltage Swing vs Output Current (Sinking)

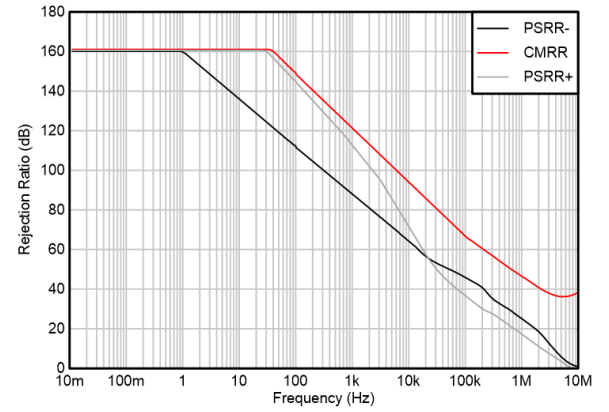
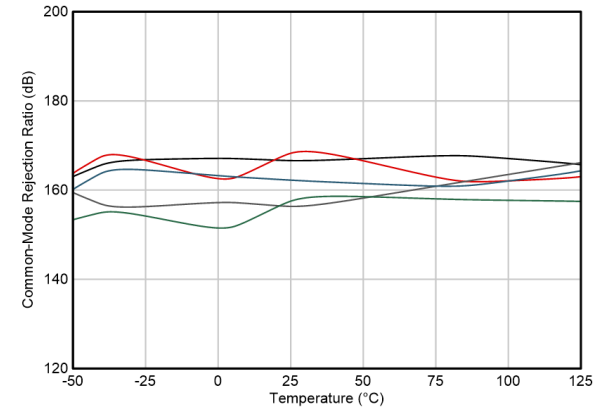


Figure 5-17. CMRR and PSRR vs Frequency

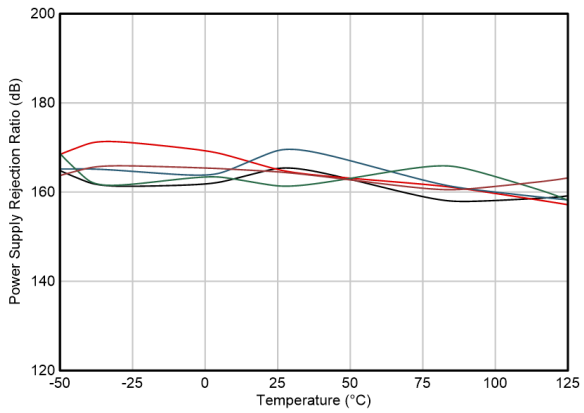


5 typical units

Figure 5-18. CMRR vs Temperature

5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18V, V_{CM} = V_S / 2, and R_L = 10kΩ (unless otherwise noted)



5 typical units

Figure 5-19. PSRR vs Temperature

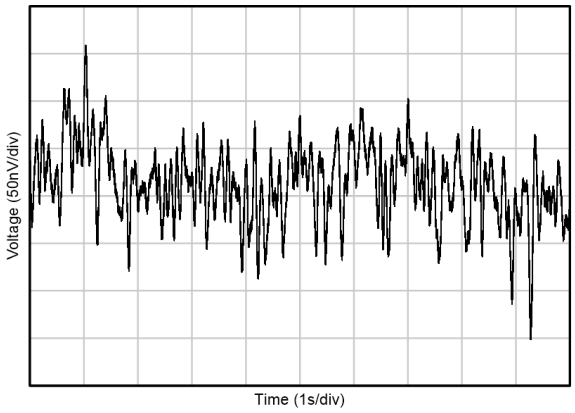


Figure 5-20. 0.1Hz to 10Hz Voltage Noise

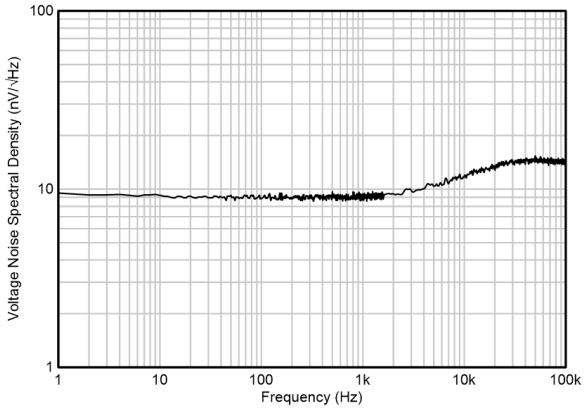


Figure 5-21. Input Voltage Noise Spectral Density vs Frequency

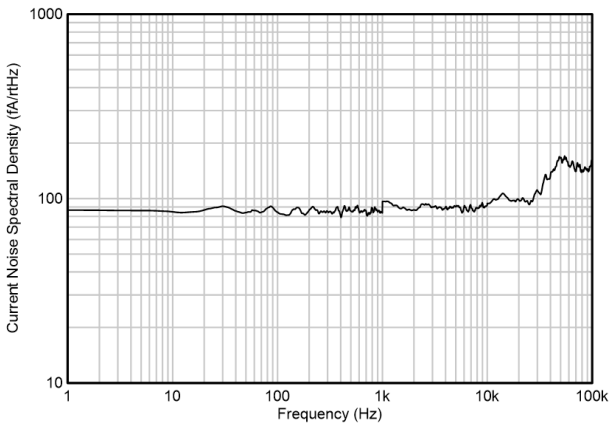
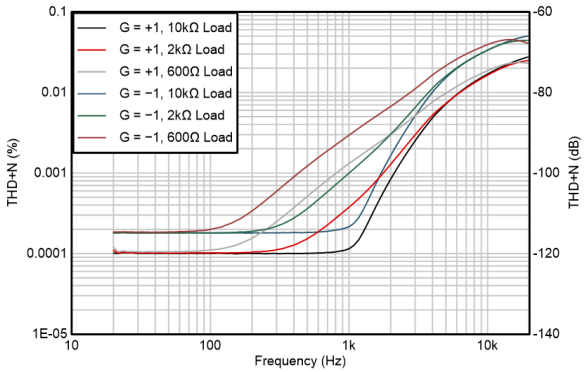
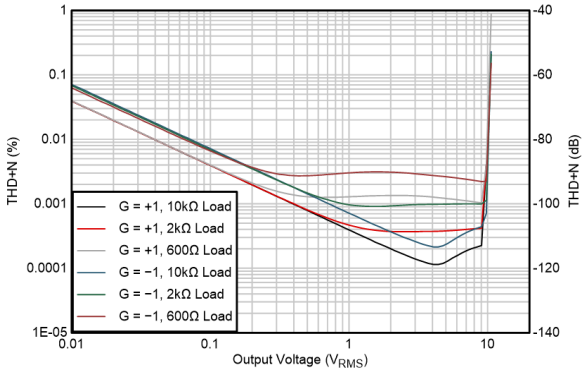


Figure 5-22. Input Current Noise Spectral Density vs Frequency



V_{OUT} = 4V_{RMS}, 80kHz bandwidth

Figure 5-23. THD+N vs Frequency

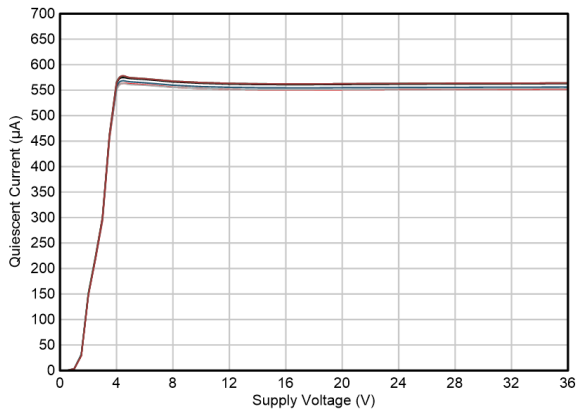


f = 1kHz

Figure 5-24. THD+N vs Output Amplitude

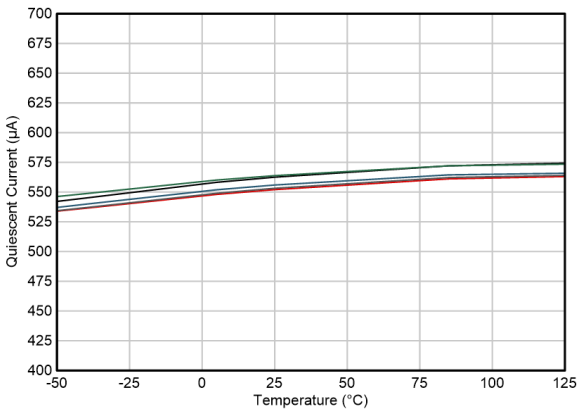
5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18V, V_{CM} = V_S / 2, and R_L = 10kΩ (unless otherwise noted)



5 typical units

Figure 5-25. Quiescent Current vs Supply Voltage



5 typical units

Figure 5-26. Quiescent Current vs Temperature

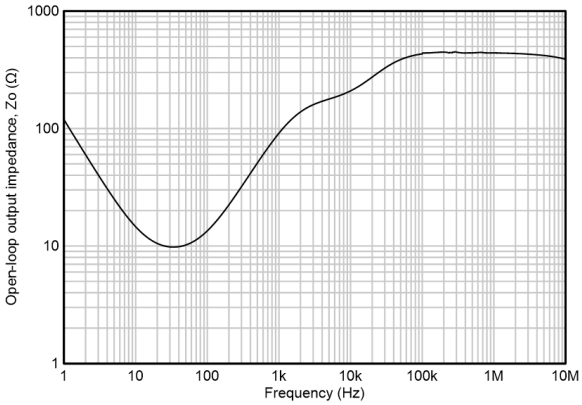
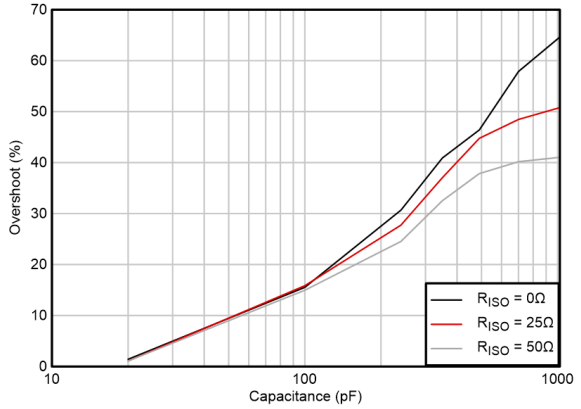
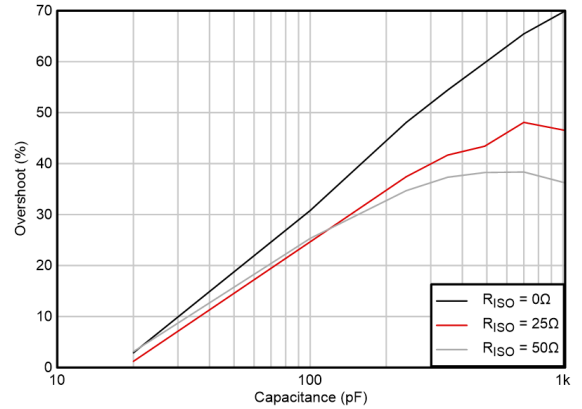


Figure 5-27. Open-Loop Output Impedance vs Frequency



Gain = –1, 10mV step

Figure 5-28. Small-Signal Overshoot vs Capacitive Load



Gain = 1, 10mV step

Figure 5-29. Small-Signal Overshoot vs Capacitive Load

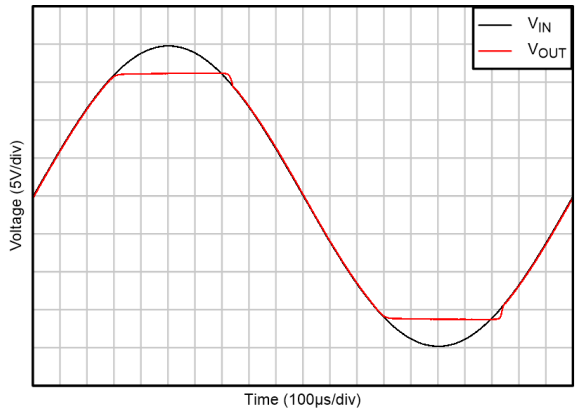


Figure 5-30. No Phase Reversal

5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18V, V_{CM} = V_S / 2, and R_L = 10kΩ (unless otherwise noted)

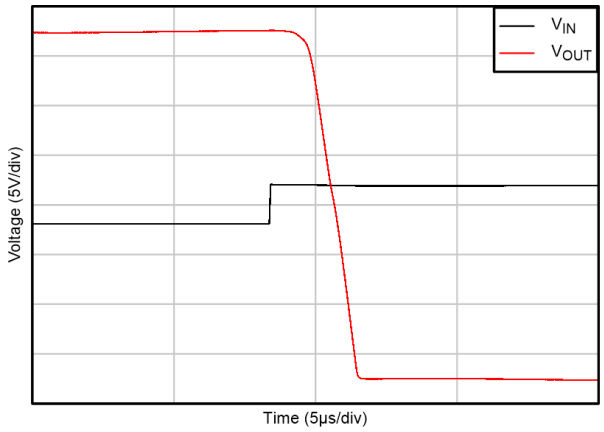


Figure 5-31. Positive Overload Recovery

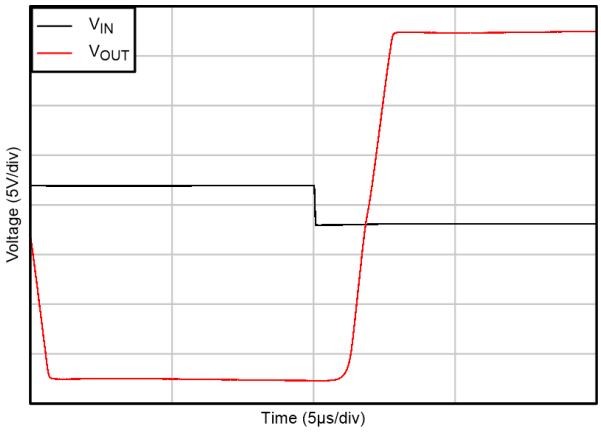
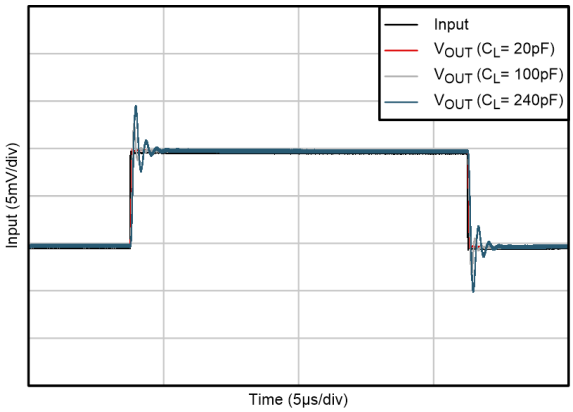
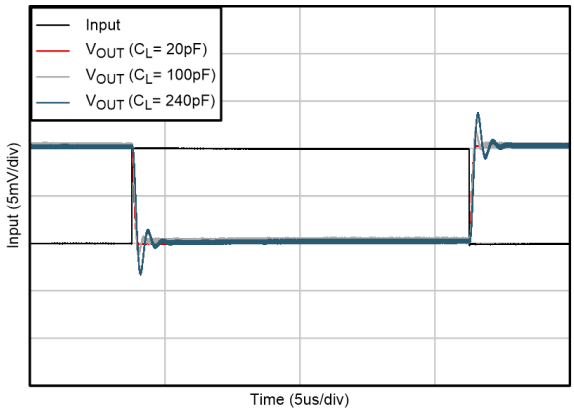


Figure 5-32. Negative Overload Recovery



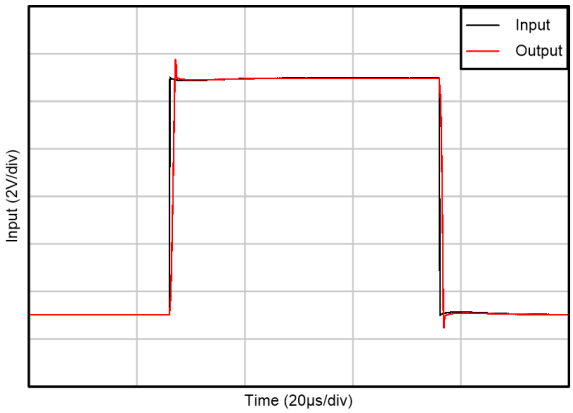
Gain = 1, 10mV step

Figure 5-33. Small-Signal Step Response



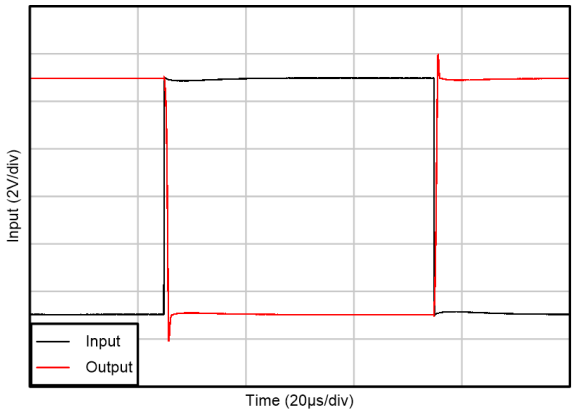
Gain = –1, 10mV step, C_F = 3pF, R_F = 10kΩ

Figure 5-34. Small-Signal Step Response



Gain = 1, 10V step

Figure 5-35. Large-Signal Step Response



Gain = –1, 10V step, C_F = 3pF, R_F = 10kΩ

Figure 5-36. Large-Signal Step Response

5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18V, V_{CM} = V_S / 2, and R_L = 10kΩ (unless otherwise noted)

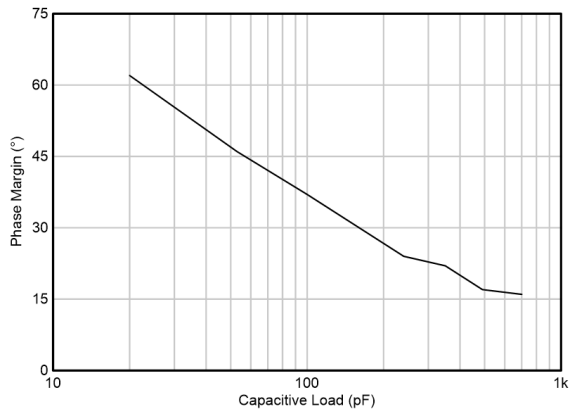
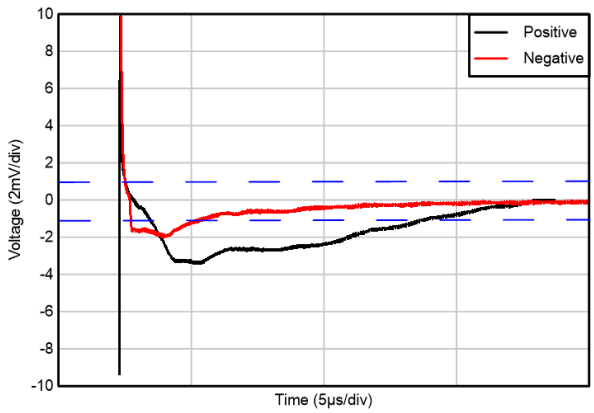


Figure 5-37. Phase Margin vs Capacitive Load



10V step, 0.01% settling

Figure 5-38. Settling Time

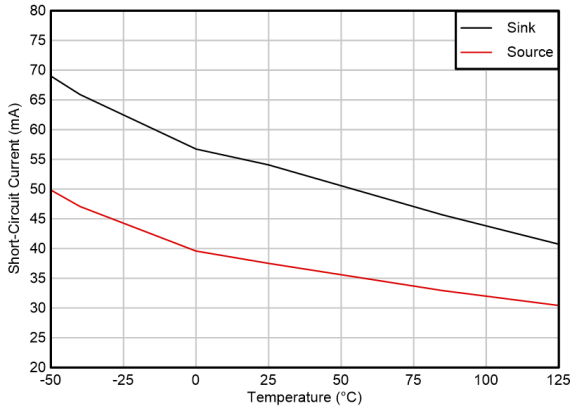


Figure 5-39. Short Circuit Current vs Temperature

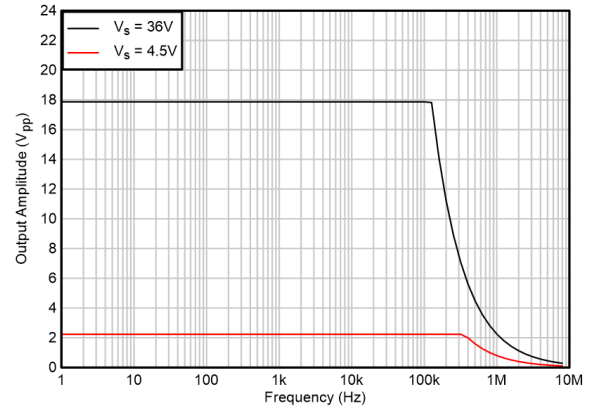


Figure 5-40. Maximum Output Voltage vs Frequency

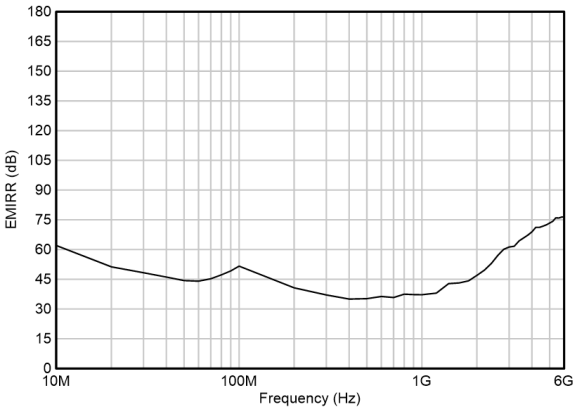


Figure 5-41. EMIRR vs Frequency

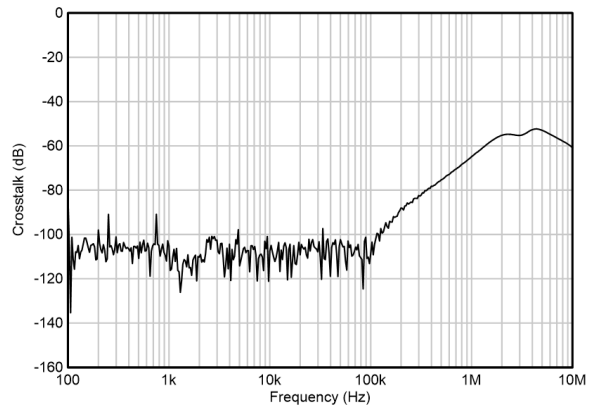


Figure 5-42. Channel Separation

6 Detailed Description

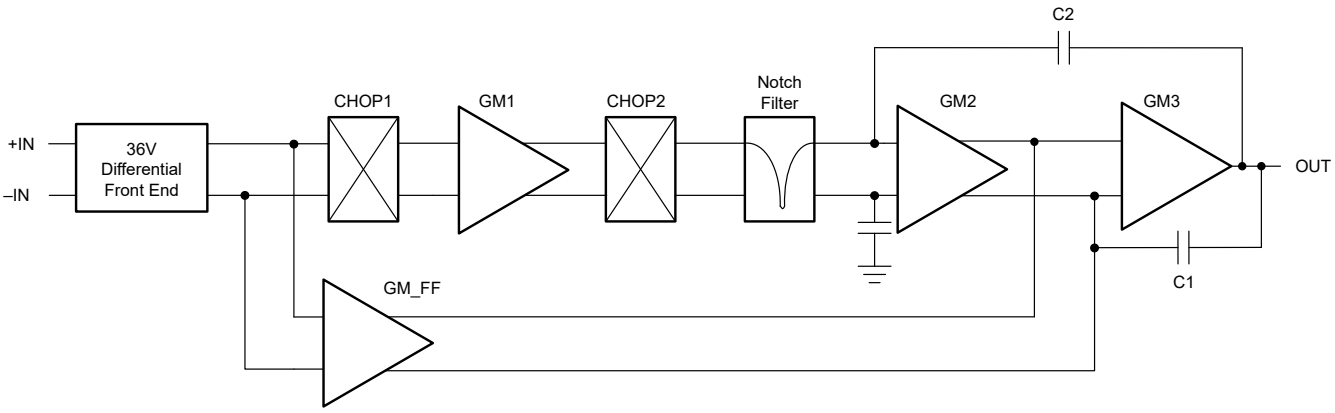
6.1 Overview

The TLVx886 operational amplifiers combine precision offset and drift with excellent overall performance, making the device a great choice for a wide variety of precision applications. The precision offset drift of only 0.01µV/°C provides stability over the entire operating temperature range of –40°C to +125°C. In addition, this device offers excellent linear performance with high CMRR, PSRR, and A_{OL}. As with all amplifiers, applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases, 0.1µF capacitors are adequate. For details and a layout example, see Section 7.4.

The TLVx886 is part of a family of zero-drift, MUX-friendly operational amplifiers. This device operates from 4.5V to 36V, consumes less than 1mA of quiescent current, is unity-gain stable, and is designed for a wide range of general-purpose and precision applications. The zero-drift architecture provides ultra-low input offset voltage and near-zero input offset voltage drift over temperature and time. This choice of architecture also offers outstanding ac performance, such as low broadband noise, and zero flicker noise when operating at less than the chopper frequency.

The following section shows a representation of the proprietary TLVx886 architecture.

6.2 Functional Block Diagram



6.3 Feature Description

The TLVx886 operational amplifiers use a proprietary, periodic auto-calibration technique to provide extremely low input offset voltage and input offset voltage drift over time and temperature. The devices have several integrated features to help maintain a high level of precision through a variety of applications. These include a phase-reversal protection, EMI rejection, electrical overstress protection, and MUX-friendly inputs.

Several design techniques and considerations to maintain the specified performance of the TLVx886 are detailed in the *Optimizing Chopper Amplifier Accuracy* and *Op Amp Offset Voltage and Bias Current Limitations* application notes.

6.3.1 Input Common-Mode Range

The TLVx886 are specified for operation from 4.5V to 36V (±2.25V to ±18V). The TLVx886 provide a wide input common-mode voltage (V_{CM}) range that includes the negative rail making them an excellent choice for single supply operation. The input common-mode voltage to the positive rail is limited to (V+) − 2V. Limit the input common mode voltage to (V–) – 0.1V ≤ V_{CM} ≤ (V+) – 2V to maintain specified performance.

6.3.2 MUX-Friendly Inputs

The TLVx886 features a proprietary input stage design that allows an input differential voltage to be applied while maintaining high input impedance. Typically, high-voltage CMOS or bipolar-junction input amplifiers feature antiparallel diodes that protect input transistors from large gate to source (V_{GS}) voltages that can exceed the semiconductor process maximum and permanently damage the device. Large V_{GS} voltages can be forced when applying a large input step, switching between channels, or attempting to use the amplifier as a comparator.

The TLVx886 solves these problems with a switched-input technique that prevents large input bias currents when large differential voltages are applied. This input architecture addresses many issues seen in switched or multiplexed applications, where large disruptions to RC filtering networks are caused by fast switching between large potentials.Figure 6-1 shows a typical application where MUX-Friendly inputs can improve settling time performance. The TLVx886 offers outstanding settling performance as a result of these design innovations and built-in slew-rate boost and wide bandwidth. The TLVx886 can also be used as a comparator. Differential and common-mode input ranges still apply.

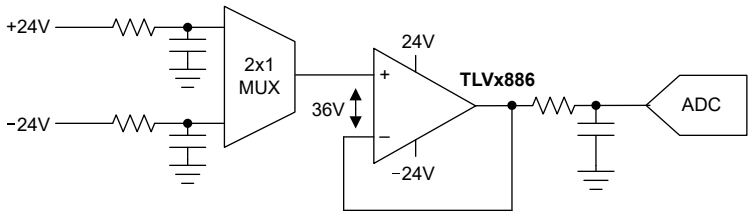


Figure 6-1. Multiplexed Application

6.3.3 Phase-Reversal Protection

The TLVx886 have internal phase-reversal protection. Some op amps exhibit a phase reversal when the input is driven beyond the linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The TLVx886 input prevents phase reversal with excessive common-mode voltage. Instead, the output limits into the appropriate rail.

6.3.4 Chopping Transients

Zero-drift amplifiers such as the TLVx886 use a switching architecture on the inputs to correct for the intrinsic offset and drift of the amplifier. Charge injection from the integrated switches on the inputs can introduce short transients in the input bias current of the amplifier. The extremely short duration of these pulses prevents the pulses from amplifying; however, the pulses can be coupled to the output of the amplifier through the feedback network. Use low value resistors to minimize the input transient effects at the output of the amplifier. Use a low-pass filter, such as an RC network, to minimize any additional noise attributed to the transients. The chopping frequency of the TLVx886 is typically 200kHz.

6.3.5 EMI Rejection

The TLVx886 provides good electromagnetic interference (EMI) rejection performance to reduce the effects of EMI interference from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the TLVx886 benefits from these design improvements.

High-frequency signals conducted or radiated to any pin of the operational amplifier can result in adverse effects, as there is insufficient amplifier loop gain to correct for signals with spectral content outside the bandwidth. Conducted or radiated EMI on inputs, power supply, or output can result in unexpected dc offsets, transient voltages, or other unknown behavior. Take care to properly shield and isolate sensitive analog nodes from noisy radio signals and digital clocks and interfaces.

6.3.6 Electrical Overstress

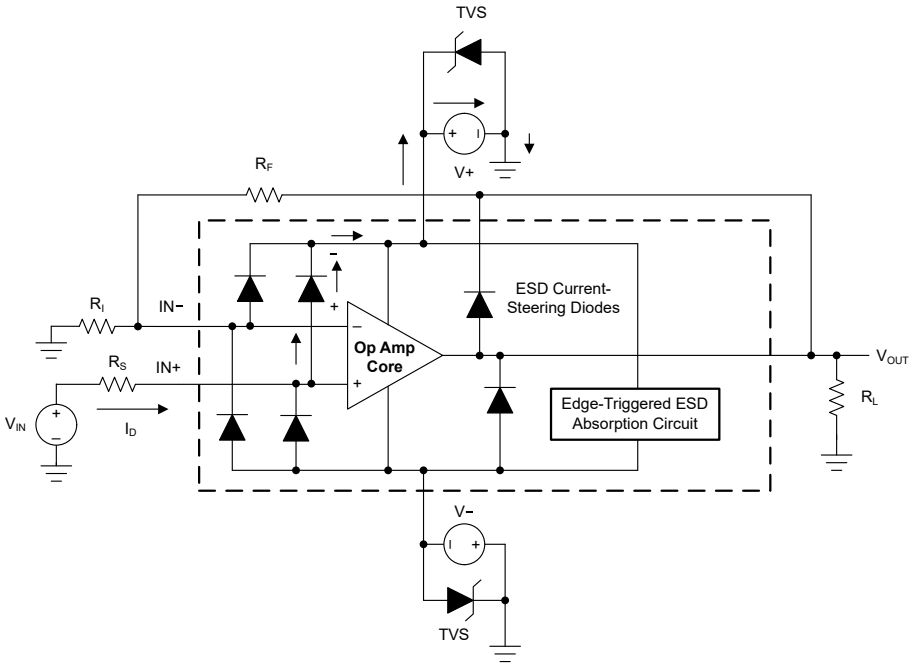
Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but can involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect from accidental ESD events both before and during product assembly.

A good understanding of this basic ESD circuitry and the relevance to an electrical overstress event is helpful. Figure 6-2 shows an illustration of the ESD circuits contained in the TLVx886 (shows as the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device internal to the op amp. This protection circuitry is intended to remain inactive during normal circuit operation.

An ESD event produces a short-duration, high-voltage pulse that is transformed into a short-duration, high-current pulse while discharging through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent damage. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more amplifier device pins, current flows through one or more steering diodes. Depending on the path that the current takes, the absorption device can activate. The absorption device has a trigger or threshold voltage that is greater than the normal operating voltage of the TLVx886, but less than the device breakdown voltage level. When this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

Figure 6-2 shows that when the operational amplifier connects into a circuit, the ESD protection components are intended to remain inactive, and do not become involved in the application circuit operation. However, circumstances can arise where an applied voltage exceeds the operating voltage range of a given pin. If this condition occurs, there is a risk that some internal ESD protection circuits are biased on and conduct current. Any such current flow occurs through steering-diode paths and rarely involves the absorption device.



Notes: V_{IN} = (V+) + 500mV.
TVS: V+ < $V_{TVSBR\ (min)}$ < 40V, where $V_{TVSBR\ (min)}$ is the minimum specified value for the TVS breakdown voltage.
Suggested value for R_S is approximately 5kΩ in an overvoltage condition.

Figure 6-2. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application

Figure 6-2 shows a specific example where the input voltage (V_{IN}) exceeds the positive supply voltage (V+) by 500mV or more. Much of what happens in the circuit depends on the supply characteristics. If V+ can sink the current, one of the upper input steering diodes conducts and directs current to $+V_S$. Excessively high current levels can flow with increasingly higher V_{IN}. As a result, the data sheet specifications recommend that applications limit the input current to 10mA.

If the supply is not capable of sinking the current, V_{IN} can begin sourcing current to the operational amplifier, and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings.

Another common question involves what happens to the amplifier if an input signal is applied to the input while the power supplies V+ or V– are at 0V. Again, this question depends on the supply characteristic while at 0V, or at a level below the input signal amplitude. If the supplies appear as high impedance, then the operational amplifier supply current can be supplied by the input source through the current-steering diodes. This state is not a normal biasing condition for the amplifier and can result in specification degradation or abnormal operation. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current, and any resistance in the input path.

If there is any uncertainty about the ability of the supply to absorb this current, add external transient voltage suppressor (TVS) diodes to the supply pins; see also Figure 6-2. The breakdown voltage must be selected such that the diode does not turn on during normal operation. However, the breakdown voltage must be low enough so that the TVS diode conducts if the supply pin begins to rise above the safe operating supply voltage level.

6.4 Device Functional Modes

The TLVx886 has a single functional mode, and is operational when the power-supply voltage is greater than 4.5V (±2.25V). The recommended power supply voltage for the TLVx886 is 36V (±18V).

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The TLVx886 operational amplifiers provide a good trade-off between gain-bandwidth, noise, and current consumption. The TLVx886 excel in applications that require signal conditioning for very low level signals like current sensing, Wheatstone bridges, thermocouples, resistance temperature detectors (RTDs), electrocardiograms (ECG). The low offset and wide bandwidth enable very high gain configurations, while the low broadband noise and near zero flicker noise help maintain signal fidelity.

7.1.1 Basic Noise Calculations

Low-noise circuit design requires careful analysis of all noise sources. In many cases, external noise sources can dominate; consider the effect of source resistance on overall op-amp noise performance. Total noise of the circuit is the root-sum-square combination of all noise components.

The resistive portion of the source impedance produces thermal noise proportional to the square root of the resistance. The source impedance is typically fixed; consequently, select op amp and the feedback resistors that minimize the respective contributions to the total noise.

Figure 7-1 shows the noninverting op-amp circuit configurations with gain. Figure 7-2 shows the inverting op-amp circuit configurations with gain. In circuit configurations with gain, the feedback network resistors also contribute noise. In general, the current noise of the op amp reacts with the feedback resistors to create additional noise components. However, the low current noise of the TLVx886 means that the current noise contribution can be ignored.

The feedback resistor values can generally be chosen to make these noise sources negligible. Low impedance feedback resistors load the output of the amplifier. The equations for total noise are shown for both configurations.

For additional resources on noise calculations, visit *TI Precision Labs*.

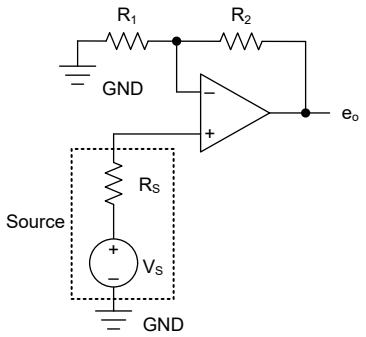


Figure 7-1. Noise Calculation in Noninverting Gain Configurations

$$E_o = e_o\sqrt{BW_N}\ [V_{RMS}] \quad (1)$$

$$e_o = \left(1 + \frac{R_2}{R_1}\right)\sqrt{e_S{}^2 + e_N{}^2 + \left(e_{R_1||R_2}\right)^2 + \left(i_N R_S\right)^2 + \left(i_N \frac{R_1 R_2}{R_1 + R_2}\right)^2}\left[\frac{V}{\sqrt{Hz}}\right] \quad (2)$$

$$e_S = \sqrt{4k_B T(K) R_S}\left[\frac{V}{\sqrt{Hz}}\right] \quad (3)$$

$$e_{R_1||R_2} = \sqrt{4k_B T(K)\left(\frac{R_1 R_2}{R_1 + R_2}\right)}\left[\frac{V}{\sqrt{Hz}}\right] \quad (4)$$

$$k_B = 1.38065\ \times 10^{-23}\left[\frac{J}{K}\right] \quad (5)$$

$$T(K) = 2.37.15 + T(°C)\ [K] \quad (6)$$

where

- e_N is the voltage noise spectral density of the amplifier. For the TLVx886, e_n = 9.2nV/$\sqrt{Hz}$ at 1kHz)
- i_N is the current noise spectral density of the amplifier. For the TLVx886, i_n = 200fA/$\sqrt{Hz}$ at 1kHz)
- e_o is the total noise density
- e_S is the thermal noise of R_S
- $e_{R_1\ ||\ R_2}$ is the thermal noise of R_1 || R_2
- k_B is the Boltzmann constant
- T(K) is the temperature in kelvins

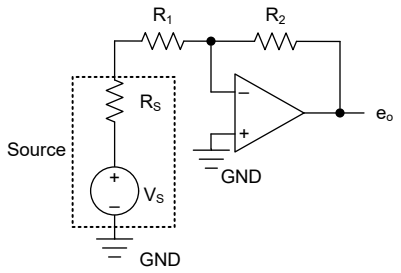


Figure 7-2. Noise Calculation in Inverting Gain Configurations

$$E_o = e_o\sqrt{BW_N}\,[V_{RMS}] \tag{7}$$

$$e_o = \left(1 + \frac{R_2}{R_S + R_1}\right)\sqrt{{e_N}^2 + \left(e_{R_1 + R_S||R_2}\right)^2 + \left(i_N\frac{(R_S + R_1)R_2}{R_S + R_1 + R_2}\right)^2}\left[\frac{V}{\sqrt{Hz}}\right] \tag{8}$$

$$e_{R_1 + R_S||R_2} = \sqrt{4k_BT(K)\left(\frac{(R_S + R_1)R_2}{R_S + R_1 + R_2}\right)}\left[\frac{V}{\sqrt{Hz}}\right] \tag{9}$$

$$k_B = 1.38065\ \times 10^{-23}\left[\frac{J}{K}\right] \tag{10}$$

$$T(K) = 2.37.15 + T(°C)\,[K] \tag{11}$$

where

- See

- e_N is the voltage noise spectral density of the amplifier. For the TLVx886, e_n = 9.2nV/$\sqrt{Hz}$ at 1kHz)
- i_N is the current noise spectral density of the amplifier. For the TLVx886, i_n = 200fA/$\sqrt{Hz}$ at 1kHz)
- e_o is the total noise density
- e_S is the thermal noise of R_S
- $e_{(R_1 + R_S)\,||\,R_2}$ is the thermal noise of $(R_1 + R_S)\,||\,R_2$
- k_B is the Boltzmann constant
- T(K) is the temperature in kelvins

7.2 Typical Applications

7.2.1 High Gain Pre-Amplifier

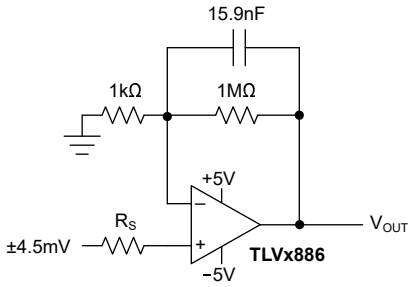


Figure 7-3. High Gain Pre-Amplifier

7.2.1.1 Design Requirements

Signal amplification is one of the fundamental functions of operational amplifiers. Amplification allows electronics to reliably interface with the outside world. Some analog signals require a specialized amplifier. Such cases are common when dealing with temperature, pressure, and biopotentials that can be millivolt or even microvolt level signals.

A very high gain is required to condition the signal for accurate digitization by an analog-to-digital converter. The circuit is very straightforward, but choosing the correct amplifier is crucial. The amplifier needs to have ultra-low input offset and input offset drift, high common-mode and power-supply rejection, and very low noise. Depending on the signal frequency of interest, a wide gain bandwidth is necessary to achieve the desired frequency response at the required gain.

Fortunately for designers, amplifiers with the aforementioned characteristics are readily available from Texas Instruments. The TLVx886 with high dc precision and low flicker noise is an excellent choice for applications requiring very high gain for low level signals.

Use the following parameters for this design example:

- Dual supply: ±5V
- Gain: 1001V/V
- Full-scale input: ±4.5mV

The following design details and equations can be used to reconfigure this design for different output voltage ranges and current loads.

7.2.1.2 Detailed Design Procedure

Designing an amplifier in a very high gain configuration requires some special considerations. Namely, designers must carefully consider the input referred dc errors and noise inherent to the amplifier. The gain of the circuit amplifies both the signal and errors of the amplifier. To achieve high resolution and precision measurements of low level signals, the amplifier must have ultra-low drift, and ultra-low noise.

Very high gain is necessary to properly scale a sensor producing a full-scale ±4.5mV signal for an analog-to-digital (ADC) input range of ±10V. Equation 12 details the procedure of selecting calculating the required gain. The output is set to ±4.5V to keep the amplifier in the linear operating output voltage range.

$$\text{Gain} = \frac{V_{OUT}}{V_{IN}} = \frac{4.5V - (-4.5V)}{4.5mV - (-4.5mV)} = 1000\frac{V}{V} \quad (12)$$

Any choice of R_F and R_I resistors can work, but consider the impact of noise on the system. The input referred noise of the configuration is given by the parallel combination of R_F and R_I as detailed in Equation 13.

$$e_{nr} = \sqrt{4KT\frac{R_F R_I}{R_F + R_I}} \quad (13)$$

When the gain is very large, R_F is much greater than R_I and input referred resistor noise is given by R_I. Naturally, setting R_I as small as possible provides the best noise performance. Note that the stability of the amplifier sets the limit on how small R_I is and thereby how large R_F is. In this application, setting R_I to 1kΩ provides a good trade-off.

Many process control and biopotential sensors produce a very small, almost dc level signal, typically <10Hz. To achieve the best noise performance possible, the bandwidth is limited with a 10Hz low pass filter set by C_F and R_R. At near dc levels, the flicker noise of the amplifier limits the noise performance of the circuit. The TLVx886 offers ultra-low flicker noise, typically about 300nV$_{PP}$. The total integrated output noise of the circuit is illustrated in Figure 7-4. The total integrated noise is a function of the resistor noise, and the inherent amplifier noise.

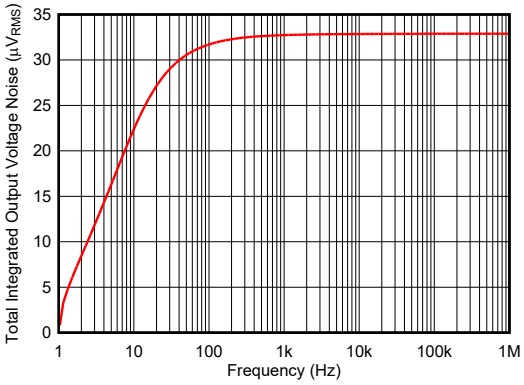


Figure 7-4. Total Integrated Output Voltage Noise

The dc precision is equally important and sets the accuracy of the circuit. While input offset voltage can be calibrated out, the input offset drift calibration is often too costly or too burdensome for some applications. The TLVx886 provides very low input offset voltage and input offset voltage drift. The percent error of the circuit can be calculated using Equation 14. The TLVx886 provides exceptionally high common-mode rejection and power supply rejection and therefore those terms are ignored for the purpose of this exercise.

$$\text{Error}_{dc} = \left(\frac{V_{os} + V_{os\_drift} + V_{os\_CMRR} + V_{os\_PSRR}}{V_{IN}}\right) \times 100 \quad (14)$$

Without room temperature calibration, the TLVx886 achieves less than 0.5% error and less than 0.1% error with room temperature calibration with a given operating temperature of 85°C. Keep in mind that the performance

shown here excludes the gain error and gain error drift that results from the resistors. To minimize the additional error use well matched, low drift resistors.

7.2.1.3 Application Curve

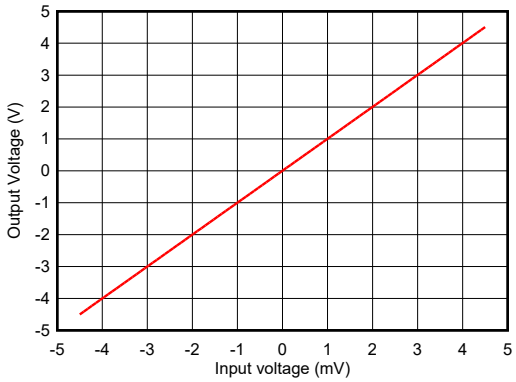


Figure 7-5. High Gain Amplifier Results

7.2.2 Difference Amplifier

Many applications require differential to single-ended conversions. Figure 7-6 shows the TLVx886 configured as a difference amplifier using the RES21A matched resistors. This circuit can be used for a variety of applications like current sensing, differential to single-ended conversions, and level shifting. The transfer function for this circuit is given by Equation 15.

$$V_{OUT} = (V_{IN+} - V_{IN-})\left(\frac{R_F}{R_I}\right) + V_{REF} \quad (15)$$

The TLVx886 along with the RES21A provide very high common-mode rejection, and offset drift performance over temperature. The RES21A is designed to maintain very tight matching of the resistor ratios and very low ratio drift providing an excellent choice for difference amplifier applications.

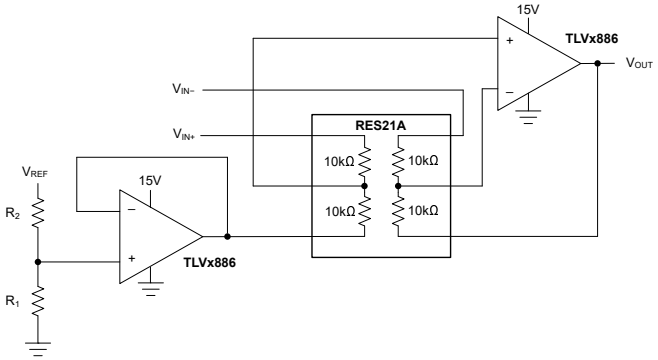


Figure 7-6. Difference Amplifier

To maintain proper operation, verify that Equation 16 and Equation 17 are satisfied to keep the input common-mode voltage within the linear operating region of the amplifier.

$$V_{IN}\left(\frac{R_2}{R_2 + R_1}\right) + V_{REF}\left(\frac{R_1}{R_2 + R_1}\right) \leq V_+ - 2V \quad (16)$$

$$V_{IN}\left(\frac{R_2}{R_2 + R_1}\right) + V_{REF}\left(\frac{R_1}{R_2 + R_1}\right) \geq V_- - 0.1V \quad (17)$$

7.2.3 Programmable Current Source

Figure 7-7 shows the basic configuration for a precision current source using the TLVx886. The circuit provides a configurable current source to a floating load. Figure 7-7 uses a digital-to-analog converter (DAC) to set the current level as per Equation 18. The additional components are placed for frequency compensation and stability, but can be omitted in some applications.

$$I_L = \frac{V_{IN}}{R_{SET}} \tag{18}$$

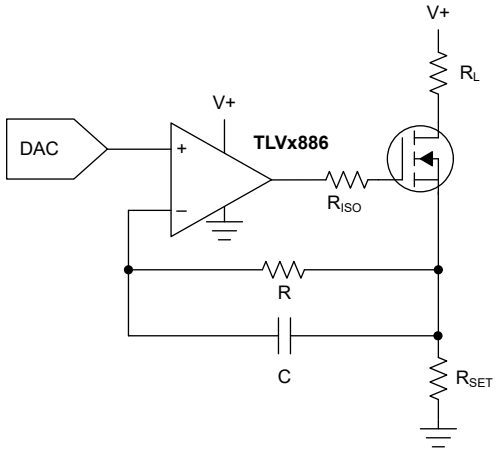


Figure 7-7. Programmable, Precision Current Source

7.2.4 Summing Amplifier

Figure 7-8 shows the TLVx886 configured as a summing amplifier. This circuit can be used to get a weighted sum of an N number of analog signals. Some applications require a weighted sum of multiple signals coming from different sensors. The low offset and drift performance of the TLVx886 enables the summation of very small signals with high gain. Depending on the choice of resistors, this circuit can provide the average of multiple analog signals. Note that the output of the circuit, as given by Equation 19 is inverted; set the power supplies accordingly.

$$V_{OUT} = -RF\left(\frac{V_{IN1}}{R1} + \frac{V_{IN2}}{R2} + \frac{V_{IN3}}{R3}\right) \tag{19}$$

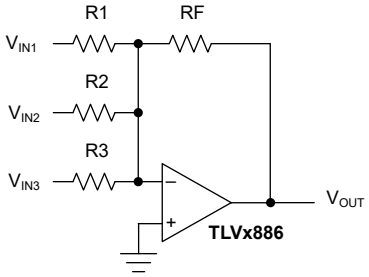


Figure 7-8. Summing Amplifier

7.3 Power Supply Recommendations

The TLVx886 are specified for operation from 4.5V to 36V (±2.25V to ±18V). The TLVx886 operates on both single and dual supplies. The TLVx886 do not require symmetrical supplies; the op amps only require a minimum voltage of 4.5V to operate.

CAUTION

Supply voltages larger than 40V can permanently damage the device (see the *Absolute Maximum Ratings* table).

Place 0.1µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see *Section 7.4*.

7.4 Layout

7.4.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices:

- For the lowest offset voltage, avoid temperature gradients that create thermoelectric (Seebeck) effects in the thermocouple junctions formed from connecting dissimilar conductors. Also:
  - Use low thermoelectric-coefficient conditions (avoid dissimilar metals).
  - Thermally isolate components from power supplies or other heat sources.
  - Shield operational amplifier and input circuitry from air currents, such as cooling fans.
- Noise can propagate into analog circuitry through the power pins of the op amp and the circuit as a whole. Bypass capacitors reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1µF ceramic bypass capacitors between each supply pin and ground, placed as close as possible to the device. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are typically devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Physically separate digital and analog grounds paying attention to the flow of the ground current. For more detailed information, see the *The PCB is a component of op amp design* analog application journal.
- To reduce parasitic coupling, run the input traces as far away as possible from the supply or output traces. If these traces cannot be separated, cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close as possible to the device. As Figure 7-10 shows, keep the feedback resistor (R3) and gain resistor (R4) close to the inverting input to minimize parasitic capacitance.
- Keep the length of input traces as short as possible. Short traces to the inverting input help to minimize parasitic capacitance on the inverting input. Always remember that the input traces are the most sensitive part of the circuit.
- For best performance, clean the PCB following board assembly.
- Any precision integrated circuit can experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, bake the PCB assembly to remove moisture introduced into the device packaging during the cleaning process. A low-temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

7.4.2 Layout Example

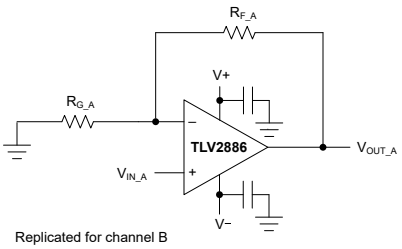


Figure 7-9. Schematic Representation

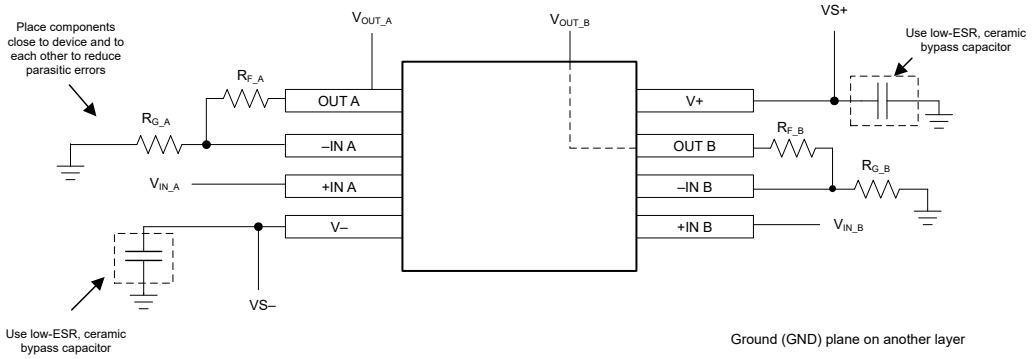


Figure 7-10. Operational Amplifier Board Layout for Noninverting Amplifier Configuration

8 Device and Documentation Support

8.1 Device Support

8.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

8.1.2 Development Support

8.1.2.1 PSpice® for TI

PSpice® for TI is a design and simulation environment that helps evaluate performance of analog circuits. Create subsystem designs and prototype designs before committing to layout and fabrication, reducing development cost and time to market.

8.1.2.2 TINA-TI™ Simulation Software (Free Download)

TINA-TI™ simulation software is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI simulation software is a free, fully-functional version of the TINA™ software, preloaded with a library of macromodels, in addition to a range of both passive and active models. TINA-TI simulation software provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Design and simulation tools web page, TINA-TI simulation software offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

Note

These files require that either the TINA software or TINA-TI software be installed. Download the free TINA-TI simulation software from the TINA-TI™ software folder.

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Zero-drift Amplifiers: Features and Benefits* application brief
- Texas Instruments, *The PCB is a component of op amp design* application note
- Texas Instruments, *Operational amplifier gain stability, Part 3: AC gain-error analysis*
- Texas Instruments, *Operational amplifier gain stability, Part 2: DC gain-error analysis*
- Texas Instruments, *Using infinite-gain, MFB filter topology in fully differential active filters* application note
- Texas Instruments, *Op Amp Performance Analysis*
- Texas Instruments, *Single-Supply Operation of Operational Amplifiers* application note
- Texas Instruments, *Shelf-Life Evaluation of Lead-Free Component Finishes* application note
- Texas Instruments, *Feedback Plots Define Op Amp AC Performance* application note
- Texas Instruments, *EMI Rejection Ratio of Operational Amplifiers* application note
- Texas Instruments, *Analog Linearization of Resistance Temperature Detectors* application note
- Texas Instruments, *TI Precision Design TIPD102 High-Side Voltage-to-Current (V-I) Converter*

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.5 Trademarks

TINA-TI™ and TI E2E™ are trademarks of Texas Instruments.
TINA™ is a trademark of DesignSoft, Inc.
PSpice® is a registered trademark of Cadence Design Systems, Inc.
All trademarks are the property of their respective owners.

8.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (February 2026) to Revision B (May 2026)	Page
• Changed TLV2886DGK from Preview to Production Data	1
• Updated *Absolute Maximum Ratings* for clarity	5

Changes from Revision * (February 2026) to Revision A (February 2026)	Page
• Updated *Features*, *Feature Description*, *Thermal Information*, *Electrical Characteristics*, *ESD Ratings* and *Typical Characteristics* to the production data specifications	1
• Updated data sheet status from *Advanced Information* to *Production Data*	1
• Changed TLV2886D from Preview to Production Data	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PTLV886DBVR	Active	Preproduction	SOT-23 (DBV) | 5	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
TLV2886DGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T286
TLV2886DR	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL2886

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

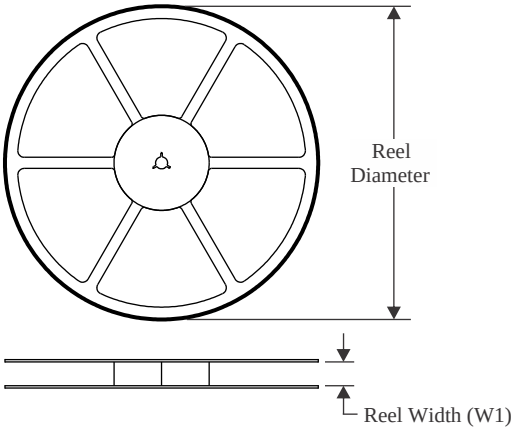
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

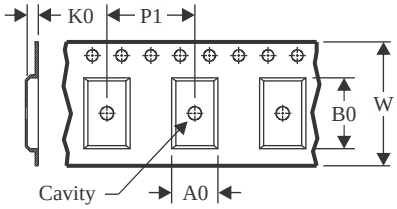
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

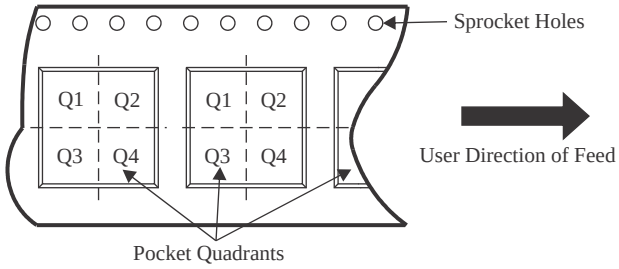


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

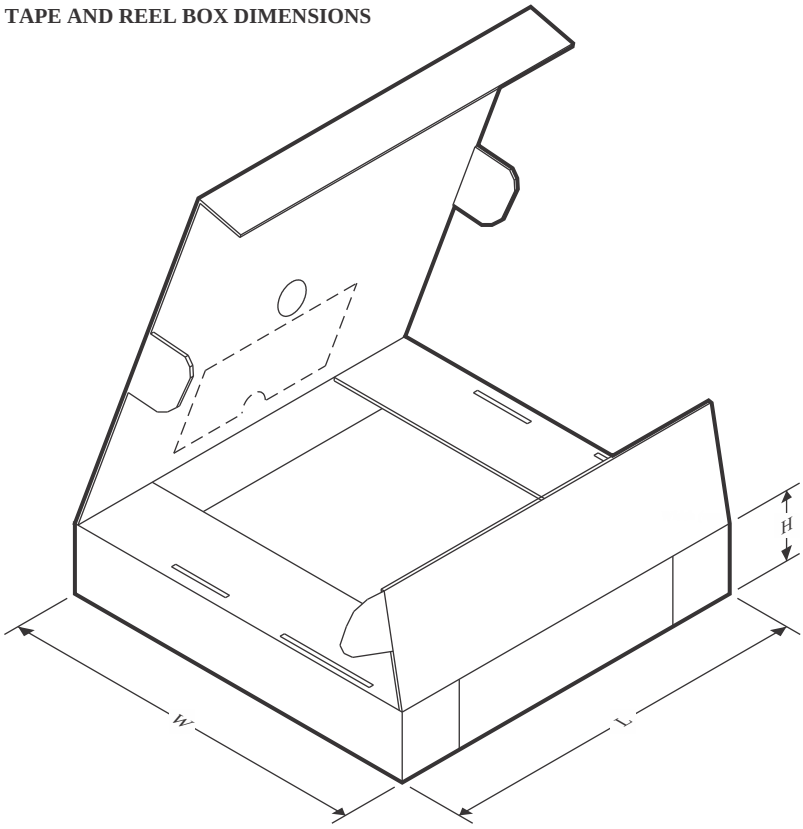
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

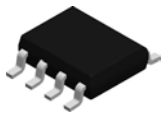
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV2886DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV2886DGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0

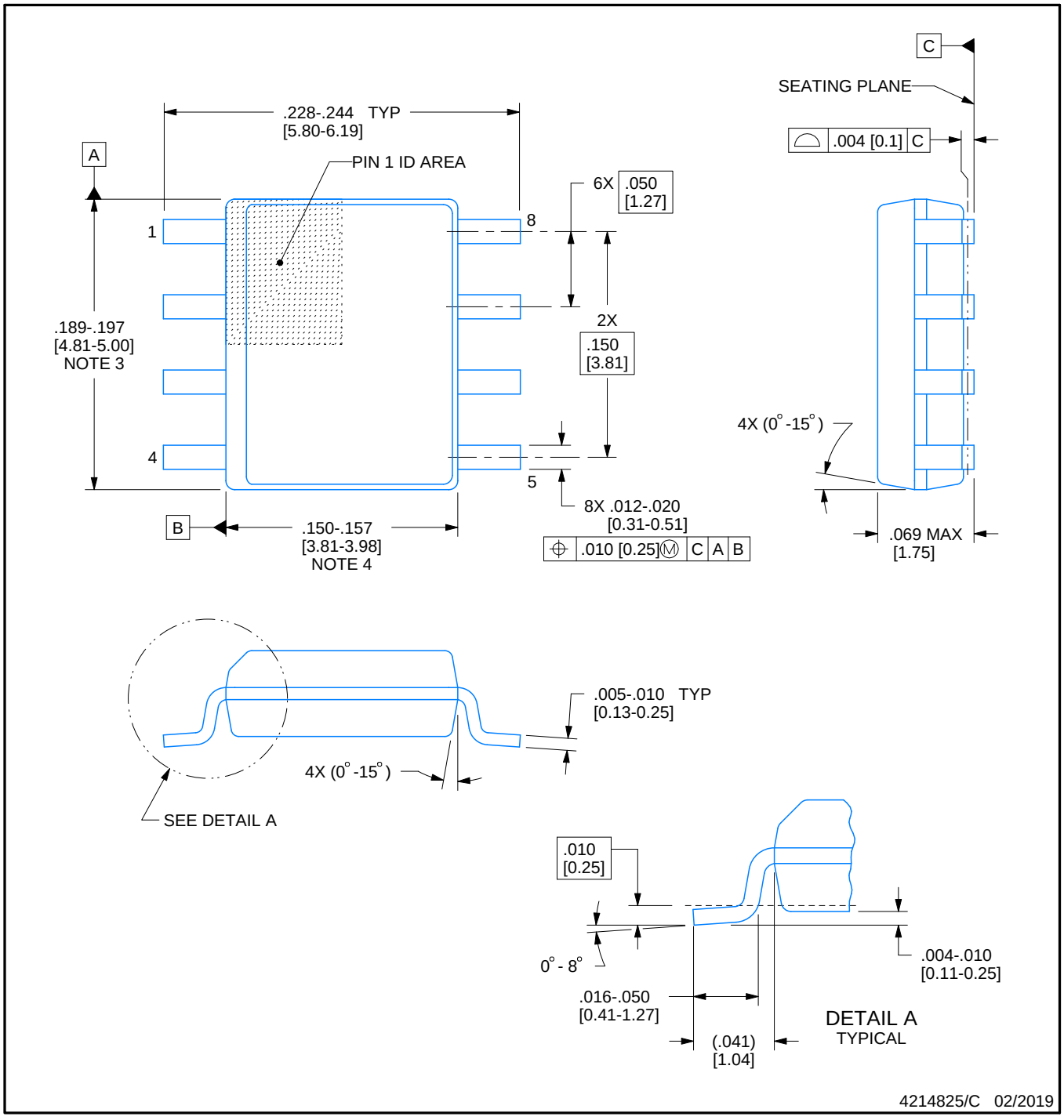


PACKAGE OUTLINE

D0008A

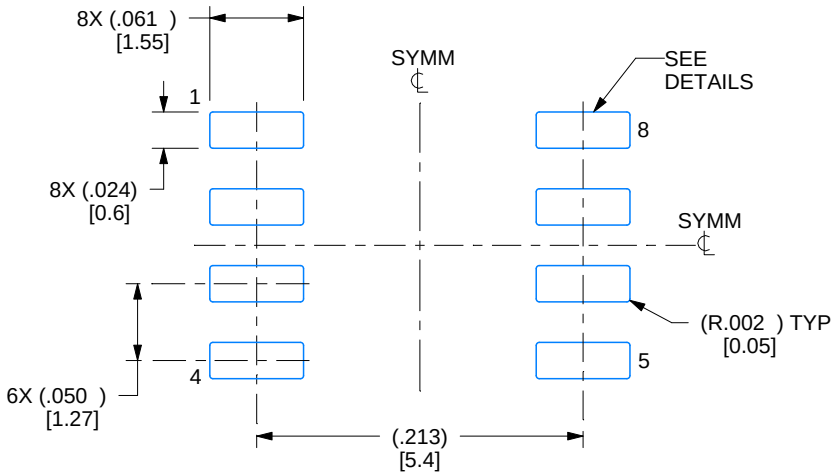
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

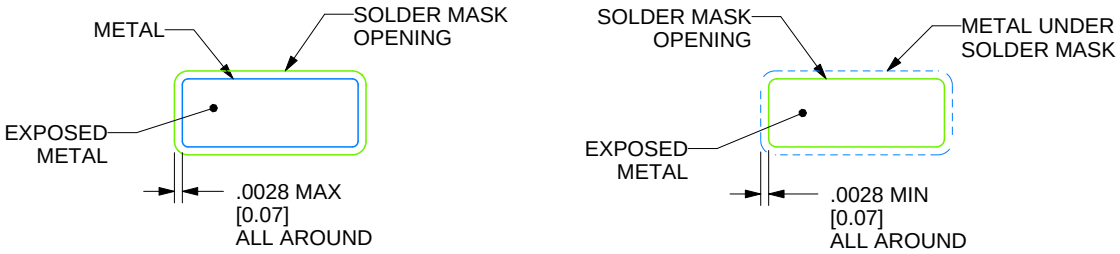


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

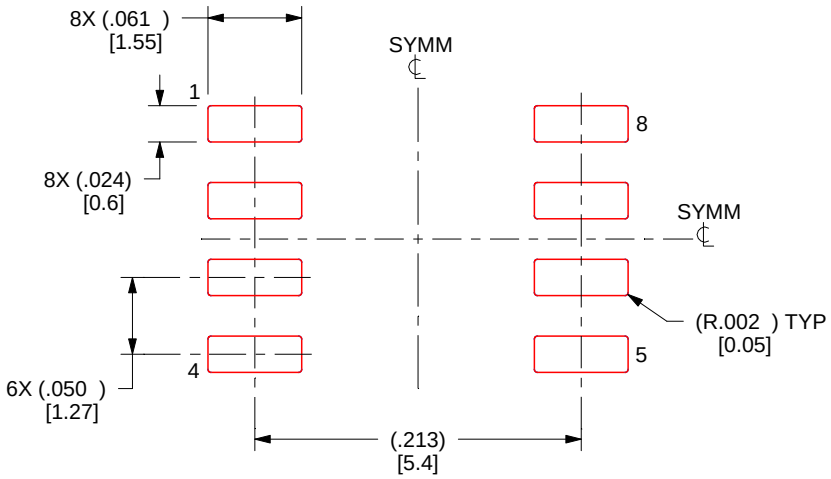
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

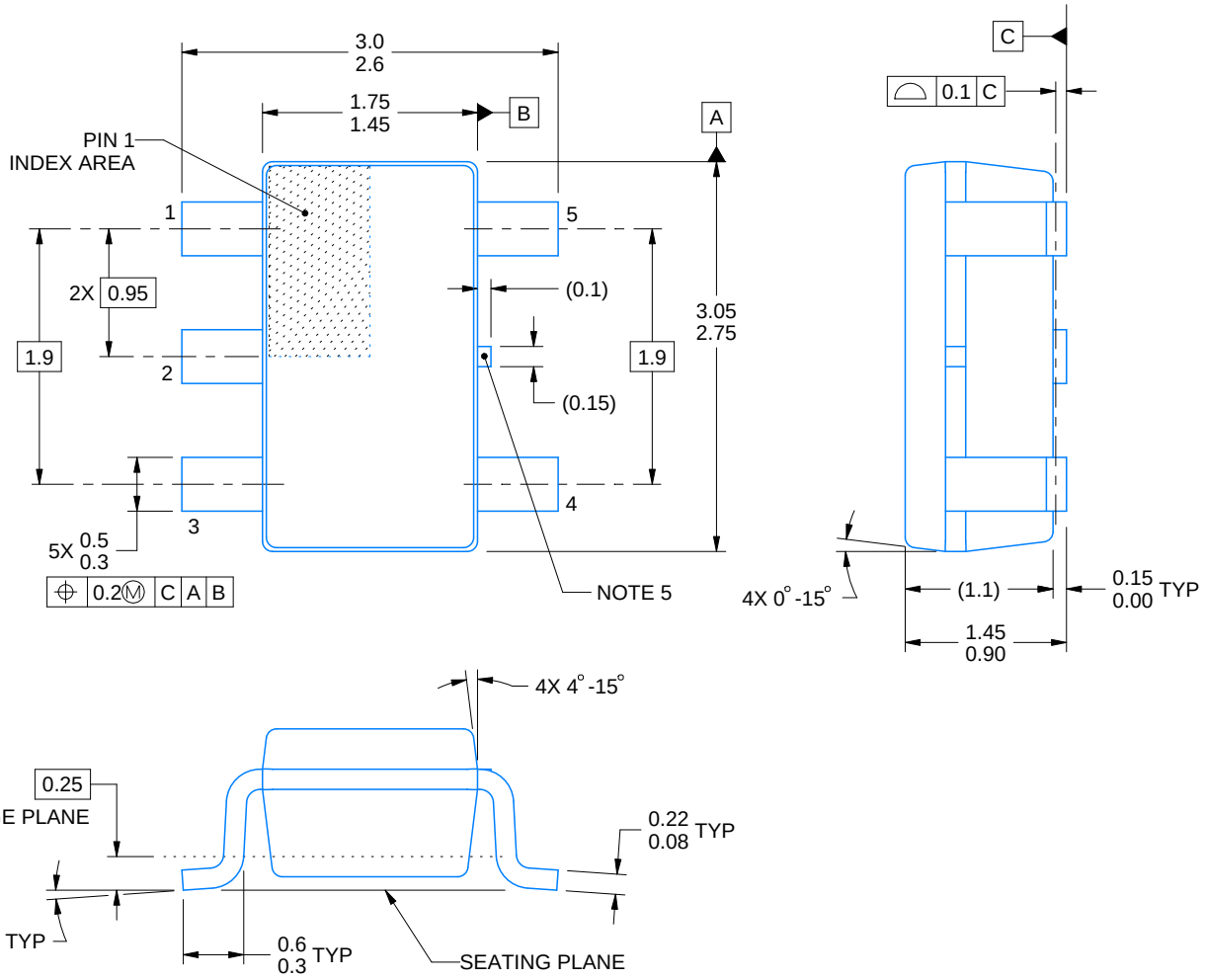
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

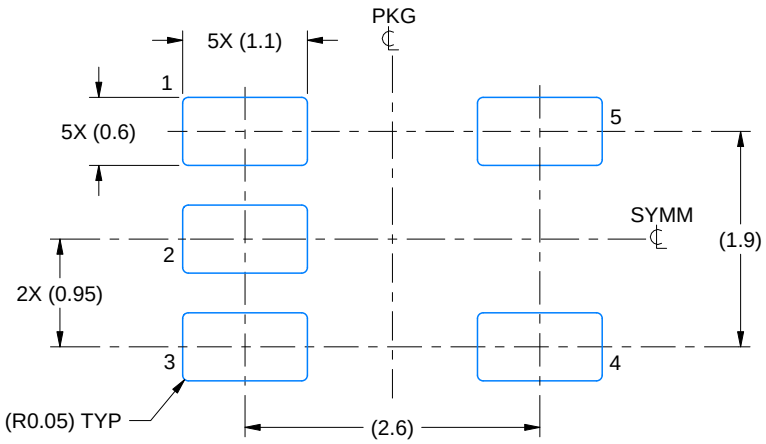
SMALL OUTLINE TRANSISTOR



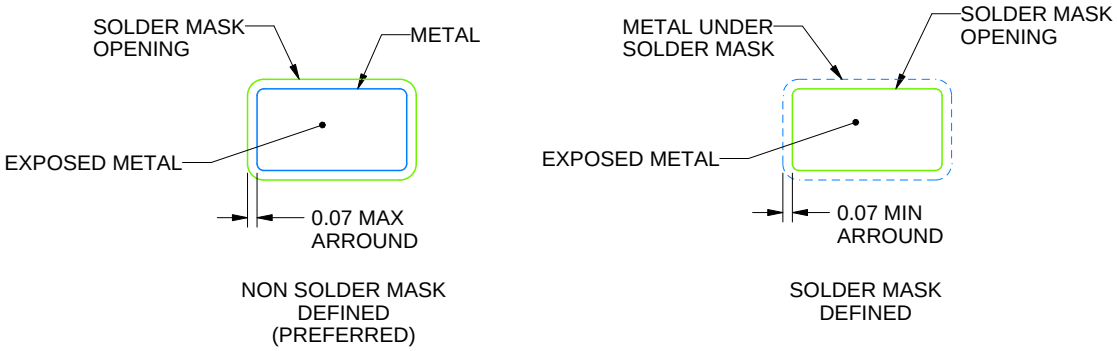
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

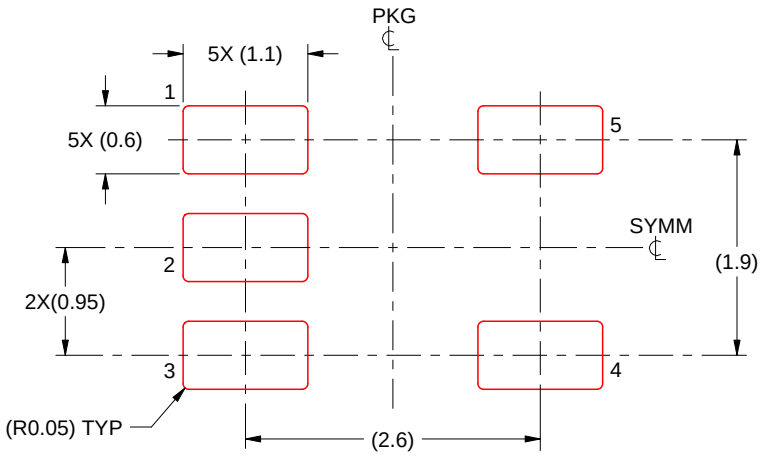


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

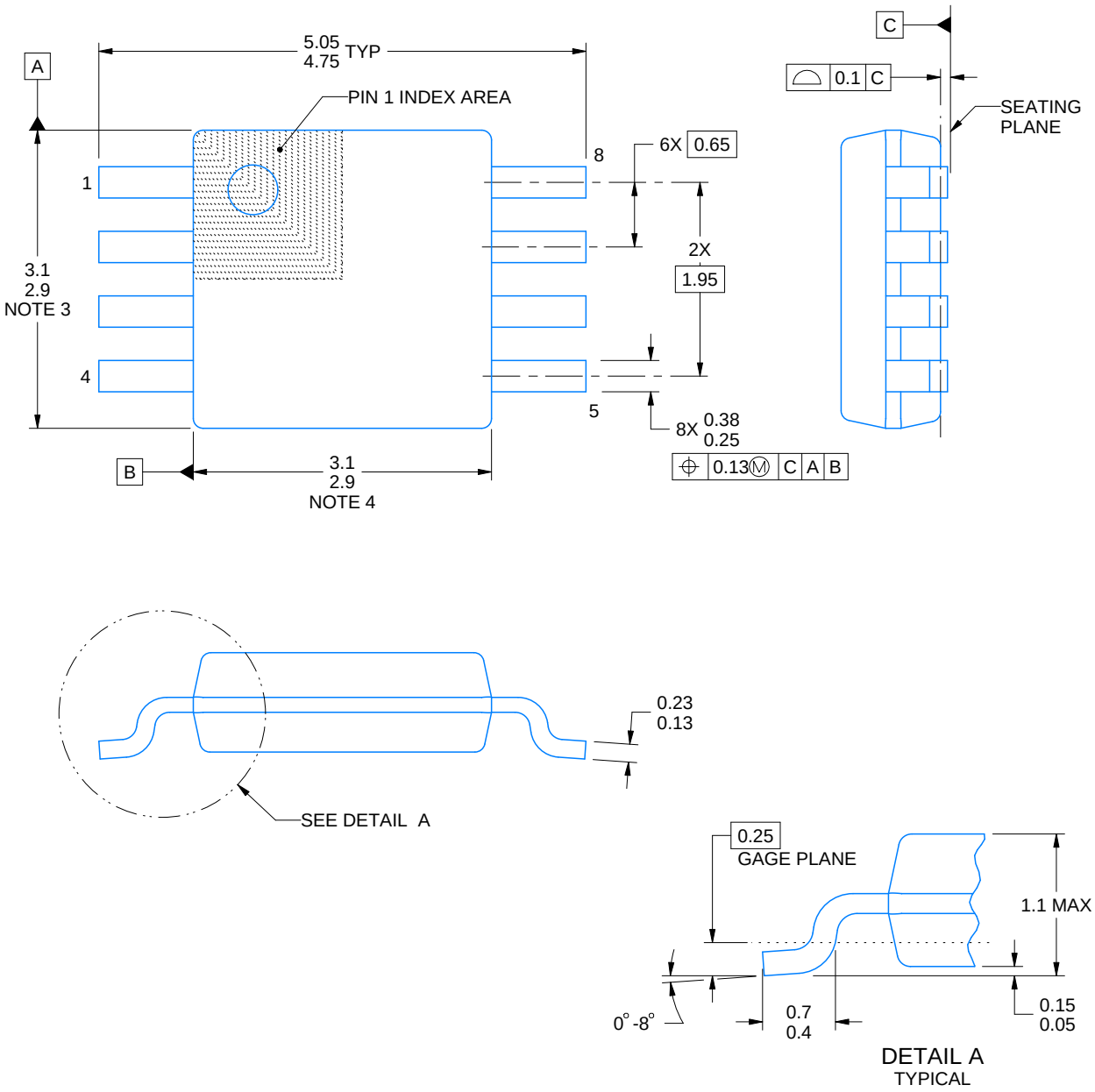
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

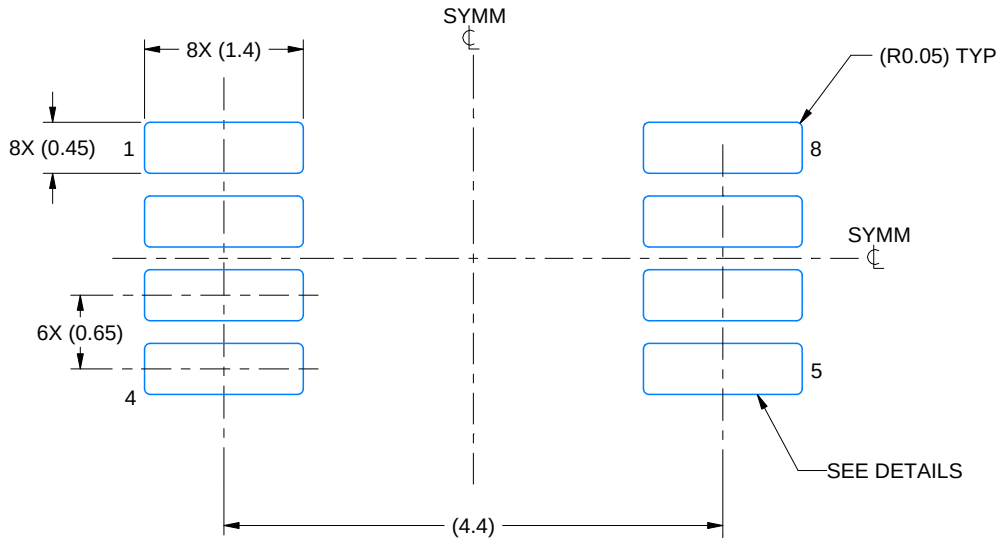
SMALL OUTLINE PACKAGE



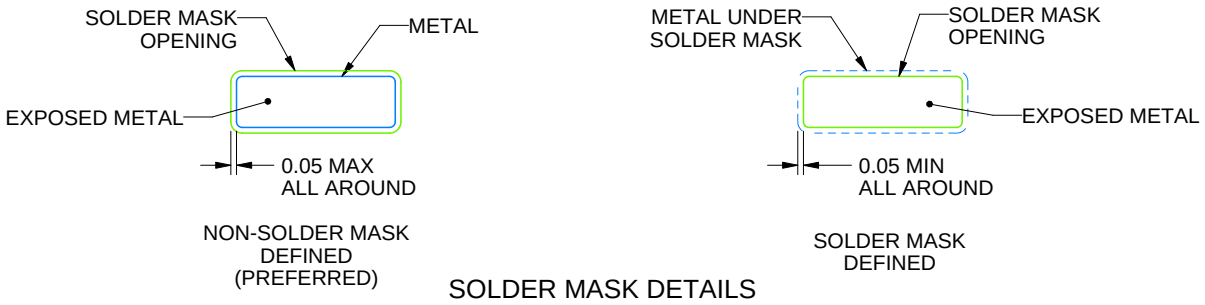
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

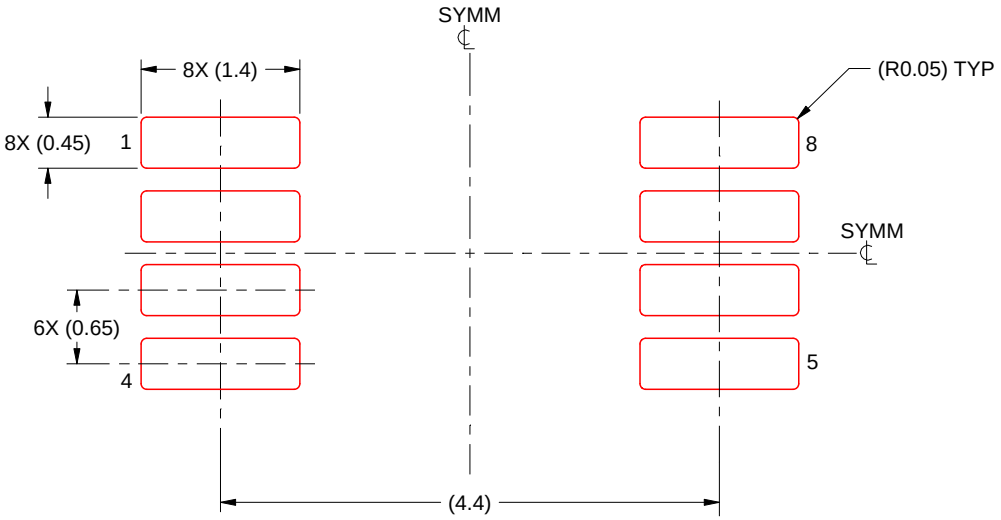


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Last updated 10/2025