

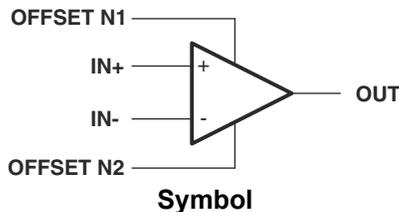
TLE2141-Q1 Excalibur™ Low-Noise High-Speed Precision Operational Amplifiers

1 Features

- Qualified for automotive applications
- Low noise:
 - 10Hz ... $15\text{nV}/\sqrt{\text{Hz}}$
 - 1kHz ... $10.5\text{nV}/\sqrt{\text{Hz}}$
- Load capability: 10000pF
- Short-circuit output current: 20mA (minimum)
- Slew rate: 27V/ μs (minimum)
- High gain-bandwidth product: 5.9MHz
- Low V_{IO} : 500 μV (maximum) at 25°C
- Single or split supply: 4V to 44V
- Fast settling time
 - 340ns to 0.1%
 - 400ns to 0.01%
- Saturation recovery: 150ns
- Large output swing:
 - $V_{CC-} + 0.1\text{V}$ to $V_{CC+} - 1\text{V}$

2 Applications

- [Traction inverter](#)
- [Onboard charger](#)
- [Automatic transmission](#)
- [DC/DC converter](#)



3 Description

The TLE2141-Q1 device is a high-performance, internally compensated operational amplifier built using the Texas Instruments complementary bipolar Excalibur™ process. It is a pin-compatible upgrade to standard industry products.

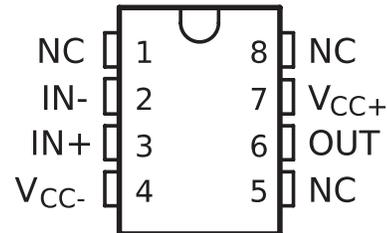
The design incorporates an input stage that simultaneously achieves low audio-band noise of $10.5\text{nV}/\sqrt{\text{Hz}}$ with a 10Hz 1/f corner and symmetrical 40V/ μs slew rate typically with loads up to 800pF. The resulting low distortion and high power bandwidth are important in high-fidelity audio applications. A fast settling time of 430ns to 0.1% of a 10V step with a 2k Ω /100pF load is useful in fast actuator/positioning drivers. Under similar test conditions, settling time to 0.01% is 640ns.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾
TLE2141-Q1	D (SOIC, 8)	4.9mm × 6mm

- (1) For all available packages, see [Section 9](#).
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.

D PACKAGE (TOP VIEW)



NC - No internal connection
Pinout



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4 Ordering Information

T _A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	SOIC – D (8 pin)	Reel of 2500	TLE2141QDRQ1	2141Q

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

		VALUE	UNIT
V _{CC+}	Supply voltage ⁽²⁾	22	V
V _{CC-}	Supply voltage	-22	V
V _{ID}	Differential input voltage ⁽³⁾	±44	V
V _I	Input voltage range (any input)	V _{CC+} to (V _{CC-} - 0.3)	V
I _I	Input current (each input)	±1	mA
I _O	Output current	±80	mA
	Total current into V _{CC+}	80	mA
	Total current out of V _{CC-}	80	mA
	Duration of short-circuit current at (or below) 25°C ⁽⁴⁾	Unlimited	
θ _{JA}	Package thermal impedance ^{(5) (6)}	D package (8 pin)	97.1 °C/W
T _A	Operating free-air temperature range	-40 to 125	°C
T _{stg}	Storage temperature range	-65 to 150	°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260	°C

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
- (3) Differential voltages are at IN+ with respect to IN-. Excessive current flows, if input, are brought below V_{CC-} - 0.3 V.
- (4) The output can be shorted to either supply. Temperature and/or supply voltages must be limited to make sure that the maximum dissipation rating is not exceeded.
- (5) Maximum power dissipation is a function of T_{J(max)}, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is P_D = (T_{J(max)} - T_A)/θ_{JA}. Operating at the absolute maximum T_J of 150°C can affect reliability.
- (6) The package thermal impedance is calculated in accordance with JESD 51-7.

5.2 Recommended Operating Conditions

		MIN	MAX	UNIT	
V _{CC±}	Supply voltage	±2	±22	V	
V _{IC}	Common-mode input voltage	V _{CC} = 5V	0	2.7	V
		V _{CC±} = ±15V	-15	12.7	
T _A	Operating free-air temperature	-40	125	°C	

5.3 Electrical Characteristics

$V_{CC} = 5V$, at specified free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A ⁽¹⁾	MIN	TYP	MAX	UNIT	
V_{IO}	Input offset voltage	$V_O = 2.5V, R_S = 50\Omega, V_{IC} = 2.5V$	25°C		225	1400	μV	
			Full range			2100		
α_{VIO}	Temperature coefficient of input offset voltage	$V_O = 2.5V, R_S = 50\Omega, V_{IC} = 2.5V$	Full range		1.7		$\mu V/^\circ C$	
I_{IO}	Input offset current	$V_O = 2.5V, R_S = 50\Omega, V_{IC} = 2.5V$	25°C		8	100	nA	
			Full range			250		
I_{IB}	Input bias current	$V_O = 2.5V, R_S = 50\Omega, V_{IC} = 2.5V$	25°C		-0.8	-2	μA	
			Full range			-2.3		
V_{ICR}	Common-mode input voltage range	$R_S = 50\Omega$	25°C	0 to 3	-0.3 to 3.2		V	
			Full range	0 to 2.7	-0.3 to 2.9			
V_{OH}	High-level output voltage		25°C	$I_{OH} = -150\mu A$	3.9	4.1	V	
				$I_{OH} = -1.5mA$	3.8	4		
				$I_{OH} = -15mA$	3.2	3.7		
			Full range	$I_{OH} = -100\mu A$	3.75			
				$I_{OH} = -1mA$	3.65			
				$I_{OH} = -10mA$	3.25			
V_{OL}	Low-level output voltage		25°C	$I_{OL} = 150\mu A$		75	125	mV
				$I_{OL} = 1.5mA$		150	225	V
				$I_{OL} = 15mA$		1.2	1.4	V
			Full range	$I_{OL} = 100\mu A$			200	mV
				$I_{OL} = 1mA$			250	mV
				$I_{OL} = 10mA$			1.25	V
A_{VD}	Large-signal differential voltage amplification	$V_{IC} = \pm 2.5V, R_L = 2k\Omega, V_O = 1V \text{ to } 1.5V$	25°C	50	220		V/mV	
			Full range	5				
r_i	Input resistance		25°C		70		M Ω	
c_i	Input capacitance		25°C		2.5		pF	
Z_o	Open-loop output impedance	$f = 1MHz$	25°C		30		Ω	
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}(\text{min}), R_S = 50\Omega$	25°C	85	118		dB	
			Full range	80				
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm} = \pm 2.5V \text{ to } \pm 15V, R_S = 50\Omega$	25°C	90	106		dB	
			Full range	85				
I_{CC}	Supply current	$V_O = 2.5V, \text{ No load}, V_{IC} = 2.5V$	25°C		3.4	4.4	mA	
			Full range			4.6		

(1) Full range is $-40^\circ C$ to $125^\circ C$.

5.4 Operating Characteristics

$V_{CC} = 5V$, $T_A = 25^\circ C$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR+	Positive slew rate	$A_{VD} = -1$, $R_L = 2k\Omega^{(1)}$, $C_L = 500\text{ pF}$		45		V/ μ s
SR-	Negative slew rate	$A_{VD} = -1$, $R_L = 2k\Omega^{(1)}$, $C_L = 500\text{ pF}$		42		V/ μ s
t_s	Settling time	$A_{VD} = -1$, 2.5V step	To 0.1%	0.66		μ s
			To 0.01%	0.99		
V_n	Equivalent input noise voltage	$R_S = 20\Omega$	f = 10Hz	15		nV/ $\sqrt{\text{Hz}}$
			f = 1kHz	10.5		
$V_{n(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1Hz to 1Hz		0.48		μ V
		f = 0.1Hz to 10Hz		0.51		
I_n	Equivalent input noise current	f = 10Hz		1.92		pA/ $\sqrt{\text{Hz}}$
		f = 1kHz		0.5		
THD+N	Total harmonic distortion plus noise	$V_O = 1V$ to $3V$, $R_L = 2k\Omega^{(1)}$, $A_{VD} = 2$, f = 10 kHz		0.0052		%
B_1	Unity-gain bandwidth	$R_L = 2k\Omega^{(1)}$, $C_L = 100\text{ pF}^{(1)}$		5.9		MHz
	Gain-bandwidth product	$R_L = 2k\Omega^{(1)}$, $C_L = 100\text{ pF}^{(1)}$, f = 100 kHz		5.8		MHz
BOM	Maximum output-swing bandwidth ⁽²⁾	$V_{O(PP)} = 2V$, $R_L = 2k\Omega^{(1)}$, $A_{VD} = 1$		380		kHz
ϕ_m	Phase margin at unity gain	$R_L = 2k\Omega^{(1)}$, $C_L = 100\text{ pF}^{(1)}$		57		$^\circ$

(1) R_L and C_L terminated to 2.5V.

(2) Measured at -0.1dB.

5.5 Electrical Characteristics

$V_{CC} = \pm 15V$, at specified free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A (1)	MIN	TYP	MAX	UNIT	
V_{IO}	Input offset voltage	$V_{IC} = 0, R_S = 50\Omega$	25°C		200	900	μV	
			Full range			1700		
α_{VIO}	Temperature coefficient of input offset voltage	$V_{IC} = 0, R_S = 50\Omega$	Full range		1.7		$\mu V/^\circ C$	
I_{IO}	Input offset current	$V_{IC} = 0, R_S = 50\Omega$	25°C		7	100	nA	
			Full range			250		
I_{IB}	Input bias current	$V_{IC} = 0, R_S = 50\Omega$	25°C		-0.7	-1.5	μA	
			Full range			-1.8		
V_{ICR}	Common-mode input voltage range	$R_S = 50\Omega$	25°C	-15 to 13	-15.3 to 13.2		V	
			Full range		-15 to 12.7	-15.3 to 12.9		
V_{OM+}	Maximum positive peak output voltage swing		25°C		$I_O = -150\mu A$	13.8	14.1	V
					$I_O = -1.5mA$	13.7	14	
					$I_O = -15mA$	13.1	13.7	
			Full range		$I_O = -100\mu A$	13.7		
					$I_O = -1mA$	13.6		
					$I_O = -10mA$	13.1		
V_{OM-}	Maximum negative peak output voltage swing		25°C		$I_O = 150\mu A$	-14.7	-14.9	V
					$I_O = 1.5mA$	-14.5	-14.8	
					$I_O = 15mA$	-13.4	-13.8	
			Full range		$I_O = 100\mu A$	-14.6		
					$I_O = 1mA$	-14.5		
					$I_O = 10mA$	-13.4		
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 10V, R_L = 2k\Omega$	25°C	100	450		V/mV	
			Full range		20			
r_i	Input resistance		25°C		65		M Ω	
c_i	Input capacitance		25°C		2.5		pF	
Z_o	Open-loop output impedance	$f = 1MHz$	25°C		30		Ω	
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}(min), R_S = 50\Omega$	25°C	85	108		dB	
			Full range		80			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm} = \pm 2.5V$ to $\pm 15V, R_S = 50\Omega$	25°C	90	106		dB	
			Full range		85			
I_{OS}	Short-circuit output current	$V_O = 0$	25°C	$V_{ID} = 1V$	-25	-50	mA	
				$V_{ID} = -1V$	20	31		
I_{CC}	Supply current	$V_O = 0, \text{No load}, V_{IC} = 2.5V$	25°C		3.5	4.5	mA	
			Full range			4.7		

(1) Full range is $-40^\circ C$ to $125^\circ C$.

5.6 Operating Characteristics

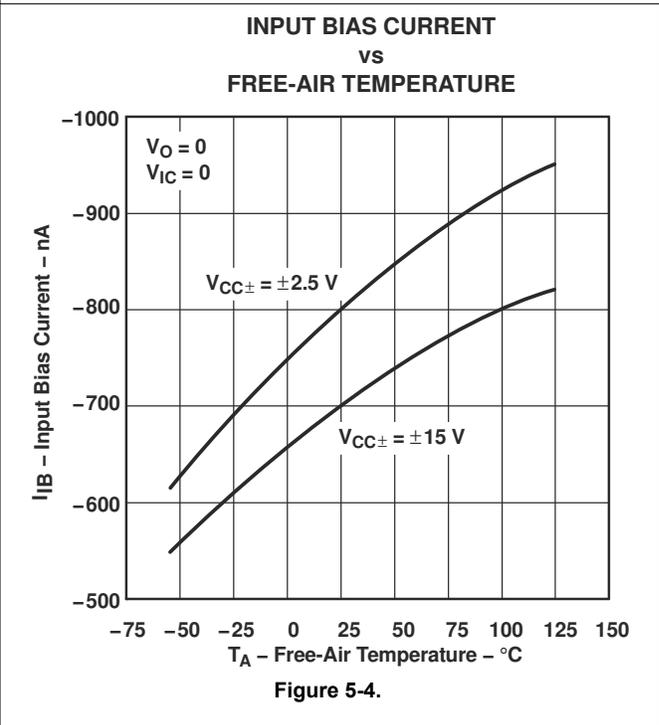
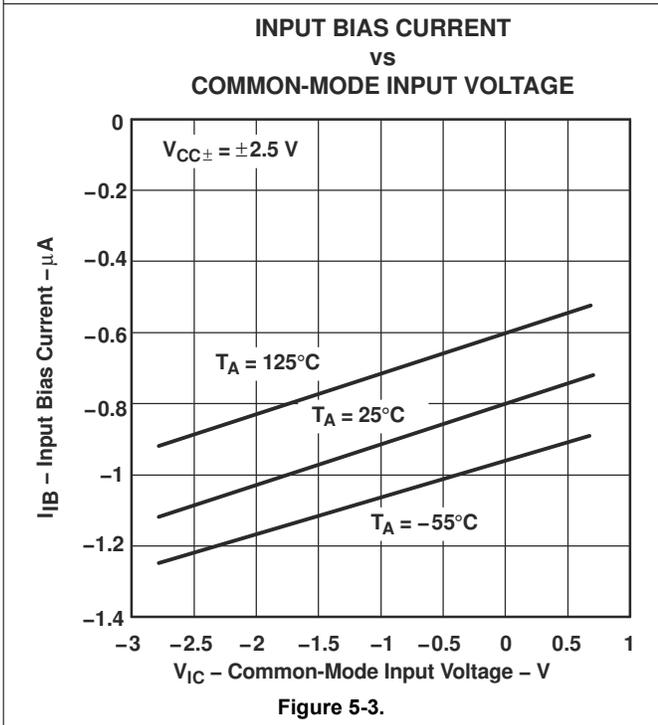
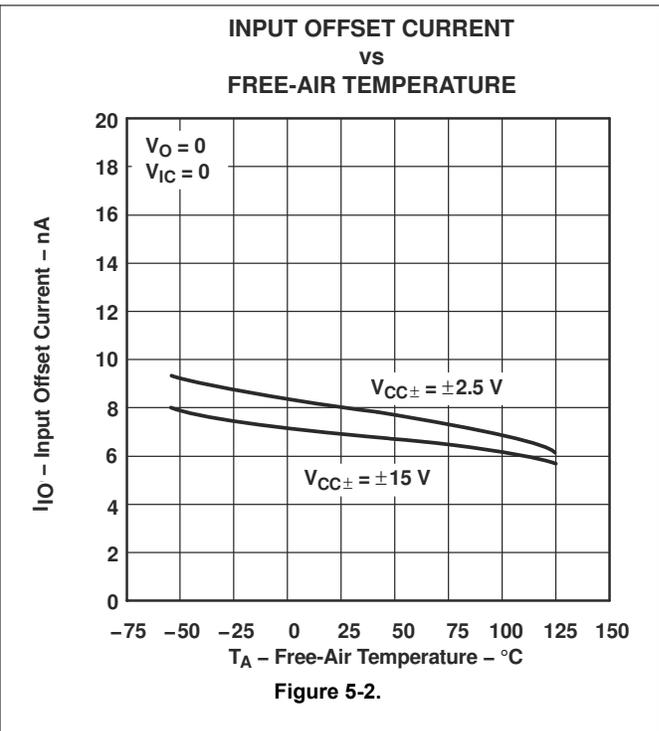
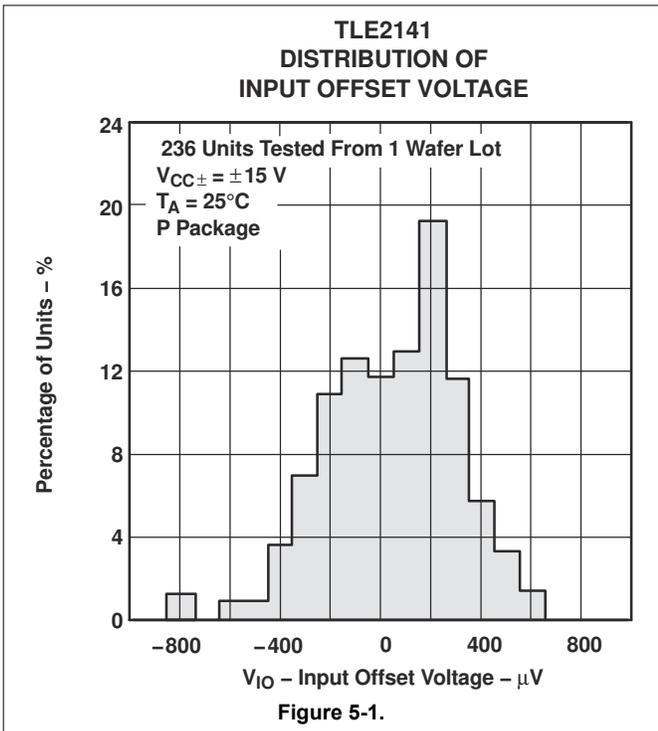
$V_{CC} = \pm 15V$, $T_A = 25^\circ C$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR+	Positive slew rate	$A_{VD} = -1$, $R_L = 2k\Omega$, $C_L = 100$ pF	27 ⁽¹⁾	45		V/ μ s
SR-	Negative slew rate	$A_{VD} = -1$, $R_L = 2k\Omega$, $C_L = 100$ pF	27 ⁽¹⁾	42		V/ μ s
t_s	Settling time	$A_{VD} = -1$, 10V step	To 0.1%	0.43		μ s
			To 0.01%	0.64		
V_n	Equivalent input noise voltage	$R_S = 20\Omega$	f = 10Hz	15		nV/ \sqrt{Hz}
			f = 1kHz	10.5		
$V_{n(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1Hz to 1Hz		0.48		μ V
		f = 0.1Hz to 10Hz		0.51		
I_n	Equivalent input noise current	f = 10Hz		1.89		pA/ \sqrt{Hz}
		f = 1kHz		0.47		
THD+N	Total harmonic distortion plus noise	$V_{O(PP)} = 20V$, $R_L = 2k\Omega$, $A_{VD} = 10$, f = 10 kHz		0.06		%
B_1	Unity-gain bandwidth	$R_L = 2k\Omega$, $C_L = 100$ pF		6		MHz
	Gain-bandwidth product	$R_L = 2k\Omega$, $C_L = 100$ pF, f = 100 kHz		5.9		MHz
BOM	Maximum output-swing bandwidth ⁽²⁾	$V_{O(PP)} = 20V$, $A_{VD} = 1$, $R_L = 2$ k Ω , $C_L = 100$ pF		668		kHz
ϕ_m	Phase margin at unity gain	$R_L = 2k\Omega$, $C_L = 100$ pF		58		$^\circ$

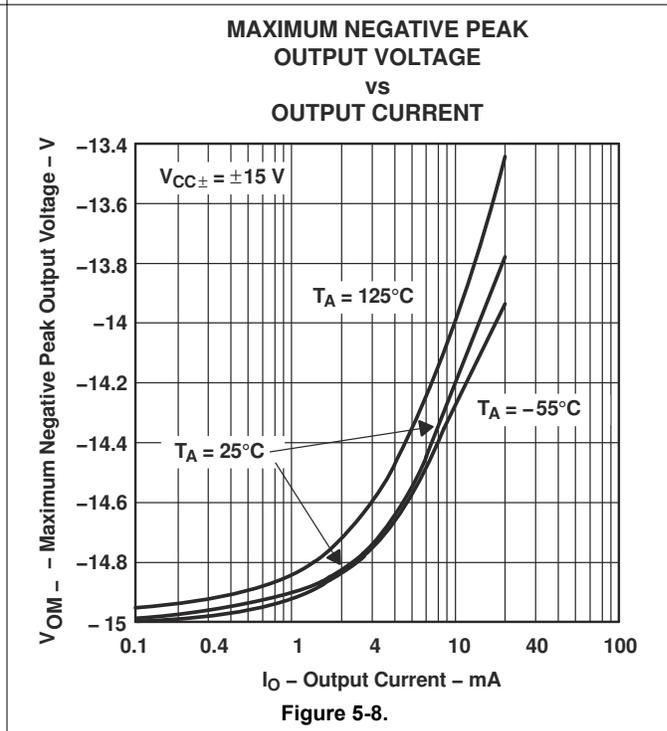
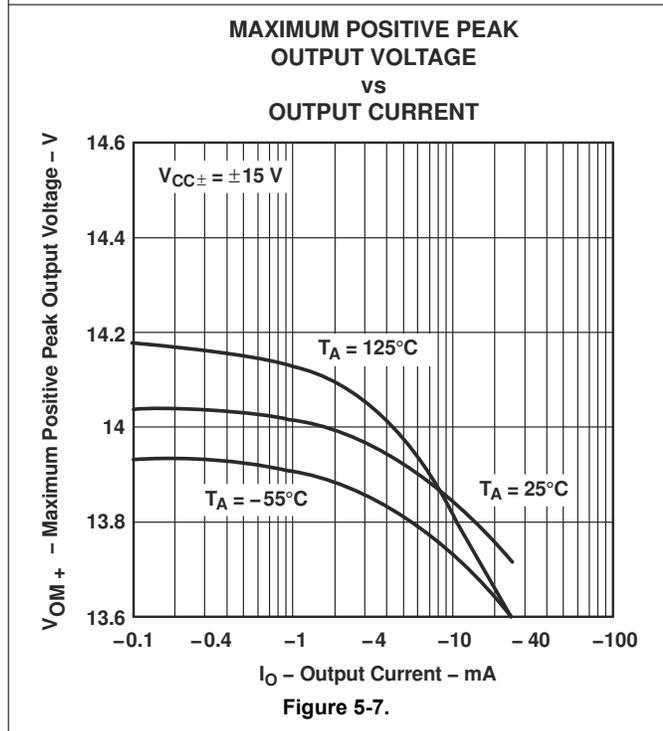
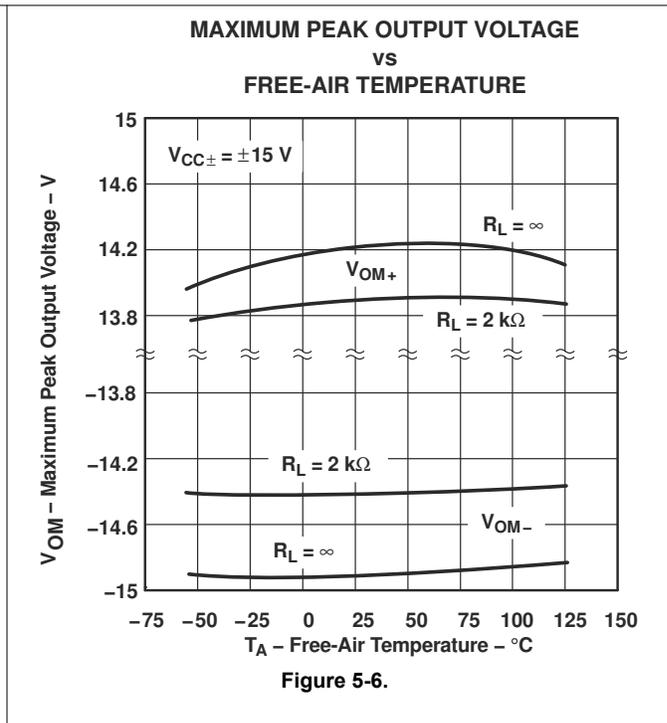
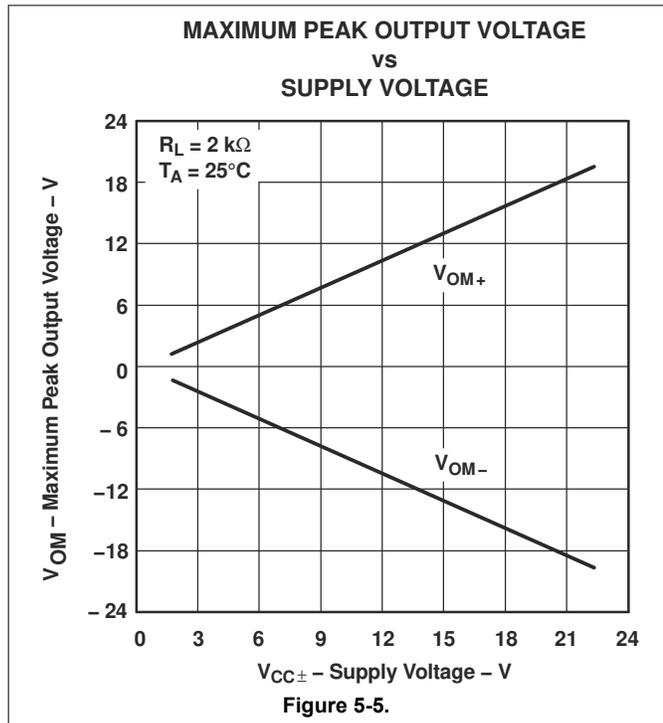
(1) Specified by characterization.

(2) Measured at -0.1dB.

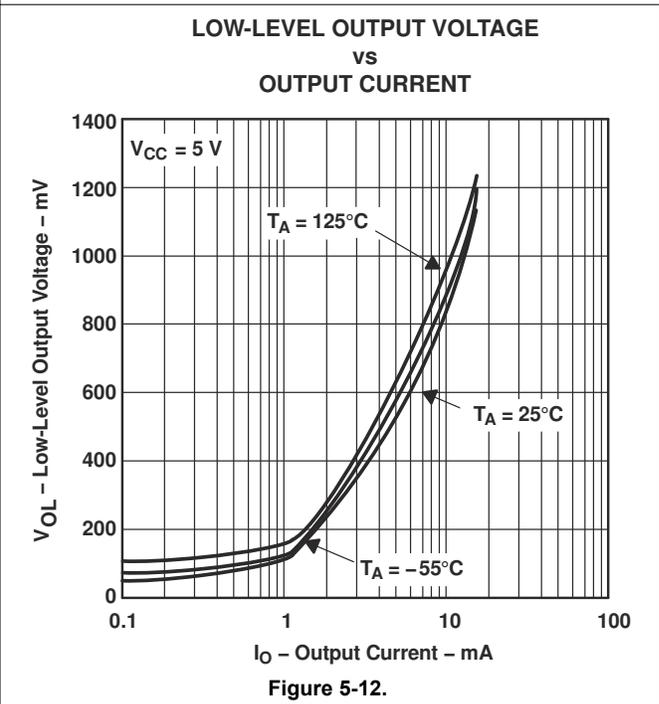
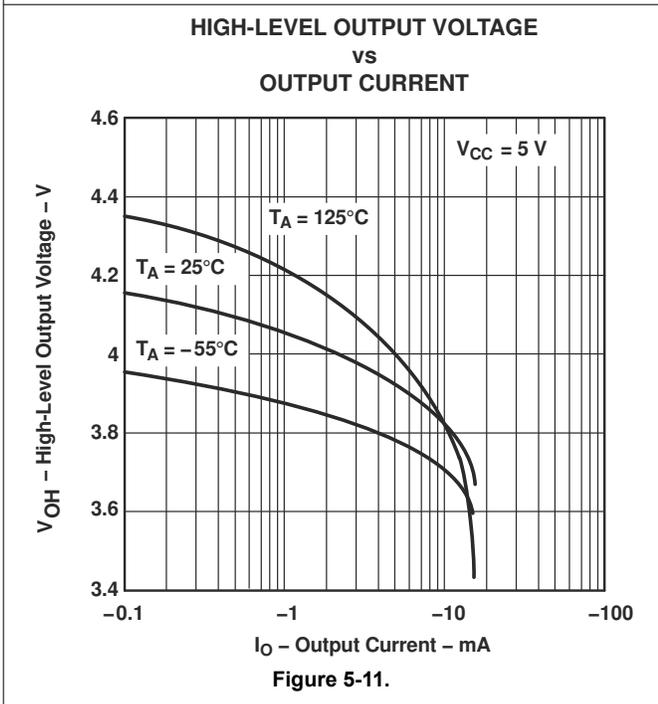
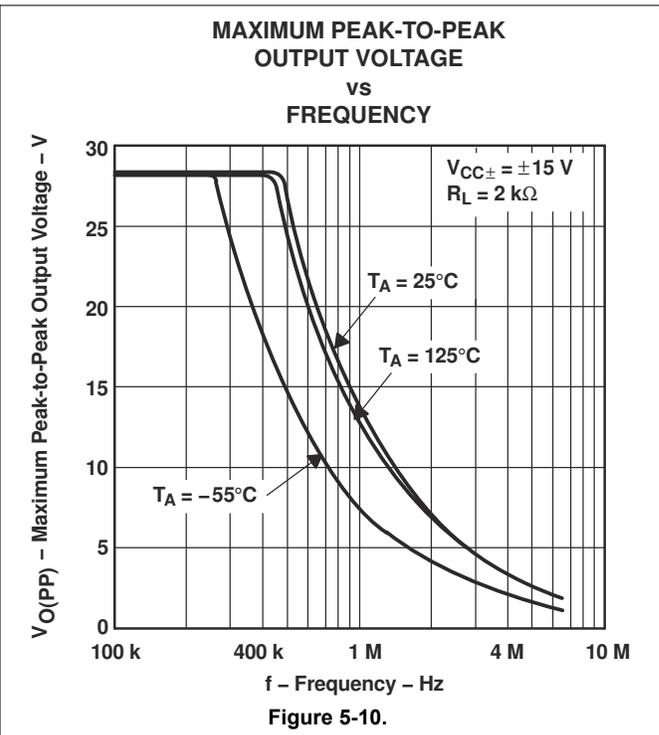
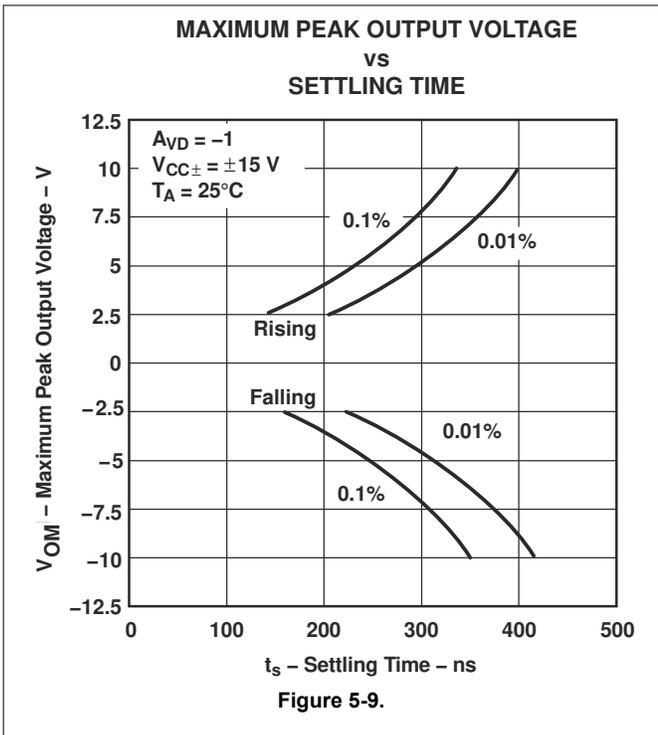
5.7 Typical Characteristics



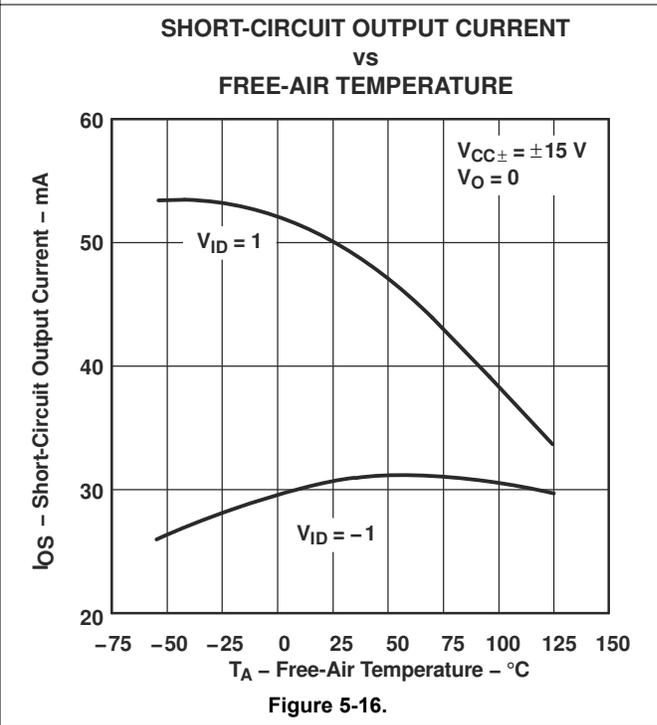
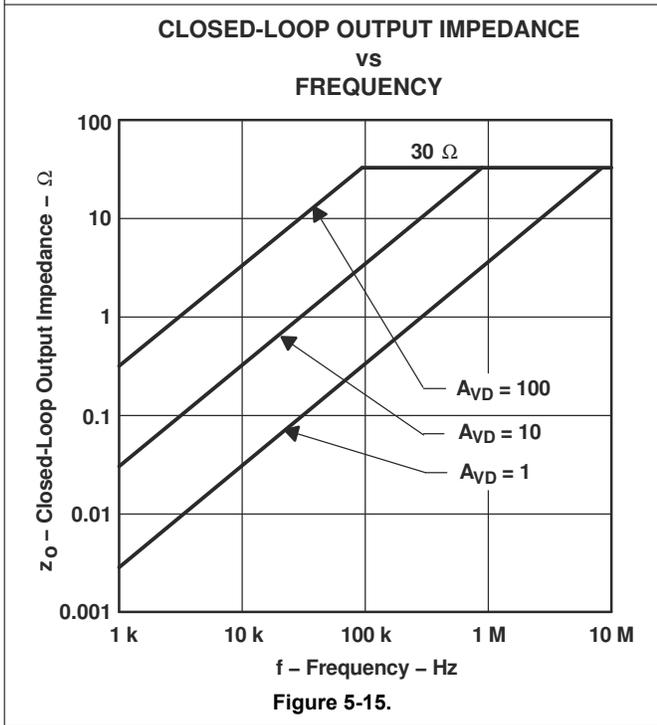
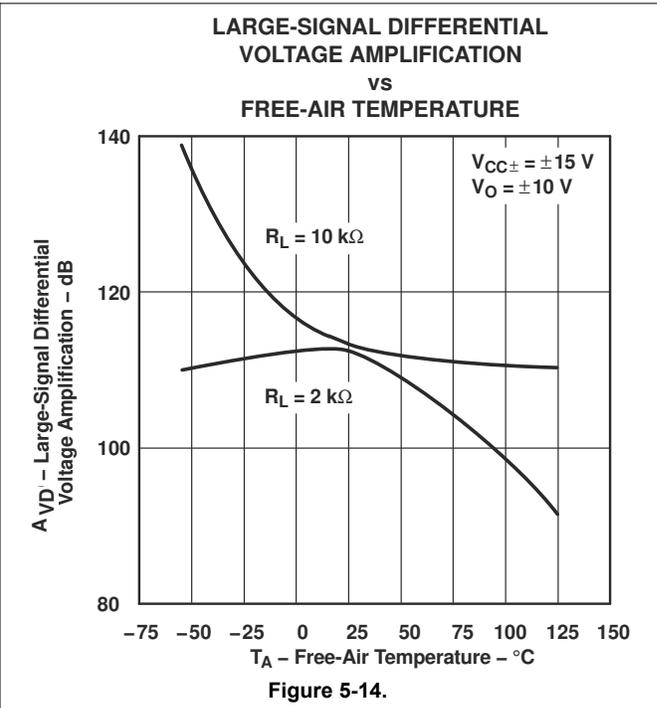
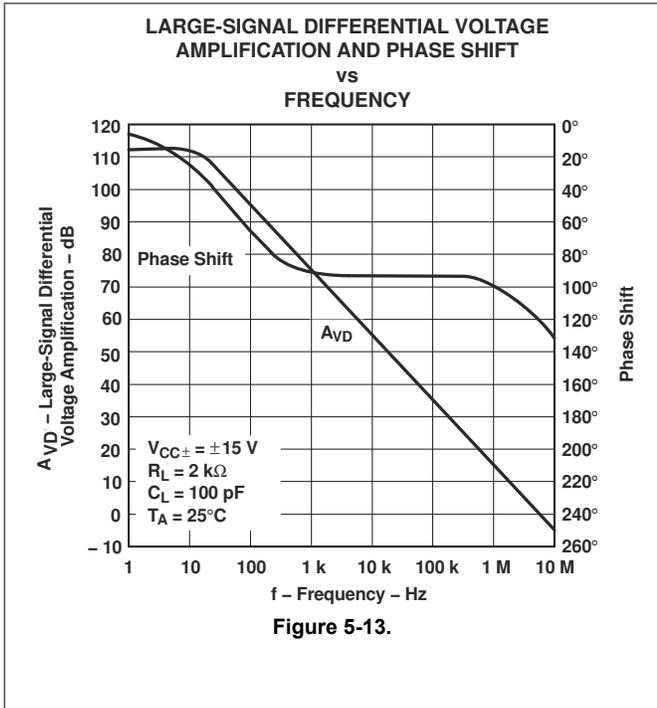
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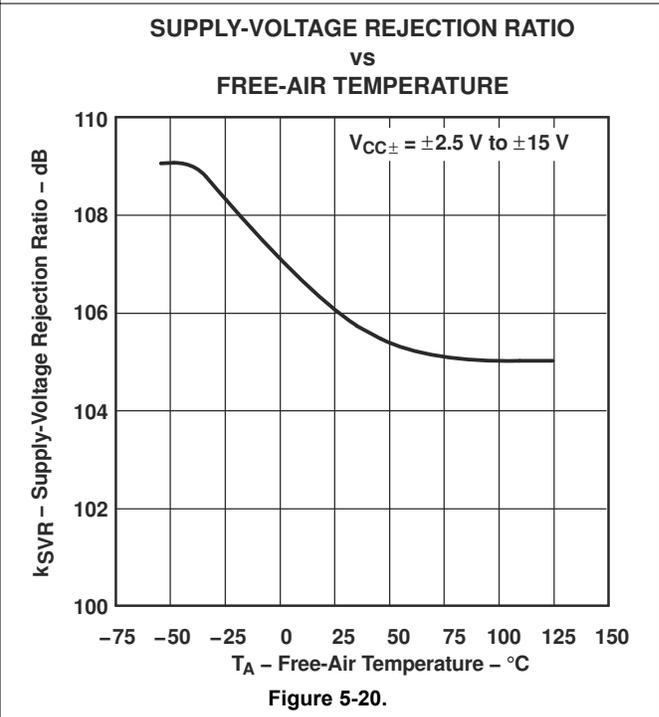
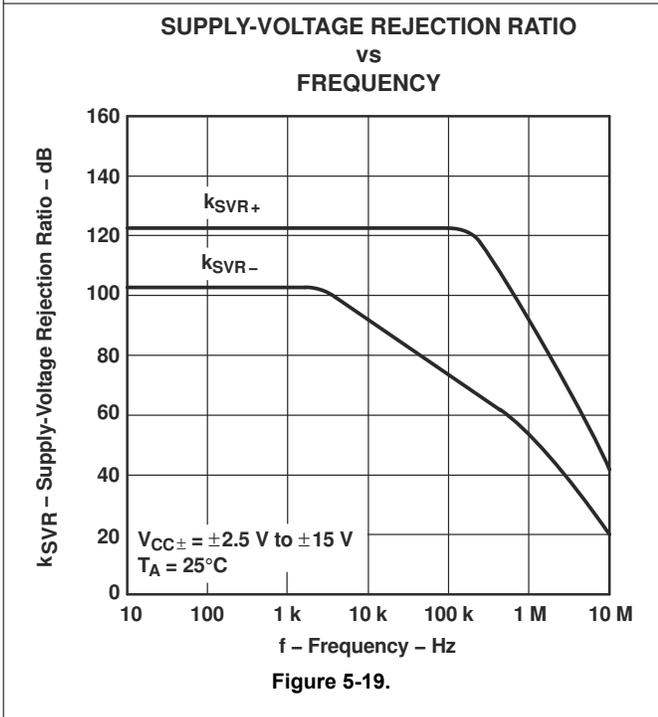
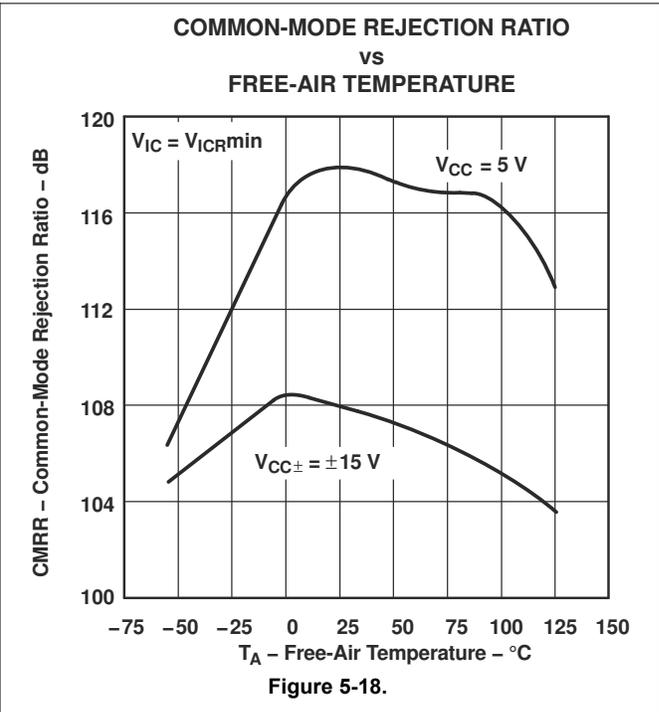
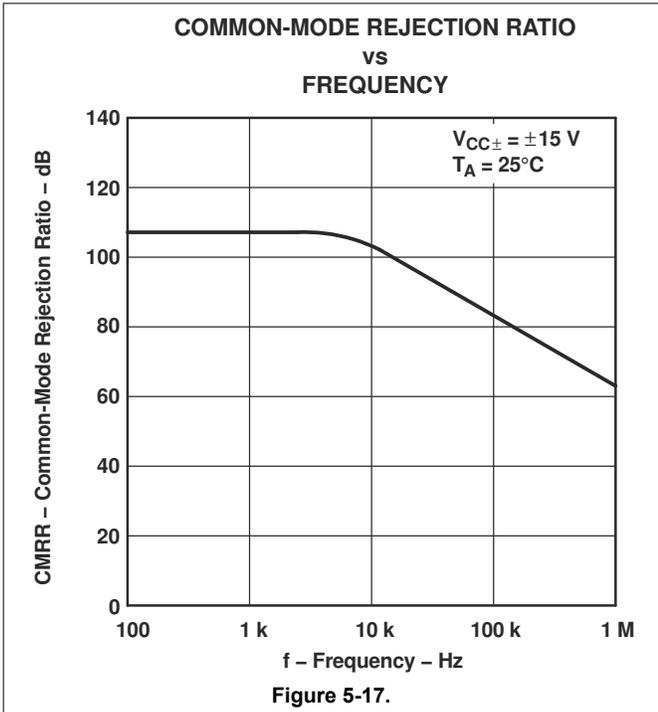
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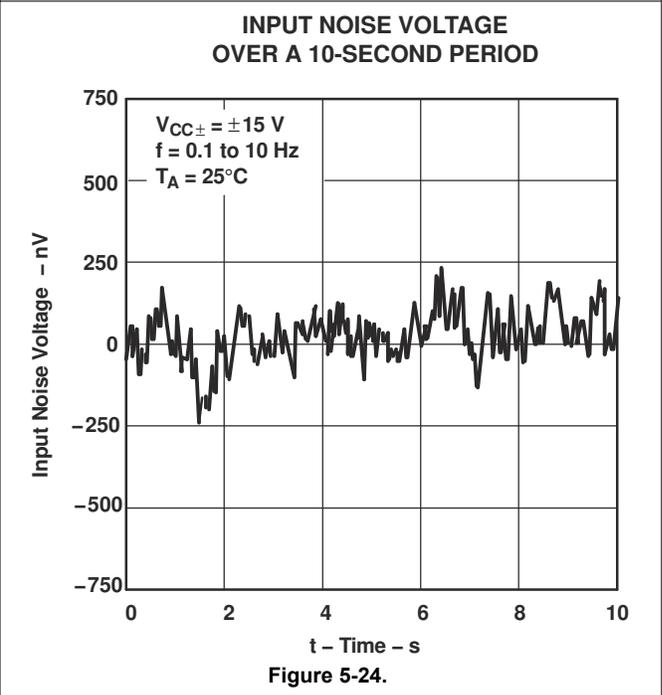
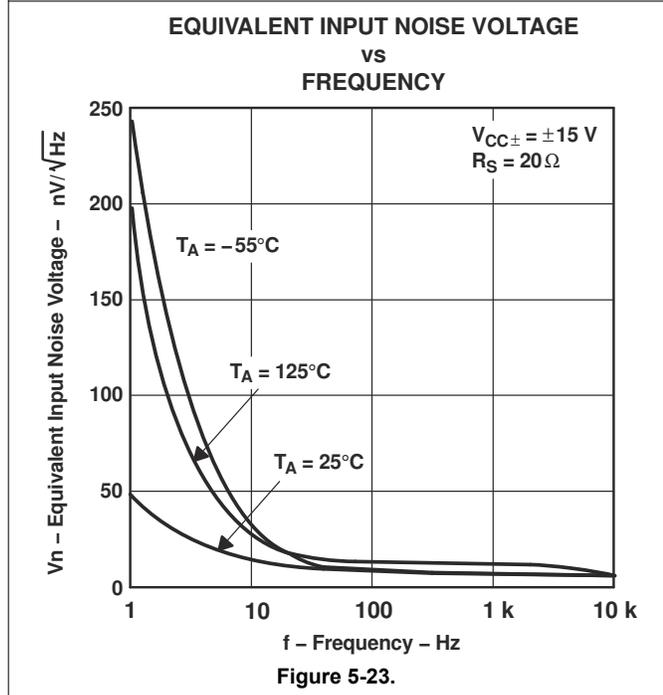
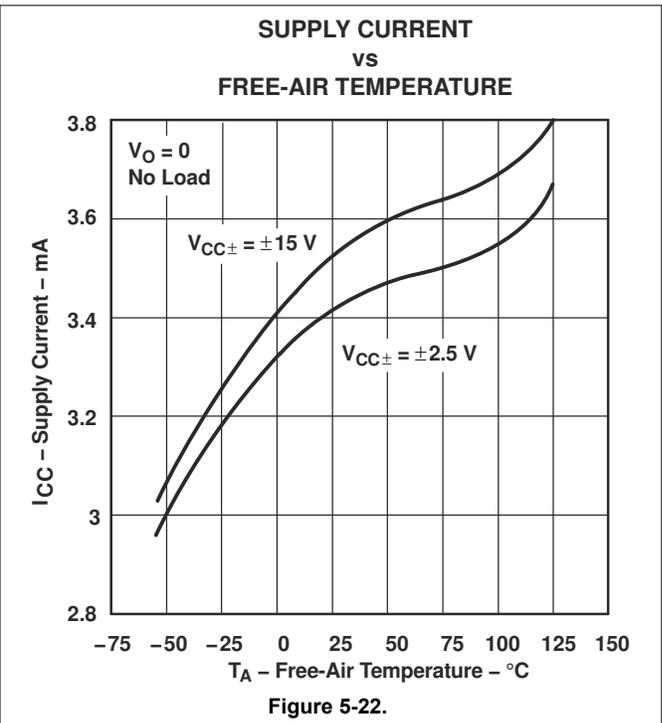
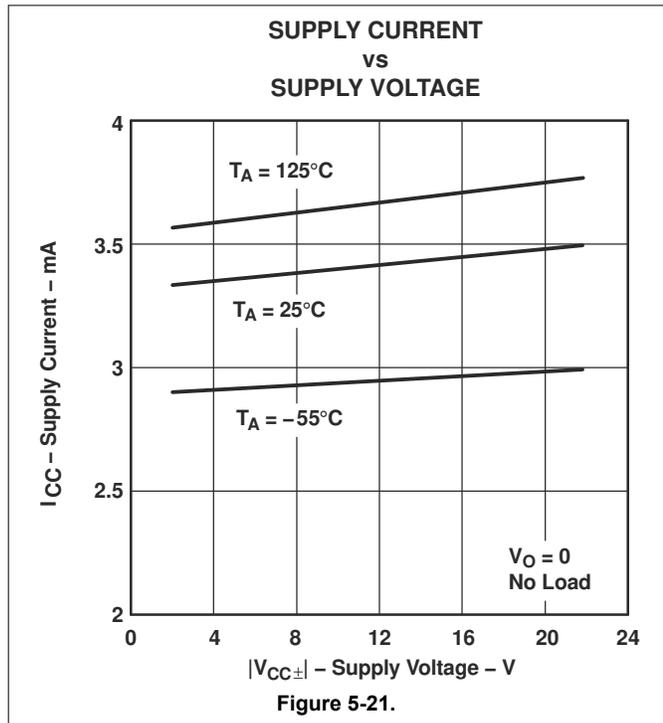
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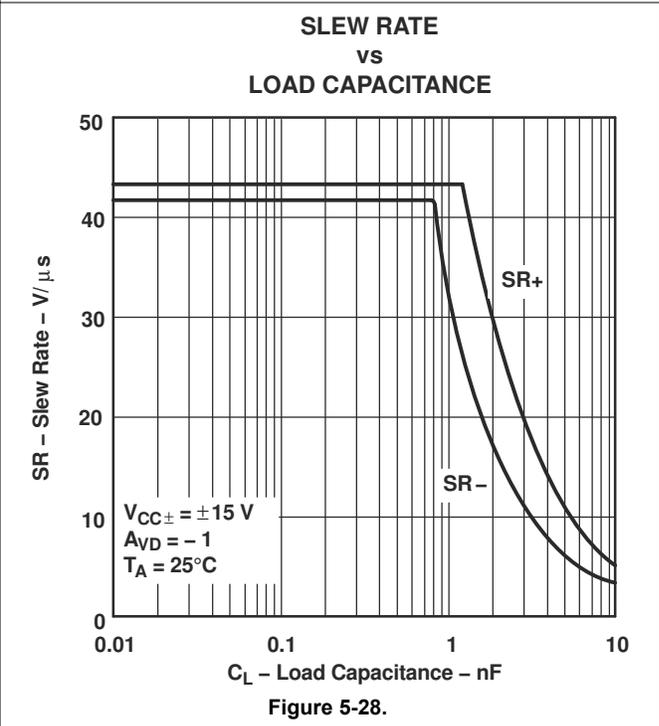
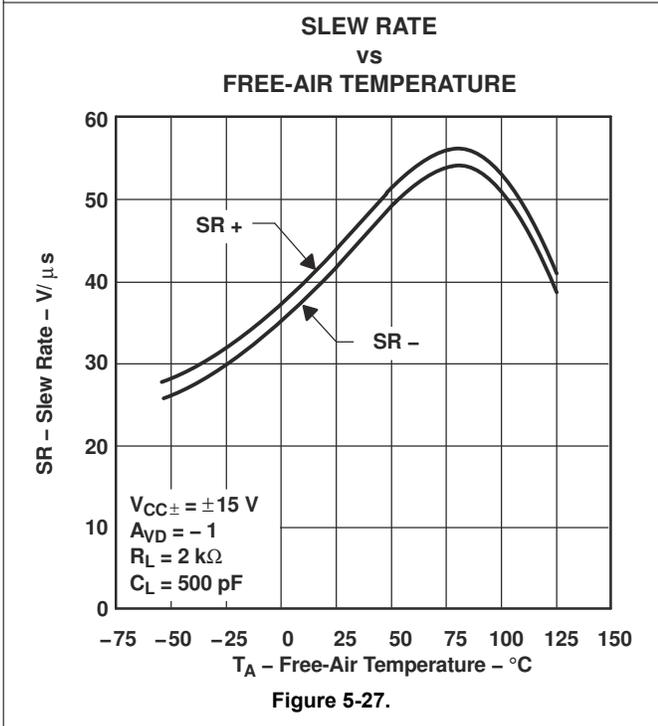
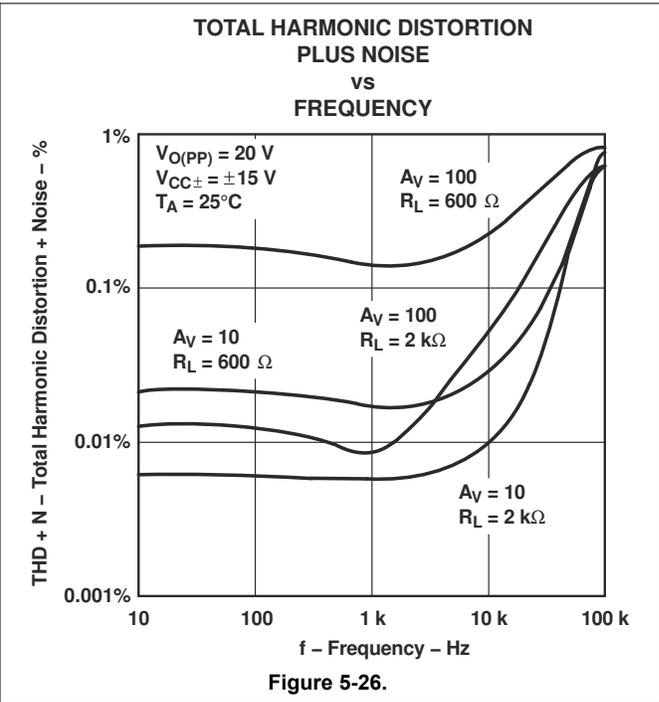
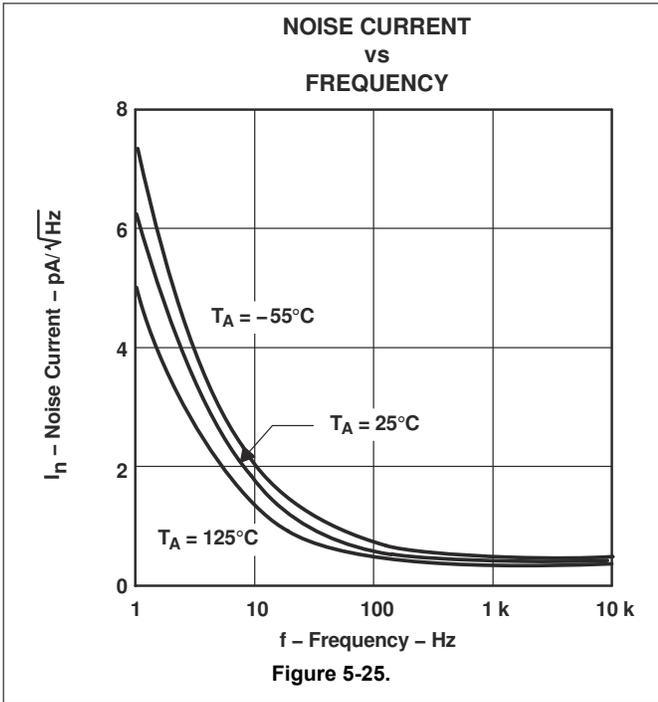
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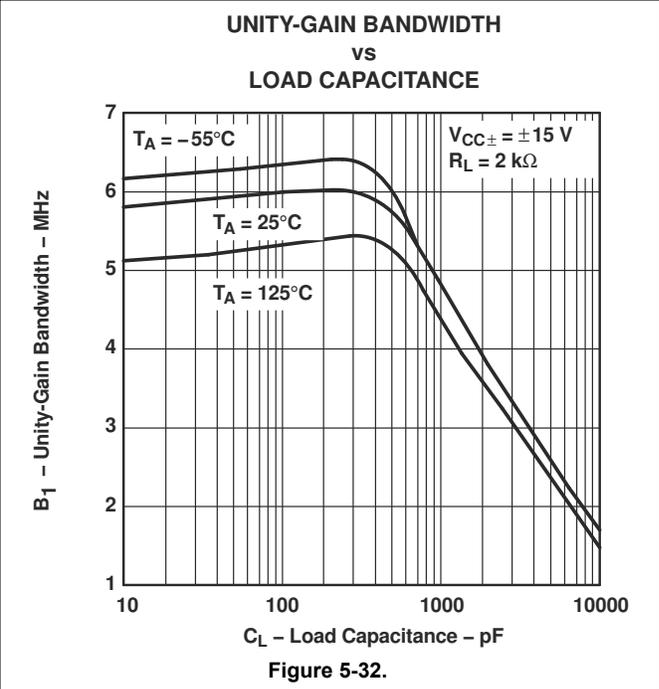
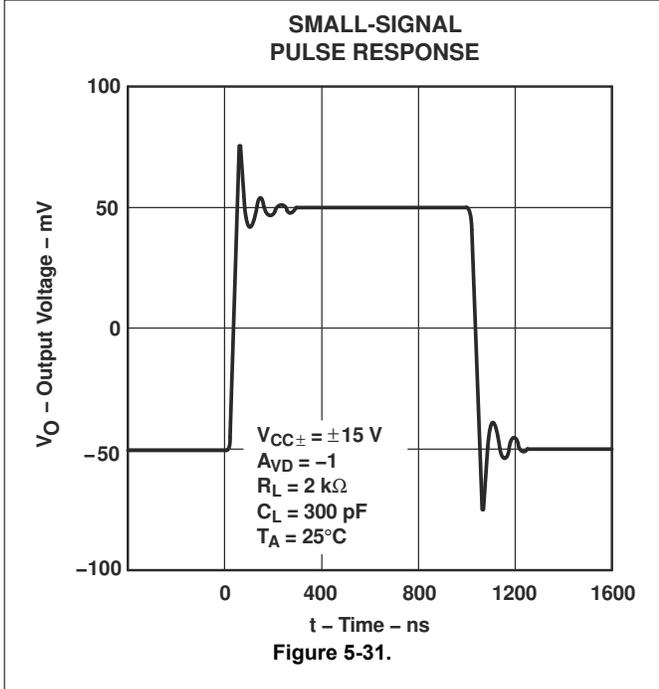
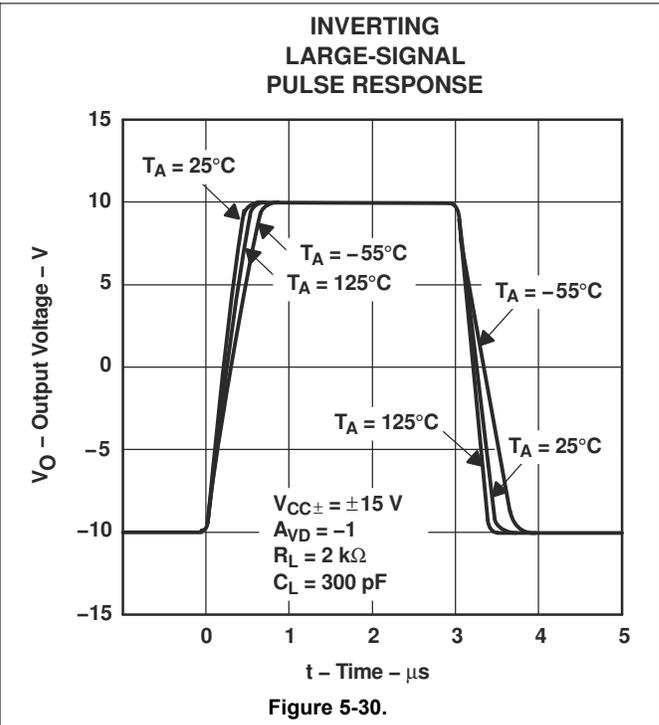
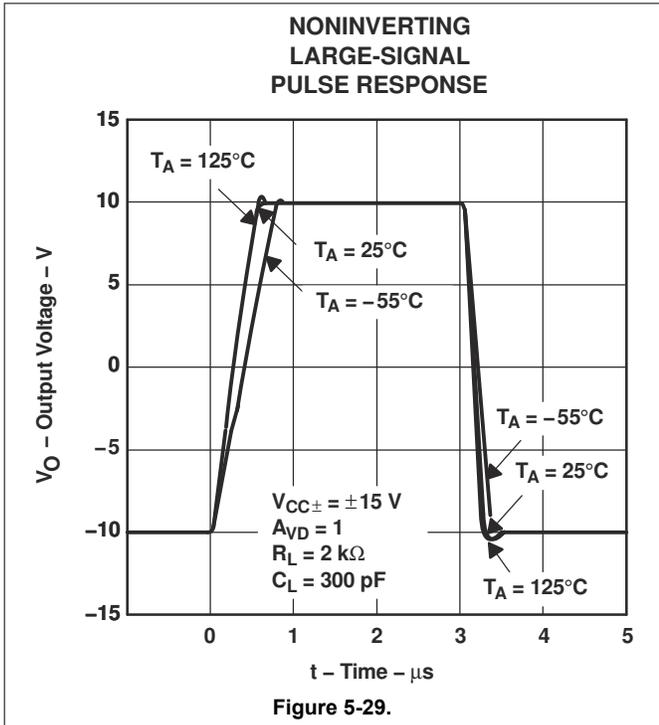
5.7 Typical Characteristics (continued)



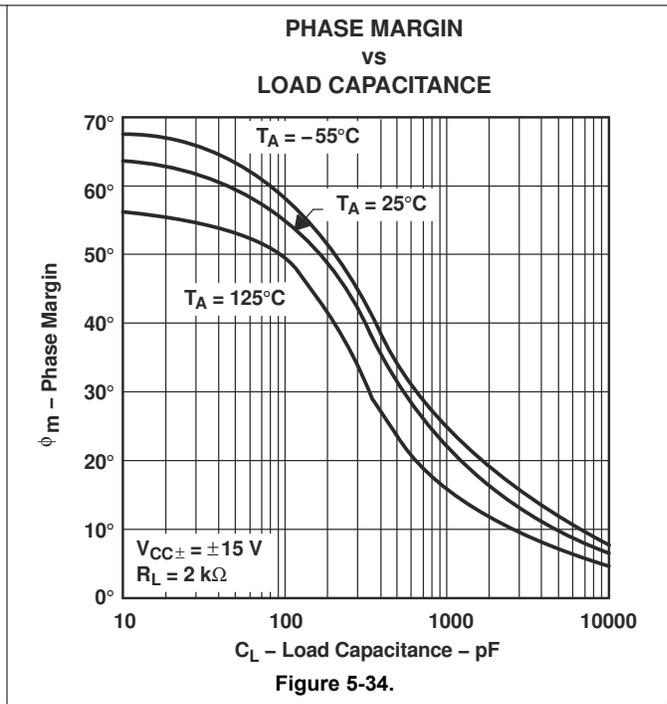
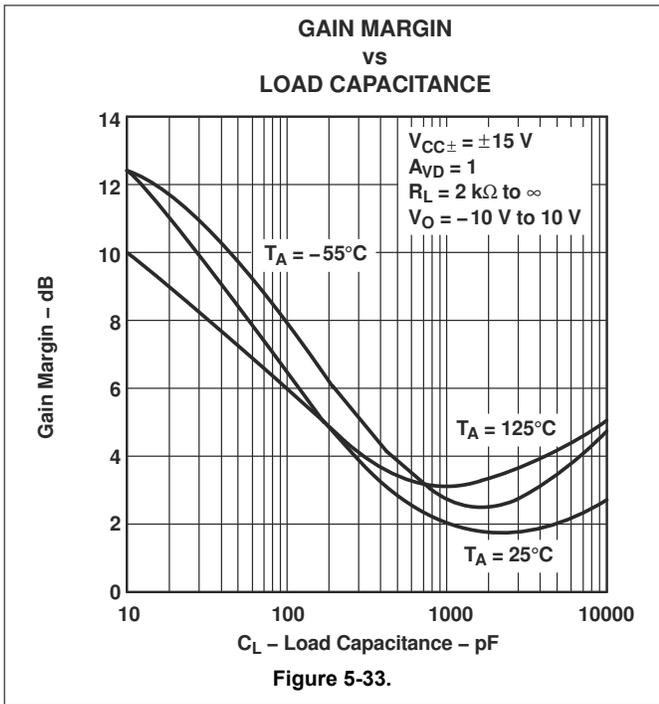
5.7 Typical Characteristics (continued)



5.7 Typical Characteristics (continued)



5.7 Typical Characteristics (continued)



6 Detailed Description

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

6.1 Overview

The TLE2141-Q1 is stable with capacitive loads up to 10nF, although the 6MHz bandwidth decreases to 1.8MHz at this high loading level. As such, this device is useful for low-droop sample-and-holds and direct buffering of long cables, including 4mA to 20mA current loops.

The special design also exhibits an improved insensitivity to inherent integrated circuit component mismatches as is evidenced by a 500 μ V maximum offset voltage and 1.7 μ V/ $^{\circ}$ C typical drift. Minimum common-mode rejection ratio and supply-voltage rejection ratio are 85dB and 90dB, respectively.

Device performance is relatively independent of supply voltage over the ± 2 V to ± 22 V range. Inputs can operate between $V_{CC-} - 0.3$ V to $V_{CC+} - 1.8$ V without inducing phase reversal, although excessive input current can flow out of each input exceeding the lower common-mode input range. The all-npn output stage provides a nearly rail-to-rail output swing of $V_{CC-} - 0.1$ V to $V_{CC+} - 1$ V under light current-loading conditions. The device can sustain shorts to either supply since output current is internally limited, but care must be taken to make sure that maximum package power dissipation is not exceeded.

The TLE2141-Q1 can also be used as a comparator. Differential inputs of $V_{CC\pm}$ can be maintained without damage to the device. Open-loop propagation delay with TTL supply levels is typically 200ns. This gives a good indication as to output stage saturation recovery when the device is driven beyond the limits of recommended output swing.

The TLE2141-Q1 is available in an industry-standard 8-pin package. The device is characterized for operation from -40° C to 125° C.

7 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

7.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

7.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

7.3 Trademarks

Excalibur™ and TI E2E™ are trademarks of Texas Instruments. All trademarks are the property of their respective owners.

7.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (September 2011) to Revision A (July 2025)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1
• Changed pins 1 and 5 from OFFSET N1 to NC and OFFSET N2 to NC.....	1
• Changed typical settling time specification from 0.34μs (0.1%, ±15V V _S) to 0.43μs, 0.4μs (0.01%, ±15V V _S) to 0.64μs, 0.16μs (0.1%, 5V V _S) to 0.66μs, and 0.22μs (0.01%, 5V V _S) to 0.99μs.....	4
• Changed typical THD+N specification at ±15V V _S from 0.01% to 0.06%.....	4
• Changed typical maximum output bandwidth specification at 5V V _S from 660kHz to 380kHz.....	4

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLE2141QDRQ1	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2141Q
TLE2141QDRQ1.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2141Q

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLE2141-Q1 :

- Catalog : [TLE2141](#)

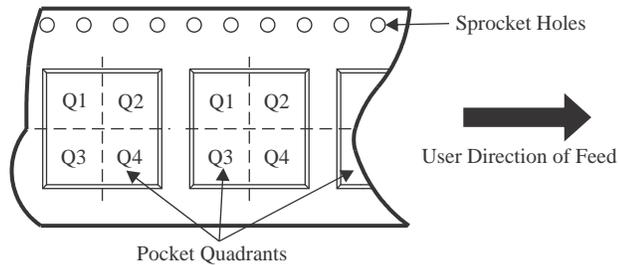
- Enhanced Product : [TLE2141-EP](#)

- Military : [TLE2141M](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


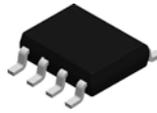
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLE2141QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLE2141QDRQ1	SOIC	D	8	2500	353.0	353.0	32.0

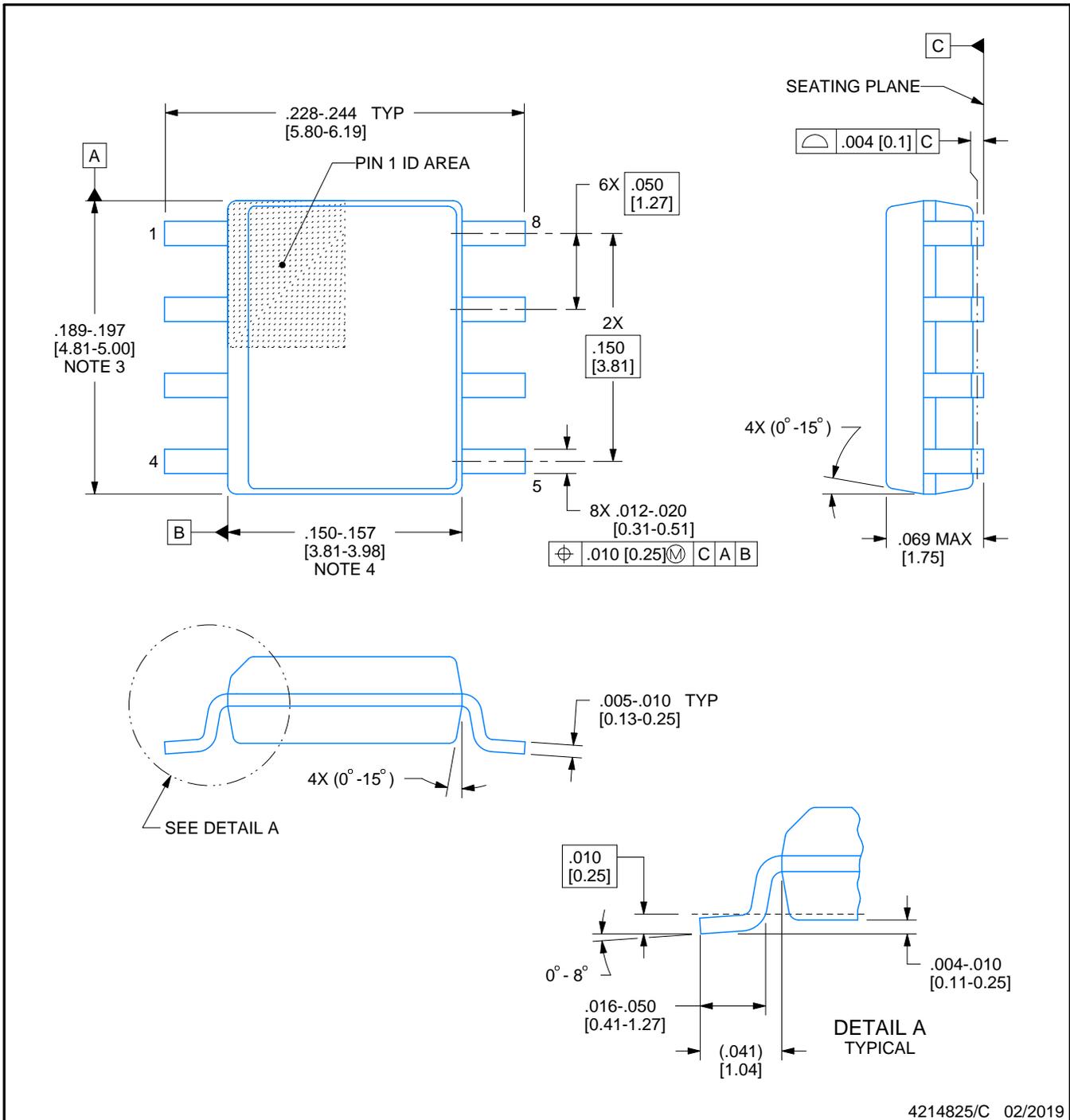


D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

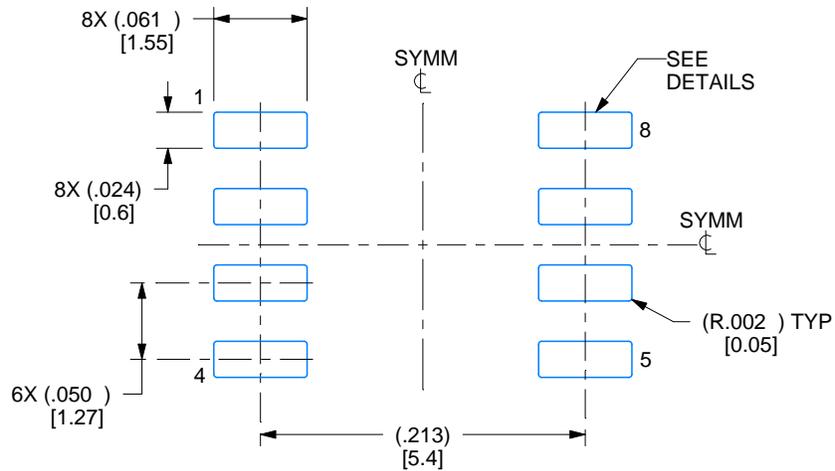
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed $.006$ [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

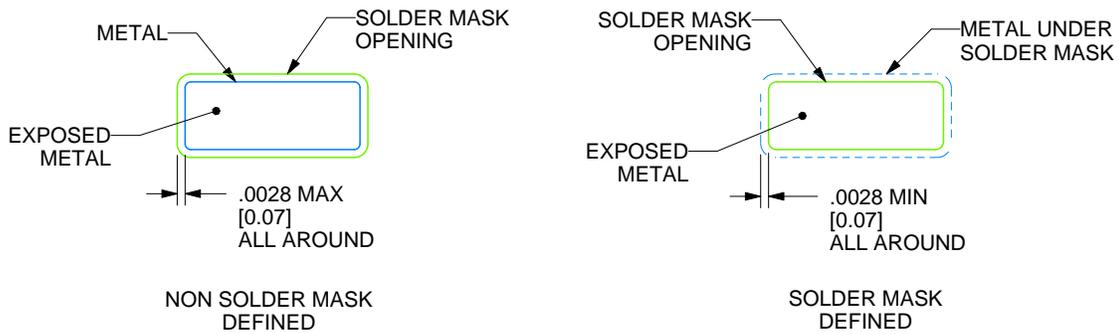
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

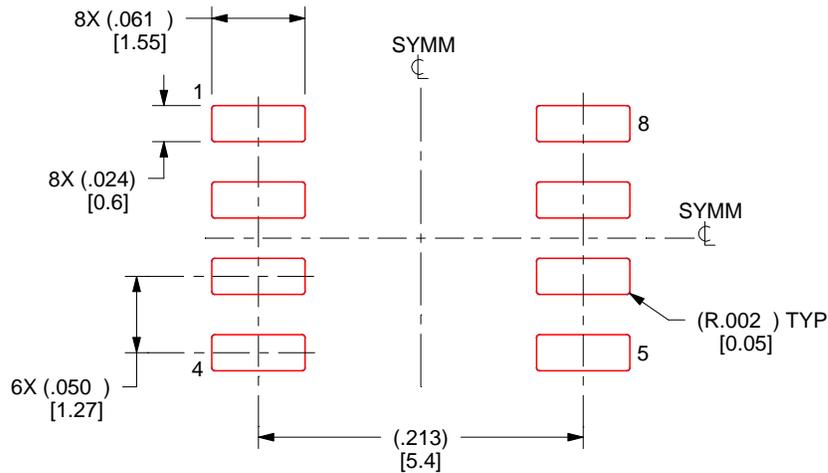
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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