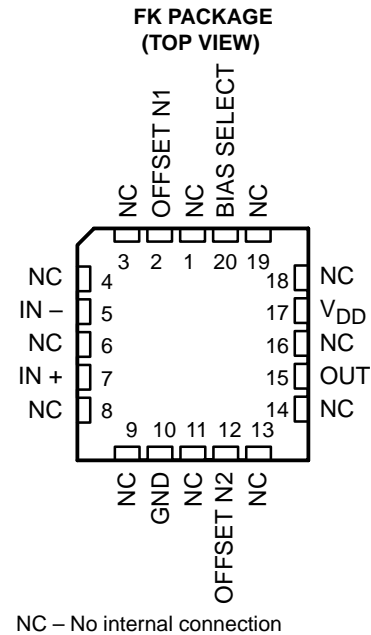
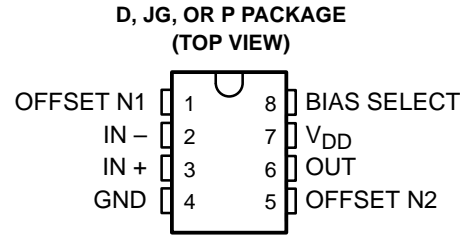


# TLC271, TLC271A, TLC271B LinCMOS™ PROGRAMMABLE LOW-POWER OPERATIONAL AMPLIFIERS

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- **Input Offset Voltage Drift . . . Typically 0.1  $\mu$ V/Month, Including the First 30 Days**
- **Wide Range of Supply Voltages Over Specified Temperature Range:**  
 $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$  . . . 3 V to 16 V  
 $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$  . . . 4 V to 16 V  
 $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  . . . 5 V to 16 V
- **Single-Supply Operation**
- **Common-Mode Input Voltage Range Extends Below the Negative Rail (C-Suffix and I-Suffix Types)**
- **Low Noise . . . 25 nV/ $\sqrt{\text{Hz}}$  Typically at  $f = 1$  kHz (High-Bias Mode)**
- **Output Voltage Range Includes Negative Rail**
- **High Input Impedance . . .  $10^{12} \Omega$  Typ**
- **ESD-Protection Circuitry**
- **Small-Outline Package Option Also Available in Tape and Reel**
- **Designed-In Latch-Up Immunity**



## description

The TLC271 operational amplifier combines a wide range of input offset voltage grades with low offset voltage drift and high input impedance. In addition, the TLC271 offers a bias-select mode that allows the user to select the best combination of power dissipation and ac performance for a particular application. These devices use Texas Instruments silicon-gate LinCMOS™ technology, which provides offset voltage stability far exceeding the stability available with conventional metal-gate processes.

### AVAILABLE OPTIONS

T <sub>A</sub>	V <sub>IO</sub> max AT 25°C	PACKAGE			
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)
0°C to 70°C	2 mV 5 mV 10 mV	TLC271BCD TLC271ACD TLC271CD	—	—	TLC271BCP TLC271ACP TLC271CP
-40°C to 85°C	2 mV 5 mV 10 mV	TLC271BID TLC271AID TLC271ID	—	—	TLC271BIP TLC271AIP TLC271IP
-55°C to 125°C	10 mV	TLC271MD	TLC271MFK	TLC271MJG	TLC271MP

The D package is available taped and reeled. Add R suffix to the device type (e.g., TLC271BCDR).



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# TLC271, TLC271A, TLC271B LinCMOS™ PROGRAMMABLE LOW-POWER OPERATIONAL AMPLIFIERS

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## DEVICE FEATURES

PARAMETER†	BIAS-SELECT MODE			UNIT
	HIGH	MEDIUM	LOW	
P <sub>D</sub>	3375	525	50	μW
SR	3.6	0.4	0.03	V/μs
V <sub>n</sub>	25	32	68	nV/√Hz
B <sub>1</sub>	1.7	0.5	0.09	MHz
A <sub>VD</sub>	23	170	480	V/mV

† Typical at V<sub>DD</sub> = 5 V, T<sub>A</sub> = 25°C

## description (continued)

Using the bias-select option, these cost-effective devices can be programmed to span a wide range of applications that previously required BiFET, NFET, or bipolar technology. Three offset voltage grades are available (C-suffix and I-suffix types), ranging from the low-cost TLC271 (10 mV) to the TLC271B (2 mV) low-offset version. The extremely high input impedance and low bias currents, in conjunction with good common-mode rejection and supply voltage rejection, make these devices a good choice for new state-of-the-art designs as well as for upgrading existing designs.

In general, many features associated with bipolar technology are available in LinCMOS™ operational amplifiers, without the power penalties of bipolar technology. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are all easily designed with the TLC271. The devices also exhibit low-voltage single-supply operation, making them ideally suited for remote and inaccessible battery-powered applications. The common-mode input voltage range includes the negative rail.

A wide range of packaging options is available, including small-outline and chip-carrier versions for high-density system applications.

The device inputs and output are designed to withstand –100-mA surge currents without sustaining latch-up.

The TLC271 incorporates internal ESD-protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from –40°C to 85°C. The M-suffix devices are characterized for operation over the full military temperature range of –55°C to 125°C.

## bias-select feature

The TLC271 offers a bias-select feature that allows the user to select any one of three bias levels depending on the level of performance desired. The tradeoffs between bias levels involve ac performance and power dissipation (see Table 1).

**Table 1. Effect of Bias Selection on Performance**

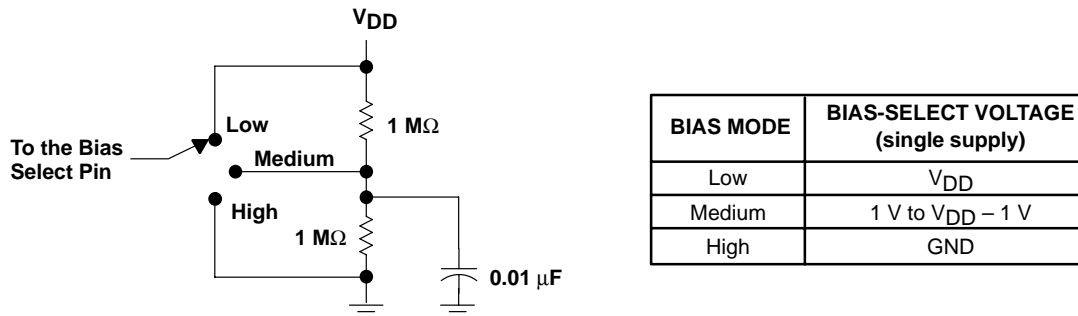
TYPICAL PARAMETER VALUES T <sub>A</sub> = 25°C, V <sub>DD</sub> = 5 V		MODE			UNIT
		HIGH BIAS R <sub>L</sub> = 10 kΩ	MEDIUM BIAS R <sub>L</sub> = 100 kΩ	LOW BIAS R <sub>L</sub> = 1 MΩ	
P <sub>D</sub>	Power dissipation	3.4	0.5	0.05	mW
SR	Slew rate	3.6	0.4	0.03	V/μs
V <sub>n</sub>	Equivalent input noise voltage at f = 1 kHz	25	32	68	nV/√Hz
B <sub>1</sub>	Unity-gain bandwidth	1.7	0.5	0.09	MHz
φ <sub>m</sub>	Phase margin	46°	40°	34°	
A <sub>VD</sub>	Large-signal differential voltage amplification	23	170	480	V/mV



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## bias selection

Bias selection is achieved by connecting the bias select pin to one of three voltage levels (see Figure 1). For medium-bias applications, it is recommended that the bias select pin be connected to the midpoint between the supply rails. This procedure is simple in split-supply applications, since this point is ground. In single-supply applications, the medium-bias mode necessitates using a voltage divider as indicated in Figure 1. The use of large-value resistors in the voltage divider reduces the current drain of the divider from the supply line. However, large-value resistors used in conjunction with a large-value capacitor require significant time to charge up to the supply midpoint after the supply is switched on. A voltage other than the midpoint can be used if it is within the voltages specified in Figure 1.



**Figure 1. Bias Selection for Single-Supply Applications**

## high-bias mode

In the high-bias mode, the TLC271 series features low offset voltage drift, high input impedance, and low noise. Speed in this mode approaches that of BiFET devices but at only a fraction of the power dissipation. Unity-gain bandwidth is typically greater than 1 MHz.

## medium-bias mode

The TLC271 in the medium-bias mode features low offset voltage drift, high input impedance, and low noise. Speed in this mode is similar to general-purpose bipolar devices but power dissipation is only a fraction of that consumed by bipolar devices.

# TLC271, TLC271A, TLC271B

## LinCMOS™ PROGRAMMABLE LOW-POWER OPERATIONAL AMPLIFIERS

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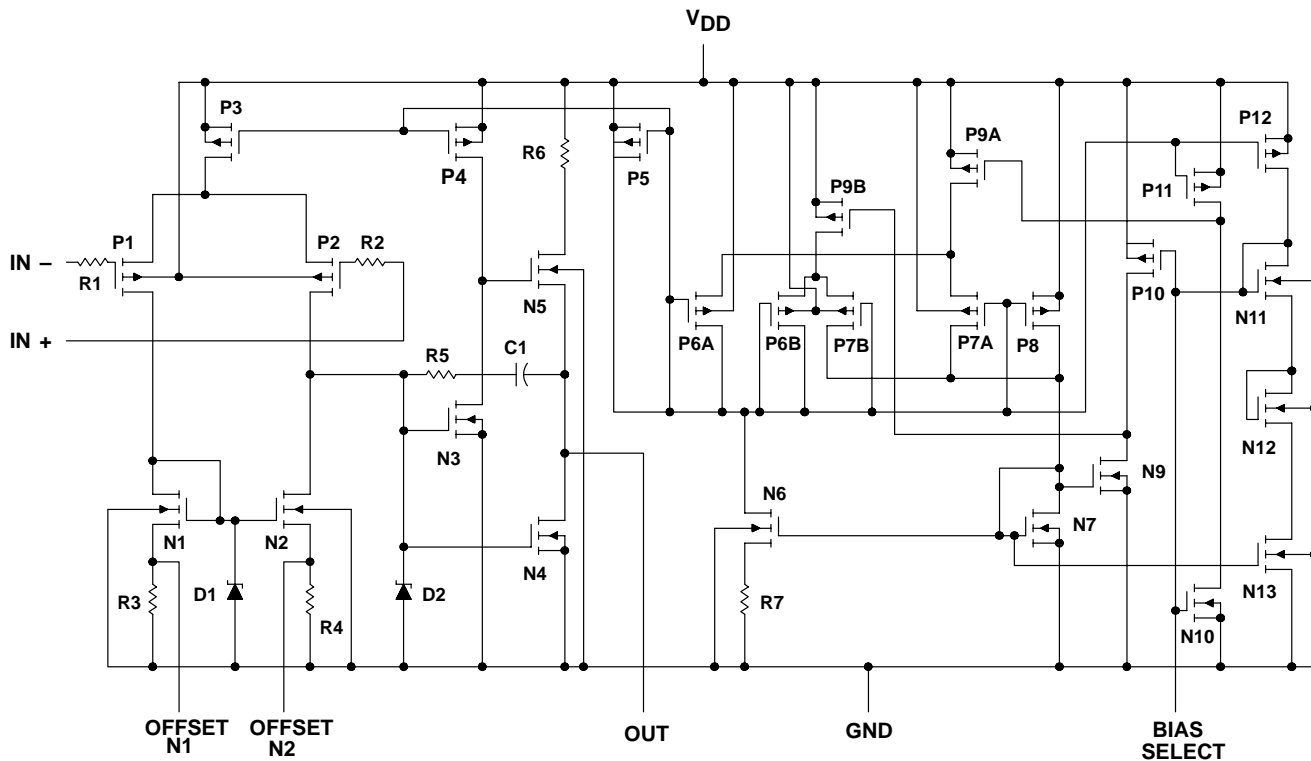
### low-bias mode

In the low-bias mode, the TLC271 features low offset voltage drift, high input impedance, extremely low power consumption, and high differential voltage gain.

#### ORDER OF CONTENTS

TOPIC	BIAS MODE
schematic	all
absolute maximum ratings	all
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electrical characteristics operating characteristics typical characteristics	low (Figures 66 – 97)
parameter measurement information	all
application information	all

### equivalent schematic



**absolute maximum ratings over operating free-air temperature (unless otherwise noted)†**

Supply voltage, $V_{DD}$ (see Note 1)	18 V
Differential input voltage, $V_{ID}$ (see Note 2)	$\pm V_{DD}$
Input voltage range, $V_I$ (any input)	–0.3 V to $V_{DD}$
Input current, $I_I$	$\pm 5$ mA
Output current, $I_O$	$\pm 30$ mA
Duration of short-circuit current at (or below) 25°C (see Note 3)	Unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature, $T_A$ : C suffix	0°C to 70°C
I suffix	–40°C to 85°C
M suffix	–55°C to 125°C
Storage temperature range	–65°C to 150°C
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package	300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.  
 2. Differential voltages are at IN+ with respect to IN–.  
 3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

**DISSIPATION RATING TABLE**

PACKAGE	$T_A \leq 25^\circ\text{C}$	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$	$T_A = 85^\circ\text{C}$	$T_A = 125^\circ\text{C}$
	POWER RATING		POWER RATING	POWER RATING	POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	200 mW

**recommended operating conditions**

		C SUFFIX		I SUFFIX		M SUFFIX		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, $V_{DD}$		3	16	4	16	5	16	V
Common-mode input voltage, $V_{IC}$	$V_{DD} = 5$ V	–0.2	3.5	–0.2	3.5	0	3.5	V
	$V_{DD} = 10$ V	–0.2	8.5	–0.2	8.5	0	8.5	
Operating free-air temperature, $T_A$		0	70	–40	85	–55	125	°C

# TLC271, TLC271A, TLC271B

## LinCMOS™ PROGRAMMABLE LOW-POWER OPERATIONAL AMPLIFIERS

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### HIGH-BIAS MODE

electrical characteristics at specified free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T <sub>A</sub> †	TLC271C, TLC271AC, TLC271BC						UNIT
				V <sub>DD</sub> = 5 V			V <sub>DD</sub> = 10 V			
				MIN	TYP	MAX	MIN	TYP	MAX	
V <sub>IO</sub>	Input offset voltage	V <sub>O</sub> = 1.4 V, V <sub>IC</sub> = 0 V, R <sub>S</sub> = 50 Ω, R <sub>L</sub> = 10 kΩ	25°C	1.1		10	1.1		10	mV
			Full range			12			12	
			25°C	0.9		5	0.9		5	
			Full range			6.5			6.5	
			25°C	0.34		2	0.39		2	
			Full range			3			3	
α <sub>VIO</sub>	Average temperature coefficient of input offset voltage		25°C to 70°C	1.8		2				μV/°C
I <sub>IO</sub>	Input offset current (see Note 4)	V <sub>O</sub> = V <sub>DD</sub> /2, V <sub>IC</sub> = V <sub>DD</sub> /2	25°C	0.1	60	0.1	60			pA
			70°C	7	300	7	300			
I <sub>IB</sub>	Input bias current (see Note 4)	V <sub>O</sub> = V <sub>DD</sub> /2, V <sub>IC</sub> = V <sub>DD</sub> /2	25°C	0.6	60	0.7	60			pA
			70°C	40	600	50	600			
V <sub>ICR</sub>	Common-mode input voltage range (see Note 5)		25°C	-0.2 to 4	-0.3 to 4.2	-0.2 to 9	-0.3 to 9.2			V
			Full range	-0.2 to 3.5		-0.2 to 8.5				V
V <sub>OH</sub>	High-level output voltage	V <sub>ID</sub> = 100 mV, R <sub>L</sub> = 10 kΩ	25°C	3.2	3.8	8	8.5			V
			0°C	3	3.8	7.8	8.5			
			70°C	3	3.8	7.8	8.4			
V <sub>OL</sub>	Low-level output voltage	V <sub>ID</sub> = -100 mV, I <sub>OL</sub> = 0	25°C	0	50	0	50			mV
			0°C	0	50	0	50			
			70°C	0	50	0	50			
A <sub>VD</sub>	Large-signal differential voltage amplification	R <sub>L</sub> = 10 kΩ, See Note 6	25°C	5	23	10	36			V/mV
			0°C	4	27	7.5	42			
			70°C	4	20	7.5	32			
CMRR	Common-mode rejection ratio	V <sub>IC</sub> = V <sub>ICRmin</sub>	25°C	65	80	65	85			dB
			0°C	60	84	60	88			
			70°C	60	85	60	88			
k <sub>SVR</sub>	Supply-voltage rejection ratio (ΔV <sub>DD</sub> /ΔV <sub>IO</sub> )	V <sub>DD</sub> = 5 V to 10 V V <sub>O</sub> = 1.4 V	25°C	65	95	65	95			dB
			0°C	60	94	60	94			
			70°C	60	96	60	96			
I <sub>I(SEL)</sub>	Input current (BIAS SELECT)	V <sub>I(SEL)</sub> = 0	25°C	-1.4		-1.9				μA
I <sub>DD</sub>	Supply current	V <sub>O</sub> = V <sub>DD</sub> /2, V <sub>IC</sub> = V <sub>DD</sub> /2, No load	25°C	675	1600	950	2000			μA
			0°C	775	1800	1125	2200			
			70°C	575	1300	750	1700			

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually.

6. At V<sub>DD</sub> = 5 V, V<sub>O</sub> = 0.25 V to 2 V; at V<sub>DD</sub> = 10 V, V<sub>O</sub> = 1 V to 6 V.



### HIGH-BIAS MODE

**electrical characteristics at specified free-air temperature (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	T <sub>A</sub> †	TLC271I, TLC271AI, TLC271BI						UNIT	
				V <sub>DD</sub> = 5 V			V <sub>DD</sub> = 10 V				
				MIN	TYP	MAX	MIN	TYP	MAX		
V <sub>IO</sub>	Input offset voltage	V <sub>O</sub> = 1.4 V, V <sub>IC</sub> = 0 V, R <sub>S</sub> = 50 Ω, R <sub>L</sub> = 10 kΩ	25°C		1.1	10		1.1	10	mV	
			Full range				13		13		
			25°C		0.9	5		0.9	5		
			Full range				7		7		
			25°C		0.34	2		0.39	2		
Full range				3.5		3.5					
α <sub>VIO</sub>	Average temperature coefficient of input offset voltage		25°C to 85°C		1.8		2		μV/°C		
I <sub>IO</sub>	Input offset current (see Note 4)	V <sub>O</sub> = V <sub>DD</sub> /2, V <sub>IC</sub> = V <sub>DD</sub> /2	25°C		0.1	60		0.1	60	pA	
			85°C		24	1000		26	1000		
I <sub>IB</sub>	Input bias current (see Note 4)	V <sub>O</sub> = V <sub>DD</sub> /2, V <sub>IC</sub> = V <sub>DD</sub> /2	25°C		0.6	60		0.7	60	pA	
			85°C		200	2000		220	2000		
V <sub>ICR</sub>	Common-mode input voltage range (see Note 5)		25°C	-0.2 to 4	-0.3 to 4.2		-0.2 to 9	-0.3 to 9.2		V	
			Full range	-0.2 to 3.5			-0.2 to 8.5			V	
V <sub>OH</sub>	High-level output voltage	V <sub>ID</sub> = 100 mV, R <sub>L</sub> = 10 kΩ	25°C		3.2	3.8		8	8.5	V	
			-40°C		3	3.8		7.8	8.5		
			85°C		3	3.8		7.8	8.5		
V <sub>OL</sub>	Low-level output voltage	V <sub>ID</sub> = -100 mV, I <sub>OL</sub> = 0	25°C			0	50		0	50	mV
			-40°C			0	50		0	50	
			85°C			0	50		0	50	
A <sub>VD</sub>	Large-signal differential voltage amplification	R <sub>L</sub> = 10 kΩ, See Note 6	25°C		5	23		10	36	V/mV	
			-40°C		3.5	32		7	46		
			85°C		3.5	19		7	31		
CMRR	Common-mode rejection ratio	V <sub>IC</sub> = V <sub>ICRmin</sub>	25°C		65	80		65	85	dB	
			-40°C		60	81		60	87		
			85°C		60	86		60	88		
k <sub>SVR</sub>	Supply-voltage rejection ratio (ΔV <sub>DD</sub> /ΔV <sub>IO</sub> )	V <sub>DD</sub> = 5 V to 10 V V <sub>O</sub> = 1.4 V	25°C		65	95		65	95	dB	
			-40°C		60	92		60	92		
			85°C		60	96		60	96		
I <sub>I(SEL)</sub>	Input current (BIAS SELECT)	V <sub>I(SEL)</sub> = 0	25°C		-1.4		-1.9		μA		
I <sub>DD</sub>	Supply current	V <sub>O</sub> = V <sub>DD</sub> /2, V <sub>IC</sub> = V <sub>DD</sub> /2, No load	25°C		675	1600		950	2000	μA	
			-40°C		950	2200		1375	2500		
			85°C		525	1200		725	1600		

† Full range is -40°C to 85°C.

- NOTES:
4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
  5. This range also applies to each input individually.
  6. At V<sub>DD</sub> = 5 V, V<sub>O</sub> = 0.25 V to 2 V; at V<sub>DD</sub> = 10 V, V<sub>O</sub> = 1 V to 6 V.

**TLC271, TLC271A, TLC271B**  
**LinCMOS™ PROGRAMMABLE LOW-POWER**  
**OPERATIONAL AMPLIFIERS**

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**HIGH-BIAS MODE**

**electrical characteristics at specified free-air temperature (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	T <sub>A</sub> †	TLC271M						UNIT
			V <sub>DD</sub> = 5 V			V <sub>DD</sub> = 10 V			
			MIN	TYP	MAX	MIN	TYP	MAX	
V <sub>IO</sub> Input offset voltage	V <sub>O</sub> = 1.4 V, V <sub>IC</sub> = 0 V, R <sub>S</sub> = 50 Ω, R <sub>L</sub> = 10 kΩ	25°C	1.1		10	1.1		10	mV
		Full range			12			12	
α <sub>VIO</sub> Average temperature coefficient of input offset voltage		25°C to 125°C	2.1			2.2			μV/°C
I <sub>IO</sub> Input offset current (see Note 4)	V <sub>O</sub> = V <sub>DD</sub> /2, V <sub>IC</sub> = V <sub>DD</sub> /2	25°C	0.1	60		0.1	60		pA
		125°C	1.4	15		1.8	15		nA
I <sub>IB</sub> Input bias current (see Note 4)	V <sub>O</sub> = V <sub>DD</sub> /2, V <sub>IC</sub> = V <sub>DD</sub> /2	25°C	0.6	60		0.7	60		pA
		125°C	9	35		10	35		nA
V <sub>ICR</sub> Common-mode input voltage range (see Note 5)		25°C	0 to 4	-0.3 to 4.2		0 to 9	-0.3 to 9.2		V
		Full range	0 to 3.5			0 to 8.5			V
V <sub>OH</sub> High-level output voltage	V <sub>ID</sub> = 100 mV, R <sub>L</sub> = 10 kΩ	25°C	3.2	3.8		8	8.5		V
		-55°C	3	3.8		7.8	8.5		
		125°C	3	3.8		7.8	8.4		
V <sub>OL</sub> Low-level output voltage	V <sub>ID</sub> = -100 mV, I <sub>OL</sub> = 0	25°C	0		50	0		50	mV
		-55°C	0		50	0		50	
		125°C	0		50	0		50	
A <sub>VD</sub> Large-signal differential voltage amplification	R <sub>L</sub> = 10 kΩ, See Note 6	25°C	5	23		10	36		V/mV
		-55°C	3.5	35		7	50		
		125°C	3.5	16		7	27		
CMRR Common-mode rejection ratio	V <sub>IC</sub> = V <sub>ICRmin</sub>	25°C	65	80		65	85		dB
		-55°C	60	81		60	87		
		125°C	60	84		60	86		
k <sub>SVR</sub> Supply-voltage rejection ratio (ΔV <sub>DD</sub> /ΔV <sub>IO</sub> )	V <sub>DD</sub> = 5 V to 10 V V <sub>O</sub> = 1.4 V	25°C	65	95		65	95		dB
		-55°C	60	90		60	90		
		125°C	60	97		60	97		
I <sub>I(SEL)</sub> Input current (BIAS SELECT)	V <sub>I(SEL)</sub> = 0	25°C	-1.4			-1.9			μA
I <sub>DD</sub> Supply current	V <sub>O</sub> = V <sub>DD</sub> /2, V <sub>IC</sub> = V <sub>DD</sub> /2, No load	25°C	675	1600		950	2000		μA
		-55°C	1000	2500		1475	3000		
		125°C	475	1100		625	1400		

† Full range is -55°C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually.

6. At V<sub>DD</sub> = 5 V, V<sub>O</sub> = 0.25 V to 2 V; at V<sub>DD</sub> = 10 V, V<sub>O</sub> = 1 V to 6 V.





### HIGH-BIAS MODE

operating characteristics at specified free-air temperature,  $V_{DD} = 5\text{ V}$

PARAMETER	TEST CONDITIONS	$T_A$	TLC271C, TLC271AC, TLC271BC			UNIT
			MIN	TYP	MAX	
SR      Slew rate at unity gain	$R_L = 10\text{ k}\Omega$ , $C_L = 20\text{ pF}$ , See Figure 98	$V_{I(PP)} = 1\text{ V}$	25°C	3.6		V/ $\mu$ s
			0°C	4		
			70°C	3		
		$V_{I(PP)} = 2.5\text{ V}$	25°C	2.9		
			0°C	3.1		
			70°C	2.5		
$V_n$ Equivalent input noise voltage	$f = 1\text{ kHz}$ , See Figure 99	$R_S = 20\ \Omega$ , 25°C	25		nV/ $\sqrt{\text{Hz}}$	
$B_{OM}$ Maximum output-swing bandwidth	$V_O = V_{OH}$ , $R_L = 10\text{ k}\Omega$ , $C_L = 20\text{ pF}$ , See Figure 98	25°C	320		kHz	
		0°C	340			
		70°C	260			
$B_1$ Unity-gain bandwidth	$V_I = 10\text{ mV}$ , See Figure 100	$C_L = 20\text{ pF}$ , 25°C	1.7		MHz	
			0°C			2
			70°C			1.3
$\phi_m$ Phase margin	$V_I = 10\text{ mV}$ , $C_L = 20\text{ pF}$ ,	$f = B_1$ , See Figure 100	25°C		46°	
			0°C		47°	
			70°C		44°	

operating characteristics at specified free-air temperature,  $V_{DD} = 10\text{ V}$

PARAMETER	TEST CONDITIONS	$T_A$	TLC271C, TLC271AC, TLC271BC			UNIT
			MIN	TYP	MAX	
SR      Slew rate at unity gain	$R_L = 10\text{ k}\Omega$ , $C_L = 20\text{ pF}$ , See Figure 98	$V_{I(PP)} = 1\text{ V}$	25°C	5.3		V/ $\mu$ s
			0°C	5.9		
			70°C	4.3		
		$V_{I(PP)} = 5.5\text{ V}$	25°C	4.6		
			0°C	5.1		
			70°C	3.8		
$V_n$ Equivalent input noise voltage	$f = 1\text{ kHz}$ , See Figure 99	$R_S = 20\ \Omega$ , 25°C	25		nV/ $\sqrt{\text{Hz}}$	
$B_{OM}$ Maximum output-swing bandwidth	$V_O = V_{OH}$ , $R_L = 10\text{ k}\Omega$ , $C_L = 20\text{ pF}$ , See Figure 98	25°C	200		kHz	
		0°C	220			
		70°C	140			
$B_1$ Unity-gain bandwidth	$V_I = 10\text{ mV}$ , See Figure 100	$C_L = 20\text{ pF}$ , 25°C	2.2		MHz	
			0°C			2.5
			70°C			1.8
$\phi_m$ Phase margin	$f = B_1$ , $C_L = 20\text{ pF}$ ,	$V_I = 10\text{ mV}$ , See Figure 100	25°C		49°	
			0°C		50°	
			70°C		46°	

**TLC271, TLC271A, TLC271B**  
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**HIGH-BIAS MODE**

operating characteristics at specified free-air temperature,  $V_{DD} = 5\text{ V}$

PARAMETER	TEST CONDITIONS	$T_A$	TLC271I, TLC271AI, TLC271BI			UNIT
			MIN	TYP	MAX	
SR Slew rate at unity gain	$R_L = 10\text{ k}\Omega$ , $C_L = 20\text{ pF}$ , See Figure 98	$V_{I(PP)} = 1\text{ V}$	25°C	3.6		V/ $\mu$ s
			-40°C	4.5		
			85°C	2.8		
		$V_{I(PP)} = 2.5\text{ V}$	25°C	2.9		
			-40°C	3.5		
			85°C	2.3		
$V_n$ Equivalent input noise voltage	$f = 1\text{ kHz}$ , See Figure 99	$R_S = 20\ \Omega$ , 25°C	25		nV/ $\sqrt{\text{Hz}}$	
$B_{OM}$ Maximum output-swing bandwidth	$V_O = V_{OH}$ , $R_L = 10\text{ k}\Omega$ , $C_L = 20\text{ pF}$ , See Figure 98	25°C	320		kHz	
		-40°C	380			
		85°C	250			
$B_1$ Unity-gain bandwidth	$V_I = 10\text{ mV}$ , See Figure 100	$C_L = 20\text{ pF}$	25°C	1.7		MHz
			-40°C	2.6		
			85°C	1.2		
$\phi_m$ Phase margin	$V_I = 10\text{ mV}$ , $C_L = 20\text{ pF}$ ,	$f = B_1$ , See Figure 100	25°C	46°		
			-40°C	49°		
			85°C	43°		

operating characteristics at specified free-air temperature,  $V_{DD} = 10\text{ V}$

PARAMETER	TEST CONDITIONS	$T_A$	TLC271I, TLC271AI, TLC271BI			UNIT
			MIN	TYP	MAX	
SR Slew rate at unity gain	$R_L = 10\text{ k}\Omega$ , $C_L = 20\text{ pF}$ , See Figure 98	$V_{I(PP)} = 1\text{ V}$	25°C	5.3		V/ $\mu$ s
			-40°C	6.8		
			85°C	4		
		$V_{I(PP)} = 5.5\text{ V}$	25°C	4.6		
			-40°C	5.8		
			85°C	3.5		
$V_n$ Equivalent input noise voltage	$f = 1\text{ kHz}$ , See Figure 99	$R_S = 20\ \Omega$ , 25°C	25		nV/ $\sqrt{\text{Hz}}$	
$B_{OM}$ Maximum output-swing bandwidth	$V_O = V_{OH}$ , $R_L = 10\text{ k}\Omega$ , $C_L = 20\text{ pF}$ , See Figure 98	25°C	200		kHz	
		-40°C	260			
		85°C	130			
$B_1$ Unity-gain bandwidth	$V_I = 10\text{ mV}$ , See Figure 100	$C_L = 20\text{ pF}$	25°C	2.2		MHz
			-40°C	3.1		
			85°C	1.7		
$\phi_m$ Phase margin	$V_I = 10\text{ mV}$ , $C_L = 20\text{ pF}$ ,	$f = B_1$ , See Figure 100	25°C	49°		
			-40°C	52°		
			85°C	46°		



### HIGH-BIAS MODE

**operating characteristics at specified free-air temperature,  $V_{DD} = 5\text{ V}$**

PARAMETER	TEST CONDITIONS	$T_A$	TLC271M			UNIT
			MIN	TYP	MAX	
SR      Slew rate at unity gain	$R_L = 10\text{ k}\Omega$ , $C_L = 20\text{ pF}$ , See Figure 98	$V_{I(PP)} = 1\text{ V}$	25°C	3.6		V/ $\mu$ s
			-55°C	4.7		
			125°C	2.3		
		$V_{I(PP)} = 2.5\text{ V}$	25°C	2.9		
			-55°C	3.7		
			125°C	2		
$V_n$ Equivalent input noise voltage	$f = 1\text{ kHz}$ , See Figure 99	$R_S = 20\ \Omega$	25°C	25		nV/ $\sqrt{\text{Hz}}$
$B_{OM}$ Maximum output-swing bandwidth	$V_O = V_{OH}$ , $R_L = 10\text{ k}\Omega$	$C_L = 20\text{ pF}$ , See Figure 98	25°C	320		kHz
			-55°C	400		
			125°C	230		
$B_1$ Unity-gain bandwidth	$V_I = 10\text{ mV}$ , See Figure 100	$C_L = 20\text{ pF}$	25°C	1.7		MHz
			-55°C	2.9		
			125°C	1.1		
$\phi_m$ Phase margin	$V_I = 10\text{ mV}$ , $C_L = 20\text{ pF}$	$f = B_1$ , See Figure 100	25°C	46°		
			-55°C	49°		
			125°C	41°		

**operating characteristics at specified free-air temperature,  $V_{DD} = 10\text{ V}$**

PARAMETER	TEST CONDITIONS	$T_A$	TLC271M			UNIT
			MIN	TYP	MAX	
SR      Slew rate at unity gain	$R_L = 10\text{ k}\Omega$ , $C_L = 20\text{ pF}$ , See Figure 98	$V_{I(PP)} = 1\text{ V}$	25°C	5.3		V/ $\mu$ s
			-55°C	7.1		
			125°C	3.1		
		$V_{I(PP)} = 5.5\text{ V}$	25°C	4.6		
			-55°C	6.1		
			125°C	2.7		
$V_n$ Equivalent input noise voltage	$f = 1\text{ kHz}$ , See Figure 99	$R_S = 20\ \Omega$	25°C	25		nV/ $\sqrt{\text{Hz}}$
$B_{OM}$ Maximum output-swing bandwidth	$V_O = V_{OH}$ , $R_L = 10\text{ k}\Omega$	$C_L = 20\text{ pF}$ , See Figure 98	25°C	200		kHz
			-55°C	280		
			125°C	110		
$B_1$ Unity-gain bandwidth	$V_I = 10\text{ mV}$ , See Figure 100	$C_L = 20\text{ pF}$	25°C	2.2		MHz
			-55°C	3.4		
			125°C	1.6		
$\phi_m$ Phase margin	$f = B_1$ , $C_L = 20\text{ pF}$	$V_I = 10\text{ mV}$ , See Figure 100	25°C	49°		
			-55°C	52°		
			125°C	44°		

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**TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)**

**Table of Graphs**

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$A_{VD}$	Large-signal differential voltage amplification	vs Frequency	28, 29
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		vs Capacitive load	32
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TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)†

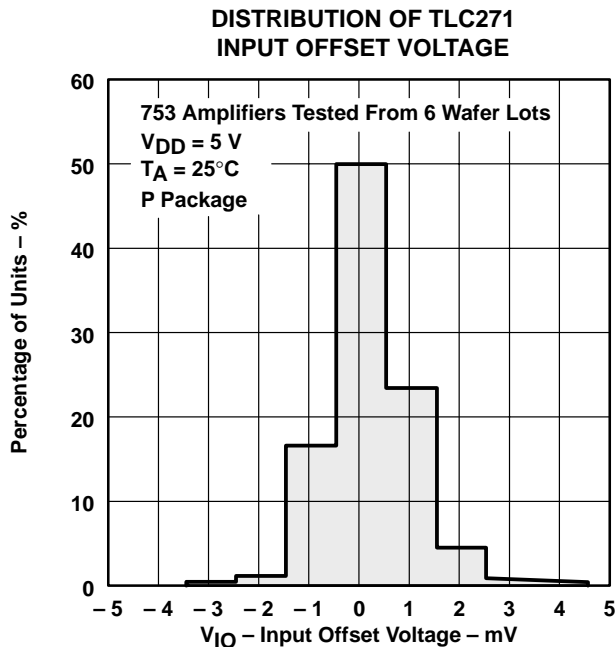


Figure 2

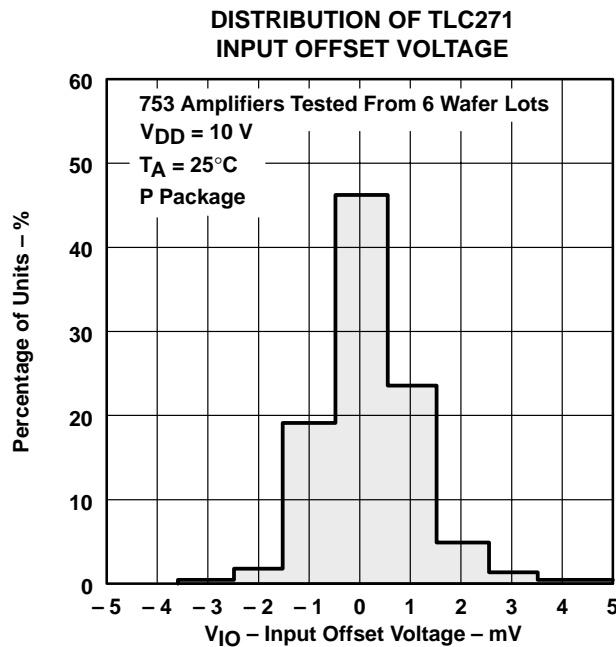


Figure 3

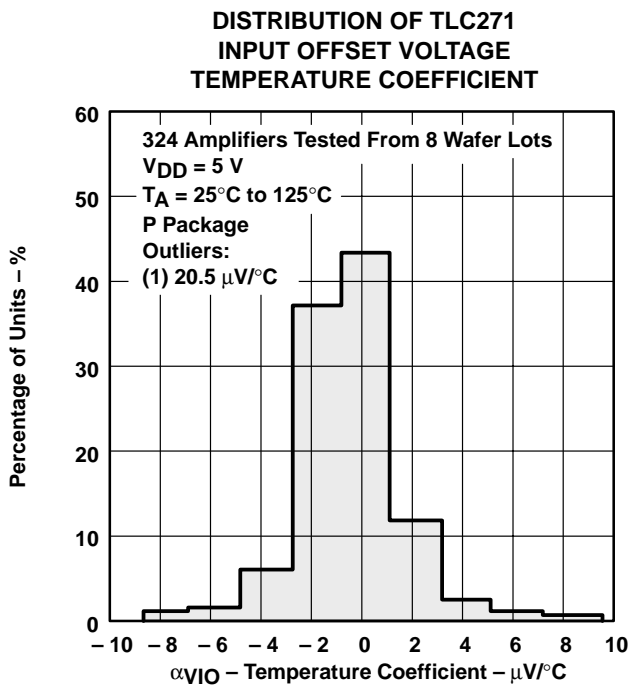


Figure 4

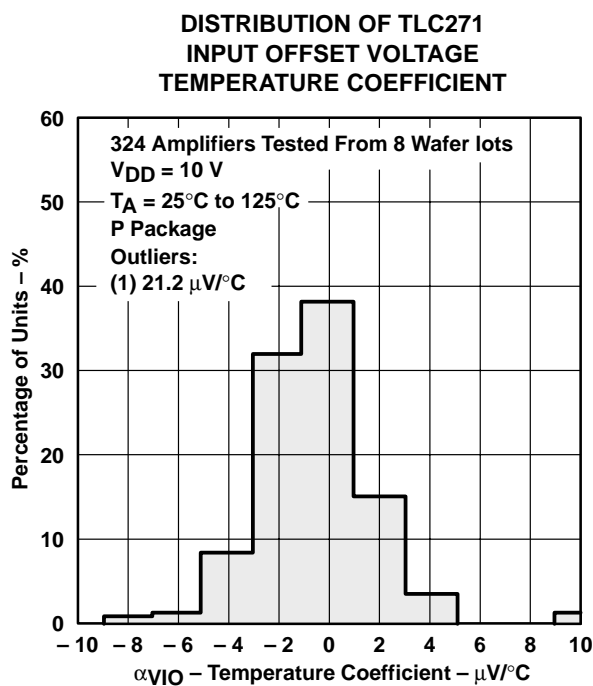
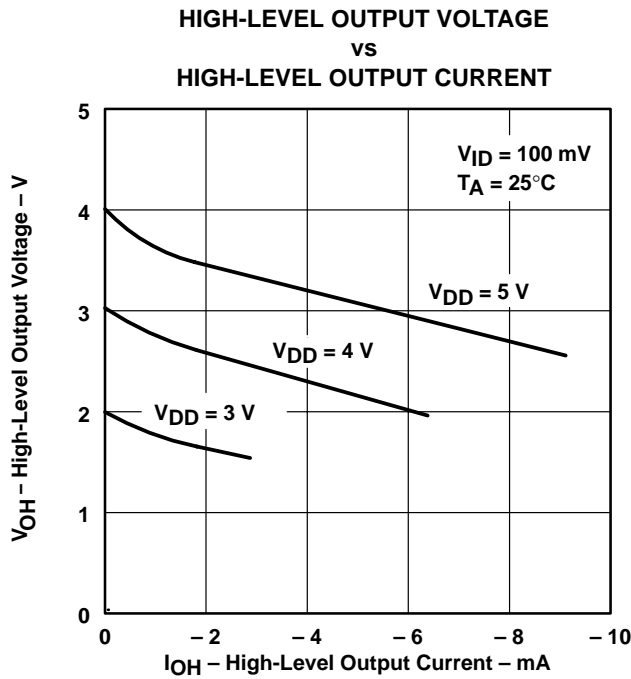


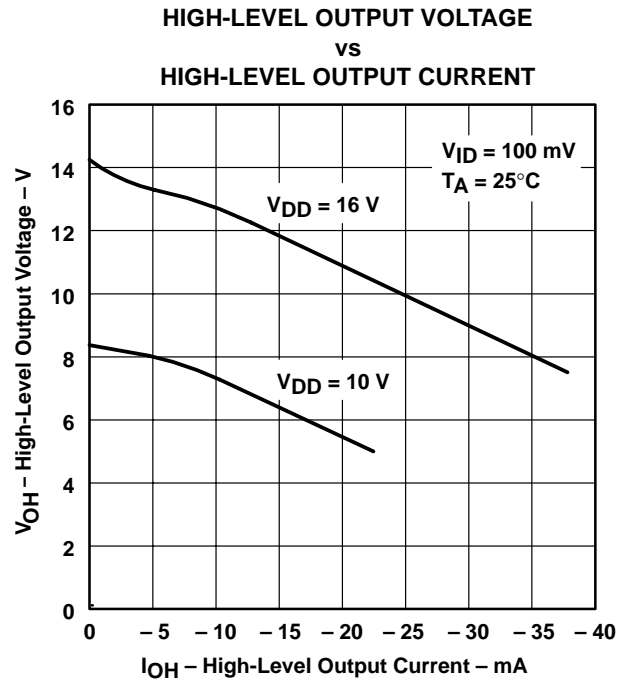
Figure 5

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

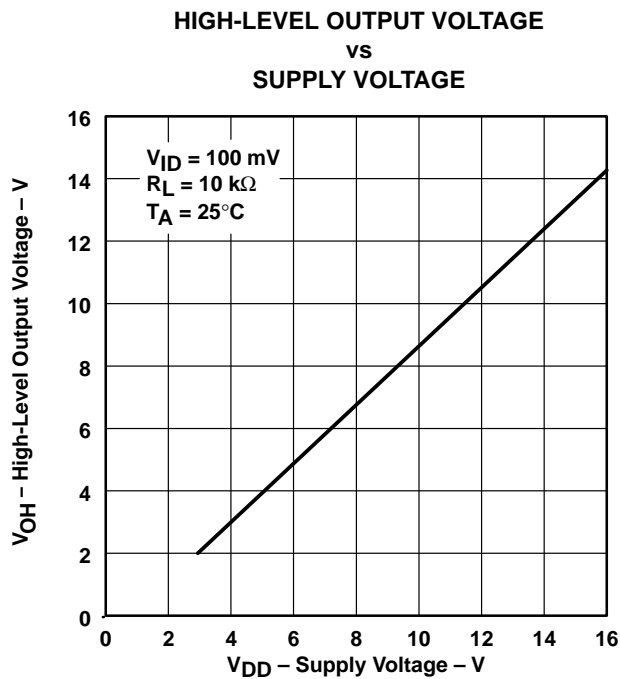
**TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)†**



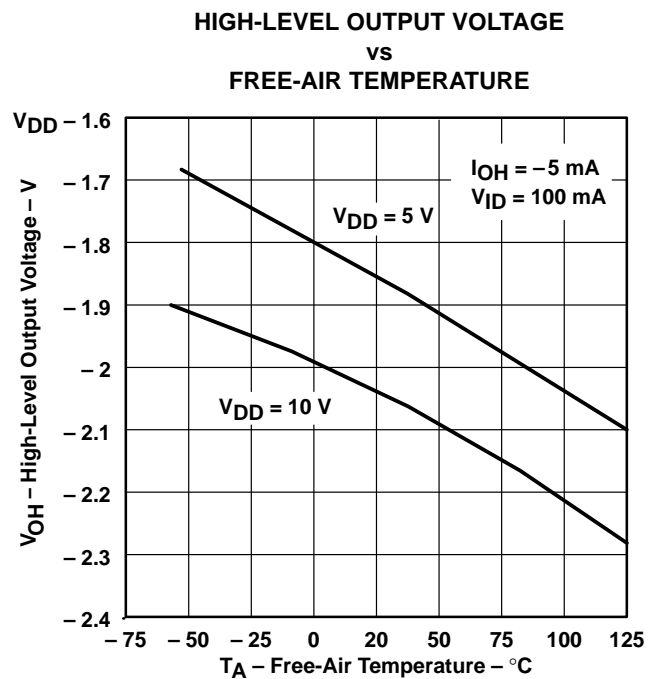
**Figure 6**



**Figure 7**



**Figure 8**



**Figure 9**

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)†

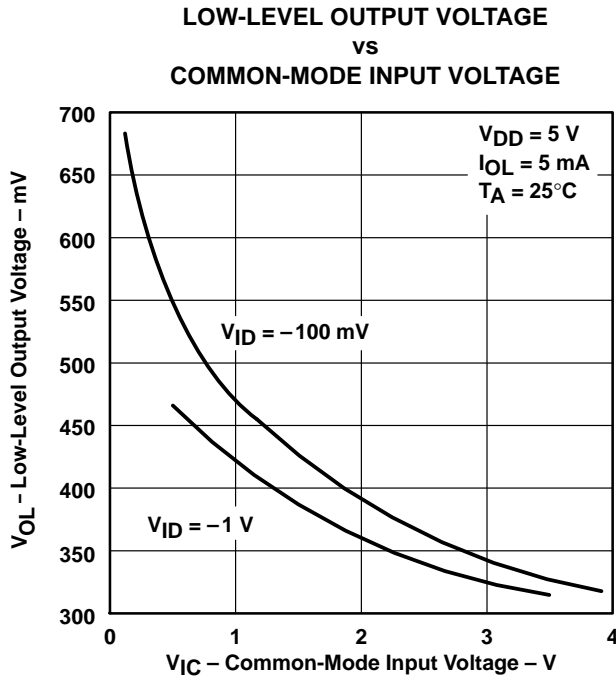


Figure 10

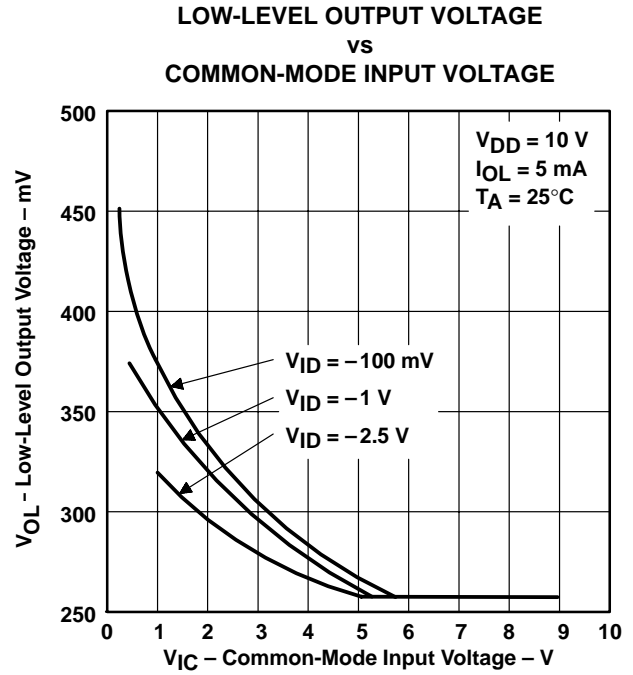


Figure 11

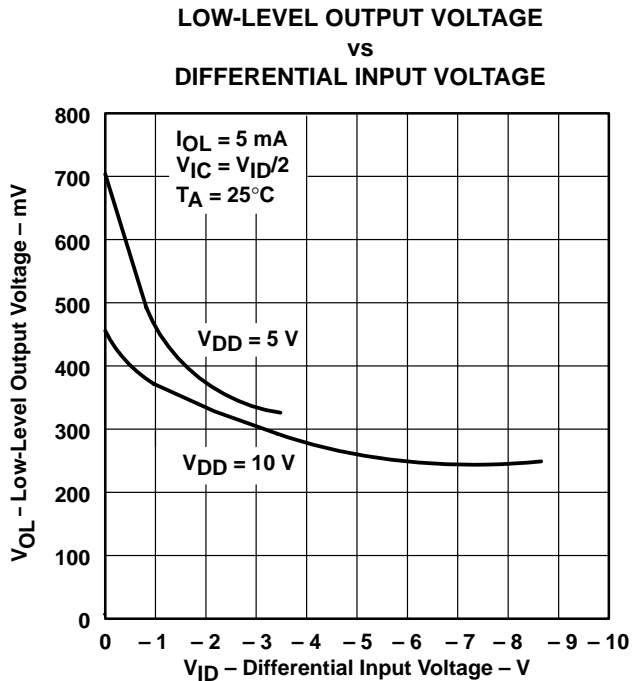


Figure 12

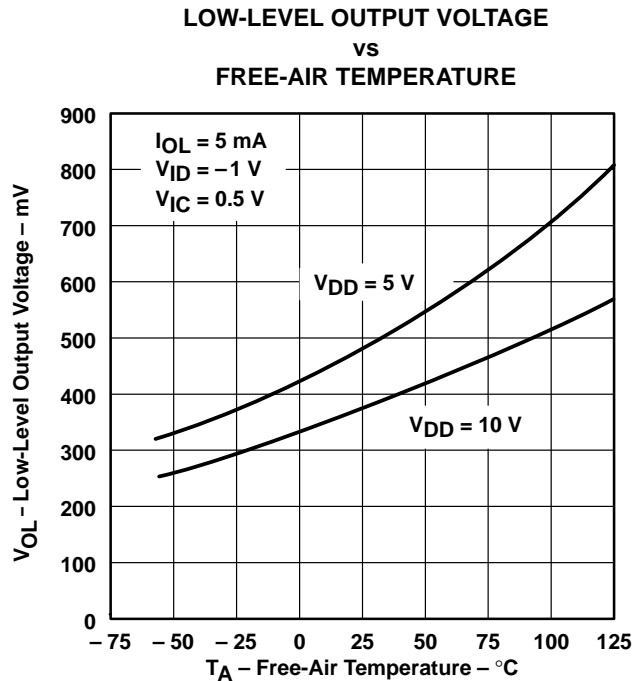
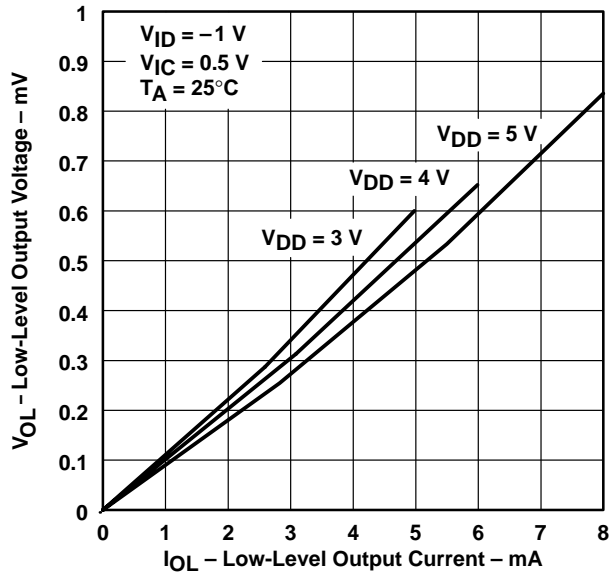


Figure 13

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

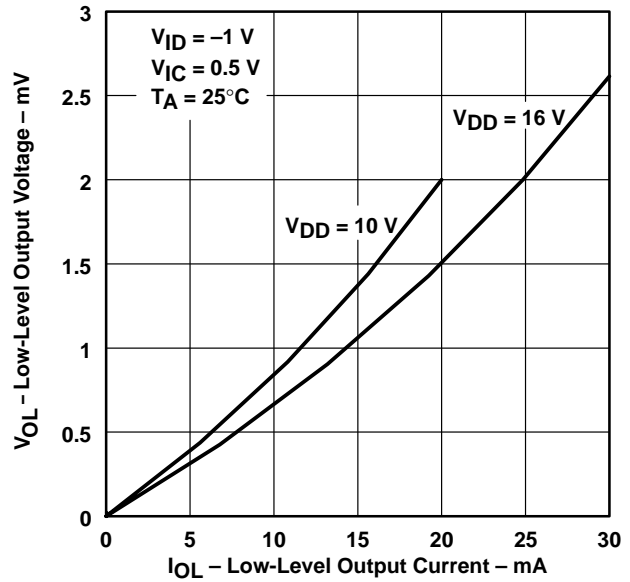
**TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)†**

**LOW-LEVEL OUTPUT VOLTAGE  
 vs  
 LOW-LEVEL OUTPUT CURRENT**



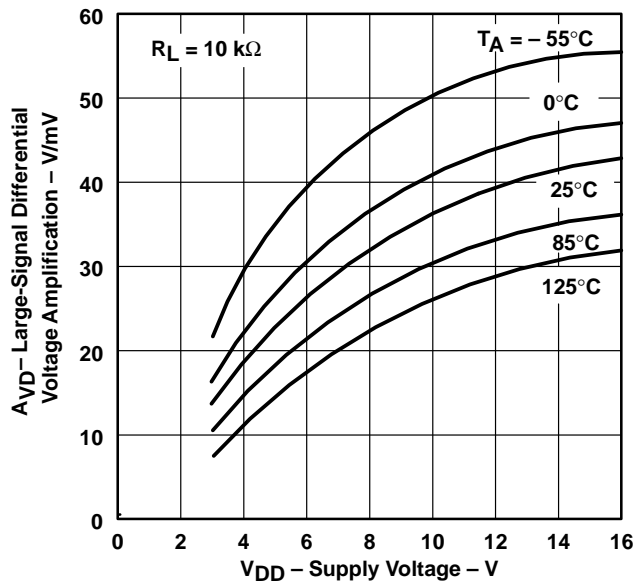
**Figure 14**

**LOW-LEVEL OUTPUT VOLTAGE  
 vs  
 LOW-LEVEL OUTPUT CURRENT**



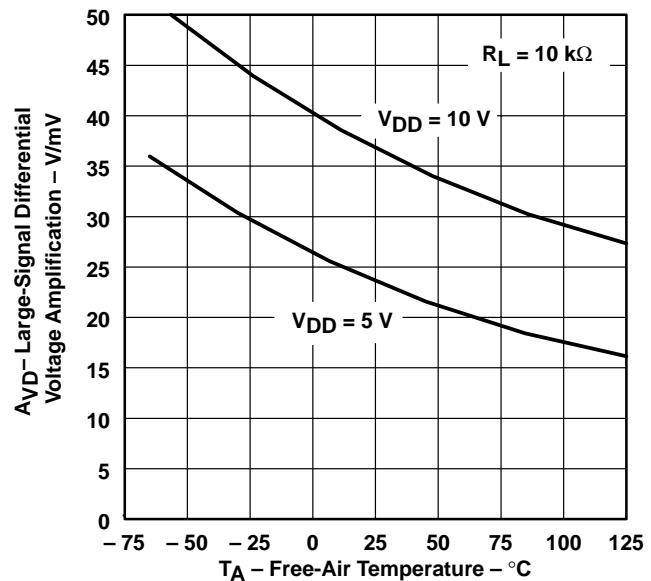
**Figure 15**

**LARGE-SIGNAL  
 DIFFERENTIAL VOLTAGE AMPLIFICATION  
 vs  
 SUPPLY VOLTAGE**



**Figure 16**

**LARGE-SIGNAL  
 DIFFERENTIAL VOLTAGE AMPLIFICATION  
 vs  
 FREE-AIR TEMPERATURE**

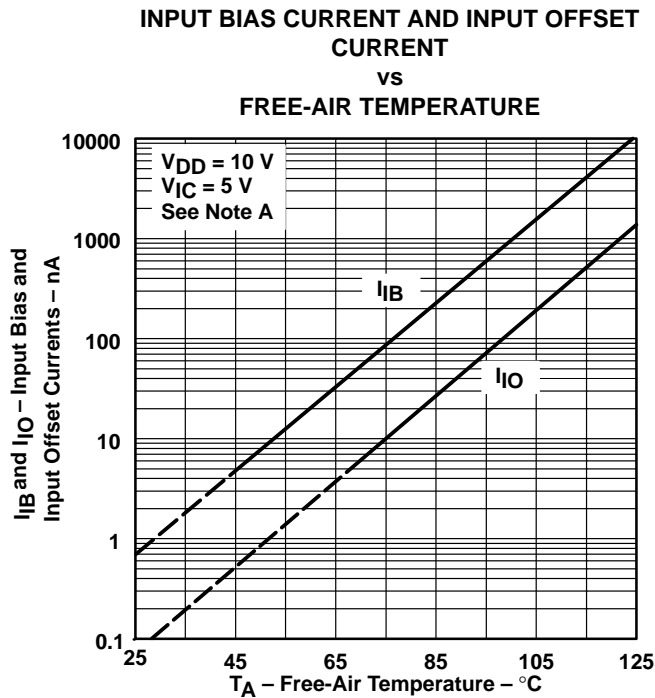


**Figure 17**

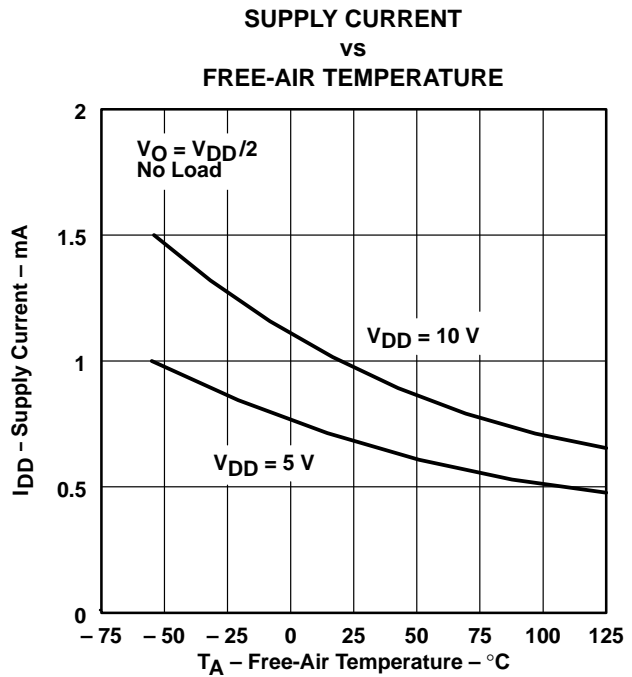
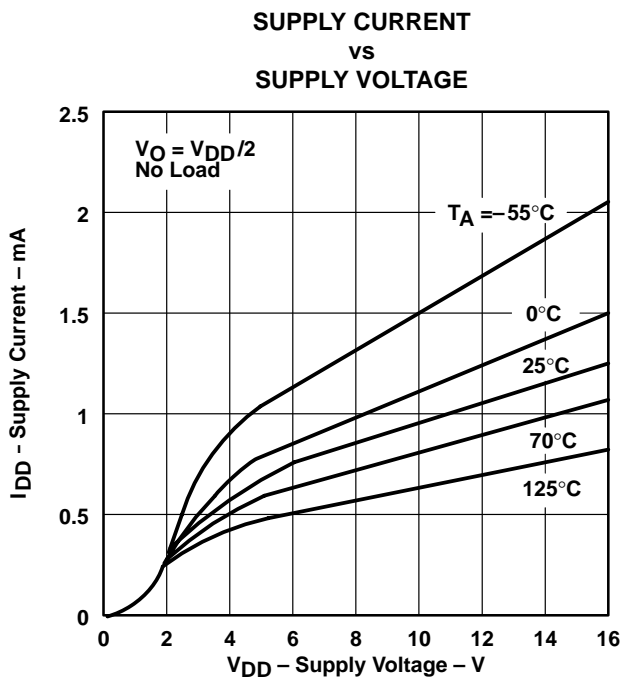
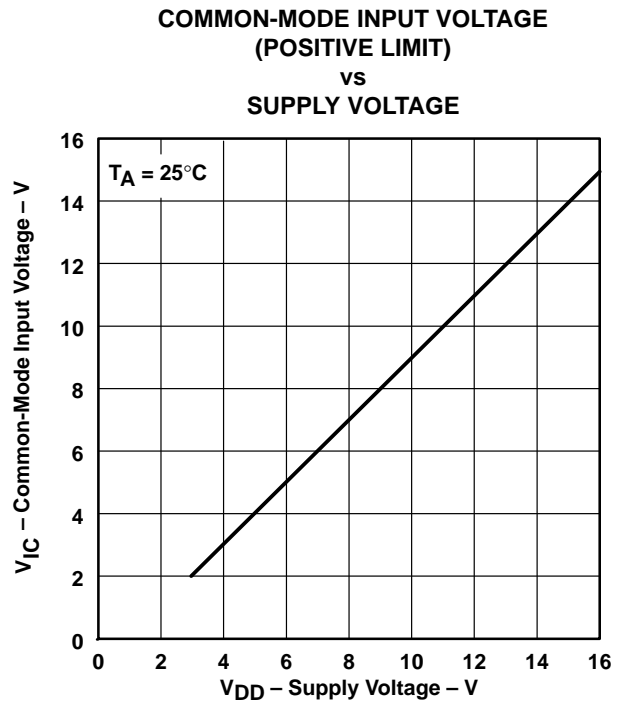
† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.



TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)†



NOTE A: The typical values of input bias current and input offset current below 5 pA were determined mathematically.



† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

**TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)†**

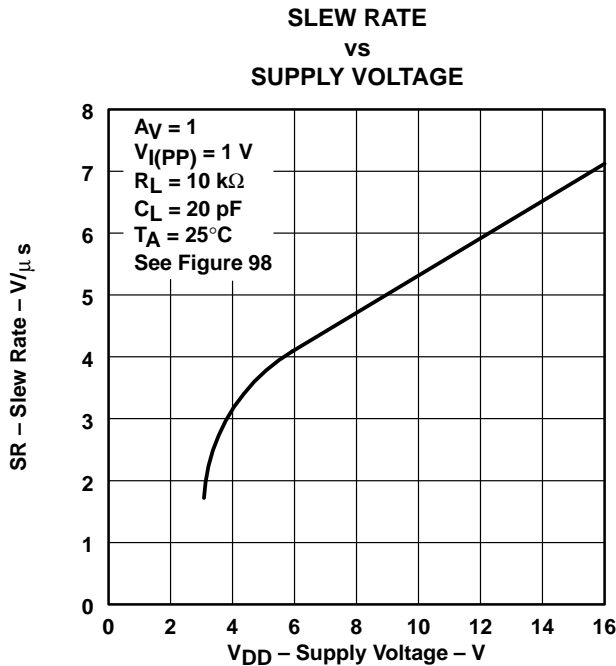


Figure 22

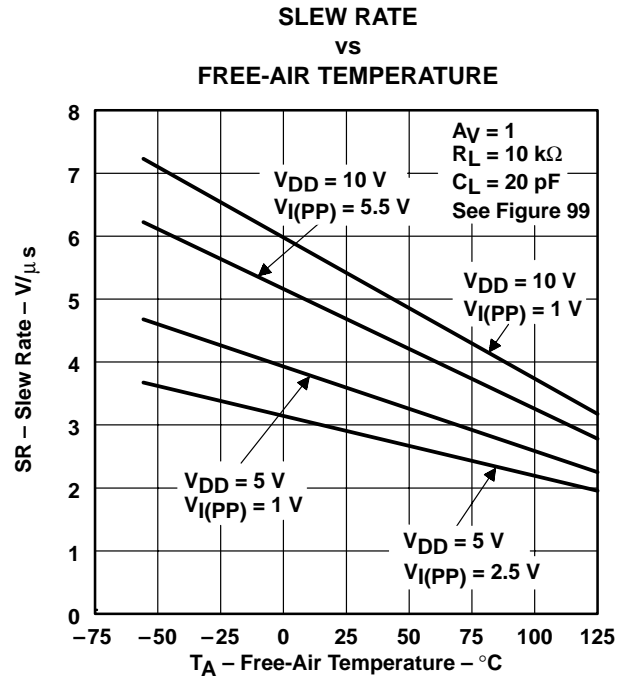


Figure 23

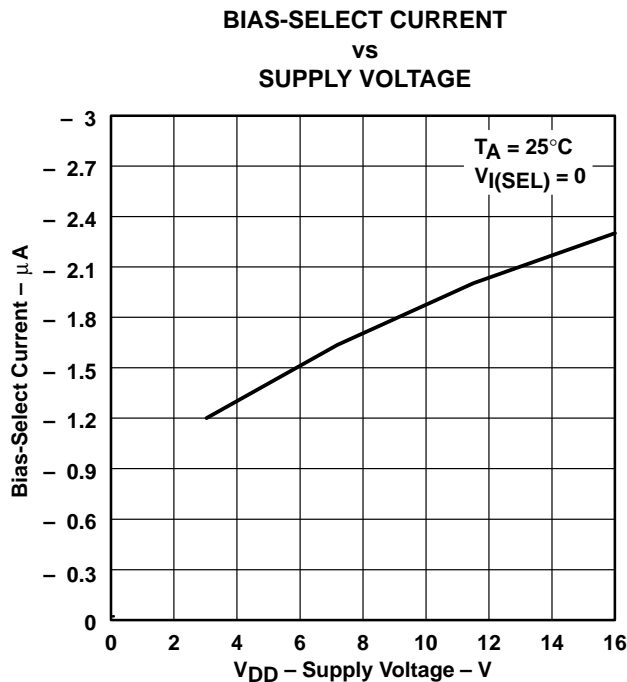


Figure 24

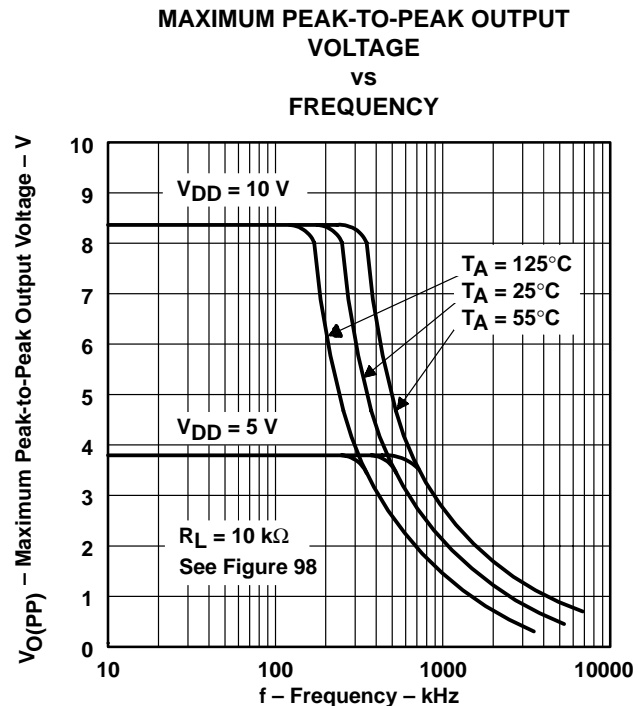


Figure 25

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)†

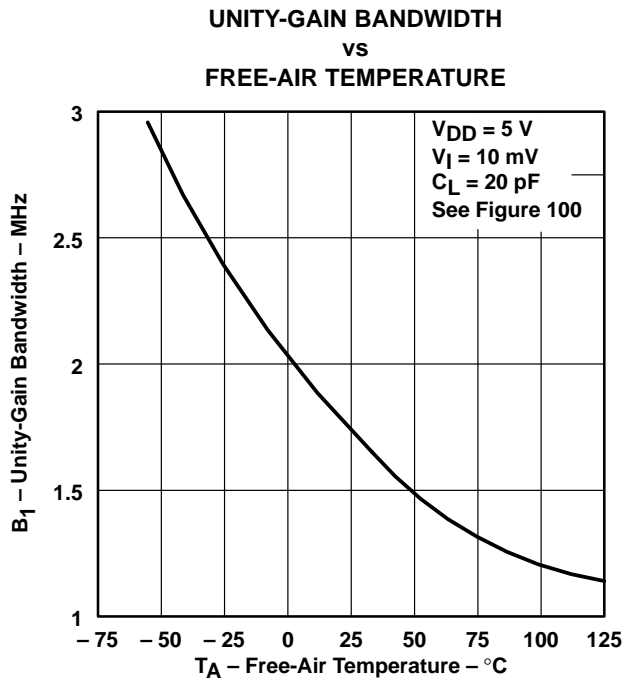


Figure 26

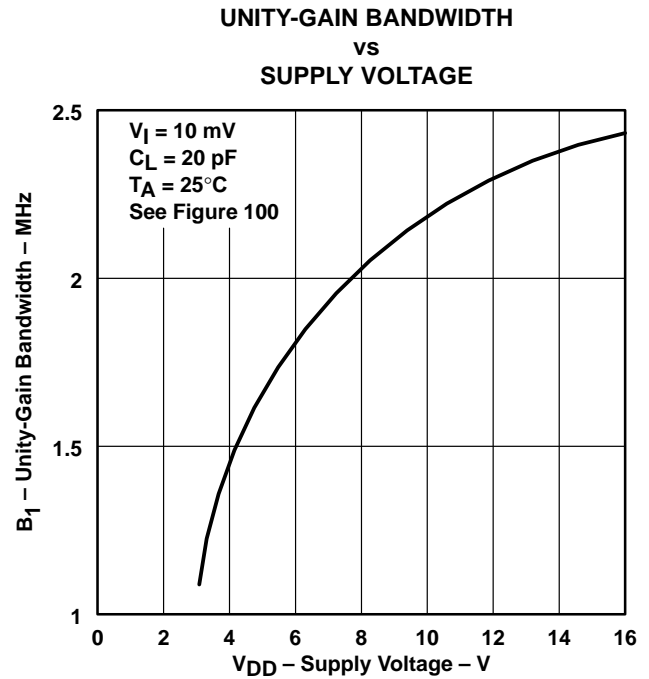


Figure 27

**LARGE-SIGNAL DIFFERENTIAL VOLTAGE  
 AMPLIFICATION AND PHASE SHIFT  
 vs  
 FREQUENCY**

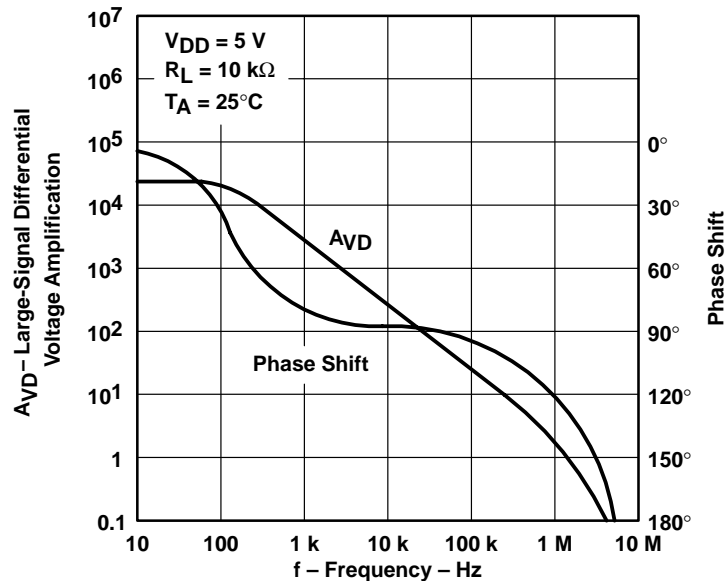


Figure 28

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)†

LARGE-SCALE DIFFERENTIAL VOLTAGE  
 AMPLIFICATION AND PHASE SHIFT

vs  
 FREQUENCY

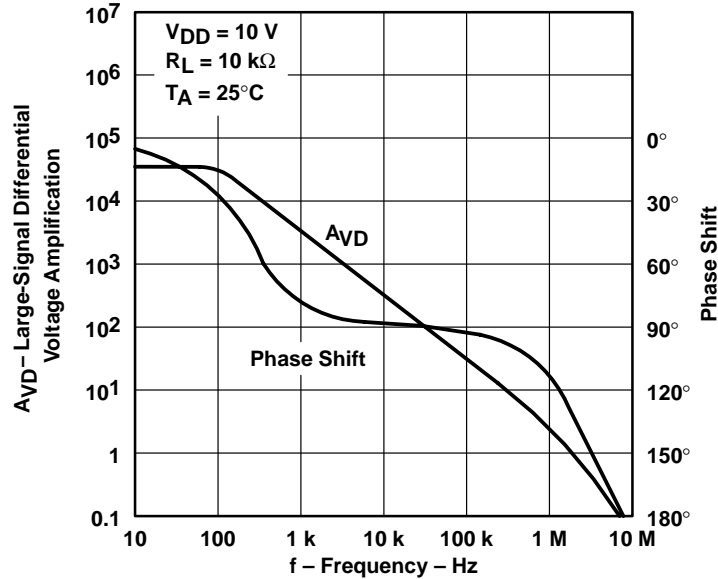


Figure 29

PHASE MARGIN  
 vs  
 SUPPLY VOLTAGE

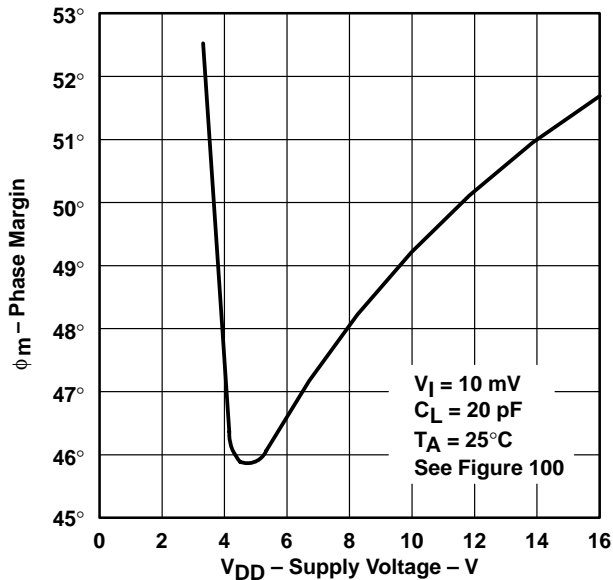


Figure 30

PHASE MARGIN  
 vs  
 FREE-AIR TEMPERATURE

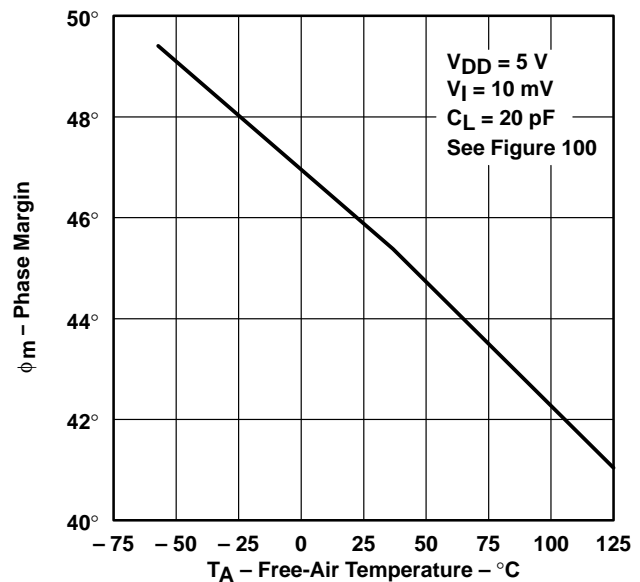


Figure 31

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)†

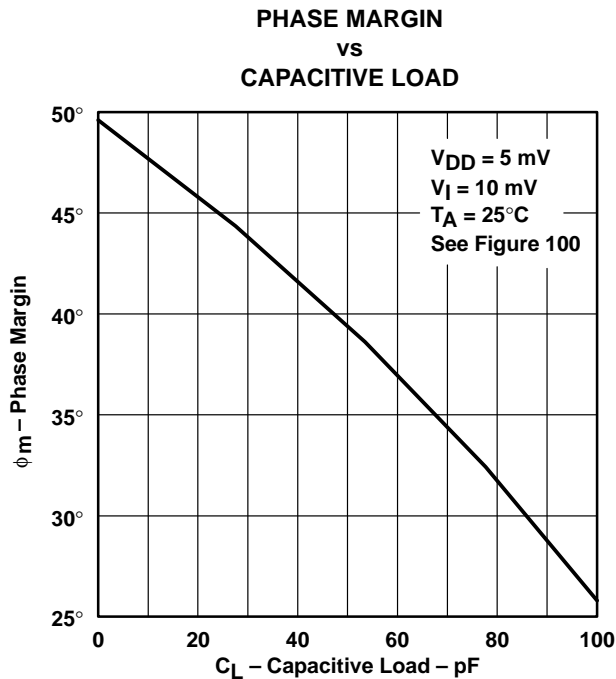


Figure 32

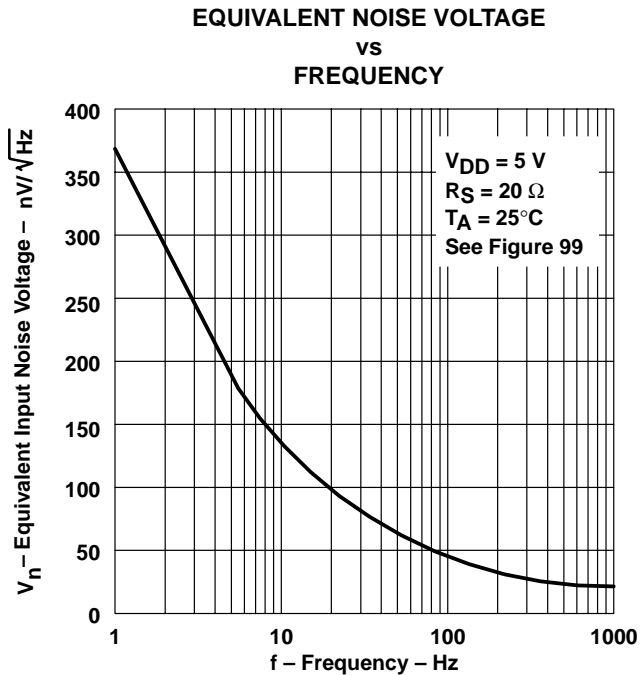


Figure 33

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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**MEDIUM-BIAS MODE**

**electrical characteristics at specified free-air temperature (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	T <sub>A</sub> †	TLC271C, TLC271AC, TLC271BC						UNIT
				V <sub>DD</sub> = 5 V			V <sub>DD</sub> = 10 V			
				MIN	TYP	MAX	MIN	TYP	MAX	
V <sub>IO</sub>	Input offset voltage	V <sub>O</sub> = 1.4 V, V <sub>IC</sub> = 0 R <sub>S</sub> = 50 Ω, R <sub>I</sub> = 100 kΩ	25°C	1.1		10	1.1		10	mV
			Full range			12			12	
			25°C	0.9		5	0.9		5	
			Full range			6.5			6.5	
			25°C	0.25		2	0.26		2	
			Full range			3			3	
α <sub>VIO</sub>	Average temperature coefficient of input offset voltage		25°C to 70°C	1.7			2.1		μV/°C	
I <sub>IO</sub>	Input offset current (see Note 4)	V <sub>O</sub> = V <sub>DD</sub> /2, V <sub>IC</sub> = V <sub>DD</sub> /2	25°C	0.1	60		0.1	60	pA	
			70°C	7	300		7	300		
I <sub>IB</sub>	Input bias current (see Note 4)	V <sub>O</sub> = V <sub>DD</sub> /2, V <sub>IC</sub> = V <sub>DD</sub> /2	25°C	0.6	60		0.7	60	pA	
			70°C	40	600		50	600		
V <sub>ICR</sub>	Common-mode input voltage range (see Note 5)		25°C	-0.2 to 4	-0.3 to 4.2		-0.2 to 9	-0.3 to 9.2	V	
			Full range	-0.2 to 3.5			-0.2 to 8.5		V	
V <sub>OH</sub>	High-level output voltage	V <sub>ID</sub> = 100 mV, R <sub>L</sub> = 100 kΩ	25°C	3.2	3.9		8	8.7	V	
			0°C	3	3.9		7.8	8.7		
			70°C	3	4		7.8	8.7		
V <sub>OL</sub>	Low-level output voltage	V <sub>ID</sub> = -100 mV, I <sub>OL</sub> = 0	25°C		0	50		0	50	mV
			0°C		0	50		0	50	
			70°C		0	50		0	50	
A <sub>VD</sub>	Large-signal differential voltage amplification	R <sub>L</sub> = 100 kΩ, See Note 6	25°C	25	170		25	275	V/mV	
			0°C	15	200		15	320		
			70°C	15	140		15	230		
CMRR	Common-mode rejection ratio	V <sub>IC</sub> = V <sub>ICRmin</sub>	25°C	65	91		65	94	dB	
			0°C	60	91		60	94		
			70°C	60	92		60	94		
k <sub>SVR</sub>	Supply-voltage rejection ratio (ΔV <sub>DD</sub> /ΔV <sub>IO</sub> )	V <sub>DD</sub> = 5 V to 10 V V <sub>O</sub> = 1.4 V	25°C	70	93		70	93	dB	
			0°C	60	92		60	92		
			70°C	60	94		60	94		
I <sub>I(SEL)</sub>	Input current (BIAS SELECT)	V <sub>I(SEL)</sub> = V <sub>DD</sub> /2	25°C	-130			-160		nA	
I <sub>DD</sub>	Supply current	V <sub>O</sub> = V <sub>DD</sub> /2, V <sub>IC</sub> = V <sub>DD</sub> /2, No load	25°C	105	280		143	300	μA	
			0°C	125	320		173	400		
			70°C	85	220		110	280		

† Full range is 0°C to 70°C.

- NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.  
5. This range also applies to each input individually.  
6. At V<sub>DD</sub> = 5 V, V<sub>O</sub> = 0.25 V to 2 V; at V<sub>DD</sub> = 10 V, V<sub>O</sub> = 1 V to 6 V.



**MEDIUM-BIAS MODE**

**electrical characteristics at specified free-air temperature (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	T <sub>A</sub> †	TLC271I, TLC271AI, TLC271BI						UNIT
				V <sub>DD</sub> = 5 V			V <sub>DD</sub> = 10 V			
				MIN	TYP	MAX	MIN	TYP	MAX	
V <sub>IO</sub>	Input offset voltage	V <sub>O</sub> = 1.4 V, V <sub>IC</sub> = 0 V, R <sub>S</sub> = 50 Ω, R <sub>L</sub> = 100 kΩ	25°C	1.1		10	1.1		10	mV
			Full range			13			13	
			25°C	0.9		5	0.9		5	
			Full range			7			7	
			25°C	0.25		2	0.26		2	
			Full range			3.5			3.5	
α <sub>VIO</sub>	Average temperature coefficient of input offset voltage		25°C to 85°C	1.7			2.1		μV/°C	
I <sub>IO</sub>	Input offset current (see Note 4)	V <sub>O</sub> = V <sub>DD</sub> /2, V <sub>IC</sub> = V <sub>DD</sub> /2	25°C	0.1	60	0.1	60	pA		
			85°C	24	1000	26	1000			
I <sub>IB</sub>	Input bias current (see Note 4)	V <sub>O</sub> = V <sub>DD</sub> /2, V <sub>IC</sub> = V <sub>DD</sub> /2	25°C	0.6	60	0.7	60	pA		
			85°C	200	2000	220	2000			
V <sub>ICR</sub>	Common-mode input voltage range (see Note 5)		25°C	-0.2 to 4	-0.3 to 4.2	-0.2 to 9	-0.3 to 9.2	V		
			Full range	-0.2 to 3.5		-0.2 to 8.5		V		
V <sub>OH</sub>	High-level output voltage	V <sub>ID</sub> = 100 mV, R <sub>L</sub> = 100 kΩ	25°C	3.2	3.9	8	8.7	V		
			-40°C	3	3.9	7.8	8.7			
			85°C	3	4	7.8	8.7			
V <sub>OL</sub>	Low-level output voltage	V <sub>ID</sub> = -100 mV, I <sub>OL</sub> = 0	25°C	0	50	0	50	mV		
			-40°C	0	50	0	50			
			85°C	0	50	0	50			
A <sub>VD</sub>	Large-signal differential voltage amplification	R <sub>L</sub> = 100 kΩ, See Note 6	25°C	25	170	25	275	V/mV		
			-40°C	15	270	15	390			
			85°C	15	130	15	220			
CMRR	Common-mode rejection ratio	V <sub>IC</sub> = V <sub>ICRmin</sub>	25°C	65	91	65	94	dB		
			-40°C	60	90	60	93			
			85°C	60	90	60	94			
k <sub>SVR</sub>	Supply-voltage rejection ratio (ΔV <sub>DD</sub> /ΔV <sub>IO</sub> )	V <sub>DD</sub> = 5 V to 10 V V <sub>O</sub> = 1.4 V	25°C	70	93	70	93	dB		
			-40°C	60	91	60	91			
			85°C	60	94	60	94			
I <sub>I(SEL)</sub>	Input current (BIAS SELECT)	V <sub>I(SEL)</sub> = V <sub>DD</sub> /2	25°C	-130		-160		nA		
I <sub>DD</sub>	Supply current	V <sub>O</sub> = V <sub>DD</sub> /2, V <sub>IC</sub> = V <sub>DD</sub> /2, No load	25°C	105	280	143	300	μA		
			-40°C	158	400	225	450			
			85°C	80	200	103	260			

† Full range is -40°C to 85°C.

- NOTES:
4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
  5. This range also applies to each input individually.
  6. At V<sub>DD</sub> = 5 V, V<sub>O</sub> = 0.25 V to 2 V; at V<sub>DD</sub> = 10 V, V<sub>O</sub> = 1 V to 6 V.

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**MEDIUM-BIAS MODE**

**electrical characteristics at specified free-air temperature (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	T <sub>A</sub> †	TLC271M						UNIT
			V <sub>DD</sub> = 5 V			V <sub>DD</sub> = 10 V			
			MIN	TYP	MAX	MIN	TYP	MAX	
V <sub>IO</sub> Input offset voltage	V <sub>O</sub> = 1.4 V, V <sub>IC</sub> = 0 V, R <sub>S</sub> = 50 Ω, R <sub>L</sub> = 100 kΩ	25°C		1.1	10		1.1	10	mV
		Full range				12		12	
α <sub>VIO</sub> Average temperature coefficient of input offset voltage		25°C to 125°C		1.7			2.1		μV/°C
I <sub>IO</sub> Input offset current (see Note 4)	V <sub>O</sub> = V <sub>DD</sub> /2, V <sub>IC</sub> = V <sub>DD</sub> /2	25°C		0.1	60		0.1	60	pA
		125°C		1.4	15		1.8	15	nA
I <sub>IB</sub> Input bias current (see Note 4)	V <sub>O</sub> = V <sub>DD</sub> /2, V <sub>IC</sub> = V <sub>DD</sub> /2	25°C		0.6	60		0.7	60	pA
		125°C		9	35		10	35	nA
V <sub>ICR</sub> Common-mode input voltage range (see Note 5)		25°C	0 to 4	-0.3 to 4.2		0 to 9	-0.3 to 9.2		V
		Full range	0 to 3.5			0 to 8.5			V
V <sub>OH</sub> High-level output voltage	V <sub>ID</sub> = 100 mV, R <sub>L</sub> = 100 kΩ	25°C	3.2	3.9		8	8.7		V
		-55°C	3	3.9		7.8	8.6		
		125°C	3	4		7.8	8.6		
V <sub>OL</sub> Low-level output voltage	V <sub>ID</sub> = -100 mV, I <sub>OL</sub> = 0	25°C		0	50		0	50	mV
		-55°C		0	50		0	50	
		125°C		0	50		0	50	
A <sub>VD</sub> Large-signal differential voltage amplification	R <sub>L</sub> = 10 kΩ See Note 6	25°C	25	170		25	275		V/mV
		-55°C	15	290		15	420		
		125°C	15	120		15	190		
CMRR Common-mode rejection ratio	V <sub>IC</sub> = V <sub>ICRmin</sub>	25°C	65	91		65	94		dB
		-55°C	60	89		60	93		
		125°C	60	91		60	93		
k <sub>SVR</sub> Supply-voltage rejection ratio (ΔV <sub>DD</sub> /ΔV <sub>IO</sub> )	V <sub>DD</sub> = 5 V to 10 V V <sub>O</sub> = 1.4 V	25°C	70	93		70	93		dB
		-55°C	60	91		60	91		
		125°C	60	94		60	94		
I <sub>I(SEL)</sub> Input current (BIAS SELECT)	V <sub>I(SEL)</sub> = V <sub>DD</sub> /2	25°C		-130		-160		nA	
I <sub>DD</sub> Supply current	V <sub>O</sub> = V <sub>DD</sub> /2, V <sub>IC</sub> = V <sub>DD</sub> /2, No load	25°C		105	280		143	300	μA
		-55°C		170	440		245	500	
		125°C		70	180		90	240	

† Full range is -55°C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually.

6. At V<sub>DD</sub> = 5 V, V<sub>O</sub> = 0.25 V to 2 V; at V<sub>DD</sub> = 10 V, V<sub>O</sub> = 1 V to 6 V.





**MEDIUM-BIAS MODE**

**operating characteristics at specified free-air temperature,  $V_{DD} = 5\text{ V}$**

PARAMETER	TEST CONDITIONS	$T_A$	TLC271C, TLC271AC, TLC271BC			UNIT
			MIN	TYP	MAX	
SR      Slew rate at unity gain	$R_L = 100\text{ k}\Omega$ , $C_L = 20\text{ pF}$ , See Figure 98	$V_{I(PP)} = 1\text{ V}$	25°C	0.43		V/ $\mu$ s
			0°C	0.46		
			70°C	0.36		
		$V_{I(PP)} = 2.5\text{ V}$	25°C	0.40		
			0°C	0.43		
			70°C	0.34		
$V_n$ Equivalent input noise voltage	$f = 1\text{ kHz}$ , See Figure 99	$R_S = 20\ \Omega$	25°C	32		nV/ $\sqrt{\text{Hz}}$
$B_{OM}$ Maximum output-swing bandwidth	$V_O = V_{OH}$ , $R_L = 100\text{ k}\Omega$ , See Figure 98	$C_L = 20\text{ pF}$ , See Figure 98	25°C	55		kHz
			0°C	60		
			70°C	50		
$B_1$ Unity-gain bandwidth	$V_I = 10\text{ mV}$ , See Figure 100	$C_L = 20\text{ pF}$ ,	25°C	525		kHz
			0°C	600		
			70°C	400		
$\phi_m$ Phase margin	$V_I = 10\text{ mV}$ , $C_L = 20\text{ pF}$ ,	$f = B_1$ , See Figure 100	25°C	40°		
			0°C	41°		
			70°C	39°		

**operating characteristics at specified free-air temperature,  $V_{DD} = 10\text{ V}$**

PARAMETER	TEST CONDITIONS	$T_A$	TLC271C, TLC271AC, TLC271BC			UNIT
			MIN	TYP	MAX	
SR      Slew rate at unity gain	$R_L = 100\text{ k}\Omega$ , $C_L = 20\text{ pF}$ , See Figure 98	$V_{I(PP)} = 1\text{ V}$	25°C	0.62		V/ $\mu$ s
			0°C	0.67		
			70°C	0.51		
		$V_{I(PP)} = 5.5\text{ V}$	25°C	0.56		
			0°C	0.61		
			70°C	0.46		
$V_n$ Equivalent input noise voltage	$f = 1\text{ kHz}$ , See Figure 99	$R_S = 20\ \Omega$	25°C	32		nV/ $\sqrt{\text{Hz}}$
$B_{OM}$ Maximum output-swing bandwidth	$V_O = V_{OH}$ , $R_L = 100\text{ k}\Omega$ , See Figure 98	$C_L = 20\text{ pF}$ , See Figure 98	25°C	35		kHz
			0°C	40		
			70°C	30		
$B_1$ Unity-gain bandwidth	$V_I = 10\text{ mV}$ , See Figure 100	$C_L = 20\text{ pF}$ ,	25°C	635		kHz
			0°C	710		
			70°C	510		
$\phi_m$ Phase margin	$V_I = 10\text{ mV}$ , $C_L = 20\text{ pF}$ ,	$f = B_1$ , See Figure 100	25°C	43°		
			0°C	44°		
			70°C	42°		

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**MEDIUM-BIAS MODE**

operating characteristics at specified free-air temperature,  $V_{DD} = 5\text{ V}$

PARAMETER	TEST CONDITIONS	$T_A$	TLC271I, TLC271AI, TLC271BI			UNIT
			MIN	TYP	MAX	
SR Slew rate at unity gain	$R_L = 100\text{ k}\Omega$ , $C_L = 20\text{ pF}$ , See Figure 98	$V_{I(PP)} = 1\text{ V}$	25°C	0.43		V/ $\mu$ s
			-40°C	0.51		
			85°C	0.35		
		$V_{I(PP)} = 2.5\text{ V}$	25°C	0.40		
			-40°C	0.48		
			85°C	0.32		
$V_n$ Equivalent input noise voltage	$f = 1\text{ kHz}$ , See Figure 99	$R_S = 20\ \Omega$ , 25°C	32		nV/ $\sqrt{\text{Hz}}$	
$B_{OM}$ Maximum output-swing bandwidth	$V_O = V_{OH}$ , $R_L = 100\text{ k}\Omega$ , See Figure 98	$C_L = 20\text{ pF}$ , See Figure 98	25°C	55		kHz
			-40°C	75		
			85°C	45		
$B_1$ Unity-gain bandwidth	$V_I = 10\text{ mV}$ , See Figure 100	$C_L = 20\text{ pF}$ ,	25°C	525		MHz
			-40°C	770		
			85°C	370		
$\phi_m$ Phase margin	$V_I = 10\text{ mV}$ , $C_L = 20\text{ pF}$ ,	$f = B_1$ , See Figure 100	25°C	40°		
			-40°C	43°		
			85°C	38°		

operating characteristics at specified free-air temperature,  $V_{DD} = 10\text{ V}$

PARAMETER	TEST CONDITIONS	$T_A$	TLC271I, TLC271AI, TLC271BI			UNIT
			MIN	TYP	MAX	
SR Slew rate at unity gain	$R_L = 100\text{ k}\Omega$ , $C_L = 20\text{ pF}$ , See Figure 98	$V_{I(PP)} = 1\text{ V}$	25°C	0.62		V/ $\mu$ s
			-40°C	0.77		
			85°C	0.47		
		$V_{I(PP)} = 5.5\text{ V}$	25°C	0.56		
			-40°C	0.70		
			85°C	0.44		
$V_n$ Equivalent input noise voltage	$f = 1\text{ kHz}$ , See Figure 99	$R_S = 20\ \Omega$ , 25°C	32		nV/ $\sqrt{\text{Hz}}$	
$B_{OM}$ Maximum output-swing bandwidth	$V_O = V_{OH,3}$ , $R_L = 100\text{ k}\Omega$ , See Figure 98	$C_L = 20\text{ pF}$ , See Figure 98	25°C	35		kHz
			-40°C	45		
			85°C	25		
$B_1$ Unity-gain bandwidth	$V_I = 10\text{ mV}$ , See Figure 100	$C_L = 20\text{ pF}$ ,	25°C	635		kHz
			-40°C	880		
			85°C	480		
$\phi_m$ Phase margin	$V_I = 10\text{ mV}$ , $C_L = 20\text{ pF}$ ,	$f = B_1$ , See Figure 100	25°C	43°		
			-40°C	46°		
			85°C	41°		



**MEDIUM-BIAS MODE**

**operating characteristics at specified free-air temperature,  $V_{DD} = 5\text{ V}$**

PARAMETER	TEST CONDITIONS	$T_A$	TLC271M			UNIT
			MIN	TYP	MAX	
SR    Slew rate at unity gain	$R_L = 100\text{ k}\Omega$ , $C_L = 20\text{ pF}$ , See Figure 98	$V_{I(PP)} = 1\text{ V}$	25°C	0.43		V/ $\mu$ s
			-55°C	0.54		
			125°C	0.29		
		$V_{I(PP)} = 2.5\text{ V}$	25°C	0.40		
			-55°C	0.50		
			125°C	0.28		
$V_n$ Equivalent input noise voltage	$f = 1\text{ kHz}$ , See Figure 99	$R_S = 20\ \Omega$ , 25°C	32		nV/ $\sqrt{\text{Hz}}$	
$B_{OM}$ Maximum output-swing bandwidth	$V_O = V_{OH}$ , $R_L = 100\text{ k}\Omega$ , See Figure 98	$C_L = 20\text{ pF}$ , See Figure 98	25°C	55		kHz
			-55°C	80		
			125°C	40		
$B_1$ Unity-gain bandwidth	$V_I = 10\text{ mV}$ , See Figure 100	$C_L = 20\text{ pF}$ ,	25°C	525		kHz
			-55°C	850		
			125°C	330		
$\phi_m$ Phase margin	$V_I = 10\text{ mV}$ , $C_L = 20\text{ pF}$ ,	$f = B_1$ , See Figure 100	25°C	40°		
			-55°C	43°		
			125°C	36°		

**operating characteristics at specified free-air temperature,  $V_{DD} = 10\text{ V}$**

PARAMETER	TEST CONDITIONS	$T_A$	TLC271M			UNIT
			MIN	TYP	MAX	
SR    Slew rate at unity gain	$R_L = 100\text{ k}\Omega$ , $C_L = 20\text{ pF}$ , See Figure 98	$V_{I(PP)} = 1\text{ V}$	25°C	0.62		V/ $\mu$ s
			-55°C	0.81		
			125°C	0.38		
		$V_{I(PP)} = 5.5\text{ V}$	25°C	0.56		
			-55°C	0.73		
			125°C	0.35		
$V_n$ Equivalent input noise voltage	$f = 1\text{ kHz}$ , See Figure 99	$R_S = 20\ \Omega$ , 25°C	32		nV/ $\sqrt{\text{Hz}}$	
$B_{OM}$ Maximum output-swing bandwidth	$V_O = V_{OH}$ , $R_L = 100\text{ k}\Omega$ , See Figure 98	$C_L = 20\text{ pF}$ , See Figure 98	25°C	35		kHz
			-55°C	50		
			125°C	20		
$B_1$ Unity-gain bandwidth	$V_I = 10\text{ mV}$ , See Figure 100	$C_L = 20\text{ pF}$ ,	25°C	635		kHz
			-55°C	960		
			125°C	440		
$\phi_m$ Phase margin	$V_I = 10\text{ mV}$ , $C_L = 20\text{ pF}$ ,	$f = B_1$ , See Figure 100	25°C	43°		
			-55°C	47°		
			125°C	39°		

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**TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)**

**Table of Graphs**

		<b>FIGURE</b>	
$V_{IO}$	Input offset voltage	Distribution	34, 35
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$V_{OL}$	Low-level output voltage	vs Common-mode input voltage	42, 43
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$I_{IO}$	Input offset current	vs Free-air temperature	50
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$I_{DD}$	Supply current	vs Supply voltage	52
		vs Free-air temperature	53
SR	Slew rate	vs Supply voltage	54
		vs Free-air temperature	55
	Bias-select current	vs Supply voltage	56
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	57
$B_1$	Unity-gain bandwidth	vs Free-air temperature	58
		vs Supply voltage	59
$\phi_m$	Phase margin	vs Supply voltage	62
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		vs Capacitive load	64
$V_n$	Equivalent input noise voltage	vs Frequency	65
		Phase shift	60, 61



TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)†

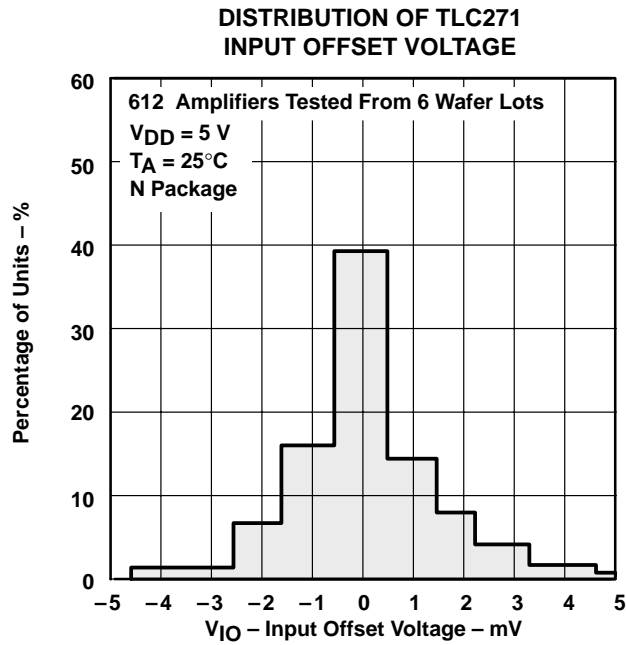


Figure 34

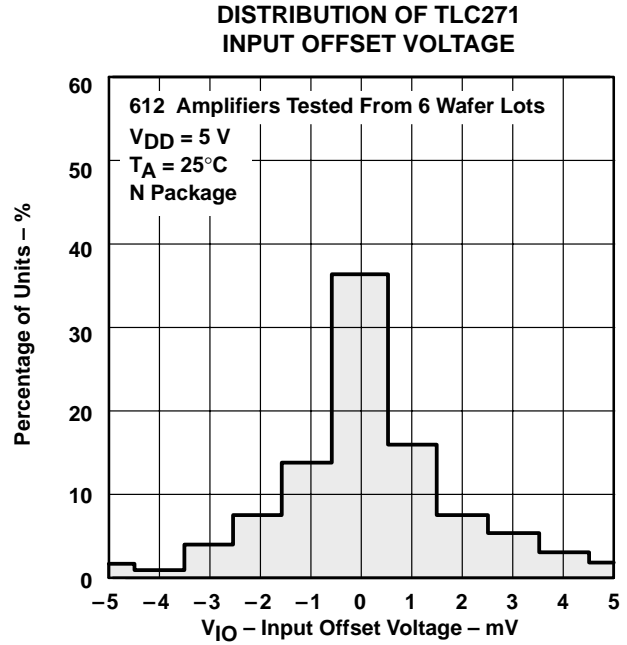


Figure 35

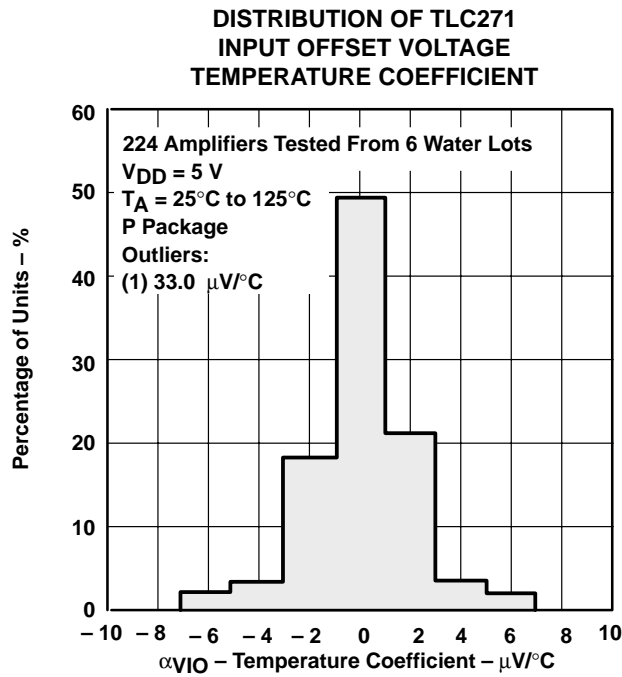


Figure 36

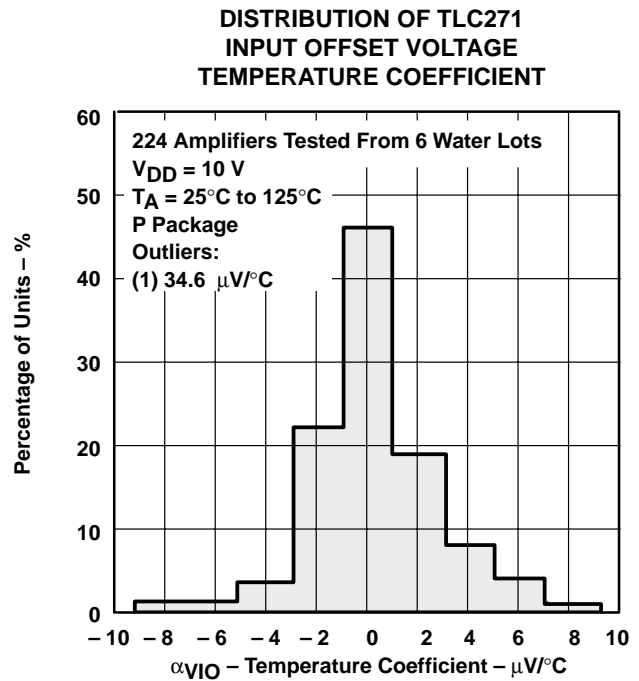


Figure 37

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

**TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)†**

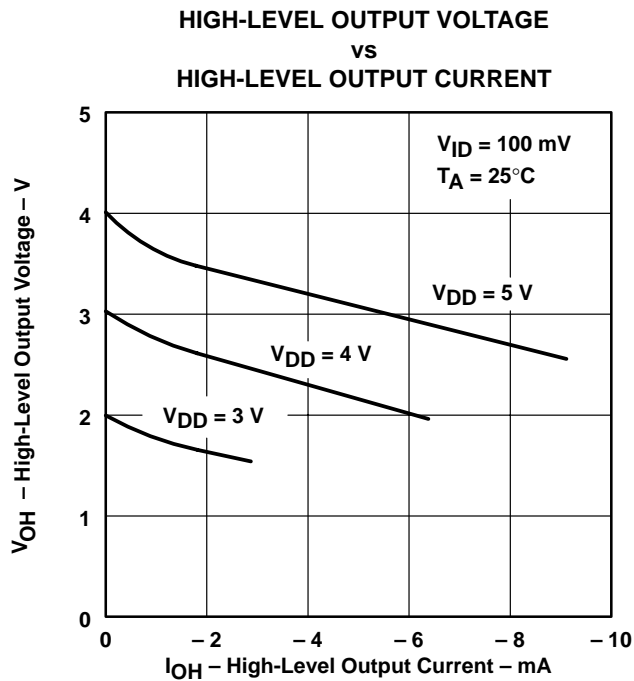


Figure 38

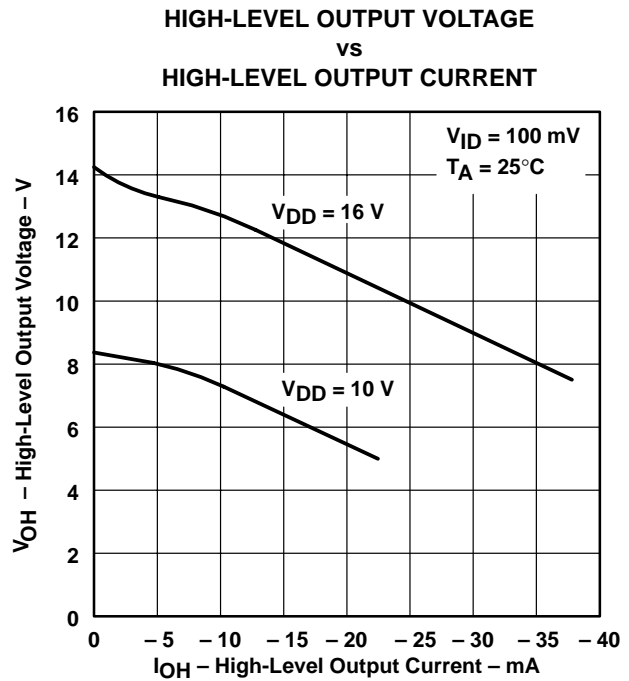


Figure 39

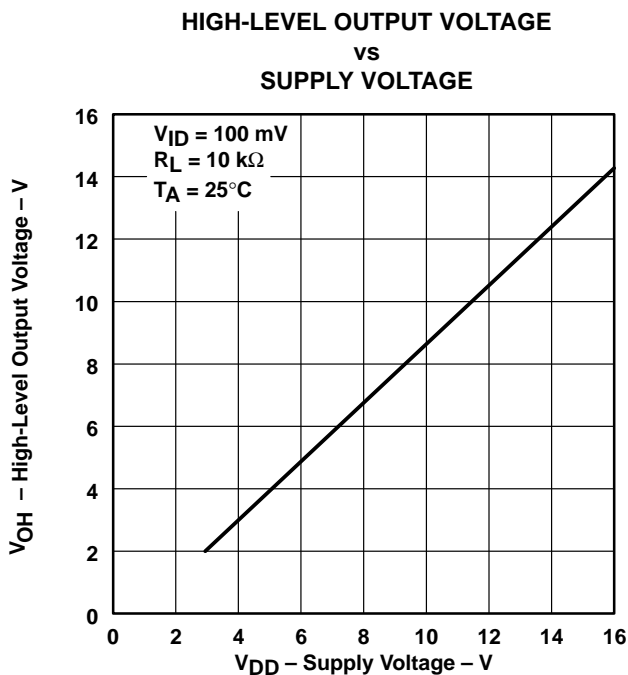


Figure 40

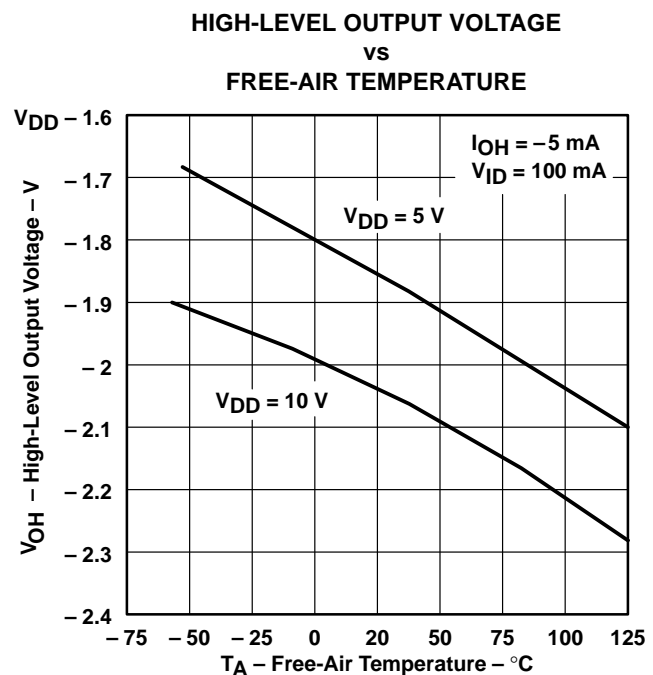


Figure 41

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)†

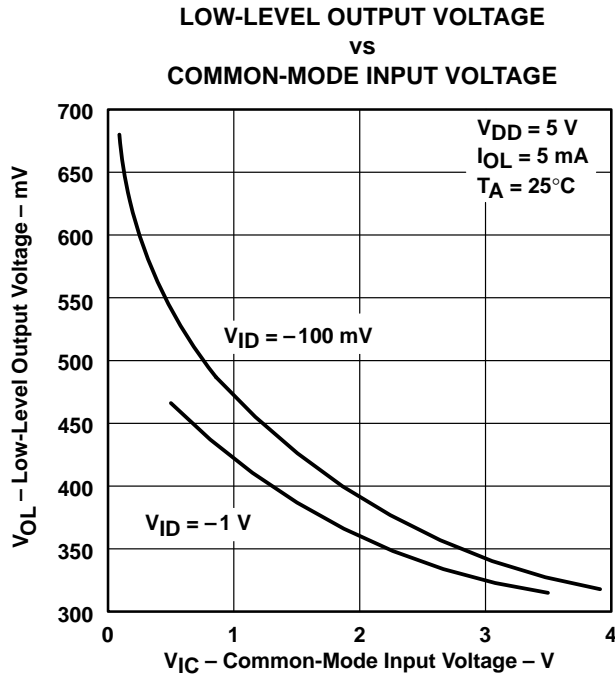


Figure 42

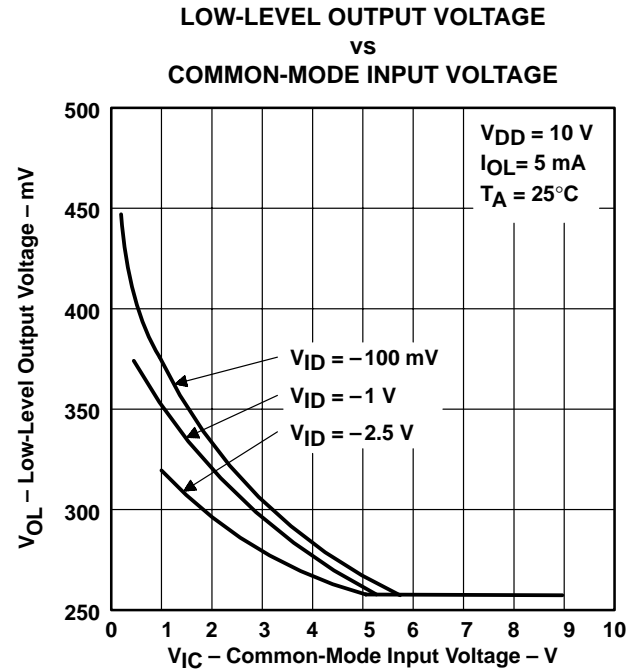


Figure 43

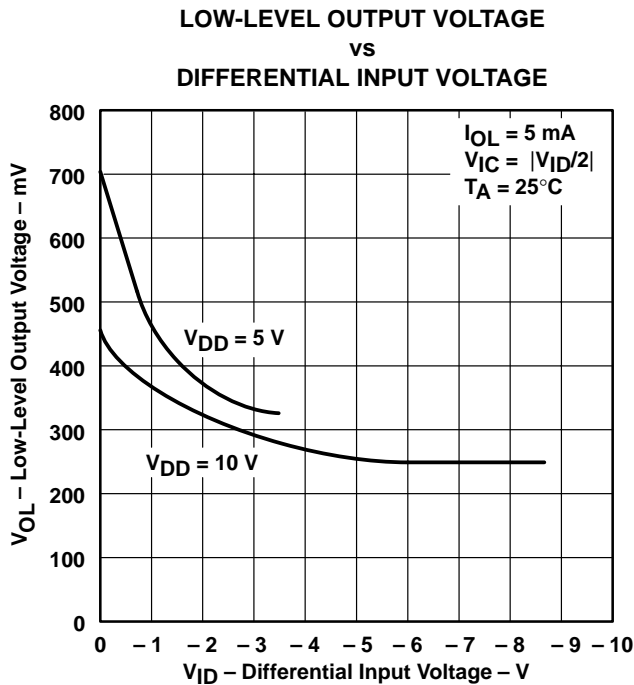


Figure 44

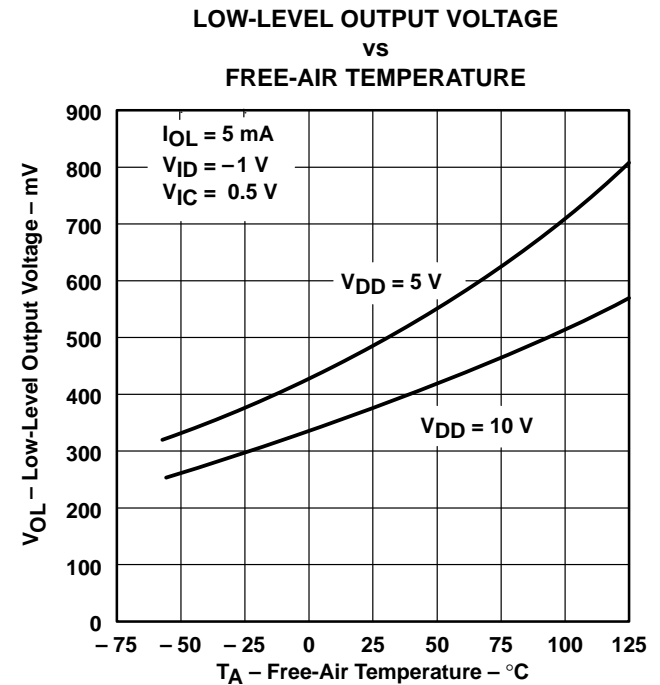
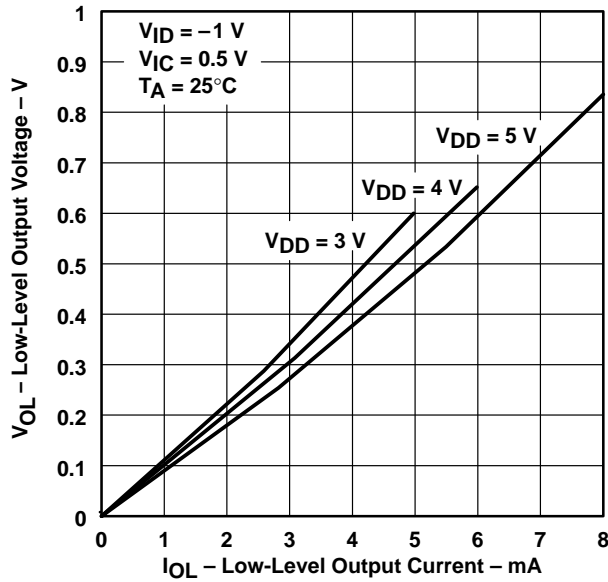


Figure 45

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

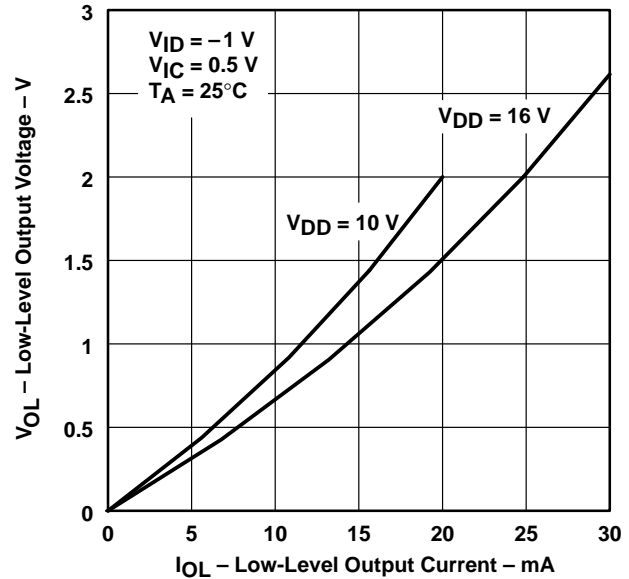
**TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)†**

**LOW-LEVEL OUTPUT VOLTAGE  
 vs  
 LOW-LEVEL OUTPUT CURRENT**



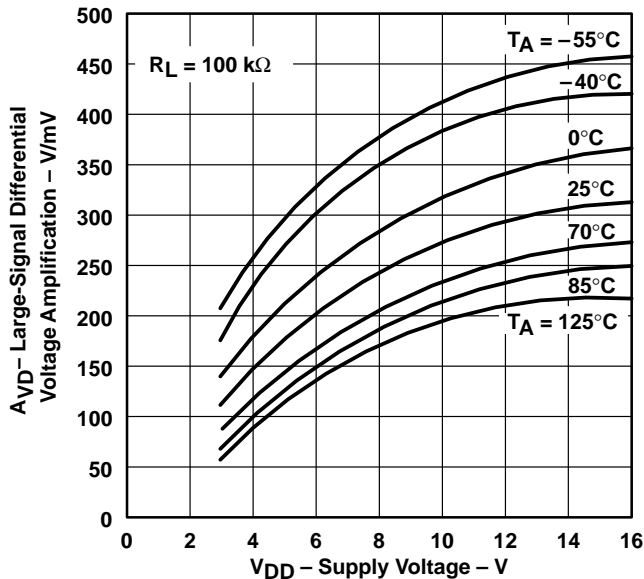
**Figure 46**

**LOW-LEVEL OUTPUT VOLTAGE  
 vs  
 LOW-LEVEL OUTPUT CURRENT**



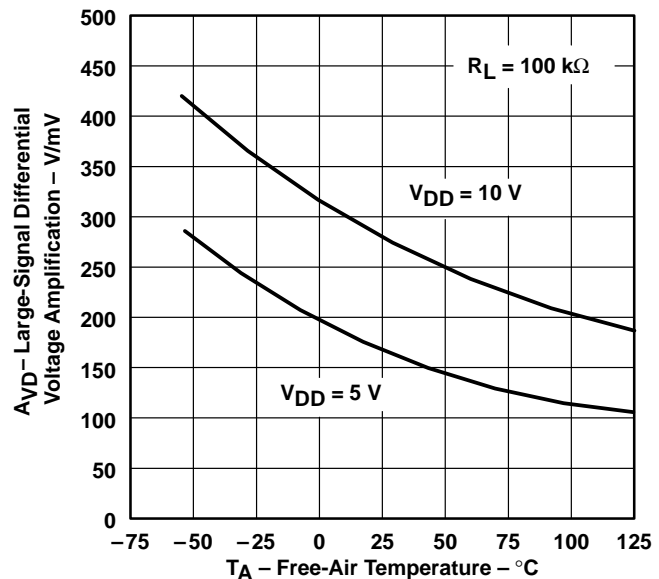
**Figure 47**

**LARGE-SIGNAL  
 DIFFERENTIAL VOLTAGE AMPLIFICATION  
 vs  
 SUPPLY VOLTAGE**



**Figure 48**

**LARGE-SIGNAL  
 DIFFERENTIAL VOLTAGE AMPLIFICATION  
 vs  
 FREE-AIR TEMPERATURE**

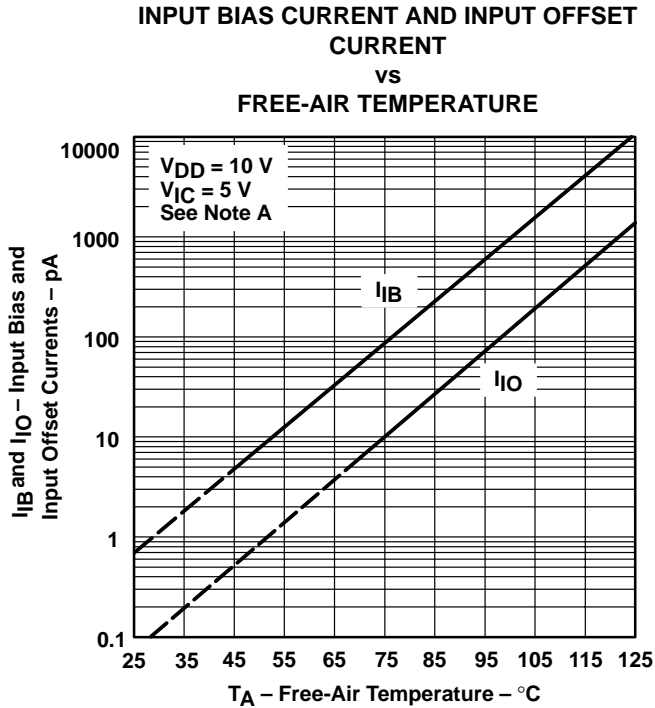


**Figure 49**

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.



TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)†



NOTE A: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

Figure 50

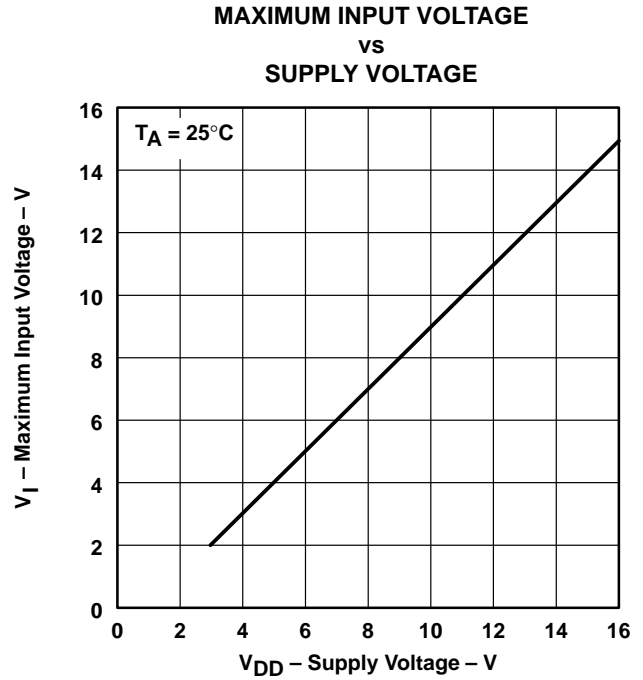


Figure 51

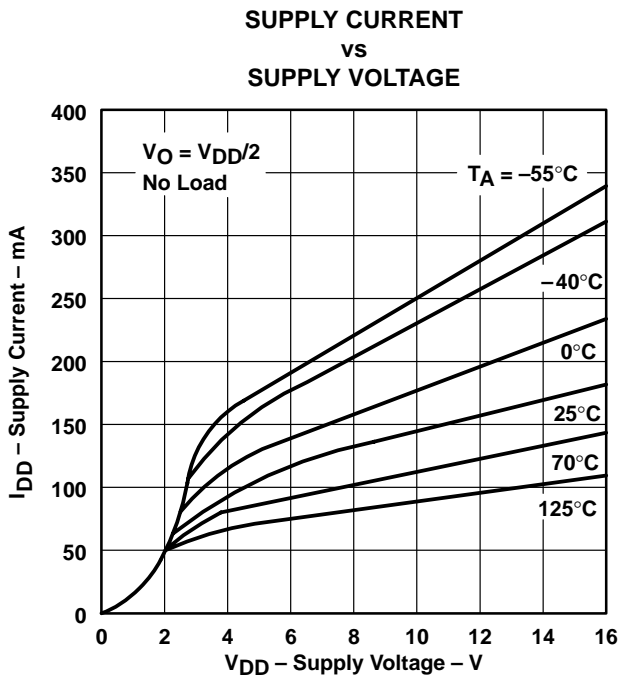


Figure 52

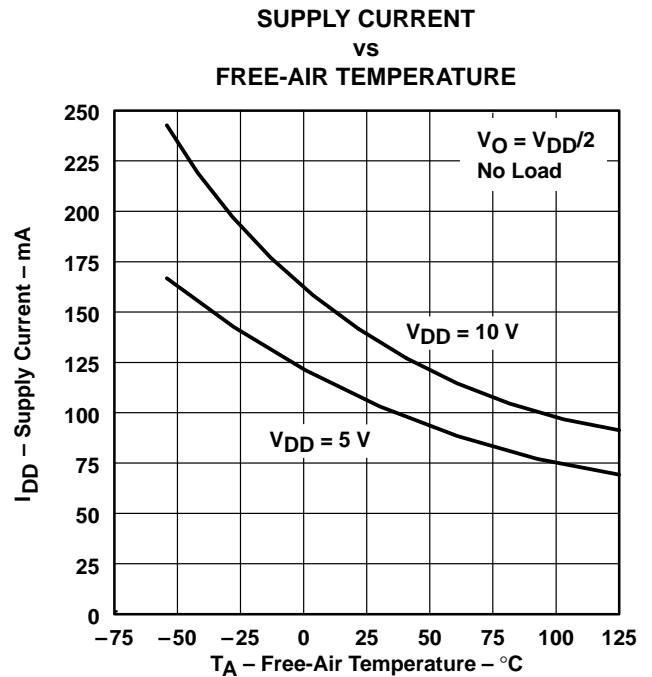
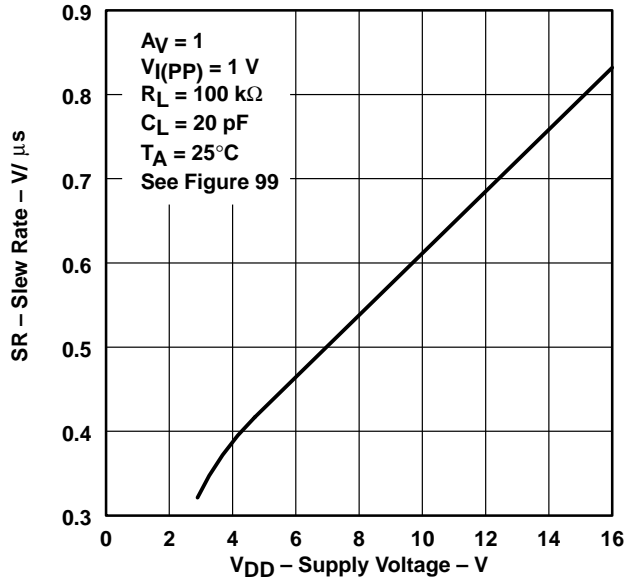


Figure 53

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

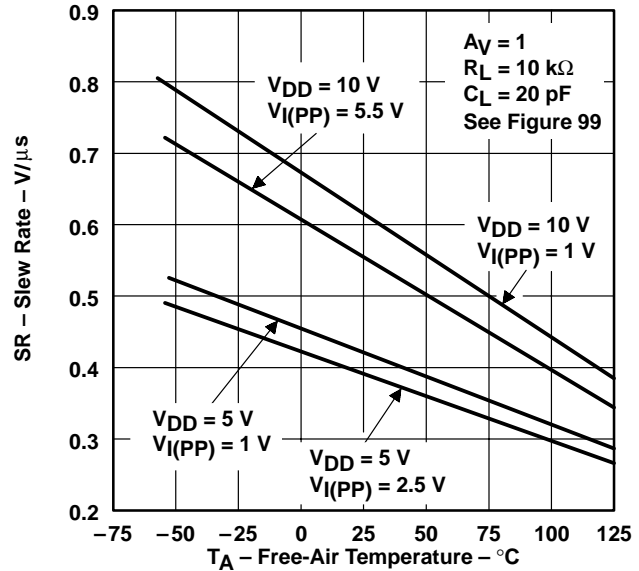
**TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)†**

**SLEW RATE  
 vs  
 SUPPLY VOLTAGE**



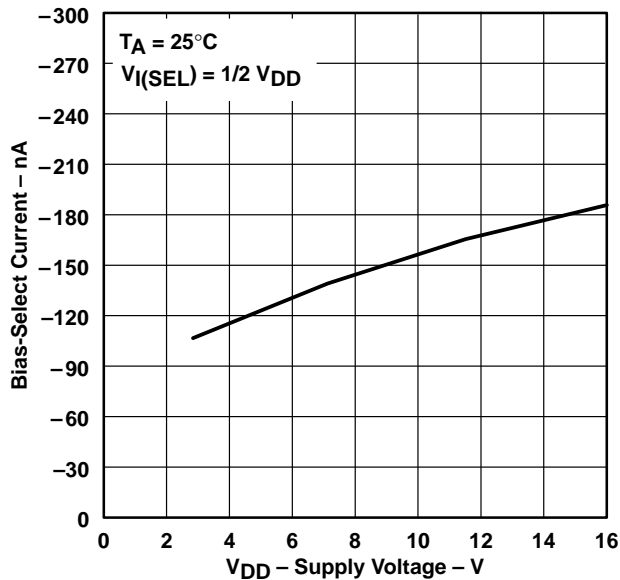
**Figure 54**

**SLEW RATE  
 vs  
 FREE-AIR TEMPERATURE**



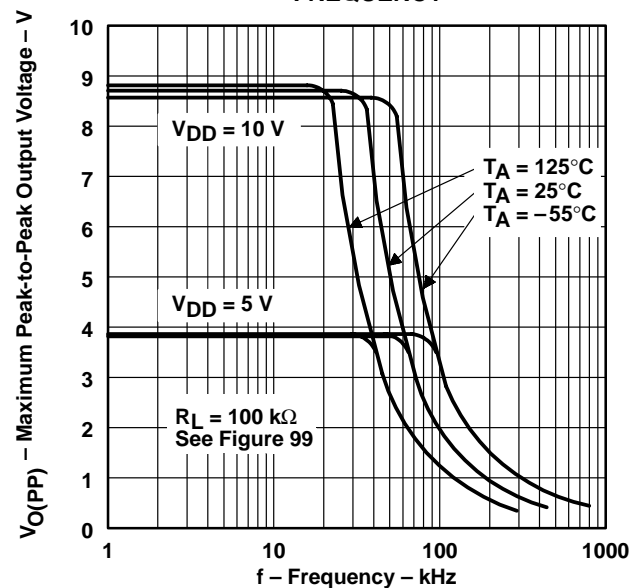
**Figure 55**

**BIAS-SELECT CURRENT  
 vs  
 SUPPLY VOLTAGE**



**Figure 56**

**MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE  
 vs  
 FREQUENCY**



**Figure 57**

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)†

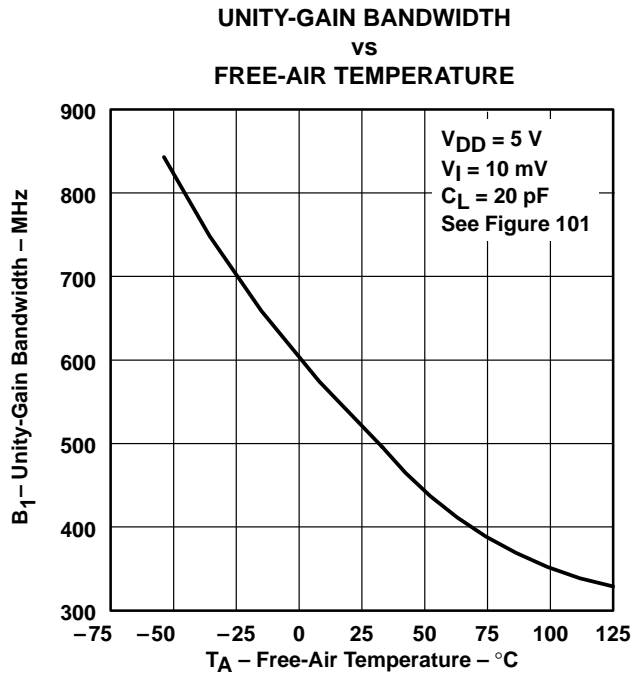


Figure 58

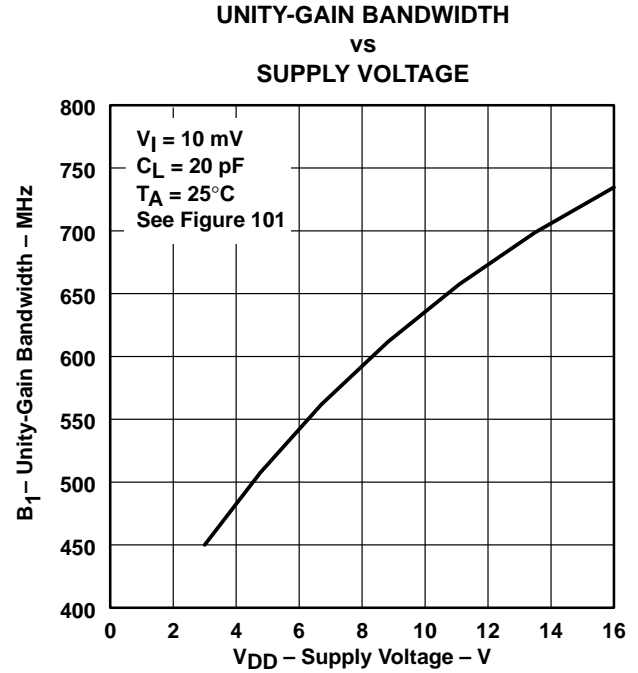


Figure 59

**LARGE-SIGNAL DIFFERENTIAL VOLTAGE  
 AMPLIFICATION AND PHASE SHIFT  
 vs  
 FREQUENCY**

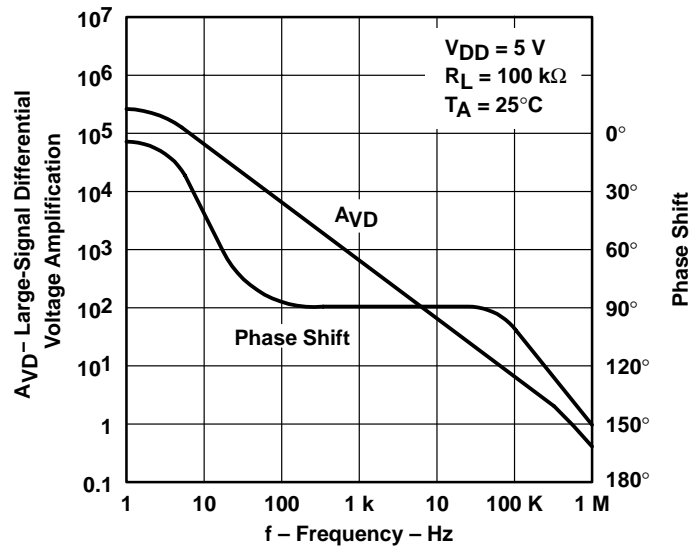


Figure 60

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

**TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)†**

**LARGE-SIGNAL DIFFERENTIAL VOLTAGE  
 AMPLIFICATION AND PHASE SHIFT  
 vs  
 FREQUENCY**

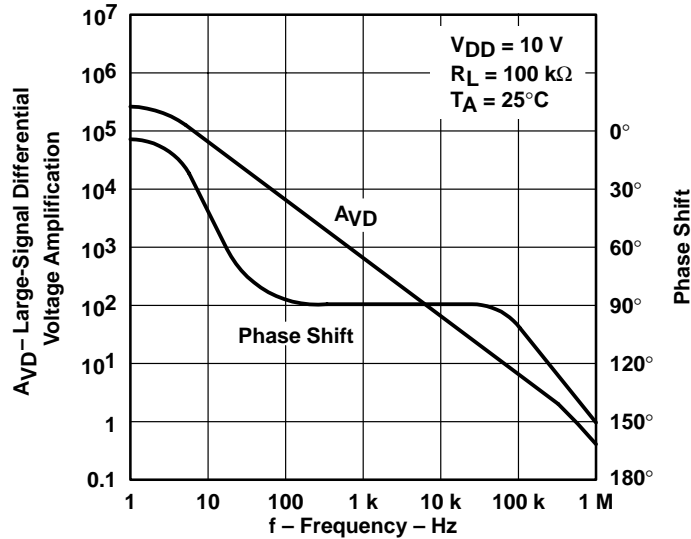


Figure 61

**PHASE MARGIN  
 vs  
 SUPPLY VOLTAGE**

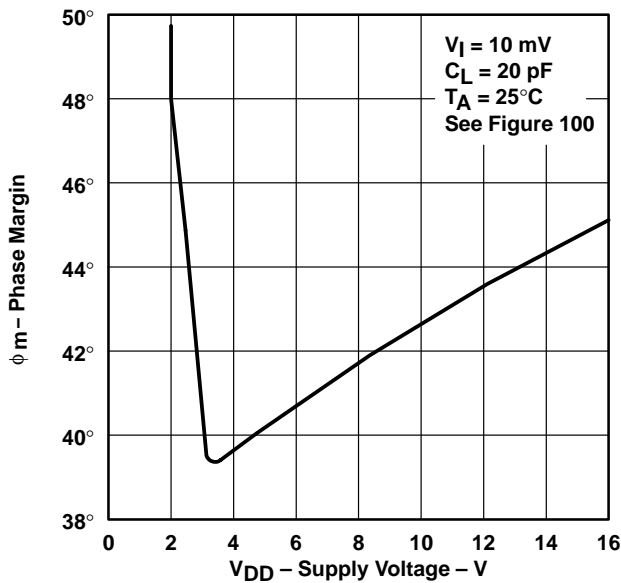


Figure 62

**PHASE MARGIN  
 vs  
 FREE-AIR TEMPERATURE**

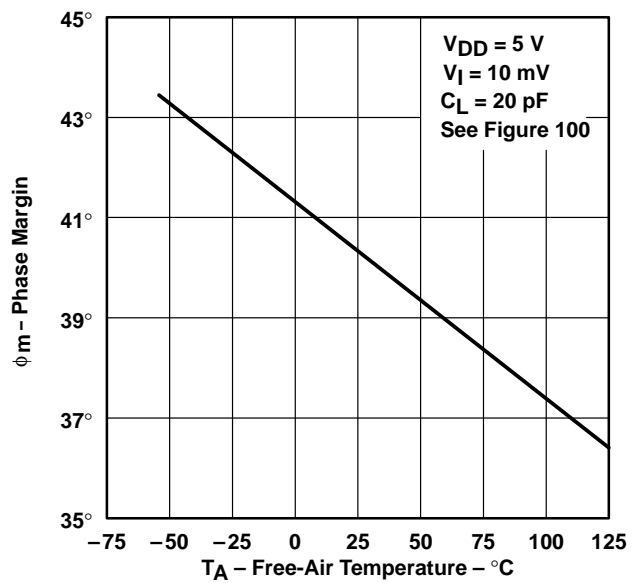


Figure 63

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)†

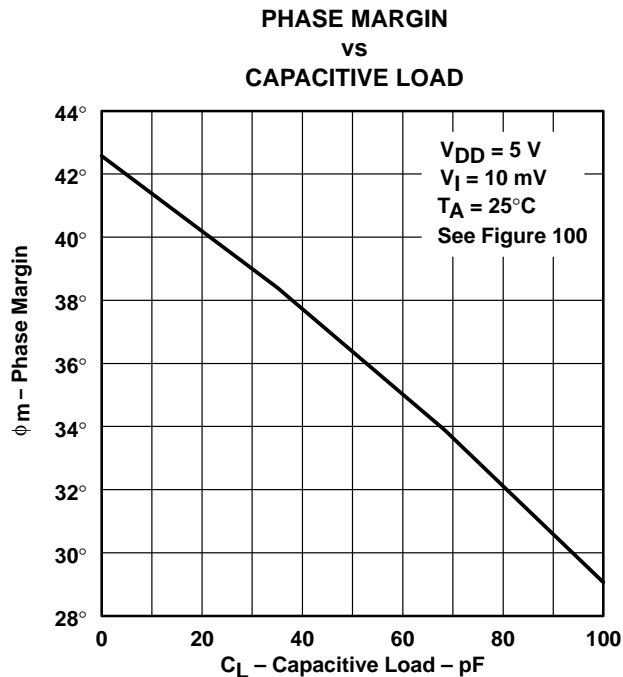


Figure 64

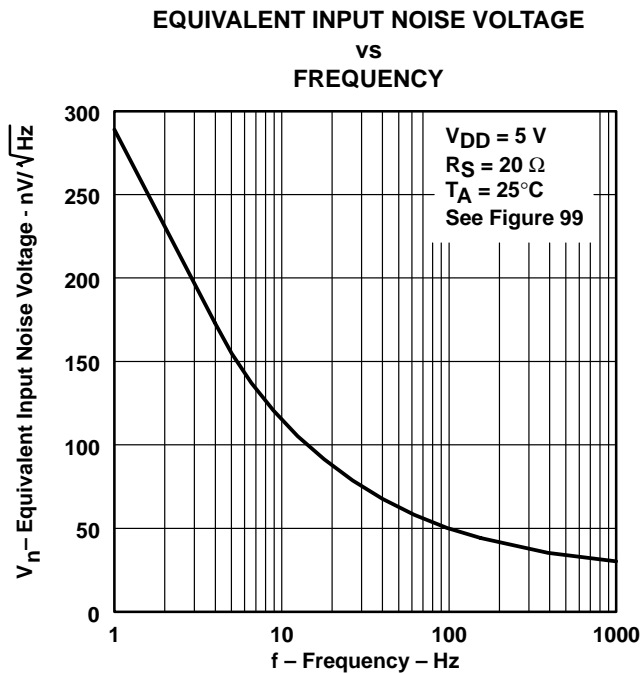


Figure 65

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

**TLC271, TLC271A, TLC271B**  
**LinCMOS™ PROGRAMMABLE LOW-POWER**  
**OPERATIONAL AMPLIFIERS**

SLOS090D – NOVEMBER 1987 – REVISED MARCH 2001

**LOW-BIAS MODE**

**electrical characteristics at specified free-air temperature (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	T <sub>A</sub> †	TLC271C, TLC271AC, TLC271BC						UNIT
				V <sub>DD</sub> = 5 V			V <sub>DD</sub> = 10 V			
				MIN	TYP	MAX	MIN	TYP	MAX	
V <sub>IO</sub>	Input offset voltage	V <sub>O</sub> = 1.4 V, V <sub>IC</sub> = 0 V, R <sub>S</sub> = 50 Ω, R <sub>I</sub> = 1 MΩ	25°C	1.1		10	1.1		10	mV
			Full range			12			12	
			25°C	0.9		5	0.9		5	
			Full range			6.5			6.5	
			25°C	0.24		2	0.26		2	
			Full range			3			3	
α <sub>VIO</sub>	Average temperature coefficient of input offset voltage		25°C to 70°C	1.1		1				μV/°C
I <sub>IO</sub>	Input offset current (see Note 4)	V <sub>O</sub> = V <sub>DD</sub> /2, V <sub>IC</sub> = V <sub>DD</sub> /2	25°C	0.1	60	0.1		60	pA	
			70°C	7	300	8		300		
I <sub>IB</sub>	Input bias current (see Note 4)	V <sub>O</sub> = V <sub>DD</sub> /2, V <sub>IC</sub> = V <sub>DD</sub> /2	25°C	0.6	60	0.7		60	pA	
			70°C	40	600	50		600		
V <sub>ICR</sub>	Common-mode input voltage range (see Note 5)		25°C	-0.2 to 4	-0.3 to 4.2	-0.2 to 9		-0.3 to 9.2	V	
			Full range	-0.2 to 3.5	-0.2 to 8.5		V			
V <sub>OH</sub>	High-level output voltage	V <sub>ID</sub> = 100 mV, R <sub>L</sub> = 1 MΩ	25°C	3.2	4.1	8		8.9	V	
			0°C	3	4.1	7.8		8.9		
			70°C	3	4.2	7.8		8.9		
V <sub>OL</sub>	Low-level output voltage	V <sub>ID</sub> = -100 mV, I <sub>OL</sub> = 0	25°C	0		50	0		50	mV
			0°C	0		50	0		50	
			70°C	0		50	0		50	
A <sub>VD</sub>	Large-signal differential voltage amplification	R <sub>L</sub> = 1 MΩ, See Note 6	25°C	50	520	50		870	V/mV	
			0°C	50	700	50		1030		
			70°C	50	380	50		660		
CMRR	Common-mode rejection ratio	V <sub>IC</sub> = V <sub>ICRmin</sub>	25°C	65	94	65		97	dB	
			0°C	60	95	60		97		
			70°C	60	95	60		97		
k <sub>SVR</sub>	Supply-voltage rejection ratio (ΔV <sub>DD</sub> /ΔV <sub>IO</sub> )	V <sub>DD</sub> = 5 V to 10 V V <sub>O</sub> = 1.4 V	25°C	70	97	70		97	dB	
			0°C	60	97	60		97		
			70°C	60	98	60		98		
I <sub>I(SEL)</sub>	Input current (BIAS SELECT)	V <sub>I(SEL)</sub> = V <sub>DD</sub>	25°C	65		95		nA		
I <sub>DD</sub>	Supply current	V <sub>O</sub> = V <sub>DD</sub> /2, V <sub>IC</sub> = V <sub>DD</sub> /2, No load	25°C	10	17	14		23	μA	
			0°C	12		21	18			33
			70°C	8		14	11			20

† Full range is 0°C to 70°C.

- NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.  
5. This range also applies to each input individually.  
6. At V<sub>DD</sub> = 5 V, V<sub>O</sub> = 0.25 V to 2 V; at V<sub>DD</sub> = 10 V, V<sub>O</sub> = 1 V to 6 V.



**LOW-BIAS MODE**

**electrical characteristics at specified free-air temperature (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	T <sub>A</sub> †	TLC271I, TLC271AI, TLC271BI						UNIT
				V <sub>DD</sub> = 5 V			V <sub>DD</sub> = 10 V			
				MIN	TYP	MAX	MIN	TYP	MAX	
V <sub>IO</sub>	Input offset voltage	TLC271I TLC271AI TLC271BI	V <sub>O</sub> = 1.4 V, V <sub>IC</sub> = 0 V, R <sub>S</sub> = 50 Ω, R <sub>L</sub> = 1 MΩ	25°C	1.1 10		1.1 10		mV	
				Full range	13		13			
				25°C	0.9 5		0.9 5			
				Full range	7		7			
				25°C	0.24 2		0.26 2			
				Full range	3.5		3.5			
α <sub>VIO</sub>	Average temperature coefficient of input offset voltage		25°C to 85°C	1.1		1		μV/°C		
I <sub>IO</sub>	Input offset current (see Note 4)	V <sub>O</sub> = V <sub>DD</sub> /2, V <sub>IC</sub> = V <sub>DD</sub> /2	25°C	0.1 60		0.1 60		pA		
			85°C	24 1000		26 1000				
I <sub>IB</sub>	Input bias current (see Note 4)	V <sub>O</sub> = V <sub>DD</sub> /2, V <sub>IC</sub> = V <sub>DD</sub> /2	25°C	0.6 60		0.7 60		pA		
			85°C	200 2000		220 2000				
V <sub>ICR</sub>	Common-mode input voltage range (see Note 5)		25°C	-0.2 to 4	-0.3 to 4.2	-0.2 to 9	-0.3 to 9.2	V		
			Full range	-0.2 to 3.5		-0.2 to 8.5		V		
V <sub>OH</sub>	High-level output voltage	V <sub>ID</sub> = 100 mV, R <sub>L</sub> = 1 MΩ	25°C	3 4.1		8 8.9		V		
			-40°C	3 4.1		7.8 8.9				
			85°C	3 4.2		7.8 8.9				
V <sub>OL</sub>	Low-level output voltage	V <sub>ID</sub> = -100 mV, I <sub>OL</sub> = 0	25°C	0 50		0 50		mV		
			-40°C	0 50		0 50				
			85°C	0 50		0 50				
A <sub>VD</sub>	Large-signal differential voltage amplification	R <sub>L</sub> = 1 MΩ See Note 6	25°C	50 520		50 870		V/mV		
			-40°C	50 900		50 1550				
			85°C	50 330		50 585				
CMRR	Common-mode rejection ratio	V <sub>IC</sub> = V <sub>ICRmin</sub>	25°C	65 94		65 97		dB		
			-40°C	60 95		60 97				
			85°C	60 95		60 98				
k <sub>SVR</sub>	Supply-voltage rejection ratio (ΔV <sub>DD</sub> /ΔV <sub>IO</sub> )	V <sub>DD</sub> = 5 V to 10 V V <sub>O</sub> = 1.4 V	25°C	70 97		70 97		dB		
			-40°C	60 97		60 97				
			85°C	60 98		60 98				
I <sub>I(SEL)</sub>	Input current (BIAS SELECT)	V <sub>I(SEL)</sub> = V <sub>DD</sub>	25°C	65		95		nA		
I <sub>DD</sub>	Supply current	V <sub>O</sub> = V <sub>DD</sub> /2, V <sub>IC</sub> = V <sub>DD</sub> /2, No load	25°C	10 17		14 23		μA		
			-40°C	16 27		25 43				
			85°C	17 13		10 18				

† Full range is -40 to 85°C.

- NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.  
5. This range also applies to each input individually.  
6. At V<sub>DD</sub> = 5 V, V<sub>O</sub> = 0.25 V to 2 V; at V<sub>DD</sub> = 10 V, V<sub>O</sub> = 1 V to 6 V.

**TLC271, TLC271A, TLC271B**  
**LinCMOS™ PROGRAMMABLE LOW-POWER**  
**OPERATIONAL AMPLIFIERS**

SLOS090D – NOVEMBER 1987 – REVISED MARCH 2001

**LOW-BIAS MODE**

**electrical characteristics at specified free-air temperature (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	T <sub>A</sub> †	TLC271M						UNIT
			V <sub>DD</sub> = 5 V			V <sub>DD</sub> = 10 V			
			MIN	TYP	MAX	MIN	TYP	MAX	
V <sub>IO</sub> Input offset voltage	V <sub>O</sub> = 1.4 V, V <sub>IC</sub> = 0 V, R <sub>S</sub> = 50 Ω, R <sub>L</sub> = 1 MΩ	25°C		1.1	10		1.1	10	mV
		Full range				12		12	
α <sub>VIO</sub> Average temperature coefficient of input offset voltage		25°C to 125°C		1.4			1.4		μV/°C
I <sub>IO</sub> Input offset current (see Note 4)	V <sub>O</sub> = V <sub>DD</sub> /2, V <sub>IC</sub> = V <sub>DD</sub> /2	25°C		0.1	60		0.1	60	pA
		125°C		1.4	15		1.8	15	nA
I <sub>IB</sub> Input bias current (see Note 4)	V <sub>O</sub> = V <sub>DD</sub> /2, V <sub>IC</sub> = V <sub>DD</sub> /2	25°C		0.6	60		0.7	60	pA
		125°C		9	35		10	35	nA
V <sub>ICR</sub> Common-mode input voltage range (see Note 5)		25°C	0 to 4	-0.3 to 4.2		0 to 9	-0.3 to 9.2		V
		Full range	0 to 3.5			0 to 8.5			V
V <sub>OH</sub> High-level output voltage	V <sub>ID</sub> = 100 mV, R <sub>L</sub> = 1 MΩ	25°C		3.2	4.1		8	8.9	V
		-55°C		3	4.1		7.8	8.8	
		125°C		3	4.2		7.8	9	
V <sub>OL</sub> Low-level output voltage	V <sub>ID</sub> = -100 mV, I <sub>OL</sub> = 0	25°C		0	50		0	50	mV
		-55°C		0	50		0	50	
		125°C		0	50		0	50	
A <sub>VD</sub> Large-signal differential voltage amplification	R <sub>L</sub> = 1 MΩ, See Note 6	25°C		50	520		50	870	V/mV
		-55°C		25	1000		25	1775	
		125°C		25	200		25	380	
CMRR Common-mode rejection ratio	V <sub>IC</sub> = V <sub>ICRmin</sub>	25°C		65	94		65	97	dB
		-55°C		60	95		60	97	
		125°C		60	85		60	91	
k <sub>SVR</sub> Supply-voltage rejection ratio (ΔV <sub>DD</sub> /ΔV <sub>IO</sub> )	V <sub>DD</sub> = 5 V to 10 V V <sub>O</sub> = 1.4 V	25°C		70	97		70	97	dB
		-55°C		60	97		60	97	
		125°C		60	98		60	98	
I <sub>I(SEL)</sub> Input current (BIAS SELECT)	V <sub>I(SEL)</sub> = V <sub>DD</sub>	25°C		65		95		nA	
I <sub>DD</sub> Supply current	V <sub>O</sub> = V <sub>DD</sub> /2, V <sub>IC</sub> = V <sub>DD</sub> /2, No load	25°C		10	17		14	23	μA
		-55°C		17	30		28	48	
		125°C		7	12		9	15	

† Full range is -55°C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually.

6. At V<sub>DD</sub> = 5 V, V<sub>O</sub> = 0.25 V to 2 V; at V<sub>DD</sub> = 10 V, V<sub>O</sub> = 1 V to 6 V.





### LOW-BIAS MODE

operating characteristics at specified free-air temperature,  $V_{DD} = 5\text{ V}$

PARAMETER	TEST CONDITIONS	$T_A$	TLC271C, TLC271AC, TLC271BC			UNIT
			MIN	TYP	MAX	
SR      Slew rate at unity gain	$R_L = 1\text{ M}\Omega$ , $C_L = 20\text{ pF}$ , See Figure 98	$V_{I(PP)} = 1\text{ V}$	25°C	0.03		V/ $\mu$ s
			0°C	0.04		
			70°C	0.03		
		$V_{I(PP)} = 2.5\text{ V}$	25°C	0.03		
			0°C	0.03		
			70°C	0.02		
$V_n$ Equivalent input noise voltage	$f = 1\text{ kHz}$ , See Figure 99	$R_S = 20\ \Omega$ ,	25°C	68		nV/ $\sqrt{\text{Hz}}$
$B_{OM}$ Maximum output-swing bandwidth	$V_O = V_{OH}$ , $R_L = 1\text{ M}\Omega$ ,	$C_L = 20\text{ pF}$ , See Figure 98	25°C	5		kHz
			0°C	6		
			70°C	4.5		
$B_1$ Unity-gain bandwidth	$V_I = 10\text{ mV}$ , See Figure 100	$C_L = 20\text{ pF}$ ,	25°C	85		kHz
			0°C	100		
			70°C	65		
$\phi_m$ Phase margin	$V_I = 10\text{ mV}$ , $C_L = 20\text{ pF}$ ,	$f = B_1$ , See Figure 100	25°C	34°		
			0°C	36°		
			70°C	30°		

operating characteristics at specified free-air temperature,  $V_{DD} = 10\text{ V}$

PARAMETER	TEST CONDITIONS	$T_A$	TLC271C, TLC271AC, TLC271BC			UNIT
			MIN	TYP	MAX	
SR      Slew rate at unity gain	$R_L = 1\text{ M}\Omega$ , $C_L = 20\text{ pF}$ , See Figure 98	$V_{I(PP)} = 1\text{ V}$	25°C	0.05		V/ $\mu$ s
			0°C	0.05		
			70°C	0.04		
		$V_{I(PP)} = 5.5\text{ V}$	25°C	0.04		
			0°C	0.05		
			70°C	0.04		
$V_n$ Equivalent input noise voltage	$f = 1\text{ kHz}$ , See Figure 99	$R_S = 20\ \Omega$ ,	25°C	68		nV/ $\sqrt{\text{Hz}}$
$B_{OM}$ Maximum output-swing bandwidth	$V_O = V_{OH}$ , $R_L = 1\text{ M}\Omega$ ,	$C_L = 20\text{ pF}$ , See Figure 98	25°C	1		kHz
			0°C	1.3		
			70°C	0.9		
$B_1$ Unity-gain bandwidth	$V_I = 10\text{ mV}$ , See Figure 100	$C_L = 20\text{ pF}$ ,	25°C	110		kHz
			0°C	125		
			70°C	90		
$\phi_m$ Phase margin	$V_I = 10\text{ mV}$ , $C_L = 20\text{ pF}$ ,	$f = B_1$ , See Figure 100	25°C	38°		
			0°C	40°		
			70°C	34°		

**TLC271, TLC271A, TLC271B**  
**LinCMOS™ PROGRAMMABLE LOW-POWER**  
**OPERATIONAL AMPLIFIERS**

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**LOW-BIAS MODE**

**operating characteristics at specified free-air temperature,  $V_{DD} = 5\text{ V}$**

PARAMETER	TEST CONDITIONS	$T_A$	TLC271I, TLC271AI, TLC271BI			UNIT
			MIN	TYP	MAX	
SR Slew rate at unity gain	$R_L = 1\text{ M}\Omega$ , $C_L = 20\text{ pF}$ , See Figure 98	$V_{I(PP)} = 1\text{ V}$	25°C	0.03		V/ $\mu\text{s}$
			-40°C	0.04		
			85°C	0.03		
		$V_{I(PP)} = 2.5\text{ V}$	25°C	0.03		
			-40°C	0.04		
			85°C	0.02		
$V_n$ Equivalent input noise voltage	$f = 1\text{ kHz}$ , See Figure 99	$R_S = 20\ \Omega$ , 25°C	68		nV/ $\sqrt{\text{Hz}}$	
$B_{OM}$ Maximum output-swing bandwidth	$V_O = V_{OH}$ , $R_L = 1\text{ M}\Omega$ , $C_L = 20\text{ pF}$ , See Figure 98	25°C	5		kHz	
		-40°C	7			
		85°C	4			
$B_1$ Unity-gain bandwidth	$V_I = 10\text{ mV}$ , See Figure 100	$C_L = 20\text{ pF}$ , 25°C	85		MHz	
		-40°C	130			
		85°C	55			
$\phi_m$ Phase margin	$V_I = 10\text{ mV}$ , $C_L = 20\text{ pF}$ , $f = B_1$ , See Figure 100	25°C	34°			
		-40°C	38°			
		85°C	28°			

**operating characteristics at specified free-air temperature,  $V_{DD} = 10\text{ V}$**

PARAMETER	TEST CONDITIONS	$T_A$	TLC271C, TLC271AC, TLC271BC			UNIT
			MIN	TYP	MAX	
SR Slew rate at unity gain	$R_L = 1\text{ M}\Omega$ , $C_L = 20\text{ pF}$ , See Figure 98	$V_{I(PP)} = 1\text{ V}$	25°C	0.05		V/ $\mu\text{s}$
			-40°C	0.06		
			85°C	0.03		
		$V_{I(PP)} = 5.5\text{ V}$	25°C	0.04		
			-40°C	0.05		
			85°C	0.03		
$V_n$ Equivalent input noise voltage	$f = 1\text{ kHz}$ , See Figure 99	$R_S = 20\ \Omega$ , 25°C	68		nV/ $\sqrt{\text{Hz}}$	
$B_{OM}$ Maximum output-swing bandwidth	$V_O = V_{OH}$ , $R_L = 1\text{ M}\Omega$ , $C_L = 20\text{ pF}$ , See Figure 98	25°C	1		kHz	
		-40°C	1.4			
		85°C	0.8			
$B_1$ Unity-gain bandwidth	$V_I = 10\text{ mV}$ , See Figure 100	$C_L = 20\text{ pF}$ , 25°C	110		MHz	
		-40°C	155			
		85°C	80			
$\phi_m$ Phase margin	$V_I = 10\text{ mV}$ , $C_L = 20\text{ pF}$ , $f = B_1$ , See Figure 100	25°C	38°			
		-40°C	42°			
		85°C	32°			



### LOW-BIAS MODE

operating characteristics at specified free-air temperature,  $V_{DD} = 5\text{ V}$

PARAMETER	TEST CONDITIONS	$T_A$	TLC271M			UNIT
			MIN	TYP	MAX	
SR    Slew rate at unity gain	$R_L = 1\text{ M}\Omega$ , $C_L = 20\text{ pF}$ , See Figure 98	$V_{I(PP)} = 1\text{ V}$	25°C	0.03		V/ $\mu$ s
			-55°C	0.04		
			125°C	0.02		
		$V_{I(PP)} = 2.5\text{ V}$	25°C	0.03		
			-55°C	0.04		
			125°C	0.02		
$V_n$ Equivalent input noise voltage	$f = 1\text{ kHz}$ , See Figure 99	$R_S = 20\ \Omega$ , 25°C	68		nV/ $\sqrt{\text{Hz}}$	
$B_{OM}$ Maximum output-swing bandwidth	$V_O = V_{OH}$ , $R_L = 1\text{ M}\Omega$ , $C_L = 20\text{ pF}$ , See Figure 98	25°C	5		kHz	
		-55°C	8			
		125°C	3			
$B_1$ Unity-gain bandwidth	$V_I = 10\text{ mV}$ , See Figure 100	$C_L = 20\text{ pF}$ , 25°C	85		kHz	
			-55°C			140
			125°C			45
$\phi_m$ Phase margin	$V_I = 10\text{ mV}$ , $C_L = 20\text{ pF}$ , $f = B_1$ , See Figure 100	25°C	34°			
		-55°C	39°			
		125°C	25°			

operating characteristics at specified free-air temperature,  $V_{DD} = 10\text{ V}$

PARAMETER	TEST CONDITIONS	$T_A$	TLC271M			UNIT
			MIN	TYP	MAX	
SR    Slew rate at unity gain	$R_L = 1\text{ M}\Omega$ , $C_L = 20\text{ pF}$ , See Figure 98	$V_{I(PP)} = 1\text{ V}$	25°C	0.05		V/ $\mu$ s
			-55°C	0.06		
			125°C	0.03		
		$V_{I(PP)} = 5.5\text{ V}$	25°C	0.04		
			-55°C	0.06		
			125°C	0.03		
$V_n$ Equivalent input noise voltage	$f = 1\text{ kHz}$ , See Figure 99	$R_S = 20\ \Omega$ , 25°C	68		nV/ $\sqrt{\text{Hz}}$	
$B_{OM}$ Maximum output-swing bandwidth	$V_O = V_{OH}$ , $R_L = 1\text{ M}\Omega$ , $C_L = 20\text{ pF}$ , See Figure 98	25°C	1		kHz	
		-55°C	1.5			
		125°C	0.7			
$B_1$ Unity-gain bandwidth	$V_I = 10\text{ mV}$ , See Figure 100	$C_L = 20\text{ pF}$ , 25°C	110		kHz	
			-55°C			165
			125°C			70
$\phi_m$ Phase margin	$V_I = 10\text{ mV}$ , $C_L = 20\text{ pF}$ , $f = B_1$ , See Figure 100	25°C	38°			
		-55°C	43°			
		125°C	29°			

**TLC271, TLC271A, TLC271B**  
**LinCMOS™ PROGRAMMABLE LOW-POWER**  
**OPERATIONAL AMPLIFIERS**

SLOS090D – NOVEMBER 1987 – REVISED MARCH 2001

**TYPICAL CHARACTERISTICS (LOW-BIAS MODE)**

**Table of Graphs**

		<b>FIGURE</b>	
$V_{IO}$	Input offset voltage	Distribution	66, 67
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$V_{OH}$	High-level output voltage	vs High-level output current	70, 71
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$I_{DD}$	Supply current	vs Supply voltage	84
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$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	89
$B_1$	Unity-gain bandwidth	vs Free-air temperature	90
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$\phi_m$	Phase margin	vs Supply voltage	94
		vs Free-air temperature	95
		vs Capacitive load	96
$V_n$	Equivalent input noise voltage	vs Frequency	97
		Phase shift	92, 93



TYPICAL CHARACTERISTICS (LOW-BIAS MODE)†

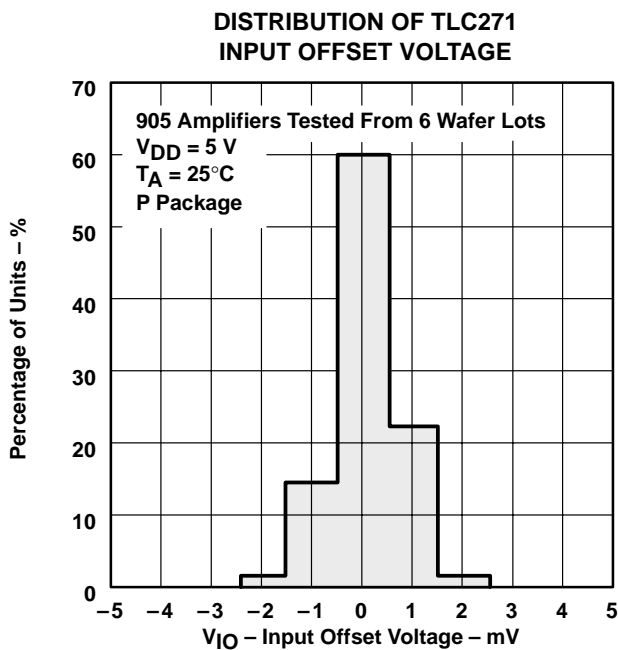


Figure 66

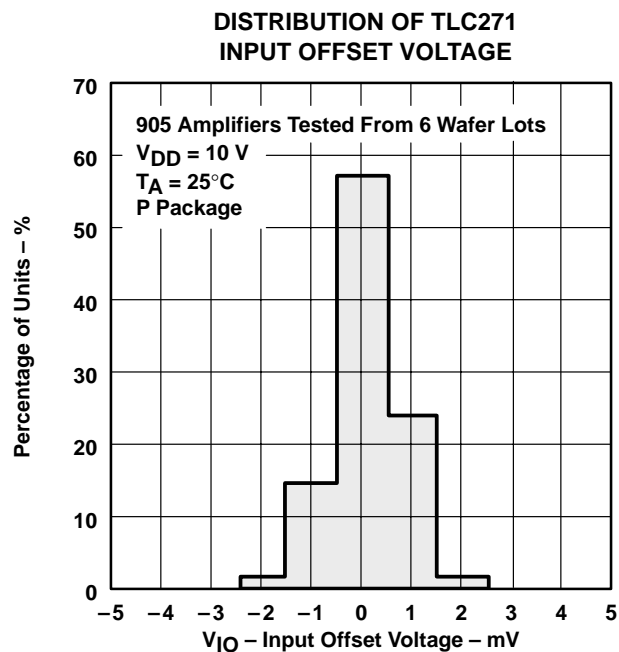


Figure 67

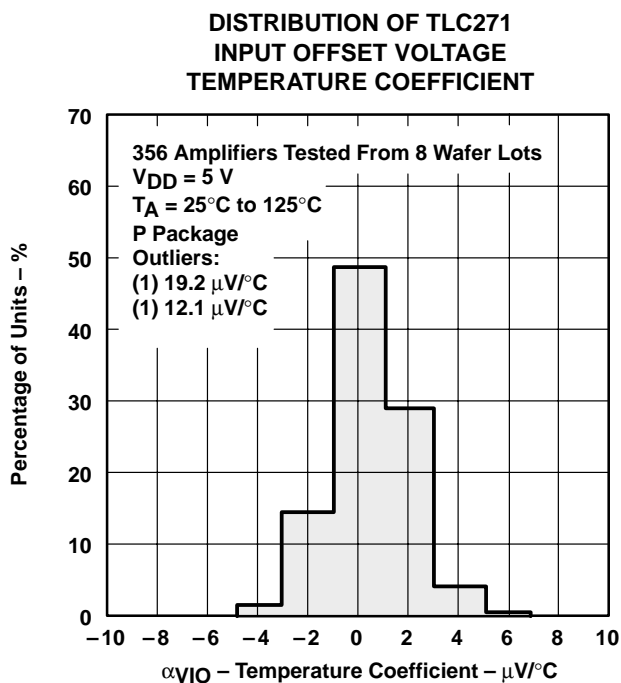


Figure 68

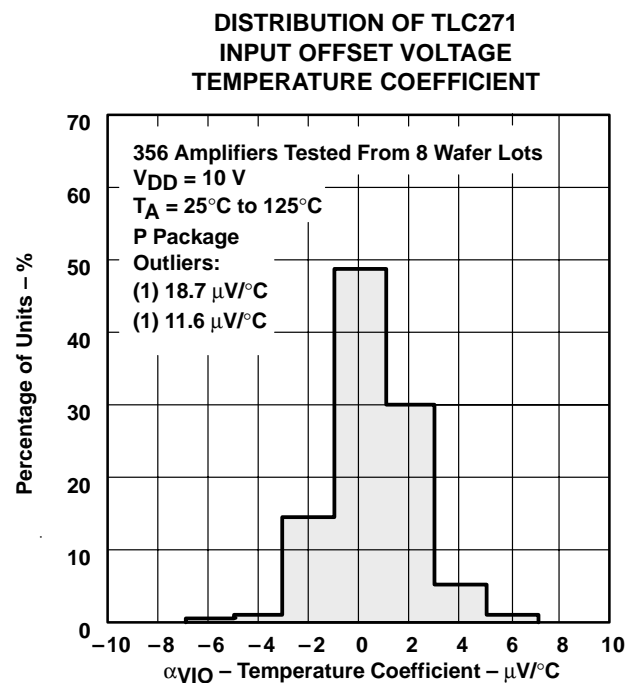
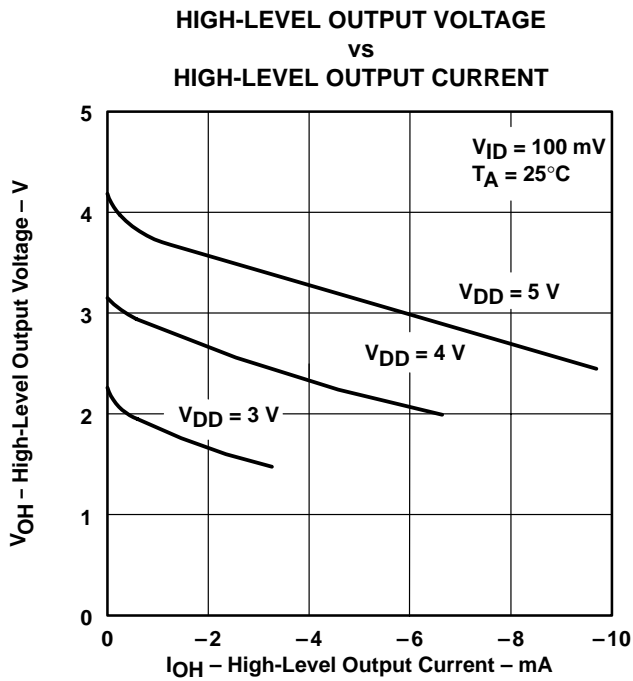


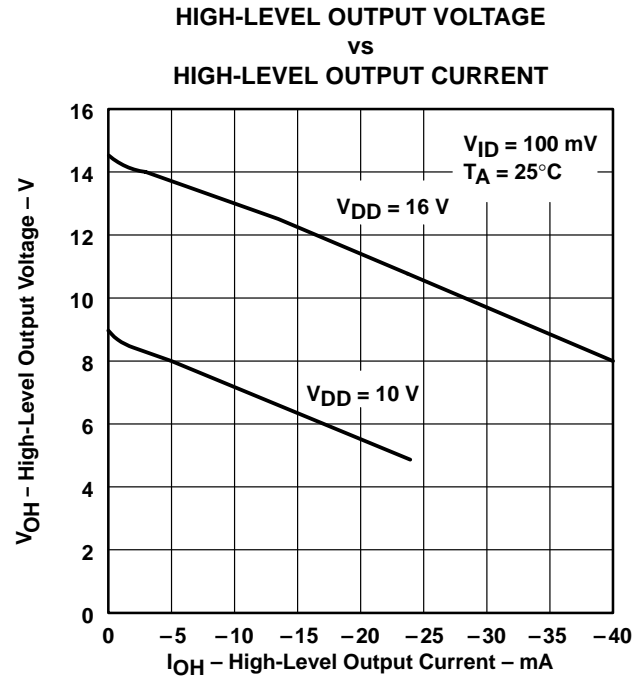
Figure 69

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

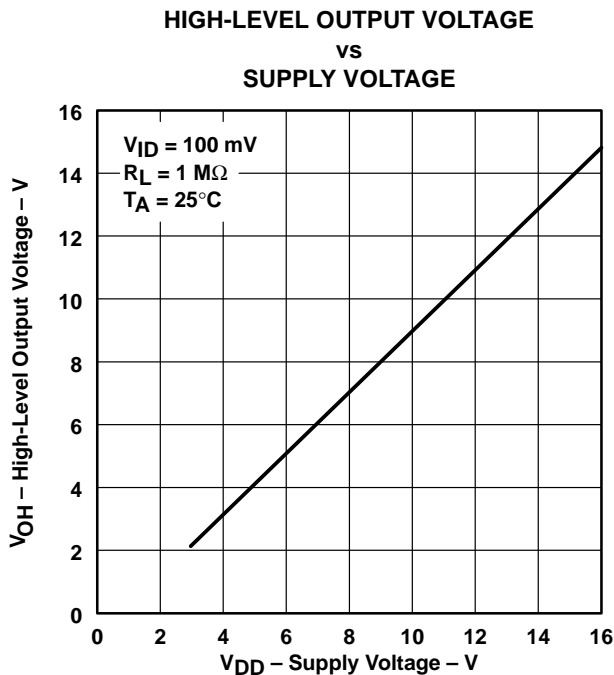
**TYPICAL CHARACTERISTICS (LOW-BIAS MODE)†**



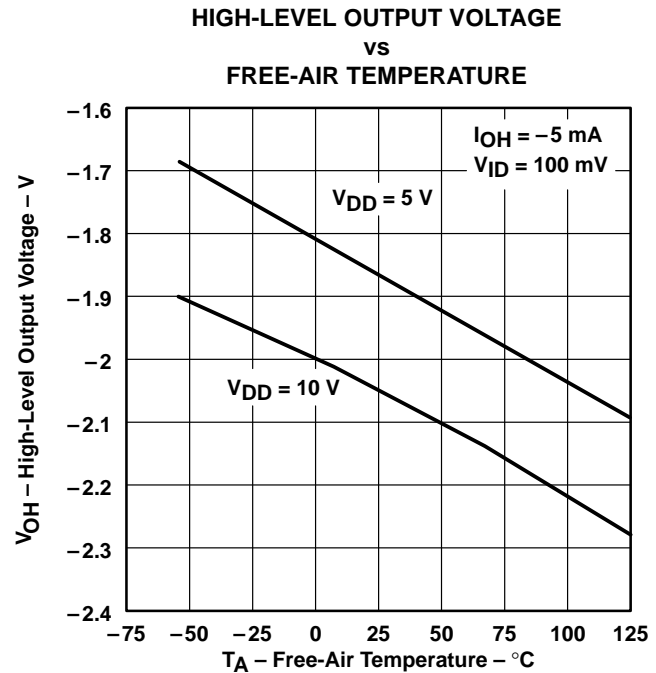
**Figure 70**



**Figure 71**



**Figure 72**



**Figure 73**

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS (LOW-BIAS MODE)†

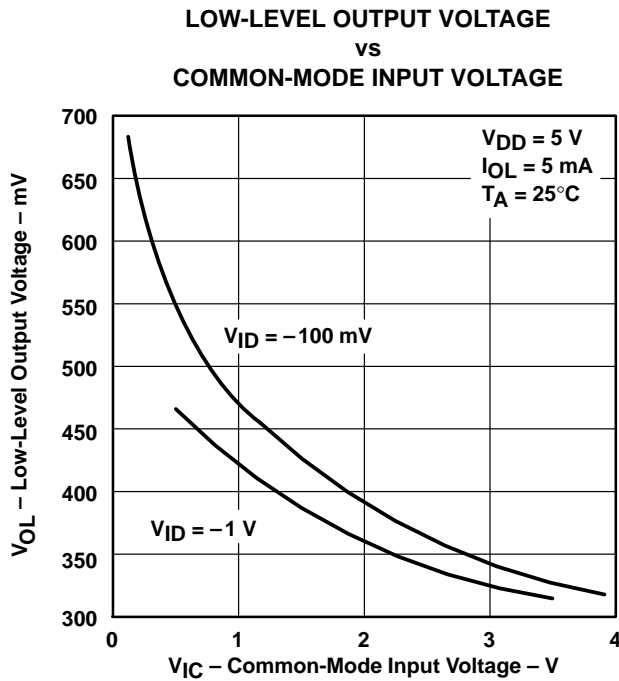


Figure 74

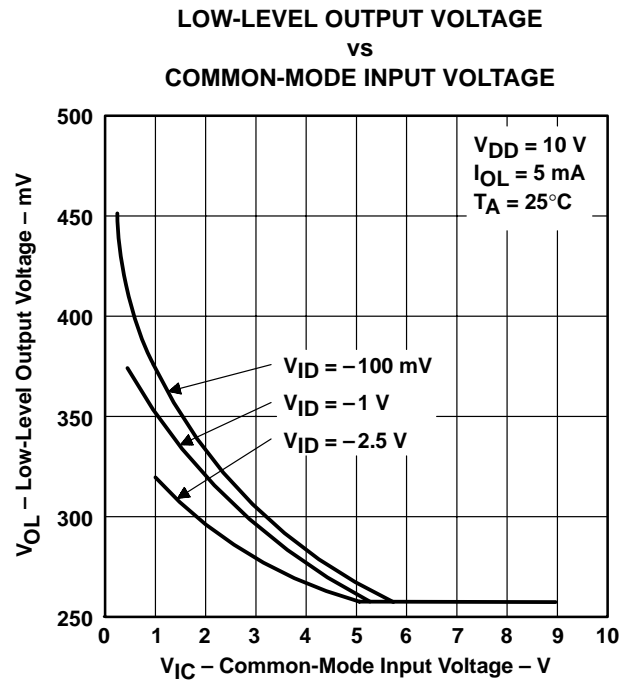


Figure 75

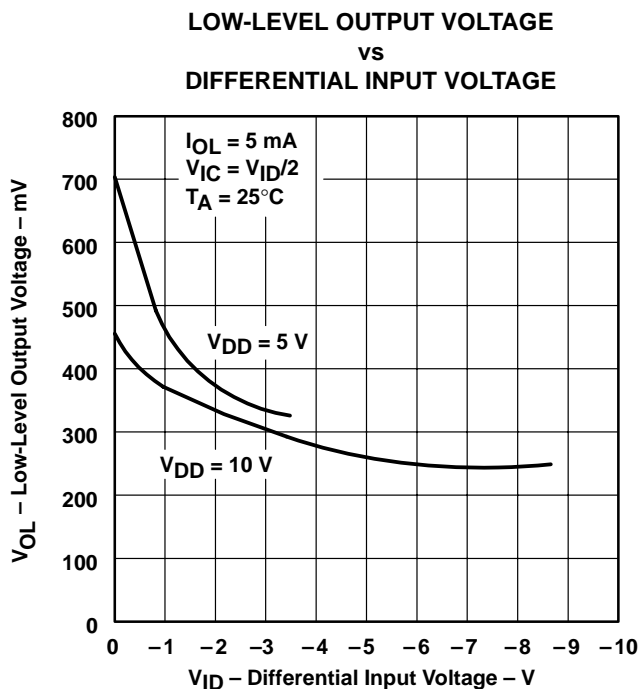


Figure 76

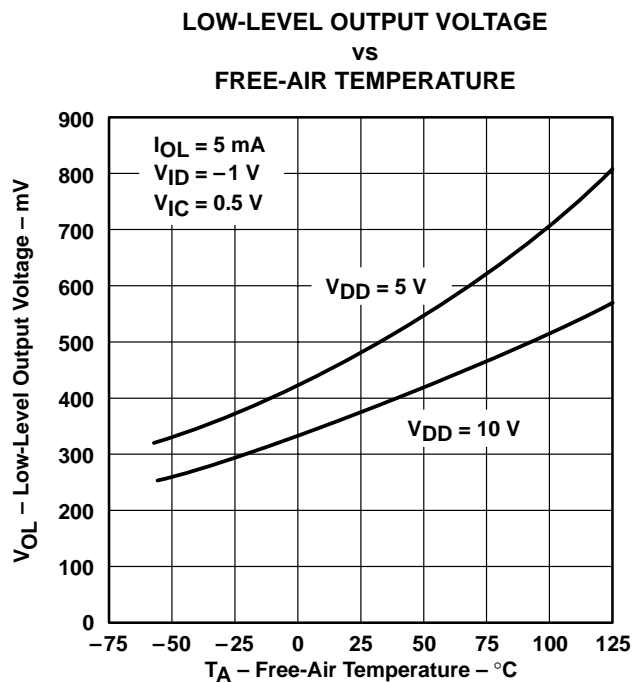
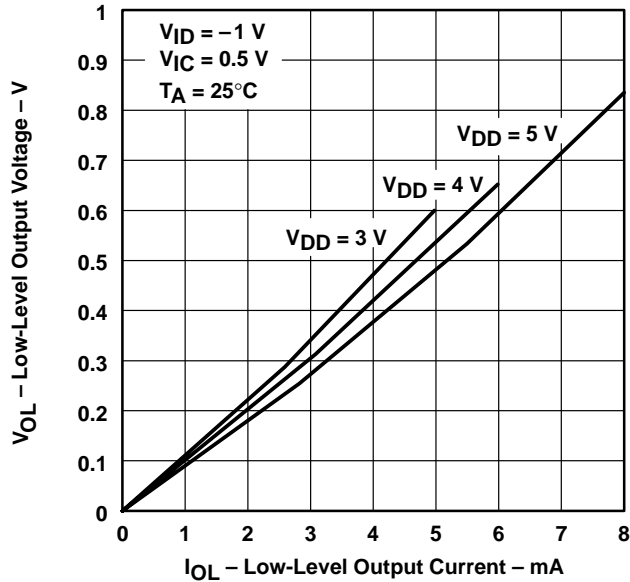


Figure 77

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

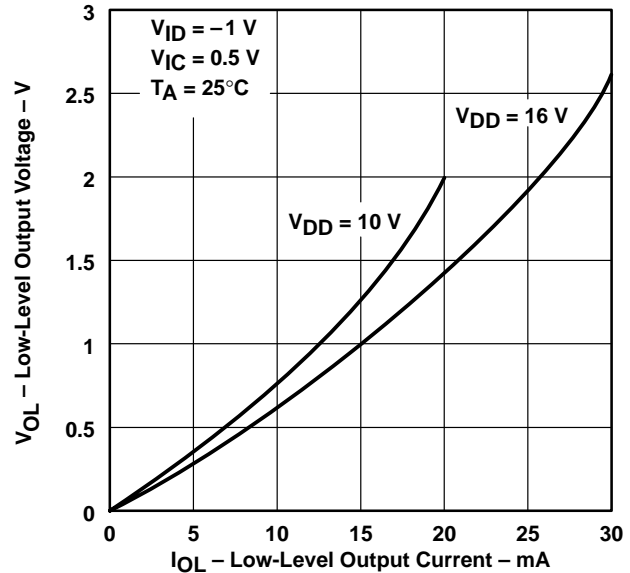
**TYPICAL CHARACTERISTICS (LOW-BIAS MODE)†**

**LOW-LEVEL OUTPUT VOLTAGE  
 vs  
 LOW-LEVEL OUTPUT CURRENT**



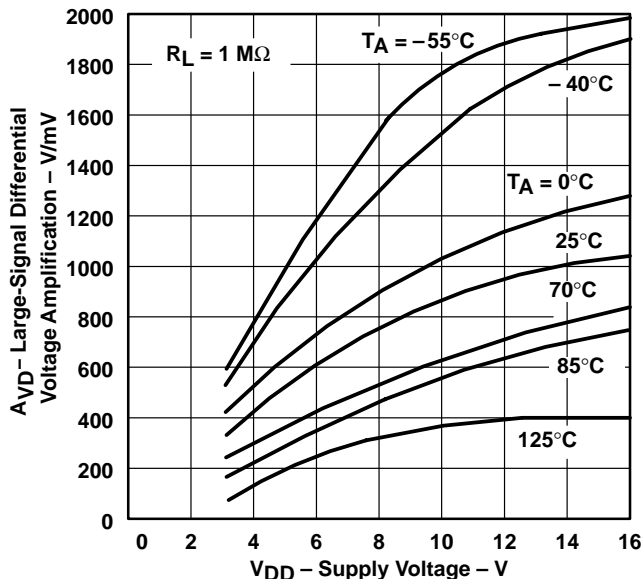
**Figure 78**

**LOW-LEVEL OUTPUT VOLTAGE  
 vs  
 LOW-LEVEL OUTPUT CURRENT**



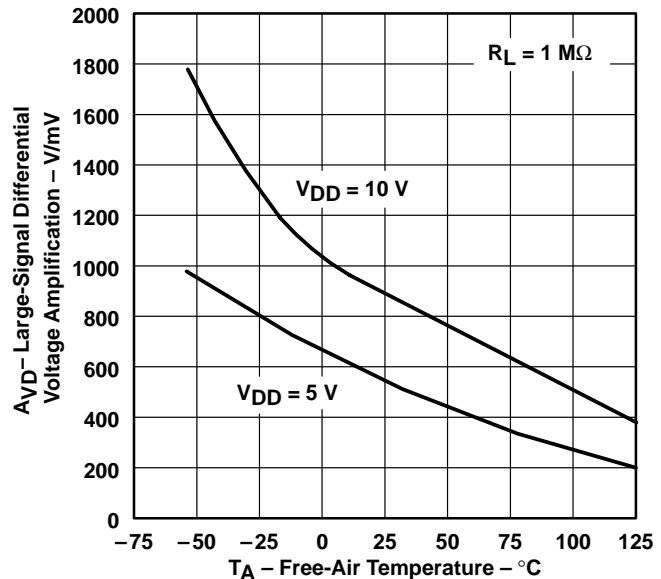
**Figure 79**

**LARGE-SIGNAL  
 DIFFERENTIAL VOLTAGE AMPLIFICATION  
 vs  
 SUPPLY VOLTAGE**



**Figure 80**

**LARGE-SIGNAL  
 DIFFERENTIAL VOLTAGE AMPLIFICATION  
 vs  
 FREE-AIR TEMPERATURE**

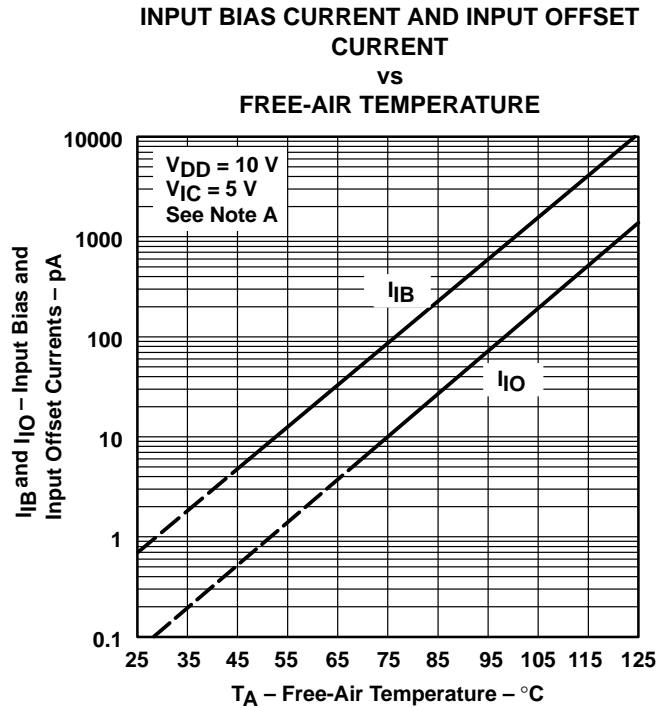


**Figure 81**

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.



TYPICAL CHARACTERISTICS (LOW-BIAS MODE)†



NOTE A: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

Figure 82

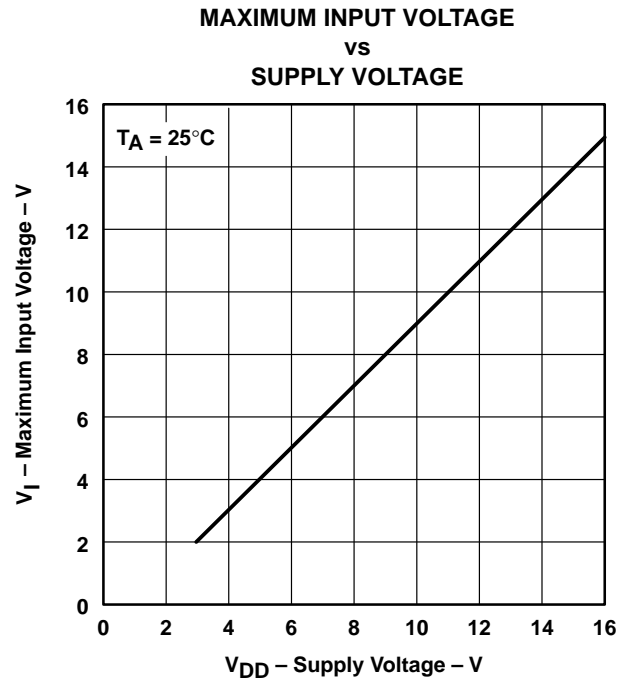


Figure 83

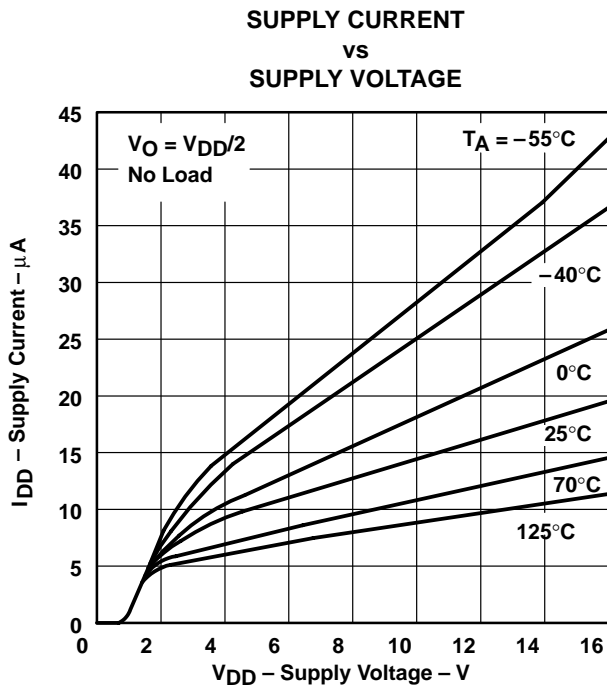


Figure 84

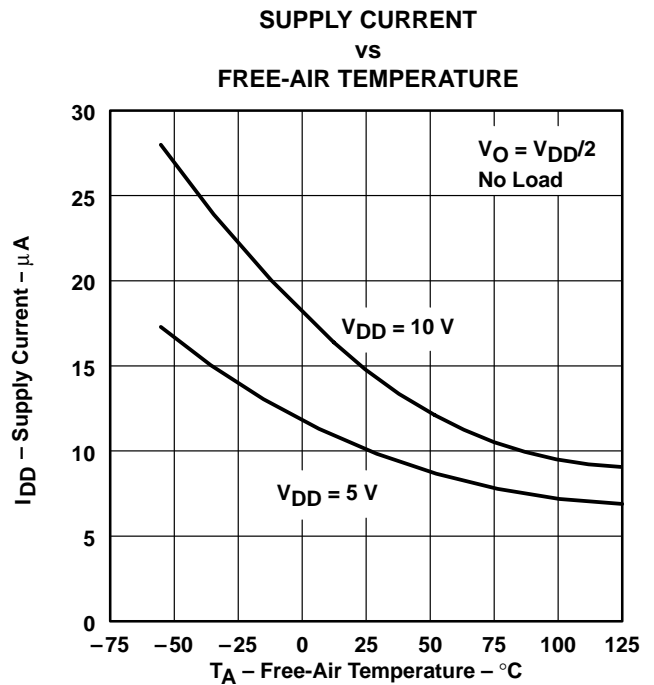
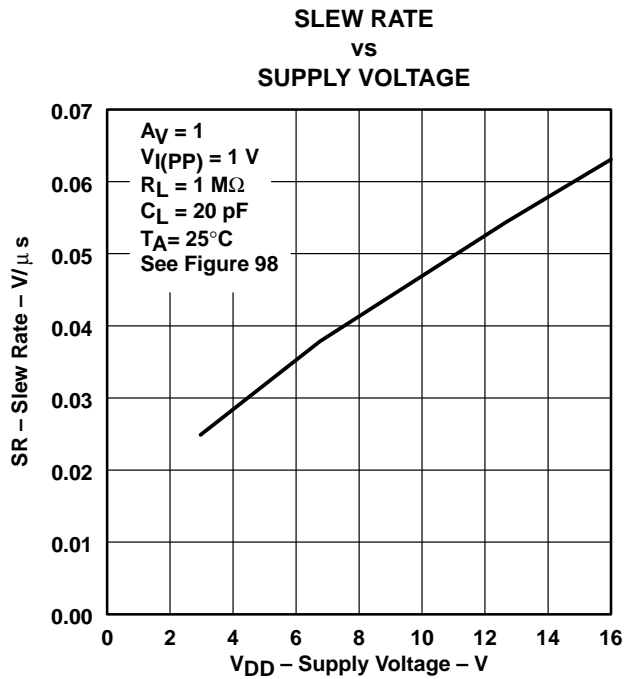


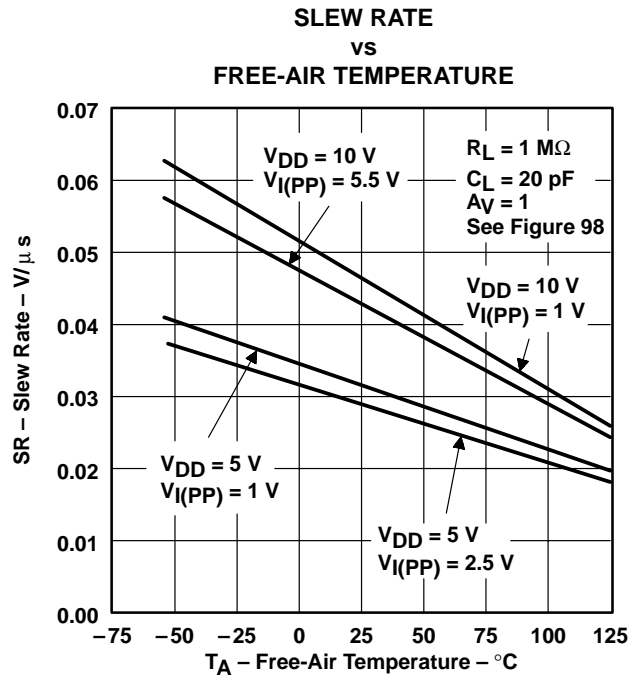
Figure 85

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

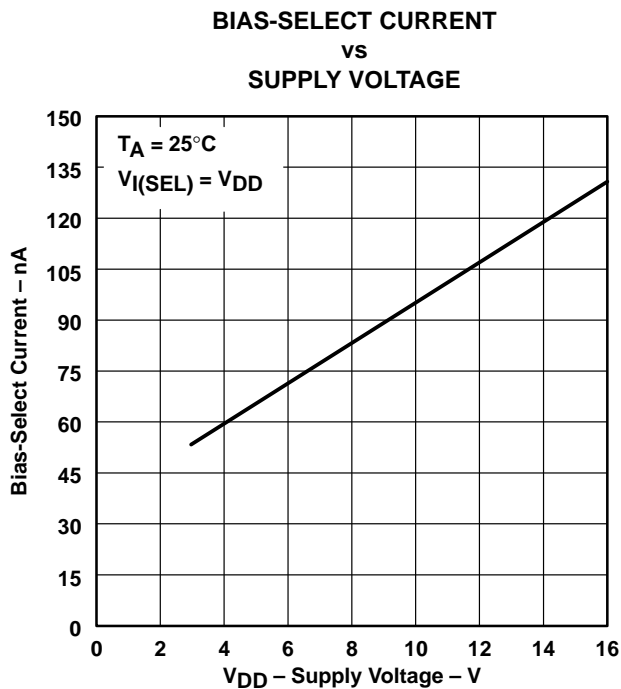
**TYPICAL CHARACTERISTICS (LOW-BIAS MODE)†**



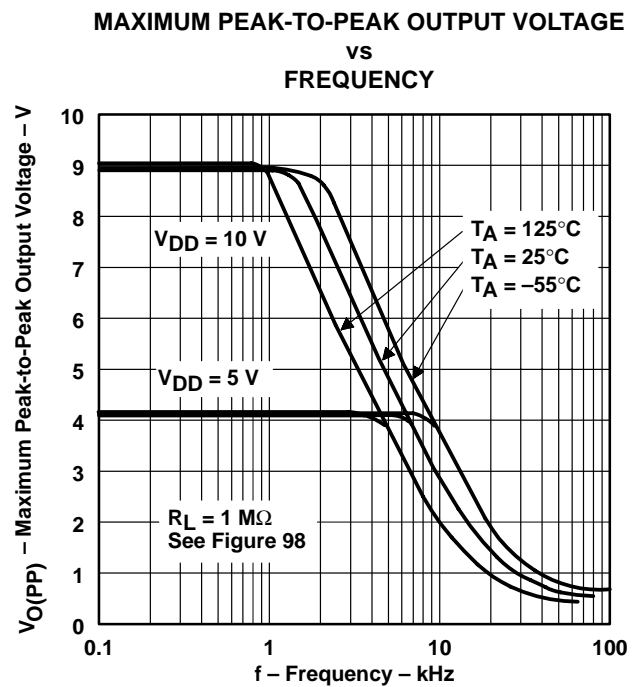
**Figure 86**



**Figure 87**



**Figure 88**



**Figure 89**

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS (LOW-BIAS MODE)†

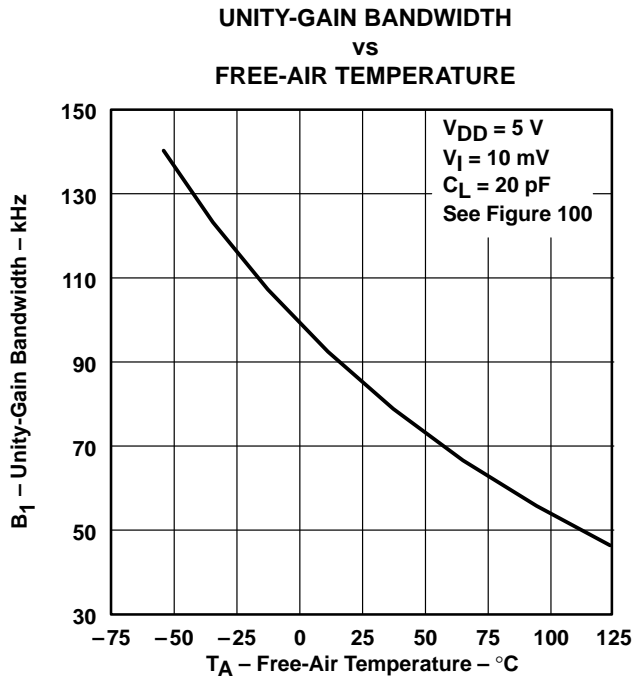


Figure 90

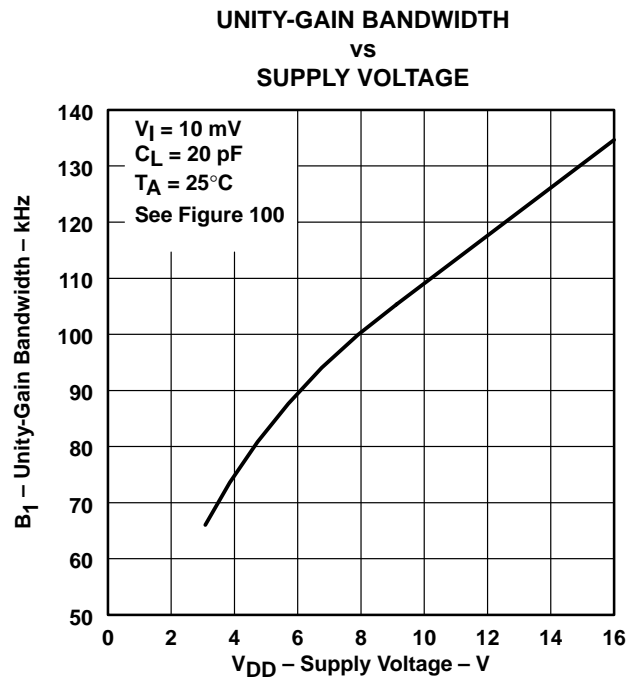


Figure 91

**LARGE-SIGNAL DIFFERENTIAL VOLTAGE  
 AMPLIFICATION AND PHASE SHIFT  
 vs  
 FREQUENCY**

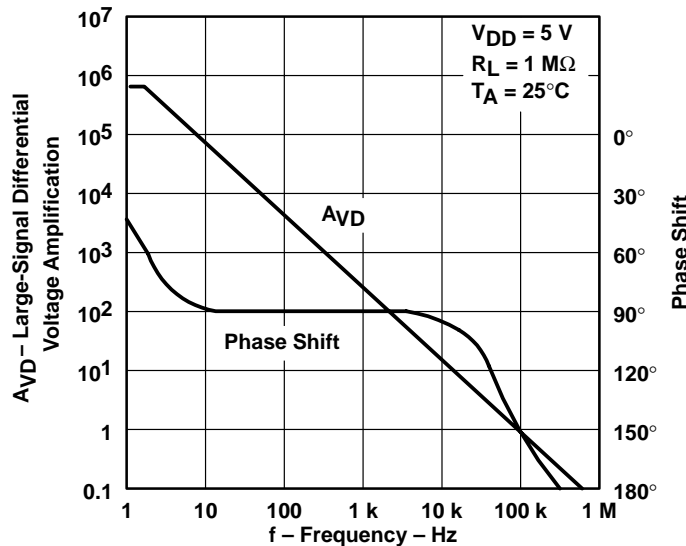


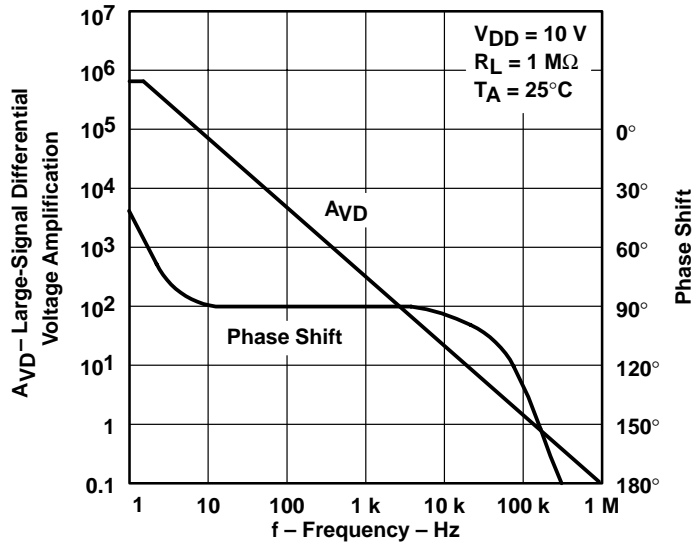
Figure 92

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

**TYPICAL CHARACTERISTICS (LOW-BIAS MODE)†**

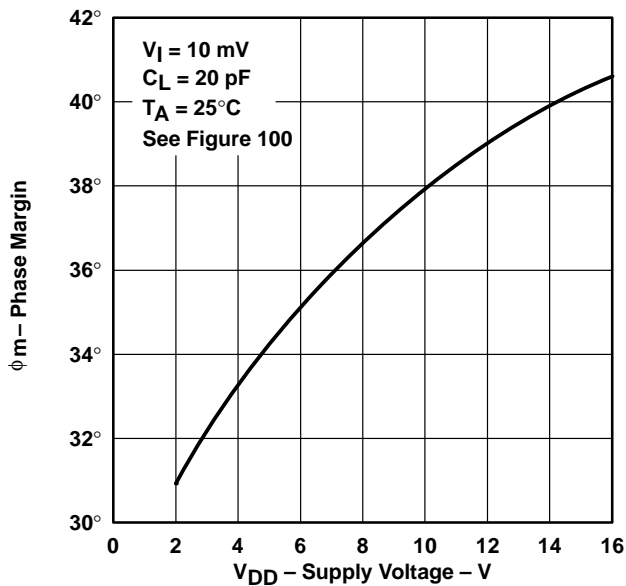
**LARGE-SIGNAL DIFFERENTIAL VOLTAGE  
 AMPLIFICATION AND PHASE SHIFT**

vs  
**FREQUENCY**



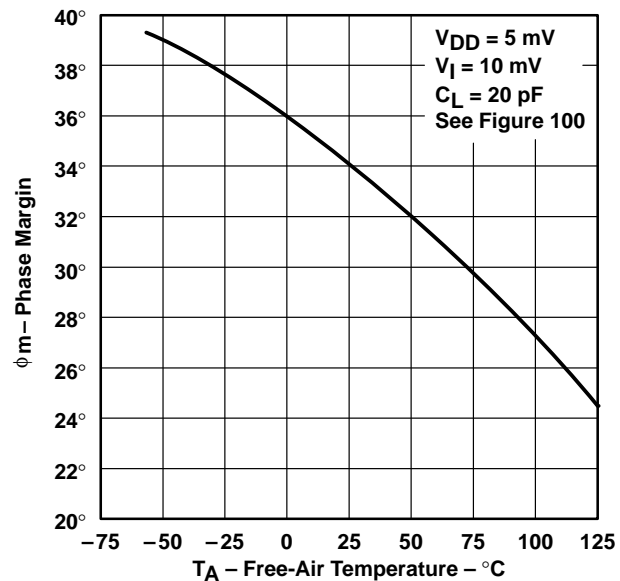
**Figure 93**

**PHASE MARGIN  
 vs  
 SUPPLY VOLTAGE**



**Figure 94**

**PHASE MARGIN  
 vs  
 FREE-AIR TEMPERATURE**



**Figure 95**

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS (LOW-BIAS MODE)†

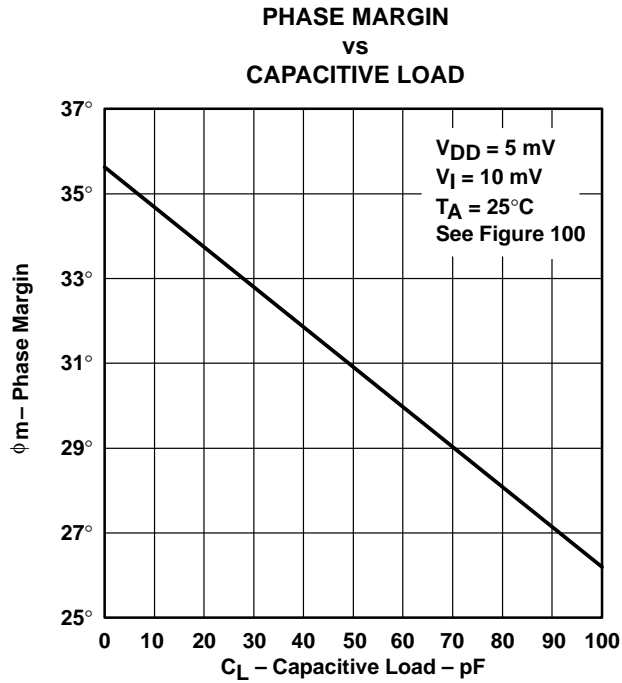


Figure 96

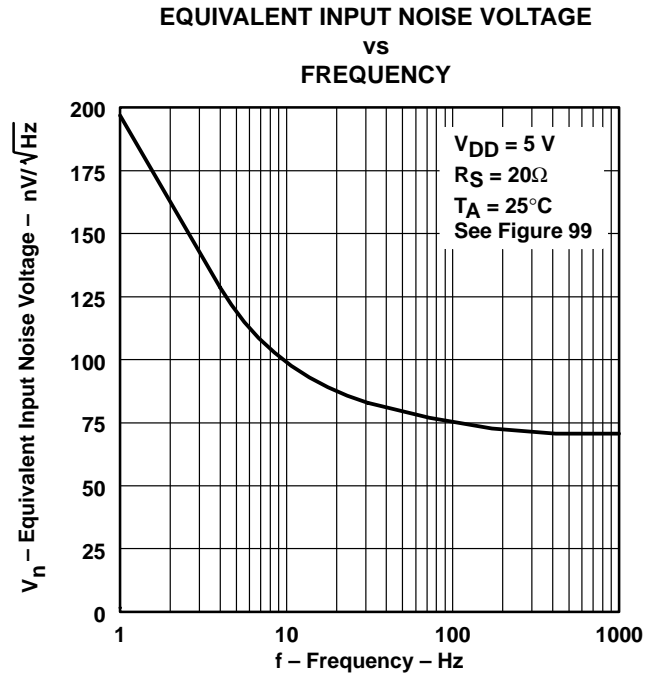


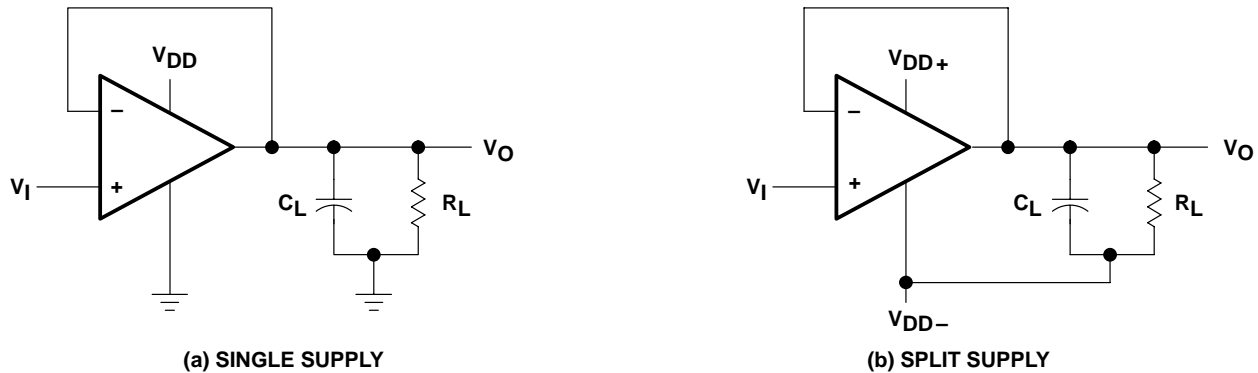
Figure 97

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

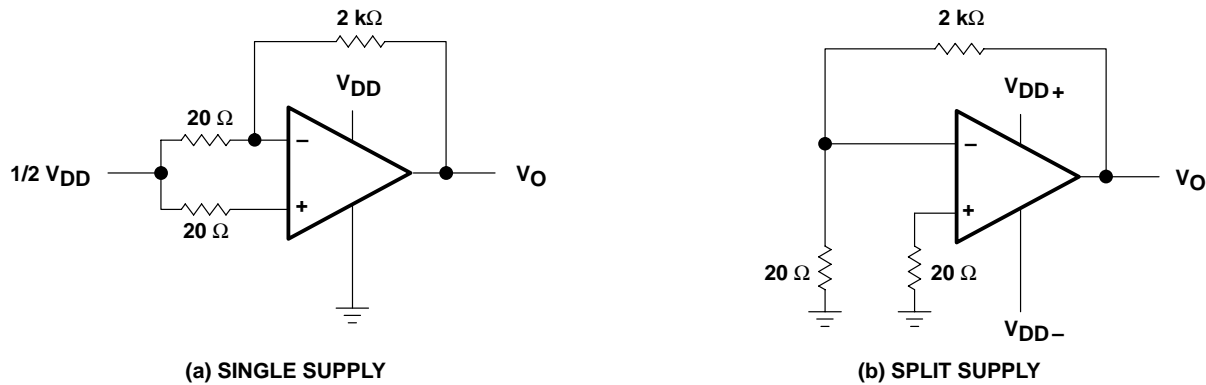
**PARAMETER MEASUREMENT INFORMATION**

**single-supply versus split-supply test circuits**

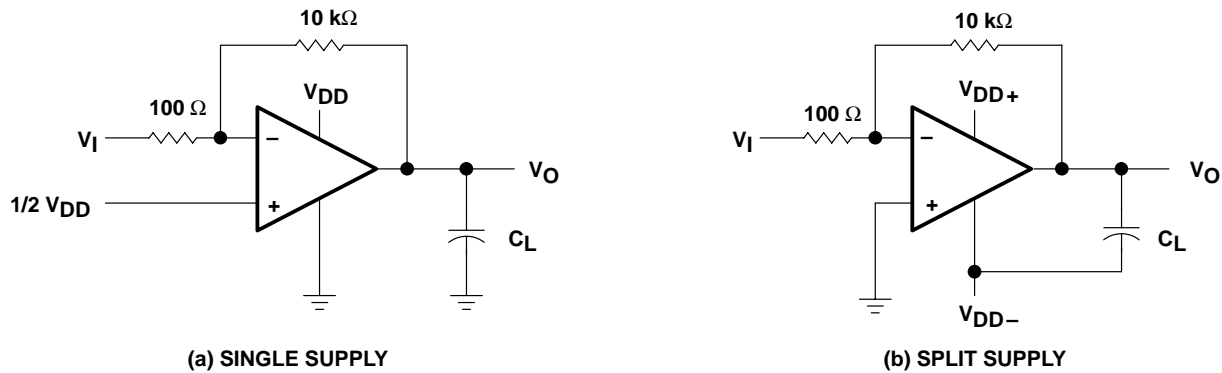
Because the TLC271 is optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit gives the same result.



**Figure 98. Unity-Gain Amplifier**



**Figure 99. Noise-Test Circuit**



**Figure 100. Gain-of-100 Inverting Amplifier**

## PARAMETER MEASUREMENT INFORMATION

### input bias current

Because of the high input impedance of the TLC271 operational amplifiers, attempts to measure the input bias current can result in erroneous readings. The bias current at normal room ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

1. Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 101). Leakages that would otherwise flow to the inputs are shunted away.
2. Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the open-socket leakage readings from the readings obtained with a device in the test socket.

One word of caution: many automatic testers as well as some bench-top operational amplifier testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into the test socket to obtain a correct reading; therefore, an open-socket reading is not feasible using this method.

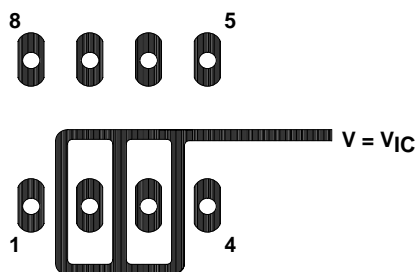


Figure 101. Isolation Metal Around Device inputs (JG and P packages)

### low-level output voltage

To obtain low-supply-voltage operation, some compromise is necessary in the input stage. This compromise results in the device low-level output being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to the Typical Characteristics section of this data sheet.

### input offset voltage temperature coefficient

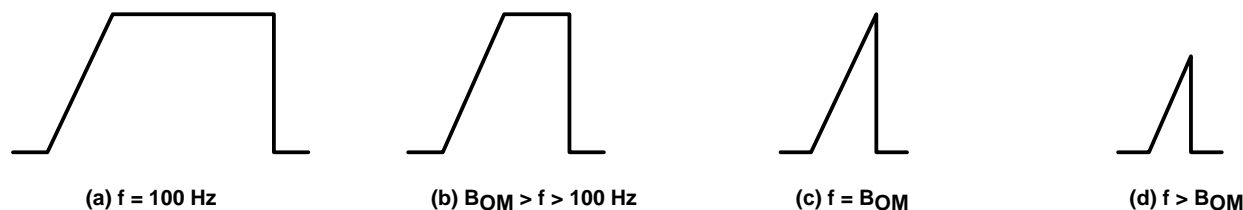
Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture results in leakage and contact resistance which can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no effect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. It is suggested that these measurements be performed at temperatures above freezing to minimize error.

**PARAMETER MEASUREMENT INFORMATION**

**full-power response**

Full-power response, the frequency above which the amplifier slew rate limits the output voltage swing, is often specified two ways: full-linear response and full-peak response. The full-linear response is generally measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for significant distortion, the full-peak response is specified in this data sheet and is measured using the circuit of Figure 98. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 102). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.



**Figure 102. Full-Power-Response Output Signal**

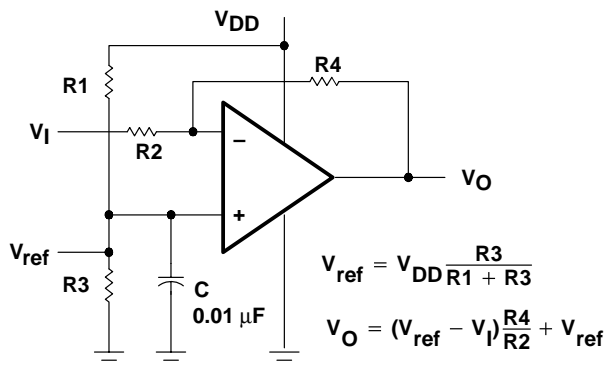
**test time**

Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices, and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.

**APPLICATION INFORMATION**

**single-supply operation**

While the TLC271 performs well using dual power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This includes an input common mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 3 V (C-suffix types), thus allowing operation with supply levels commonly available for TTL and HCMOS; however, for maximum dynamic range, 16-V single-supply operation is recommended.



**Figure 103. Inverting Amplifier With Voltage Reference**



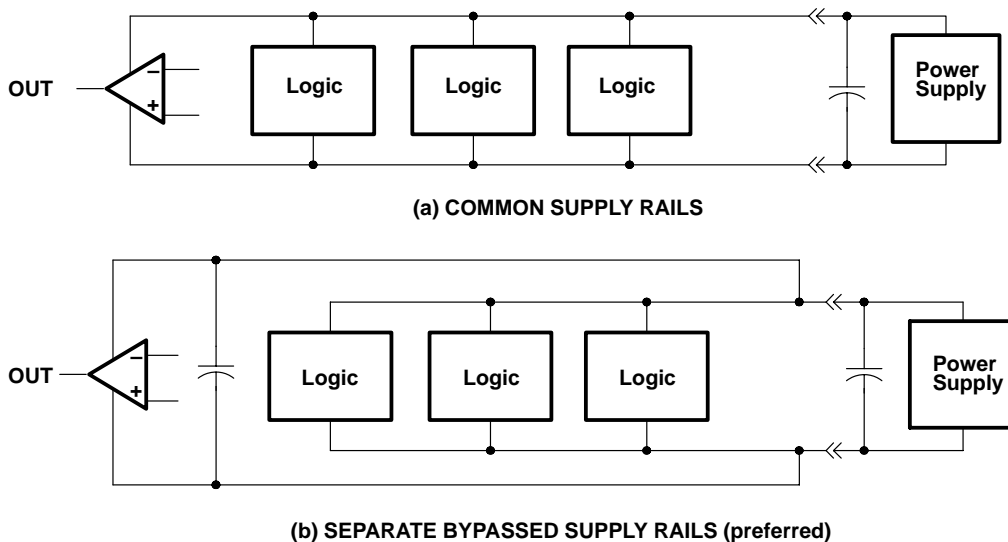
**APPLICATION INFORMATION**

**single-supply operation (continued)**

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. A resistive voltage divider is usually sufficient to establish this reference level (see Figure 103). The low input bias current consumption of the TLC271 permits the use of very large resistive values to implement the voltage divider, thus minimizing power consumption.

The TLC271 works well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

1. Power the linear devices from separate bypassed supply lines (see Figure 104); otherwise, the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
2. Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, RC decoupling may be necessary in high-frequency applications.

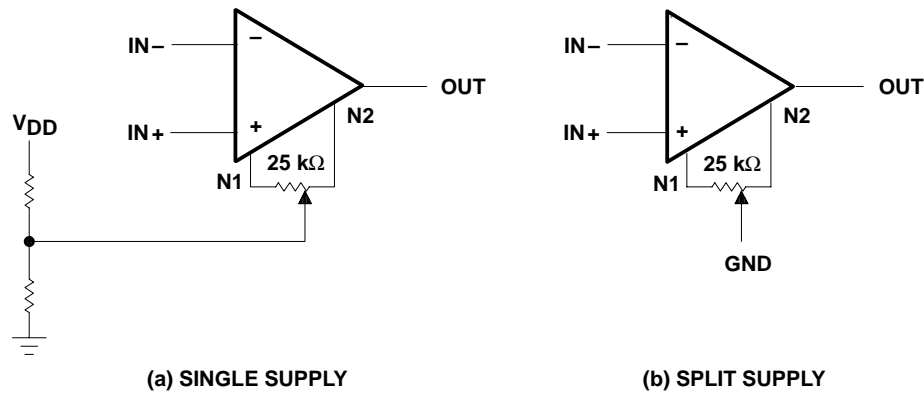


**Figure 104. Common Versus Separate Supply Rails**

**APPLICATION INFORMATION**

**input offset voltage nulling**

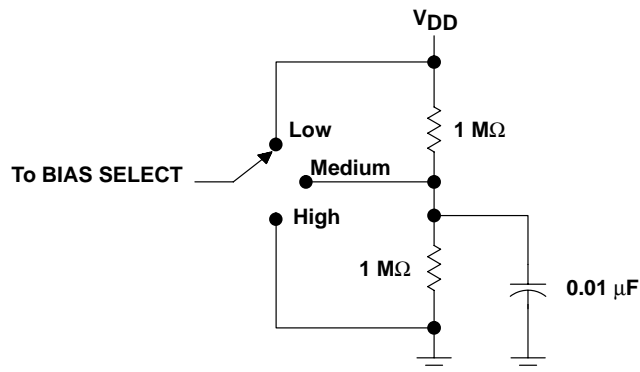
The TLC271 offers external input offset null control. Nulling of the input offset voltage may be achieved by adjusting a 25-kΩ potentiometer connected between the offset null terminals with the wiper connected as shown in Figure 105. The amount of nulling range varies with the bias selection. In the high-bias mode, the nulling range allows the maximum offset voltage specified to be trimmed to zero. In low-bias and medium-bias modes, total nulling may not be possible.



**Figure 105. Input Offset Voltage Null Circuit**

**bias selection**

Bias selection is achieved by connecting the bias select pin to one of the three voltage levels (see Figure 106). For medium-bias applications, R is recommended that the bias select pin be connected to the mid-point between the supply rails. This is a simple procedure in split-supply applications, since this point is ground. In single-supply applications, the medium-bias mode necessitates using a voltage divider as indicated. The use of large-value resistors in the voltage divider reduces the current drain of the divider from the supply line. However, large-value resistors used in conjunction with a large-value capacitor requires significant time to charge up to the supply midpoint after the supply is switched on. A voltage other than the midpoint may be used if it is within the voltages specified in the table of Figure 106.



BIAS MODE	BIAS-SELECT VOLTAGE (single supply)
Low	$V_{DD}$
Medium	1 V to $V_{DD} - 1$ V
High	GND

**Figure 106. Bias Selection for Single-Supply Applications**

## APPLICATION INFORMATION

### input characteristics

The TLC271 is specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. Note that the lower range limit includes the negative rail, while the upper range limit is specified at  $V_{DD} - 1\text{ V}$  at  $T_A = 25^\circ\text{C}$  and at  $V_{DD} - 1.5\text{ V}$  at all other temperatures.

The use of the polysilicon-gate process and the careful input circuit design gives the TLC271 very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically  $0.1\ \mu\text{V}/\text{month}$ , including the first month of operation.

Because of the extremely high input impedance and resulting low bias current requirements, the TLC271 is well suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 101 in the Parameter Measurement Information section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 107).

The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.

### noise performance

The noise specifications in operational amplifier circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TLC271 results in a very low noise current, which is insignificant in most applications. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than  $50\ \text{k}\Omega$ , since bipolar devices exhibit greater noise currents.

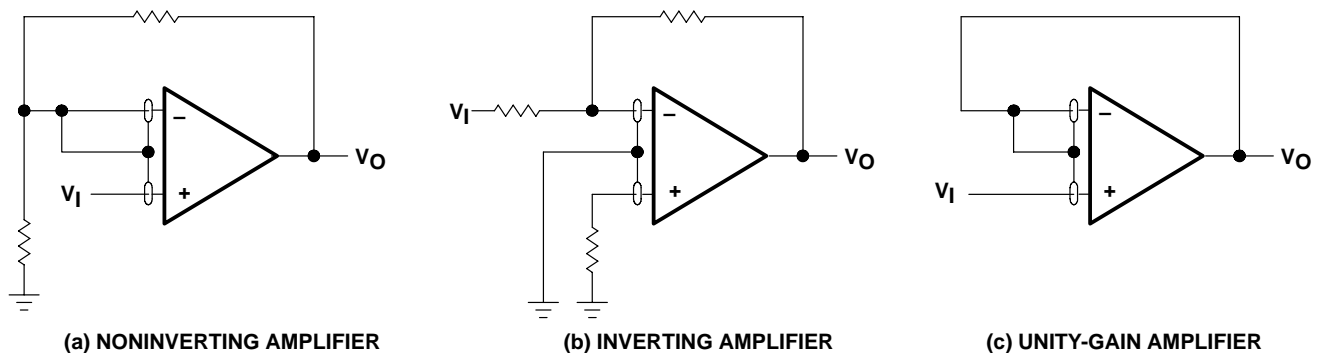
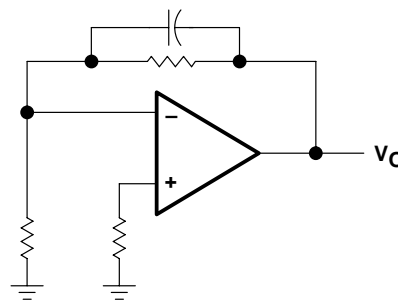


Figure 107. Guard-Ring Schemes

**APPLICATION INFORMATION**

**feedback**

Operational amplifier circuits almost always employ feedback, and since feedback is the first prerequisite for oscillation, a little caution is appropriate. Most oscillation problems result from driving capacitive loads and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 108). The value of this capacitor is optimized empirically.



**Figure 108. Compensation for Input Capacitance**

**electrostatic discharge protection**

The TLC271 incorporates an internal electrostatic-discharge (ESD) protection circuit that prevents functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised, however, when handling these devices as exposure to ESD may result in the degradation of the device parametric performance. The protection circuit also causes the input bias currents to be temperature dependent and have the characteristics of a reverse-biased diode.

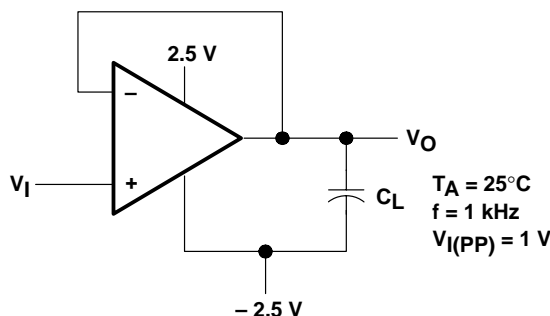
**latch-up**

Because CMOS devices are susceptible to latch-up due to their inherent parasitic thyristors, the TLC271 inputs and output were designed to withstand –100-mA surge currents without sustaining latchup; however, techniques should be used to reduce the chance of latch-up whenever possible. Internal protection diodes should not by design be forward biased. Applied input and output voltage should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 μF typical) located across the supply rails as close to the device as possible.

The current path established if latch-up occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and/or voltages on either the output or inputs that exceed the supply voltage. Once latch-up occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latch-up occurring increases with increasing temperature and supply voltages.

**output characteristics**

The output stage of the TLC271 is designed to sink and source relatively high amounts of current (see Typical Characteristics). If the output is subjected to a short-circuit condition, this high current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

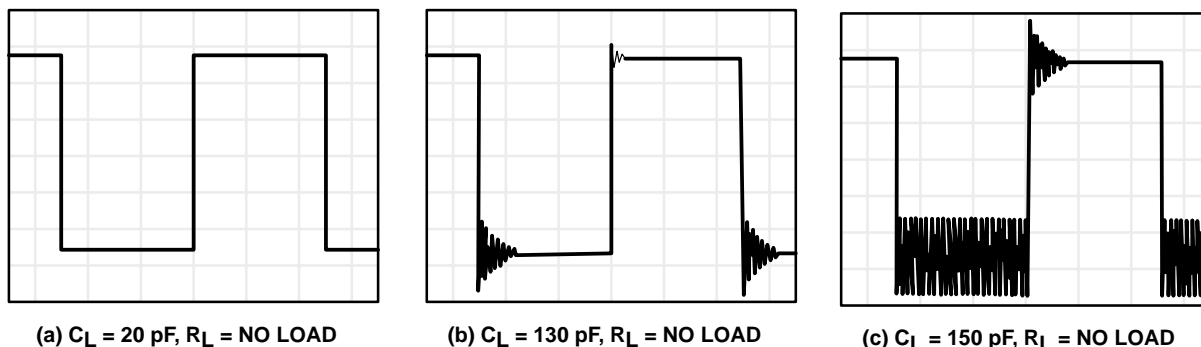


**Figure 109. Test Circuit for Output Characteristics**

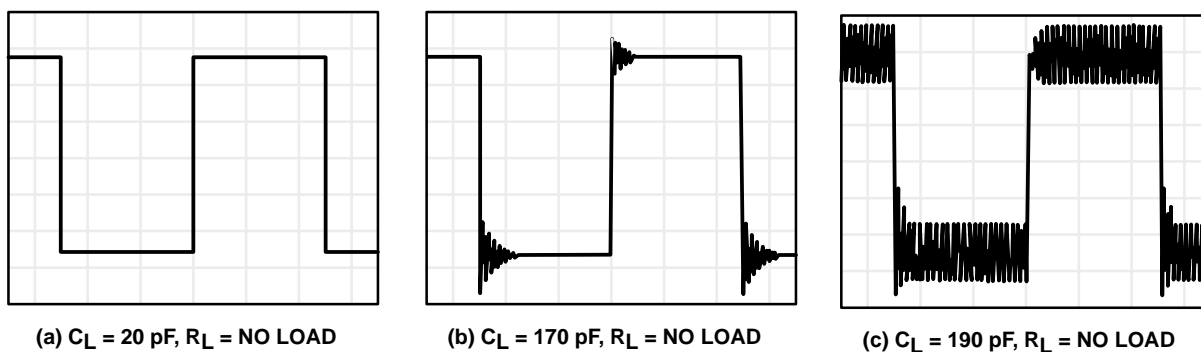
**APPLICATION INFORMATION**

**output characteristics (continued)**

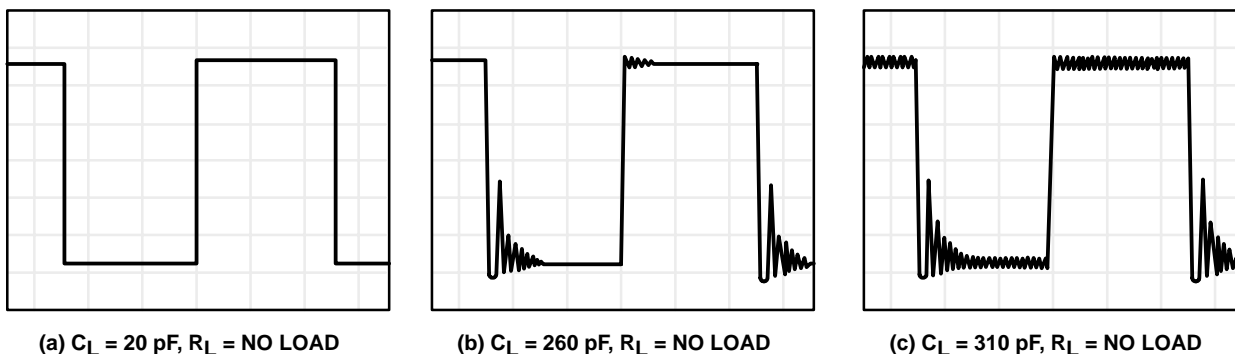
All operating characteristics of the TLC271 were measured using a 20-pF load. The devices drive higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation (see Figures 110, 111, and 112). In many cases, adding some compensation in the form of a series resistor in the feedback loop alleviates the problem.



**Figure 110. Effect of Capacitive Loads in High-Bias Mode**



**Figure 111. Effect of Capacitive Loads in Medium-Bias Mode**

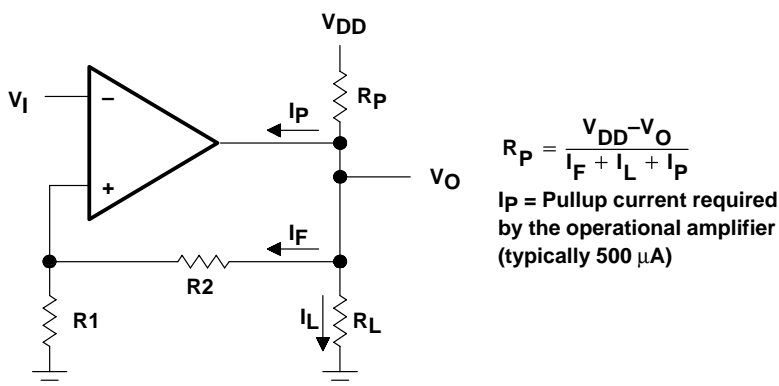


**Figure 112. Effect of Capacitive Loads in Low-Bias Mode**

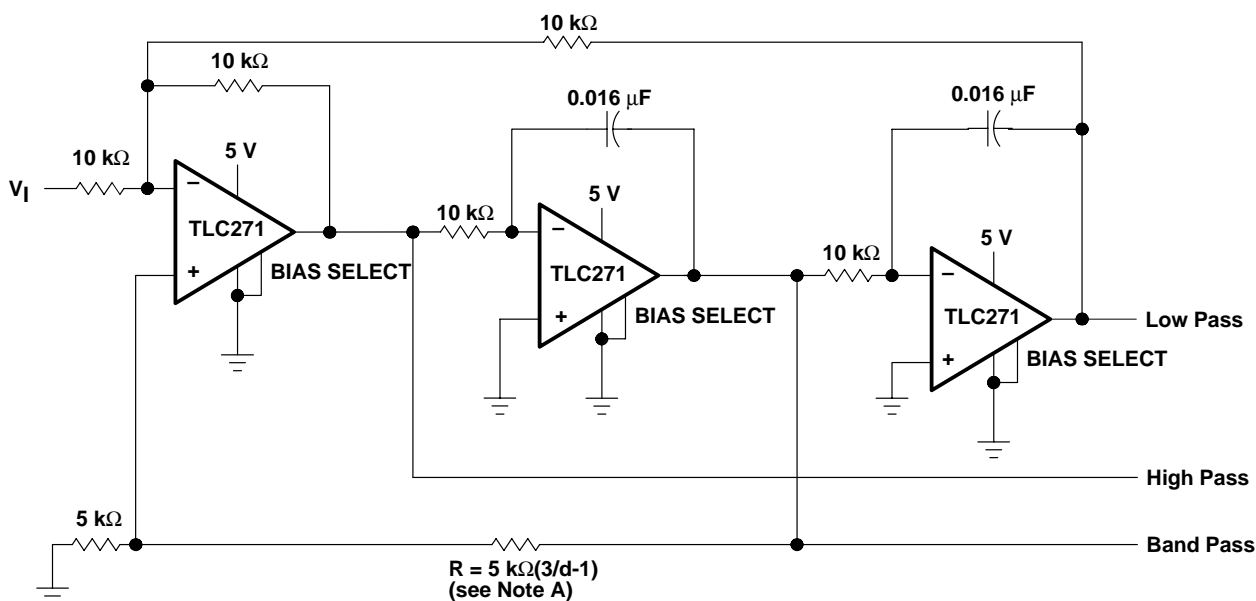
**APPLICATION INFORMATION**

**output characteristics (continued)**

Although the TLC271 possesses excellent high-level output voltage and current capability, methods are available for boosting this capability, if needed. The simplest method involves the use of a pullup resistor ( $R_P$ ) connected from the output to the positive supply rail (see Figure 113). There are two disadvantages to the use of this circuit. First, the NMOS pulldown transistor, N4 (see equivalent schematic) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on-resistance between approximately 60  $\Omega$  and 180  $\Omega$ , depending on how hard the operational amplifier input is driven. With very low values of  $R_P$ , a voltage offset from 0 V at the output occurs. Secondly, pullup resistor  $R_P$  acts as a drain load to N4 and the gain of the operational amplifier is reduced at output voltage levels where N5 is not supplying the output current.



**Figure 113. Resistive Pullup to Increase  $V_{OH}$**

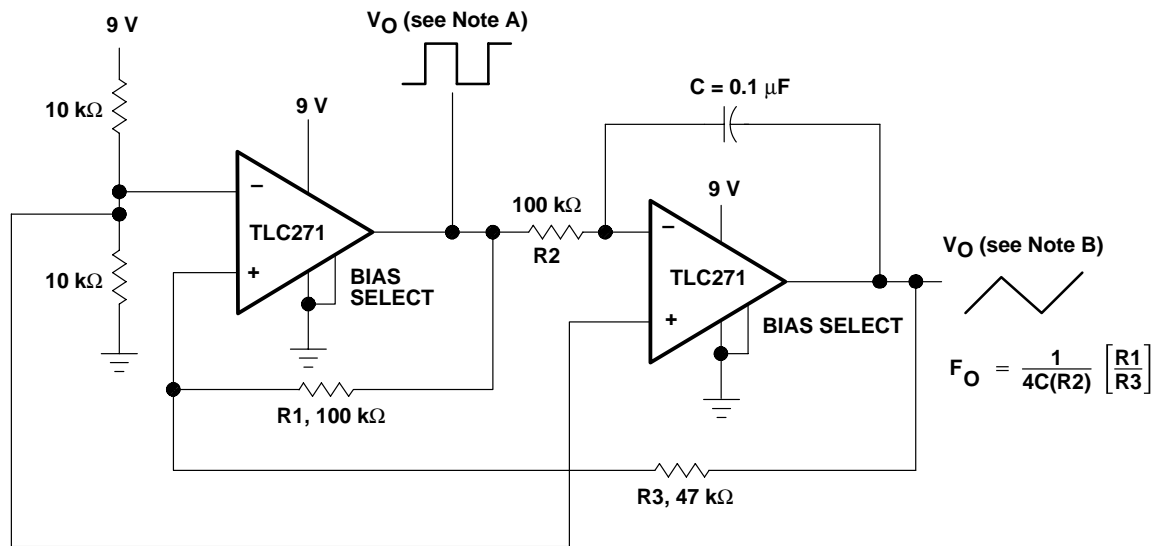


NOTE B: d = damping factor, I/O

**Figure 114. State-Variable Filter**

**APPLICATION INFORMATION**

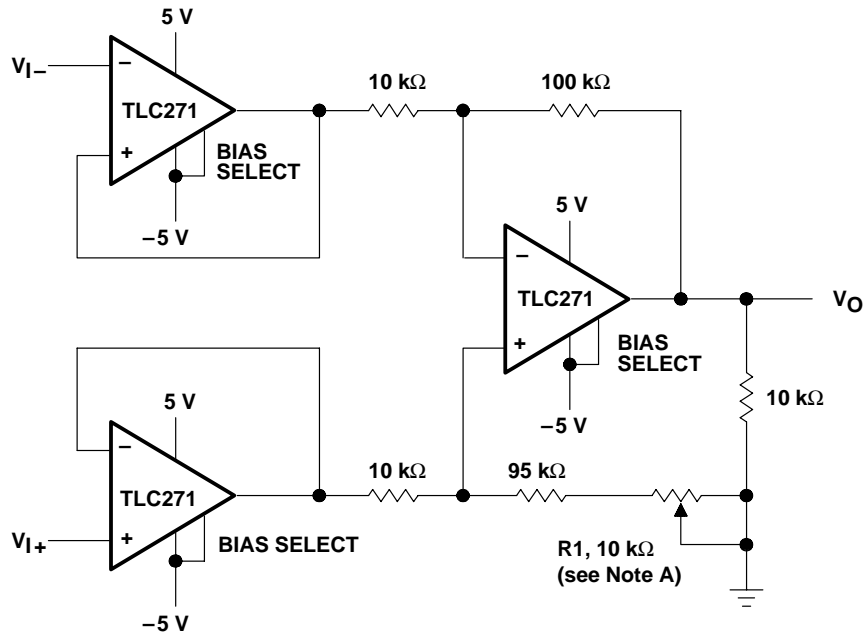
**output characteristics (continued)**



- NOTES: A.  $V_{O(PP)} = 8\text{ V}$   
 B.  $V_{O(PP)} = 4\text{ V}$

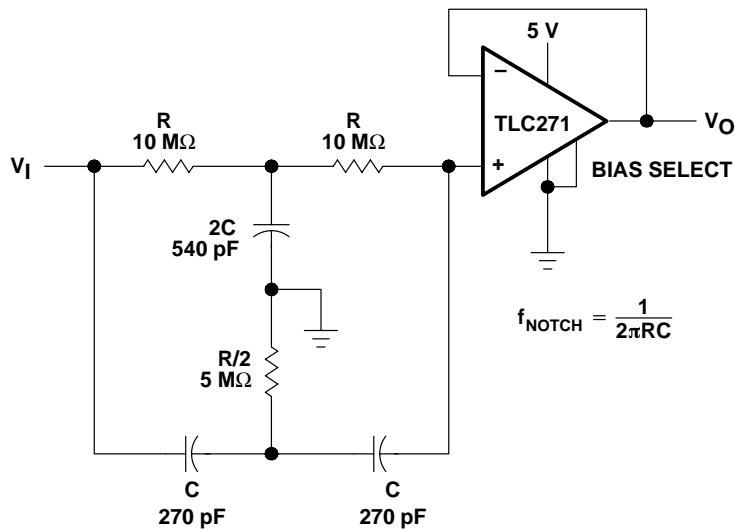
**Figure 115. Single-Supply Function Generator**

**APPLICATION INFORMATION (HIGH-BIAS MODE)**



NOTE A: CMRR adjustment must be noninductive.

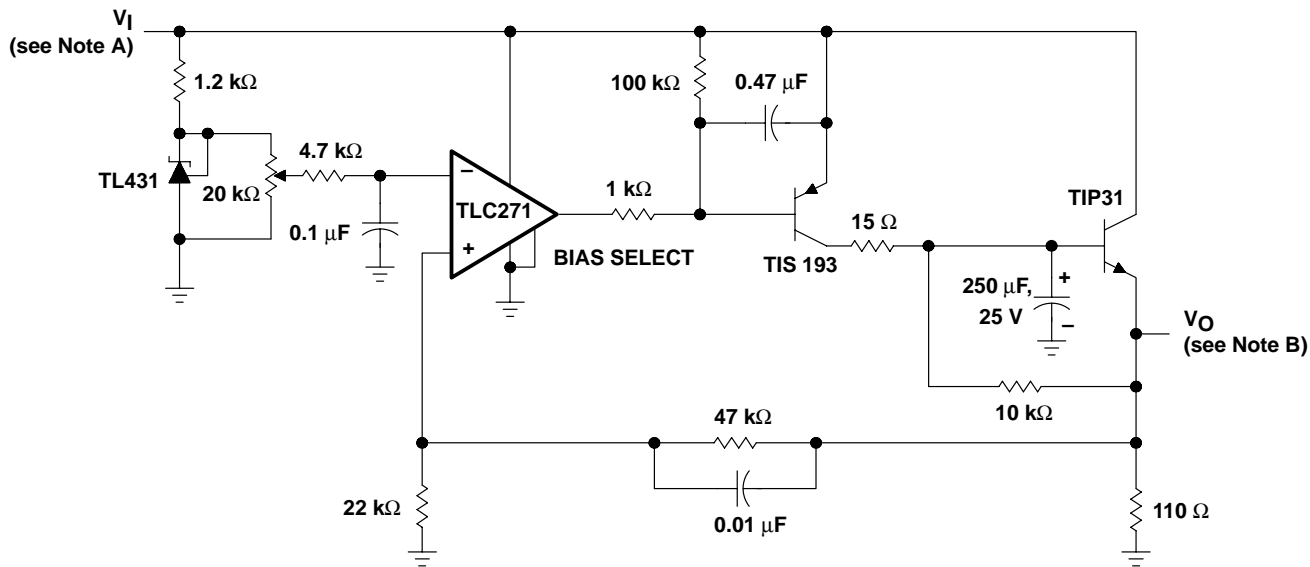
**Figure 116. Low-Power Instrumentation Amplifier**



**Figure 117. Single-Supply Twin-T Notch Filter**



APPLICATION INFORMATION (HIGH-BIAS MODE)



NOTES: A.  $V_I = 3.5$  to  $15$  V  
 B.  $V_O = 2.0$  V,  $0$  to  $1$  A

Figure 118. Logic-Array Power Supply

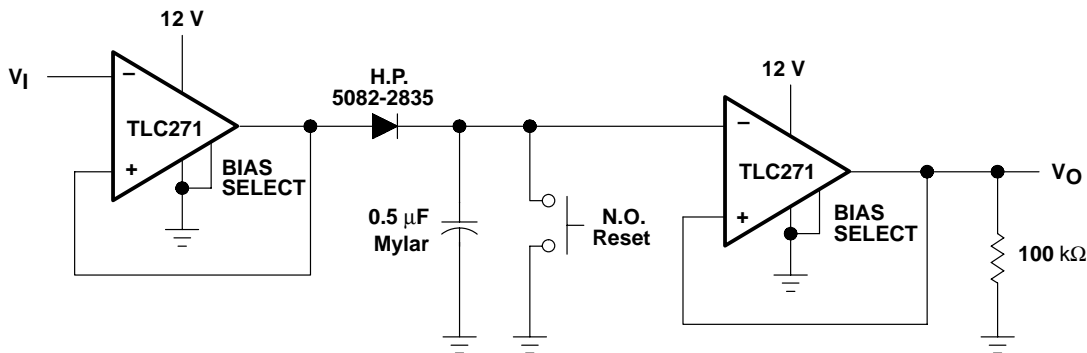
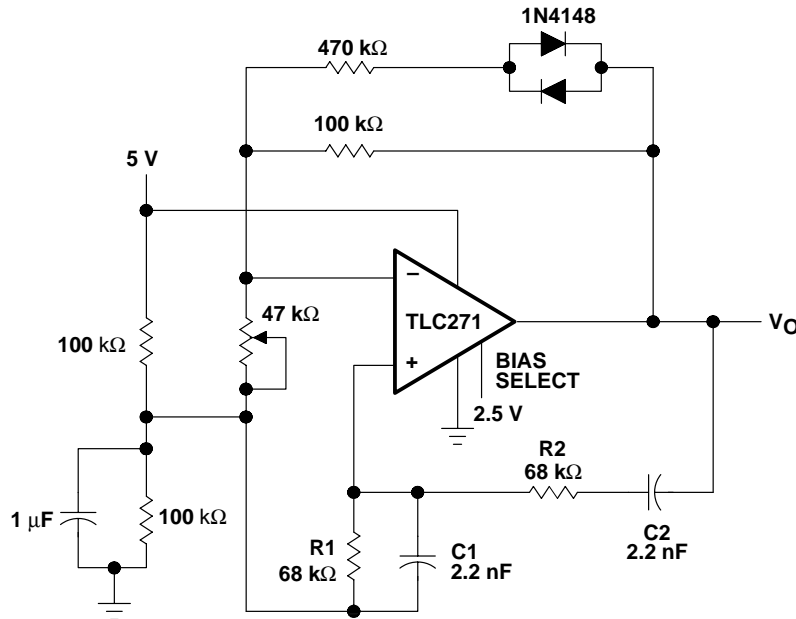


Figure 119. Positive-Peak Detector

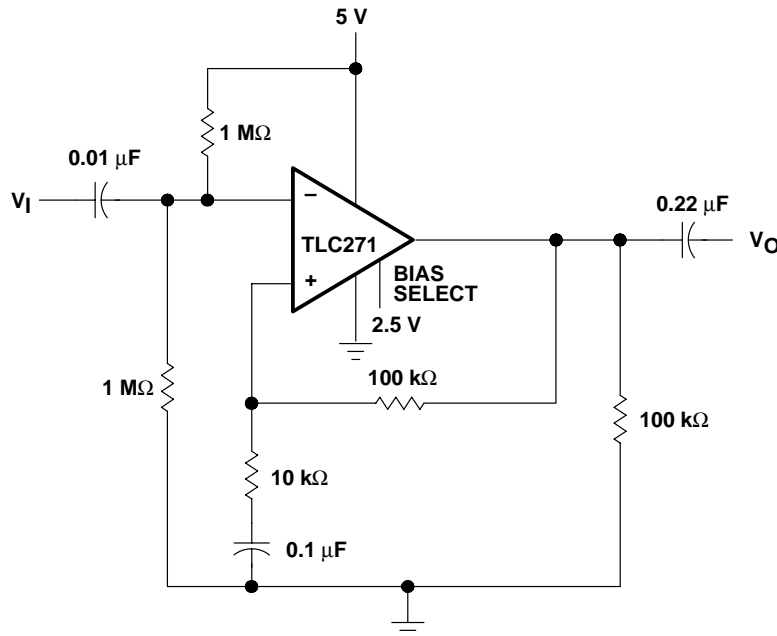
**APPLICATION INFORMATION (MEDIUM-BIAS MODE)**



NOTES: A.  $V_{O(PP)} = 2\text{ V}$

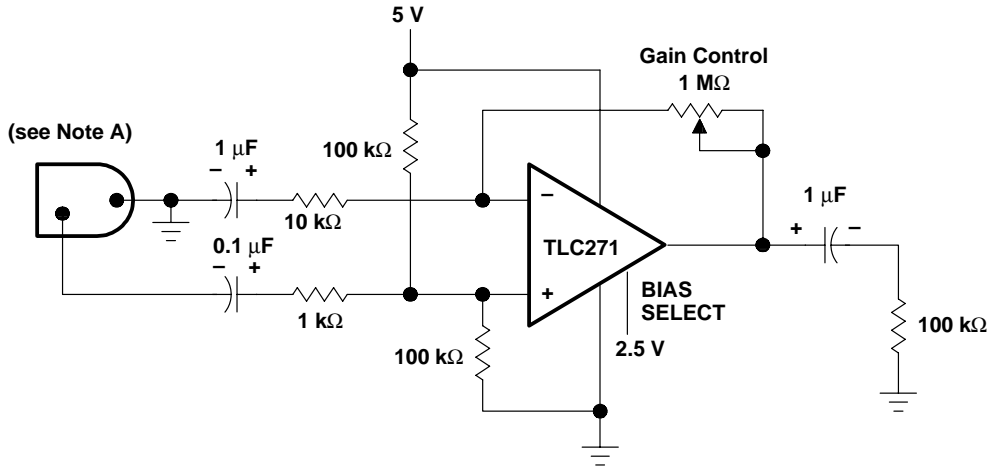
B.  $f_o = \frac{1}{2\pi\sqrt{R_1R_2C_1C_2}}$

**Figure 120. Wein Oscillator**



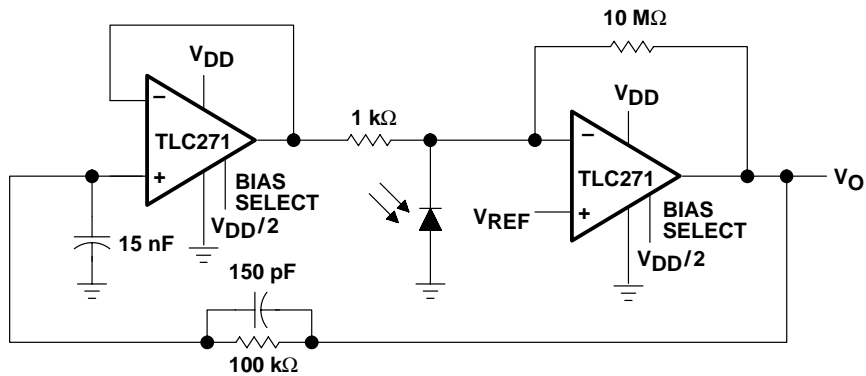
**Figure 121. Single-Supply AC Amplifier**

APPLICATION INFORMATION (MEDIUM-BIAS MODE)



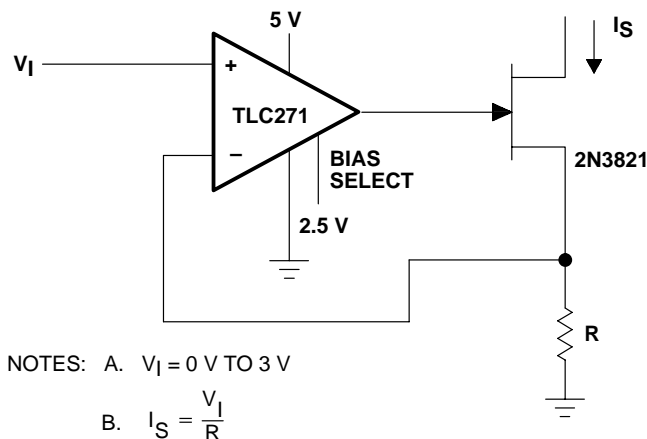
NOTE A: Low to medium impedance dynamic mike

Figure 122. Microphone Preamplifier



NOTES: A.  $V_{DD} = 4\text{ V to }15\text{ V}$   
 B.  $V_{ref} = 0\text{ V to }V_{DD}-2\text{ V}$

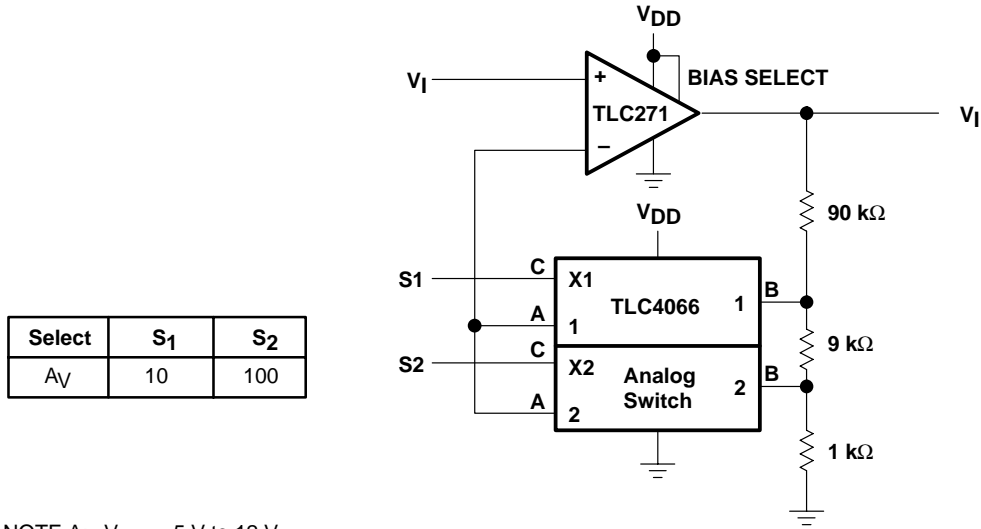
Figure 123. Photo-Diode Amplifier With Ambient Light Rejection



NOTES: A.  $V_I = 0\text{ V TO }3\text{ V}$   
 B.  $I_S = \frac{V_I}{R}$

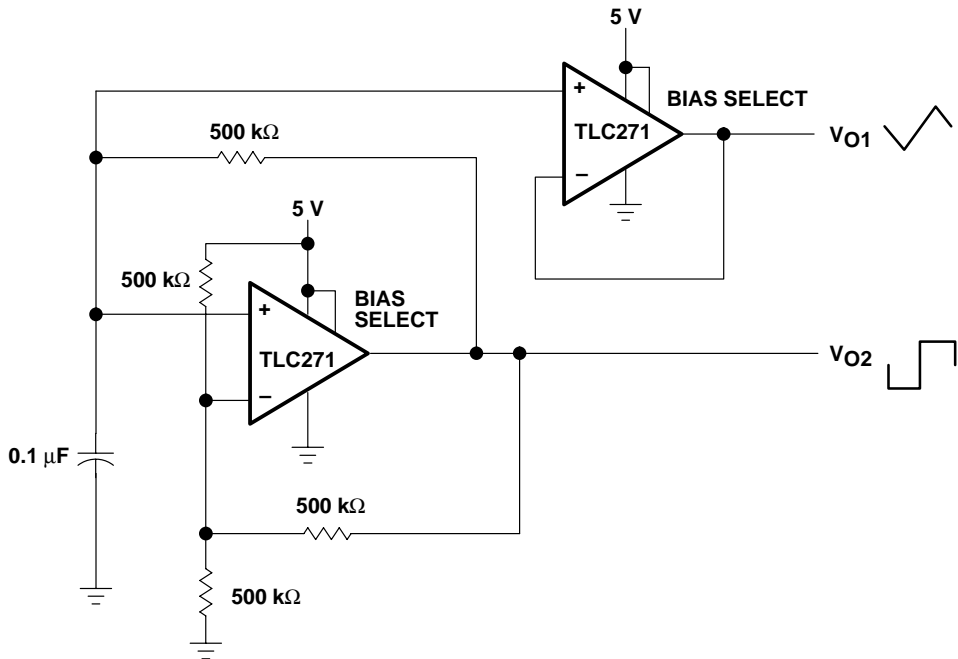
Figure 124. Precision Low-Current Sink

**APPLICATION INFORMATION (LOW-BIAS MODE)**



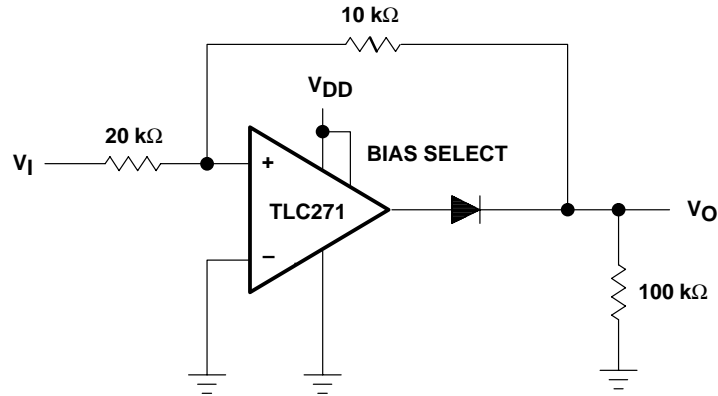
NOTE A: V<sub>DD</sub> = 5 V to 12 V

**Figure 125. Amplifier With Digital Gain Selection**



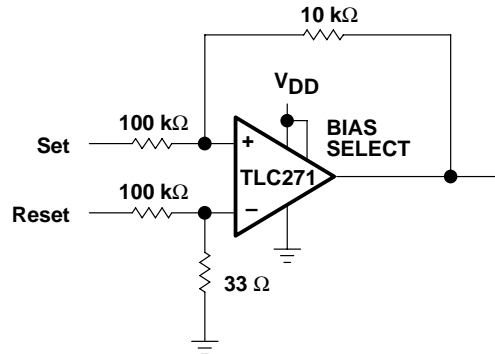
**Figure 126. Multivibrator**

APPLICATION INFORMATION (LOW-BIAS MODE)



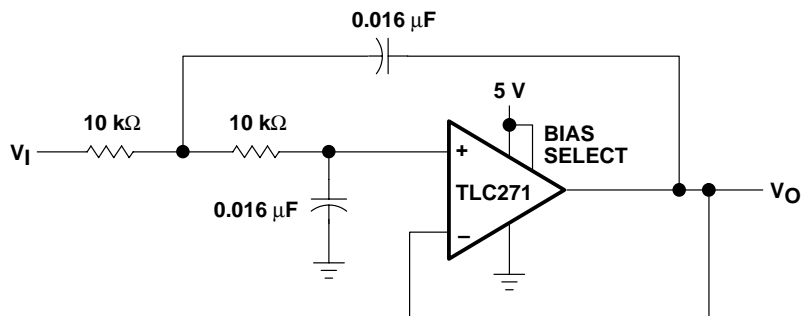
NOTE A:  $V_{DD} = 5\text{ V to }16\text{ V}$

Figure 127. Full-Wave Rectifier



NOTE A:  $V_{DD} = 5\text{ V to }16\text{ V}$

Figure 128. Set/Reset Flip-Flop



NOTE A: Normalized to  $F_C = 1\text{ kHz}$  and  $R_L = 10\text{ k}\Omega$

Figure 129. Two-Pole Low-Pass Butterworth Filter

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">TLC271ACD</a>	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	271AC
TLC271ACD.A	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	271AC
<a href="#">TLC271ACDR</a>	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	271AC
TLC271ACDR.A	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	271AC
<a href="#">TLC271ACP</a>	Active	Production	PDIP (P)   8	50   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLC271ACP
TLC271ACP.A	Active	Production	PDIP (P)   8	50   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLC271ACP
<a href="#">TLC271ACPS</a>	Active	Production	SO (PS)   8	80   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P271A
TLC271ACPS.A	Active	Production	SO (PS)   8	80   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P271A
<a href="#">TLC271ACPSR</a>	Active	Production	SO (PS)   8	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P271A
TLC271ACPSR.A	Active	Production	SO (PS)   8	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P271A
<a href="#">TLC271AID</a>	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	271AI
TLC271AID.A	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	271AI
TLC271AIDG4	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	271AI
<a href="#">TLC271AIDR</a>	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	271AI
TLC271AIDR.A	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	271AI
<a href="#">TLC271AIP</a>	Active	Production	PDIP (P)   8	50   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLC271AIP
TLC271AIP.A	Active	Production	PDIP (P)   8	50   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLC271AIP
<a href="#">TLC271BCD</a>	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	271BC
TLC271BCD.A	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	271BC
<a href="#">TLC271BCDR</a>	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	271BC
TLC271BCDR.A	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	271BC
<a href="#">TLC271BCP</a>	Active	Production	PDIP (P)   8	50   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLC271BCP
TLC271BCP.A	Active	Production	PDIP (P)   8	50   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLC271BCP
<a href="#">TLC271BCPS</a>	Active	Production	SO (PS)   8	80   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P271B
TLC271BCPS.A	Active	Production	SO (PS)   8	80   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P271B
<a href="#">TLC271BID</a>	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	271BI
TLC271BID.A	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	271BI
TLC271BIDG4	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	271BI
<a href="#">TLC271BIDR</a>	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	271BI

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLC271BIDR.A	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	271BI
<a href="#">TLC271BIP</a>	Active	Production	PDIP (P)   8	50   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLC271BIP
TLC271BIP.A	Active	Production	PDIP (P)   8	50   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLC271BIP
<a href="#">TLC271CD</a>	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	271C
TLC271CD.A	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	271C
<a href="#">TLC271CP</a>	Active	Production	PDIP (P)   8	50   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLC271CP
TLC271CP.A	Active	Production	PDIP (P)   8	50   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLC271CP
<a href="#">TLC271CPS</a>	Active	Production	SO (PS)   8	80   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P271
TLC271CPS.A	Active	Production	SO (PS)   8	80   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P271
<a href="#">TLC271CPSR</a>	Active	Production	SO (PS)   8	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P271
TLC271CPSR.A	Active	Production	SO (PS)   8	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P271
<a href="#">TLC271CPW</a>	Active	Production	TSSOP (PW)   8	150   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P271
TLC271CPW.A	Active	Production	TSSOP (PW)   8	150   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P271
<a href="#">TLC271CPWR</a>	Active	Production	TSSOP (PW)   8	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P271
TLC271CPWR.A	Active	Production	TSSOP (PW)   8	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P271
TLC271CPWRG4	Active	Production	TSSOP (PW)   8	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P271
<a href="#">TLC271ID</a>	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	271I
TLC271ID.A	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	271I
<a href="#">TLC271IDR</a>	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	271I
TLC271IDR.A	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	271I
<a href="#">TLC271IP</a>	Active	Production	PDIP (P)   8	50   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLC271IP
TLC271IP.A	Active	Production	PDIP (P)   8	50   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLC271IP
<a href="#">TLC271MDR</a>	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	271M
TLC271MDR.A	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	271M
<a href="#">TLC271MDRG4</a>	Obsolete	Production	SOIC (D)   8	-	-	Call TI	Call TI	-55 to 125	

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC271ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC271ACPSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
TLC271AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC271BCDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC271BIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC271CPSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
TLC271CPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLC271IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC271MDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC271ACDR	SOIC	D	8	2500	353.0	353.0	32.0
TLC271ACPSR	SO	PS	8	2000	353.0	353.0	32.0
TLC271AIDR	SOIC	D	8	2500	353.0	353.0	32.0
TLC271BCDR	SOIC	D	8	2500	353.0	353.0	32.0
TLC271BIDR	SOIC	D	8	2500	340.5	338.1	20.6
TLC271CPSR	SO	PS	8	2000	353.0	353.0	32.0
TLC271CPWR	TSSOP	PW	8	2000	353.0	353.0	32.0
TLC271IDR	SOIC	D	8	2500	353.0	353.0	32.0
TLC271MDR	SOIC	D	8	2500	350.0	350.0	43.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TLC271ACD	D	SOIC	8	75	507	8	3940	4.32
TLC271ACD.A	D	SOIC	8	75	507	8	3940	4.32
TLC271ACP	P	PDIP	8	50	506	13.97	11230	4.32
TLC271ACP.A	P	PDIP	8	50	506	13.97	11230	4.32
TLC271ACPS	PS	SOP	8	80	530	10.5	4000	4.1
TLC271ACPS.A	PS	SOP	8	80	530	10.5	4000	4.1
TLC271AID	D	SOIC	8	75	507	8	3940	4.32
TLC271AID.A	D	SOIC	8	75	507	8	3940	4.32
TLC271AIDG4	D	SOIC	8	75	507	8	3940	4.32
TLC271AIP	P	PDIP	8	50	506	13.97	11230	4.32
TLC271AIP.A	P	PDIP	8	50	506	13.97	11230	4.32
TLC271BCD	D	SOIC	8	75	507	8	3940	4.32
TLC271BCD.A	D	SOIC	8	75	507	8	3940	4.32
TLC271BCP	P	PDIP	8	50	506	13.97	11230	4.32
TLC271BCP.A	P	PDIP	8	50	506	13.97	11230	4.32
TLC271BCPS	PS	SOP	8	80	530	10.5	4000	4.1
TLC271BCPS.A	PS	SOP	8	80	530	10.5	4000	4.1
TLC271BID	D	SOIC	8	75	507	8	3940	4.32
TLC271BID.A	D	SOIC	8	75	507	8	3940	4.32
TLC271BIDG4	D	SOIC	8	75	507	8	3940	4.32
TLC271BIP	P	PDIP	8	50	506	13.97	11230	4.32
TLC271BIP.A	P	PDIP	8	50	506	13.97	11230	4.32
TLC271CD	D	SOIC	8	75	507	8	3940	4.32
TLC271CD.A	D	SOIC	8	75	507	8	3940	4.32
TLC271CP	P	PDIP	8	50	506	13.97	11230	4.32
TLC271CP.A	P	PDIP	8	50	506	13.97	11230	4.32
TLC271CPS	PS	SOP	8	80	530	10.5	4000	4.1
TLC271CPS.A	PS	SOP	8	80	530	10.5	4000	4.1
TLC271CPW	PW	TSSOP	8	150	530	10.2	3600	3.5

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<b>Device</b>	<b>Package Name</b>	<b>Package Type</b>	<b>Pins</b>	<b>SPQ</b>	<b>L (mm)</b>	<b>W (mm)</b>	<b>T (μm)</b>	<b>B (mm)</b>
TLC271CPW.A	PW	TSSOP	8	150	530	10.2	3600	3.5
TLC271ID	D	SOIC	8	75	507	8	3940	4.32
TLC271ID.A	D	SOIC	8	75	507	8	3940	4.32
TLC271IP	P	PDIP	8	50	506	13.97	11230	4.32
TLC271IP.A	P	PDIP	8	50	506	13.97	11230	4.32



D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

### NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
 EXPOSED METAL SHOWN  
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# MECHANICAL DATA

PS (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



PS (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001 variation BA.

PW0008A



**PACKAGE OUTLINE**  
**TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.

# EXAMPLE BOARD LAYOUT

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:10X



SOLDER MASK DETAILS  
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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