THVD1330 32-Mbps 3.3-V RS485 Transceiver with IEC ESD Protection

1 Features

- Meets or exceeds the requirements of the TIA/EIA-485A standard
- 3 V to 3.6 V supply voltage
- Half-Duplex RS-422/RS-485
- High speed operation: 32 Mbps max data rate
- Bus I/O protection
  - ± 16 kV HBM ESD
  - ± 8 kV IEC 61000-4-2 Contact Discharge
- Extended industrial temperature range: −40°C to 125°C
- Bus common mode range: −7 V to 12 V
- Low shutdown current 5 µA max
- Glitch-free power-up or down for hot plug-in capability
- Open, short, and idle bus failsafe receiver

2 Applications

- Wireless infrastructure
- Factory automation & control
- Building automation
- Grid infrastructure

3 Description

THVD1330 is a robust half-duplex RS-485 transceiver for industrial applications. The bus pins are immune to high levels of IEC Contact Discharge ESD events eliminating the need of additional system level protection components. Both the transmitter and receiver are capable of operating at maximum 32 Mbps signaling rate. The device is optimized for small propagation delay variation to support time-sensitive applications such as Baseband unit (BBU) and Remote radio unit (RRU).

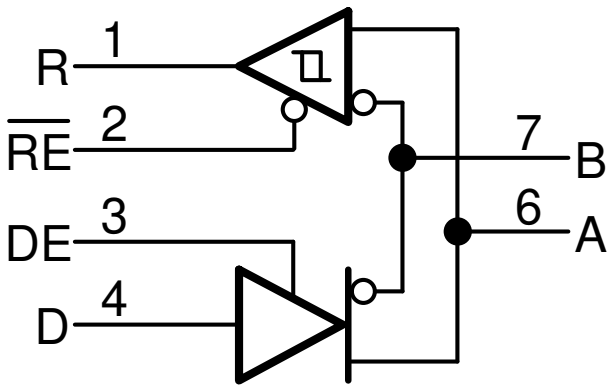
The device operates from a single 3.3 V supply. The wide common-mode voltage range and low input leakage on bus pins make THVD1330 suitable for multi-point applications over long cable runs.

THVD1330 is available in industry standard 8-pin SOIC package for drop-in compatibility. The device is characterized from –40°C to 125°C.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
THVD1330	SOIC (D, 8)	4.9 mm × 6 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematic

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4 Revision History

Date	Revision	Notes
September 2023	*	Initial release

5 Pin Configuration and Functions

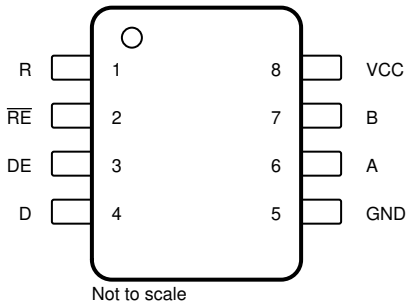


Figure 5-1. D Package, 8-Pin SOIC (Top View)

Table 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
R	1	Digital output	Receive data output
$\overline{RE}$	2	Digital input	Receiver enable, active low (internal pull-up)
DE	3	Digital input	Driver enable, active high (internal pull-down)
D	4	Digital input	Driver data input
GND	5	Ground	Local device ground
A	6	Bus input/output	Bus I/O port, A (complementary to B)
B	7	Bus input/output	Bus I/O port, B (complementary to A)
V_{CC}	8	Power	3.3 V supply

6 Specifications

6.1 Absolute Maximum Ratings

(1) (2)

		MIN	MAX	UNIT
Supply voltage	V_{CC}	–0.3	6	V
Bus voltage	Voltage at any bus pin (A or B)	–9	14	V
Input voltage	Voltage at any logic pin (D, DE or $\overline{RE}$)	–0.5	6	V
Receiver output current	I_O	–11	11	mA
Junction temperature, T_J			170	°C
Storage temperature, T_{stg}		–55	145	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to Ground terminal

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Contact discharge, per IEC61000-4-2	Bus terminals and GND	±8,000	V
		Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	Bus terminals and GND	±16,000	
			All pins except bus terminals and GND	±4,000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)		±1,000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
V_I	Input voltage at any bus terminal (separately or common mode)(1)	–7		12	V
V_{IH}	High-level input voltage (driver, driver enable, and receiver enable inputs)	2		V_{CC}	V
V_{IL}	Low-level input voltage (driver, driver enable, and receiver enable inputs)	0		0.8	V
V_{ID}	Differential input voltage	–12		12	V
I_O	Output current, driver	–60		60	mA
I_{OR}	Output current, receiver	–8		8	mA
R_L	Differential load resistance	54	60		Ω
$1/t_{UI}$	Signaling rate			32	Mbps
T_A	Operating ambient temperature	–40		125	°C

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

6.4 Thermal Information

THERMAL METRIC(1)		THVD1330 D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	116.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	63.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	62.6	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

over operating free-air temperature range, Typical values are at 25 ℃ and 3.3 V supply (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
Driver								
$\lvert V_{OD}\rvert$	Driver differential output voltage magnitude	R_L = 60 Ω, -7 V ≤ V_{test} ≤ 12 V, See Figure 6-1			1.5			V
		R_L = 54 Ω, See Figure 6-2			1.5			V
		No load			2		3.6	V
$\Delta\lvert V_{OD}\rvert$	Change in differential output voltage	R_L = 54 Ω, See Figure 6-2			–50		50	mV
V_{OC}	Common-mode output voltage	R_L = 54 Ω, See Figure 6-2			1.4		2.5	V
$V_{OC(SS)}$	Change in steady-state common-mode output voltage	R_L = 54 Ω , See Figure 6-2			–50		50	mV
$V_{OC(pp)}$	Peak-to-peak common-mode output voltage	R_L = 54 Ω , C_L=50pF, PRR=500KHz, See Figure 6-2				400		mV
I_{OS}	Short-circuit output current	DE = V_{CC}, -7 V <V_O < 12 V, Voltage applied on one bus line with other bus line floating			–250		250	mA
C_{OD}	Differential output capacitance	V_I=0.4 sin (4E6πt) + 0.5 V, DE=0				16		pF
Receiver								
I_I	Bus input current		V_{CC} = 3.6 V	V_I = 12 V		200	500	μA
				V_I = -7 V	–400	–200		
			V_{CC} = 0 V	V_I = 12 V		250	500	
				V_I = -7 V	–400	–150		
V_{TH+}	Positive-going input-threshold voltage(1)	Over common-mode range of (+12V,-7V)				–75	–20	mV
V_{TH-}	Negative-going input-threshold voltage(1)				–200	–125		mV
V_{HYS}	Input hysteresis					50		mV
V_{OH}	Output high voltage	I_{OH} = -8 mA			2.4			V
V_{OL}	Output low voltage	I_{OL} = 8 mA					0.4	V
I_{OZ}	Output high-impedance current	V_O = 0 V or V_{CC}, $\overline{RE}$ = V_{CC}			–1		1	μA
C_{ID}	Differential input capacitance	VI=0.4 sin (4E6πt) + 0.5 V, DE=0				15		pF
Logic								

6.5 Electrical Characteristics (continued)

over operating free-air temperature range, Typical values are at 25 °C and 3.3 V supply (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{IN}	Input current DE	V_{IN}= 5V		0		100	µA
	Input current DE	V_{IN}= 0V		0		100	µA
	Input current D	V_{IN}= 5V		–100		0	µA
	Input current D	V_{IN}= 0V		–100		0	µA
	Input current ($\overline{RE}$)	V_{IN} = 2V		–30		0	µA
		V_{IN} = 0.8V		–30		0	µA
Thermal Protection							
T_{SHDN}	Thermal shutdown threshold	Temperature rising		150	170		°C
T_{HYS}	Thermal shutdown hysteresis				10		°C
Supply							
I_{CC}	Supply current (quiescent)	Driver and receiver enabled	$\overline{RE}$ = 0 V, DE = V_{CC}, No load			2	mA
		Driver enabled, receiver disabled	$\overline{RE}$ = V_{CC}, DE = V_{CC}, No load			1.5	mA
		Driver disabled, receiver enabled	$\overline{RE}$ = 0 V, DE = 0 V, No load			1.5	mA
		Driver and receiver disabled	$\overline{RE}$ = V_{CC}, DE = 0 V, D = V_{CC}, No load			5	µA

(1) Under any specific conditions, V_{TH+} is assured to be at least V_{HYS} higher than $V_{TH–}$.

6.6 Switching Characteristics

Over recommended operating conditions

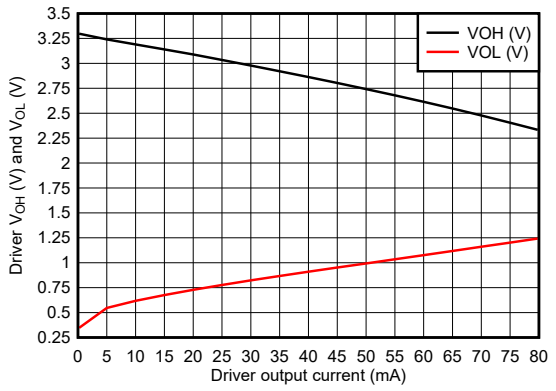
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Driver: 32Mbps							
t_r, t_f	Differential output rise/fall time	R_L = 54Ω, C_L = 50 pF, PRR=500KHz, Across full range of process, voltage and temperature	See Figure 6-3	3	4.5	10	ns
t_{PHL}, t_{PLH}	Propagation delay			5	8.5	16	ns
$t_{SK(P)}$	Pulse skew, $\lvert t_{PHL} - t_{PLH} \rvert$					1.5	ns
$t_{SK(PP)}$	Part to part skew					6	ns
t_{PHL}, t_{PLH}	Propagation delay	R_L = 54Ω , C_L = 50pF, V_{CC} = 3.3 V +/ 3%, T_A = -20°C to 85°C		6		13.8	ns
t_{PHZ}	Disable time	PRR = 500KHz, R_L = 110 Ω, C_L = 50 pF	See Figure 6-4 and Figure 6-5			25	ns
t_{PLZ}	Disable time	PRR = 500KHz, R_L = 110 Ω, C_L = 50 pF				26	ns
t_{PZH}	Enable time	$\overline{RE}$ = 0 V, PRR = 500KHz, R_L = 110 Ω, C_L = 50 pF				31	ns
t_{PZL}						26	ns
t_{PZH2}	Enable time	$\overline{RE}$ = V_{CC}, PRR = 100KHz, R_L = 110 Ω± 1%, C_L = 50 pF ± 20%, 50% to 2.3V				6	µs
t_{PZL2}						6	µs
Receiver: 32Mbps							

6.6 Switching Characteristics (continued)

Over recommended operating conditions

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_r, t_f	Differential output rise/fall time	PRR = 500KHz, C_L = 15pF, Across process, full range of voltage and ambient temperature	See Figure 6-6	1	2	5	ns
t_{PHL}, t_{PLH}	Propagation delay			12.5	20	25	ns
$t_{SK(P)}$	Pulse skew, $\|t_{PHL} - t_{PLH}\|$					1.5	ns
$t_{SK(PP)}$	Part to part skew					8	ns
t_{PHL}, t_{PLH}	Propagation delay	PRR = 500KHz, C_L = 15pF, V_{CC} = 3.3V +/- 3%, T_A = -20°C to 85°C		13		20	ns
t_{PHL}, t_{PLH}	Propagation delay	PRR = 500KHz, C_L = 30pF, V_{CC} = 3.3V +/- 3%, T_A = -20°C to 85°C		13.4		21	ns
t_{PHZ}	Output disable time from high-level	PRR = 500KHz, C_L= 15 pF	See Figure 6-7 and Figure 6-8			20	ns
t_{PLZ}	Output disable time from low-level	PRR = 500KHz, C_L= 15 pF				15	ns
t_{PZH}	Output enable time to high-level	DE = V_{CC} , PRR = 500KHz, C_L = 15pF				15	ns
t_{PZL}	Output enable time to low-level					15	ns
t_{PZH2}	Output enable time to high-level	DE = 0V , PRR = 100KHz, 50% to 1.5V, C_L = 15pF ± 20%				6	µs
t_{PZL2}	Output enable time to low-level					6	µs

6.7 Typical Characteristics

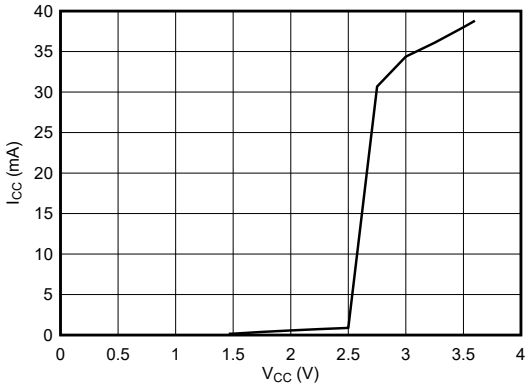


V_{CC} = 3.3 V DE = V_{CC} D = GND

Figure 6-1. Driver Output voltage vs Driver Output Current

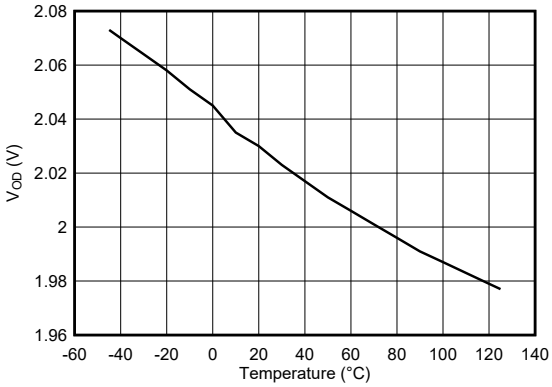
V_{CC} = 3.3 V DE = V_{CC} D = GND

Figure 6-2. Driver Differential Output voltage vs Driver Output Current



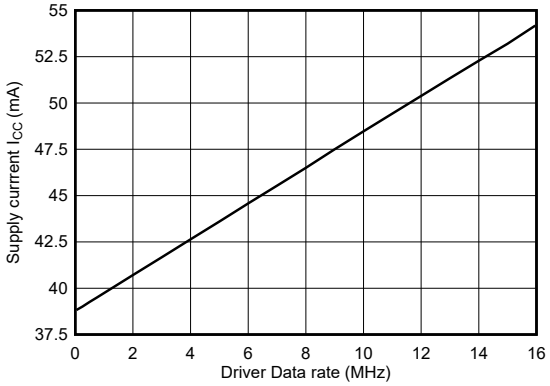
R_L = 54 Ω DE = V_{CC} D = V_{CC}
T_A = 25°C

Figure 6-3. Supply Current vs Supply Voltage



DE = V_{CC} D = V_{CC} RL = 54 Ω

Figure 6-4. Driver output differential voltage vs Temperature



R_L = 54 Ω CL = 50 pF DE = V_{CC}
Temperature = 25 °C

Figure 6-5. Supply Current vs Signal Rate

7 Parameter Measurement Information

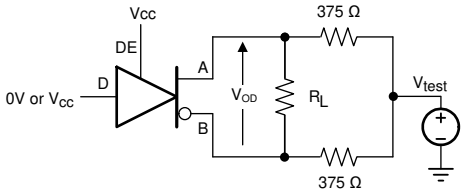


Figure 7-1. Measurement of Driver Differential Output Voltage With Common-Mode Load

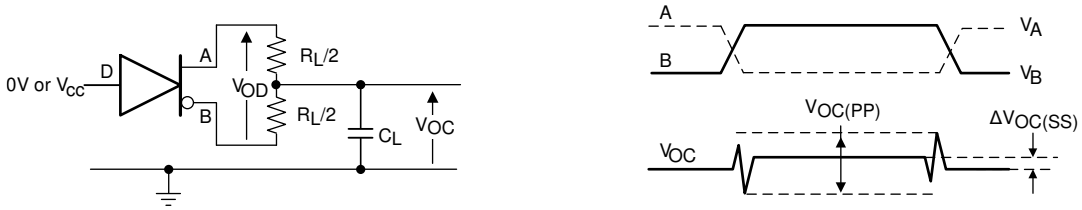
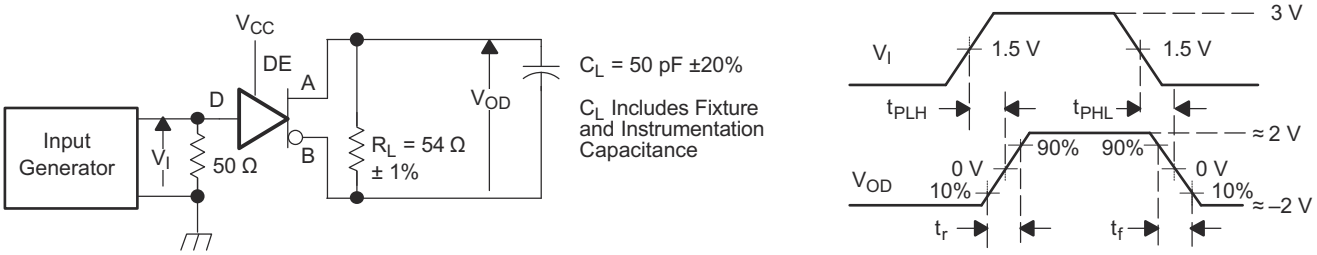
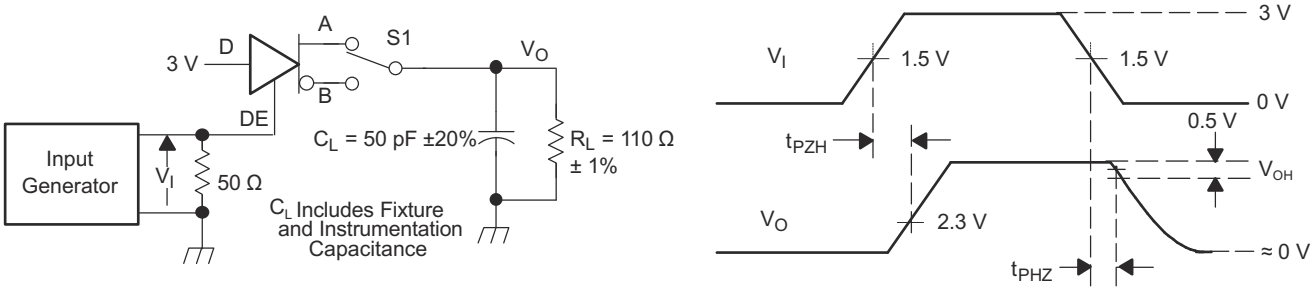


Figure 7-2. Measurement of Driver Differential and Common-Mode Output With RS-485 Load



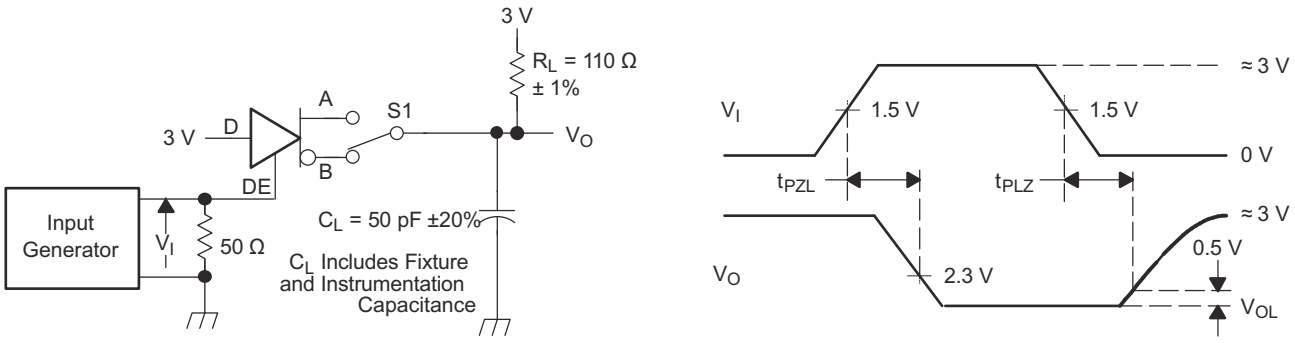
Generator: PRR = 500 kHz, 50% Duty Cycle, t_r < 60 ns, t_f < 6 ns Z_O = 50 Ω

Figure 7-3. Driver Switching Test Circuit and Voltage Waveforms



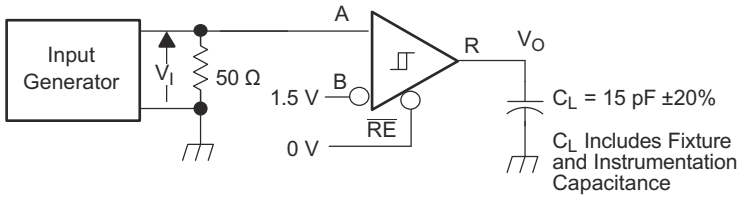
Generator: PRR = 500 kHz, 50% Duty Cycle, t_r < 60 ns, t_f < 6 ns Z_O = 50 Ω

Figure 7-4. Driver High-Level Enable and Disable Time Test Circuit and Voltage Waveforms



Generator: PRR = 500 kHz, 50% Duty Cycle, t_r < 60 ns, t_f < 6 ns Z_O = 50 Ω

Figure 7-5. Driver Low-Level Output Enable and Disable Time Test Circuit and Voltage Waveforms



Generator: PRR = 500 kHz, 50% Duty Cycle, t_r <6 ns, t_f <6 ns, Z_o = 50 Ω

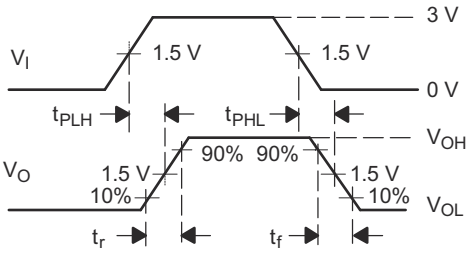


Figure 7-6. Receiver Switching Test Circuit and Voltage Waveforms

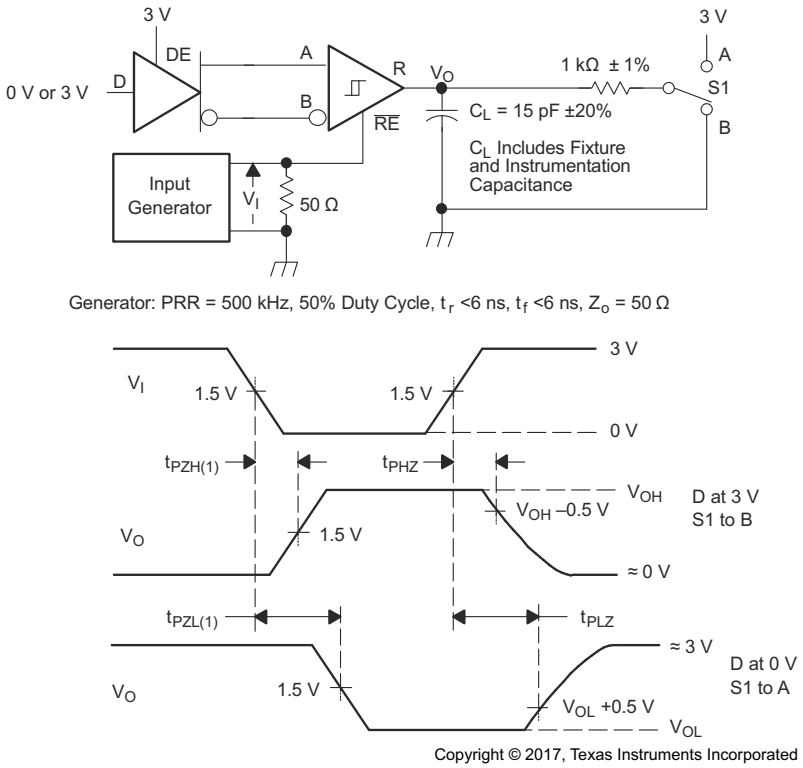


Figure 7-7. Receiver Enable and Disable Time Test Circuit and Voltage Waveforms With Drivers Enabled

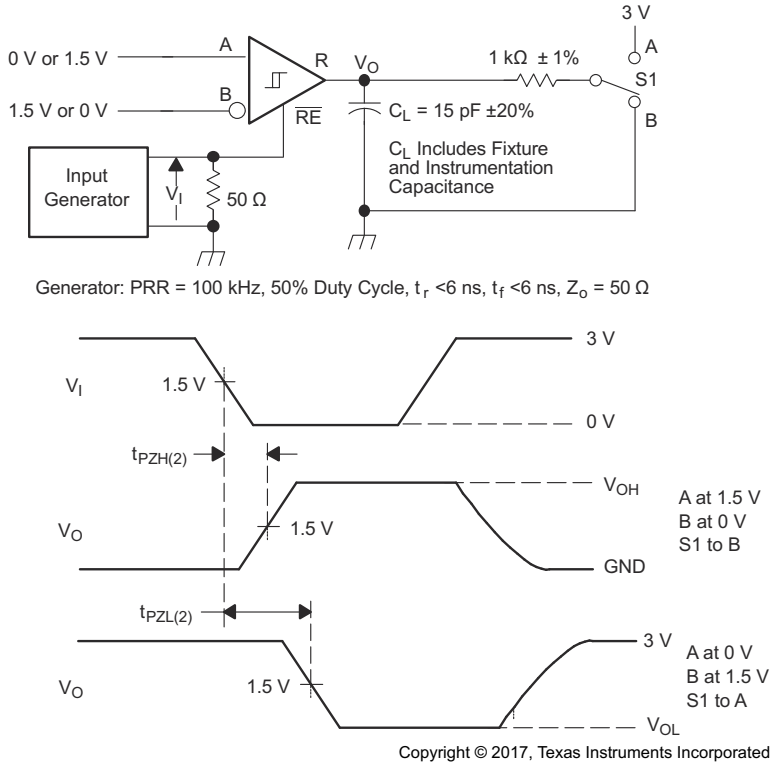


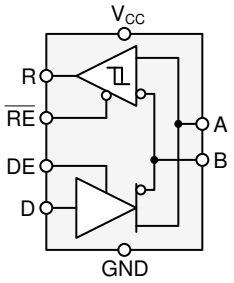
Figure 7-8. Receiver Enable Time From Standby (Driver Disabled)

8 Detailed Description

8.1 Overview

The THVD1330 is a low-power, half-duplex RS-485 transceiver suitable for data transmission up to 32 Mbps. This device has active-high driver enable and active-low receiver enable. Disabling both driver and receiver can achieve a standby current of less than 5 µA.

8.2 Functional Block Diagrams



8.3 Feature Description

Internal ESD protection circuits protect the transceiver against Electrostatic Discharges (ESD) according to IEC 61000-4-2 of up to ±8 kV (Contact Discharge).

The THVD1330 provides internal biasing of the receiver input thresholds in combination with large input-threshold hysteresis. With a input hysteresis (typical) of V_{HYS} = 50 mV, the receiver output remains logic high under a bus-idle or bus-short conditions without the need for external failsafe biasing resistors. Device operation is specified over a wide temperature range from –40°C to 125°C.

8.4 Device Functional Modes

When the driver enable pin, DE, is logic high, the differential outputs A and B follow the logic states at data input D. A logic high at D causes A to turn high and B to turn low. In this case, the differential output voltage defined as $V_{OD} = V_A – V_B$ is positive. When D is low, the output states reverse, B turns high, A becomes low, and V_{OD} is negative.

When DE is low, both outputs turn high-impedance. In this condition the logic state at D is irrelevant. The DE pin has an internal pull-down resistor to ground, thus when left open the driver is disabled (high-impedance) by default. The D pin has an internal pull-up resistor to V_{CC}, thus, when left open while the driver is enabled, output A turns high and B turns low.

Table 8-1. Driver Function Table

INPUT	ENABLE	OUTPUTS		FUNCTION
D	DE	A	B	
H	H	H	L	Actively drive bus high
L	H	L	H	Actively drive bus low
X	L	Z	Z	Driver disabled
X	OPEN	Z	Z	Driver disabled by default
OPEN	H	H	L	Actively drive bus high by default

When the receiver enable pin, $\overline{RE}$, is logic low, the receiver is enabled. When the differential input voltage defined as $V_{ID} = V_A – V_B$ is positive and higher than the positive input threshold, V_{IT+}, the receiver output, R, turns high. When V_{ID} is negative and lower than the negative input threshold, V_{IT-}, the receiver output, R, turns low. If V_{ID} is between V_{IT+} and V_{IT-} the output is indeterminate.

When $\overline{RE}$ is logic high or left open, the receiver output is high-impedance and the magnitude and polarity of V_{ID} are irrelevant. Internal biasing of the receiver inputs causes the output to go failsafe-high when the transceiver is

disconnected from the bus (open-circuit), the bus lines are shorted (short-circuit), or the bus is not actively driven (idle bus).

Table 8-2. Receiver Function Table

DIFFERENTIAL INPUT	ENABLE	OUTPUT	FUNCTION
$V_{ID} = V_A - V_B$	$\overline{RE}$	R	
$V_{IT+} < V_{ID}$	L	H	Receive valid bus high
$V_{IT-} < V_{ID} < V_{IT+}$	L	?	Indeterminate bus state
$V_{ID} < V_{IT-}$	L	L	Receive valid bus low
X	H	Z	Receiver disabled
X	OPEN	Z	Receiver disabled by default
Open-circuit bus	L	H	Fail-safe high output
Short-circuit bus	L	H	Fail-safe high output
Idle (terminated) bus	L	H	Fail-safe high output

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The THVD1330 is a half-duplex RS-485 transceiver commonly used for asynchronous data transmissions. The driver and receiver enable pins allow for the configuration of different operating modes.

- Using independent enable lines provides the most flexible control as it allows for the driver and the receiver to be turned on and off individually. While this configuration requires two control lines, it allows for selective listening into the bus traffic, whether the driver is transmitting data or not.
- Combining the enable signals simplifies the interface to the controller by forming a single direction-control signal. In this configuration, the transceiver operates as a driver when the direction-control line is high, and as a receiver when the direction-control line is low.
- Only one line is required when connecting the receiver-enable input to ground and controlling only the driver-enable input. In this configuration, a node not only receives the data from the bus, but also the data it sends and can verify that the correct data have been transmitted.

9.2 Typical Application

An RS-485 bus consists of multiple transceivers connecting in parallel to a bus cable. To eliminate line reflections, each cable end is terminated with a termination resistor, R_T, whose value matches the characteristic impedance, Z_0, of the cable. This method, known as parallel termination, allows for higher data rates over longer cable length.

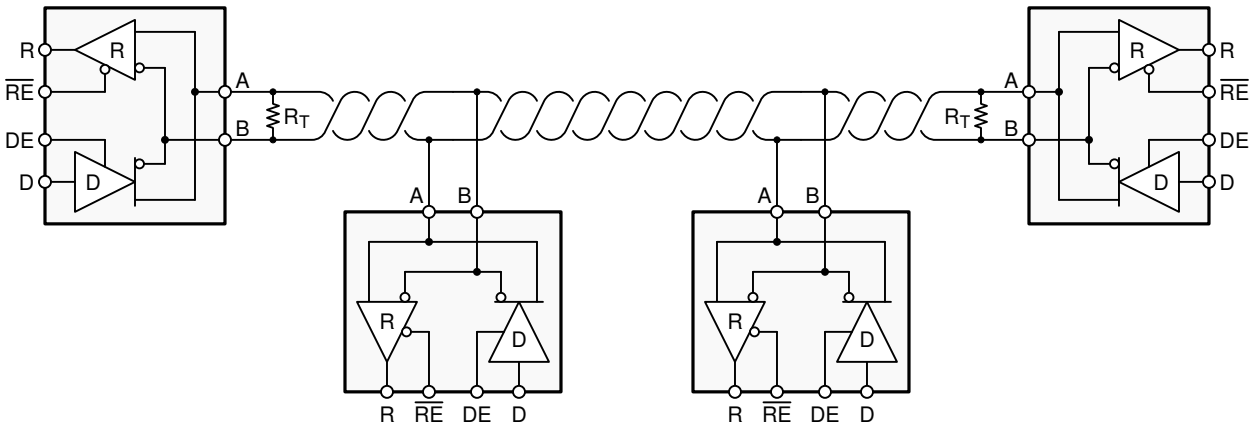


Figure 9-1. Typical RS-485 Network With Half-Duplex Transceivers

9.2.1 Design Requirements

RS-485 is a robust electrical standard suitable for long-distance networking that is used in a wide range of applications with varying requirements, such as distance, data rate, and number of nodes.

9.2.1.1 Data Rate and Bus Length

There is an inverse relationship between data rate and cable length, which means the higher the data rate, the shorter the cable length; and conversely, the lower the data rate, the longer the cable length. While most RS-485 systems use data rates between 10 kbps and 100 kbps, some applications require data rates up to 300 kbps at distances of 4000 feet and longer. Longer distances are possible by allowing for small signal jitter of up to 5 or 10%.

9.2.1.2 Stub Length

When connecting a node to the bus, the distance between the transceiver inputs and the cable trunk, known as the stub, must be as short as possible. Stubs present a non-terminated piece of bus line which can introduce reflections as the length of the stub increases. As a general guideline, the electrical length, or round-trip delay, of a stub is less than one-tenth of the rise time of the driver, thus giving a maximum physical stub length as shown in Equation 1.

$$L_{(STUB)} \leq 0.1 \times t_r \times v \times c \quad (1)$$

where

- t_r is the 10/90 rise time of the driver
- c is the speed of light (3×10^8 m/s)
- v is the signal velocity of the cable or trace as a factor of c

9.2.1.3 Bus Loading

The RS-485 standard specifies that a compliant driver must be able to driver 32 unit loads (UL), where 1 unit load represents a load impedance of approximately 12 kΩ. Connecting up to 64 receivers to the bus is possible because the THVD1330 consists of 1/2 UL transceivers.

9.2.1.4 Receiver Failsafe

The differential receivers of the THVD1330 are *failsafe* to invalid bus states caused by the following:

- Open bus conditions, such as a disconnected connector
- Shorted bus conditions, such as cable damage shorting the twisted-pair together
- Idle bus conditions that occur when no driver on the bus is actively driving

In any of these cases, the differential receiver output a failsafe logic high state so that the output of the receiver is not indeterminate.

Receiver failsafe is accomplished by offsetting the receiver thresholds such that the *input indeterminate* range does not include zero volts differential. To comply with the RS-422 and RS-485 standards, the receiver output must output a high when the differential input V_{ID} is more positive than 200 mV, and must output a low when V_{ID} is less than –200 mV. The receiver parameters which determine the failsafe performance are V_{IT+}, $V_{IT–}$, and V_{HYS} (the separation between V_{IT+} and $V_{IT–}$). As shown in the Table 7-2, differential signals less than –200 mV always cause a low receiver output. Differential signals greater than 200 mV always cause a high receiver output.

When the differential input signal is close to zero, it is still above the V_{IT+} threshold, and the receiver output is high. Only when the differential input is more than V_{HYS} below V_{IT+} does the receiver output transition to a low state. Therefore, the noise immunity of the receiver inputs during a bus fault conditions includes the receiver hysteresis value, V_{HYS}, as well as the value of V_{IT+}.

9.2.1.5 Transient Protection

The bus pins of the THVD1330 transceiver family include on-chip ESD protection against ±16-kV HBM and ±8-kV IEC 61000-4-2 contact discharge. The International Electrotechnical Commission (IEC) ESD test is far more severe than the HBM ESD test. The 50% higher charge capacitance, $C_{(S)}$, and 78% lower discharge resistance, $R_{(D)}$, of the IEC model produce significantly higher discharge currents than the HBM model.

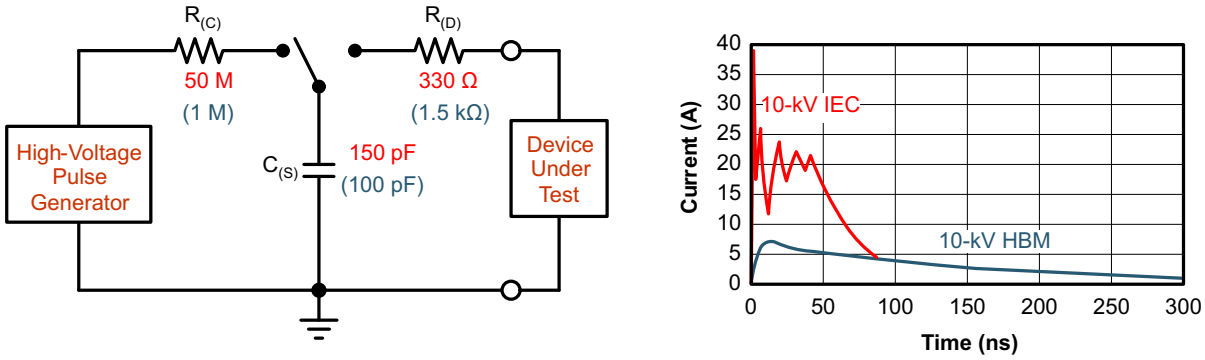


Figure 9-2. HBM and IEC ESD Models and Currents in Comparison (HBM Values in Parenthesis)

The on-chip implementation of IEC ESD protection significantly increases the robustness of equipment. Common discharge events occur because of human contact with connectors and cables. Designers can choose to implement protection against longer duration transients, typically referred to as surge transients.

9.2.2 Detailed Design Procedure

To protect bus nodes against high-energy transients, the implementation of external transient protection devices is necessary. Figure 9-3 suggest a protection circuit against 1 kV surge (IEC 61000-4-5) transients. Table 9-1 shows the associated Bill of Materials.

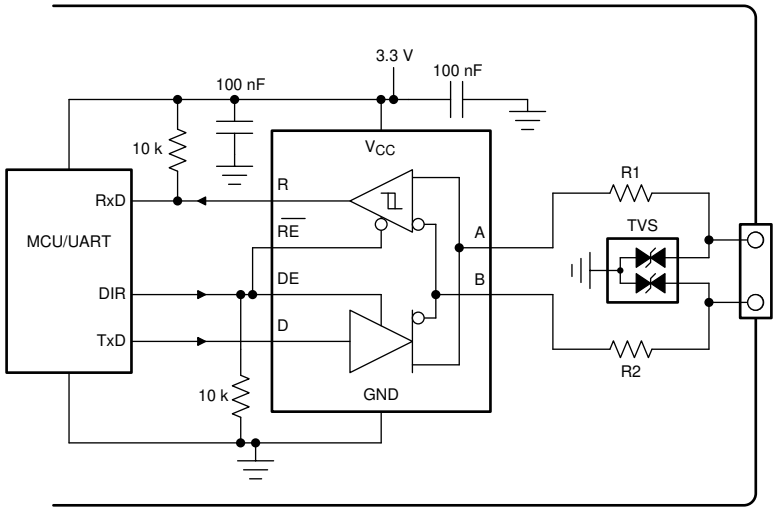


Figure 9-3. Transient Protection Against ESD, EFT, and Surge Transients for Half-Duplex Devices

Table 9-1. Bill of Materials

DEVICE	FUNCTION	ORDER NUMBER	MANUFACTURER(1)
XCVR	RS-485 transceiver	THVD1330	TI
R1	10-Ω, pulse-proof thick-film resistor	CRCW0603010RJNEAHP	Vishay
R2			
TVS	Bidirectional 400-W transient suppressor	CDSOT23-SM712	Bourns

(1) See the Third-Party Products Disclaimer.

9.2.3 Application Curves

Figure 9-4 shows typical supply current consumption of the device at 54 Ω load and 50 pF load capacitor with driver enabled and data is toggled at varying data rates.

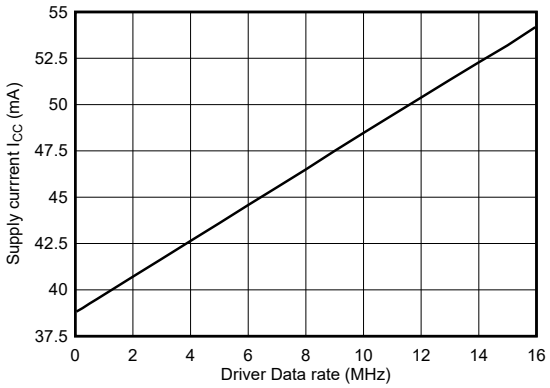


Figure 9-4. Supply Current vs Signal Rate

9.3 Power Supply Recommendations

For reliable operation at all data rates and supply voltages, each supply is decoupled with a 100 nF ceramic capacitor located as close as possible to the supply pins. This helps reduce supply voltage ripple present on the outputs of switched-mode power supplies. This also helps to compensate for the resistance and inductance of the PCB power planes.

9.4 Layout

9.4.1 Layout Guidelines

Robust and reliable bus node design often requires the use of external transient protection devices to protect against surge transients that occurs in industrial environments. Since these transients have a wide frequency bandwidth (from approximately 3 MHz to 300 MHz), high-frequency layout techniques are applied during PCB design.

1. Place the protection circuitry close to the bus connector to prevent noise transients from propagating across the board.
2. Use V_{CC} and ground planes to provide low inductance. Note that high-frequency currents tend to follow the path of least impedance and not the path of least resistance.
3. Design the protection components into the direction of the signal path. Do not force the transient currents to divert from the signal path to reach the protection device.
4. Apply 100-nF to 220-nF bypass capacitors as close as possible to the V_{CC} pins of transceiver, UART and controller ICs on the board.
5. Use at least two vias for V_{CC} and ground connections of bypass capacitors and protection devices to minimize effective via inductance.
6. Use 1-kΩ to 10-kΩ pullup and pulldown resistors for enable lines to limit noise currents in theses lines during transient events.
7. Insert pulse-proof resistors into the A and B bus lines if the TVS clamping voltage is higher than the specified maximum voltage of the transceiver bus pins. These resistors limit the residual clamping current into the transceiver and prevent it from latching up.
8. While pure TVS protection is sufficient for surge transients up to 1 kV, higher transients require metal-oxide varistors (MOVs) which reduce the transients to a few hundred volts of clamping voltage, and transient blocking units (TBUs) that limit transient current to less than 1 mA.

9.4.2 Layout Example

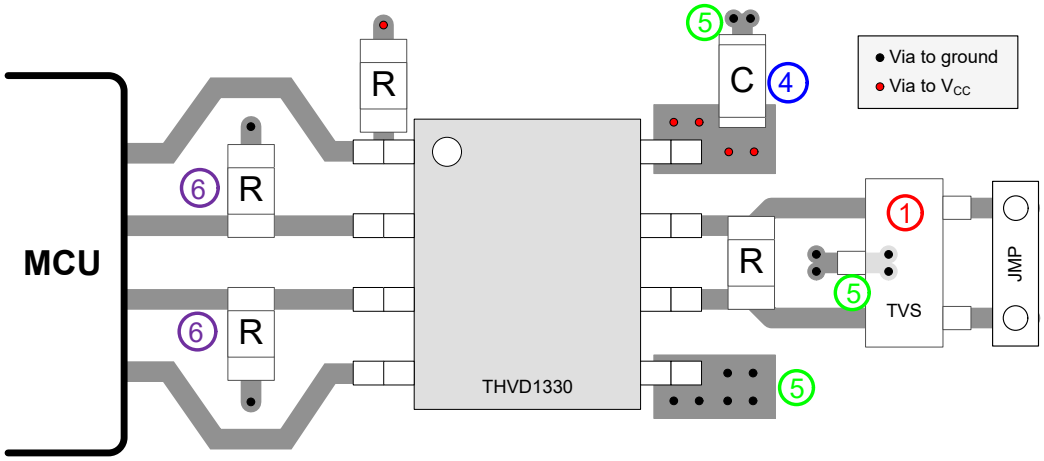


Figure 9-5. Layout Example

10 Device and Documentation Support

10.1 Third-Party Products Disclaimer

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10.2 Device Support

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10.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
THVD1330DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T1330
THVD1330DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T1330

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

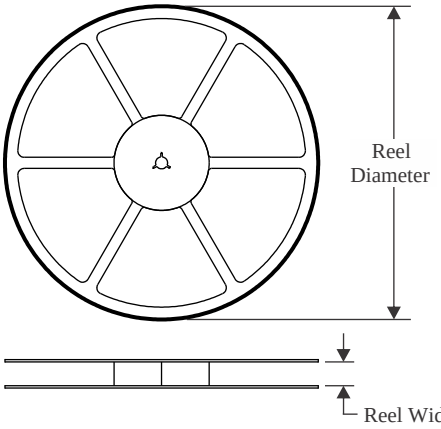
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

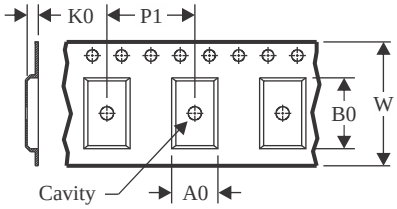
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

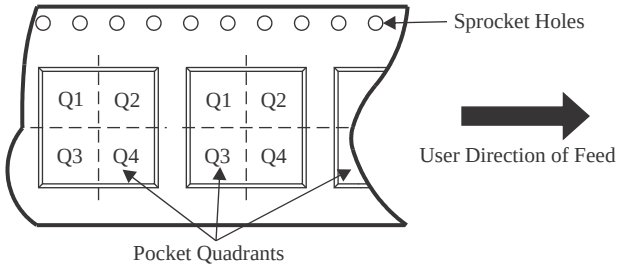


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

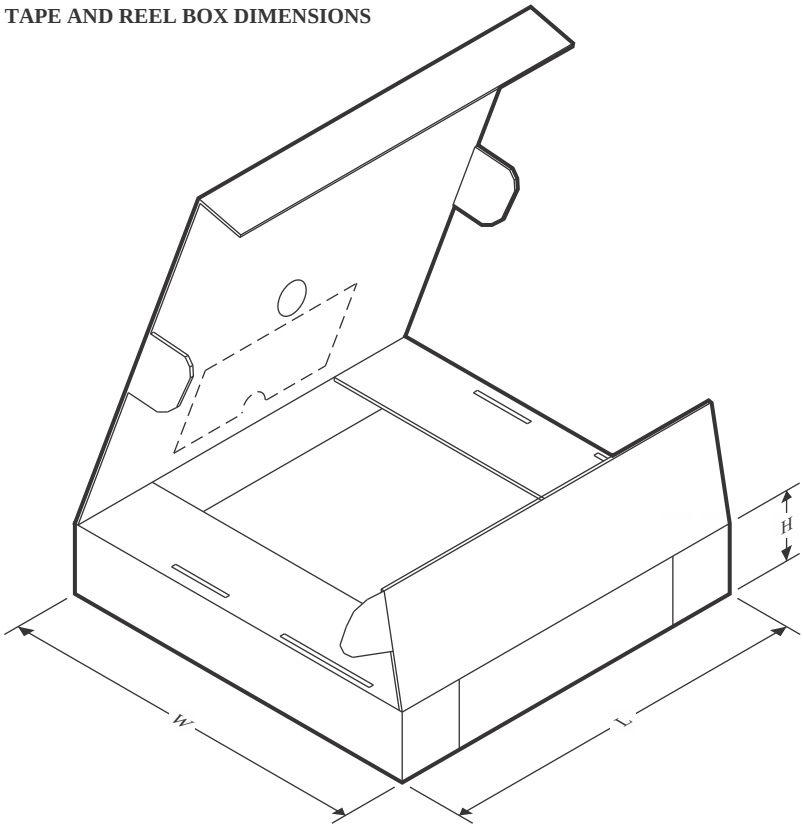
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

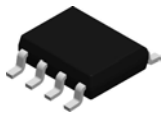
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THVD1330DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THVD1330DR	SOIC	D	8	2500	353.0	353.0	32.0

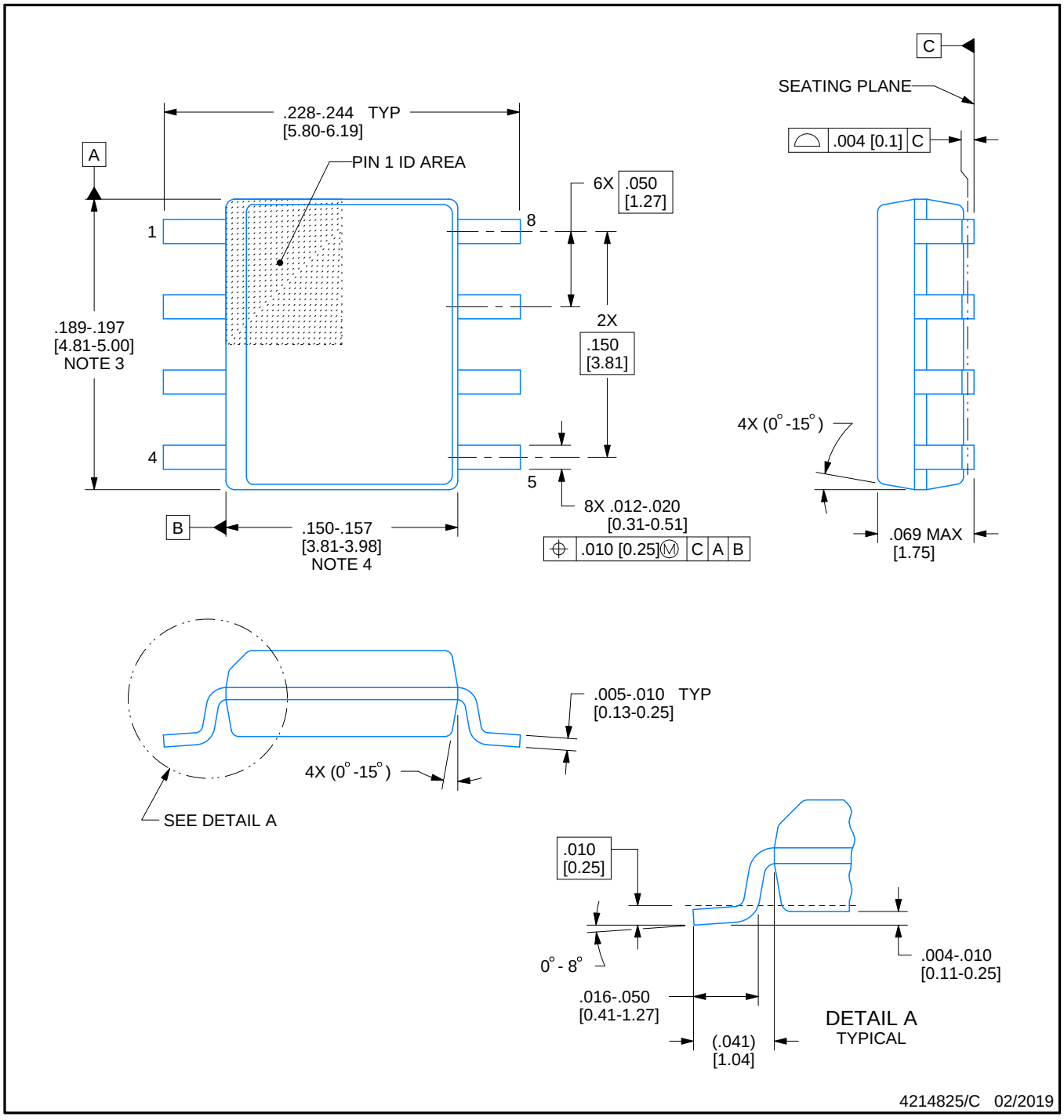


PACKAGE OUTLINE

D0008A

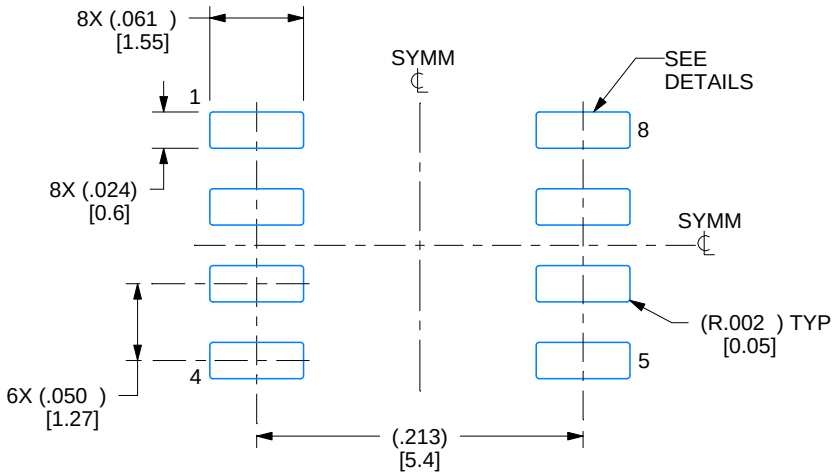
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

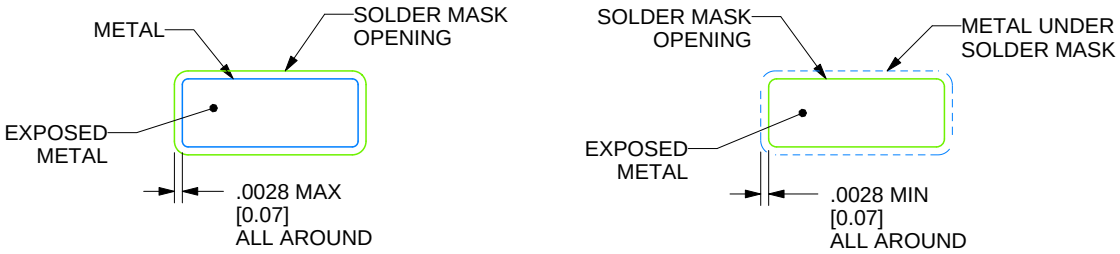


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

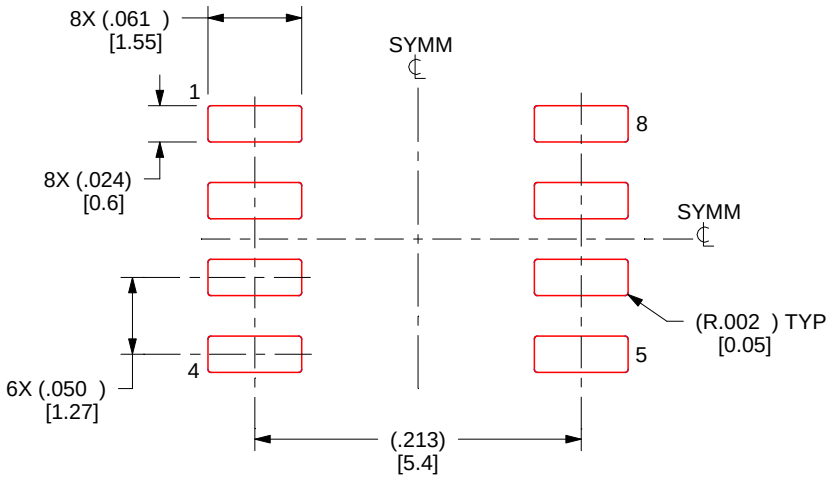
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025