TDA2Ex SoC for Advanced Driver Assistance Systems (ADAS) 23mm Package (ABC Package) Silicon Revision 2.0 and 2.1

1 Device Overview

1.1 Features

- Architecture designed for ADAS applications
- Video, image, and graphics processing support
  - Full-HD video (1920 × 1080p, 60 fps)
  - Multiple video inputs and video outputs
- Arm® Cortex®-A15 microprocessor subsystem
- C66x floating-point VLIW DSP cores
  - Fully object-code compatible with C67x and C64x+
  - Up to thirty-two 16 × 16-bit fixed-point multiplies per cycle
- Up to 512KB of on-chip L3 RAM
- Level 3 (L3) and level 4 (L4) interconnects
- DDR3/DDR3L External Memory Interface (EMIF) module
  - Supports up to DDR3-1333 (667 MHz)
  - Up to 2GB across single chip select
- Dual Arm® Cortex®-M4 Image Processing Units (IPU)
- IVA-HD subsystem
- Display subsystem
  - Display controller with DMA engine and up to three pipelines
  - HDMI™ encoder: HDMI 1.4a and DVI 1.0 compliant
- Single-core PowerVR® SGX544 3D GPU
- 2D-graphics accelerator (BB2D) subsystem
  - Vivante® GC320 core
- Video Processing Engine (VPE)
- One Video Input Port (VIP) module
  - Support for up to four multiplexed input ports
- General-Purpose Memory Controller (GPMC)
- Enhanced Direct Memory Access (EDMA) controller
- 2-Port Gigabit Ethernet switch
  - Up to two external ports, one internal
- Sixteen 32-bit general-purpose timers
- 32-bit MPU watchdog timer
- Six high speed Inter-Integrated Circuit (I^2C™) ports
- Ten configurable UART/IrDA/CIR modules
- Four Multichannel Serial Peripheral Interfaces (McSPI)
- Quad Serial Peripheral Interface (QSPI™)
- SATA interface
- Eight Multichannel Audio Serial Port (McASP) modules
- SuperSpeed USB 3.0 dual-role device
- High Speed USB 2.0 dual-role device
- High Speed USB 2.0 on-the-go
- Four MultiMedia Card/ Secure Digital®/Secure Digital Input Output interfaces (MMC™/ SD®/SDIO)
- PCI-Express® (PCIe®) revision 3.0 Port with integrated PHY
  - One 2-lane gen2-compliant port
  - or Two 1-lane gen2-compliant ports
- Dual Controller Area Network (DCAN) modules
  - CAN 2.0B protocol
- MIPI® Camera Serial Interface 2 (CSI-2)
- Up to 215 General-Purpose I/O (GPIO) pins
- Real-Time Clock subsystem (RTCSS)
- Device Security Features
  - Hardware crypto accelerators and DMA
  - Firewalls
  - JTAG lock
  - Secure keys
  - Secure ROM and boot
  - Customer programmable keys (Silicon Revision 2.1)
- Power, reset, and clock management
- On-chip debug with CTools technology
- 28-nm CMOS technology
- 23 mm × 23 mm, 0.8-mm Pitch, 760-Pin BGA (ABC)

1.2 Applications

- Mono, Stereo or Tri-Optic Front Camera
  - Object detection
  - Pedestrian detection
  - Traffic sign recognition
  - Lane detection and departure warning
  - Automatic emergency braking
  - Adaptive cruise control
  - Forward collision warning
  - High beam assist
- LVDS or ethernet surround view
  - 2D surround view
  - 3D surround view
  - Rear object detection
  - Parking assist
  - Pedestrian detection
  - Lane tracking
  - Drive recording
- Sensor fusion – vision, radar, ultrasonic, lidar sensors
  - Object data fusion
  - Raw data fusion

1.3 Description

TI's new TDA2Ex System-on-Chip (SoC) is a highly optimized and scalable family of devices designed to meet the requirements of leading Advanced Driver Assistance Systems (ADAS). The TDA2Ex family enables broad ADAS applications in today's automobile by integrating an optimal mix of performance, low power, and ADAS vision analytics processing that aims to facilitate a more autonomous and collision-free driving experience.

The TDA2Ex SoC enables sophisticated embedded vision technology in today's automobile by enabling a board range of ADAS applications including park assist, surround view and sensor fusion on a single architecture.

The TDA2Ex SoC incorporates a heterogeneous, scalable architecture that includes a mix of TI's fixed and floating-point TMS320C66x digital signal processor (DSP) generation core, Arm® Cortex®-A15 MPCore™ and dual- Arm® Cortex®-M4 processors. The integration of a video accelerator for decoding multiple video streams over an Ethernet AVB network, along with graphics accelerator for rendering virtual views, enable a 3D viewing experience. The TDA2Ex SoC also integrates a host of peripherals including multicamera interfaces (both parallel and serial, including CSI-2) to enable Ethernet or LVDS-based surround view systems, displays and GigB Ethernet AVB.

Additionally, TI provides a complete set of development tools for the Arm® and DSP, including C compilers, a DSP assembly optimizer to simplify programming and scheduling, and a debugging interface for visibility into source code execution.

Cryptographic acceleration is available in all devices. All other supported security features, including support for secure boot, debug security and support for trusted execution environment is available on High-Security (HS) devices. For more information about HS devices, contact your TI representative.

The TDA2Ex ADAS processor is qualified according to the AEC-Q100 standard.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE
TDA2EGABC	FCBGA (760)	23.0 mm × 23.0 mm

(1) For more information, see Section 10, *Mechanical, Packaging, and Orderable Information*.

1.4 Functional Block Diagram

Figure 1-1 is functional block diagram for the device.

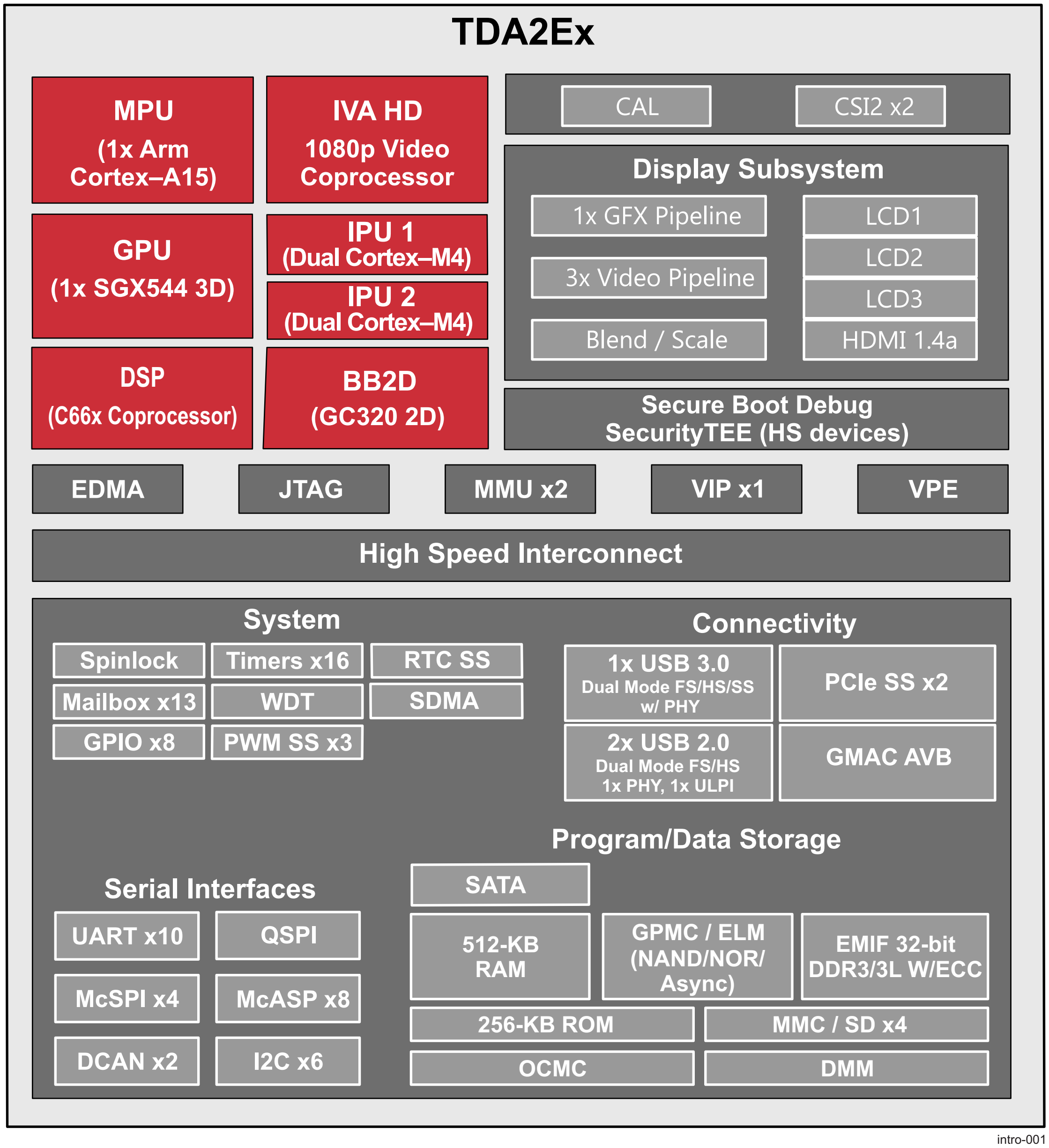

Figure 1-1. TDA2Ex Block Diagram

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2 Revision History

3 Device Comparison

Table 3-1 shows a comparison between devices, highlighting the differences.

Table 3-1. Device Comparison[(2)]

FEATURES			DEVICE
			TDA2EG
Features			
CTRL_WKUP_STD_FUSE_DIE_ID_2[31:24] Base PN register bit field value[(1)(2)]			TDA2EGx: 20 (0x14)
Processors/Accelerators			
Speed Grades			H, D
Arm Single Cortex-A15 Microprocessor (MPU) Subsystem		MPU core 0	Yes
C66x VLIW DSP		DSP1	Yes
BitBLT 2D Hardware Acceleration Engine (BB2D)		BB2D	Yes
Display Subsystem		VOUT1	Yes
		VOUT2	Yes
		VOUT3	Yes
		HDMI	Yes
Dual Arm Cortex-M4 Image Processing Unit (IPU)		IPU1	Yes
		IPU2	Yes
Image Video Accelarator (IVA)		IVA	Yes
SGX544 Single-Core 3D Graphics Processing Unit (GPU)		GPU	Yes
Video Input Port (VIP)	VIP1	vin1a	Yes
		vin1b	Yes
		vin2a	Yes
		vin2b	Yes
Video Processing Engine (VPE)		VPE	Yes
Program/Data Storage			
On-Chip Shared Memory (RAM)		OCMC_RAM1	512KB
General-Purpose Memory Controller (GPMC)		GPMC	Yes
DDR3 Memory Controller		EMIF1	up to 2GB across single chip select
		SECDED/ECC	Yes
Dynamic Memory Manager (DMM)		DMM	Yes
Peripherals			
Dual Controller Area Network (DCAN) Interface		DCAN1	Yes
		DCAN2	Yes
Enhanced DMA (EDMA)		EDMA	Yes
System DMA (DMA_SYSTEM)		DMA_SYSTEM	Yes
Ethernet Subsystem (Ethernet SS)		GMAC_SW[0]	MII, RMII, or RGMII
		GMAC_SW[1]	MII, RMII, or RGMII
General-Purpose I/O (GPIO)		GPIO	up to 215
Inter-Integrated Circuit (I2C) Interface		I2C	6
System Mailbox Module		MAILBOX	13
Camera Adaptation Layer (CAL) Camera Serial Interface 2 (CSI2)		CSI2_0	1 CLK + 4 Data Line
		CSI2_1	1 CLK + 2 Data Line

Table 3-1. Device Comparison(2) (continued)

FEATURES		DEVICE TDA2EG
Multichannel Audio Serial Port (McASP)	McASP1	16 serializers
	McASP2	16 serializers
	McASP3	4 serializers
	McASP4	4 serializers
	McASP5	4 serializers
	McASP6	4 serializers
	McASP7	4 serializers
	McASP8	4 serializers
MultiMedia Card/Secure Digital/Secure Digital Input Output Interface (MMC/SD/SDIO)	MMC1	1x UHSI 4b
	MMC2	1x eMMC™ 8b
	MMC3	1x SDIO 8b
	MMC4	1x SDIO 4b
PCI-Express 3.0 Port with Integrated PHY	PCIe_SS1	Yes
	PCIe_SS2	Yes
Serial Advanced Technology Attachment (SATA)	SATA	Yes
Real-Time Clock Subsystem (RTCSS)	RTCSS	Yes
Multichannel Serial Peripheral Interface (McSPI)	McSPI	4
Quad SPI (QSPI)	QSPI	Yes
Spinlock Module	SPINLOCK	Yes
Timers, General-Purpose	TIMERS GP	16
Timer, Watchdog	WD TIMER	Yes
Pulse-Width Modulation Subsystem (PWMSS)	PWMSS1	Yes
	PWMSS2	Yes
	PWMSS3	Yes
Universal Asynchronous Receiver/Transmitter (UART)	UART	10
Universal Serial Bus (USB3.0)	USB1 (SuperSpeed, Dual-Role-Device [DRD])	Yes
Universal Serial Bus (USB2.0)	USB2 (High Speed, Dual-Role-Device [DRD], with embedded HS PHY)	Yes
	USB3 (High Speed, OTG2.0, with ULPI)	Yes
	USB4 (High Speed, OTG2.0, with ULPI)	No

(1) For more details about the CTRL_WKUP_STD_FUSE_DIE_ID_2 register and Base PN bit field, see the *TDA2Ex Technical Reference Manual*.

(2) XDRA726 base part number with X speed grade indicator is the part number for the superset device. Software should constrain the features and speed used to match the intended production device. The Base PN register bit field value is 0x4.

3.1 Related Products

Automotive Processors

TDAx ADAS SoCs TI's TDAx Driver Assistance System-on-Chip (SoC) family offers scalable and open solutions and a common hardware and software architecture for Advanced Driver Assistance Systems (ADAS) applications including camera-based front (mono and stereo), rear, surround view and night vision systems, and mid- and long-range radar and sensor fusion systems.

Companion Products for TDAx Review products that are frequently purchased or used in conjunction with this product.

4 Terminal Configuration and Functions

4.1 Terminal Assignment

Figure 4-1 shows the ball locations for the 760 plastic ball grid array (PBGA) package and is used in conjunction with Table 4-2 through Table 4-31 to locate signal names and ball grid numbers.

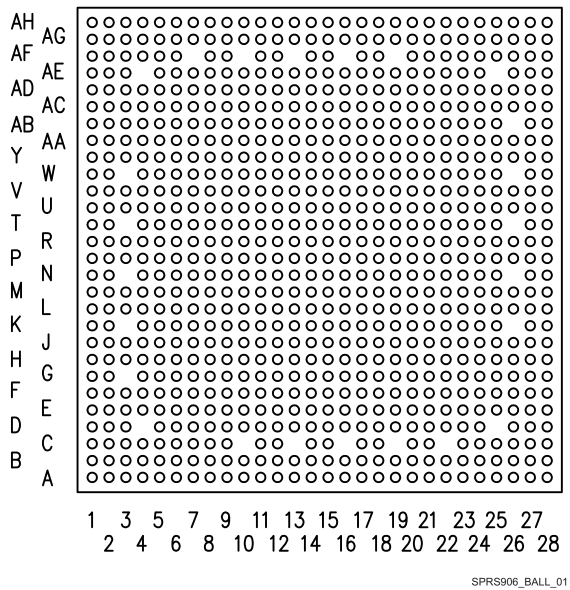

Figure 4-1. ABC S-PBGA-N760 Package (Bottom View)

NOTE

The following bottom balls are not pinned out: AF7, AF10, AF13, AF16, AF19, AE4, AE25, AB26, W3, W26, T3, T26, N3, N26, K3, K26, G3, D4, D25, C10, C13, C16, C19, C22.

These balls do not exist on the package.

NOTE

The following bottom balls are not connected: AH11, AH12, AG2, AG8, AG11, AG12, AF4, AF6, AF8, AF9, AE3, AE5, AE6, AE8, AE9, AD3, AD8, AD9, Y15, Y16, V18, V19, U18, U19, U22, U23, U24, U25, U26, U27, U28, T22, T23, T27, T28, R20, R22, R23, R24, R25, R26, R27, R28, P19, P22, P23, P24, P25, P26, P27, N20, N22, N23, N27, N28, M20, M21, M22, M23, M24, M25, M26, M27, M28, L20, L21, L22, L23, L24, L25, L26, L27, L28, K20, K21, K22, K23, K27, K28, J20, J21, J22, J23, J24, J25, J26, J27, H20, H21, H22, H23, H24, H25, H26, H27, H28, G22, G23, G24, G25, G26, G27, G28, F24, F25, F26, F27, F28, E24, E26, E27, E28

These balls can be connected as desired, including to VSS. For users designing TDA2x compatible PCB, please refer to TDA2x Data Manual for appropriate requirements.

4.1.1 Unused Balls Connection Requirements

This section describes the connection requirements of the unused and reserved balls.

NOTE

The following balls are reserved: A27, Y5, Y10, B28, AC1, AC2, AA1, AA2, AB1, AB2, AD14.

These balls must be left unconnected.

NOTE

All unused power supply balls must be supplied with the voltages specified in the Section 5.4, *Recommended Operating Conditions,* unless alternative tie-off options are included in Section 4.4, *Signal Descriptions*.

Table 4-1. Unused Balls Specific Connection Requirements

BALLS	CONNECTION REQUIREMENTS
AE15, AC15, AE14, D20, AD17, AC16, V27, AH25, AE27, AD27, Y28	These balls must be connected to GND through an external pull resistor if unused.
E20, D21, E23, C20, C21, V28, F18, AG25, AE28, AD28, Y27, F17, C25	These balls must be connected to the corresponding power supply through an external pull resistor if unused.
K14 (vpp)	This ball must be left unconnected if unused
AF14 (rtc_iso)	This ball should be connected to the corresponding power supply through an external pull resistor if unused; or can be connected to F22 (porz) when RTC unused (level translation may be needed)
AB17 (rtc_porz)	This ball should be connected to VSS when RTC is unused; or can be connected to F22 (porz) when RTC unused (level translation may be needed)

NOTE

All other unused signal balls **with** a Pad Configuration register can be left unconnected with their internal pullup or pulldown resistor enabled.

NOTE

All other unused signal balls **without** a Pad Configuration register can be left unconnected.

4.2 Ball Characteristics

Table 4-2 describes the terminal characteristics and the signals multiplexed on each ball. The following list describes the table column headers:

1. **BALL NUMBER:**This column lists ball numbers on the bottom side associated with each signal on the bottom.
2. **BALL NAME:** This column lists mechanical name from package device (name is taken from muxmode 0).
3. **SIGNAL NAME:**This column lists names of signals multiplexed on each ball (also notice that the name of the ball is the signal name in muxmode 0).

NOTE

Table 4-2 does not take into account the subsystem multiplexing signals. Subsystem multiplexing signals are described in Section 4.4, *Signal Descriptions*.

NOTE

In driver off mode, the buffer is configured in high-impedance.

NOTE

In some cases Table 4-2 may present more than one signal name per muxmode for the same ball. First signal in the list is the dominant function as selected via CTRL_CORE_PAD_* register.

All other signals are virtual functions that present alternate multiplexing options. This virtual functions are controlled via CTRL_CORE_ALT_SELECT_MUX or CTRL_CORE_VIP_MUX_SELECT register. For more information on how to use these options, see *Pad Configuration Registers* section, *Control Module* chapter in the device TRM.

4. **MUXMODE:** Multiplexing mode number:
   a. MUXMODE 0 is the primary mode; this means that when MUXMODE=0 is set, the function mapped on the pin corresponds to the name of the pin. The primary muxmode is not necessarily the default muxmode.

   NOTE

   The default mode is the mode at the release of the reset; also see the RESET REL. MUXMODE column.

   b. MUXMODE 1 through 15 are possible muxmodes for alternate functions. On each pin, some muxmodes are effectively used for alternate functions, while some muxmodes are not used. Only MUXMODE values which correspond to defined functions should be used.
   c. An empty box means Not Applicable.
5. **TYPE:** Signal type and direction:
   – I = Input
   – O = Output
   – IO = Input or Output
   – D = Open drain
   – DS = Differential Signaling
   – A = Analog
   – PWR = Power
   – GND = Ground
   – CAP = LDO Capacitor

NOTE

The RX buffer within the pad logic should be disabled on all pins that are not being used as an input. For more information, see the *Control Module / Control Module Functional Description / PAD Functional Multiplexing and Configuration* section in the device TRM.

6. **BALL RESET STATE:** The state of the terminal at power-on reset:
   – drive 0 (OFF): The buffer drives V_{OL} (pulldown or pullup resistor not activated)
   – drive 1 (OFF): The buffer drives V_{OH} (pulldown or pullup resistor not activated)
   – OFF: High-impedance
   – PD: High-impedance with an active pulldown resistor
   – PU: High-impedance with an active pullup resistor
   – An empty box means Not Applicable

NOTE

Designs that contain pullup or pulldown resistors, either on the board or in attached devices that oppose internal pullup or pulldown resistors, that are active while the device is held in reset, must not remain in reset for long periods of time.

7. **BALL RESET REL. STATE:** The state of the terminal at the deactivation of the rstoutn signal (also

mapped to the PRCM SYS_WARM_OUT_RST signal)

- drive 0 (OFF): The buffer drives V_{OL} (pulldown or pullup resistor not activated)
- drive clk (OFF): The buffer drives a toggling clock (pulldown or pullup resistor not activated)
- drive 1 (OFF): The buffer drives V_{OH} (pulldown or pullup resistor not activated)
- OFF: High-impedance
- PD: High-impedance with an active pulldown resistor
- PU: High-impedance with an active pullup resistor
- An empty box means Not Applicable

NOTE

For more information on the CORE_PWRON_RET_RST reset signal and its reset sources, see *Power, Reset, and Clock Management* chapter in the device TRM.

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8. **BALL RESET REL. MUXMODE:** This muxmode is automatically configured at the release of the rstoutn signal (also mapped to the PRCM SYS_WARM_OUT_RST signal).
   An empty box means Not Applicable.
9. **IO VOLTAGE VALUE**: This column describes the IO voltage value (VDDS supply).
   An empty box means Not Applicable.
10. **POWER:** The voltage supply that powers the terminal IO buffers.
    An empty box means Not Applicable.
11. **HYS:** Indicates if the input buffer is with hysteresis:
    - Yes: With hysteresis
    - No: Without hysteresis
    - An empty box: Not Applicable

NOTE

For more information, see the hysteresis values in Section 5.7, *Electrical Characteristics*.

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12. **BUFFER TYPE:** Drive strength of the associated output buffer.
    An empty box means Not Applicable.

NOTE

For programmable buffer strength:

- The default value is given in Table 4-2.
- A note describes all possible values according to the selected muxmode.

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13. **PULLUP / PULLDOWN TYPE:** Denotes the presence of an internal pullup or pulldown resistor. Pullup and pulldown resistors can be enabled or disabled via software.
    - PU: Internal pullup
    - PD: Internal pulldown
    - PU/PD: Internal pullup and pulldown
    - PUx/PDy: Programmable internal pullup and pulldown
    - PDy: Programmable internal pulldown
    - An empty box means No pull

NOTE

Internal pullup or pulldown resistors must be disabled when opposed by an external pullup or pulldown resistor on the board or within an attached device.

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14. **DSIS:** The deselected input state (DSIS) indicates the state driven on the peripheral input (logic "0" or logic "1") when the peripheral pin function is not selected by any of the PINCNTLx registers.
    - 0: Logic 0 driven on the peripheral's input signal port.

– 1: Logic 1 driven on the peripheral's input signal port.
– blank: Pin state driven on the peripheral's input signal port.

NOTE

Configuring two pins to the same input signal is not supported as it can yield unexpected results. This can be easily prevented with the proper software configuration (Hi-Z mode is not an input signal).

NOTE

When a pad is set into a multiplexing mode which is not defined by pin multiplexing, that pad’s behavior is undefined. This should be avoided.

NOTE

Some of the EMIF1 signals have an additional state change at the release of porz. The state that the signals change to at the release of porz is as follows:

drive 0 (OFF) for: ddr1_csn0, ddr1_ck, ddr1_nck, ddr1_casn, ddr1_rasn, ddr1_wen, ddr1_ba[2:0], ddr1_a[15:0].

OFF for: ddr1_ecc_d[7:0], ddr1_dqm[3:0], ddr1_dqm_ecc, ddr1_dqs[3:0], ddr1_dqsn[3:0], ddr1_dqs_ecc, ddr1_dqsn_ecc, ddr1_d[31:0].

NOTE

Dual rank support is not available on this device, but signal names are retained for consistency with the TDA2xx family of devices.

Table 4-2. Ball Characteristics(1)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	BALL RESET REL. MUXMODE [8]	I/O VOLTAGE VALUE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/DOWN TYPE [13]	DSIS [14]
K9	cap_vbbldo_dsp	cap_vbbldo_dsp		CAP									
Y14	cap_vbbldo_gpu	cap_vbbldo_gpu		CAP									
J10	cap_vbbldo_iva	cap_vbbldo_iva		CAP									
J16	cap_vbbldo_mpu	cap_vbbldo_mpu		CAP									
T20	cap_vddram_core1	cap_vddram_core1		CAP									
L9	cap_vddram_core3	cap_vddram_core3		CAP									
J19	cap_vddram_core4	cap_vddram_core4		CAP									
J9	cap_vddram_dsp	cap_vddram_dsp		CAP									
Y13	cap_vddram_gpu	cap_vddram_gpu		CAP									
K16	cap_vddram_iva	cap_vddram_iva		CAP									
K19	cap_vddram_mpu	cap_vddram_mpu		CAP									
AE1	csi2_0_dx0	csi2_0_dx0	0	I				1.8	vdda_csi	Yes	LVCMOS CSI2	PU/PD	
AF1	csi2_0_dx1	csi2_0_dx1	0	I				1.8	vdda_csi	Yes	LVCMOS CSI2	PU/PD	
AF2	csi2_0_dx2	csi2_0_dx2	0	I				1.8	vdda_csi	Yes	LVCMOS CSI2	PU/PD	
AH4	csi2_0_dx3	csi2_0_dx3	0	I				1.8	vdda_csi	Yes	LVCMOS CSI2	PU/PD	
AH3	csi2_0_dx4	csi2_0_dx4	0	I				1.8	vdda_csi	Yes	LVCMOS CSI2	PU/PD	
AD2	csi2_0_dy0	csi2_0_dy0	0	I				1.8	vdda_csi	Yes	LVCMOS CSI2	PU/PD	
AE2	csi2_0_dy1	csi2_0_dy1	0	I				1.8	vdda_csi	Yes	LVCMOS CSI2	PU/PD	
AF3	csi2_0_dy2	csi2_0_dy2	0	I				1.8	vdda_csi	Yes	LVCMOS CSI2	PU/PD	
AG4	csi2_0_dy3	csi2_0_dy3	0	I				1.8	vdda_csi	Yes	LVCMOS CSI2	PU/PD	
AG3	csi2_0_dy4	csi2_0_dy4	0	I				1.8	vdda_csi	Yes	LVCMOS CSI2	PU/PD	
AG5	csi2_1_dx0	csi2_1_dx0	0	I				1.8	vdda_csi	Yes	LVCMOS CSI2	PU/PD	
AG6	csi2_1_dx1	csi2_1_dx1	0	I				1.8	vdda_csi	Yes	LVCMOS CSI2	PU/PD	
AH7	csi2_1_dx2	csi2_1_dx2	0	I				1.8	vdda_csi	Yes	LVCMOS CSI2	PU/PD	
AH5	csi2_1_dy0	csi2_1_dy0	0	I				1.8	vdda_csi	Yes	LVCMOS CSI2	PU/PD	
AH6	csi2_1_dy1	csi2_1_dy1	0	I				1.8	vdda_csi	Yes	LVCMOS CSI2	PU/PD	
AG7	csi2_1_dy2	csi2_1_dy2	0	I				1.8	vdda_csi	Yes	LVCMOS CSI2	PU/PD	

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	BALL RESET REL. MUXMODE [8]	I/O VOLTAGE VALUE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/DOWN TYPE [13]	DSIS [14]
G19	dcan1_rx	dcan1_rx	0	IO	PU	PU	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	1
		uart8_txd	2	O									
		mmc2_sdwp	3	I									0
		sata1_led	4	O									
		hdmi1_cec	6	IO									
		gpio1_15	14	IO									
		Driver off	15	I									
G20	dcan1_tx	dcan1_tx	0	IO	PU	PU	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	1
		uart8_rxd	2	I									1
		mmc2_sdcd	3	I									1
		hdmi1_hpd	6	IO									
		gpio1_14	14	IO									
		Driver off	15	I									
AD20	ddr1_a0	ddr1_a0	0	O	PD	drive 1 (OFF)		1.35/1.5	vdds_ddr1	No	LVCMOS DDR	PUx/PDy	
AC19	ddr1_a1	ddr1_a1	0	O	PD	drive 1 (OFF)		1.35/1.5	vdds_ddr1	No	LVCMOS DDR	PUx/PDy	
AC20	ddr1_a2	ddr1_a2	0	O	PD	drive 1 (OFF)		1.35/1.5	vdds_ddr1	No	LVCMOS DDR	PUx/PDy	
AB19	ddr1_a3	ddr1_a3	0	O	PD	drive 1 (OFF)		1.35/1.5	vdds_ddr1	No	LVCMOS DDR	PUx/PDy	
AF21	ddr1_a4	ddr1_a4	0	O	PD	drive 1 (OFF)		1.35/1.5	vdds_ddr1	No	LVCMOS DDR	PUx/PDy	
AH22	ddr1_a5	ddr1_a5	0	O	PD	drive 1 (OFF)		1.35/1.5	vdds_ddr1	No	LVCMOS DDR	PUx/PDy	
AG23	ddr1_a6	ddr1_a6	0	O	PD	drive 1 (OFF)		1.35/1.5	vdds_ddr1	No	LVCMOS DDR	PUx/PDy	
AE21	ddr1_a7	ddr1_a7	0	O	PD	drive 1 (OFF)		1.35/1.5	vdds_ddr1	No	LVCMOS DDR	PUx/PDy	
AF22	ddr1_a8	ddr1_a8	0	O	PD	drive 1 (OFF)		1.35/1.5	vdds_ddr1	No	LVCMOS DDR	PUx/PDy	
AE22	ddr1_a9	ddr1_a9	0	O	PD	drive 1 (OFF)		1.35/1.5	vdds_ddr1	No	LVCMOS DDR	PUx/PDy	
AD21	ddr1_a10	ddr1_a10	0	O	PD	drive 1 (OFF)		1.35/1.5	vdds_ddr1	No	LVCMOS DDR	PUx/PDy	
AD22	ddr1_a11	ddr1_a11	0	O	PD	drive 1 (OFF)		1.35/1.5	vdds_ddr1	No	LVCMOS DDR	PUx/PDy	
AC21	ddr1_a12	ddr1_a12	0	O	PD	drive 1 (OFF)		1.35/1.5	vdds_ddr1	No	LVCMOS DDR	PUx/PDy	
AF18	ddr1_a13	ddr1_a13	0	O	PD	drive 1 (OFF)		1.35/1.5	vdds_ddr1	No	LVCMOS DDR	PUx/PDy	
AE17	ddr1_a14	ddr1_a14	0	O	PD	drive 1 (OFF)		1.35/1.5	vdds_ddr1	No	LVCMOS DDR	PUx/PDy	

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	BALL RESET REL. MUXMODE [8]	I/O VOLTAGE VALUE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/DOWN TYPE [13]	DSIS [14]
AD18	ddr1_a15	ddr1_a15	0	O	PD	drive 1 (OFF)		1.35/1.5	vdds_ddr1	No	LVCMOS DDR	PUx/PDy	
AF17	ddr1_ba0	ddr1_ba0	0	O	PU	drive 1 (OFF)		1.35/1.5	vdds_ddr1	No	LVCMOS DDR	PUx/PDy	
AE18	ddr1_ba1	ddr1_ba1	0	O	PU	drive 1 (OFF)		1.35/1.5	vdds_ddr1	No	LVCMOS DDR	PUx/PDy	
AB18	ddr1_ba2	ddr1_ba2	0	O	PU	drive 1 (OFF)		1.35/1.5	vdds_ddr1	No	LVCMOS DDR	PUx/PDy	
AC18	ddr1_casn	ddr1_casn	0	O	PU	drive 1 (OFF)		1.35/1.5	vdds_ddr1	No	LVCMOS DDR	PUx/PDy	
AG24	ddr1_ck	ddr1_ck	0	O	PD	drive 0 (OFF)		1.35/1.5	vdds_ddr1	No	LVCMOS DDR	PUx/PDy	
AG22	ddr1_cke	ddr1_cke	0	O	PU	drive 1 (OFF)		1.35/1.5	vdds_ddr1	No	LVCMOS DDR	PUx/PDy	
AH23	ddr1_csn0	ddr1_csn0	0	O	PU	drive 1 (OFF)		1.35/1.5	vdds_ddr1	No	LVCMOS DDR	PUx/PDy	
AB16	ddr1_csn1	ddr1_csn1	0	O	PU	drive 1 (OFF)		1.35/1.5	vdds_ddr1	No	LVCMOS DDR	PUx/PDy	
AF25	ddr1_d0	ddr1_d0	0	IO	PD	PD		1.35/1.5	vdds_ddr1	No	LVCMOS DDR	PUx/PDy	
AF26	ddr1_d1	ddr1_d1	0	IO	PD	PD		1.35/1.5	vdds_ddr1	No	LVCMOS DDR	PUx/PDy	
AG26	ddr1_d2	ddr1_d2	0	IO	PD	PD		1.35/1.5	vdds_ddr1	No	LVCMOS DDR	PUx/PDy	
AH26	ddr1_d3	ddr1_d3	0	IO	PD	PD		1.35/1.5	vdds_ddr1	No	LVCMOS DDR	PUx/PDy	
AF24	ddr1_d4	ddr1_d4	0	IO	PD	PD		1.35/1.5	vdds_ddr1	No	LVCMOS DDR	PUx/PDy	
AE24	ddr1_d5	ddr1_d5	0	IO	PD	PD		1.35/1.5	vdds_ddr1	No	LVCMOS DDR	PUx/PDy	
AF23	ddr1_d6	ddr1_d6	0	IO	PD	PD		1.35/1.5	vdds_ddr1	No	LVCMOS DDR	PUx/PDy	
AE23	ddr1_d7	ddr1_d7	0	IO	PD	PD		1.35/1.5	vdds_ddr1	No	LVCMOS DDR	PUx/PDy	
AC23	ddr1_d8	ddr1_d8	0	IO	PD	PD		1.35/1.5	vdds_ddr1	No	LVCMOS DDR	PUx/PDy	
AF27	ddr1_d9	ddr1_d9	0	IO	PD	PD		1.35/1.5	vdds_ddr1	No	LVCMOS DDR	PUx/PDy	
AG27	ddr1_d10	ddr1_d10	0	IO	PD	PD		1.35/1.5	vdds_ddr1	No	LVCMOS DDR	PUx/PDy	
AF28	ddr1_d11	ddr1_d11	0	IO	PD	PD		1.35/1.5	vdds_ddr1	No	LVCMOS DDR	PUx/PDy	
AE26	ddr1_d12	ddr1_d12	0	IO	PD	PD		1.35/1.5	vdds_ddr1	No	LVCMOS DDR	PUx/PDy	
AC25	ddr1_d13	ddr1_d13	0	IO	PD	PD		1.35/1.5	vdds_ddr1	No	LVCMOS DDR	PUx/PDy	

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	BALL RESET REL. MUXMODE [8]	I/O VOLTAGE VALUE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/DOWN TYPE [13]	DSIS [14]
AC24	ddr1_d14	ddr1_d14	0	IO	PD	PD		1.35/1.5	vdds_ddr1	No	LVCMOS DDR	PUx/PDy	
AD25	ddr1_d15	ddr1_d15	0	IO	PD	PD		1.35/1.5	vdds_ddr1	No	LVCMOS DDR	PUx/PDy	
V20	ddr1_d16	ddr1_d16	0	IO	PD	PD		1.35/1.5	vdds_ddr1	No	LVCMOS DDR	PUx/PDy	
W20	ddr1_d17	ddr1_d17	0	IO	PD	PD		1.35/1.5	vdds_ddr1	No	LVCMOS DDR	PUx/PDy	
AB28	ddr1_d18	ddr1_d18	0	IO	PD	PD		1.35/1.5	vdds_ddr1	No	LVCMOS DDR	PUx/PDy	
AC28	ddr1_d19	ddr1_d19	0	IO	PD	PD		1.35/1.5	vdds_ddr1	No	LVCMOS DDR	PUx/PDy	
AC27	ddr1_d20	ddr1_d20	0	IO	PD	PD		1.35/1.5	vdds_ddr1	No	LVCMOS DDR	PUx/PDy	
Y19	ddr1_d21	ddr1_d21	0	IO	PD	PD		1.35/1.5	vdds_ddr1	No	LVCMOS DDR	PUx/PDy	
AB27	ddr1_d22	ddr1_d22	0	IO	PD	PD		1.35/1.5	vdds_ddr1	No	LVCMOS DDR	PUx/PDy	
Y20	ddr1_d23	ddr1_d23	0	IO	PD	PD		1.35/1.5	vdds_ddr1	No	LVCMOS DDR	PUx/PDy	
AA23	ddr1_d24	ddr1_d24	0	IO	PD	PD		1.35/1.5	vdds_ddr1	No	LVCMOS DDR	PUx/PDy	
Y22	ddr1_d25	ddr1_d25	0	IO	PD	PD		1.35/1.5	vdds_ddr1	No	LVCMOS DDR	PUx/PDy	
Y23	ddr1_d26	ddr1_d26	0	IO	PD	PD		1.35/1.5	vdds_ddr1	No	LVCMOS DDR	PUx/PDy	
AA24	ddr1_d27	ddr1_d27	0	IO	PD	PD		1.35/1.5	vdds_ddr1	No	LVCMOS DDR	PUx/PDy	
Y24	ddr1_d28	ddr1_d28	0	IO	PD	PD		1.35/1.5	vdds_ddr1	No	LVCMOS DDR	PUx/PDy	
AA26	ddr1_d29	ddr1_d29	0	IO	PD	PD		1.35/1.5	vdds_ddr1	No	LVCMOS DDR	PUx/PDy	
AA25	ddr1_d30	ddr1_d30	0	IO	PD	PD		1.35/1.5	vdds_ddr1	No	LVCMOS DDR	PUx/PDy	
AA28	ddr1_d31	ddr1_d31	0	IO	PD	PD		1.35/1.5	vdds_ddr1	No	LVCMOS DDR	PUx/PDy	
AD23	ddr1_dqm0	ddr1_dqm0	0	O	PU	drive 1 (OFF)		1.35/1.5	vdds_ddr1	No	LVCMOS DDR	PUx/PDy	
AB23	ddr1_dqm1	ddr1_dqm1	0	O	PU	drive 1 (OFF)		1.35/1.5	vdds_ddr1	No	LVCMOS DDR	PUx/PDy	
AC26	ddr1_dqm2	ddr1_dqm2	0	O	PU	drive 1 (OFF)		1.35/1.5	vdds_ddr1	No	LVCMOS DDR	PUx/PDy	
AA27	ddr1_dqm3	ddr1_dqm3	0	O	PU	drive 1 (OFF)		1.35/1.5	vdds_ddr1	No	LVCMOS DDR	PUx/PDy	
V26	ddr1_dqm_ecc	ddr1_dqm_ecc	0	O	PU	drive 1 (OFF)		1.35/1.5	vdds_ddr1	No	LVCMOS DDR	PUx/PDy	

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	BALL RESET REL. MUXMODE [8]	I/O VOLTAGE VALUE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/DOWN TYPE [13]	DSIS [14]
AH25	ddr1_dqs0	ddr1_dqs0	0	IO	PD	PD		1.35/1.5	vdds_ddr1		LVCMOS DDR	PUx/PDy	
AE27	ddr1_dqs1	ddr1_dqs1	0	IO	PD	PD		1.35/1.5	vdds_ddr1		LVCMOS DDR	PUx/PDy	
AD27	ddr1_dqs2	ddr1_dqs2	0	IO	PD	PD		1.35/1.5	vdds_ddr1		LVCMOS DDR	PUx/PDy	
Y28	ddr1_dqs3	ddr1_dqs3	0	IO	PD	PD		1.35/1.5	vdds_ddr1		LVCMOS DDR	PUx/PDy	
AG25	ddr1_dqsn0	ddr1_dqsn0	0	IO	PU	PU		1.35/1.5	vdds_ddr1		LVCMOS DDR	PUx/PDy	
AE28	ddr1_dqsn1	ddr1_dqsn1	0	IO	PU	PU		1.35/1.5	vdds_ddr1		LVCMOS DDR	PUx/PDy	
AD28	ddr1_dqsn2	ddr1_dqsn2	0	IO	PU	PU		1.35/1.5	vdds_ddr1		LVCMOS DDR	PUx/PDy	
Y27	ddr1_dqsn3	ddr1_dqsn3	0	IO	PU	PU		1.35/1.5	vdds_ddr1		LVCMOS DDR	PUx/PDy	
V28	ddr1_dqsn_ecc	ddr1_dqsn_ecc	0	IO	PU	PU		1.35/1.5	vdds_ddr1		LVCMOS DDR	PUx/PDy	
V27	ddr1_dqs_ecc	ddr1_dqs_ecc	0	IO	PD	PD		1.35/1.5	vdds_ddr1		LVCMOS DDR	PUx/PDy	
W22	ddr1_ecc_d0	ddr1_ecc_d0	0	IO	PD	PD		1.35/1.5	vdds_ddr1	No	LVCMOS DDR	PUx/PDy	
V23	ddr1_ecc_d1	ddr1_ecc_d1	0	IO	PD	PD		1.35/1.5	vdds_ddr1	No	LVCMOS DDR	PUx/PDy	
W19	ddr1_ecc_d2	ddr1_ecc_d2	0	IO	PD	PD		1.35/1.5	vdds_ddr1	No	LVCMOS DDR	PUx/PDy	
W23	ddr1_ecc_d3	ddr1_ecc_d3	0	IO	PD	PD		1.35/1.5	vdds_ddr1	No	LVCMOS DDR	PUx/PDy	
Y25	ddr1_ecc_d4	ddr1_ecc_d4	0	IO	PD	PD		1.35/1.5	vdds_ddr1	No	LVCMOS DDR	PUx/PDy	
V24	ddr1_ecc_d5	ddr1_ecc_d5	0	IO	PD	PD		1.35/1.5	vdds_ddr1	No	LVCMOS DDR	PUx/PDy	
V25	ddr1_ecc_d6	ddr1_ecc_d6	0	IO	PD	PD		1.35/1.5	vdds_ddr1	No	LVCMOS DDR	PUx/PDy	
Y26	ddr1_ecc_d7	ddr1_ecc_d7	0	IO	PD	PD		1.35/1.5	vdds_ddr1	No	LVCMOS DDR	PUx/PDy	
AH24	ddr1_nck	ddr1_nck	0	O	PU	drive 1 (OFF)		1.35/1.5	vdds_ddr1	No	LVCMOS DDR	PUx/PDy	
AE20	ddr1_odt0	ddr1_odt0	0	O	PD	drive 0 (OFF)		1.35/1.5	vdds_ddr1	No	LVCMOS DDR	PUx/PDy	
AC17	ddr1_odt1	ddr1_odt1	0	O	PD	drive 0 (OFF)		1.35/1.5	vdds_ddr1	No	LVCMOS DDR	PUx/PDy	
AF20	ddr1_rasn	ddr1_rasn	0	O	PU	drive 1 (OFF)		1.35/1.5	vdds_ddr1	No	LVCMOS DDR	PUx/PDy	
AG21	ddr1_rst	ddr1_rst	0	O	PD	drive 0 (OFF)		1.35/1.5	vdds_ddr1	No	LVCMOS DDR	PUx/PDy	

Table 4-2. Ball Characteristics[1] (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	BALL RESET REL. MUXMODE [8]	I/O VOLTAGE VALUE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/DOWN TYPE [13]	DSIS [14]
Y18	ddr1_vref0	ddr1_vref0	0	PWR	OFF	drive 1 (OFF)		1.35/1.5	vdds_ddr1	No	LVCMOS DDR		
AH21	ddr1_wen	ddr1_wen	0	O	PU	drive 1 (OFF)		1.35/1.5	vdds_ddr1	No	LVCMOS DDR	PUx/PDy	
G21	emu0	emu0	0	IO	PU	PU	0	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	
		gpio8_30	14	IO									
D24	emu1	emu1	0	IO	PU	PU	0	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	
		gpio8_31	14	IO									
AC5	gpio6_10	gpio6_10	0	IO	PU	PU	15	1.8/3.3	vddshv7	Yes	Dual Voltage LVCMOS	PU/PD	
		mdio_mclk	1	O									1
		i2c3_sda	2	IO									1
		usb3_ulpi_d7	3	IO									0
		vin2b_hsync1	4	I									
		vin1a_clk0	9	I									0
		ehrpwm2A	10	O									
		gpio6_10	14	IO									
		Driver off	15	I									
AB4	gpio6_11	gpio6_11	0	IO	PU	PU	15	1.8/3.3	vddshv7	Yes	Dual Voltage LVCMOS	PU/PD	
		mdio_d	1	IO									1
		i2c3_scl	2	IO									1
		usb3_ulpi_d6	3	IO									0
		vin2b_vsync1	4	I									
		vin1a_de0	9	I									0
		ehrpwm2B	10	O									
		gpio6_11	14	IO									
		Driver off	15	I									
E21	gpio6_14	gpio6_14	0	IO	PU	PU	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	
		mcasp1_axr8	1	IO									0
		dcan2_tx	2	IO									1
		uart10_rxd	3	I									1
		vout2_hsync	6	O									
		vin2a_hsync0 vin1a_hsync0	8	I									
		i2c3_sda	9	IO									1
		timer1	10	IO									
		gpio6_14	14	IO									
		Driver off	15	I									

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	BALL RESET REL. MUXMODE [8]	I/O VOLTAGE VALUE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/DOWN TYPE [13]	DSIS [14]
F20	gpio6_15	gpio6_15	0	IO	PU	PU	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	
		mcasp1_axr9	1	IO									0
		dcan2_rx	2	IO									1
		uart10_txd	3	O									
		vout2_vsync	6	O									
		vin2a_vsync0 vin1a_vsync0	8	I									
		i2c3_scl	9	IO									1
		timer2	10	IO									
		gpio6_15	14	IO									
		Driver off	15	I									
F21	gpio6_16	gpio6_16	0	IO	PU	PU	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	
		mcasp1_axr10	1	IO									0
		vout2_fld	6	O									
		vin2a_fld0 vin1a_fld0	8	I									
		clkout1	9	O									
		timer3	10	IO									
		gpio6_16	14	IO									
		Driver off	15	I									
R6	gpmc_a0	gpmc_a0	0	O	PD	PD	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	
		vin1a_d16	2	I									0
		vout3_d16	3	O									
		vin2a_d0 vin1a_d0	4	I									
		vin1b_d0	6	I									0
		i2c4_scl	7	IO									1
		uart5_rxd	8	I									1
		gpio7_3 gpmc_a26 gpmc_a16	14	IO									
		Driver off	15	I									

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	BALL RESET REL. MUXMODE [8]	I/O VOLTAGE VALUE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/DOWN TYPE [13]	DSIS [14]
T9	gpmc_a1	gpmc_a1	0	O	PD	PD	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	
		vin1a_d17	2	I									0
		vout3_d17	3	O									
		vin2a_d1 vin1a_d1	4	I									
		vin1b_d1	6	I									0
		i2c4_sda	7	IO									1
		uart5_txd	8	O									
		gpio7_4	14	IO									
		Driver off	15	I									
T6	gpmc_a2	gpmc_a2	0	O	PD	PD	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	
		vin1a_d18	2	I									0
		vout3_d18	3	O									
		vin2a_d2 vin1a_d2	4	I									
		vin1b_d2	6	I									0
		uart7_rxd	7	I									1
		uart5_ctsn	8	I									1
		gpio7_5	14	IO									
		Driver off	15	I									
T7	gpmc_a3	gpmc_a3	0	O	PD	PD	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	
		qspi1_cs2	1	O									1
		vin1a_d19	2	I									0
		vout3_d19	3	O									
		vin2a_d3 vin1a_d3	4	I									
		vin1b_d3	6	I									0
		uart7_txd	7	O									
		uart5_rtsn	8	O									
		gpio7_6	14	IO									
		Driver off	15	I									

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	BALL RESET REL. MUXMODE [8]	I/O VOLTAGE VALUE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/DOWN TYPE [13]	DSIS [14]
P6	gpmc_a4	gpmc_a4	0	O	PD	PD	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	
		qspi1_cs3	1	O									1
		vin1a_d20	2	I									0
		vout3_d20	3	O									
		vin2a_d4 vin1a_d4	4	I									
		vin1b_d4	6	I									0
		i2c5_scl	7	IO									1
		uart6_rxd	8	I									1
		gpio1_26	14	IO									
		Driver off	15	I									
R9	gpmc_a5	gpmc_a5	0	O	PD	PD	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	
		vin1a_d21	2	I									0
		vout3_d21	3	O									
		vin2a_d5 vin1a_d5	4	I									
		vin1b_d5	6	I									0
		i2c5_sda	7	IO									1
		uart6_txd	8	O									
		gpio1_27	14	IO									
		Driver off	15	I									
R5	gpmc_a6	gpmc_a6	0	O	PD	PD	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	
		vin1a_d22	2	I									0
		vout3_d22	3	O									
		vin2a_d6 vin1a_d6	4	I									
		vin1b_d6	6	I									0
		uart8_rxd	7	I									1
		uart6_ctsn	8	I									1
		gpio1_28	14	IO									
		Driver off	15	I									

Table 4-2. Ball Characteristics[(1)] (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	BALL RESET REL. MUXMODE [8]	I/O VOLTAGE VALUE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/DOWN TYPE [13]	DSIS [14]
P5	gpmc_a7	gpmc_a7	0	O	PD	PD	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	
		vin1a_d23	2	I									0
		vout3_d23	3	O									
		vin2a_d7 vin1a_d7	4	I									
		vin1b_d7	6	I									0
		uart8_txd	7	O									
		uart6_rtsn	8	O									
		gpio1_29	14	IO									
		Driver off	15	I									
N7	gpmc_a8	gpmc_a8	0	O	PD	PD	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	
		vin1a_hsync0	2	I									0
		vout3_hsync	3	O									
		vin1b_hsync1	6	I									0
		timer12	7	IO									
		spi4_sclk	8	IO									0
		gpio1_30	14	IO									
		Driver off	15	I									
R4	gpmc_a9	gpmc_a9	0	O	PD	PD	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	
		vin1a_vsync0	2	I									0
		vout3_vsync	3	O									
		vin1b_vsync1	6	I									0
		timer11	7	IO									
		spi4_d1	8	IO									0
		gpio1_31	14	IO									
		Driver off	15	I									
N9	gpmc_a10	gpmc_a10	0	O	PD	PD	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	
		vin1a_de0	2	I									0
		vout3_de	3	O									
		vin1b_clk1	6	I									0
		timer10	7	IO									
		spi4_d0	8	IO									0
		gpio2_0	14	IO									
		Driver off	15	I									

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	BALL RESET REL. MUXMODE [8]	I/O VOLTAGE VALUE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/DOWN TYPE [13]	DSIS [14]
P9	gpmc_a11	gpmc_a11	0	O	PD	PD	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	
		vin1a_fld0	2	I									0
		vout3_fld	3	O									
		vin2a_fld0 vin1a_fld0	4	I									
		vin1b_de1	6	I									0
		timer9	7	IO									
		spi4_cs0	8	IO									1
		gpio2_1	14	IO									
		Driver off	15	I									
P4	gpmc_a12	gpmc_a12	0	O	PD	PD	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	
		vin2a_clk0 vin1a_clk0	4	I									
		gpmc_a0	5	O									
		vin1b_fld1	6	I									0
		timer8	7	IO									
		spi4_cs1	8	IO									1
		dma_evt1	9	I									0
		gpio2_2	14	IO									
		Driver off	15	I									
R3	gpmc_a13	gpmc_a13	0	O	PD	PD	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	
		qspi1_rtclk	1	I									0
		vin2a_hsync0 vin1a_hsync0	4	I									
		timer7	7	IO									
		spi4_cs2	8	IO									1
		dma_evt2	9	I									0
		gpio2_3	14	IO									
		Driver off	15	I									
T2	gpmc_a14	gpmc_a14	0	O	PD	PD	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	
		qspi1_d3	1	IO									0
		vin2a_vsync0 vin1a_vsync0	4	I									
		timer6	7	IO									
		spi4_cs3	8	IO									1
		gpio2_4	14	IO									
		Driver off	15	I									

Table 4-2. Ball Characteristics[(1)] (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	BALL RESET REL. MUXMODE [8]	I/O VOLTAGE VALUE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/DOWN TYPE [13]	DSIS [14]
U2	gpmc_a15	gpmc_a15	0	O	PD	PD	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	
		qspi1_d2	1	IO									0
		vin2a_d8 vin1a_d8	4	I									
		timer5	7	IO									
		gpio2_5	14	IO									
		Driver off	15	I									
U1	gpmc_a16	gpmc_a16	0	O	PD	PD	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	
		qspi1_d0	1	IO									0
		vin2a_d9 vin1a_d9	4	I									
		gpio2_6	14	IO									
		Driver off	15	I									
P3	gpmc_a17	gpmc_a17	0	O	PD	PD	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	
		qspi1_d1	1	IO									0
		vin2a_d10 vin1a_d10	4	I									
		gpio2_7	14	IO									
		Driver off	15	I									
R2	gpmc_a18	gpmc_a18	0	O	PD	PD	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	
		qspi1_sclk	1	IO									
		vin2a_d11 vin1a_d11	4	I									
		gpio2_8	14	IO									
		Driver off	15	I									
K7[(9)]	gpmc_a19	gpmc_a19	0	O	PD	PD	15	1.8/3.3	vddshv11	Yes	Dual Voltage LVCMOS	PU/PD	
		mmc2_dat4	1	IO									1
		gpmc_a13	2	O									
		vin2a_d12 vin1a_d12	4	I									
		vin2b_d0 vin1b_d0	6	I									
		gpio2_9	14	IO									
		Driver off	15	I									

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	BALL RESET REL. MUXMODE [8]	I/O VOLTAGE VALUE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/DOWN TYPE [13]	DSIS [14]
M7(9)	gpmc_a20	gpmc_a20	0	O	PD	PD	15	1.8/3.3	vddshv11	Yes	Dual Voltage LVCMOS	PU/PD	
		mmc2_dat5	1	IO									1
		gpmc_a14	2	O									
		vin2a_d13 vin1a_d13	4	I									
		vin2b_d1 vin1b_d1	6	I									
		gpio2_10	14	IO									
		Driver off	15	I									
J5(9)	gpmc_a21	gpmc_a21	0	O	PD	PD	15	1.8/3.3	vddshv11	Yes	Dual Voltage LVCMOS	PU/PD	
		mmc2_dat6	1	IO									1
		gpmc_a15	2	O									
		vin2a_d14 vin1a_d14	4	I									
		vin2b_d2 vin1b_d2	6	I									
		gpio2_11	14	IO									
		Driver off	15	I									
K6(9)	gpmc_a22	gpmc_a22	0	O	PD	PD	15	1.8/3.3	vddshv11	Yes	Dual Voltage LVCMOS	PU/PD	
		mmc2_dat7	1	IO									1
		gpmc_a16	2	O									
		vin2a_d15 vin1a_d15	4	I									
		vin2b_d3 vin1b_d3	6	I									
		gpio2_12	14	IO									
		Driver off	15	I									
J7	gpmc_a23	gpmc_a23	0	O	PD	PD	15	1.8/3.3	vddshv11	Yes	Dual Voltage LVCMOS	PU/PD	
		mmc2_clk	1	IO									1
		gpmc_a17	2	O									
		vin2a_fld0 vin1a_fld0	4	I									
		vin2b_d4 vin1b_d4	6	I									
		gpio2_13	14	IO									
		Driver off	15	I									

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	BALL RESET REL. MUXMODE [8]	I/O VOLTAGE VALUE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/DOWN TYPE [13]	DSIS [14]
J4 (9)	gpmc_a24	gpmc_a24	0	O	PD	PD	15	1.8/3.3	vddshv11	Yes	Dual Voltage LVCMOS	PU/PD	
		mmc2_dat0	1	IO									1
		gpmc_a18	2	O									
		vin2b_d5 vin1b_d5	6	I									
		gpio2_14	14	IO									
		Driver off	15	I									
J6 (9)	gpmc_a25	gpmc_a25	0	O	PD	PD	15	1.8/3.3	vddshv11	Yes	Dual Voltage LVCMOS	PU/PD	
		mmc2_dat1	1	IO									1
		gpmc_a19	2	O									
		vin2b_d6 vin1b_d6	6	I									
		gpio2_15	14	IO									
		Driver off	15	I									
H4 (9)	gpmc_a26	gpmc_a26	0	O	PD	PD	15	1.8/3.3	vddshv11	Yes	Dual Voltage LVCMOS	PU/PD	
		mmc2_dat2	1	IO									1
		gpmc_a20	2	O									
		vin2b_d7 vin1b_d7	6	I									
		gpio2_16	14	IO									
		Driver off	15	I									
H5 (9)	gpmc_a27	gpmc_a27	0	O	PD	PD	15	1.8/3.3	vddshv11	Yes	Dual Voltage LVCMOS	PU/PD	
		mmc2_dat3	1	IO									1
		gpmc_a21	2	O									
		vin2b_hsync1 vin1b_hsync1	6	I									
		gpio2_17	14	IO									
		Driver off	15	I									
M6	gpmc_ad0	gpmc_ad0	0	IO	OFF	OFF	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin1a_d0	2	I									0
		vout3_d0	3	O									
		gpio1_6	14	IO									
		sysboot0	15	I									
M2	gpmc_ad1	gpmc_ad1	0	IO	OFF	OFF	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin1a_d1	2	I									0
		vout3_d1	3	O									
		gpio1_7	14	IO									
		sysboot1	15	I									

Table 4-2. Ball Characteristics[(1)] (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	BALL RESET REL. MUXMODE [8]	I/O VOLTAGE VALUE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/DOWN TYPE [13]	DSIS [14]
L5	gpmc_ad2	gpmc_ad2	0	IO	OFF	OFF	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin1a_d2	2	I									0
		vout3_d2	3	O									
		gpio1_8	14	IO									
		sysboot2	15	I									
M1	gpmc_ad3	gpmc_ad3	0	IO	OFF	OFF	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin1a_d3	2	I									0
		vout3_d3	3	O									
		gpio1_9	14	IO									
		sysboot3	15	I									
L6	gpmc_ad4	gpmc_ad4	0	IO	OFF	OFF	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin1a_d4	2	I									0
		vout3_d4	3	O									
		gpio1_10	14	IO									
		sysboot4	15	I									
L4	gpmc_ad5	gpmc_ad5	0	IO	OFF	OFF	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin1a_d5	2	I									0
		vout3_d5	3	O									
		gpio1_11	14	IO									
		sysboot5	15	I									
L3	gpmc_ad6	gpmc_ad6	0	IO	OFF	OFF	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin1a_d6	2	I									0
		vout3_d6	3	O									
		gpio1_12	14	IO									
		sysboot6	15	I									
L2	gpmc_ad7	gpmc_ad7	0	IO	OFF	OFF	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin1a_d7	2	I									0
		vout3_d7	3	O									
		gpio1_13	14	IO									
		sysboot7	15	I									
L1	gpmc_ad8	gpmc_ad8	0	IO	OFF	OFF	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin1a_d8	2	I									0
		vout3_d8	3	O									
		gpio7_18	14	IO									
		sysboot8	15	I									

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	BALL RESET REL. MUXMODE [8]	I/O VOLTAGE VALUE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/DOWN TYPE [13]	DSIS [14]
K2	gpmc_ad9	gpmc_ad9	0	IO	OFF	OFF	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin1a_d9	2	I									0
		vout3_d9	3	O									
		gpio7_19	14	IO									
		sysboot9	15	I									
J1	gpmc_ad10	gpmc_ad10	0	IO	OFF	OFF	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin1a_d10	2	I									0
		vout3_d10	3	O									
		gpio7_28	14	IO									
		sysboot10	15	I									
J2	gpmc_ad11	gpmc_ad11	0	IO	OFF	OFF	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin1a_d11	2	I									0
		vout3_d11	3	O									
		gpio7_29	14	IO									
		sysboot11	15	I									
H1	gpmc_ad12	gpmc_ad12	0	IO	OFF	OFF	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin1a_d12	2	I									0
		vout3_d12	3	O									
		gpio1_18	14	IO									
		sysboot12	15	I									
J3	gpmc_ad13	gpmc_ad13	0	IO	OFF	OFF	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin1a_d13	2	I									0
		vout3_d13	3	O									
		gpio1_19	14	IO									
		sysboot13	15	I									
H2	gpmc_ad14	gpmc_ad14	0	IO	OFF	OFF	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin1a_d14	2	I									0
		vout3_d14	3	O									
		gpio1_20	14	IO									
		sysboot14	15	I									
H3	gpmc_ad15	gpmc_ad15	0	IO	OFF	OFF	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin1a_d15	2	I									0
		vout3_d15	3	O									
		gpio1_21	14	IO									
		sysboot15	15	I									

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	BALL RESET REL. MUXMODE [8]	I/O VOLTAGE VALUE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/DOWN TYPE [13]	DSIS [14]
N1	gpmc_advn_ale	gpmc_advn_ale	0	O	PU	PU	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	
		gpmc_cs6	1	O									
		clkout2	2	O									
		gpmc_wait1	3	I									1
		vin2a_vsync0 vin1a_vsync0	4	I									
		gpmc_a2	5	O									
		gpmc_a23	6	O									
		timer3	7	IO									
		i2c3_sda	8	IO									1
		dma_evt2	9	I									0
		gpio2_23 gpmc_a19	14	IO									
		Driver off	15	I									
N6	gpmc_ben0	gpmc_ben0	0	O	PU	PU	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	
		gpmc_cs4	1	O									
		vin2b_de1 vin1b_de1	6	I									
		timer2	7	IO									
		dma_evt3	9	I									0
		gpio2_26 gpmc_a21	14	IO									
		Driver off	15	I									
M4	gpmc_ben1	gpmc_ben1	0	O	PU	PU	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	
		gpmc_cs5	1	O									
		vin2b_clk1 vin1b_clk1	4	I									
		gpmc_a3	5	O									
		vin2b_fld1 vin1b_fld1	6	I									
		timer1	7	IO									
		dma_evt4	9	I									0
		gpio2_27 gpmc_a22	14	IO									
		Driver off	15	I									

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	BALL RESET REL. MUXMODE [8]	I/O VOLTAGE VALUE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/DOWN TYPE [13]	DSIS [14]
P7	gpmc_clk	gpmc_clk	0	IO	PU	PU	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	0
		gpmc_cs7	1	O									
		clkout1	2	O									
		gpmc_wait1	3	I									1
		vin2a_hsync0 vin1a_hsync0	4	I									
		vin2a_de0 vin1a_de0	5	I									
		vin2b_clk1 vin1b_clk1	6	I									
		timer4	7	IO									
		i2c3_scl	8	IO									1
		dma_evt1	9	I									0
		gpio2_22 gpmc_a20	14	IO									
		Driver off	15	I									
T1	gpmc_cs0	gpmc_cs0	0	O	PU	PU	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	
		gpio2_19	14	IO									
		Driver off	15	I									
H6	gpmc_cs1	gpmc_cs1	0	O	PU	PU	15	1.8/3.3	vddshv11	Yes	Dual Voltage LVCMOS	PU/PD	
		mmc2_cmd	1	IO									1
		gpmc_a22	2	O									
		vin2a_de0 vin1a_de0	4	I									
		vin2b_vsync1 vin1b_vsync1	6	I									
		gpio2_18	14	IO									
		Driver off	15	I									
P2	gpmc_cs2	gpmc_cs2	0	O	PU	PU	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	
		qspi1_cs0	1	IO									1
		gpio2_20 gpmc_a23 gpmc_a13	14	IO									
		Driver off	15	I									

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	BALL RESET REL. MUXMODE [8]	I/O VOLTAGE VALUE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/DOWN TYPE [13]	DSIS [14]
P1	gpmc_cs3	gpmc_cs3	0	O	PU	PU	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	
		qspi1_cs1	1	O									1
		vin1a_clk0	2	I									0
		vout3_clk	3	O									
		gpmc_a1	5	O									
		gpio2_21 gpmc_a24 gpmc_a14	14	IO									
		Driver off	15	I									
M5	gpmc_oen_ren	gpmc_oen_ren	0	O	PU	PU	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	
		gpio2_24	14	IO									
		Driver off	15	I									
N2	gpmc_wait0	gpmc_wait0	0	I	PU	PU	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	1
		gpio2_28 gpmc_a25 gpmc_a15	14	IO									
		Driver off	15	I									
M3	gpmc_wen	gpmc_wen	0	O	PU	PU	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	
		gpio2_25	14	IO									
		Driver off	15	I									
AG16	hdmi1_clockx	hdmi1_clockx	0	O				1.8	vdda_hdmi		HDMIPHY	Pdy	
AH16	hdmi1_clocky	hdmi1_clocky	0	O				1.8	vdda_hdmi		HDMIPHY	Pdy	
AG17	hdmi1_data0x	hdmi1_data0x	0	O				1.8	vdda_hdmi		HDMIPHY	Pdy	
AH17	hdmi1_data0y	hdmi1_data0y	0	O				1.8	vdda_hdmi		HDMIPHY	Pdy	
AG18	hdmi1_data1x	hdmi1_data1x	0	O				1.8	vdda_hdmi		HDMIPHY	Pdy	
AH18	hdmi1_data1y	hdmi1_data1y	0	O				1.8	vdda_hdmi		HDMIPHY	Pdy	
AG19	hdmi1_data2x	hdmi1_data2x	0	O				1.8	vdda_hdmi		HDMIPHY	Pdy	
AH19	hdmi1_data2y	hdmi1_data2y	0	O				1.8	vdda_hdmi		HDMIPHY	Pdy	
C20	i2c1_scl	i2c1_scl	0	IO				1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS I2C	PU/PD	
		Driver off	15	I									
C21	i2c1_sda	i2c1_sda	0	IO				1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS I2C	PU/PD	
		Driver off	15	I									
F17	i2c2_scl	i2c2_scl	0	IO			15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS I2C	PU/PD	1
		hdmi1_ddc_sda	1	IO									
		Driver off	15	I									
C25	i2c2_sda	i2c2_sda	0	IO			15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS I2C	PU/PD	1
		hdmi1_ddc_scl	1	IO									
		Driver off	15	I									
AH15	ljcb_clkn	ljcb_clkn	0	IO				1.8	vdda_pcie		LJCB		

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	BALL RESET REL. MUXMODE [8]	I/O VOLTAGE VALUE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/DOWN TYPE [13]	DSIS [14]
AG15	ljcb_clkp	ljcb_clkp	0	IO				1.8	vdda_pcie		LJCB		
B14	mcasp1_aclkr	mcasp1_aclkr	0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		mcasp7_axr2	1	IO									0
		vout2_d0	6	O									
		vin2a_d0 vin1a_d0	8	I									
		i2c4_sda	10	IO									1
		gpio5_0	14	IO									
		Driver off	15	I									
C14	mcasp1_aclkx	mcasp1_aclkx	0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin1a_fld0	7	I									0
		i2c3_sda	10	IO									1
		gpio7_31	14	IO									
		Driver off	15	I									
G12	mcasp1_axr0	mcasp1_axr0	0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		uart6_rxd	3	I									1
		vin1a_vsync0	7	I									0
		i2c5_sda	10	IO									1
		gpio5_2	14	IO									
		Driver off	15	I									
F12	mcasp1_axr1	mcasp1_axr1	0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		uart6_txd	3	O									
		vin1a_hsync0	7	I									0
		i2c5_scl	10	IO									1
		gpio5_3	14	IO									
		Driver off	15	I									
G13	mcasp1_axr2	mcasp1_axr2	0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		mcasp6_axr2	1	IO									0
		uart6_ctsn	3	I									1
		vout2_d2	6	O									
		vin2a_d2 vin1a_d2	8	I									
		gpio5_4	14	IO									
		Driver off	15	I									

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	BALL RESET REL. MUXMODE [8]	I/O VOLTAGE VALUE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/DOWN TYPE [13]	DSIS [14]
J11	mcasp1_axr3	mcasp1_axr3	0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		mcasp6_axr3	1	IO									0
		uart6_rtsn	3	O									
		vout2_d3	6	O									
		vin2a_d3 vin1a_d3	8	I									
		gpio5_5	14	IO									
		Driver off	15	I									
E12	mcasp1_axr4	mcasp1_axr4	0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		mcasp4_axr2	1	IO									0
		vout2_d4	6	O									
		vin2a_d4 vin1a_d4	8	I									
		gpio5_6	14	IO									
		Driver off	15	I									
F13	mcasp1_axr5	mcasp1_axr5	0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		mcasp4_axr3	1	IO									0
		vout2_d5	6	O									
		vin2a_d5 vin1a_d5	8	I									
		gpio5_7	14	IO									
		Driver off	15	I									
C12	mcasp1_axr6	mcasp1_axr6	0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		mcasp5_axr2	1	IO									0
		vout2_d6	6	O									
		vin2a_d6 vin1a_d6	8	I									
		gpio5_8	14	IO									
		Driver off	15	I									
D12	mcasp1_axr7	mcasp1_axr7	0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		mcasp5_axr3	1	IO									0
		vout2_d7	6	O									
		vin2a_d7 vin1a_d7	8	I									
		timer4	10	IO									
		gpio5_9	14	IO									
		Driver off	15	I									

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	BALL RESET REL. MUXMODE [8]	I/O VOLTAGE VALUE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/DOWN TYPE [13]	DSIS [14]
B12	mcasp1_axr8	mcasp1_axr8	0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		mcasp6_axr0	1	IO									0
		spi3_sclk	3	IO									0
		vin1a_d15	7	I									0
		timer5	10	IO									
		gpio5_10	14	IO									
		Driver off	15	I									
A11	mcasp1_axr9	mcasp1_axr9	0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		mcasp6_axr1	1	IO									0
		spi3_d1	3	IO									0
		vin1a_d14	7	I									0
		timer6	10	IO									
		gpio5_11	14	IO									
		Driver off	15	I									
B13	mcasp1_axr10	mcasp1_axr10	0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		mcasp6_aclkx	1	IO									0
		mcasp6_aclkr	2	IO									
		spi3_d0	3	IO									0
		vin1a_d13	7	I									0
		timer7	10	IO									
		gpio5_12	14	IO									
		Driver off	15	I									
A12	mcasp1_axr11	mcasp1_axr11	0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		mcasp6_fsx	1	IO									0
		mcasp6_fsr	2	IO									
		spi3_cs0	3	IO									1
		vin1a_d12	7	I									0
		timer8	10	IO									
		gpio4_17	14	IO									
		Driver off	15	I									
E14	mcasp1_axr12	mcasp1_axr12	0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		mcasp7_axr0	1	IO									0
		spi3_cs1	3	IO									1
		vin1a_d11	7	I									0
		timer9	10	IO									
		gpio4_18	14	IO									
		Driver off	15	I									

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	BALL RESET REL. MUXMODE [8]	I/O VOLTAGE VALUE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/DOWN TYPE [13]	DSIS [14]
A13	mcasp1_axr13	mcasp1_axr13	0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		mcasp7_axr1	1	IO									0
		vin1a_d10	7	I									0
		timer10	10	IO									
		gpio6_4	14	IO									
		Driver off	15	I									
G14	mcasp1_axr14	mcasp1_axr14	0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		mcasp7_aclkx	1	IO									0
		mcasp7_aclkr	2	IO									
		vin1a_d9	7	I									0
		timer11	10	IO									
		gpio6_5	14	IO									
		Driver off	15	I									
F14	mcasp1_axr15	mcasp1_axr15	0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		mcasp7_fsx	1	IO									0
		mcasp7_fsr	2	IO									
		vin1a_d8	7	I									0
		timer12	10	IO									
		gpio6_6	14	IO									
		Driver off	15	I									
J14	mcasp1_fsr	mcasp1_fsr	0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		mcasp7_axr3	1	IO									0
		vout2_d1	6	O									
		vin2a_d1 vin1a_d1	8	I									
		i2c4_scl	10	IO									1
		gpio5_1	14	IO									
		Driver off	15	I									
D14	mcasp1_fsx	mcasp1_fsx	0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin1a_de0	7	I									0
		i2c3_scl	10	IO									1
		gpio7_30	14	IO									
		Driver off	15	I									

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	BALL RESET REL. MUXMODE [8]	I/O VOLTAGE VALUE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/DOWN TYPE [13]	DSIS [14]
E15	mcasp2_aclkr	mcasp2_aclkr	0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		mcasp8_axr2	1	IO									0
		vout2_d8	6	O									
		vin2a_d8 vin1a_d8	8	I									
		Driver off	15	I									
A19	mcasp2_aclkx	mcasp2_aclkx	0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin1a_d7	7	I									0
		Driver off	15	I									
B15	mcasp2_axr0	mcasp2_axr0	0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		vout2_d10	6	O									
		vin2a_d10 vin1a_d10	8	I									
		Driver off	15	I									
A15	mcasp2_axr1	mcasp2_axr1	0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		vout2_d11	6	O									
		vin2a_d11 vin1a_d11	8	I									
		Driver off	15	I									
C15	mcasp2_axr2	mcasp2_axr2	0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		mcasp3_axr2	1	IO									0
		vin1a_d5	7	I									0
		gpio6_8	14	IO									
		Driver off	15	I									
A16	mcasp2_axr3	mcasp2_axr3	0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		mcasp3_axr3	1	IO									0
		vin1a_d4	7	I									0
		gpio6_9	14	IO									
		Driver off	15	I									
D15	mcasp2_axr4	mcasp2_axr4	0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		mcasp8_axr0	1	IO									0
		vout2_d12	6	O									
		vin2a_d12 vin1a_d12	8	I									
		gpio1_4	14	IO									
		Driver off	15	I									

Table 4-2. Ball Characteristics[(1)] (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	BALL RESET REL. MUXMODE [8]	I/O VOLTAGE VALUE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/DOWN TYPE [13]	DSIS [14]
B16	mcasp2_axr5	mcasp2_axr5	0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		mcasp8_axr1	1	IO									0
		vout2_d13	6	O									
		vin2a_d13 vin1a_d13	8	I									
		gpio6_7	14	IO									
		Driver off	15	I									
B17	mcasp2_axr6	mcasp2_axr6	0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		mcasp8_aclkx	1	IO									0
		mcasp8_aclkr	2	IO									
		vout2_d14	6	O									
		vin2a_d14 vin1a_d14	8	I									
		gpio2_29	14	IO									
		Driver off	15	I									
A17	mcasp2_axr7	mcasp2_axr7	0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		mcasp8_fsx	1	IO									0
		mcasp8_fsr	2	IO									
		vout2_d15	6	O									
		vin2a_d15 vin1a_d15	8	I									
		gpio1_5	14	IO									
		Driver off	15	I									
A20	mcasp2_fsr	mcasp2_fsr	0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		mcasp8_axr3	1	IO									0
		vout2_d9	6	O									
		vin2a_d9 vin1a_d9	8	I									
		Driver off	15	I									
A18	mcasp2_fsx	mcasp2_fsx	0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin1a_d6	7	I									0
		Driver off	15	I									
B18	mcasp3_aclkx	mcasp3_aclkx	0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		mcasp3_aclkr	1	IO									
		mcasp2_axr12	2	IO									0
		uart7_rxd	3	I									1
		vin1a_d3	7	I									0
		gpio5_13	14	IO									
		Driver off	15	I									

Table 4-2. Ball Characteristics[(1)] (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	BALL RESET REL. MUXMODE [8]	I/O VOLTAGE VALUE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/DOWN TYPE [13]	DSIS [14]
B19	mcasp3_axr0	mcasp3_axr0	0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		mcasp2_axr14	2	IO									0
		uart7_ctsn	3	I									1
		uart5_rxd	4	I									1
		vin1a_d1	7	I									0
		Driver off	15	I									
C17	mcasp3_axr1	mcasp3_axr1	0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		mcasp2_axr15	2	IO									0
		uart7_rtsn	3	O									
		uart5_txd	4	O									
		vin1a_d0	7	I									0
		vin1a_fld0	9	I									0
		Driver off	15	I									
F15	mcasp3_fsx	mcasp3_fsx	0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		mcasp3_fsr	1	IO									
		mcasp2_axr13	2	IO									0
		uart7_txd	3	O									
		vin1a_d2	7	I									0
		gpio5_14	14	IO									
		Driver off	15	I									
C18	mcasp4_aclkx	mcasp4_aclkx	0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		mcasp4_aclkr	1	IO									
		spi3_sclk	2	IO									0
		uart8_rxd	3	I									1
		i2c4_sda	4	IO									1
		vout2_d16	6	O									
		vin2a_d16 vin1a_d16	8	I									
		vin1a_d15	9	I									0
		Driver off	15	I									

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	BALL RESET REL. MUXMODE [8]	I/O VOLTAGE VALUE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/DOWN TYPE [13]	DSIS [14]
G16	mcasp4_axr0	mcasp4_axr0	0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		spi3_d0	2	IO									0
		uart8_ctsn	3	I									1
		uart4_rxd	4	I									1
		vout2_d18	6	O									
		vin2a_d18 vin1a_d18	8	I									
		vin1a_d13	9	I									0
		i2c6_scl	14	IO									
		Driver off	15	I									
D17	mcasp4_axr1	mcasp4_axr1	0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		spi3_cs0	2	IO									1
		uart8_rtsn	3	O									
		uart4_txd	4	O									
		vout2_d19	6	O									
		vin2a_d19 vin1a_d19	8	I									
		vin1a_d12	9	I									0
		i2c6_sda	14	IO									
		Driver off	15	I									
A21	mcasp4_fsx	mcasp4_fsx	0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		mcasp4_fsr	1	IO									
		spi3_d1	2	IO									0
		uart8_txd	3	O									
		i2c4_scl	4	IO									1
		vout2_d17	6	O									
		vin2a_d17 vin1a_d17	8	I									
		vin1a_d14	9	I									0
		Driver off	15	I									

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	BALL RESET REL. MUXMODE [8]	I/O VOLTAGE VALUE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/DOWN TYPE [13]	DSIS [14]
AA3	mcasp5_aclkx	mcasp5_aclkx	0	IO	PD	PD	15	1.8/3.3	vddshv7	Yes	Dual Voltage LVCMOS	PU/PD	0
		mcasp5_aclkr	1	IO									
		spi4_sclk	2	IO									0
		uart9_rxd	3	I									1
		i2c5_sda	4	IO									1
		vout2_d20	6	O									
		vin2a_d20 vin1a_d20	8	I									
		vin1a_d11	9	I									0
		Driver off	15	I									
AB3	mcasp5_axr0	mcasp5_axr0	0	IO	PD	PD	15	1.8/3.3	vddshv7	Yes	Dual Voltage LVCMOS	PU/PD	0
		spi4_d0	2	IO									0
		uart9_ctsn	3	I									1
		uart3_rxd	4	I									1
		vout2_d22	6	O									
		vin2a_d22 vin1a_d22	8	I									
		vin1a_d9	9	I									0
		Driver off	15	I									
AA4	mcasp5_axr1	mcasp5_axr1	0	IO	PD	PD	15	1.8/3.3	vddshv7	Yes	Dual Voltage LVCMOS	PU/PD	0
		spi4_cs0	2	IO									1
		uart9_rtsn	3	O									
		uart3_txd	4	O									
		vout2_d23	6	O									
		vin2a_d23 vin1a_d23	8	I									
		vin1a_d8	9	I									0
		Driver off	15	I									
AB9	mcasp5_fsx	mcasp5_fsx	0	IO	PD	PD	15	1.8/3.3	vddshv7	Yes	Dual Voltage LVCMOS	PU/PD	0
		mcasp5_fsr	1	IO									
		spi4_d1	2	IO									0
		uart9_txd	3	O									
		i2c5_scl	4	IO									1
		vout2_d21	6	O									
		vin2a_d21 vin1a_d21	8	I									
		vin1a_d10	9	I									0
		Driver off	15	I									

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	BALL RESET REL. MUXMODE [8]	I/O VOLTAGE VALUE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/DOWN TYPE [13]	DSIS [14]
U4	mdio_d	mdio_d	0	IO	PU	PU	15	1.8/3.3	vddshv9	Yes	Dual Voltage LVCMOS	PU/PD	1
		uart3_ctsn	1	I									1
		mii0_txer	3	O									0
		vin2a_d0	4	I									0
		vin1b_d0	5	I									0
		gpio5_16	14	IO									
		Driver off	15	I									
V1	mdio_mclk	mdio_mclk	0	O	PU	PU	15	1.8/3.3	vddshv9	Yes	Dual Voltage LVCMOS	PU/PD	1
		uart3_rtsn	1	O									
		mii0_col	3	I									0
		vin2a_clk0	4	I									
		vin1b_clk1	5	I									0
		gpio5_15	14	IO									
		Driver off	15	I									
W6	mmc1_clk	mmc1_clk	0	IO	PU	PU	15	1.8/3.3	vddshv8	Yes	SDIO2KV1833	Pux/PDy	1
		gpio6_21	14	IO									
		Driver off	15	I									
Y6	mmc1_cmd	mmc1_cmd	0	IO	PU	PU	15	1.8/3.3	vddshv8	Yes	SDIO2KV1833	Pux/PDy	1
		gpio6_22	14	IO									
		Driver off	15	I									
AA6	mmc1_dat0	mmc1_dat0	0	IO	PU	PU	15	1.8/3.3	vddshv8	Yes	SDIO2KV1833	Pux/PDy	1
		gpio6_23	14	IO									
		Driver off	15	I									
Y4	mmc1_dat1	mmc1_dat1	0	IO	PU	PU	15	1.8/3.3	vddshv8	Yes	SDIO2KV1833	Pux/PDy	1
		gpio6_24	14	IO									
		Driver off	15	I									
AA5	mmc1_dat2	mmc1_dat2	0	IO	PU	PU	15	1.8/3.3	vddshv8	Yes	SDIO2KV1833	Pux/PDy	1
		gpio6_25	14	IO									
		Driver off	15	I									
Y3	mmc1_dat3	mmc1_dat3	0	IO	PU	PU	15	1.8/3.3	vddshv8	Yes	SDIO2KV1833	Pux/PDy	1
		gpio6_26	14	IO									
		Driver off	15	I									
W7	mmc1_sdcd	mmc1_sdcd	0	I	PU	PU	15	1.8/3.3	vddshv8	Yes	Dual Voltage LVCMOS	PU/PD	1
		uart6_rxd	3	I									1
		i2c4_sda	4	IO									1
		gpio6_27	14	IO									
		Driver off	15	I									

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	BALL RESET REL. MUXMODE [8]	I/O VOLTAGE VALUE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/DOWN TYPE [13]	DSIS [14]
Y9	mmc1_sdwp	mmc1_sdwp	0	I	PD	PD	15	1.8/3.3	vddshv8	Yes	Dual Voltage LVCMOS	PU/PD	0
		uart6_txd	3	O									
		i2c4_scl	4	IO									1
		gpio6_28	14	IO									
		Driver off	15	I									
AD4	mmc3_clk	mmc3_clk	0	IO	PU	PU	15	1.8/3.3	vddshv7	Yes	Dual Voltage LVCMOS	PU/PD	1
		usb3_ulpi_d5	3	IO									0
		vin2b_d7	4	I									0
		vin1a_d7	9	I									0
		ehrpwm2_tripzone_input	10	IO									0
		gpio6_29	14	IO									
		Driver off	15	I									
AC4	mmc3_cmd	mmc3_cmd	0	IO	PU	PU	15	1.8/3.3	vddshv7	Yes	Dual Voltage LVCMOS	PU/PD	1
		spi3_sclk	1	IO									0
		usb3_ulpi_d4	3	IO									0
		vin2b_d6	4	I									0
		vin1a_d6	9	I									0
		eCAP2_in_PWM2_out	10	IO									0
		gpio6_30	14	IO									
		Driver off	15	I									
AC7	mmc3_dat0	mmc3_dat0	0	IO	PU	PU	15	1.8/3.3	vddshv7	Yes	Dual Voltage LVCMOS	PU/PD	1
		spi3_d1	1	IO									0
		uart5_rxd	2	I									1
		usb3_ulpi_d3	3	IO									0
		vin2b_d5	4	I									0
		vin1a_d5	9	I									0
		eQEP3A_in	10	I									0
		gpio6_31	14	IO									
		Driver off	15	I									
AC6	mmc3_dat1	mmc3_dat1	0	IO	PU	PU	15	1.8/3.3	vddshv7	Yes	Dual Voltage LVCMOS	PU/PD	1
		spi3_d0	1	IO									0
		uart5_txd	2	O									
		usb3_ulpi_d2	3	IO									0
		vin2b_d4	4	I									0
		vin1a_d4	9	I									0
		eQEP3B_in	10	I									0
		gpio7_0	14	IO									
		Driver off	15	I									

Table 4-2. Ball Characteristics[(1)] (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	BALL RESET REL. MUXMODE [8]	I/O VOLTAGE VALUE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/DOWN TYPE [13]	DSIS [14]
AC9	mmc3_dat2	mmc3_dat2	0	IO	PU	PU	15	1.8/3.3	vddshv7	Yes	Dual Voltage LVCMOS	PU/PD	1
		spi3_cs0	1	IO									1
		uart5_ctsn	2	I									1
		usb3_ulpi_d1	3	IO									0
		vin2b_d3	4	I									0
		vin1a_d3	9	I									0
		eQEP3_index	10	IO									0
		gpio7_1	14	IO									
		Driver off	15	I									
AC3	mmc3_dat3	mmc3_dat3	0	IO	PU	PU	15	1.8/3.3	vddshv7	Yes	Dual Voltage LVCMOS	PU/PD	1
		spi3_cs1	1	IO									1
		uart5_rtsn	2	O									
		usb3_ulpi_d0	3	IO									0
		vin2b_d2	4	I									0
		vin1a_d2	9	I									0
		eQEP3_strobe	10	IO									0
		gpio7_2	14	IO									
		Driver off	15	I									
AC8	mmc3_dat4	mmc3_dat4	0	IO	PU	PU	15	1.8/3.3	vddshv7	Yes	Dual Voltage LVCMOS	PU/PD	1
		spi4_sclk	1	IO									0
		uart10_rxd	2	I									1
		usb3_ulpi_nxt	3	I									0
		vin2b_d1	4	I									0
		vin1a_d1	9	I									0
		ehrpwm3A	10	O									
		gpio1_22	14	IO									
		Driver off	15	I									
AD6	mmc3_dat5	mmc3_dat5	0	IO	PU	PU	15	1.8/3.3	vddshv7	Yes	Dual Voltage LVCMOS	PU/PD	1
		spi4_d1	1	IO									0
		uart10_txd	2	O									
		usb3_ulpi_dir	3	I									0
		vin2b_d0	4	I									0
		vin1a_d0	9	I									0
		ehrpwm3B	10	O									
		gpio1_23	14	IO									
		Driver off	15	I									

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	BALL RESET REL. MUXMODE [8]	I/O VOLTAGE VALUE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/DOWN TYPE [13]	DSIS [14]
AB8	mmc3_dat6	mmc3_dat6	0	IO	PU	PU	15	1.8/3.3	vddshv7	Yes	Dual Voltage LVCMOS	PU/PD	1
		spi4_d0	1	IO									0
		uart10_ctsn	2	I									1
		usb3_ulpi_stp	3	O									
		vin2b_de1	4	I									
		vin1a_hsync0	9	I									0
		ehrpwm3_tripzone_input	10	IO									0
		gpio1_24	14	IO									
		Driver off	15	I									
AB5	mmc3_dat7	mmc3_dat7	0	IO	PU	PU	15	1.8/3.3	vddshv7	Yes	Dual Voltage LVCMOS	PU/PD	1
		spi4_cs0	1	IO									1
		uart10_rtsn	2	O									
		usb3_ulpi_clk	3	I									0
		vin2b_clk1	4	I									
		vin1a_vsync0	9	I									0
		eCAP3_in_PWM3_out	10	IO									0
		gpio1_25	14	IO									
		Driver off	15	I									
D21	nmin_dsp	nmin_dsp	0	I	PD	PD		1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	
Y11	on_off	on_off	0	O	PU	drive 1 (OFF)		1.8/3.3	vddshv5	Yes	BC1833IHHV	PU/PD	
AG13	pcie_rxn0	pcie_rxn0	0	I	OFF	OFF		1.8	vdda_pcie0		SERDES		
AH13	pcie_rxp0	pcie_rxp0	0	I	OFF	OFF		1.8	vdda_pcie0		SERDES		
AG14	pcie_txn0	pcie_txn0	0	O				1.8	vdda_pcie0		SERDES		
AH14	pcie_txp0	pcie_txp0	0	O				1.8	vdda_pcie0		SERDES		
F22	porz	porz	0	I				1.8/3.3	vddshv3	Yes	IHHV1833	PU/PD	
E23	resetn	resetn	0	I	PU	PU		1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	
U5	rgmii0_rxc	rgmii0_rxc	0	I	PD	PD	15	1.8/3.3	vddshv9	Yes	Dual Voltage LVCMOS	PU/PD	0
		rmii1_txen	2	O									
		mii0_txclk	3	I									0
		vin2a_d5	4	I									0
		vin1b_d5	5	I									0
		usb3_ulpi_d2	6	IO									0
		gpio5_26	14	IO									
		Driver off	15	I									

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	BALL RESET REL. MUXMODE [8]	I/O VOLTAGE VALUE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/DOWN TYPE [13]	DSIS [14]
V5	rgmii0_rxctl	rgmii0_rxctl	0	I	PD	PD	15	1.8/3.3	vddshv9	Yes	Dual Voltage LVCMOS	PU/PD	0
		rmii1_txd1	2	O									
		mii0_txd3	3	O									
		vin2a_d6	4	I									0
		vin1b_d6	5	I									0
		usb3_ulpi_d3	6	IO									0
		gpio5_27	14	IO									
		Driver off	15	I									
W2	rgmii0_rxd0	rgmii0_rxd0	0	I	PD	PD	15	1.8/3.3	vddshv9	Yes	Dual Voltage LVCMOS	PU/PD	0
		rmii0_txd0	1	O									
		mii0_txd0	3	O									
		vin2a_fld0	4	I									
		vin1b_fld1	5	I									0
		usb3_ulpi_d7	6	IO									0
		gpio5_31	14	IO									
		Driver off	15	I									
Y2	rgmii0_rxd1	rgmii0_rxd1	0	I	PD	PD	15	1.8/3.3	vddshv9	Yes	Dual Voltage LVCMOS	PU/PD	0
		rmii0_txd1	1	O									
		mii0_txd1	3	O									
		vin2a_d9	4	I									0
		usb3_ulpi_d6	6	IO									0
		gpio5_30	14	IO									
		Driver off	15	I									
V3	rgmii0_rxd2	rgmii0_rxd2	0	I	PD	PD	15	1.8/3.3	vddshv9	Yes	Dual Voltage LVCMOS	PU/PD	0
		rmii0_txen	1	O									
		mii0_txen	3	O									
		vin2a_d8	4	I									0
		usb3_ulpi_d5	6	IO									0
		gpio5_29	14	IO									
		Driver off	15	I									
V4	rgmii0_rxd3	rgmii0_rxd3	0	I	PD	PD	15	1.8/3.3	vddshv9	Yes	Dual Voltage LVCMOS	PU/PD	0
		rmii1_txd0	2	O									
		mii0_txd2	3	O									
		vin2a_d7	4	I									0
		vin1b_d7	5	I									0
		usb3_ulpi_d4	6	IO									0
		gpio5_28	14	IO									
		Driver off	15	I									

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	BALL RESET REL. MUXMODE [8]	I/O VOLTAGE VALUE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/DOWN TYPE [13]	DSIS [14]
W9	rgmii0_txc	rgmii0_txc	0	O	PD	PD	15	1.8/3.3	vddshv9	Yes	Dual Voltage LVCMOS	PU/PD	
		uart3_ctsn	1	I									1
		rmii1_rxd1	2	I									0
		mii0_rxd3	3	I									0
		vin2a_d3	4	I									0
		vin1b_d3	5	I									0
		usb3_ulpi_clk	6	I									0
		spi3_d0	7	IO									0
		spi4_cs2	8	IO									1
		gpio5_20	14	IO									
		Driver off	15	I									
V9	rgmii0_txctl	rgmii0_txctl	0	O	PD	PD	15	1.8/3.3	vddshv9	Yes	Dual Voltage LVCMOS	PU/PD	
		uart3_rtsn	1	O									
		rmii1_rxd0	2	I									0
		mii0_rxd2	3	I									0
		vin2a_d4	4	I									0
		vin1b_d4	5	I									0
		usb3_ulpi_stp	6	O									
		spi3_cs0	7	IO									1
		spi4_cs3	8	IO									1
		gpio5_21	14	IO									
		Driver off	15	I									
U6	rgmii0_txd0	rgmii0_txd0	0	O	PD	PD	15	1.8/3.3	vddshv9	Yes	Dual Voltage LVCMOS	PU/PD	
		rmii0_rxd0	1	I									0
		mii0_rxd0	3	I									0
		vin2a_d10	4	I									0
		usb3_ulpi_d1	6	IO									0
		spi4_cs0	7	IO									1
		uart4_rtsn	8	O									
		gpio5_25	14	IO									
		Driver off	15	I									

Table 4-2. Ball Characteristics[(1)] (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	BALL RESET REL. MUXMODE [8]	I/O VOLTAGE VALUE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/DOWN TYPE [13]	DSIS [14]
V6	rgmii0_txd1	rgmii0_txd1	0	O	PD	PD	15	1.8/3.3	vddshv9	Yes	Dual Voltage LVCMOS	PU/PD	
		rmii0_rxd1	1	I									0
		mii0_rxd1	3	I									0
		vin2a_vsync0	4	I									
		vin1b_vsync1	5	I									0
		usb3_ulpi_d0	6	IO									0
		spi4_d0	7	IO									0
		uart4_ctsn	8	IO									1
		gpio5_24	14	IO									
		Driver off	15	I									
U7	rgmii0_txd2	rgmii0_txd2	0	O	PD	PD	15	1.8/3.3	vddshv9	Yes	Dual Voltage LVCMOS	PU/PD	
		rmii0_rxer	1	I									0
		mii0_rxer	3	I									0
		vin2a_hsync0	4	I									
		vin1b_hsync1	5	I									0
		usb3_ulpi_nxt	6	I									0
		spi4_d1	7	IO									0
		uart4_txd	8	O									
		gpio5_23	14	IO									
		Driver off	15	I									
V7	rgmii0_txd3	rgmii0_txd3	0	O	PD	PD	15	1.8/3.3	vddshv9	Yes	Dual Voltage LVCMOS	PU/PD	
		rmii0_crs	1	I									0
		mii0_crs	3	I									0
		vin2a_de0	4	I									
		vin1b_de1	5	I									0
		usb3_ulpi_dir	6	I									0
		spi4_sclk	7	IO									0
		uart4_rxd	8	I									1
		gpio5_22	14	IO									
		Driver off	15	I									
U3	RMII_MHZ_50_CLK	RMII_MHZ_50_CLK	0	IO	PD	PD	15	1.8/3.3	vddshv9	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin2a_d11	4	I									0
		gpio5_17	14	IO									
		Driver off	15	I									
F23	rstoutn	rstoutn	0	O	PD	PD		1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	
E18	rtck	rtck	0	O	PU	OFF	0	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	
		gpio8_29	14	IO									

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	BALL RESET REL. MUXMODE [8]	I/O VOLTAGE VALUE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/DOWN TYPE [13]	DSIS [14]
AF14	rtc_iso	rtc_iso	0	I				1.8/3.3	vddshv5	Yes	IHHV1833	PU/PD	
AE14	rtc_osc_xi_clkin32	rtc_osc_xi_clkin32	0	I				1.8	vdda_rtc	No	LVCMOS OSC		
AD14	rtc_osc_xo	rtc_osc_xo	0	O				1.8	vdda_rtc	No	LVCMOS OSC		
AB17	rtc_porz	rtc_porz	0	I				1.8/3.3	vddshv5	Yes	IHHV1833	PU/PD	
AH9	sata1_rxn0	sata1_rxn0	0	I	OFF	OFF		1.8	vdda_sata		SATAPHY		
AG9	sata1_rxp0	sata1_rxp0	0	I	OFF	OFF		1.8	vdda_sata		SATAPHY		
AG10	sata1_txn0	sata1_txn0	0	O				1.8	vdda_sata		SATAPHY		
AH10	sata1_txp0	sata1_txp0	0	O				1.8	vdda_sata		SATAPHY		
A24	spi1_cs0	spi1_cs0	0	IO	PU	PU	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	1
		gpio7_10	14	IO									
		Driver off	15	I									
A22	spi1_cs1	spi1_cs1	0	IO	PU	PU	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	1
		sata1_led	2	O									
		spi2_cs1	3	IO									1
		gpio7_11	14	IO									
		Driver off	15	I									
B21	spi1_cs2	spi1_cs2	0	IO	PU	PU	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	1
		uart4_rxd	1	I									1
		mmc3_sdcd	2	I									1
		spi2_cs2	3	IO									1
		dcan2_tx	4	IO									1
		mdio_mclk	5	O									1
		hdmi1_hpd	6	IO									
		gpio7_12	14	IO									
		Driver off	15	I									
B20	spi1_cs3	spi1_cs3	0	IO	PU	PU	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	1
		uart4_txd	1	O									
		mmc3_sdwp	2	I									0
		spi2_cs3	3	IO									1
		dcan2_rx	4	IO									1
		mdio_d	5	IO									1
		hdmi1_cec	6	IO									
		gpio7_13	14	IO									
		Driver off	15	I									

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	BALL RESET REL. MUXMODE [8]	I/O VOLTAGE VALUE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/DOWN TYPE [13]	DSIS [14]
B25	spi1_d0	spi1_d0	0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		gpio7_9	14	IO									
		Driver off	15	I									
F16	spi1_d1	spi1_d1	0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		gpio7_8	14	IO									
		Driver off	15	I									
A25	spi1_sclk	spi1_sclk	0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		gpio7_7	14	IO									
		Driver off	15	I									
B24	spi2_cs0	spi2_cs0	0	IO	PU	PU	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	1
		uart3_rtsn	1	O									
		uart5_txd	2	O									
		gpio7_17	14	IO									
		Driver off	15	I									
G17	spi2_d0	spi2_d0	0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		uart3_ctsn	1	I									1
		uart5_rxd	2	I									1
		gpio7_16	14	IO									
		Driver off	15	I									
B22	spi2_d1	spi2_d1	0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		uart3_txd	1	O									
		gpio7_15	14	IO									
		Driver off	15	I									
A26	spi2_sclk	spi2_sclk	0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		uart3_rxd	1	I									1
		gpio7_14	14	IO									
		Driver off	15	I									
E20	tclk	tclk	0	I	PU	PU	0	1.8/3.3	vddshv3	Yes	IQ1833	PU/PD	
D23	tdi	tdi	0	I	PU	PU	0	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	
		gpio8_27	14	I									
F19	tdo	tdo	0	O	PU	PU	0	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	
		gpio8_28	14	IO									
F18	tms	tms	0	I	PU	PU	0	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	
D20	trstn	trstn	0	I	PD	PD		1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	BALL RESET REL. MUXMODE [8]	I/O VOLTAGE VALUE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/DOWN TYPE [13]	DSIS [14]
E25	uart1_ctsn	uart1_ctsn	0	I	PU	PU	15	1.8/3.3	vddshv4	Yes	Dual Voltage LVCMOS	PU/PD	1
		uart9_rxd	2	I									1
		mmc4_clk	3	IO									1
		gpio7_24	14	IO									
		Driver off	15	I									
C27	uart1_rtsn	uart1_rtsn	0	O	PU	PU	15	1.8/3.3	vddshv4	Yes	Dual Voltage LVCMOS	PU/PD	
		uart9_txd	2	O									
		mmc4_cmd	3	IO									1
		gpio7_25	14	IO									
		Driver off	15	I									
B27	uart1_rxd	uart1_rxd	0	I	PU	PU	15	1.8/3.3	vddshv4	Yes	Dual Voltage LVCMOS	PU/PD	1
		mmc4_sdcd	3	I									1
		gpio7_22	14	IO									
		Driver off	15	I									
C26	uart1_txd	uart1_txd	0	O	PU	PU	15	1.8/3.3	vddshv4	Yes	Dual Voltage LVCMOS	PU/PD	
		mmc4_sdwp	3	I									0
		gpio7_23	14	IO									
		Driver off	15	I									
D27	uart2_ctsn	uart2_ctsn	0	I	PU	PU	15	1.8/3.3	vddshv4	Yes	Dual Voltage LVCMOS	PU/PD	1
		uart3_rxd	2	I									1
		mmc4_dat2	3	IO									1
		uart10_rxd	4	I									1
		uart1_dtrn	5	O									
		gpio1_16	14	IO									
		Driver off	15	I									
C28	uart2_rtsn	uart2_rtsn	0	O	PU	PU	15	1.8/3.3	vddshv4	Yes	Dual Voltage LVCMOS	PU/PD	
		uart3_txd	1	O									
		uart3_irtx	2	O									
		mmc4_dat3	3	IO									1
		uart10_txd	4	O									
		uart1_rin	5	I									1
		gpio1_17	14	IO									
		Driver off	15	I									

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	BALL RESET REL. MUXMODE [8]	I/O VOLTAGE VALUE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/DOWN TYPE [13]	DSIS [14]
D28	uart2_rxd	uart3_ctsn	1	I	PU	PU	15	1.8/3.3	vddshv4	Yes	Dual Voltage LVCMOS	PU/PD	1
		uart3_rctx	2	O									
		mmc4_dat0	3	IO									1
		uart2_rxd	4	I									1
		uart1_dcdn	5	I									1
		gpio7_26	14	IO									
		Driver off	15	I									
D26	uart2_txd	uart2_txd	0	O	PU	PU	15	1.8/3.3	vddshv4	Yes	Dual Voltage LVCMOS	PU/PD	
		uart3_rtsn	1	O									
		uart3_sd	2	O									
		mmc4_dat1	3	IO									1
		uart2_txd	4	O									
		uart1_dsrn	5	I									0
		gpio7_27	14	IO									
		Driver off	15	I									
V2	uart3_rxd	uart3_rxd	0	I	PD	PD	15	1.8/3.3	vddshv9	Yes	Dual Voltage LVCMOS	PU/PD	1
		rmii1_crs	2	I									0
		mii0_rxdv	3	I									0
		vin2a_d1	4	I									0
		vin1b_d1	5	I									0
		spi3_sclk	7	IO									0
		gpio5_18	14	IO									
		Driver off	15	I									
Y1	uart3_txd	uart3_txd	0	O	PD	PD	15	1.8/3.3	vddshv9	Yes	Dual Voltage LVCMOS	PU/PD	
		rmii1_rxer	2	I									0
		mii0_rxclk	3	I									0
		vin2a_d2	4	I									0
		vin1b_d2	5	I									0
		spi3_d1	7	IO									0
		spi4_cs1	8	IO									1
		gpio5_19	14	IO									
		Driver off	15	I									
AC12	usb1_dm	usb1_dm	0	IO	OFF	OFF		3.3	vdda33v_usb1		USBPHY		
AD12	usb1_dp	usb1_dp	0	IO	OFF	OFF		3.3	vdda33v_usb1		USBPHY		

Table 4-2. Ball Characteristics[(1)] (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	BALL RESET REL. MUXMODE [8]	I/O VOLTAGE VALUE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/DOWN TYPE [13]	DSIS [14]
AB10	usb1_drvvbus	usb1_drvvbus	0	O	PD	PD	15	1.8/3.3	vddshv6	Yes	Dual Voltage LVCMOS	PU/PD	
		timer16	7	IO									
		gpio6_12	14	IO									
		Driver off	15	I									
AF11	usb2_dm	usb2_dm	0	IO				3.3	vdda33v_usb2	No	USBPHY		
AE11	usb2_dp	usb2_dp	0	IO				3.3	vdda33v_usb2	No	USBPHY		
AC10	usb2_drvvbus	usb2_drvvbus	0	O	PD	PD	15	1.8/3.3	vddshv6	Yes	Dual Voltage LVCMOS	PU/PD	
		timer15	7	IO									
		gpio6_13	14	IO									
		Driver off	15	I									
AF12	usb_rxn0	usb_rxn0	0	I	OFF	OFF		1.8	vdda_usb1		SERDES		
		pcie_rxn1	1	I									
AE12	usb_rxp0	usb_rxp0	0	I	OFF	OFF		1.8	vdda_usb1		SERDES		
		pcie_rxp1	1	I									
AC11	usb_txn0	usb_txn0	0	O				1.8	vdda_usb1		SERDES		
		pcie_txn1	1	O									
AD11	usb_txp0	usb_txp0	0	O				1.8	vdda_usb1		SERDES		
		pcie_txp1	1	O									
H13, H14, J17, J18, L7, L8, N10, N13, P11, P12, P13, R11, R16, R19, T13, T16, T19, U13, U16, U8, U9, V16, V8	vdd	vdd		PWR									
K14	vpp	vpp[(10)]		PWR									
AA12	vdda33v_usb1	vdda33v_usb1		PWR									
Y12	vdda33v_usb2	vdda33v_usb2		PWR									
P14	vdda_core_gmac	vdda_core_gmac		PWR									
W12	vdda_csi	vdda_csi		PWR									
R17	vdda_ddr	vdda_ddr		PWR									
N11	vdda_debug	vdda_debug		PWR									
N12	vdda_dsp_iva	vdda_dsp_iva		PWR									
R14	vdda_gpu	vdda_gpu		PWR									
Y17	vdda_hdmi	vdda_hdmi		PWR									
N16	vdda_mpu_abe	vdda_mpu_abe		PWR									
AD16, AE16	vdda_osc	vdda_osc		PWR									
AA17	vdda_pcie	vdda_pcie		PWR									
AA16	vdda_pcie0	vdda_pcie0		PWR									

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	BALL RESET REL. MUXMODE [8]	I/O VOLTAGE VALUE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/DOWN TYPE [13]	DSIS [14]
M14	vdda_per	vdda_per		PWR									
P15	vdda_pll_spare	vdda_pll_spare		PWR									
AB13	vdda_rtc	vdda_rtc		PWR									
V13	vdda_sata	vdda_sata		PWR									
AA13	vdda_usb1	vdda_usb1		PWR									
AB12	vdda_usb2	vdda_usb2		PWR									
W14	vdda_usb3	vdda_usb3		PWR									
P16	vdda_video	vdda_video		PWR									
G18, H17, M8, M9, N8, P8, R8, T8, V21, V22, W17, W18	vdds18v	vdds18v		PWR									
AA18, AA19, N21, P20, P21, W21, Y21	vdds18v_ddr1	vdds18v_ddr1		PWR									
E3, E5, G4, G5, H8, H9	vddshv1	vddshv1		PWR									
B6, D10, E10, H10, H11	vddshv2	vddshv2		PWR									
B23, D16, D22, E16, E22, G15, H15, H16, H18, H19	vddshv3	vddshv3		PWR									
C24	vddshv4	vddshv4		PWR									
V12	vddshv5	vddshv5		PWR									
AD5, AD7, AE7, AF5	vddshv6	vddshv6		PWR									
AB6, AB7	vddshv7	vddshv7		PWR									
W8, Y8	vddshv8	vddshv8		PWR									
U10, W4, W5	vddshv9	vddshv9		PWR									
N4, N5, P10, R10, R7, T4, T5	vddshv10	vddshv10		PWR									
J8, K8	vddshv11	vddshv11		PWR									
AA21, AA22, AB21, AB22, AB24, AB25, AC22, AD26, AG20, AG28, AH27, T24, T25, W16, W27	vdds_ddr1	vdds_ddr1		PWR									
AA7, Y7	vdds_mlbp	vdds_mlbp		PWR									
K10, K11, L10, L11, M10, M11	vdd_dsp	vdd_dsp		PWR									
U11, U12, V10, V11, V14, W10, W11, W13	vdd_gpu	vdd_gpu		PWR									

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	BALL RESET REL. MUXMODE [8]	I/O VOLTAGE VALUE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/DOWN TYPE [13]	DSIS [14]
J13, K12, K13, L12, M12, M13	vdd_iva	vdd_iva		PWR									
K17, K18, L15, L16, L17, L18, L19, M15, M16, M17, M18, N17, N18, P17, P18, R18	vdd_mpu	vdd_mpu		PWR									
AB15	vdd_rtc	vdd_rtc		PWR									
E1	vin2a_clk0	vin2a_clk0	0	I	PD	PD	15	1.8/3.3	vddshv1	Yes	Dual Voltage LVCMOS	PU/PD	
		vout2_fld	4	O									
		emu5	5	O									
		eQEP1A_in	10	I									0
		gpio3_28 gpmc_a27 gpmc_a17	14	IO									
		Driver off	15	I									
F2	vin2a_d0	vin2a_d0	0	I	PD	PD	15	1.8/3.3	vddshv1	Yes	Dual Voltage LVCMOS	PU/PD	0
		vout2_d23	4	O									
		emu10	5	O									
		uart9_ctsn	7	I									1
		spi4_d0	8	IO									0
		ehrpwm1B	10	O									
		gpio4_1	14	IO									
		Driver off	15	I									
F3	vin2a_d1	vin2a_d1	0	I	PD	PD	15	1.8/3.3	vddshv1	Yes	Dual Voltage LVCMOS	PU/PD	0
		vout2_d22	4	O									
		emu11	5	O									
		uart9_rtsn	7	O									
		spi4_cs0	8	IO									1
		ehrpwm1_tripzone_input	10	IO									0
		gpio4_2	14	IO									
		Driver off	15	I									
D1	vin2a_d2	vin2a_d2	0	I	PD	PD	15	1.8/3.3	vddshv1	Yes	Dual Voltage LVCMOS	PU/PD	0
		vout2_d21	4	O									
		emu12	5	O									
		uart10_rxd	8	I									1
		eCAP1_in_PWM1_out	10	IO									0
		gpio4_3	14	IO									
		Driver off	15	I									

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	BALL RESET REL. MUXMODE [8]	I/O VOLTAGE VALUE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/DOWN TYPE [13]	DSIS [14]
E2	vin2a_d3	vin2a_d3	0	I	PD	PD	15	1.8/3.3	vddshv1	Yes	Dual Voltage LVCMOS	PU/PD	0
		vout2_d20	4	O									
		emu13	5	O									
		uart10_txd	8	O									
		ehrpwm1_synci	10	I									0
		gpio4_4	14	IO									
		Driver off	15	I									
D2	vin2a_d4	vin2a_d4	0	I	PD	PD	15	1.8/3.3	vddshv1	Yes	Dual Voltage LVCMOS	PU/PD	0
		vout2_d19	4	O									
		emu14	5	O									
		uart10_ctsn	8	I									1
		ehrpwm1_synco	10	O									
		gpio4_5	14	IO									
		Driver off	15	I									
F4	vin2a_d5	vin2a_d5	0	I	PD	PD	15	1.8/3.3	vddshv1	Yes	Dual Voltage LVCMOS	PU/PD	0
		vout2_d18	4	O									
		emu15	5	O									
		uart10_rtsn	8	O									
		eQEP2A_in	10	I									0
		gpio4_6	14	IO									
		Driver off	15	I									
C1	vin2a_d6	vin2a_d6	0	I	PD	PD	15	1.8/3.3	vddshv1	Yes	Dual Voltage LVCMOS	PU/PD	0
		vout2_d17	4	O									
		emu16	5	O									
		mii1_rxd1	8	I									0
		eQEP2B_in	10	I									0
		gpio4_7	14	IO									
		Driver off	15	I									
E4	vin2a_d7	vin2a_d7	0	I	PD	PD	15	1.8/3.3	vddshv1	Yes	Dual Voltage LVCMOS	PU/PD	0
		vout2_d16	4	O									
		emu17	5	O									
		mii1_rxd2	8	I									0
		eQEP2_index	10	IO									0
		gpio4_8	14	IO									
		Driver off	15	I									

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	BALL RESET REL. MUXMODE [8]	I/O VOLTAGE VALUE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/DOWN TYPE [13]	DSIS [14]
F5	vin2a_d8	vin2a_d8	0	I	PD	PD	15	1.8/3.3	vddshv1	Yes	Dual Voltage LVCMOS	PU/PD	0
		vout2_d15	4	O									
		emu18	5	O									
		mii1_rxd3	8	I									0
		eQEP2_strobe	10	IO									0
		gpio4_9 gpmc_a26	14	IO									
		Driver off	15	I									
E6	vin2a_d9	vin2a_d9	0	I	PD	PD	15	1.8/3.3	vddshv1	Yes	Dual Voltage LVCMOS	PU/PD	0
		vout2_d14	4	O									
		emu19	5	O									
		mii1_rxd0	8	I									0
		ehrpwm2A	10	O									
		gpio4_10 gpmc_a25	14	IO									
		Driver off	15	I									
D3	vin2a_d10	vin2a_d10	0	I	PD	PD	15	1.8/3.3	vddshv1	Yes	Dual Voltage LVCMOS	PU/PD	0
		mdio_mclk	3	O									1
		vout2_d13	4	O									
		ehrpwm2B	10	O									
		gpio4_11 gpmc_a24	14	IO									
		Driver off	15	I									
F6	vin2a_d11	vin2a_d11	0	I	PD	PD	15	1.8/3.3	vddshv1	Yes	Dual Voltage LVCMOS	PU/PD	0
		mdio_d	3	IO									1
		vout2_d12	4	O									
		ehrpwm2_tripzone_input	10	IO									0
		gpio4_12 gpmc_a23	14	IO									
		Driver off	15	I									
D5	vin2a_d12	vin2a_d12	0	I	PD	PD	15	1.8/3.3	vddshv1	Yes	Dual Voltage LVCMOS	PU/PD	0
		rgmii1_txc	3	O									
		vout2_d11	4	O									
		mii1_rxclk	8	I									0
		eCAP2_in_PWM2_out	10	IO									0
		gpio4_13	14	IO									
		Driver off	15	I									

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	BALL RESET REL. MUXMODE [8]	I/O VOLTAGE VALUE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/DOWN TYPE [13]	DSIS [14]
C2	vin2a_d13	vin2a_d13	0	I	PD	PD	15	1.8/3.3	vddshv1	Yes	Dual Voltage LVCMOS	PU/PD	0
		rgmii1_txctl	3	O									
		vout2_d10	4	O									
		mii1_rxdv	8	I									0
		eQEP3A_in	10	I									0
		gpio4_14	14	IO									
		Driver off	15	I									
C3	vin2a_d14	vin2a_d14	0	I	PD	PD	15	1.8/3.3	vddshv1	Yes	Dual Voltage LVCMOS	PU/PD	0
		rgmii1_txd3	3	O									
		vout2_d9	4	O									
		mii1_txclk	8	I									0
		eQEP3B_in	10	I									0
		gpio4_15	14	IO									
		Driver off	15	I									
C4	vin2a_d15	vin2a_d15	0	I	PD	PD	15	1.8/3.3	vddshv1	Yes	Dual Voltage LVCMOS	PU/PD	0
		rgmii1_txd2	3	O									
		vout2_d8	4	O									
		mii1_txd0	8	O									
		eQEP3_index	10	IO									0
		gpio4_16	14	IO									
		Driver off	15	I									
B2	vin2a_d16	vin2a_d16	0	I	PD	PD	15	1.8/3.3	vddshv1	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin2b_d7	2	I									0
		rgmii1_txd1	3	O									
		vout2_d7	4	O									
		mii1_txd1	8	O									
		eQEP3_strobe	10	IO									0
		gpio4_24	14	IO									
		Driver off	15	I									
D6	vin2a_d17	vin2a_d17	0	I	PD	PD	15	1.8/3.3	vddshv1	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin2b_d6	2	I									0
		rgmii1_txd0	3	O									
		vout2_d6	4	O									
		mii1_txd2	8	O									
		ehrpwm3A	10	O									
		gpio4_25	14	IO									
		Driver off	15	I									

Table 4-2. Ball Characteristics[(1)] (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	BALL RESET REL. MUXMODE [8]	I/O VOLTAGE VALUE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/DOWN TYPE [13]	DSIS [14]
C5	vin2a_d18	vin2a_d18	0	I	PD	PD	15	1.8/3.3	vddshv1	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin2b_d5	2	I									0
		rgmii1_rxc	3	I									0
		vout2_d5	4	O									
		mii1_txd3	8	O									
		ehrpwm3B	10	O									
		gpio4_26	14	IO									
		Driver off	15	I									
A3	vin2a_d19	vin2a_d19	0	I	PD	PD	15	1.8/3.3	vddshv1	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin2b_d4	2	I									0
		rgmii1_rxctl	3	I									0
		vout2_d4	4	O									
		mii1_txer	8	O									0
		ehrpwm3_tripzone_input	10	IO									0
		gpio4_27	14	IO									
		Driver off	15	I									
B3	vin2a_d20	vin2a_d20	0	I	PD	PD	15	1.8/3.3	vddshv1	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin2b_d3	2	I									0
		rgmii1_rxd3	3	I									0
		vout2_d3	4	O									
		mii1_rxer	8	I									0
		eCAP3_in_PWM3_out	10	IO									0
		gpio4_28	14	IO									
		Driver off	15	I									
B4	vin2a_d21	vin2a_d21	0	I	PD	PD	15	1.8/3.3	vddshv1	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin2b_d2	2	I									0
		rgmii1_rxd2	3	I									0
		vout2_d2	4	O									
		mii1_col	8	I									0
		gpio4_29	14	IO									
		Driver off	15	I									
B5	vin2a_d22	vin2a_d22	0	I	PD	PD	15	1.8/3.3	vddshv1	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin2b_d1	2	I									0
		rgmii1_rxd1	3	I									0
		vout2_d1	4	O									
		mii1_crs	8	I									0
		gpio4_30	14	IO									
		Driver off	15	I									

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	BALL RESET REL. MUXMODE [8]	I/O VOLTAGE VALUE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/DOWN TYPE [13]	DSIS [14]
A4	vin2a_d23	vin2a_d23	0	I	PD	PD	15	1.8/3.3	vddshv1	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin2b_d0	2	I									0
		rgmii1_rxd0	3	I									0
		vout2_d0	4	O									
		mii1_txen	8	O									
		gpio4_31	14	IO									
		Driver off	15	I									
G2	vin2a_de0	vin2a_de0	0	I	PD	PD	15	1.8/3.3	vddshv1	Yes	Dual Voltage LVCMOS	PU/PD	
		vin2a_fld0	1	I									
		vin2b_fld1	2	I									
		vin2b_de1	3	I									
		vout2_de	4	O									
		emu6	5	O									
		eQEP1B_in	10	I									0
		gpio3_29	14	IO									
		Driver off	15	I									
H7	vin2a_fld0	vin2a_fld0	0	I	PD	PD	15	1.8/3.3	vddshv1	Yes	Dual Voltage LVCMOS	PU/PD	
		vin2b_clk1	2	I									
		vout2_clk	4	O									
		emu7	5	O									
		eQEP1_index	10	IO									0
		gpio3_30 gpmc_a27 gpmc_a18	14	IO									
		Driver off	15	I									
G1	vin2a_hsync0	vin2a_hsync0	0	I	PD	PD	15	1.8/3.3	vddshv1	Yes	Dual Voltage LVCMOS	PU/PD	
		vin2b_hsync1	3	I									
		vout2_hsync	4	O									
		emu8	5	O									
		uart9_rxd	7	I									1
		spi4_sclk	8	IO									0
		eQEP1_strobe	10	IO									0
		gpio3_31 gpmc_a27	14	IO									
		Driver off	15	I									

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	BALL RESET REL. MUXMODE [8]	I/O VOLTAGE VALUE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/DOWN TYPE [13]	DSIS [14]
G6	vin2a_vsync0	vin2a_vsync0	0	I	PD	PD	15	1.8/3.3	vddshv1	Yes	Dual Voltage LVCMOS	PU/PD	
		vin2b_vsync1	3	I									
		vout2_vsync	4	O									
		emu9	5	O									
		uart9_txd	7	O									
		spi4_d1	8	IO									0
		ehrpwm1A	10	O									
		gpio4_0	14	IO									
		Driver off	15	I									
D11	vout1_clk	vout1_clk	0	O	PD	PD	15	1.8/3.3	vddshv2	Yes	Dual Voltage LVCMOS	PU/PD	
		vin2a_fld0 vin1a_fld0	3	I									
		vin1a_fld0	4	I									0
		spi3_cs0	8	IO									1
		gpio4_19	14	IO									
		Driver off	15	I									
F11	vout1_d0	vout1_d0	0	O	PD	PD	15	1.8/3.3	vddshv2	Yes	Dual Voltage LVCMOS	PU/PD	
		uart5_rxd	2	I									1
		vin2a_d16 vin1a_d16	3	I									
		vin1a_d16	4	I									0
		spi3_cs2	8	IO									1
		gpio8_0	14	IO									
		Driver off	15	I									
G10	vout1_d1	vout1_d1	0	O	PD	PD	15	1.8/3.3	vddshv2	Yes	Dual Voltage LVCMOS	PU/PD	
		uart5_txd	2	O									
		vin2a_d17 vin1a_d17	3	I									
		vin1a_d17	4	I									0
		gpio8_1	14	IO									
		Driver off	15	I									

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	BALL RESET REL. MUXMODE [8]	I/O VOLTAGE VALUE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/DOWN TYPE [13]	DSIS [14]
F10	vout1_d2	vout1_d2	0	O	PD	PD	15	1.8/3.3	vddshv2	Yes	Dual Voltage LVCMOS	PU/PD	
		emu2	2	O									
		vin2a_d18 vin1a_d18	3	I									
		vin1a_d18	4	I									0
		obs0	5	O									
		obs16	6	O									
		obs_irq1	7	O									
		gpio8_2	14	IO									
		Driver off	15	I									
G11	vout1_d3	vout1_d3	0	O	PD	PD	15	1.8/3.3	vddshv2	Yes	Dual Voltage LVCMOS	PU/PD	
		emu5	2	O									
		vin2a_d19 vin1a_d19	3	I									
		vin1a_d19	4	I									0
		obs1	5	O									
		obs17	6	O									
		obs_dmarq1	7	O									
		gpio8_3	14	IO									
		Driver off	15	I									
E9	vout1_d4	vout1_d4	0	O	PD	PD	15	1.8/3.3	vddshv2	Yes	Dual Voltage LVCMOS	PU/PD	
		emu6	2	O									
		vin2a_d20 vin1a_d20	3	I									
		vin1a_d20	4	I									0
		obs2	5	O									
		obs18	6	O									
		gpio8_4	14	IO									
		Driver off	15	I									
F9	vout1_d5	vout1_d5	0	O	PD	PD	15	1.8/3.3	vddshv2	Yes	Dual Voltage LVCMOS	PU/PD	
		emu7	2	O									
		vin2a_d21 vin1a_d21	3	I									
		vin1a_d21	4	I									0
		obs3	5	O									
		obs19	6	O									
		gpio8_5	14	IO									
		Driver off	15	I									

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	BALL RESET REL. MUXMODE [8]	I/O VOLTAGE VALUE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/DOWN TYPE [13]	DSIS [14]
F8	vout1_d6	vout1_d6	0	O	PD	PD	15	1.8/3.3	vddshv2	Yes	Dual Voltage LVCMOS	PU/PD	
		emu8	2	O									
		vin2a_d22 vin1a_d22	3	I									
		vin1a_d22	4	I									0
		obs4	5	O									
		obs20	6	O									
		gpio8_6	14	IO									
		Driver off	15	I									
E7	vout1_d7	vout1_d7	0	O	PD	PD	15	1.8/3.3	vddshv2	Yes	Dual Voltage LVCMOS	PU/PD	
		emu9	2	O									
		vin2a_d23 vin1a_d23	3	I									
		vin1a_d23	4	I									0
		gpio8_7	14	IO									
		Driver off	15	I									
E8	vout1_d8	vout1_d8	0	O	PD	PD	15	1.8/3.3	vddshv2	Yes	Dual Voltage LVCMOS	PU/PD	
		uart6_rxd	2	I									1
		vin2a_d8 vin1a_d8	3	I									
		vin1a_d8	4	I									0
		gpio8_8	14	IO									
		Driver off	15	I									
D9	vout1_d9	vout1_d9	0	O	PD	PD	15	1.8/3.3	vddshv2	Yes	Dual Voltage LVCMOS	PU/PD	
		uart6_txd	2	O									
		vin2a_d9 vin1a_d9	3	I									
		vin1a_d9	4	I									0
		gpio8_9	14	IO									
		Driver off	15	I									
D7	vout1_d10	vout1_d10	0	O	PD	PD	15	1.8/3.3	vddshv2	Yes	Dual Voltage LVCMOS	PU/PD	
		emu3	2	O									
		vin2a_d10 vin1a_d10	3	I									
		vin1a_d10	4	I									0
		obs5	5	O									
		obs21	6	O									
		obs_irq2	7	O									
		gpio8_10	14	IO									
		Driver off	15	I									

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	BALL RESET REL. MUXMODE [8]	I/O VOLTAGE VALUE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/DOWN TYPE [13]	DSIS [14]
D8	vout1_d11	vout1_d11	0	O	PD	PD	15	1.8/3.3	vddshv2	Yes	Dual Voltage LVCMOS	PU/PD	
		emu10	2	O									
		vin2a_d11 vin1a_d11	3	I									
		vin1a_d11	4	I									0
		obs6	5	O									
		obs22	6	O									
		obs_dmarq2	7	O									
		gpio8_11	14	IO									
		Driver off	15	I									
A5	vout1_d12	vout1_d12	0	O	PD	PD	15	1.8/3.3	vddshv2	Yes	Dual Voltage LVCMOS	PU/PD	
		emu11	2	O									
		vin2a_d12 vin1a_d12	3	I									
		vin1a_d12	4	I									0
		obs7	5	O									
		obs23	6	O									
		gpio8_12	14	IO									
		Driver off	15	I									
C6	vout1_d13	vout1_d13	0	O	PD	PD	15	1.8/3.3	vddshv2	Yes	Dual Voltage LVCMOS	PU/PD	
		emu12	2	O									
		vin2a_d13 vin1a_d13	3	I									
		vin1a_d13	4	I									0
		obs8	5	O									
		obs24	6	O									
		gpio8_13	14	IO									
		Driver off	15	I									
C8	vout1_d14	vout1_d14	0	O	PD	PD	15	1.8/3.3	vddshv2	Yes	Dual Voltage LVCMOS	PU/PD	
		emu13	2	O									
		vin2a_d14 vin1a_d14	3	I									
		vin1a_d14	4	I									0
		obs9	5	O									
		obs25	6	O									
		gpio8_14	14	IO									
		Driver off	15	I									

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	BALL RESET REL. MUXMODE [8]	I/O VOLTAGE VALUE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/DOWN TYPE [13]	DSIS [14]
C7	vout1_d15	vout1_d15	0	O	PD	PD	15	1.8/3.3	vddshv2	Yes	Dual Voltage LVCMOS	PU/PD	
		emu14	2	O									
		vin2a_d15 vin1a_d15	3	I									
		vin1a_d15	4	I									0
		obs10	5	O									
		obs26	6	O									
		gpio8_15	14	IO									
		Driver off	15	I									
B7	vout1_d16	vout1_d16	0	O	PD	PD	15	1.8/3.3	vddshv2	Yes	Dual Voltage LVCMOS	PU/PD	
		uart7_rxd	2	I									1
		vin2a_d0 vin1a_d0	3	I									
		vin1a_d0	4	I									0
		gpio8_16	14	IO									
		Driver off	15	I									
B8	vout1_d17	vout1_d17	0	O	PD	PD	15	1.8/3.3	vddshv2	Yes	Dual Voltage LVCMOS	PU/PD	
		uart7_txd	2	O									
		vin2a_d1 vin1a_d1	3	I									
		vin1a_d1	4	I									0
		gpio8_17	14	IO									
		Driver off	15	I									
A7	vout1_d18	vout1_d18	0	O	PD	PD	15	1.8/3.3	vddshv2	Yes	Dual Voltage LVCMOS	PU/PD	
		emu4	2	O									
		vin2a_d2 vin1a_d2	3	I									
		vin1a_d2	4	I									0
		obs11	5	O									
		obs27	6	O									
		gpio8_18	14	IO									
		Driver off	15	I									

Table 4-2. Ball Characteristics[(1)] (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	BALL RESET REL. MUXMODE [8]	I/O VOLTAGE VALUE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/DOWN TYPE [13]	DSIS [14]
A8	vout1_d19	vout1_d19	0	O	PD	PD	15	1.8/3.3	vddshv2	Yes	Dual Voltage LVCMOS	PU/PD	
		emu15	2	O									
		vin2a_d3 vin1a_d3	3	I									
		vin1a_d3	4	I									0
		obs12	5	O									
		obs28	6	O									
		gpio8_19	14	IO									
		Driver off	15	I									
C9	vout1_d20	vout1_d20	0	O	PD	PD	15	1.8/3.3	vddshv2	Yes	Dual Voltage LVCMOS	PU/PD	
		emu16	2	O									
		vin2a_d4 vin1a_d4	3	I									
		vin1a_d4	4	I									0
		obs13	5	O									
		obs29	6	O									
		gpio8_20	14	IO									
		Driver off	15	I									
A9	vout1_d21	vout1_d21	0	O	PD	PD	15	1.8/3.3	vddshv2	Yes	Dual Voltage LVCMOS	PU/PD	
		emu17	2	O									
		vin2a_d5 vin1a_d5	3	I									
		vin1a_d5	4	I									0
		obs14	5	O									
		obs30	6	O									
		gpio8_21	14	IO									
		Driver off	15	I									
B9	vout1_d22	vout1_d22	0	O	PD	PD	15	1.8/3.3	vddshv2	Yes	Dual Voltage LVCMOS	PU/PD	
		emu18	2	O									
		vin2a_d6 vin1a_d6	3	I									
		vin1a_d6	4	I									0
		obs15	5	O									
		obs31	6	O									
		gpio8_22	14	IO									
		Driver off	15	I									

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	BALL RESET REL. MUXMODE [8]	I/O VOLTAGE VALUE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/DOWN TYPE [13]	DSIS [14]
A10	vout1_d23	vout1_d23	0	O	PD	PD	15	1.8/3.3	vddshv2	Yes	Dual Voltage LVCMOS	PU/PD	
		emu19	2	O									
		vin2a_d7 vin1a_d7	3	I									
		vin1a_d7	4	I									0
		spi3_cs3	8	IO									1
		gpio8_23	14	IO									
		Driver off	15	I									
B10	vout1_de	vout1_de	0	O	PD	PD	15	1.8/3.3	vddshv2	Yes	Dual Voltage LVCMOS	PU/PD	
		vin2a_de0 vin1a_de0	3	I									
		vin1a_de0	4	I									0
		spi3_d1	8	IO									0
		gpio4_20	14	IO									
		Driver off	15	I									
B11	vout1_fld	vout1_fld	0	O	PD	PD	15	1.8/3.3	vddshv2	Yes	Dual Voltage LVCMOS	PU/PD	
		vin2a_clk0 vin1a_clk0	3	I									
		vin1a_clk0	4	I									0
		spi3_cs1	8	IO									1
		gpio4_21	14	IO									
		Driver off	15	I									
C11	vout1_hsync	vout1_hsync	0	O	PD	PD	15	1.8/3.3	vddshv2	Yes	Dual Voltage LVCMOS	PU/PD	
		vin2a_hsync0 vin1a_hsync0	3	I									
		vin1a_hsync0	4	I									0
		spi3_d0	8	IO									0
		gpio4_22	14	IO									
		Driver off	15	I									
E11	vout1_vsync	vout1_vsync	0	O	PD	PD	15	1.8/3.3	vddshv2	Yes	Dual Voltage LVCMOS	PU/PD	
		vin2a_vsync0 vin1a_vsync0	3	I									
		vin1a_vsync0	4	I									0
		spi3_sclk	8	IO									0
		gpio4_23	14	IO									
		Driver off	15	I									

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	BALL RESET REL. MUXMODE [8]	I/O VOLTAGE VALUE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/DOWN TYPE [13]	DSIS [14]
A1, A14, A2, A23, A28, A6, AA14, AA15, AA20, AA8, AA9, AB14, AB20, AD1, AD24, AG1, AH1, AH2, AH20, AH28, B1, D13, D19, E13, E19, F1, F7, G7, G8, G9, H12, J12, J15, J28, K1, K15, K24, K25, K4, K5, L13, L14, M19, N14, N15, N19, N24, N25, P28, R1, R12, R13, R21, T10, T11, T12, T14, T15, T17, T18, T21, U14, U15, U17, U20, U21, V15, V17, W1, W15, W24, W25, W28	vss	vss		GND									
AA10, AH8	vssa_csi	vssa_csi		GND									
AD19, AE19	vssa_hdmi	vssa_hdmi		GND									
AF15	vssa_osc0	vssa_osc0		GND									
AC14	vssa_osc1	vssa_osc1		GND									
AD13, AE13	vssa_pcie	vssa_pcie		GND									
AE10	vssa_sata	vssa_sata		GND									
AA11, AB11	vssa_usb	vssa_usb		GND									
AD10	vssa_usb3	vssa_usb3		GND									
R15	vssa_video	vssa_video		GND									
AD17	Wakeup0	Wakeup0	0	I			15	1.8/3.3	vddshv5	Yes	IHHV1833	PU/PD	
		dcan1_rx	1	I									1
		gpio1_0 sys_nirq2	14	I									
		Driver off	15	I									
AC16	Wakeup3	Wakeup3	0	I			15	1.8/3.3	vddshv5	Yes	IHHV1833	PU/PD	
		sys_nirq1	1	I									
		gpio1_3 dcan2_rx	14	I									
		Driver off	15	I									
AE15	xi_osc0	xi_osc0	0	I				1.8	vdda_osc	No	LVCMOS Analog		
AC15	xi_osc1	xi_osc1	0	I				1.8	vdda_osc	No	LVCMOS Analog		
AD15	xo_osc0	xo_osc0	0	O				1.8	vdda_osc	No	LVCMOS Analog		

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	BALL RESET REL. MUXMODE [8]	I/O VOLTAGE VALUE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/DOWN TYPE [13]	DSIS [14]
AC13	xo_osc1	xo_osc1	0	A				1.8	vdda_osc	No	LVCMOS Analog		
D18	xref_clk0	xref_clk0	0	I	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	
		mcasp2_axr8	1	IO									0
		mcasp1_axr4	2	IO									0
		mcasp1_ahclkx	3	O									
		mcasp5_ahclkx	4	O									
		vin1a_d0	7	I									0
		clkout2	9	O									
		timer13	10	IO									
		gpio6_17	14	IO									
		Driver off	15	I									
E17	xref_clk1	xref_clk1	0	I	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	
		mcasp2_axr9	1	IO									0
		mcasp1_axr5	2	IO									0
		mcasp2_ahclkx	3	O									
		mcasp6_ahclkx	4	O									
		vin1a_clk0	7	I									0
		timer14	10	IO									
		gpio6_18	14	IO									
		Driver off	15	I									
B26	xref_clk2	xref_clk2	0	I	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	
		mcasp2_axr10	1	IO									0
		mcasp1_axr6	2	IO									0
		mcasp3_ahclkx	3	O									
		mcasp7_ahclkx	4	O									
		vout2_clk	6	O									
		vin2a_clk0 vin1a_clk0	8	I									
		timer15	10	IO									
		gpio6_19	14	IO									
		Driver off	15	I									

Table 4-2. Ball Characteristics(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	BALL RESET REL. MUXMODE [8]	I/O VOLTAGE VALUE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/DOWN TYPE [13]	DSIS [14]
C23	xref_clk3	xref_clk3	0	I	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	
		mcasp2_axr11	1	IO									0
		mcasp1_axr7	2	IO									0
		mcasp4_ahclkx	3	O									
		mcasp8_ahclkx	4	O									
		vout2_de	6	O									
		vin2a_de0 vin1a_de0	8	I									
		clkout3	9	O									
		timer16	10	IO									
		gpio6_20	14	IO									
		Driver off	15	I									

(1) N/A stands for Not Applicable.

(2) For more information on recommended operating conditions, see Table 5-4, *Recommended Operating Conditions*.

(3) The pullup or pulldown block strength is equal to: minimum = 50 µA, typical = 100 µA, maximum = 250 µA.

(4) The output impedance settings of this IO cell are programmable; by default, the value is DS[1:0] = 10, this means 40 Ω. For more information on DS[1:0] register configuration, see the device TRM.

(5) IO drive strength for usb1_dp, usb1_dm, usb2_dp and usb2_dm: minimum 18.3 mA, maximum 89 mA (for a power supply vdda33v_usb1 and vdda33v_usb2 = 3.46 V).

(6) Minimum PU = 900 Ω, maximum PU = 3.090 kΩ and minimum PD = 14.25 kΩ, maximum PD = 24.8 kΩ.
For more information, see chapter 7 of the USB2.0 specification, in particular section Signaling / Device Speed Identification.

(7) This function will not be supported on some pin-compatible roadmap devices. Pin compatibility can be maintained in the future by not using these GPIO signals.

(8) In PUx / PDy, x and y = 60 to 200 µA.
The output impedance settings (or drive strengths) of this IO are programmable (34 Ω, 40 Ω, 48 Ω, 60 Ω, 80 Ω) depending on the values of the I[2:0] registers.

(9) The internal pull resistors for balls K7, M7, J5, K6, J4, J6, H4, H5 are permanently disabled when sysboot15 is set to 0 as described in the section Sysboot Configuration of the Device TRM. If internal pull-up/down resistors are desired on these balls then sysboot15 should be set to 1. If gpmc boot mode is used with SYSBOOT15=0 (not recommended) then external pull-downs should be implemented to keep the address bus at logic-1 value during boot since the gpmc ms-address bits are high-z during boot.

(10) This signal is valid only for High-Security devices. For more details, see Section 5.8 *VPP Specification for One-Time Programmable (OTP) eFUSEs*. For General Purpose devices do not connect any signal, test point, or board trace to this signal.

4.3 Multiplexing Characteristics

Table 4-3 describes the device multiplexing (no characteristics are available).

NOTE

This table doesn't take into account subsystem multiplexing signals. Subsystem multiplexing signals are described in Section 4.4, *Signal Descriptions*.

NOTE

For more information, see *Control Module* chapter, *PAD Functional Multiplexing and Configuration* section in the device TRM.

NOTE

Configuring two pins to the same input signal is not supported as it can yield unexpected results. This can be easily prevented with the proper software configuration (Hi-Z mode is not an input signal).

NOTE

When a pad is set into a multiplexing mode which is not defined by pin multiplexing, that pad's behavior is undefined. This should be avoided.

NOTE

In some cases Table 4-3 may present more than one signal per muxmode for the same ball. First signal in the list is the dominant function as selected via CTRL_CORE_PAD_* register.

All other signals are virtual functions that present alternate multiplexing options. This virtual functions are controlled via CTRL_CORE_ALT_SELECT_MUX or CTRL_CORE_VIP_MUX_SELECT register. For more information on how to use these options, see *Pad Configuration Registers* section, *Control Module* chapter in the device TRM.

CAUTION

The I/O timings provided in Section 7, *Timing Requirements and Switching Characteristics* are valid only if signals within a single IOSET are used. The IOSETs are defined in the corresponding tables.

NOTE

Dual rank support is not available on this device, but signal names are retained for consistency with the TDA2xx family of devices.

Table 4-3. Multiplexing Characteristics

ADDRESS	REGISTER NAME	BALL NUMBER	MUXMODE FIELD SETTINGS (CTRL_CORE_PAD_*[3:0])												
			0	1	2	3*	4*	5*	6*	7	8*	9	10	14*	15
		Y23	ddr1_d26												
		Y19	ddr1_d21												

Table 4-3. Multiplexing Characteristics (continued)

ADDRESS	REGISTER NAME	BALL NUMBER	MUXMODE FIELD SETTINGS (CTRL_CORE_PAD_*[3:0])												
			0	1	2	3*	4*	5*	6*	7	8*	9	10	14*	15
		AE15	xi_osc0												
		AH24	ddr1_nck												
		AG15	ljcb_clkp												
		AF24	ddr1_d4												
		V25	ddr1_ecc_d6												
		AB16	ddr1_csn1												
		AG19	hdmi1_data2x												
		AF21	ddr1_a4												
		AG5	csi2_1_dx0												
		W23	ddr1_ecc_d3												
		Y27	ddr1_dqsn3												
		AC24	ddr1_d14												
		AF28	ddr1_d11												
		AA23	ddr1_d24												
		AD18	ddr1_a15												
		AH16	hdmi1_clocky												
		AH5	csi2_1_dy0												
		AC20	ddr1_a2												
		AA24	ddr1_d27												
		W19	ddr1_ecc_d2												
		AG21	ddr1_rst												
		AE28	ddr1_dqsn1												
		AC11	usb_txn0	pcie_txn1											
		AG25	ddr1_dqsn0												
		AC17	ddr1_odt1												
		AG4	csi2_0_dy3												
		W20	ddr1_d17												
		AF14	rtc_iso												
		AA27	ddr1_dqm3												
		AF25	ddr1_d0												
		AF2	csi2_0_dx2												
		AF23	ddr1_d6												
		AG18	hdmi1_data1x												
		AH6	csi2_1_dy1												
		AG10	sata1_txn0												
		AF20	ddr1_rasn												
		V26	ddr1_dqm_ecc												
		V20	ddr1_d16												

Table 4-3. Multiplexing Characteristics (continued)

ADDRESS	REGISTER NAME	BALL NUMBER	MUXMODE FIELD SETTINGS (CTRL_CORE_PAD_*[3:0])												
			0	1	2	3*	4*	5*	6*	7	8*	9	10	14*	15
		AH13	pcie_rxp0												
		AC18	ddr1_casn												
		AG9	sata1_rxp0												
		AH23	ddr1_csn0												
		AE11	usb2_dp												
		Y24	ddr1_d28												
		AH15	ljcb_clkn												
		AD20	ddr1_a0												
		AA25	ddr1_d30												
		AD14	rtc_osc_xo												
		AC25	ddr1_d13												
		AB23	ddr1_dqm1												
		AE1	csi2_0_dx0												
		AH19	hdmi1_data2y												
		AB27	ddr1_d22												
		AG14	pcie_txn0												
		Y28	ddr1_dqs3												
		AB19	ddr1_a3												
		AH10	sata1_txp0												
		AG24	ddr1_ck												
		AE24	ddr1_d5												
		AC15	xi_osc1												
		AC21	ddr1_a12												
		AF12	usb_rxn0	pcie_rxn1											
		AH9	sata1_rxn0												
		AC26	ddr1_dqm2												
		AA28	ddr1_d31												
		AD23	ddr1_dqm0												
		AE27	ddr1_dqs1												
		AF27	ddr1_d9												
		V24	ddr1_ecc_d5												
		AG27	ddr1_d10												
		AF22	ddr1_a8												
		AH21	ddr1_wen												
		AE21	ddr1_a7												
		AC12	usb1_dm												
		Y20	ddr1_d23												
		AC27	ddr1_d20												
		AE23	ddr1_d7												

Table 4-3. Multiplexing Characteristics (continued)

ADDRESS	REGISTER NAME	BALL NUMBER	MUXMODE FIELD SETTINGS (CTRL_CORE_PAD_*[3:0])												
			0	1	2	3*	4*	5*	6*	7	8*	9	10	14*	15
		AG22	ddr1_cke												
		AD27	ddr1_dqs2												
		AH26	ddr1_d3												
		AH14	pcie_txp0												
		AD21	ddr1_a10												
		Y25	ddr1_ecc_d4												
		AE17	ddr1_a14												
		AG7	csi2_1_dy2												
		AH18	hdmi1_data1y												
		AH22	ddr1_a5												
		W22	ddr1_ecc_d0												
		V23	ddr1_ecc_d1												
		AE12	usb_rxp0	pcie_rxp1											
		AE14	rtc_osc_xi_clkin32												
		AF3	csi2_0_dy2												
		AG23	ddr1_a6												
		AG6	csi2_1_dx1												
		AB18	ddr1_ba2												
		AG17	hdmi1_data0x												
		AF26	ddr1_d1												
		AD11	usb_txp0	pcie_txp1											
		V27	ddr1_dqs_ecc												
		AF17	ddr1_ba0												
		AE26	ddr1_d12												
		AC19	ddr1_a1												
		AG13	pcie_rxn0												
		AB28	ddr1_d18												
		Y26	ddr1_ecc_d7												
		AH3	csi2_0_dx4												
		AD22	ddr1_a11												
		AD28	ddr1_dqsn2												
		AD2	csi2_0_dy0												
		AE18	ddr1_ba1												
		AE20	ddr1_odt0												
		AF11	usb2_dm												
		AD15	xo_osc0												
		AH7	csi2_1_dx2												
		AE22	ddr1_a9												

Table 4-3. Multiplexing Characteristics (continued)

ADDRESS	REGISTER NAME	BALL NUMBER	MUXMODE FIELD SETTINGS (CTRL_CORE_PAD_*[3:0])												
			0	1	2	3*	4*	5*	6*	7	8*	9	10	14*	15
		Y18	ddr1_vref0												
		AC13	xo_osc1												
		AD12	usb1_dp												
		Y22	ddr1_d25												
		AH17	hdmi1_data0y												
		AH4	csi2_0_dx3												
		AE2	csi2_0_dy1												
		AG26	ddr1_d2												
		AH25	ddr1_dqs0												
		AF18	ddr1_a13												
		AC28	ddr1_d19												
		AG3	csi2_0_dy4												
		V28	ddr1_dqsn_ecc												
		AC23	ddr1_d8												
		F22	porz												
		AG16	hdmi1_clockx												
		AF1	csi2_0_dx1												
		AA26	ddr1_d29												
		AD25	ddr1_d15												
0x1400	CTRL_CORE_PAD_GPMC_AD0	M6	gpmc_ad0		vin1a_d0	vout3_d0								gpio1_6	sysboot0
0x1404	CTRL_CORE_PAD_GPMC_AD1	M2	gpmc_ad1		vin1a_d1	vout3_d1								gpio1_7	sysboot1
0x1408	CTRL_CORE_PAD_GPMC_AD2	L5	gpmc_ad2		vin1a_d2	vout3_d2								gpio1_8	sysboot2
0x140C	CTRL_CORE_PAD_GPMC_AD3	M1	gpmc_ad3		vin1a_d3	vout3_d3								gpio1_9	sysboot3
0x1410	CTRL_CORE_PAD_GPMC_AD4	L6	gpmc_ad4		vin1a_d4	vout3_d4								gpio1_10	sysboot4
0x1414	CTRL_CORE_PAD_GPMC_AD5	L4	gpmc_ad5		vin1a_d5	vout3_d5								gpio1_11	sysboot5
0x1418	CTRL_CORE_PAD_GPMC_AD6	L3	gpmc_ad6		vin1a_d6	vout3_d6								gpio1_12	sysboot6
0x141C	CTRL_CORE_PAD_GPMC_AD7	L2	gpmc_ad7		vin1a_d7	vout3_d7								gpio1_13	sysboot7
0x1420	CTRL_CORE_PAD_GPMC_AD8	L1	gpmc_ad8		vin1a_d8	vout3_d8								gpio7_18	sysboot8
0x1424	CTRL_CORE_PAD_GPMC_AD9	K2	gpmc_ad9		vin1a_d9	vout3_d9								gpio7_19	sysboot9
0x1428	CTRL_CORE_PAD_GPMC_AD10	J1	gpmc_ad10		vin1a_d10	vout3_d10								gpio7_28	sysboot10

Table 4-3. Multiplexing Characteristics (continued)

ADDRESS	REGISTER NAME	BALL NUMBER	MUXMODE FIELD SETTINGS (CTRL_CORE_PAD_*[3:0])												
			0	1	2	3*	4*	5*	6*	7	8*	9	10	14*	15
0x142C	CTRL_CORE_PAD_ GPMC_AD11	J2	gpmc_ad11		vin1a_d11	vout3_d11								gpio7_29	sysboot11
0x1430	CTRL_CORE_PAD_ GPMC_AD12	H1	gpmc_ad12		vin1a_d12	vout3_d12								gpio1_18	sysboot12
0x1434	CTRL_CORE_PAD_ GPMC_AD13	J3	gpmc_ad13		vin1a_d13	vout3_d13								gpio1_19	sysboot13
0x1438	CTRL_CORE_PAD_ GPMC_AD14	H2	gpmc_ad14		vin1a_d14	vout3_d14								gpio1_20	sysboot14
0x143C	CTRL_CORE_PAD_ GPMC_AD15	H3	gpmc_ad15		vin1a_d15	vout3_d15								gpio1_21	sysboot15
0x1440	CTRL_CORE_PAD_ GPMC_A0	R6	gpmc_a0		vin1a_d16	vout3_d16	vin2a_d0 vin1a_d0		vin1b_d0	i2c4_scl	uart5_rxd			gpio7_3 gpmc_a26 gpmc_a16	Driver off
0x1444	CTRL_CORE_PAD_ GPMC_A1	T9	gpmc_a1		vin1a_d17	vout3_d17	vin2a_d1 vin1a_d1		vin1b_d1	i2c4_sda	uart5_txd			gpio7_4	Driver off
0x1448	CTRL_CORE_PAD_ GPMC_A2	T6	gpmc_a2		vin1a_d18	vout3_d18	vin2a_d2 vin1a_d2		vin1b_d2	uart7_rxd	uart5_ctsn			gpio7_5	Driver off
0x144C	CTRL_CORE_PAD_ GPMC_A3	T7	gpmc_a3	qspi1_cs2	vin1a_d19	vout3_d19	vin2a_d3 vin1a_d3		vin1b_d3	uart7_txd	uart5_rtsn			gpio7_6	Driver off
0x1450	CTRL_CORE_PAD_ GPMC_A4	P6	gpmc_a4	qspi1_cs3	vin1a_d20	vout3_d20	vin2a_d4 vin1a_d4		vin1b_d4	i2c5_scl	uart6_rxd			gpio1_26	Driver off
0x1454	CTRL_CORE_PAD_ GPMC_A5	R9	gpmc_a5		vin1a_d21	vout3_d21	vin2a_d5 vin1a_d5		vin1b_d5	i2c5_sda	uart6_txd			gpio1_27	Driver off
0x1458	CTRL_CORE_PAD_ GPMC_A6	R5	gpmc_a6		vin1a_d22	vout3_d22	vin2a_d6 vin1a_d6		vin1b_d6	uart8_rxd	uart6_ctsn			gpio1_28	Driver off
0x145C	CTRL_CORE_PAD_ GPMC_A7	P5	gpmc_a7		vin1a_d23	vout3_d23	vin2a_d7 vin1a_d7		vin1b_d7	uart8_txd	uart6_rtsn			gpio1_29	Driver off
0x1460	CTRL_CORE_PAD_ GPMC_A8	N7	gpmc_a8		vin1a_hsync0	vout3_hsync			vin1b_hsync1	timer12	spi4_sclk			gpio1_30	Driver off
0x1464	CTRL_CORE_PAD_ GPMC_A9	R4	gpmc_a9		vin1a_vsync0	vout3_vsync			vin1b_vsync1	timer11	spi4_d1			gpio1_31	Driver off
0x1468	CTRL_CORE_PAD_ GPMC_A10	N9	gpmc_a10		vin1a_de0	vout3_de			vin1b_clk1	timer10	spi4_d0			gpio2_0	Driver off
0x146C	CTRL_CORE_PAD_ GPMC_A11	P9	gpmc_a11		vin1a_fld0	vout3_fld	vin2a_fld0 vin1a_fld0		vin1b_de1	timer9	spi4_cs0			gpio2_1	Driver off
0x1470	CTRL_CORE_PAD_ GPMC_A12	P4	gpmc_a12				vin2a_clk0 vin1a_clk0	gpmc_a0	vin1b_fld1	timer8	spi4_cs1	dma_evt1		gpio2_2	Driver off
0x1474	CTRL_CORE_PAD_ GPMC_A13	R3	gpmc_a13	qspi1_rtclk			vin2a_hsync0 vin1a_hsync0			timer7	spi4_cs2	dma_evt2		gpio2_3	Driver off
0x1478	CTRL_CORE_PAD_ GPMC_A14	T2	gpmc_a14	qspi1_d3			vin2a_vsync0 vin1a_vsync0			timer6	spi4_cs3			gpio2_4	Driver off
0x147C	CTRL_CORE_PAD_ GPMC_A15	U2	gpmc_a15	qspi1_d2			vin2a_d8 vin1a_d8			timer5				gpio2_5	Driver off
0x1480	CTRL_CORE_PAD_ GPMC_A16	U1	gpmc_a16	qspi1_d0			vin2a_d9 vin1a_d9							gpio2_6	Driver off
0x1484	CTRL_CORE_PAD_ GPMC_A17	P3	gpmc_a17	qspi1_d1			vin2a_d10 vin1a_d10							gpio2_7	Driver off

Table 4-3. Multiplexing Characteristics (continued)

ADDRESS	REGISTER NAME	BALL NUMBER	MUXMODE FIELD SETTINGS (CTRL_CORE_PAD_*[3:0])												
			0	1	2	3*	4*	5*	6*	7	8*	9	10	14*	15
0x1488	CTRL_CORE_PAD_GPMC_A18	R2	gpmc_a18	qspi1_sclk			vin2a_d11 vin1a_d11							gpio2_8	Driver off
0x148C	CTRL_CORE_PAD_GPMC_A19	K7	gpmc_a19	mmc2_dat4	gpmc_a13		vin2a_d12 vin1a_d12		vin2b_d0 vin1b_d0					gpio2_9	Driver off
0x1490	CTRL_CORE_PAD_GPMC_A20	M7	gpmc_a20	mmc2_dat5	gpmc_a14		vin2a_d13 vin1a_d13		vin2b_d1 vin1b_d1					gpio2_10	Driver off
0x1494	CTRL_CORE_PAD_GPMC_A21	J5	gpmc_a21	mmc2_dat6	gpmc_a15		vin2a_d14 vin1a_d14		vin2b_d2 vin1b_d2					gpio2_11	Driver off
0x1498	CTRL_CORE_PAD_GPMC_A22	K6	gpmc_a22	mmc2_dat7	gpmc_a16		vin2a_d15 vin1a_d15		vin2b_d3 vin1b_d3					gpio2_12	Driver off
0x149C	CTRL_CORE_PAD_GPMC_A23	J7	gpmc_a23	mmc2_clk	gpmc_a17		vin2a_fld0 vin1a_fld0		vin2b_d4 vin1b_d4					gpio2_13	Driver off
0x14A0	CTRL_CORE_PAD_GPMC_A24	J4	gpmc_a24	mmc2_dat0	gpmc_a18				vin2b_d5 vin1b_d5					gpio2_14	Driver off
0x14A4	CTRL_CORE_PAD_GPMC_A25	J6	gpmc_a25	mmc2_dat1	gpmc_a19				vin2b_d6 vin1b_d6					gpio2_15	Driver off
0x14A8	CTRL_CORE_PAD_GPMC_A26	H4	gpmc_a26	mmc2_dat2	gpmc_a20				vin2b_d7 vin1b_d7					gpio2_16	Driver off
0x14AC	CTRL_CORE_PAD_GPMC_A27	H5	gpmc_a27	mmc2_dat3	gpmc_a21				vin2b_hsync1 vin1b_hsync1					gpio2_17	Driver off
0x14B0	CTRL_CORE_PAD_GPMC_CS1	H6	gpmc_cs1	mmc2_cmd	gpmc_a22		vin2a_de0 vin1a_de0		vin2b_vsync1 vin1b_vsync1					gpio2_18	Driver off
0x14B4	CTRL_CORE_PAD_GPMC_CS0	T1	gpmc_cs0											gpio2_19	Driver off
0x14B8	CTRL_CORE_PAD_GPMC_CS2	P2	gpmc_cs2	qspi1_cs0										gpio2_20 gpmc_a23 gpmc_a13	Driver off
0x14BC	CTRL_CORE_PAD_GPMC_CS3	P1	gpmc_cs3	qspi1_cs1	vin1a_clk0	vout3_clk		gpmc_a1						gpio2_21 gpmc_a24 gpmc_a14	Driver off
0x14C0	CTRL_CORE_PAD_GPMC_CLK	P7	gpmc_clk	gpmc_cs7	clkout1	gpmc_wait1	vin2a_hsync0 vin1a_hsync0	vin2a_de0 vin1a_de0	vin2b_clk1 vin1b_clk1	timer4	i2c3_scl	dma_evt1		gpio2_22 gpmc_a20	Driver off
0x14C4	CTRL_CORE_PAD_GPMC_ADVN_ALE	N1	gpmc_advn_ale	gpmc_cs6	clkout2	gpmc_wait1	vin2a_vsync0 vin1a_vsync0	gpmc_a2	gpmc_a23	timer3	i2c3_sda	dma_evt2		gpio2_23 gpmc_a19	Driver off
0x14C8	CTRL_CORE_PAD_GPMC_OEN_REN	M5	gpmc_oen_ren											gpio2_24	Driver off
0x14CC	CTRL_CORE_PAD_GPMC_WEN	M3	gpmc_wen											gpio2_25	Driver off
0x14D0	CTRL_CORE_PAD_GPMC_BEN0	N6	gpmc_ben0	gpmc_cs4					vin2b_de1 vin1b_de1	timer2		dma_evt3		gpio2_26 gpmc_a21	Driver off
0x14D4	CTRL_CORE_PAD_GPMC_BEN1	M4	gpmc_ben1	gpmc_cs5			vin2b_clk1 vin1b_clk1	gpmc_a3	vin2b_fld1 vin1b_fld1	timer1		dma_evt4		gpio2_27 gpmc_a22	Driver off
0x14D8	CTRL_CORE_PAD_GPMC_WAIT0	N2	gpmc_wait0											gpio2_28 gpmc_a25 gpmc_a15	Driver off
0x1554	CTRL_CORE_PAD_VIN2A_CLK0	E1	vin2a_clk0				vout2_fld	emu5					eQEP1A_in	gpio3_28 gpmc_a27 gpmc_a17	Driver off

Table 4-3. Multiplexing Characteristics (continued)

ADDRESS	REGISTER NAME	BALL NUMBER	MUXMODE FIELD SETTINGS (CTRL_CORE_PAD_*[3:0])												
			0	1	2	3*	4*	5*	6*	7	8*	9	10	14*	15
0x1558	CTRL_CORE_PAD_VIN2A_DE0	G2	vin2a_de0	vin2a_fld0	vin2b_fld1	vin2b_de1	vout2_de	emu6					eQEP1B_in	gpio3_29	Driver off
0x155C	CTRL_CORE_PAD_VIN2A_FLD0	H7	vin2a_fld0		vin2b_clk1		vout2_clk	emu7					eQEP1_index	gpio3_30 gpmc_a27 gpmc_a18	Driver off
0x1560	CTRL_CORE_PAD_VIN2A_HSYNC0	G1	vin2a_hsync0			vin2b_hsync1	vout2_hsync	emu8		uart9_rxd	spi4_sclk		eQEP1_strobe	gpio3_31 gpmc_a27	Driver off
0x1564	CTRL_CORE_PAD_VIN2A_VSYNC0	G6	vin2a_vsync0			vin2b_vsync1	vout2_vsync	emu9		uart9_txd	spi4_d1		ehrpwm1A	gpio4_0	Driver off
0x1568	CTRL_CORE_PAD_VIN2A_D0	F2	vin2a_d0				vout2_d23	emu10		uart9_ctsn	spi4_d0		ehrpwm1B	gpio4_1	Driver off
0x156C	CTRL_CORE_PAD_VIN2A_D1	F3	vin2a_d1				vout2_d22	emu11		uart9_rtsn	spi4_cs0		ehrpwm1_tripzone_input	gpio4_2	Driver off
0x1570	CTRL_CORE_PAD_VIN2A_D2	D1	vin2a_d2				vout2_d21	emu12			uart10_rxd		eCAP1_in_PWM1_out	gpio4_3	Driver off
0x1574	CTRL_CORE_PAD_VIN2A_D3	E2	vin2a_d3				vout2_d20	emu13			uart10_txd		ehrpwm1_synci	gpio4_4	Driver off
0x1578	CTRL_CORE_PAD_VIN2A_D4	D2	vin2a_d4				vout2_d19	emu14			uart10_ctsn		ehrpwm1_synco	gpio4_5	Driver off
0x157C	CTRL_CORE_PAD_VIN2A_D5	F4	vin2a_d5				vout2_d18	emu15			uart10_rtsn		eQEP2A_in	gpio4_6	Driver off
0x1580	CTRL_CORE_PAD_VIN2A_D6	C1	vin2a_d6				vout2_d17	emu16			mii1_rxd1		eQEP2B_in	gpio4_7	Driver off
0x1584	CTRL_CORE_PAD_VIN2A_D7	E4	vin2a_d7				vout2_d16	emu17			mii1_rxd2		eQEP2_index	gpio4_8	Driver off
0x1588	CTRL_CORE_PAD_VIN2A_D8	F5	vin2a_d8				vout2_d15	emu18			mii1_rxd3		eQEP2_strobe	gpio4_9 gpmc_a26	Driver off
0x158C	CTRL_CORE_PAD_VIN2A_D9	E6	vin2a_d9				vout2_d14	emu19			mii1_rxd0		ehrpwm2A	gpio4_10 gpmc_a25	Driver off
0x1590	CTRL_CORE_PAD_VIN2A_D10	D3	vin2a_d10			mdio_mclk	vout2_d13						ehrpwm2B	gpio4_11 gpmc_a24	Driver off
0x1594	CTRL_CORE_PAD_VIN2A_D11	F6	vin2a_d11			mdio_d	vout2_d12						ehrpwm2_tripzone_input	gpio4_12 gpmc_a23	Driver off
0x1598	CTRL_CORE_PAD_VIN2A_D12	D5	vin2a_d12			rgmii1_txc	vout2_d11				mii1_rxclk		eCAP2_in_PWM2_out	gpio4_13	Driver off
0x159C	CTRL_CORE_PAD_VIN2A_D13	C2	vin2a_d13			rgmii1_txctl	vout2_d10				mii1_rxdv		eQEP3A_in	gpio4_14	Driver off
0x15A0	CTRL_CORE_PAD_VIN2A_D14	C3	vin2a_d14			rgmii1_txd3	vout2_d9				mii1_txclk		eQEP3B_in	gpio4_15	Driver off
0x15A4	CTRL_CORE_PAD_VIN2A_D15	C4	vin2a_d15			rgmii1_txd2	vout2_d8				mii1_txd0		eQEP3_index	gpio4_16	Driver off
0x15A8	CTRL_CORE_PAD_VIN2A_D16	B2	vin2a_d16		vin2b_d7	rgmii1_txd1	vout2_d7				mii1_txd1		eQEP3_strobe	gpio4_24	Driver off
0x15AC	CTRL_CORE_PAD_VIN2A_D17	D6	vin2a_d17		vin2b_d6	rgmii1_txd0	vout2_d6				mii1_txd2		ehrpwm3A	gpio4_25	Driver off
0x15B0	CTRL_CORE_PAD_VIN2A_D18	C5	vin2a_d18		vin2b_d5	rgmii1_rxc	vout2_d5				mii1_txd3		ehrpwm3B	gpio4_26	Driver off

Table 4-3. Multiplexing Characteristics (continued)

ADDRESS	REGISTER NAME	BALL NUMBER	MUXMODE FIELD SETTINGS (CTRL_CORE_PAD_*[3:0])												
			0	1	2	3*	4*	5*	6*	7	8*	9	10	14*	15
0x15B4	CTRL_CORE_PAD_VIN2A_D19	A3	vin2a_d19		vin2b_d4	rgmii1_rxctl	vout2_d4				mii1_txer		ehrpwm3_tripzone_input	gpio4_27	Driver off
0x15B8	CTRL_CORE_PAD_VIN2A_D20	B3	vin2a_d20		vin2b_d3	rgmii1_rxd3	vout2_d3				mii1_rxer		eCAP3_in_PWM3_out	gpio4_28	Driver off
0x15BC	CTRL_CORE_PAD_VIN2A_D21	B4	vin2a_d21		vin2b_d2	rgmii1_rxd2	vout2_d2				mii1_col			gpio4_29	Driver off
0x15C0	CTRL_CORE_PAD_VIN2A_D22	B5	vin2a_d22		vin2b_d1	rgmii1_rxd1	vout2_d1				mii1_crs			gpio4_30	Driver off
0x15C4	CTRL_CORE_PAD_VIN2A_D23	A4	vin2a_d23		vin2b_d0	rgmii1_rxd0	vout2_d0				mii1_txen			gpio4_31	Driver off
0x15C8	CTRL_CORE_PAD_VOUT1_CLK	D11	vout1_clk			vin2a_fld0 vin1a_fld0	vin1a_fld0				spi3_cs0			gpio4_19	Driver off
0x15CC	CTRL_CORE_PAD_VOUT1_DE	B10	vout1_de			vin2a_de0 vin1a_de0	vin1a_de0				spi3_d1			gpio4_20	Driver off
0x15D0	CTRL_CORE_PAD_VOUT1_FLD	B11	vout1_fld			vin2a_clk0 vin1a_clk0	vin1a_clk0				spi3_cs1			gpio4_21	Driver off
0x15D4	CTRL_CORE_PAD_VOUT1_HSYNC	C11	vout1_hsync			vin2a_hsync0 vin1a_hsync0	vin1a_hsync0				spi3_d0			gpio4_22	Driver off
0x15D8	CTRL_CORE_PAD_VOUT1_VSYNC	E11	vout1_vsync			vin2a_vsync0 vin1a_vsync0	vin1a_vsync0				spi3_sclk			gpio4_23	Driver off
0x15DC	CTRL_CORE_PAD_VOUT1_D0	F11	vout1_d0		uart5_rxd	vin2a_d16 vin1a_d16	vin1a_d16				spi3_cs2			gpio8_0	Driver off
0x15E0	CTRL_CORE_PAD_VOUT1_D1	G10	vout1_d1		uart5_txd	vin2a_d17 vin1a_d17	vin1a_d17							gpio8_1	Driver off
0x15E4	CTRL_CORE_PAD_VOUT1_D2	F10	vout1_d2		emu2	vin2a_d18 vin1a_d18	vin1a_d18	obs0	obs16	obs_irq1				gpio8_2	Driver off
0x15E8	CTRL_CORE_PAD_VOUT1_D3	G11	vout1_d3		emu5	vin2a_d19 vin1a_d19	vin1a_d19	obs1	obs17	obs_dmarq1				gpio8_3	Driver off
0x15EC	CTRL_CORE_PAD_VOUT1_D4	E9	vout1_d4		emu6	vin2a_d20 vin1a_d20	vin1a_d20	obs2	obs18					gpio8_4	Driver off
0x15F0	CTRL_CORE_PAD_VOUT1_D5	F9	vout1_d5		emu7	vin2a_d21 vin1a_d21	vin1a_d21	obs3	obs19					gpio8_5	Driver off
0x15F4	CTRL_CORE_PAD_VOUT1_D6	F8	vout1_d6		emu8	vin2a_d22 vin1a_d22	vin1a_d22	obs4	obs20					gpio8_6	Driver off
0x15F8	CTRL_CORE_PAD_VOUT1_D7	E7	vout1_d7		emu9	vin2a_d23 vin1a_d23	vin1a_d23							gpio8_7	Driver off
0x15FC	CTRL_CORE_PAD_VOUT1_D8	E8	vout1_d8		uart6_rxd	vin2a_d8 vin1a_d8	vin1a_d8							gpio8_8	Driver off
0x1600	CTRL_CORE_PAD_VOUT1_D9	D9	vout1_d9		uart6_txd	vin2a_d9 vin1a_d9	vin1a_d9							gpio8_9	Driver off
0x1604	CTRL_CORE_PAD_VOUT1_D10	D7	vout1_d10		emu3	vin2a_d10 vin1a_d10	vin1a_d10	obs5	obs21	obs_irq2				gpio8_10	Driver off
0x1608	CTRL_CORE_PAD_VOUT1_D11	D8	vout1_d11		emu10	vin2a_d11 vin1a_d11	vin1a_d11	obs6	obs22	obs_dmarq2				gpio8_11	Driver off
0x160C	CTRL_CORE_PAD_VOUT1_D12	A5	vout1_d12		emu11	vin2a_d12 vin1a_d12	vin1a_d12	obs7	obs23					gpio8_12	Driver off
0x1610	CTRL_CORE_PAD_VOUT1_D13	C6	vout1_d13		emu12	vin2a_d13 vin1a_d13	vin1a_d13	obs8	obs24					gpio8_13	Driver off

Table 4-3. Multiplexing Characteristics (continued)

ADDRESS	REGISTER NAME	BALL NUMBER	MUXMODE FIELD SETTINGS (CTRL_CORE_PAD_*[3:0])											
			0	1	2	3*	4*	5*	6*	7	8*	9	10	14*	15
0x1614	CTRL_CORE_PAD_VOUT1_D14	C8	vout1_d14		emu13	vin2a_d14 vin1a_d14	vin1a_d14	obs9	obs25					gpio8_14	Driver off
0x1618	CTRL_CORE_PAD_VOUT1_D15	C7	vout1_d15		emu14	vin2a_d15 vin1a_d15	vin1a_d15	obs10	obs26					gpio8_15	Driver off
0x161C	CTRL_CORE_PAD_VOUT1_D16	B7	vout1_d16		uart7_rxd	vin2a_d0 vin1a_d0	vin1a_d0							gpio8_16	Driver off
0x1620	CTRL_CORE_PAD_VOUT1_D17	B8	vout1_d17		uart7_txd	vin2a_d1 vin1a_d1	vin1a_d1							gpio8_17	Driver off
0x1624	CTRL_CORE_PAD_VOUT1_D18	A7	vout1_d18		emu4	vin2a_d2 vin1a_d2	vin1a_d2	obs11	obs27					gpio8_18	Driver off
0x1628	CTRL_CORE_PAD_VOUT1_D19	A8	vout1_d19		emu15	vin2a_d3 vin1a_d3	vin1a_d3	obs12	obs28					gpio8_19	Driver off
0x162C	CTRL_CORE_PAD_VOUT1_D20	C9	vout1_d20		emu16	vin2a_d4 vin1a_d4	vin1a_d4	obs13	obs29					gpio8_20	Driver off
0x1630	CTRL_CORE_PAD_VOUT1_D21	A9	vout1_d21		emu17	vin2a_d5 vin1a_d5	vin1a_d5	obs14	obs30					gpio8_21	Driver off
0x1634	CTRL_CORE_PAD_VOUT1_D22	B9	vout1_d22		emu18	vin2a_d6 vin1a_d6	vin1a_d6	obs15	obs31					gpio8_22	Driver off
0x1638	CTRL_CORE_PAD_VOUT1_D23	A10	vout1_d23		emu19	vin2a_d7 vin1a_d7	vin1a_d7				spi3_cs3			gpio8_23	Driver off
0x163C	CTRL_CORE_PAD_MDIO_MCLK	V1	mdio_mclk	uart3_rtsn		mii0_col	vin2a_clk0	vin1b_clk1						gpio5_15	Driver off
0x1640	CTRL_CORE_PAD_MDIO_D	U4	mdio_d	uart3_ctsn		mii0_txer	vin2a_d0	vin1b_d0						gpio5_16	Driver off
0x1644	CTRL_CORE_PAD_RMII_MHZ_50_CLK	U3	RMII_MHZ_50_CLK				vin2a_d11							gpio5_17	Driver off
0x1648	CTRL_CORE_PAD_UART3_RXD	V2	uart3_rxd		rmii1_crs	mii0_rxdv	vin2a_d1	vin1b_d1		spi3_sclk				gpio5_18	Driver off
0x164C	CTRL_CORE_PAD_UART3_TXD	Y1	uart3_txd		rmii1_rxer	mii0_rxclk	vin2a_d2	vin1b_d2		spi3_d1	spi4_cs1			gpio5_19	Driver off
0x1650	CTRL_CORE_PAD_RGMII0_TXC	W9	rgmii0_txc	uart3_ctsn	rmii1_rxd1	mii0_rxd3	vin2a_d3	vin1b_d3	usb3_ulpi_clk	spi3_d0	spi4_cs2			gpio5_20	Driver off
0x1654	CTRL_CORE_PAD_RGMII0_TXCTL	V9	rgmii0_txctl	uart3_rtsn	rmii1_rxd0	mii0_rxd2	vin2a_d4	vin1b_d4	usb3_ulpi_stp	spi3_cs0	spi4_cs3			gpio5_21	Driver off
0x1658	CTRL_CORE_PAD_RGMII0_TXD3	V7	rgmii0_txd3	rmii0_crs		mii0_crs	vin2a_de0	vin1b_de1	usb3_ulpi_dir	spi4_sclk	uart4_rxd			gpio5_22	Driver off
0x165C	CTRL_CORE_PAD_RGMII0_TXD2	U7	rgmii0_txd2	rmii0_rxer		mii0_rxer	vin2a_hsync0	vin1b_hsync1	usb3_ulpi_nxt	spi4_d1	uart4_txd			gpio5_23	Driver off
0x1660	CTRL_CORE_PAD_RGMII0_TXD1	V6	rgmii0_txd1	rmii0_rxd1		mii0_rxd1	vin2a_vsync0	vin1b_vsync1	usb3_ulpi_d0	spi4_d0	uart4_ctsn			gpio5_24	Driver off
0x1664	CTRL_CORE_PAD_RGMII0_TXD0	U6	rgmii0_txd0	rmii0_rxd0		mii0_rxd0	vin2a_d10		usb3_ulpi_d1	spi4_cs0	uart4_rtsn			gpio5_25	Driver off
0x1668	CTRL_CORE_PAD_RGMII0_RXC	U5	rgmii0_rxc		rmii1_txen	mii0_txclk	vin2a_d5	vin1b_d5	usb3_ulpi_d2					gpio5_26	Driver off
0x166C	CTRL_CORE_PAD_RGMII0_RXCTL	V5	rgmii0_rxctl		rmii1_txd1	mii0_txd3	vin2a_d6	vin1b_d6	usb3_ulpi_d3					gpio5_27	Driver off
0x1670	CTRL_CORE_PAD_RGMII0_RXD3	V4	rgmii0_rxd3		rmii1_txd0	mii0_txd2	vin2a_d7	vin1b_d7	usb3_ulpi_d4					gpio5_28	Driver off

Table 4-3. Multiplexing Characteristics (continued)

ADDRESS	REGISTER NAME	BALL NUMBER	MUXMODE FIELD SETTINGS (CTRL_CORE_PAD_*[3:0])												
			0	1	2	3*	4*	5*	6*	7	8*	9	10	14*	15
0x1674	CTRL_CORE_PAD_RGMII0_RXD2	V3	rgmii0_rxd2	rmii0_txen		mii0_txen	vin2a_d8		usb3_ulpi_d5					gpio5_29	Driver off
0x1678	CTRL_CORE_PAD_RGMII0_RXD1	Y2	rgmii0_rxd1	rmii0_txd1		mii0_txd1	vin2a_d9		usb3_ulpi_d6					gpio5_30	Driver off
0x167C	CTRL_CORE_PAD_RGMII0_RXD0	W2	rgmii0_rxd0	rmii0_txd0		mii0_txd0	vin2a_fld0	vin1b_fld1	usb3_ulpi_d7					gpio5_31	Driver off
0x1680	CTRL_CORE_PAD_USB1_DRVVBUS	AB10	usb1_drvvbus							timer16				gpio6_12	Driver off
0x1684	CTRL_CORE_PAD_USB2_DRVVBUS	AC10	usb2_drvvbus							timer15				gpio6_13	Driver off
0x1688	CTRL_CORE_PAD_GPIO6_14	E21	gpio6_14	mcasp1_axr8	dcan2_tx	uart10_rxd			vout2_hsync		vin2a_hsync0 vin1a_hsync0	i2c3_sda	timer1	gpio6_14	Driver off
0x168C	CTRL_CORE_PAD_GPIO6_15	F20	gpio6_15	mcasp1_axr9	dcan2_rx	uart10_txd			vout2_vsync		vin2a_vsync0 vin1a_vsync0	i2c3_scl	timer2	gpio6_15	Driver off
0x1690	CTRL_CORE_PAD_GPIO6_16	F21	gpio6_16	mcasp1_axr10					vout2_fld		vin2a_fld0 vin1a_fld0	clkout1	timer3	gpio6_16	Driver off
0x1694	CTRL_CORE_PAD_XREF_CLK0	D18	xref_clk0	mcasp2_axr8	mcasp1_axr4	mcasp1_ahclkx	mcasp5_ahclkx			vin1a_d0		clkout2	timer13	gpio6_17	Driver off
0x1698	CTRL_CORE_PAD_XREF_CLK1	E17	xref_clk1	mcasp2_axr9	mcasp1_axr5	mcasp2_ahclkx	mcasp6_ahclkx			vin1a_clk0			timer14	gpio6_18	Driver off
0x169C	CTRL_CORE_PAD_XREF_CLK2	B26	xref_clk2	mcasp2_axr10	mcasp1_axr6	mcasp3_ahclkx	mcasp7_ahclkx		vout2_clk		vin2a_clk0 vin1a_clk0		timer15	gpio6_19	Driver off
0x16A0	CTRL_CORE_PAD_XREF_CLK3	C23	xref_clk3	mcasp2_axr11	mcasp1_axr7	mcasp4_ahclkx	mcasp8_ahclkx		vout2_de		vin2a_de0 vin1a_de0	clkout3	timer16	gpio6_20	Driver off
0x16A4	CTRL_CORE_PAD_MCASP1_ACLKX	C14	mcasp1_aclkx							vin1a_fld0			i2c3_sda	gpio7_31	Driver off
0x16A8	CTRL_CORE_PAD_MCASP1_FSX	D14	mcasp1_fsx							vin1a_de0			i2c3_scl	gpio7_30	Driver off
0x16AC	CTRL_CORE_PAD_MCASP1_ACLKR	B14	mcasp1_aclkr	mcasp7_axr2					vout2_d0		vin2a_d0 vin1a_d0		i2c4_sda	gpio5_0	Driver off
0x16B0	CTRL_CORE_PAD_MCASP1_FSR	J14	mcasp1_fsr	mcasp7_axr3					vout2_d1		vin2a_d1 vin1a_d1		i2c4_scl	gpio5_1	Driver off
0x16B4	CTRL_CORE_PAD_MCASP1_AXR0	G12	mcasp1_axr0			uart6_rxd				vin1a_vsync0			i2c5_sda	gpio5_2	Driver off
0x16B8	CTRL_CORE_PAD_MCASP1_AXR1	F12	mcasp1_axr1			uart6_txd				vin1a_hsync0			i2c5_scl	gpio5_3	Driver off
0x16BC	CTRL_CORE_PAD_MCASP1_AXR2	G13	mcasp1_axr2	mcasp6_axr2		uart6_ctsn			vout2_d2		vin2a_d2 vin1a_d2			gpio5_4	Driver off
0x16C0	CTRL_CORE_PAD_MCASP1_AXR3	J11	mcasp1_axr3	mcasp6_axr3		uart6_rtsn			vout2_d3		vin2a_d3 vin1a_d3			gpio5_5	Driver off
0x16C4	CTRL_CORE_PAD_MCASP1_AXR4	E12	mcasp1_axr4	mcasp4_axr2					vout2_d4		vin2a_d4 vin1a_d4			gpio5_6	Driver off
0x16C8	CTRL_CORE_PAD_MCASP1_AXR5	F13	mcasp1_axr5	mcasp4_axr3					vout2_d5		vin2a_d5 vin1a_d5			gpio5_7	Driver off
0x16CC	CTRL_CORE_PAD_MCASP1_AXR6	C12	mcasp1_axr6	mcasp5_axr2					vout2_d6		vin2a_d6 vin1a_d6			gpio5_8	Driver off
0x16D0	CTRL_CORE_PAD_MCASP1_AXR7	D12	mcasp1_axr7	mcasp5_axr3					vout2_d7		vin2a_d7 vin1a_d7		timer4	gpio5_9	Driver off

Table 4-3. Multiplexing Characteristics (continued)

ADDRESS	REGISTER NAME	BALL NUMBER	MUXMODE FIELD SETTINGS (CTRL_CORE_PAD_*[3:0])												
			0	1	2	3*	4*	5*	6*	7	8*	9	10	14*	15
0x16D4	CTRL_CORE_PAD_MCASP1_AXR8	B12	mcasp1_axr8	mcasp6_axr0		spi3_sclk				vin1a_d15			timer5	gpio5_10	Driver off
0x16D8	CTRL_CORE_PAD_MCASP1_AXR9	A11	mcasp1_axr9	mcasp6_axr1		spi3_d1				vin1a_d14			timer6	gpio5_11	Driver off
0x16DC	CTRL_CORE_PAD_MCASP1_AXR10	B13	mcasp1_axr10	mcasp6_aclkx	mcasp6_aclkr	spi3_d0				vin1a_d13			timer7	gpio5_12	Driver off
0x16E0	CTRL_CORE_PAD_MCASP1_AXR11	A12	mcasp1_axr11	mcasp6_fsx	mcasp6_fsr	spi3_cs0				vin1a_d12			timer8	gpio4_17	Driver off
0x16E4	CTRL_CORE_PAD_MCASP1_AXR12	E14	mcasp1_axr12	mcasp7_axr0		spi3_cs1				vin1a_d11			timer9	gpio4_18	Driver off
0x16E8	CTRL_CORE_PAD_MCASP1_AXR13	A13	mcasp1_axr13	mcasp7_axr1						vin1a_d10			timer10	gpio6_4	Driver off
0x16EC	CTRL_CORE_PAD_MCASP1_AXR14	G14	mcasp1_axr14	mcasp7_aclkx	mcasp7_aclkr					vin1a_d9			timer11	gpio6_5	Driver off
0x16F0	CTRL_CORE_PAD_MCASP1_AXR15	F14	mcasp1_axr15	mcasp7_fsx	mcasp7_fsr					vin1a_d8			timer12	gpio6_6	Driver off
0x16F4	CTRL_CORE_PAD_MCASP2_ACLKX	A19	mcasp2_aclkx							vin1a_d7					Driver off
0x16F8	CTRL_CORE_PAD_MCASP2_FSX	A18	mcasp2_fsx							vin1a_d6					Driver off
0x16FC	CTRL_CORE_PAD_MCASP2_ACLKR	E15	mcasp2_aclkr	mcasp8_axr2					vout2_d8		vin2a_d8 vin1a_d8				Driver off
0x1700	CTRL_CORE_PAD_MCASP2_FSR	A20	mcasp2_fsr	mcasp8_axr3					vout2_d9		vin2a_d9 vin1a_d9				Driver off
0x1704	CTRL_CORE_PAD_MCASP2_AXR0	B15	mcasp2_axr0						vout2_d10		vin2a_d10 vin1a_d10				Driver off
0x1708	CTRL_CORE_PAD_MCASP2_AXR1	A15	mcasp2_axr1						vout2_d11		vin2a_d11 vin1a_d11				Driver off
0x170C	CTRL_CORE_PAD_MCASP2_AXR2	C15	mcasp2_axr2	mcasp3_axr2						vin1a_d5				gpio6_8	Driver off
0x1710	CTRL_CORE_PAD_MCASP2_AXR3	A16	mcasp2_axr3	mcasp3_axr3						vin1a_d4				gpio6_9	Driver off
0x1714	CTRL_CORE_PAD_MCASP2_AXR4	D15	mcasp2_axr4	mcasp8_axr0					vout2_d12		vin2a_d12 vin1a_d12			gpio1_4	Driver off
0x1718	CTRL_CORE_PAD_MCASP2_AXR5	B16	mcasp2_axr5	mcasp8_axr1					vout2_d13		vin2a_d13 vin1a_d13			gpio6_7	Driver off
0x171C	CTRL_CORE_PAD_MCASP2_AXR6	B17	mcasp2_axr6	mcasp8_aclkx	mcasp8_aclkr				vout2_d14		vin2a_d14 vin1a_d14			gpio2_29	Driver off
0x1720	CTRL_CORE_PAD_MCASP2_AXR7	A17	mcasp2_axr7	mcasp8_fsx	mcasp8_fsr				vout2_d15		vin2a_d15 vin1a_d15			gpio1_5	Driver off
0x1724	CTRL_CORE_PAD_MCASP3_ACLKX	B18	mcasp3_aclkx	mcasp3_aclkr	mcasp2_axr12	uart7_rxd				vin1a_d3				gpio5_13	Driver off
0x1728	CTRL_CORE_PAD_MCASP3_FSX	F15	mcasp3_fsx	mcasp3_fsr	mcasp2_axr13	uart7_txd				vin1a_d2				gpio5_14	Driver off
0x172C	CTRL_CORE_PAD_MCASP3_AXR0	B19	mcasp3_axr0		mcasp2_axr14	uart7_ctsn	uart5_rxd			vin1a_d1					Driver off
0x1730	CTRL_CORE_PAD_MCASP3_AXR1	C17	mcasp3_axr1		mcasp2_axr15	uart7_rtsn	uart5_txd			vin1a_d0		vin1a_fld0			Driver off

Table 4-3. Multiplexing Characteristics (continued)

ADDRESS	REGISTER NAME	BALL NUMBER	MUXMODE FIELD SETTINGS (CTRL_CORE_PAD_*[3:0])												
			0	1	2	3*	4*	5*	6*	7	8*	9	10	14*	15
0x1734	CTRL_CORE_PAD_ MCASP4_ACLKX	C18	mcasp4_aclkx	mcasp4_aclkr	spi3_sclk	uart8_rxd	i2c4_sda		vout2_d16		vin2a_d16 vin1a_d16	vin1a_d15			Driver off
0x1738	CTRL_CORE_PAD_ MCASP4_FSX	A21	mcasp4_fsx	mcasp4_fsr	spi3_d1	uart8_txd	i2c4_scl		vout2_d17		vin2a_d17 vin1a_d17	vin1a_d14			Driver off
0x173C	CTRL_CORE_PAD_ MCASP4_AXR0	G16	mcasp4_axr0		spi3_d0	uart8_ctsn	uart4_rxd		vout2_d18		vin2a_d18 vin1a_d18	vin1a_d13		i2c6_scl	Driver off
0x1740	CTRL_CORE_PAD_ MCASP4_AXR1	D17	mcasp4_axr1		spi3_cs0	uart8_rtsn	uart4_txd		vout2_d19		vin2a_d19 vin1a_d19	vin1a_d12		i2c6_sda	Driver off
0x1744	CTRL_CORE_PAD_ MCASP5_ACLKX	AA3	mcasp5_aclkx	mcasp5_aclkr	spi4_sclk	uart9_rxd	i2c5_sda		vout2_d20		vin2a_d20 vin1a_d20	vin1a_d11			Driver off
0x1748	CTRL_CORE_PAD_ MCASP5_FSX	AB9	mcasp5_fsx	mcasp5_fsr	spi4_d1	uart9_txd	i2c5_scl		vout2_d21		vin2a_d21 vin1a_d21	vin1a_d10			Driver off
0x174C	CTRL_CORE_PAD_ MCASP5_AXR0	AB3	mcasp5_axr0		spi4_d0	uart9_ctsn	uart3_rxd		vout2_d22		vin2a_d22 vin1a_d22	vin1a_d9			Driver off
0x1750	CTRL_CORE_PAD_ MCASP5_AXR1	AA4	mcasp5_axr1		spi4_cs0	uart9_rtsn	uart3_txd		vout2_d23		vin2a_d23 vin1a_d23	vin1a_d8			Driver off
0x1754	CTRL_CORE_PAD_ MMC1_CLK	W6	mmc1_clk											gpio6_21	Driver off
0x1758	CTRL_CORE_PAD_ MMC1_CMD	Y6	mmc1_cmd											gpio6_22	Driver off
0x175C	CTRL_CORE_PAD_ MMC1_DAT0	AA6	mmc1_dat0											gpio6_23	Driver off
0x1760	CTRL_CORE_PAD_ MMC1_DAT1	Y4	mmc1_dat1											gpio6_24	Driver off
0x1764	CTRL_CORE_PAD_ MMC1_DAT2	AA5	mmc1_dat2											gpio6_25	Driver off
0x1768	CTRL_CORE_PAD_ MMC1_DAT3	Y3	mmc1_dat3											gpio6_26	Driver off
0x176C	CTRL_CORE_PAD_ MMC1_SDCD	W7	mmc1_sdcd			uart6_rxd	i2c4_sda							gpio6_27	Driver off
0x1770	CTRL_CORE_PAD_ MMC1_SDWP	Y9	mmc1_sdwp			uart6_txd	i2c4_scl							gpio6_28	Driver off
0x1774	CTRL_CORE_PAD_ GPIO6_10	AC5	gpio6_10	mdio_mclk	i2c3_sda	usb3_ulpi_d7	vin2b_hsync1					vin1a_clk0	ehrpwm2A	gpio6_10	Driver off
0x1778	CTRL_CORE_PAD_ GPIO6_11	AB4	gpio6_11	mdio_d	i2c3_scl	usb3_ulpi_d6	vin2b_vsync1					vin1a_de0	ehrpwm2B	gpio6_11	Driver off
0x177C	CTRL_CORE_PAD_ MMC3_CLK	AD4	mmc3_clk			usb3_ulpi_d5	vin2b_d7					vin1a_d7	ehrpwm2_trip zone_input	gpio6_29	Driver off
0x1780	CTRL_CORE_PAD_ MMC3_CMD	AC4	mmc3_cmd	spi3_sclk		usb3_ulpi_d4	vin2b_d6					vin1a_d6	eCAP2_in_P WM2_out	gpio6_30	Driver off
0x1784	CTRL_CORE_PAD_ MMC3_DAT0	AC7	mmc3_dat0	spi3_d1	uart5_rxd	usb3_ulpi_d3	vin2b_d5					vin1a_d5	eQEP3A_in	gpio6_31	Driver off
0x1788	CTRL_CORE_PAD_ MMC3_DAT1	AC6	mmc3_dat1	spi3_d0	uart5_txd	usb3_ulpi_d2	vin2b_d4					vin1a_d4	eQEP3B_in	gpio7_0	Driver off
0x178C	CTRL_CORE_PAD_ MMC3_DAT2	AC9	mmc3_dat2	spi3_cs0	uart5_ctsn	usb3_ulpi_d1	vin2b_d3					vin1a_d3	eQEP3_index	gpio7_1	Driver off
0x1790	CTRL_CORE_PAD_ MMC3_DAT3	AC3	mmc3_dat3	spi3_cs1	uart5_rtsn	usb3_ulpi_d0	vin2b_d2					vin1a_d2	eQEP3_strob e	gpio7_2	Driver off

Table 4-3. Multiplexing Characteristics (continued)

ADDRESS	REGISTER NAME	BALL NUMBER	MUXMODE FIELD SETTINGS (CTRL_CORE_PAD_*[3:0])												
			0	1	2	3*	4*	5*	6*	7	8*	9	10	14*	15
0x1794	CTRL_CORE_PAD_MMC3_DAT4	AC8	mmc3_dat4	spi4_sclk	uart10_rxd	usb3_ulpi_nxt	vin2b_d1					vin1a_d1	ehrpwm3A	gpio1_22	Driver off
0x1798	CTRL_CORE_PAD_MMC3_DAT5	AD6	mmc3_dat5	spi4_d1	uart10_txd	usb3_ulpi_dir	vin2b_d0					vin1a_d0	ehrpwm3B	gpio1_23	Driver off
0x179C	CTRL_CORE_PAD_MMC3_DAT6	AB8	mmc3_dat6	spi4_d0	uart10_ctsn	usb3_ulpi_stp	vin2b_de1					vin1a_hsync0	ehrpwm3_tripzone_input	gpio1_24	Driver off
0x17A0	CTRL_CORE_PAD_MMC3_DAT7	AB5	mmc3_dat7	spi4_cs0	uart10_rtsn	usb3_ulpi_clk	vin2b_clk1					vin1a_vsync0	eCAP3_in_PWM3_out	gpio1_25	Driver off
0x17A4	CTRL_CORE_PAD_SPI1_SCLK	A25	spi1_sclk											gpio7_7	Driver off
0x17A8	CTRL_CORE_PAD_SPI1_D1	F16	spi1_d1											gpio7_8	Driver off
0x17AC	CTRL_CORE_PAD_SPI1_D0	B25	spi1_d0											gpio7_9	Driver off
0x17B0	CTRL_CORE_PAD_SPI1_CS0	A24	spi1_cs0											gpio7_10	Driver off
0x17B4	CTRL_CORE_PAD_SPI1_CS1	A22	spi1_cs1		sata1_led	spi2_cs1								gpio7_11	Driver off
0x17B8	CTRL_CORE_PAD_SPI1_CS2	B21	spi1_cs2	uart4_rxd	mmc3_sdcd	spi2_cs2	dcan2_tx	mdio_mclk	hdmi1_hpd					gpio7_12	Driver off
0x17BC	CTRL_CORE_PAD_SPI1_CS3	B20	spi1_cs3	uart4_txd	mmc3_sdwp	spi2_cs3	dcan2_rx	mdio_d	hdmi1_cec					gpio7_13	Driver off
0x17C0	CTRL_CORE_PAD_SPI2_SCLK	A26	spi2_sclk	uart3_rxd										gpio7_14	Driver off
0x17C4	CTRL_CORE_PAD_SPI2_D1	B22	spi2_d1	uart3_txd										gpio7_15	Driver off
0x17C8	CTRL_CORE_PAD_SPI2_D0	G17	spi2_d0	uart3_ctsn	uart5_rxd									gpio7_16	Driver off
0x17CC	CTRL_CORE_PAD_SPI2_CS0	B24	spi2_cs0	uart3_rtsn	uart5_txd									gpio7_17	Driver off
0x17D0	CTRL_CORE_PAD_DCAN1_TX	G20	dcan1_tx		uart8_rxd	mmc2_sdcd			hdmi1_hpd					gpio1_14	Driver off
0x17D4	CTRL_CORE_PAD_DCAN1_RX	G19	dcan1_rx		uart8_txd	mmc2_sdwp	sata1_led		hdmi1_cec					gpio1_15	Driver off
0x17E0	CTRL_CORE_PAD_UART1_RXD	B27	uart1_rxd			mmc4_sdcd								gpio7_22	Driver off
0x17E4	CTRL_CORE_PAD_UART1_TXD	C26	uart1_txd			mmc4_sdwp								gpio7_23	Driver off
0x17E8	CTRL_CORE_PAD_UART1_CTSN	E25	uart1_ctsn		uart9_rxd	mmc4_clk								gpio7_24	Driver off
0x17EC	CTRL_CORE_PAD_UART1_RTSN	C27	uart1_rtsn		uart9_txd	mmc4_cmd								gpio7_25	Driver off
0x17F0	CTRL_CORE_PAD_UART2_RXD	D28		uart3_ctsn	uart3_rctx	mmc4_dat0	uart2_rxd	uart1_dcdn						gpio7_26	Driver off
0x17F4	CTRL_CORE_PAD_UART2_TXD	D26	uart2_txd	uart3_rtsn	uart3_sd	mmc4_dat1	uart2_txd	uart1_dsrn						gpio7_27	Driver off
0x17F8	CTRL_CORE_PAD_UART2_CTSN	D27	uart2_ctsn		uart3_rxd	mmc4_dat2	uart10_rxd	uart1_dtrn						gpio1_16	Driver off

Table 4-3. Multiplexing Characteristics (continued)

ADDRESS	REGISTER NAME	BALL NUMBER	MUXMODE FIELD SETTINGS (CTRL_CORE_PAD_*[3:0])											
			0	1	2	3*	4*	5*	6*	7	8*	9	10	14*	15
0x17FC	CTRL_CORE_PAD_UART2_RTSN	C28	uart2_rtsn	uart3_txd	uart3_irtx	mmc4_dat3	uart10_txd	uart1_rin						gpio1_17	Driver off
0x1800	CTRL_CORE_PAD_I2C1_SDA	C21	i2c1_sda												Driver off
0x1804	CTRL_CORE_PAD_I2C1_SCL	C20	i2c1_scl												Driver off
0x1808	CTRL_CORE_PAD_I2C2_SDA	C25	i2c2_sda	hdmi1_ddc_scl											Driver off
0x180C	CTRL_CORE_PAD_I2C2_SCL	F17	i2c2_scl	hdmi1_ddc_sda											Driver off
0x1818	CTRL_CORE_PAD_WAKEUP0	AD17	Wakeup0	dcan1_rx										gpio1_0 sys_nirq2	Driver off
0x1824	CTRL_CORE_PAD_WAKEUP3	AC16	Wakeup3	sys_nirq1										gpio1_3 dcan2_rx	Driver off
0x1828	CTRL_CORE_PAD_ON_OFF	Y11	on_off												
0x182C	CTRL_CORE_PAD_RTC_PORZ	AB17	rtc_porz												
0x1830	CTRL_CORE_PAD_TMS	F18	tms												
0x1834	CTRL_CORE_PAD_TDI	D23	tdi											gpio8_27	
0x1838	CTRL_CORE_PAD_TDO	F19	tdo											gpio8_28	
0x183C	CTRL_CORE_PAD_TCLK	E20	tclk												
0x1840	CTRL_CORE_PAD_TRSTN	D20	trstn												
0x1844	CTRL_CORE_PAD_RTCK	E18	rtck											gpio8_29	
0x1848	CTRL_CORE_PAD_EMU0	G21	emu0											gpio8_30	
0x184C	CTRL_CORE_PAD_EMU1	D24	emu1											gpio8_31	
0x185C	CTRL_CORE_PAD_RESETN	E23	resetn												
0x1860	CTRL_CORE_PAD_NMIN_DSP	D21	nmin_dsp												
0x1864	CTRL_CORE_PAD_RSTOUTN	F23	rstoutn												

1. N/A stands for Not Applicable.

4.4 Signal Descriptions

Many signals are available on multiple pins, according to the software configuration of the pin multiplexing options.

1. **SIGNAL NAME:** The name of the signal passing through the pin.

NOTE

The subsystem multiplexing signals are not described in Table 4-2 and Table 4-3.

2. **DESCRIPTION:** Description of the signal
3. **TYPE:** Signal direction and type:
   – I = Input
   – O = Output
   – IO = Input or output
   – D = Open Drain
   – DS = Differential
   – A = Analog
   – PWR = Power
   – GND = Ground
4. **BALL:** Associated ball(s) bottom

NOTE

For more information, see *Control Module* chapter, *Control Module Register Manual* section in the device TRM.

4.4.1 Video Input Ports (VIP)

NOTE

For more information, see *Video Input Port* chapter in the device TRM.

CAUTION

The I/O timings provided in Section 7, *Timing Requirements and Switching Characteristics* are valid only for VIN1 and VIN2 if signals within a single IOSET are used. The IOSETs are defined in Table 7-4 and Table 7-5.

Table 4-4. VIP Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	BALL
Video Input 1			
vin1a_clk0	Video Input 1 Port A Clock input.Input clock for 8-bit 16-bit or 24-bit Port A video capture. Input data is sampled on the CLK0 edge.	I	AC5 / B11 / E17 / P1 / P4 / B26
vin1a_d0	Video Input 1 Port A Data input	I	AD6 / B7 / C17 / D18 / M6 / R6 / B14
vin1a_d1	Video Input 1 Port A Data input	I	AC8 / B19 / B8 / M2 / T9 / J14
vin1a_d2	Video Input 1 Port A Data input	I	A7 / AC3 / F15 / L5 / T6 / G13
vin1a_d3	Video Input 1 Port A Data input	I	A8 / AC9 / B18 / M1 / T7 / J11
vin1a_d4	Video Input 1 Port A Data input	I	A16 / AC6 / C9 / L6 / P6 / E12

Table 4-4. VIP Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
vin1a_d5	Video Input 1 Port A Data input	I	A9 / AC7 / C15 / L4 / R9 / F13
vin1a_d6	Video Input 1 Port A Data input	I	A18 / AC4 / B9 / L3 / R5 / C12
vin1a_d7	Video Input 1 Port A Data input	I	A10 / A19 / AD4 / L2 / P5 / D12
vin1a_d8	Video Input 1 Port A Data input	I	AA4 / E8 / F14 / L1 / U2 / E15
vin1a_d9	Video Input 1 Port A Data input	I	AB3 / D9 / G14 / K2 / U1 / A20
vin1a_d10	Video Input 1 Port A Data input	I	A13 / AB9 / D7 / J1 / P3 / B15
vin1a_d11	Video Input 1 Port A Data input	I	AA3 / D8 / E14 / J2 / R2 / A15
vin1a_d12	Video Input 1 Port A Data input	I	A12 / A5 / D17 / H1 / K7 / D15
vin1a_d13	Video Input 1 Port A Data input	I	B13 / C6 / G16 / J3 / M7 / B16
vin1a_d14	Video Input 1 Port A Data input	I	A11 / A21 / C8 / H2 / J5 / B17
vin1a_d15	Video Input 1 Port A Data input	I	B12 / C18 / C7 / H3 / K6 / A17
vin1a_d16	Video Input 1 Port A Data input	I	F11 / R6 / C18
vin1a_d17	Video Input 1 Port A Data input	I	G10 / T9 / A21
vin1a_d18	Video Input 1 Port A Data input	I	F10 / T6 / G16
vin1a_d19	Video Input 1 Port A Data input	I	G11 / T7 / D17
vin1a_d20	Video Input 1 Port A Data input	I	E9 / P6 / AA3
vin1a_d21	Video Input 1 Port A Data input	I	F9 / R9 / AB9
vin1a_d22	Video Input 1 Port A Data input	I	F8 / R5 / AB3
vin1a_d23	Video Input 1 Port A Data input	I	E7 / P5 / AA4
vin1a_de0	Video Input 1 Port A Field ID input	I	AB4 / B10 / D14 / N9 / H6 / C23 / P7
vin1a_fld0	Video Input 1 Port A Field ID input	I	C14 / C17 / D11 / P9 / J7 / F21
vin1a_hsync0	Video Input 1 Port A Horizontal Sync input	I	AB8 / C11 / F12 / N7 / R3 / P7 / E21
vin1a_vsync0	Video Input 1 Port A Vertical Sync input	I	AB5 / E11 / G12 / R4 / T2 / N1 / F20
vin1b_clk1	Video Input 1 Port B Clock input	I	N9 / V1 / M4 / P7
vin1b_d0	Video Input 1 Port B Data input	I	R6 / U4 / K7
vin1b_d1	Video Input 1 Port B Data input	I	T9 / V2 / M7
vin1b_d2	Video Input 1 Port B Data input	I	T6 / Y1 / J5
vin1b_d3	Video Input 1 Port B Data input	I	T7 / W9 / K6
vin1b_d4	Video Input 1 Port B Data input	I	P6 / V9 / J7
vin1b_d5	Video Input 1 Port B Data input	I	R9 / U5 / J4
vin1b_d6	Video Input 1 Port B Data input	I	R5 / V5 / J6
vin1b_d7	Video Input 1 Port B Data input	I	P5 / V4 / H4
vin1b_de1	Video Input 1 Port B Field ID input	I	P9 / V7 / N6
vin1b_fld1	Video Input 1 Port B Field ID input	I	P4 / W2 / M4
vin1b_hsync1	Video Input 1 Port B Horizontal Sync input	I	N7 / U7 / H5
vin1b_vsync1	Video Input 1 Port B Vertical Sync input	I	R4 / V6 / H6
Video Input 2			

Table 4-4. VIP Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
vin2a_clk0	Video Input 2 Port A Clock input	I	B11 / B26 / E1 / P4 / V1
vin2a_d0	Video Input 2 Port A Data input	I	B14 / B7 / F2 / R6 / U4
vin2a_d1	Video Input 2 Port A Data input	I	B8 / F3 / J14 / T9 / V2
vin2a_d2	Video Input 2 Port A Data input	I	A7 / D1 / G13 / T6 / Y1
vin2a_d3	Video Input 2 Port A Data input	I	A8 / E2 / J11 / T7 / W9
vin2a_d4	Video Input 2 Port A Data input	I	C9 / D2 / E12 / P6 / V9
vin2a_d5	Video Input 2 Port A Data input	I	A9 / F13 / F4 / R9 / U5
vin2a_d6	Video Input 2 Port A Data input	I	B9 / C1 / C12 / R5 / V5
vin2a_d7	Video Input 2 Port A Data input	I	A10 / D12 / E4 / P5 / V4
vin2a_d8	Video Input 2 Port A Data input	I	E15 / E8 / F5 / U2 / V3
vin2a_d9	Video Input 2 Port A Data input	I	A20 / D9 / E6 / U1 / Y2
vin2a_d10	Video Input 2 Port A Data input	I	B15 / D3 / D7 / P3 / U6
vin2a_d11	Video Input 2 Port A Data input	I	A15 / D8 / F6 / R2 / U3
vin2a_d12	Video Input 2 Port A Data input	I	A5 / D15 / D5 / K7
vin2a_d13	Video Input 2 Port A Data input	I	B16 / C2 / C6 / M7
vin2a_d14	Video Input 2 Port A Data input	I	B17 / C3 / C8 / J5
vin2a_d15	Video Input 2 Port A Data input	I	A17 / C4 / C7 / K6
vin2a_d16	Video Input 2 Port A Data input	I	B2 / C18 / F11
vin2a_d17	Video Input 2 Port A Data input	I	A21 / D6 / G10
vin2a_d18	Video Input 2 Port A Data input	I	C5 / F10 / G16
vin2a_d19	Video Input 2 Port A Data input	I	A3 / D17 / G11
vin2a_d20	Video Input 2 Port A Data input	I	AA3 / B3 / E9
vin2a_d21	Video Input 2 Port A Data input	I	AB9 / B4 / F9
vin2a_d22	Video Input 2 Port A Data input	I	AB3 / B5 / F8
vin2a_d23	Video Input 2 Port A Data input	I	A4 / AA4 / E7
vin2a_de0	Video Input 2 Port A Field ID input	I	B10 / C23 / G2 / H6 / P7 / V7
vin2a_fld0	Video Input 2 Port A Field ID input	I	D11 / F21 / G2 / H7 / J7 / P9 / W2
vin2a_hsync0	Video Input 2 Port A Horizontal Sync input	I	C11 / E21 / G1 / P7 / R3 / U7
vin2a_vsync0	Video Input 2 Port A Vertical Sync input	I	E11 / F20 / G6 / N1 / T2 / V6
vin2b_clk1	Video Input 2 Port B Clock input	I	AB5 / H7 / M4 / P7
vin2b_d0	Video Input 2 Port B Data input	I	A4 / AD6 / K7
vin2b_d1	Video Input 2 Port B Data input	I	AC8 / B5 / M7
vin2b_d2	Video Input 2 Port B Data input	I	AC3 / B4 / J5
vin2b_d3	Video Input 2 Port B Data input	I	AC9 / B3 / K6
vin2b_d4	Video Input 2 Port B Data input	I	A3 / AC6 / J7
vin2b_d5	Video Input 2 Port B Data input	I	AC7 / C5 / J4

Table 4-4. VIP Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
vin2b_d6	Video Input 2 Port B Data input	I	AC4 / D6 / J6
vin2b_d7	Video Input 2 Port B Data input	I	AD4 / B2 / H4
vin2b_de1	Video Input 2 Port B Field ID input	I	AB8 / G2 / N6
vin2b_fld1	Video Input 2 Port B Field ID input	I	G2 / M4
vin2b_hsync1	Video Input 2 Port B Horizontal Sync input	I	AC5 / G1 / H5
vin2b_vsync1	Video Input 2 Port B Vertical Sync input	I	AB4 / G6 / H6

4.4.2 Display Subsystem – Video Output Ports

CAUTION

The I/O timings provided in Section 7, *Timing Requirements and Switching Characteristics* are valid only if signals within a single IOSET are used. The IOSETs are defined inTable 7-18.

Table 4-5. DSS Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	BALL
DPI Video Output 1			
vout1_clk	Video Output 1 Clock output	O	D11
vout1_de	Video Output 1 Data Enable output	O	B10
vout1_fld	Video Output 1 Field ID output.This signal is not used for embedded sync modes.	O	B11
vout1_hsync	Video Output 1 Horizontal Sync output.This signal is not used for embedded sync modes.	O	C11
vout1_vsync	Video Output 1 Vertical Sync output.This signal is not used for embedded sync modes.	O	E11
vout1_d0	Video Output 1 Data output	O	F11
vout1_d1	Video Output 1 Data output	O	G10
vout1_d2	Video Output 1 Data output	O	F10
vout1_d3	Video Output 1 Data output	O	G11
vout1_d4	Video Output 1 Data output	O	E9
vout1_d5	Video Output 1 Data output	O	F9
vout1_d6	Video Output 1 Data output	O	F8
vout1_d7	Video Output 1 Data output	O	E7
vout1_d8	Video Output 1 Data output	O	E8
vout1_d9	Video Output 1 Data output	O	D9
vout1_d10	Video Output 1 Data output	O	D7
vout1_d11	Video Output 1 Data output	O	D8
vout1_d12	Video Output 1 Data output	O	A5
vout1_d13	Video Output 1 Data output	O	C6
vout1_d14	Video Output 1 Data output	O	C8
vout1_d15	Video Output 1 Data output	O	C7
vout1_d16	Video Output 1 Data output	O	B7
vout1_d17	Video Output 1 Data output	O	B8
vout1_d18	Video Output 1 Data output	O	A7
vout1_d19	Video Output 1 Data output	O	A8
vout1_d20	Video Output 1 Data output	O	C9
vout1_d21	Video Output 1 Data output	O	A9
vout1_d22	Video Output 1 Data output	O	B9

Table 4-5. DSS Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
vout1_d23	Video Output 1 Data output	O	A10
DPI Video Output 2			
vout2_clk	Video Output 2 Clock output	O	H7 / B26
vout2_de	Video Output 2 Data Enable output	O	G2 / C23
vout2_fld	Video Output 2 Field ID output.This signal is not used for embedded sync modes.	O	E1 / F21
vout2_hsync	Video Output 2 Horizontal Sync output.This signal is not used for embedded sync modes.	O	G1 / E21
vout2_vsync	Video Output 2 Vertical Sync output.This signal is not used for embedded sync modes.	O	G6 / F20
vout2_d0	Video Output 2 Data output	O	A4 / B14
vout2_d1	Video Output 2 Data output	O	B5 / J14
vout2_d2	Video Output 2 Data output	O	B4 / G13
vout2_d3	Video Output 2 Data output	O	B3 / J11
vout2_d4	Video Output 2 Data output	O	A3 / E12
vout2_d5	Video Output 2 Data output	O	C5 / F13
vout2_d6	Video Output 2 Data output	O	D6 / C12
vout2_d7	Video Output 2 Data output	O	B2 / D12
vout2_d8	Video Output 2 Data output	O	C4 / E15
vout2_d9	Video Output 2 Data output	O	C3 / A20
vout2_d10	Video Output 2 Data output	O	C2 / B15
vout2_d11	Video Output 2 Data output	O	D5 / A15
vout2_d12	Video Output 2 Data output	O	F6 / D15
vout2_d13	Video Output 2 Data output	O	D3 / B16
vout2_d14	Video Output 2 Data output	O	E6 / B17
vout2_d15	Video Output 2 Data output	O	F5 / A17
vout2_d16	Video Output 2 Data output	O	E4 / C18
vout2_d17	Video Output 2 Data output	O	C1 / A21
vout2_d18	Video Output 2 Data output	O	F4 / G16
vout2_d19	Video Output 2 Data output	O	D2 / D17
vout2_d20	Video Output 2 Data output	O	E2 / AA3
vout2_d21	Video Output 2 Data output	O	D1 / AB9
vout2_d22	Video Output 2 Data output	O	F3 / AB3
vout2_d23	Video Output 2 Data output	O	F2 / AA4
DPI Video Output 3			
vout3_clk	Video Output 3 Clock output	O	P1
vout3_d0	Video Output 3 Data output	O	M6
vout3_d1	Video Output 3 Data output	O	M2
vout3_d2	Video Output 3 Data output	O	L5
vout3_d3	Video Output 3 Data output	O	M1
vout3_d4	Video Output 3 Data output	O	L6
vout3_d5	Video Output 3 Data output	O	L4
vout3_d6	Video Output 3 Data output	O	L3
vout3_d7	Video Output 3 Data output	O	L2
vout3_d8	Video Output 3 Data output	O	L1
vout3_d9	Video Output 3 Data output	O	K2
vout3_d10	Video Output 3 Data output	O	J1
vout3_d11	Video Output 3 Data output	O	J2
vout3_d12	Video Output 3 Data output	O	H1
vout3_d13	Video Output 3 Data output	O	J3

Table 4-5. DSS Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
vout3_d14	Video Output 3 Data output	O	H2
vout3_d15	Video Output 3 Data output	O	H3
vout3_d16	Video Output 3 Data output	O	R6
vout3_d17	Video Output 3 Data output	O	T9
vout3_d18	Video Output 3 Data output	O	T6
vout3_d19	Video Output 3 Data output	O	T7
vout3_d20	Video Output 3 Data output	O	P6
vout3_d21	Video Output 3 Data output	O	R9
vout3_d22	Video Output 3 Data output	O	R5
vout3_d23	Video Output 3 Data output	O	P5
vout3_de	Video Output 3 Data Enable output	O	N9
vout3_fld	Video Output 3 Field ID output.This signal is not used for embedded sync modes.	O	P9
vout3_hsync	Video Output 3 Horizontal Sync output.This signal is not used for embedded sync modes.	O	N7
vout3_vsync	Video Output 3 Vertical Sync output.This signal is not used for embedded sync modes.	O	R4

4.4.3 Display Subsystem – High-Definition Multimedia Interface (HDMI)

NOTE

For more information, see *Display Subsystem* chapter in the device TRM.

Table 4-6. HDMI Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	BALL
hdmi1_cec	HDMI consumer electronic control	IOD	B20/ G19
hdmi1_hpd	HDMI display hot plug detect	IOD	B21/ G20
hdmi1_ddc_scl	HDMI display data channel clock	IOD	C25
hdmi1_ddc_sda	HDMI display data channel data	IOD	F17
hdmi1_clockx	HDMI clock differential positive or negative	ODS	AG16
hdmi1_clocky	HDMI clock differential positive or negative	ODS	AH16
hdmi1_data2x	HDMI data 2 differential positive or negative	ODS	AG19
hdmi1_data2y	HDMI data 2 differential positive or negative	ODS	AH19
hdmi1_data1x	HDMI data 1 differential positive or negative	ODS	AG18
hdmi1_data1y	HDMI data 1 differential positive or negative	ODS	AH18
hdmi1_data0x	HDMI data 0 differential positive or negative	ODS	AG17
hdmi1_data0y	HDMI data 0 differential positive or negative	ODS	AH17

4.4.4 Camera Serial Interface 2 CAL bridge (CSI2)

NOTE

For more information, see *Camera Interface Subsystem* chapter in the device TRM.

Table 4-7. CSI 2 Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	BALL
csi2_0_dx0	Serial data/clock input - line 0 (position 1)	I	AE1
csi2_0_dy0	Serial data/clock input - line 0 (position 1)	I	AD2
csi2_0_dx1	Serial data/clock input - line 1 (position 2)	I	AF1

Table 4-7. CSI 2 Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
csi2_0_dy1	Serial data/clock input - line 1 (position 2)	I	AE2
csi2_0_dx2	Serial data/clock input - line 2 (position 3)	I	AF2
csi2_0_dy2	Serial data/clock input - line 2 (position 3)	I	AF3
csi2_0_dx3	Serial data/clock input - line 3 (position 4)	I	AH4
csi2_0_dy3	Serial data/clock input - line 3 (position 4)	I	AG4
csi2_0_dx4	Serial data input only - line 4 (position 5) (1)	I	AH3
csi2_0_dy4	Serial data input only - line 4 (position 5) (1)	I	AG3
csi2_1_dx0	Serial data/clock input - line 0 (position 1)	I	AG5
csi2_1_dy0	Serial data/clock input - line 0 (position 1)	I	AH5
csi2_1_dx1	Serial data/clock input - line 1 (position 2)	I	AG6
csi2_1_dy1	Serial data/clock input - line 1 (position 2)	I	AH6
csi2_1_dx2	Serial data/clock input - line 2 (position 3)	I	AH7
csi2_1_dy2	Serial data/clock input - line 2 (position 3)	I	AG7

(1) Line 4 (position 5) supports only data. For more information, see *Camera Interface Subsystem* chapter in the device TRM.

4.4.5 External Memory Interface (EMIF SDRAM)

NOTE

For more information, see *Memory Subsystem* chapter, *EMIF Controller* section in the device TRM.

NOTE

Dual rank support is not available on this device, but signal names are retained for consistency with the TDA2xx family of devices.

NOTE

The index number 1 which is part of the EMIF1 signal prefixes (ddr1_*) listed in Table 4-8, *EMIF SDRAM Signal Descriptions*, column "SIGNAL NAME" not to be confused with DDR1 type of SDRAM memories.

Table 4-8. EMIF SDRAM Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	BALL
EMIF SDRAM Channel 1			
ddr1_csn0	EMIF1 Chip Select 0	O	AH23
ddr1_csn1	EMIF1 Chip Select 1	O	AB16
ddr1_cke	EMIF1 Clock Enable	O	AG22
ddr1_ck	EMIF1 Clock	O	AG24
ddr1_nck	EMIF1 Negative Clock	O	AH24
ddr1_odt0	EMIF1 On-Die Termination for Chip Select 0	O	AE20
ddr1_odt1	EMIF1 On-Die Termination for Chip Select 1	O	AC17
ddr1_casn	EMIF1 Column Address Strobe	O	AC18
ddr1_rasn	EMIF1 Row Address Strobe	O	AF20
ddr1_wen	EMIF1 Write Enable	O	AH21
ddr1_rst	EMIF1 Reset output (DDR3-SDRAM only)	O	AG21
ddr1_ba0	EMIF1 Bank Address	O	AF17
ddr1_ba1	EMIF1 Bank Address	O	AE18

Table 4-8. EMIF SDRAM Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
ddr1_ba2	EMIF1 Bank Address	O	AB18
ddr1_a0	EMIF1 Address Bus	O	AD20
ddr1_a1	EMIF1 Address Bus	O	AC19
ddr1_a2	EMIF1 Address Bus	O	AC20
ddr1_a3	EMIF1 Address Bus	O	AB19
ddr1_a4	EMIF1 Address Bus	O	AF21
ddr1_a5	EMIF1 Address Bus	O	AH22
ddr1_a6	EMIF1 Address Bus	O	AG23
ddr1_a7	EMIF1 Address Bus	O	AE21
ddr1_a8	EMIF1 Address Bus	O	AF22
ddr1_a9	EMIF1 Address Bus	O	AE22
ddr1_a10	EMIF1 Address Bus	O	AD21
ddr1_a11	EMIF1 Address Bus	O	AD22
ddr1_a12	EMIF1 Address Bus	O	AC21
ddr1_a13	EMIF1 Address Bus	O	AF18
ddr1_a14	EMIF1 Address Bus	O	AE17
ddr1_a15	EMIF1 Address Bus	O	AD18
ddr1_d0	EMIF1 Data Bus	IO	AF25
ddr1_d1	EMIF1 Data Bus	IO	AF26
ddr1_d2	EMIF1 Data Bus	IO	AG26
ddr1_d3	EMIF1 Data Bus	IO	AH26
ddr1_d4	EMIF1 Data Bus	IO	AF24
ddr1_d5	EMIF1 Data Bus	IO	AE24
ddr1_d6	EMIF1 Data Bus	IO	AF23
ddr1_d7	EMIF1 Data Bus	IO	AE23
ddr1_d8	EMIF1 Data Bus	IO	AC23
ddr1_d9	EMIF1 Data Bus	IO	AF27
ddr1_d10	EMIF1 Data Bus	IO	AG27
ddr1_d11	EMIF1 Data Bus	IO	AF28
ddr1_d12	EMIF1 Data Bus	IO	AE26
ddr1_d13	EMIF1 Data Bus	IO	AC25
ddr1_d14	EMIF1 Data Bus	IO	AC24
ddr1_d15	EMIF1 Data Bus	IO	AD25
ddr1_d16	EMIF1 Data Bus	IO	V20
ddr1_d17	EMIF1 Data Bus	IO	W20
ddr1_d18	EMIF1 Data Bus	IO	AB28
ddr1_d19	EMIF1 Data Bus	IO	AC28
ddr1_d20	EMIF1 Data Bus	IO	AC27
ddr1_d21	EMIF1 Data Bus	IO	Y19
ddr1_d22	EMIF1 Data Bus	IO	AB27
ddr1_d23	EMIF1 Data Bus	IO	Y20
ddr1_d24	EMIF1 Data Bus	IO	AA23
ddr1_d25	EMIF1 Data Bus	IO	Y22
ddr1_d26	EMIF1 Data Bus	IO	Y23
ddr1_d27	EMIF1 Data Bus	IO	AA24
ddr1_d28	EMIF1 Data Bus	IO	Y24
ddr1_d29	EMIF1 Data Bus	IO	AA26

Table 4-8. EMIF SDRAM Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
ddr1_d30	EMIF1 Data Bus	IO	AA25
ddr1_d31	EMIF1 Data Bus	IO	AA28
ddr1_ecc_d0	EMIF1 ECC Data Bus	IO	W22
ddr1_ecc_d1	EMIF1 ECC Data Bus	IO	V23
ddr1_ecc_d2	EMIF1 ECC Data Bus	IO	W19
ddr1_ecc_d3	EMIF1 ECC Data Bus	IO	W23
ddr1_ecc_d4	EMIF1 ECC Data Bus	IO	Y25
ddr1_ecc_d5	EMIF1 ECC Data Bus	IO	V24
ddr1_ecc_d6	EMIF1 ECC Data Bus	IO	V25
ddr1_ecc_d7	EMIF1 ECC Data Bus	IO	Y26
ddr1_dqm0	EMIF1 Data Mask	O	AD23
ddr1_dqm1	EMIF1 Data Mask	O	AB23
ddr1_dqm2	EMIF1 Data Mask	O	AC26
ddr1_dqm3	EMIF1 Data Mask	O	AA27
ddr1_dqm_ecc	EMIF1 ECC Data Mask	O	V26
ddr1_dqs0	Data strobe 0 input/output for byte 0 of the 32-bit data bus. This signal is output to the EMIF1 memory when writing and input when reading.	IO	AH25
ddr1_dqsn0	Data strobe 0 invert	IO	AG25
ddr1_dqs1	Data strobe 1 input/output for byte 1 of the 32-bit data bus. This signal is output to the EMIF1 memory when writing and input when reading.	IO	AE27
ddr1_dqsn1	Data strobe 1 invert	IO	AE28
ddr1_dqs2	Data strobe 2 input/output for byte 2 of the 32-bit data bus. This signal is output to the EMIF1 memory when writing and input when reading.	IO	AD27
ddr1_dqsn2	Data strobe 2 invert	IO	AD28
ddr1_dqs3	Data strobe 3 input/output for byte 3 of the 32-bit data bus. This signal is output to the EMIF1 memory when writing and input when reading.	IO	Y28
ddr1_dqsn3	Data strobe 3 invert	IO	Y27
ddr1_dqs_ecc	EMIF1 ECC Data strobe input/output. This signal is output to the EMIF1 memory when writing and input when reading.	IO	V27
ddr1_dqsn_ecc	EMIF1 ECC Complementary Data strobe	IO	V28
ddr1_vref0	Reference Power Supply EMIF1	A	Y18

4.4.6 General-Purpose Memory Controller (GPMC)

NOTE

For more information, see *Memory Subsystem* chapter, *General-Purpose Memory Controller* section in the device TRM.

Table 4-9. GPMC Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	BALL
gpmc_ad0	GPMC Data 0 in A/D nonmultiplexed mode and additionally Address 1 in A/D multiplexed mode	IO	M6
gpmc_ad1	GPMC Data 1 in A/D nonmultiplexed mode and additionally Address 2 in A/D multiplexed mode	IO	M2
gpmc_ad2	GPMC Data 2 in A/D nonmultiplexed mode and additionally Address 3 in A/D multiplexed mode	IO	L5
gpmc_ad3	GPMC Data 3 in A/D nonmultiplexed mode and additionally Address 4 in A/D multiplexed mode	IO	M1
gpmc_ad4	GPMC Data 4 in A/D nonmultiplexed mode and additionally Address 5 in A/D multiplexed mode	IO	L6

Table 4-9. GPMC Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
gpmc_ad5	GPMC Data 5 in A/D nonmultiplexed mode and additionally Address 6 in A/D multiplexed mode	IO	L4
gpmc_ad6	GPMC Data 6 in A/D nonmultiplexed mode and additionally Address 7 in A/D multiplexed mode	IO	L3
gpmc_ad7	GPMC Data 7 in A/D nonmultiplexed mode and additionally Address 8 in A/D multiplexed mode	IO	L2
gpmc_ad8	GPMC Data 8 in A/D nonmultiplexed mode and additionally Address 9 in A/D multiplexed mode	IO	L1
gpmc_ad9	GPMC Data 9 in A/D nonmultiplexed mode and additionally Address 10 in A/D multiplexed mode	IO	K2
gpmc_ad10	GPMC Data 10 in A/D nonmultiplexed mode and additionally Address 11 in A/D multiplexed mode	IO	J1
gpmc_ad11	GPMC Data 11 in A/D nonmultiplexed mode and additionally Address 12 in A/D multiplexed mode	IO	J2
gpmc_ad12	GPMC Data 12 in A/D nonmultiplexed mode and additionally Address 13 in A/D multiplexed mode	IO	H1
gpmc_ad13	GPMC Data 13 in A/D nonmultiplexed mode and additionally Address 14 in A/D multiplexed mode	IO	J3
gpmc_ad14	GPMC Data 14 in A/D nonmultiplexed mode and additionally Address 15 in A/D multiplexed mode	IO	H2
gpmc_ad15	GPMC Data 15 in A/D nonmultiplexed mode and additionally Address 16 in A/D multiplexed mode	IO	H3
gpmc_a0	GPMC Address 0. Only used to effectively address 8-bit data nonmultiplexed memories	O	R6 / P4
gpmc_a1	GPMC address 1 in A/D nonmultiplexed mode and Address 17 in A/D multiplexed mode	O	T9 / P1
gpmc_a2	GPMC address 2 in A/D nonmultiplexed mode and Address 18 in A/D multiplexed mode	O	T6 / N1
gpmc_a3	GPMC address 3 in A/D nonmultiplexed mode and Address 19 in A/D multiplexed mode	O	T7 / M4
gpmc_a4	GPMC address 4 in A/D nonmultiplexed mode and Address 20 in A/D multiplexed mode	O	P6
gpmc_a5	GPMC address 5 in A/D nonmultiplexed mode and Address 21 in A/D multiplexed mode	O	R9
gpmc_a6	GPMC address 6 in A/D nonmultiplexed mode and Address 22 in A/D multiplexed mode	O	R5
gpmc_a7	GPMC address 7 in A/D nonmultiplexed mode and Address 23 in A/D multiplexed mode	O	P5
gpmc_a8	GPMC address 8 in A/D nonmultiplexed mode and Address 24 in A/D multiplexed mode	O	N7
gpmc_a9	GPMC address 9 in A/D nonmultiplexed mode and Address 25 in A/D multiplexed mode	O	R4
gpmc_a10	GPMC address 10 in A/D nonmultiplexed mode and Address 26 in A/D multiplexed mode	O	N9
gpmc_a11	GPMC address 11 in A/D nonmultiplexed mode and unused in A/D multiplexed mode	O	P9
gpmc_a12	GPMC address 12 in A/D nonmultiplexed mode and unused in A/D multiplexed mode	O	P4
gpmc_a13	GPMC address 13 in A/D nonmultiplexed mode and unused in A/D multiplexed mode	O	R3 / K7 / P2
gpmc_a14	GPMC address 14 in A/D nonmultiplexed mode and unused in A/D multiplexed mode	O	T2 / M7 / P1
gpmc_a15	GPMC address 15 in A/D nonmultiplexed mode and unused in A/D multiplexed mode	O	U2 / J5 / N2
gpmc_a16	GPMC address 16 in A/D nonmultiplexed mode and unused in A/D multiplexed mode	O	U1 / K6 / R6

Table 4-9. GPMC Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
gpmc_a17	GPMC address 17 in A/D nonmultiplexed mode and unused in A/D multiplexed mode	O	P3 / J7 / E1
gpmc_a18	GPMC address 18 in A/D nonmultiplexed mode and unused in A/D multiplexed mode	O	R2 / J4 / H7
gpmc_a19	GPMC address 19 in A/D nonmultiplexed mode and unused in A/D multiplexed mode	O	K7(3) / J6
gpmc_a20	GPMC address 20 in A/D nonmultiplexed mode and unused in A/D multiplexed mode	O	M7(3) / H4
gpmc_a21	GPMC address 21 in A/D nonmultiplexed mode and unused in A/D multiplexed mode	O	J5(3) / H5
gpmc_a22	GPMC address 22 in A/D nonmultiplexed mode and unused in A/D multiplexed mode	O	K6(3) / H6
gpmc_a23	GPMC address 23 in A/D nonmultiplexed mode and unused in A/D multiplexed mode	O	F6 / J7 / N1 / P2
gpmc_a24	GPMC address 24 in A/D nonmultiplexed mode and unused in A/D multiplexed mode	O	D3 / J4(3) / P1
gpmc_a25	GPMC address 25 in A/D nonmultiplexed mode and unused in A/D multiplexed mode	O	E6 / J6(3) / N2
gpmc_a26	GPMC address 26 in A/D nonmultiplexed mode and unused in A/D multiplexed mode	O	F5 / H4(3) / R6
gpmc_a27	GPMC address 27 in A/D nonmultiplexed mode and Address 27 in A/D multiplexed mode	O	G1 / H5(3) / E1 / H7
gpmc_cs0	GPMC Chip Select 0 (active low)	O	T1
gpmc_cs1	GPMC Chip Select 1 (active low)	O	H6
gpmc_cs2	GPMC Chip Select 2 (active low)	O	P2
gpmc_cs3	GPMC Chip Select 3 (active low)	O	P1
gpmc_cs4	GPMC Chip Select 4 (active low)	O	N6
gpmc_cs5	GPMC Chip Select 5 (active low)	O	M4
gpmc_cs6	GPMC Chip Select 6 (active low)	O	N1
gpmc_cs7	GPMC Chip Select 7 (active low)	O	P7
gpmc_clk(1)(2)	GPMC Clock output	IO	P7
gpmc_advn_ale	GPMC address valid active low or address latch enable	O	N1
gpmc_oen_ren	GPMC output enable active low or read enable	O	M5
gpmc_wen	GPMC write enable active low	O	M3
gpmc_ben0	GPMC lower-byte enable active low	O	N6
gpmc_ben1	GPMC upper-byte enable active low	O	M4
gpmc_wait0	GPMC external indication of wait 0	I	N2
gpmc_wait1	GPMC external indication of wait 1	I	P7 / N1

(1) This clock signal is implemented as 'pad loopback' inside the device - the output signal is looped back through the input buffer to serve as the internal reference signal. Series termination is recommended (as close to device pin as possible) to improve signal integrity of the clock input. Any nonmonotonicity in voltage that occurs at the pad loopback clock pin between V_{IH} and V_{IL} must be less than V_{HYS}.

(2) The gpio6_16.clkout1 signal can be used as an “always-on” alternative to gpmc_clk provided that the external device can support the associated timing. See Table 7-25 *GPMC/NOR Flash Interface Switching Characteristics - Synchronous Mode - Default* and Table 7-27 *GPMC/NOR Flash Interface Switching Characteristics - Synchronous Mode - Alternate* for timing information.

(3) The internal pull resistors for balls K7, M7, J5, K6, J4, J6, H4, H5 are permanently disabled when sysboot15 is set to 0 as described in the section Sysboot Configuration of the Device TRM. If internal pull-up/down resistors are desired on these balls then sysboot15 should be set to 1. If gpmc boot mode is used with SYSBOOT15=0 (not recommended) then external pull-downs should be implemented to keep the address bus at logic-1 value during boot since the gpmc ms-address bits are high-z during boot.

4.4.7 Timers

NOTE
For more information, see *Timers* chapter in the device TRM.

Table 4-10. Timers Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	BALL
timer1	PWM output/event trigger input	IO	M4 / E21
timer2	PWM output/event trigger input	IO	N6 / F20
timer3	PWM output/event trigger input	IO	N1 / F21
timer4	PWM output/event trigger input	IO	P7 / D12
timer5	PWM output/event trigger input	IO	U2 / B12
timer6	PWM output/event trigger input	IO	T2 / A11
timer7	PWM output/event trigger input	IO	R3 / B13
timer8	PWM output/event trigger input	IO	P4 / A12
timer9	PWM output/event trigger input	IO	P9 / E14
timer10	PWM output/event trigger input	IO	N9 / A13
timer11	PWM output/event trigger input	IO	R4 / G14
timer12	PWM output/event trigger input	IO	N7 / F14
timer13	PWM output/event trigger input	IO	D18
timer14	PWM output/event trigger input	IO	E17
timer15	PWM output/event trigger input	IO	AC10 / B26
timer16	PWM output/event trigger input	IO	AB10 / C23

4.4.8 Inter-Integrated Circuit Interface (I2C)

NOTE
For more information, see *Multimaster High Speed I2C Controller* section in the device TRM.

NOTE
I2C1 and I2C2 do not support HS-mode.

Table 4-11. I2C Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	BALL
Inter-Integrated Circuit Interface 1 (I2C1)			
i2c1_scl	I2C1 Clock	IOD	C20
i2c1_sda	I2C1 Data	IOD	C21
Inter-Integrated Circuit Interface 2 (I2C2)			
i2c2_scl	I2C2 Clock	IOD	F17
i2c2_sda	I2C2 Data	IOD	C25
Inter-Integrated Circuit Interface 3 (I2C3)			
i2c3_scl	I2C3 Clock	IOD	P7/ D14/ AB4/ F20
i2c3_sda	I2C3 Data	IOD	N1/ C14/ AC5/ E21
Inter-Integrated Circuit Interface 4 (I2C4)			
i2c4_scl	I2C4 Clock	IOD	R6/ J14/ A21/ Y9
i2c4_sda	I2C4 Data	IOD	T9/ B14/ C18/ W7
Inter-Integrated Circuit Interface 5 (I2C5)			

Table 4-11. I2C Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
i2c5_scl	I2C5 Clock	IOD	AB9/ P6/ F12
i2c5_sda	I2C5 Data	IOD	AA3/ R9/ G12
Inter-Integrated Circuit Interface 6 (I2C6)			
i2c6_scl	I2C6 Clock	IOD	G16
i2c6_sda	I2C6 Data	IOD	D17

4.4.9 *Universal Asynchronous Receiver Transmitter (UART)*

NOTE

For more information about UART booting, see *UART/IrDA/CIR* section in the device TRM.

Table 4-12. UART Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	BALL
Universal Asynchronous Receiver/Transmitter 1 (UART1)			
uart1_dcdn	UART1 Data Carrier Detect active low	I	D28
uart1_dsrn	UART1 Data Set Ready Active Low	I	D26
uart1_dtrn	UART1 Data Terminal Ready Active Low	O	D27
uart1_rin	UART1 Ring Indicator	I	C28
uart1_rxd	UART1 Receive Data	I	B27
uart1_txd	UART1 Transmit Data	O	C26
uart1_ctsn	UART1 clear to send active low	I	E25
uart1_rtsn	UART1 request to send active low	O	C27
Universal Asynchronous Receiver/Transmitter 2 (UART2)			
uart2_rxd	UART2 Receive Data	I	D28
uart2_txd	UART2 Transmit Data	O	D26
uart2_ctsn	UART2 clear to send active low	I	D27
uart2_rtsn	UART2 request to send active low	O	C28
Universal Asynchronous Receiver/Transmitter 3 (UART3)/IrDA			
uart3_rxd	UART3 Receive Data	I	V2/ AB3/ A26 / D27
uart3_txd	UART3 Transmit Data	O	Y1/ AA4/ B22/ C28
uart3_ctsn	UART3 clear to send active low	I	U4/ W9/ G17/ D28
uart3_rtsn	UART3 request to send active low	O	V1/ V9/ D26/ B24
uart3_rctx	Remote control data	O	D28
uart3_sd	Infrared transceiver configure/shutdown	O	D26
uart3_irrx	Infrared data input. Also functions as uart3_rxd Receive Data Input when IrDA mode is not used.	I	D27
uart3_irtx	Infrared data output	O	C28
Universal Asynchronous Receiver/Transmitter 4 (UART4)			
uart4_rxd	UART4 Receive Data	I	V7/ G16/ B21
uart4_txd	UART4 Transmit Data	O	U7/ D17/ B20
uart4_ctsn	UART4 clear to send active low	I	V6
uart4_rtsn	UART4 request to send active low	O	U6
Universal Asynchronous Receiver/Transmitter 5 (UART5)			
uart5_rxd	UART5 Receive Data	I	R6/ F11/ B19/ AC7/ G17
uart5_txd	UART5 Transmit Data	O	T9/ G10/ C17/ AC6/ B24

Table 4-12. UART Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
uart5_ctsn	UART5 clear to send active low	I	T6 / AC9
uart5_rtsn	UART5 request to send active low	O	T7 / AC3
Universal Asynchronous Receiver/Transmitter 6 (UART6)			
uart6_rxd	UART6 Receive Data	I	P6/ E8/ G12/ W7
uart6_txd	UART6 Transmit Data	O	R9/ D9/ F12/ Y9
uart6_ctsn	UART6 clear to send active low	I	R5 / G13
uart6_rtsn	UART6 request to send active low	O	P5 / J11
Universal Asynchronous Receiver/Transmitter 7 (UART7)			
uart7_rxd	UART7 Receive Data	I	B18 / B7 / T6
uart7_txd	UART7 Transmit Data	O	B8 / F15 / T7
uart7_ctsn	UART7 clear to send active low	I	B19
uart7_rtsn	UART7 request to send active low	O	C17
Universal Asynchronous Receiver/Transmitter 8 (UART8)			
uart8_rxd	UART8 Receive Data	I	C18 / G20 / R5
uart8_txd	UART8 Transmit Data	O	A21 / G19 / P5
uart8_ctsn	UART8 clear to send active low	I	G16
uart8_rtsn	UART8 request to send active low	O	D17
Universal Asynchronous Receiver/Transmitter 9 (UART9)			
uart9_rxd	UART9 Receive Data	I	G1/ AA3/ E25
uart9_txd	UART9 Transmit Data	O	G6/ AB9/ C27
uart9_ctsn	UART9 clear to send active low	I	F2 / AB3
uart9_rtsn	UART9 request to send active low	O	F3/ AA4
Universal Asynchronous Receiver/Transmitter 10 (UART10)			
uart10_rxd	UART10 Receive Data	I	D1/ E21/ AC8/ D27
uart10_txd	UART10 Transmit Data	O	E2/ F20/ AD6/ C28
uart10_ctsn	UART10 clear to send active low	I	D2 / AB8
uart10_rtsn	UART10 request to send active low	O	F4 / AB5

4.4.10 Multichannel Serial Peripheral Interface (McSPI)

CAUTION

The I/O timings provided in Section 7, *Timing Requirements and Switching Characteristics* are applicable for all combinations of signals for SPI1 and SPI2. However, the timings are valid only for SPI3 and SPI4 if signals within a single IOSET are used. The IOSETS are defined in Table 7-40.

NOTE

For more information, see *Multichannel Serial Peripheral Interface* section in the device TRM.

Table 4-13. SPI Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	BALL
Serial Peripheral Interface 1			
spi1_sclk[(1)]	SPI1 Clock	IO	A25
spi1_d1	SPI1 Data. Can be configured as either MISO or MOSI.	IO	F16

Table 4-13. SPI Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
spi1_d0	SPI1 Data. Can be configured as either MISO or MOSI.	IO	B25
spi1_cs0	SPI1 Chip Select	IO	A24
spi1_cs1	SPI1 Chip Select	IO	A22
spi1_cs2	SPI1 Chip Select	IO	B21
spi1_cs3	SPI1 Chip Select	IO	B20
Serial Peripheral Interface 2			
spi2_sclk(1)	SPI2 Clock	IO	A26
spi2_d1	SPI2 Data. Can be configured as either MISO or MOSI.	IO	B22
spi2_d0	SPI2 Data. Can be configured as either MISO or MOSI.	IO	G17
spi2_cs0	SPI2 Chip Select	IO	B24
spi2_cs1	SPI2 Chip Select	IO	A22
spi2_cs2	SPI2 Chip Select	IO	B21
spi2_cs3	SPI2 Chip Select	IO	B20
Serial Peripheral Interface 3			
spi3_sclk(1)	SPI3 Clock	IO	AC4 / B12 / C18 / E11 / V2
spi3_d1	SPI3 Data. Can be configured as either MISO or MOSI.	IO	A11 / A21 / AC7 / B10 / Y1
spi3_d0	SPI3 Data. Can be configured as either MISO or MOSI.	IO	AC6 / B13 / C11 / G16 / W9
spi3_cs0	SPI3 Chip Select	IO	A12 / AC9 / D11 / D17 / V9
spi3_cs1	SPI3 Chip Select	IO	AC3 / B11 / E14
spi3_cs2	SPI3 Chip Select	IO	F11
spi3_cs3	SPI3 Chip Select	IO	A10
Serial Peripheral Interface 4			
spi4_sclk(1)	SPI4 Clock	IO	N7/ G1/ AA3/ V7/ AC8
spi4_d1	SPI4 Data. Can be configured as either MISO or MOSI.	IO	R4/ G6/ AB9/ U7/ AD6
spi4_d0	SPI4 Data. Can be configured as either MISO or MOSI.	IO	N9/ F2/ AB3/ V6/ AB8
spi4_cs0	SPI4 Chip Select	IO	P9/ F3/ AA4/ U6/ AB5
spi4_cs1	SPI4 Chip Select	IO	P4 / Y1
spi4_cs2	SPI4 Chip Select	IO	R3 / W9
spi4_cs3	SPI4 Chip Select	IO	T2 / V9

(1) This clock signal is implemented as 'pad loopback' inside the device - the output signal is looped back through the input buffer to serve as the internal reference signal. Series termination is recommended (as close to device pin as possible) to improve signal integrity of the clock input. Any nonmonotonicity in voltage that occurs at the pad loopback clock pin between V_{IH} and V_{IL} must be less than V_{HYS}.

4.4.11 Quad Serial Peripheral Interface (QSPI)

NOTE

For more information, see *Quad Serial Peripheral Interface* section in the device TRM.

Table 4-14. QSPI Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	BALL
qspi1_sclk	QSPI1 Serial Clock	IO	R2

Table 4-14. QSPI Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
qspi1_rtclk	QSPI1 Return Clock Input. Must be connected from QSPI1_SCLK on PCB. Refer to PCB Guidelines for QSPI1	I	R3
qspi1_d0	QSPI1 Data[0]. This pin is output data for all commands/writes and for dual read and quad read modes it becomes input data pin during read phase.	IO	U1
qspi1_d1	QSPI1 Data[1]. Input read data in all modes.	IO	P3
qspi1_d2	QSPI1 Data[2]. This pin is used only in quad read mode as input data pin during read phase	IO	U2
qspi1_d3	QSPI1 Data[3]. This pin is used only in quad read mode as input data pin during read phase	IO	T2
qspi1_cs0	QSPI1 Chip Select[0]. This pin is Used for QSPI1 boot modes.	IO	P2
qspi1_cs1	QSPI1 Chip Select[1]	O	P1
qspi1_cs2	QSPI1 Chip Select[2]	O	T7
qspi1_cs3	QSPI1 Chip Select[3]	O	P6

4.4.12 Multichannel Audio Serial Port (McASP)

NOTE

For more information, see *Multichannel Audio Serial Port* section in the device TRM.

Table 4-15. McASP Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	BALL
Multichannel Audio Serial Port 1			
mcasp1_axr0	McASP1 Transmit/Receive Data	IO	G12
mcasp1_axr1	McASP1 Transmit/Receive Data	IO	F12
mcasp1_axr2	McASP1 Transmit/Receive Data	IO	G13
mcasp1_axr3	McASP1 Transmit/Receive Data	IO	J11
mcasp1_axr4	McASP1 Transmit/Receive Data	IO	D18/ E12
mcasp1_axr5	McASP1 Transmit/Receive Data	IO	E17 / F13
mcasp1_axr6	McASP1 Transmit/Receive Data	IO	B26 / C12
mcasp1_axr7	McASP1 Transmit/Receive Data	IO	C23 / D12
mcasp1_axr8	McASP1 Transmit/Receive Data	IO	E21 / B12
mcasp1_axr9	McASP1 Transmit/Receive Data	IO	F20/ A11
mcasp1_axr10	McASP1 Transmit/Receive Data	IO	F21 / B13
mcasp1_axr11	McASP1 Transmit/Receive Data	IO	A12
mcasp1_axr12	McASP1 Transmit/Receive Data	IO	E14
mcasp1_axr13	McASP1 Transmit/Receive Data	IO	A13
mcasp1_axr14	McASP1 Transmit/Receive Data	IO	G14
mcasp1_axr15	McASP1 Transmit/Receive Data	IO	F14
mcasp1_fsx	McASP1 Transmit Frame Sync	IO	D14
mcasp1_aclkr(1)	McASP1 Receive Bit Clock	IO	B14
mcasp1_fsr	McASP1 Receive Frame Sync	IO	J14
mcasp1_ahclkx	McASP1 Transmit High-Frequency Master Clock	O	D18
mcasp1_aclkx(1)	McASP1 Transmit Bit Clock	IO	C14
Multichannel Audio Serial Port 2			
mcasp2_axr0	McASP2 Transmit/Receive Data	IO	B15
mcasp2_axr1	McASP2 Transmit/Receive Data	IO	A15
mcasp2_axr2	McASP2 Transmit/Receive Data	IO	C15

Table 4-15. McASP Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
mcasp2_axr3	McASP2 Transmit/Receive Data	IO	A16
mcasp2_axr4	McASP2 Transmit/Receive Data	IO	D15
mcasp2_axr5	McASP2 Transmit/Receive Data	IO	B16
mcasp2_axr6	McASP2 Transmit/Receive Data	IO	B17
mcasp2_axr7	McASP2 Transmit/Receive Data	IO	A17
mcasp2_axr8	McASP2 Transmit/Receive Data	IO	D18
mcasp2_axr9	McASP2 Transmit/Receive Data	IO	E17
mcasp2_axr10	McASP2 Transmit/Receive Data	IO	B26
mcasp2_axr11	McASP2 Transmit/Receive Data	IO	C23
mcasp2_axr12	McASP2 Transmit/Receive Data	IO	B18
mcasp2_axr13	McASP2 Transmit/Receive Data	IO	F15
mcasp2_axr14	McASP2 Transmit/Receive Data	IO	B19
mcasp2_axr15	McASP2 Transmit/Receive Data	IO	C17
mcasp2_fsx	McASP2 Transmit Frame Sync	IO	A18
mcasp2_aclkr(1)	McASP2 Receive Bit Clock	IO	E15
mcasp2_fsr	McASP2 Receive Frame Sync	IO	A20
mcasp2_ahclkx	McASP2 Transmit High-Frequency Master Clock	O	E17
mcasp2_aclkx(1)	McASP2 Transmit Bit Clock	IO	A19
Multichannel Audio Serial Port 3			
mcasp3_axr0	McASP3 Transmit/Receive Data	IO	B19
mcasp3_axr1	McASP3 Transmit/Receive Data	IO	C17
mcasp3_axr2	McASP3 Transmit/Receive Data	IO	C15
mcasp3_axr3	McASP3 Transmit/Receive Data	IO	A16
mcasp3_fsx	McASP3 Transmit Frame Sync	IO	F15
mcasp3_ahclkx	McASP3 Transmit High-Frequency Master Clock	O	B26
mcasp3_aclkx(1)	McASP3 Transmit Bit Clock	IO	B18
mcasp3_aclkr(1)	McASP3 Receive Bit Clock	IO	B18
mcasp3_fsr	McASP3 Receive Frame Sync	IO	F15
Multichannel Audio Serial Port 4			
mcasp4_axr0	McASP4 Transmit/Receive Data	IO	G16
mcasp4_axr1	McASP4 Transmit/Receive Data	IO	D17
mcasp4_axr2	McASP4 Transmit/Receive Data	IO	E12
mcasp4_axr3	McASP4 Transmit/Receive Data	IO	F13
mcasp4_fsx	McASP4 Transmit Frame Sync	IO	A21
mcasp4_ahclkx	McASP4 Transmit High-Frequency Master Clock	O	C23
mcasp4_aclkx(1)	McASP4 Transmit Bit Clock	IO	C18
mcasp4_aclkr(1)	McASP4 Receive Bit Clock	IO	C18
mcasp4_fsr	McASP4 Receive Frame Sync	IO	A21
Multichannel Audio Serial Port 5			
mcasp5_axr0	McASP5 Transmit/Receive Data	IO	AB3
mcasp5_axr1	McASP5 Transmit/Receive Data	IO	AA4
mcasp5_axr2	McASP5 Transmit/Receive Data	IO	C12
mcasp5_axr3	McASP5 Transmit/Receive Data	IO	D12
mcasp5_fsx	McASP5 Transmit Frame Sync	IO	AB9
mcasp5_ahclkx	McASP5 Transmit High-Frequency Master Clock	O	D18
mcasp5_aclkx(1)	McASP5 Transmit Bit Clock	IO	AA3
mcasp5_aclkr(1)	McASP5 Receive Bit Clock	IO	AA3

Table 4-15. McASP Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
mcasp5_fsr	McASP5 Receive Frame Sync	IO	AB9
Multichannel Audio Serial Port 6			
mcasp6_axr0	McASP6 Transmit/Receive Data	IO	B12
mcasp6_axr1	McASP6 Transmit/Receive Data	IO	A11
mcasp6_axr2	McASP6 Transmit/Receive Data	IO	G13
mcasp6_axr3	McASP6 Transmit/Receive Data	IO	J11
mcasp6_ahclkx	McASP6 Transmit High-Frequency Master Clock	O	E17
mcasp6_aclkx(1)	McASP6 Transmit Bit Clock	IO	B13
mcasp6_fsx	McASP6 Transmit Frame Sync	IO	A12
mcasp6_aclkr(1)	McASP6 Receive Bit Clock	IO	B13
mcasp6_fsr	McASP6 Receive Frame Sync	IO	A12
Multichannel Audio Serial Port 7			
mcasp7_axr0	McASP7 Transmit/Receive Data	IO	E14
mcasp7_axr1	McASP7 Transmit/Receive Data	IO	A13
mcasp7_axr2	McASP7 Transmit/Receive Data	IO	B14
mcasp7_axr3	McASP7 Transmit/Receive Data	IO	J14
mcasp7_ahclkx	McASP7 Transmit High-Frequency Master Clock	O	B26
mcasp7_aclkx(1)	McASP7 Transmit Bit Clock	IO	G14
mcasp7_fsx	McASP7 Transmit Frame Sync	IO	F14
mcasp7_aclkr(1)	McASP7 Receive Bit Clock	IO	G14
mcasp7_fsr	McASP7 Receive Frame Sync	IO	F14
Multichannel Audio Serial Port 8			
mcasp8_axr0	McASP8 Transmit/Receive Data	IO	D15
mcasp8_axr1	McASP8 Transmit/Receive Data	IO	B16
mcasp8_axr2	McASP8 Transmit/Receive Data	IO	E15
mcasp8_axr3	McASP8 Transmit/Receive Data	IO	A20
mcasp8_ahclkx	McASP8 Transmit High-Frequency Master Clock	O	C23
mcasp8_aclkx(1)	McASP8 Transmit Bit Clock	IO	B17
mcasp8_fsx	McASP8 Transmit Frame Sync	IO	A17
mcasp8_aclkr(1)	McASP8 Receive Bit Clock	IO	B17
mcasp8_fsr	McASP8 Receive Frame Sync	IO	A17

(1) This clock signal is implemented as 'pad loopback' inside the device - the output signal is looped back through the input buffer to serve as the internal reference signal. Series termination is recommended (as close to device pin as possible) to improve signal integrity of the clock input. Any non monotonicity in voltage that occurs at the pad loopback clock pin between V_{IH} and V_{IL} must be less than V_{HYS}.

4.4.13 Universal Serial Bus (USB)

NOTE

For more information, see *SuperSpeed USB DRD* section in the device TRM.

Table 4-16. Universal Serial Bus Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	BALL
Universal Serial Bus 1			
usb1_dp	USB1 USB2.0 differential signal pair (positive)	IODS	AD12
usb1_dm	USB1 USB2.0 differential signal pair (negative)	IODS	AC12
usb1_drvvbus	USB1 Drive VBUS signal	O	AB10
usb_rxn0(1)	USB1 USB3.0 receiver negative lane	IDS	AF12

Table 4-16. Universal Serial Bus Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
usb_rxp0[(1)]	USB1 USB3.0 receiver positive lane	IDS	AE12
usb_txn0[(1)]	USB1 USB3.0 transmitter negative lane	ODS	AC11
usb_txp0[(1)]	USB1 USB3.0 transmitter positive lane	ODS	AD11
Universal Serial Bus 2			
usb2_dp	USB2 USB2.0 differential signal pair (positive)	IODS	AE11
usb2_dm	USB2 USB2.0 differential signal pair (negative)	IODS	AF11
usb2_drvvbus	USB2 Drive VBUS signal	O	AC10
Universal Serial Bus 3			
usb3_ulpi_d0	USB3 - ULPI 8-bit data bus	IO	AC3 / V6
usb3_ulpi_d1	USB3 - ULPI 8-bit data bus	IO	AC9 / U6
usb3_ulpi_d2	USB3 - ULPI 8-bit data bus	IO	AC6 / U5
usb3_ulpi_d3	USB3 - ULPI 8-bit data bus	IO	AC7 / V5
usb3_ulpi_d4	USB3 - ULPI 8-bit data bus	IO	AC4 / V4
usb3_ulpi_d5	USB3 - ULPI 8-bit data bus	IO	AD4 / V3
usb3_ulpi_d6	USB3 - ULPI 8-bit data bus	IO	AB4 / Y2
usb3_ulpi_d7	USB3 - ULPI 8-bit data bus	IO	AC5 / W2
usb3_ulpi_nxt	USB3 - ULPI next	I	AC8 / U7
usb3_ulpi_dir	USB3 - ULPI bus direction	I	AD6 / V7
usb3_ulpi_stp	USB3 - ULPI stop	O	AB8 / V9
usb3_ulpi_clk	USB3 - ULPI functional clock	I	AB5 / W9

(1) Signals are enabled by selecting the correct field in the PCIE_B1C0_MODE_SEL register. There are no CTRL_CORE_PAD* register involved.

4.4.14 SATA

NOTE

For more information, see *SATA Controller* section in the device TRM.

Table 4-17. SATA Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	BALL
sata1_rxn0	SATA differential negative receiver lane 0	IDS	AH9
sata1_rxp0	SATA differential positive receiver lane 0	IDS	AG9
sata1_txn0	SATA differential negative transmitter lane 0	ODS	AG10
sata1_txp0	SATA differential positive transmitter lane 0	ODS	AH10
sata1_led	SATA channel activity indicator	O	A22 / G19

4.4.15 Peripheral Component Interconnect Express (PCIe)

NOTE

For more information, see *PCIe Controller* sections in the device TRM.

Table 4-18. PCIe Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	BALL
pcie_rxn0	PCIe1_PHY_RX Receive Data Lane 0 (negative) - mapped to PCIe_SS1 only.	IDS	AG13
pcie_rxp0	PCIe1_PHY_RX Receive Data Lane 0 (positive) - mapped to PCIe_SS1 only.	IDS	AH13

Table 4-18. PCIe Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
pcie_txn0	PCIe1_PHY_TX Transmit Data Lane 0 (negative) - mapped to PCIe_SS1 only.	ODS	AG14
pcie_txp0	PCIe1_PHY_TX Transmit Data Lane 0 (positive) - mapped to PCIe_SS1 only.	ODS	AH14
pcie_rxn1	PCIe2_PHY_RX Receive Data Lane 1 (negative) - mapped to either PCIe_SS1 (dual lane- mode) or PCIe_SS2 (single lane- mode)	IDS	AF12
pcie_rxp1	PCIe2_PHY_RX Receive Data Lane 1 (positive) - mapped to either PCIe_SS1 (dual lane- mode) or PCIe_SS2 (single lane- mode)	IDS	AE12
pcie_txn1	PCIe2_PHY_TX Transmit Data Lane 1 (negative) - mapped to either PCIe_SS1 (dual lane- mode) or PCIe_SS2 (single lane- mode)	ODS	AC11
pcie_txp1	PCIe2_PHY_TX Transmit Data Lane 1 (positive) - mapped to either PCIe_SS1 (dual lane- mode) or PCIe_SS2 (single lane- mode)	ODS	AD11
ljcb_clkp	PCIe1_PHY shared Reference Clock Input / Output Differential Pair (positive)	IODS	AG15
ljcb_clkn	PCIe1_PHY shared Reference Clock Input / Output Differential Pair (negative)	IODS	AH15

4.4.16 Controller Area Network Interface (DCAN)

NOTE

For more information, see *DCAN* section in the device TRM.

Table 4-19. DCAN Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	BALL
DCAN 1			
dcan1_tx	DCAN1 transmit data pin	IO	G20
dcan1_rx	DCAN1 receive data pin	IO	G19 / AD17
DCAN 2			
dcan2_tx	DCAN2 transmit data pin	IO	E21/ B21
dcan2_rx	DCAN2 receive data pin	IO	F20/ B20/ AC16

4.4.17 Ethernet Interface (GMAC_SW)

CAUTION

The I/O timings provided in Section 7, *Timing Requirements and Switching Characteristics* are valid only if signals within a single IOSET are used. The IOSETs are defined in Table 7-73, Table 7-78 and Table 7-85.

NOTE

For more information, see *Gigabit Ethernet Switch (GMAC_SW)* section in the device TRM.

Table 4-20. GMAC Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	BALL
rgmii0_txc	RGMII0 Transmit Clock	O	W9
rgmii0_txctl	RGMII0 Transmit Enable	O	V9
rgmii0_txd3	RGMII0 Transmit Data	O	V7

Table 4-20. GMAC Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
rgmii0_txd2	RGMII0 Transmit Data	O	U7
rgmii0_txd1	RGMII0 Transmit Data	O	V6
rgmii0_txd0	RGMII0 Transmit Data	O	U6
rgmii0_rxc	RGMII0 Receive Clock	I	U5
rgmii0_rxctl	RGMII0 Receive Control	I	V5
rgmii0_rxd3	RGMII0 Receive Data	I	V4
rgmii0_rxd2	RGMII0 Receive Data	I	V3
rgmii0_rxd1	RGMII0 Receive Data	I	Y2
rgmii0_rxd0	RGMII0 Receive Data	I	W2
rgmii1_txc	RGMII1 Transmit Clock	O	D5
rgmii1_txctl	RGMII1 Transmit Enable	O	C2
rgmii1_txd3	RGMII1 Transmit Data	O	C3
rgmii1_txd2	RGMII1 Transmit Data	O	C4
rgmii1_txd1	RGMII1 Transmit Data	O	B2
rgmii1_txd0	RGMII1 Transmit Data	O	D6
rgmii1_rxc	RGMII1 Receive Clock	I	C5
rgmii1_rxctl	RGMII1 Receive Control	I	A3
rgmii1_rxd3	RGMII1 Receive Data	I	B3
rgmii1_rxd2	RGMII1 Receive Data	I	B4
rgmii1_rxd1	RGMII1 Receive Data	I	B5
rgmii1_rxd0	RGMII1 Receive Data	I	A4
mii1_rxd1	MII1 Receive Data	I	C1
mii1_rxd2	MII1 Receive Data	I	E4
mii1_rxd3	MII1 Receive Data	I	F5
mii1_rxd0	MII1 Receive Data	I	E6
mii1_rxclk	MII1 Receive Clock	I	D5
mii1_rxdv	MII1 Receive Data Valid	I	C2
mii1_txclk	MII1 Transmit Clock	I	C3
mii1_txd0	MII1 Transmit Data	O	C4
mii1_txd1	MII1 Transmit Data	O	B2
mii1_txd2	MII1 Transmit Data	O	D6
mii1_txd3	MII1 Transmit Data	O	C5
mii1_txer	MII1 Transmit Error	I	A3
mii1_rxer	MII1 Receive Data Error	I	B3
mii1_col	MII1 Collision Detect (Sense)	I	B4
mii1_crs	MII1 Carrier Sense	I	B5
mii1_txen	MII1 Transmit Data Enable	O	A4
mii0_rxd1	MII0 Receive Data	I	V6
mii0_rxd2	MII0 Receive Data	I	V9
mii0_rxd3	MII0 Receive Data	I	W9
mii0_rxd0	MII0 Receive Data	I	U6
mii0_rxclk	MII0 Receive Clock	I	Y1
mii0_rxdv	MII0 Receive Data Valid	I	V2
mii0_txclk	MII0 Transmit Clock	I	U5
mii0_txd0	MII0 Transmit Data	O	W2
mii0_txd1	MII0 Transmit Data	O	Y2
mii0_txd2	MII0 Transmit Data	O	V4

Table 4-20. GMAC Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
mii0_txd3	MII0 Transmit Data	O	V5
mii0_txer	MII0 Transmit Error	I	U4
mii0_rxer	MII0 Receive Data Error	I	U7
mii0_col	MII0 Collision Detect (Sense)	I	V1
mii0_crs	MII0 Carrier Sense	I	V7
mii0_txen	MII0 Transmit Data Enable	O	V3
rmii1_crs	RMII1 Carrier Sense	I	V2
rmii1_rxer	RMII1 Receive Data Error	I	Y1
rmii1_rxd1	RMII1 Receive Data	I	W9
rmii1_rxd0	RMII1 Receive Data	I	V9
rmii1_txen	RMII1 Transmit Data Enable	O	U5
rmii1_txd1	RMII1 Transmit Data	O	V5
rmii1_txd0	RMII1 Transmit Data	O	V4
rmii0_crs	RMII0 Carrier Sense	I	V7
rmii0_rxer	RMII0 Receive Data Error	I	U7
rmii0_rxd1	RMII0 Receive Data	I	V6
rmii0_rxd0	RMII0 Receive Data	I	U6
rmii0_txen	RMII0 Transmit Data Enable	O	V3
rmii0_txd1	RMII0 Transmit Data	O	Y2
rmii0_txd0	RMII0 Transmit Data	O	W2
mdio_mclk	Management Data Serial Clock	O	AC5 / V1 / B21 / D3
mdio_d	Management Data	IO	AB4 / U4 / B20 / F6

4.4.18 eMMC/SD/SDIO

NOTE

For more information, see *eMMC/SD/SDIO* chapter in the device TRM.

Table 4-21. eMMC/SD/SDIO Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	BALL
Multi Media Card 1			
mmc1_clk[(1)]	MMC1 clock	IO	W6
mmc1_cmd	MMC1 command	IO	Y6
mmc1_sdcd	MMC1 Card Detect	I	W7
mmc1_sdwp	MMC1 Write Protect	I	Y9
mmc1_dat0	MMC1 data bit 0	IO	AA6
mmc1_dat1	MMC1 data bit 1	IO	Y4
mmc1_dat2	MMC1 data bit 2	IO	AA5
mmc1_dat3	MMC1 data bit 3	IO	Y3
Multi Media Card 2			
mmc2_clk[(1)]	MMC2 clock	IO	J7
mmc2_cmd	MMC2 command	IO	H6
mmc2_sdcd	MMC2 Card Detect	I	G20
mmc2_sdwp	MMC2 Write Protect	I	G19
mmc2_dat0	MMC2 data bit 0	IO	J4
mmc2_dat1	MMC2 data bit 1	IO	J6

Table 4-21. eMMC/SD/SDIO Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
mmc2_dat2	MMC2 data bit 2	IO	H4
mmc2_dat3	MMC2 data bit 3	IO	H5
mmc2_dat4	MMC2 data bit 4	IO	K7
mmc2_dat5	MMC2 data bit 5	IO	M7
mmc2_dat6	MMC2 data bit 6	IO	J5
mmc2_dat7	MMC2 data bit 7	IO	K6
Multi Media Card 3			
mmc3_clk(1)	MMC3 clock	IO	AD4
mmc3_cmd	MMC3 command	IO	AC4
mmc3_sdcd	MMC3 Card Detect	I	B21
mmc3_sdwp	MMC3 Write Protect	I	B20
mmc3_dat0	MMC3 data bit 0	IO	AC7
mmc3_dat1	MMC3 data bit 1	IO	AC6
mmc3_dat2	MMC3 data bit 2	IO	AC9
mmc3_dat3	MMC3 data bit 3	IO	AC3
mmc3_dat4	MMC3 data bit 4	IO	AC8
mmc3_dat5	MMC3 data bit 5	IO	AD6
mmc3_dat6	MMC3 data bit 6	IO	AB8
mmc3_dat7	MMC3 data bit 7	IO	AB5
Multi Media Card 4			
mmc4_clk(1)	MMC4 clock	IO	E25
mmc4_cmd	MMC4 command	IO	C27
mmc4_sdcd	MMC4 Card Detect	I	B27
mmc4_sdwp	MMC4 Write Protect	I	C26
mmc4_dat0	MMC4 data bit 0	IO	D28
mmc4_dat1	MMC4 data bit 1	IO	D26
mmc4_dat2	MMC4 data bit 2	IO	D27
mmc4_dat3	MMC4 data bit 3	IO	C28

(1) By default, this clock signal is implemented as 'pad loopback' inside the device - the output signal is looped back through the input buffer to serve as the internal reference signal. mmc1_clk and mmc2_clk have an optional software programmable setting to use an 'internal loopback clock' instead of the default 'pad loopback clock'. If the 'pad loopback clock' is used, series termination is recommended (as close to device pin as possible) to improve signal integrity of the clock input. Any nonmonotonicity in voltage that occurs at the pad loopback clock pin between V_{IH} and V_{IL} must be less than V_{HYS}.

4.4.19 General-Purpose Interface (GPIO)

NOTE

For more information, see *General-Purpose Interface* chapter in the device TRM.

Table 4-22. GPIOs Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	BALL
GPIO 1			
gpio1_0	General-Purpose Input	I	AD17
gpio1_3	General-Purpose Input	I	AC16
gpio1_4	General-Purpose Input/Output	IO	D15
gpio1_5	General-Purpose Input/Output	IO	A17
gpio1_6	General-Purpose Input/Output	IO	M6
gpio1_7	General-Purpose Input/Output	IO	M2

Table 4-22. GPIOs Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
gpio1_8	General-Purpose Input/Output	IO	L5
gpio1_9	General-Purpose Input/Output	IO	M1
gpio1_10	General-Purpose Input/Output	IO	L6
gpio1_11	General-Purpose Input/Output	IO	L4
gpio1_12	General-Purpose Input/Output	IO	L3
gpio1_13	General-Purpose Input/Output	IO	L2
gpio1_14	General-Purpose Input/Output	IO	G20
gpio1_15	General-Purpose Input/Output	IO	G19
gpio1_16	General-Purpose Input/Output	IO	D27
gpio1_17	General-Purpose Input/Output	IO	C28
gpio1_18	General-Purpose Input/Output	IO	H1
gpio1_19	General-Purpose Input/Output	IO	J3
gpio1_20	General-Purpose Input/Output	IO	H2
gpio1_21	General-Purpose Input/Output	IO	H3
gpio1_22	General-Purpose Input/Output	IO	AC8
gpio1_23	General-Purpose Input/Output	IO	AD6
gpio1_24	General-Purpose Input/Output	IO	AB8
gpio1_25	General-Purpose Input/Output	IO	AB5
gpio1_26	General-Purpose Input/Output	IO	P6
gpio1_27	General-Purpose Input/Output	IO	R9
gpio1_28	General-Purpose Input/Output	IO	R5
gpio1_29	General-Purpose Input/Output	IO	P5
gpio1_30	General-Purpose Input/Output	IO	N7
gpio1_31	General-Purpose Input/Output	IO	R4
GPIO 2			
gpio2_0	General-Purpose Input/Output	IO	N9
gpio2_1	General-Purpose Input/Output	IO	P9
gpio2_2	General-Purpose Input/Output	IO	P4
gpio2_3	General-Purpose Input/Output	IO	R3
gpio2_4	General-Purpose Input/Output	IO	T2
gpio2_5	General-Purpose Input/Output	IO	U2
gpio2_6	General-Purpose Input/Output	IO	U1
gpio2_7	General-Purpose Input/Output	IO	P3
gpio2_8	General-Purpose Input/Output	IO	R2
gpio2_9	General-Purpose Input/Output	IO	K7
gpio2_10	General-Purpose Input/Output	IO	M7
gpio2_11	General-Purpose Input/Output	IO	J5
gpio2_12	General-Purpose Input/Output	IO	K6
gpio2_13	General-Purpose Input/Output	IO	J7
gpio2_14	General-Purpose Input/Output	IO	J4
gpio2_15	General-Purpose Input/Output	IO	J6
gpio2_16	General-Purpose Input/Output	IO	H4
gpio2_17	General-Purpose Input/Output	IO	H5
gpio2_18	General-Purpose Input/Output	IO	H6
gpio2_19	General-Purpose Input/Output	IO	T1
gpio2_20	General-Purpose Input/Output	IO	P2
gpio2_21	General-Purpose Input/Output	IO	P1

Table 4-22. GPIOs Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
gpio2_22	General-Purpose Input/Output	IO	P7
gpio2_23	General-Purpose Input/Output	IO	N1
gpio2_24	General-Purpose Input/Output	IO	M5
gpio2_25	General-Purpose Input/Output	IO	M3
gpio2_26	General-Purpose Input/Output	IO	N6
gpio2_27	General-Purpose Input/Output	IO	M4
gpio2_28	General-Purpose Input/Output	IO	N2
gpio2_29	General-Purpose Input/Output	IO	B17
GPIO 3			
gpio3_28	General-Purpose Input/Output	IO	E1
gpio3_29	General-Purpose Input/Output	IO	G2
gpio3_30	General-Purpose Input/Output	IO	H7
gpio3_31	General-Purpose Input/Output	IO	G1
GPIO 4			
gpio4_0	General-Purpose Input/Output	IO	G6
gpio4_1	General-Purpose Input/Output	IO	F2
gpio4_2	General-Purpose Input/Output	IO	F3
gpio4_3	General-Purpose Input/Output	IO	D1
gpio4_4	General-Purpose Input/Output	IO	E2
gpio4_5	General-Purpose Input/Output	IO	D2
gpio4_6	General-Purpose Input/Output	IO	F4
gpio4_7	General-Purpose Input/Output	IO	C1
gpio4_8	General-Purpose Input/Output	IO	E4
gpio4_9	General-Purpose Input/Output	IO	F5
gpio4_10	General-Purpose Input/Output	IO	E6
gpio4_11	General-Purpose Input/Output	IO	D3
gpio4_12	General-Purpose Input/Output	IO	F6
gpio4_13	General-Purpose Input/Output	IO	D5
gpio4_14	General-Purpose Input/Output	IO	C2
gpio4_15	General-Purpose Input/Output	IO	C3
gpio4_16	General-Purpose Input/Output	IO	C4
gpio4_17	General-Purpose Input/Output	IO	A12
gpio4_18	General-Purpose Input/Output	IO	E14
gpio4_19	General-Purpose Input/Output	IO	D11
gpio4_20	General-Purpose Input/Output	IO	B10
gpio4_21	General-Purpose Input/Output	IO	B11
gpio4_22	General-Purpose Input/Output	IO	C11
gpio4_23	General-Purpose Input/Output	IO	E11
gpio4_24	General-Purpose Input/Output	IO	B2
gpio4_25	General-Purpose Input/Output	IO	D6
gpio4_26	General-Purpose Input/Output	IO	C5
gpio4_27	General-Purpose Input/Output	IO	A3
gpio4_28	General-Purpose Input/Output	IO	B3
gpio4_29	General-Purpose Input/Output	IO	B4
gpio4_30	General-Purpose Input/Output	IO	B5
gpio4_31	General-Purpose Input/Output	IO	A4
GPIO 5			

Table 4-22. GPIOs Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
gpio5_0	General-Purpose Input/Output	IO	B14
gpio5_1	General-Purpose Input/Output	IO	J14
gpio5_2	General-Purpose Input/Output	IO	G12
gpio5_3	General-Purpose Input/Output	IO	F12
gpio5_4	General-Purpose Input/Output	IO	G13
gpio5_5	General-Purpose Input/Output	IO	J11
gpio5_6	General-Purpose Input/Output	IO	E12
gpio5_7	General-Purpose Input/Output	IO	F13
gpio5_8	General-Purpose Input/Output	IO	C12
gpio5_9	General-Purpose Input/Output	IO	D12
gpio5_10	General-Purpose Input/Output	IO	B12
gpio5_11	General-Purpose Input/Output	IO	A11
gpio5_12	General-Purpose Input/Output	IO	B13
gpio5_13	General-Purpose Input/Output	IO	B18
gpio5_14	General-Purpose Input/Output	IO	F15
gpio5_15	General-Purpose Input/Output	IO	V1
gpio5_16	General-Purpose Input/Output	IO	U4
gpio5_17	General-Purpose Input/Output	IO	U3
gpio5_18	General-Purpose Input/Output	IO	V2
gpio5_19	General-Purpose Input/Output	IO	Y1
gpio5_20	General-Purpose Input/Output	IO	W9
gpio5_21	General-Purpose Input/Output	IO	V9
gpio5_22	General-Purpose Input/Output	IO	V7
gpio5_23	General-Purpose Input/Output	IO	U7
gpio5_24	General-Purpose Input/Output	IO	V6
gpio5_25	General-Purpose Input/Output	IO	U6
gpio5_26	General-Purpose Input/Output	IO	U5
gpio5_27	General-Purpose Input/Output	IO	V5
gpio5_28	General-Purpose Input/Output	IO	V4
gpio5_29	General-Purpose Input/Output	IO	V3
gpio5_30	General-Purpose Input/Output	IO	Y2
gpio5_31	General-Purpose Input/Output	IO	W2
GPIO 6			
gpio6_4	General-Purpose Input/Output	IO	A13
gpio6_5	General-Purpose Input/Output	IO	G14
gpio6_6	General-Purpose Input/Output	IO	F14
gpio6_7	General-Purpose Input/Output	IO	B16
gpio6_8	General-Purpose Input/Output	IO	C15
gpio6_9	General-Purpose Input/Output	IO	A16
gpio6_10	General-Purpose Input/Output	IO	AC5
gpio6_11	General-Purpose Input/Output	IO	AB4
gpio6_12	General-Purpose Input/Output	IO	AB10
gpio6_13	General-Purpose Input/Output	IO	AC10
gpio6_14	General-Purpose Input/Output	IO	E21
gpio6_15	General-Purpose Input/Output	IO	F20
gpio6_16	General-Purpose Input/Output	IO	F21
gpio6_17	General-Purpose Input/Output	IO	D18

Table 4-22. GPIOs Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
gpio6_18	General-Purpose Input/Output	IO	E17
gpio6_19	General-Purpose Input/Output	IO	B26
gpio6_20	General-Purpose Input/Output	IO	C23
gpio6_21	General-Purpose Input/Output	IO	W6
gpio6_22	General-Purpose Input/Output	IO	Y6
gpio6_23	General-Purpose Input/Output	IO	AA6
gpio6_24	General-Purpose Input/Output	IO	Y4
gpio6_25	General-Purpose Input/Output	IO	AA5
gpio6_26	General-Purpose Input/Output	IO	Y3
gpio6_27	General-Purpose Input/Output	IO	W7
gpio6_28	General-Purpose Input/Output	IO	Y9
gpio6_29	General-Purpose Input/Output	IO	AD4
gpio6_30	General-Purpose Input/Output	IO	AC4
gpio6_31	General-Purpose Input/Output	IO	AC7
GPIO 7			
gpio7_0	General-Purpose Input/Output	IO	AC6
gpio7_1	General-Purpose Input/Output	IO	AC9
gpio7_2	General-Purpose Input/Output	IO	AC3
gpio7_3	General-Purpose Input/Output	IO	R6
gpio7_4	General-Purpose Input/Output	IO	T9
gpio7_5	General-Purpose Input/Output	IO	T6
gpio7_6	General-Purpose Input/Output	IO	T7
gpio7_7	General-Purpose Input/Output	IO	A25
gpio7_8	General-Purpose Input/Output	IO	F16
gpio7_9	General-Purpose Input/Output	IO	B25
gpio7_10	General-Purpose Input/Output	IO	A24
gpio7_11	General-Purpose Input/Output	IO	A22
gpio7_12	General-Purpose Input/Output	IO	B21
gpio7_13	General-Purpose Input/Output	IO	B20
gpio7_14	General-Purpose Input/Output	IO	A26
gpio7_15	General-Purpose Input/Output	IO	B22
gpio7_16	General-Purpose Input/Output	IO	G17
gpio7_17	General-Purpose Input/Output	IO	B24
gpio7_18	General-Purpose Input/Output	IO	L1
gpio7_19	General-Purpose Input/Output	IO	K2
gpio7_22	General-Purpose Input/Output	IO	B27
gpio7_23	General-Purpose Input/Output	IO	C26
gpio7_24	General-Purpose Input/Output	IO	E25
gpio7_25	General-Purpose Input/Output	IO	C27
gpio7_26	General-Purpose Input/Output	IO	D28
gpio7_27	General-Purpose Input/Output	IO	D26
gpio7_28	General-Purpose Input/Output	IO	J1
gpio7_29	General-Purpose Input/Output	IO	J2
gpio7_30	General-Purpose Input/Output	IO	D14
gpio7_31	General-Purpose Input/Output	IO	C14
GPIO 8			
gpio8_0	General-Purpose Input/Output	IO	F11

Table 4-22. GPIOs Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
gpio8_1	General-Purpose Input/Output	IO	G10
gpio8_2	General-Purpose Input/Output	IO	F10
gpio8_3	General-Purpose Input/Output	IO	G11
gpio8_4	General-Purpose Input/Output	IO	E9
gpio8_5	General-Purpose Input/Output	IO	F9
gpio8_6	General-Purpose Input/Output	IO	F8
gpio8_7	General-Purpose Input/Output	IO	E7
gpio8_8	General-Purpose Input/Output	IO	E8
gpio8_9	General-Purpose Input/Output	IO	D9
gpio8_10	General-Purpose Input/Output	IO	D7
gpio8_11	General-Purpose Input/Output	IO	D8
gpio8_12	General-Purpose Input/Output	IO	A5
gpio8_13	General-Purpose Input/Output	IO	C6
gpio8_14	General-Purpose Input/Output	IO	C8
gpio8_15	General-Purpose Input/Output	IO	C7
gpio8_16	General-Purpose Input/Output	IO	B7
gpio8_17	General-Purpose Input/Output	IO	B8
gpio8_18	General-Purpose Input/Output	IO	A7
gpio8_19	General-Purpose Input/Output	IO	A8
gpio8_20	General-Purpose Input/Output	IO	C9
gpio8_21	General-Purpose Input/Output	IO	A9
gpio8_22	General-Purpose Input/Output	IO	B9
gpio8_23	General-Purpose Input/Output	IO	A10
gpio8_27	General-Purpose Input	I	D23
gpio8_28	General-Purpose Input/Output	IO	F19
gpio8_29	General-Purpose Input/Output	IO	E18
gpio8_30 (1)	General-Purpose Input/Output	IO	G21
gpio8_31 (1)	General-Purpose Input/Output	IO	D24

(1) gpio8_30 is multiplexed with EMU0 and gpio8_31 is multiplexed with EMU1. These pins will be sampled at reset release by the test and emulation logic. Therefore, if they are used as GPIO pins, they must return to the high state whenever the device enters reset. This can be controlled by logic driven from rstoutn. After the device exits reset (indicated by rstoutn rising), these can return to GPIO mode.

4.4.20 Pulse Width Modulation (PWM) Interface

NOTE

For more information, see *Pulse-Width Modulation Subsystem* chapter in the device TRM.

Table 4-23. PWM Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	BALL
PWMSS1			
eQEP1A_in	EQEP1 Quadrature Input A	I	E1
eQEP1B_in	EQEP1 Quadrature Input B	I	G2
eQEP1_index	EQEP1 Index Input	IO	H7
eQEP1_strobe	EQEP1 Strobe Input	IO	G1
ehrpwm1A	EHRPWM1 Output A	O	G6
ehrpwm1B	EHRPWM1 Output B	O	F2
ehrpwm1_tripzone_input	EHRPWM1 Trip Zone Input	IO	AG7 / F3

Table 4-23. PWM Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
eCAP1_in_PWM1_out	ECAP1 Capture Input / PWM Output	IO	AH6 / D1
ehrpwm1_synci	EHRPWM1 Sync Input	I	AH3 / E2
ehrpwm1_synco	EHRPWM1 Sync Output	O	AH5 / D2
PWMSS2			
eQEP2A_in	EQEP2 Quadrature Input A	I	AG6 / F4
eQEP2B_in	EQEP2 Quadrature Input B	I	AH4 / C1
eQEP2_index	EQEP2 Index Input	IO	AG4 / E4
eQEP2_strobe	EQEP2 Strobe Input	IO	F5
ehrpwm2A	EHRPWM2 Output A	O	AC5 / E6
ehrpwm2B	EHRPWM2 Output B	O	AB4 / D3
ehrpwm2_tripzone_input	EHRPWM2 Trip Zone Input	IO	AD4 / F6
eCAP2_in_PWM2_out	ECAP2 Capture Input / PWM Output	IO	AC4 / D5
PWMSS3			
eQEP3A_in	EQEP3 Quadrature Input A	I	AC7 / C2
eQEP3B_in	EQEP3 Quadrature Input B	I	AC6 / C3
eQEP3_index	EQEP3 Index Input	IO	AC9 / C4
eQEP3_strobe	EQEP3 Strobe Input	IO	AC3 / B2
ehrpwm3A	EHRPWM3 Output A	O	AC8 / D6
ehrpwm3B	EHRPWM3 Output B	O	AD6 / C5
ehrpwm3_tripzone_input	EHRPWM3 Trip Zone Input	IO	AB8 / A3
eCAP3_in_PWM3_out	ECAP3 Capture Input / PWM Output	IO	AB5 / B3

4.4.21 Test Interfaces

CAUTION

The I/O timings provided in Section 7, *Timing Requirements and Switching Characteristics* are valid only if signals within a single IOSET are used. The IOSETs are defined in Table 7-136.

NOTE

For more information, see *On-Chip Debug Support* chapter in the device TRM.

Table 4-24. Debug Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	BALL
tms	JTAG® test port mode select. An external pullup resistor should be used on this ball.	IO	F18
tdi	JTAG test data	I	D23
tdo	JTAG test port data	O	F19
tclk	JTAG test clock	I	E20
trstn	JTAG test reset	I	D20
rtck	JTAG return clock	O	E18
emu0(1)	Emulator pin 0	IO	G21
emu1(1)	Emulator pin 1	IO	D24
emu2	Emulator pin 2	O	F10

Table 4-24. Debug Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
emu3	Emulator pin 3	O	D7
emu4	Emulator pin 4	O	A7
emu5	Emulator pin 5	O	E1 / G11
emu6	Emulator pin 6	O	G2 / E9
emu7	Emulator pin 7	O	H7 / F9
emu8	Emulator pin 8	O	G1 / F8
emu9	Emulator pin 9	O	G6 / E7
emu10	Emulator pin 10	O	F2 / D8
emu11	Emulator pin 11	O	F3 / A5
emu12	Emulator pin 12	O	D1 / C6
emu13	Emulator pin 13	O	E2 / C8
emu14	Emulator pin 14	O	D2 / C7
emu15	Emulator pin 15	O	F4 / A8
emu16	Emulator pin 16	O	C1 / C9
emu17	Emulator pin 17	O	E4 / A9
emu18	Emulator pin 18	O	F5 / B9
emu19	Emulator pin 19	O	E6 / A10

(1) EMU0 and EMU1 are multiplexed with GPIO. These pins will be sampled at reset release by the test and emulation logic. Therefore, if they are used as GPIO pins, they must return to the high state whenever the device enters reset. This can be controlled by logic driven from rstoutn. After the device exits reset (indicated by rstoutn rising), these can return to GPIO mode.

4.4.22 System and Miscellaneous

4.4.22.1 Sysboot

NOTE

For more information, see *Initialization* chapter in the device TRM.

Table 4-25. Sysboot Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	BALL
sysboot0	Boot Mode Configuration 0. The value latched on this pin upon porz reset release will determine the boot mode configuration of the device.	I	M6
sysboot1	Boot Mode Configuration 1. The value latched on this pin upon porz reset release will determine the boot mode configuration of the device.	I	M2
sysboot2	Boot Mode Configuration 2. The value latched on this pin upon porz reset release will determine the boot mode configuration of the device.	I	L5
sysboot3	Boot Mode Configuration 3. The value latched on this pin upon porz reset release will determine the boot mode configuration of the device.	I	M1
sysboot4	Boot Mode Configuration 4. The value latched on this pin upon porz reset release will determine the boot mode configuration of the device.	I	L6
sysboot5	Boot Mode Configuration 5. The value latched on this pin upon porz reset release will determine the boot mode configuration of the device.	I	L4
sysboot6	Boot Mode Configuration 6. The value latched on this pin upon porz reset release will determine the boot mode configuration of the device.	I	L3
sysboot7	Boot Mode Configuration 7. The value latched on this pin upon porz reset release will determine the boot mode configuration of the device.	I	L2
sysboot8	Boot Mode Configuration 8. The value latched on this pin upon porz reset release will determine the boot mode configuration of the device.	I	L1
sysboot9	Boot Mode Configuration 9. The value latched on this pin upon porz reset release will determine the boot mode configuration of the device.	I	K2

Table 4-25. Sysboot Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
sysboot10	Boot Mode Configuration 10. The value latched on this pin upon porz reset release will determine the boot mode configuration of the device.	I	J1
sysboot11	Boot Mode Configuration 11. The value latched on this pin upon porz reset release will determine the boot mode configuration of the device.	I	J2
sysboot12	Boot Mode Configuration 12. The value latched on this pin upon porz reset release will determine the boot mode configuration of the device.	I	H1
sysboot13	Boot Mode Configuration 13. The value latched on this pin upon porz reset release will determine the boot mode configuration of the device.	I	J3
sysboot14	Boot Mode Configuration 14. The value latched on this pin upon porz reset release will determine the boot mode configuration of the device.	I	H2
sysboot15	Boot Mode Configuration 15. The value latched on this pin upon porz reset release will determine the boot mode configuration of the device.	I	H3

4.4.22.2 Power, Reset, and Clock Management (PRCM)

NOTE

For more information, see the *Power, Reset, and Clock Management* chapter in the device TRM.

Table 4-26. PRCM Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	BALL
clkout1	Device Clock output 1. Can be used externally for devices with non-critical timing requirements, or for debug, or as a reference clock on GPMC as described in Table 7-25 *GPMC/NOR Flash Interface Switching Characteristics - Synchronous Mode - Default* and Table 7-27 *GPMC/NOR Flash Interface Switching Characteristics - Synchronous Mode - Alternate*.	O	F21 / P7
clkout2	Device Clock output 2. Can be used externally for devices with non-critical timing requirements, or for debug.	O	D18 / N1
clkout3	Device Clock output 3. Can be used xternally for devices with non-critical timing requirements, or for debug.	O	C23
rstoutn	Reset out (Active low) output is asserted low whenever any global reset condition exists. After a brief delay, it will be set high upon removal of the internal global reset condition (that is, porz, warm reset). It is only functional after its output buffer's reference voltage (vddshv3) is valid. If it is used as a reset for device peripheral components, then it should be AND gated with porz to avoid the possibility of reset signal glitches during a power up sequence.(2)	O	F23
resetn	Reset (active low) input's falling edge can trigger a device warm reset state from an external component. This signal should be high prior to or simultaneous with, porz rising. If the signal is not used in the system, resetn should be pulled high with an external pull-up resistor to vddshv3.	I	E23
porz	Power on Reset (active low) input must be asserted low during a device power up sequence or cold reset state when all supplies are disabled. Typically, an external PMIC is the source and sets porz high after all supplies reach valid operating levels. Asserting porz low puts the entire device in a safe reset state.	I	F22
xref_clk0	External Reference Clock 0. For Audio and other Peripherals.	I	D18
xref_clk1	External Reference Clock 1. For Audio and other Peripherals.	I	E17
xref_clk2	External Reference Clock 2. For Audio and other Peripherals.	I	B26
xref_clk3	External Reference Clock 3. For Audio and other Peripherals.	I	C23
xi_osc0	System Oscillator OSC0 Crystal input / LVCMOS clock input. Functions as the input connection to a crystal when the internal oscillator OSC0 is used. Functions as an LVCMOS-compatible input clock when an external oscillator is used.	I	AE15

Table 4-26. PRCM Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
xo_osc0	System Oscillator OSC0 Crystal output	O	AD15
xi_osc1	Auxiliary Oscillator OSC1 Crystal input / LVCMOS clock input. Functions as the input connection to a crystal when the internal oscillator OSC1 is used. Functions as an LVCMOS-compatible input clock when an external oscillator is used.	I	AC15
xo_osc1	Auxiliary Oscillator OSC1 Crystal output	A	AC13
RMII_MHZ_50_CLK(1)	RMII Reference Clock (50MHz). This pin is an input when external reference is used or output when internal reference is used.	IO	U3

(1) This clock signal is implemented as 'pad loopback' inside the device - the output signal is looped back through the input buffer to serve as the internal reference signal. Series termination is recommended (as close to device pin as possible) to improve signal integrity of the clock input. Any nonmonotonicity in voltage that occurs at the pad loopback clock pin between V_{IH} and V_{IL} must be less than V_{HYS}.

(2) Note that rstoutn is only valid after vddshv3 is valid. If the rstoutn signal will be used as a reset into other devices attached to the SOC, it must be AND'ed with porz. This will prevent glitches occurring during supply ramping being propagated.

4.4.22.3 Real-Time Clock (RTC) Interface

NOTE

For more information, see *Real-Time Clock (RTC)* chapter in the device TRM.

Table 4-27. RTC Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	BALL
Wakeup0	RTC External Wakeup Input 0	I	AD17
Wakeup1	RTC External Wakeup Input 1	I	AC17
Wakeup2	RTC External Wakeup Input 2	I	AB16
Wakeup3	RTC External Wakeup Input 3	I	AC16
rtc_porz	RTC Power Domain Power-On Reset Input	I	AB17
rtc_osc_xi_clkin32	RTC Oscillator Input. Crystal connection to internal RTC oscillator. Functions as an RTC clock input when an external oscillator is used.	I	AE14
rtc_osc_xo	RTC Oscillator Output	O	AD14
rtc_iso(1)	RTC Domain Isolation Signal	I	AF14
on_off	RTC Power Enable output pin	O	Y11

(1) This signal must be kept 0 if device power supplies are not valid during RTC mode and 1 during normal operation. This can typically be achieved by connecting rtc_iso to the same signal driving porz (not rtc_porz) with appropriate voltage level translation if necessary.

4.4.22.4 System Direct Memory Access (SDMA)

NOTE

For more information, see *DMA Controllers* chapter in the device TRM.

Table 4-28. System DMA Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	BALL
dma_evt1	System DMA Event Input 1	I	P7 / P4
dma_evt2	System DMA Event Input 2	I	N1 / R3
dma_evt3	System DMA Event Input 3	I	N6
dma_evt4	System DMA Event Input 4	I	M4

4.4.22.5 Interrupt Controllers (INTC)

NOTE
For more information, see *Interrupt Controllers* chapter in the device TRM.

Table 4-29. INTC Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	BALL
nmin_dsp	Non maskable interrupt input, active-low. This pin can be optionally routed to the DSP NMI input or as generic input to the Arm cores. Note that by default this pin has an internal pulldown resistor enabled. This internal pulldown should be disabled or countered by a stronger external pullup resistor before routing to the DSP or Arm processors.	I	D21
sys_nirq2	External interrupt event to any device INTC	I	AD17
sys_nirq1	External interrupt event to any device INTC	I	AC16

4.4.22.6 Observability

NOTE
For more information, see *Control Module* chapter in the device TRM.

Table 4-30. Observability Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	BALL
obs0	Observation Output 0	O	F10
obs1	Observation Output 1	O	G11
obs2	Observation Output 2	O	E9
obs3	Observation Output 3	O	F9
obs4	Observation Output 4	O	F8
obs5	Observation Output 5	O	D7
obs6	Observation Output 6	O	D8
obs7	Observation Output 7	O	A5
obs8	Observation Output 8	O	C6
obs9	Observation Output 9	O	C8
obs10	Observation Output 10	O	C7
obs11	Observation Output 11	O	A7
obs12	Observation Output 12	O	A8
obs13	Observation Output 13	O	C9
obs14	Observation Output 14	O	A9
obs15	Observation Output 15	O	B9
obs16	Observation Output 16	O	F10
obs17	Observation Output 17	O	G11
obs18	Observation Output 18	O	E9
obs19	Observation Output 19	O	F9
obs20	Observation Output 20	O	F8
obs21	Observation Output 21	O	D7
obs22	Observation Output 22	O	D8
obs23	Observation Output 23	O	A5
obs24	Observation Output 24	O	C6
obs25	Observation Output 25	O	C8
obs26	Observation Output 26	O	C7

Table 4-30. Observability Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
obs27	Observation Output 27	O	A7
obs28	Observation Output 28	O	A8
obs29	Observation Output 29	O	C9
obs30	Observation Output 30	O	A9
obs31	Observation Output 31	O	B9
obs_dmarq1	DMA Request External Observation Output 1	O	G11
obs_dmarq2	DMA Request External Observation Output 2	O	D8
obs_irq1	IRQ External Observation Output 1	O	F10
obs_irq2	IRQ External Observation Output 2	O	D7

4.4.23 Power Supplies

NOTE

For more information, see *Power, Reset, and Clock Management* chapter in the device TRM.

Table 4-31. Power Supply Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	BALL
vdd	Core voltage domain supply	PWR	H13 / H14 / J17 / J18 / L7 / L8 / N10 / N13 / P11 / P12 / P13 / R11 / R16 / R19 / T13 / T16 / T19 / U13 / U16 / U8 / U9 / V16 / V8
vpp(2)	eFuse power supply	PWR	K14
vss	Ground	GND	A1 / A14 / A2 / A23 / A28 / A6 / AA14 / AA15 / AA20 / AA8 / AA9 / AB14 / AB20 / AD1 / AD24 / AG1 / AH1 / AH2 / AH20 / AH28 / B1 / D13 / D19 / E13 / E19 / F1 / F7 / G7 / G8 / G9 / H12 / J12 / J15 / J28 / K1 / K15 / K24 / K25 / K4 / K5 / L13 / L14 / M19 / N14 / N15 / N19 / N24 / N25 / P28 / R1 / R12 / R13 / R21 / T10 / T11 / T12 / T14 / T15 / T17 / T18 / T21 / U14 / U15 / U17 / U20 / U21 / V15 / V17 / W1 / W15 / W24 / W25 / W28
cap_vbbldo_gpu(1)	External capacitor connection for the GPU vbb ldo output	CAP	Y14
cap_vbbldo_iva(1)	External capacitor connection for the IVA vbb ldo output	CAP	J10
cap_vbbldo_mpu(1)	External capacitor connection for the MPU vbb ldo output	CAP	J16
cap_vbbldo_dsp(1)	External capacitor connection for the DSP vbb ldo output	CAP	K9
cap_vddram_core1(1)	External capacitor connection for the Core SRAM array ldo1 output	CAP	T20
cap_vddram_core3(1)	External capacitor connection for the Core SRAM array ldo3 output	CAP	L9
cap_vddram_core4(1)	External capacitor connection for the Core SRAM array ldo4 output	CAP	J19
cap_vddram_mpu(1)	External capacitor connection for the MPU SRAM array ldo output	CAP	K19
cap_vddram_gpu(1)	External capacitor connection for the GPU SRAM array ldo output	CAP	Y13

Table 4-31. Power Supply Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
cap_vddram_iva[(1)]	External capacitor connection for the IVA SRAM array ldo output	CAP	K16
cap_vddram_dsp[(1)]	External capacitor connection for the DSP	CAP	J9
vdda_dsp_iva	DSP PLL and IVA PLL analog power supply	PWR	N12
vdda_core_gmac	DPLL_CORE and CORE HSDIVIDER analog power supply	PWR	P14
vdda_pll_spare	DPLL_SPARE analog power supply	PWR	P15
vdda_per	DPLL_ABE, DPLL_PER, and PER HSDIVIDER analog power supply	PWR	M14
vdda_mpu_abe	MPU_ABE PLL analog power supply	PWR	N16
vdda33v_usb1	HS USB1 3.3V analog power supply. If USB1 is not used, this pin can alternatively be connected to VSS if the following requirements are met: - The usb1_dm/usb1_dp pins are left unconnected - The USB1 PHY is kept powered down	PWR	AA12
vdda33v_usb2	HS USB2 3.3V analog power supply. If USB2 is not used, this pin can alternatively be connected to VSS if the following requirements are met: - The usb2_dm/usb2_dp pins are left unconnected - The USB2 PHY is kept powered down	PWR	Y12
vdda_ddr	DPLL_DDR and DDR HSDIVIDER analog power supply	PWR	R17
vdda_debug	DPLL_DEBUG analog power supply	PWR	N11
vdda_gpu	DPLL_GPU analog power supply	PWR	R14
vdda_hdmi	PLL_HDMI and HDMI analog power supply	PWR	Y17
vdda_osc	HFOSC analog power supply	PWR	AD16 / AE16
vdda_pcie	DPLL_PCIe_REF and PCIe analog power supply	PWR	AA17
vdda_pcie0	PCIe ch0 RX/TX analog power supply	PWR	AA16
vdda_rtc	RTC bias and RTC LFOSC analog power supply	PWR	AB13
vdda_sata	DPLL_SATA and SATA RX/TX analog power supply	PWR	V13
vdda_usb1	DPLL_USB and HS USB1 1.8V analog power supply	PWR	AA13
vdda_usb2	HS USB2 1.8V analog power supply	PWR	AB12
vdda_usb3	DPLL_USB_OTG_SS and USB3.0 RX/TX analog power supply	PWR	W14
vdda_csi	CSI Interface 1.8v Supply	PWR	W12
vdda_video	VIDEO1 and VIDEO2 PLL analog power supply	PWR	P16
vdds18v	1.8V power supply	PWR	G18 / H17 / M8 / M9 / N8 / P8 / R8 / T8 / V21 / V22 / W17 / W18
vdds18v_ddr1	EMIF1 bias power supply	PWR	AA18 / AA19 / N21 / P20 / P21 / W21 / Y21
vddshv1	Dual Voltage (1.8V or 3.3V) power supply for the VIN2 Power Group pins	PWR	E3 / E5 / G4 / G5 / H8 / H9
vddshv2	Dual Voltage (1.8V or 3.3V) power supply for the VOUT Power Group pins	PWR	B6 / D10 / E10 / H10 / H11
vddshv3	Dual Voltage (1.8V or 3.3V) power supply for the GENERAL Power Group pins	PWR	B23 / D16 / D22 / E16 / E22 / G15 / H15 / H16 / H18 / H19
vddshv4	Dual Voltage (1.8V or 3.3V) power supply for the MMC4 Power Group pins	PWR	C24
vddshv5	Dual Voltage (1.8V or 3.3V) power supply for the RTC Power Group pins	PWR	V12
vddshv6	Dual Voltage (1.8V or 3.3V) power supply for the VIN1 Power Group pins	PWR	AD5 / AD7 / AE7 / AF5
vddshv7	Dual Voltage (1.8V or 3.3V) power supply for the WIFI Power Group pins	PWR	AB6 / AB7
vddshv8	Dual Voltage (1.8V or 3.3V) power supply for the MMC1 Power Group pins	PWR	W8 / Y8

Table 4-31. Power Supply Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
vddshv9	Dual Voltage (1.8V or 3.3V) power supply for the RGMII Power Group pins	PWR	U10 / W4 / W5
vddshv10	Dual Voltage (1.8V or 3.3V) power supply for the GPMC Power Group pins	PWR	N4 / N5 / P10 / R10 / R7 / T4 / T5
vddshv11	Dual Voltage (1.8V or 3.3V) power supply for the MMC2 Power Group pins	PWR	J8 / K8
vdds_ddr1	EMIF1 power supply (1.5V for DDR3 mode / 1.35V DDR3L mode)	PWR	AA21 / AA22 / AB21 / AB22 / AB24 / AB25 / AC22 / AD26 / AG20 / AG28 / AH27 / T24 / T25 / W16 / W27
vdds_mlbp	MLBP IO power supply	PWR	AA7 / Y7
vdd_dsp	DSP voltage domain supply	PWR	K10 / K11 / L10 / L11 / M10 / M11
vdd_gpu	GPU voltage domain supply	PWR	U11 / U12 / V10 / V11 / V14 / W10 / W11 / W13
vdd_iva	IVA voltage domain supply	PWR	J13 / K12 / K13 / L12 / M12 / M13
vdd_mpu	MPU voltage domain supply	PWR	K17 / K18 / L15 / L16 / L17 / L18 / L19 / M15 / M16 / M17 / M18 / N17 / N18 / P17 / P18 / R18
vdd_rtc	RTC voltage domain supply	PWR	AB15
vssa_hdmi	DPLL_HDMI and HDMI PHY analog ground	GND	AD19 / AE19
vssa_osc0	OSC0 analog ground	GND	AF15
vssa_osc1	OSC1 analog ground	GND	AC14
vssa_pcie	PCIe analog ground	GND	AD13 / AE13
vssa_sata	SATA analog ground	GND	AE10
vssa_usb	HS USB1 and HS USB2 analog ground	GND	AA11 / AB11
vssa_usb3	DPLL_USB and USB3.0 RX/TX analog ground	GND	AD10
vssa_csi	CSI Interface 0v Supply	GND	AA10 / AH8
vssa_video	DPLL_VIDEO1 analog ground	GND	R15

(1) This pin must always be connected via a 1-µF capacitor to vss.

(2) This signal is valid only for High-Security devices. For more details, see Section 5.8 *VPP Specification for One-Time Programmable (OTP) eFUSEs*. For General Purpose devices do not connect any signal, test point, or board trace to this signal.

5 Specifications

NOTE

For more information, see *Power, Reset, and Clock Management* section in the device TRM.

NOTE

The index numbers 1 which is part of the EMIF1 signal prefixes (ddr1_*) listed in Table 4-8, *EMIF SDRAM Signal Descriptions*, column "SIGNAL NAME" not to be confused with DDR1 type of SDRAM memories.

NOTE

Audio Back End (ABE) module is not supported for this family of devices, but “ABE” name is still present in some clock or DPLL names.

CAUTION

All IO Cells are NOT Fail-safe compliant and should not be externally driven in absence of their IO supply.

5.1 Absolute Maximum Ratings

Stresses beyond those listed as absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Section 5.4, *Recommended Operating Conditions*, is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Table 5-1. Absolute Maximum Rating Over Junction Temperature Range

PARAMETER[(1)]			MIN	MAX	UNIT
V_{SUPPLY} (Steady-State)	Supply Voltage Ranges (Steady-State)	Core (vdd, vdd_mpu, vdd_gpu, vdd_dsp, vdd_iva, vdd_rtc)	-0.3	1.5	V
		Analog (vdda_usb1, vdda_usb2, vdda_per, vdda_ddr, vdda_debug, vdda_mpu_abe, vdda_usb3, vdda_csi, vdda_core_gmac, vdda_pll_spare, vdda_dsp_iva, vdda_gpu, dda_hdmi, vdda_pcie, vdda_pcie0, vdda_sata, vdda_video, vdda_osc, vdda_rtc)	-0.3	2.0	V
		Analog 3.3V (vdda33v_usb1, vdda33v_usb2)	-0.3	3.8	V
		vdds18v, vdds18v_ddr1, vdds_mlbp, vdds_ddr1	-0.3	2.1	V
		vddshv1-11 (1.8V mode)	-0.3	2.1	V
		vddshv1-7 (3.3V mode), vddshv9-11 (3.3V mode)	-0.3	3.8	V
		vddshv8 (3.3V mode)	-0.3	3.6	V

Table 5-1. Absolute Maximum Rating Over Junction Temperature Range (continued)

PARAMETER(1)			MIN	MAX	UNIT
V_{IO} (Steady-State)	Input and Output Voltage Ranges (Steady-State)	Core I/Os	-0.3	1.5	V
		Analog I/Os (except HDMI)	-0.3	2.0	V
		HDMI I/Os	-0.3	3.5	V
		I/O 1.35V	-0.3	1.65	V
		I/O 1.5V	-0.3	1.8	V
		1.8V I/Os	-0.3	2.1	V
		3.3V I/Os (except those powered by vddshv8)	-0.3	3.8	V
		3.3V I/Os (powered by vddshv8)	-0.3	3.6	V
SR	Maximum slew rate, all supplies			10^5	V/s
V_{IO} (Transient Overshoot / Undershoot)	Input and Output Voltage Ranges (Transient Overshoot/Undershoot) Note: valid for up to 20% of the signal period. See Figure 5-1, *IO Transient Voltage Ranges*.			0.2*VDD (2)	V
T_J	Operating junction temperature range	Automotive	-40	+125	°C
T_{STG}	Storage temperature range after soldered onto PC Board		-55	+150	°C
Latch-up I-Test	I-test(3), All I/Os (if different then one line per level)		-100	100	mA
Latch-up OV-Test	Over-voltage Test(4), All supplies (if different levels then one line per level)		N/A	1.5*Vsupply max	V

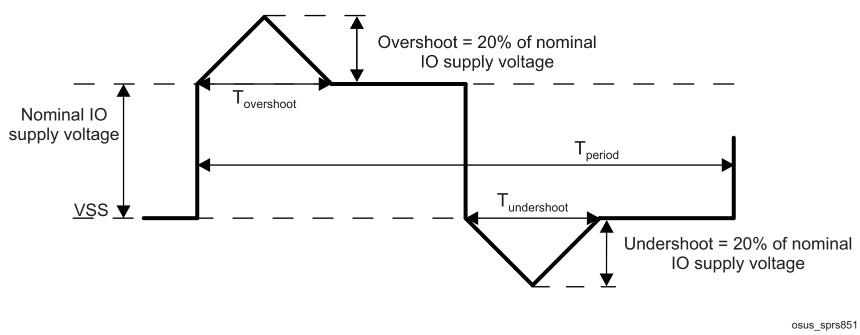
(1) See I/Os supplied by this power pin in Table 4-2 *Ball Characteristics*

(2) VDD is the voltage on the corresponding power-supply pin(s) for the IO.

(3) Per JEDEC JESD78 at 125°C with specified I/O pin injection current and clamp voltage of 1.5 times maximum recommended I/O voltage and negative 0.5 times maximum recommended I/O voltage.

(4) Per JEDEC JESD78 at 125°C.

(5) The maximum valid input voltage on an IO pin cannot exceed 0.3 volts when the supply powering the IO is turned off. This requirement applies to all the IO pins which are not fail-safe and for all values of IO supply voltage. Special attention should be applied anytime peripheral devices are not powered from the same power sources used to power the respective IO supply. It is important the attached peripheral never sources a voltage outside the valid input voltage range, including power supply ramp-up and ramp-down sequences.



(1) $T_{overshoot} + T_{undershoot} < 20\%$ of T_{period}

Figure 5-1. IO Transient Voltage Ranges

5.2 ESD Ratings

Table 5-2. ESD Ratings

			VALUE	UNIT
V_{ESD} Electrostatic discharge	Human-Body model (HBM), per AEC Q100-002[(1)]		±1000	V
	Charged-device model (CDM), per AEC Q100-011	HDMIPHY Pins (AG16, AH16, AG19, AH19, AG18, AH18, AG17, AH17)	±200	
		All Pins (other than HDMIPHY)	±250	
		Corner pins (A1, AH1, A28, AH28)	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Power-On-Hour (POH) Limits

The information in the section below is provided solely for your convenience and does not extend or modify the warranty provided under TI's standard terms and conditions for TI semiconductor products.

NOTE

POH is a functional of voltage, temperature and time. Usage at higher voltages and temperatures will result in a reduction in POH to achieve the same reliability performance. For assessment of alternate use cases, contact your local TI representative.

Table 5-3. Power-On-Hour (POH) Limits

IP	DUTY CYCLE	VOLTAGE DOMAIN	VOLTAGE (V) (MAX)	FREQUENCY (MHz) (MAX)	Tj(°C)	POH
All	100%	All	All Supported OPPs		Automotive Profile[(1)]	20000

(1) Automotive profile is defined as 20000 power on hours with junction temperature as follows: 5%@-40°C, 65%@70°C, 20%@110°C, 10%@125°C.

5.4 Recommended Operating Conditions

The device is used under the recommended operating conditions described in Table 5-4.

NOTE

Logic functions and parameter values are not assured out of the range specified in the recommended operating conditions.

Table 5-4. Recommended Operating Conditions

PARAMETER	DESCRIPTION	MIN [(2)]	NOM	MAX DC [(3)]	MAX [(2)]	UNIT
Input Power Supply Voltage Range						
vdd	Core voltage domain supply	See Section 5.5				V
vdd_mpu	Supply voltage range for MPU domain	See Section 5.5				V
vdd_gpu	GPU voltage domain supply	See Section 5.5				V
vdd_dsp	DSP voltage domain supply	See Section 5.5				V
vdd_iva	IVA voltage domain supply	See Section 5.5				V
vdd_rtc	RTC voltage domain supply	See Section 5.5				V

Table 5-4. Recommended Operating Conditions (continued)

PARAMETER	DESCRIPTION	MIN [2]	NOM	MAX DC [3]	MAX [2]	UNIT
vdda_usb1	DPLL_USB and HS USB1 1.8V analog power supply	1.71	1.80	1.836	1.89	V
	Maximum noise (peak-peak)		50			mV_{PPmax}
vdda_usb2	HS USB2 1.8V analog power supply	1.71	1.80	1.836	1.89	V
	Maximum noise (peak-peak)		50			mV_{PPmax}
vdda33v_usb1	HS USB1 3.3V analog power supply.If USB1 is not used, this pin can alternatively be connected to VSS if the following requirements are met: - The usb1_dm/usb1_dp pins are left unconnected - The USB1 PHY is kept powered down	3.135	3.3	3.366	3.465	V
	Maximum noise (peak-peak)		50			mV_{PPmax}
vdda33v_usb2	HS USB2 3.3V analog power supply. If USB2 is not used, this pin can alternatively be connected to VSS if the following requirements are met: - The usb2_dm/usb2_dp pins are left unconnected - The USB2 PHY is kept powered down	3.135	3.3	3.366	3.465	V
	Maximum noise (peak-peak)		50			mV_{PPmax}
vdda_per	PER PLL and PER HSDIVIDER analog power supply	1.71	1.80	1.836	1.89	V
	Maximum noise (peak-peak)		50			mV_{PPmax}
vdda_ddr	DPLL_DDR and DDR HSDIVIDER analog power supply	1.71	1.80	1.836	1.89	V
	Maximum noise (peak-peak)		50			mV_{PPmax}
vdda_debug	DPLL_DEBUG analog power supply	1.71	1.80	1.836	1.89	V
	Maximum noise (peak-peak)		50			mV_{PPmax}
vdda_dsp_iva	DPLL_DSP and DPLL_IVA analog power supply	1.71	1.80	1.836	1.89	V
	Maximum noise (peak-peak)		50			mV_{PPmax}
vdda_core_gmac	DPLL_CORE and CORE HSDIVIDER analog power supply	1.71	1.80	1.836	1.89	V
	Maximum noise (peak-peak)		50			mV_{PPmax}
vdda_pll_spare	DPLL_SPARE analog power supply	1.71	1.80	1.836	1.89	V
	Maximum noise (peak-peak)		50			mV_{PPmax}
vdda_gpu	DPLL_GPU analog power supply	1.71	1.80	1.836	1.89	V
	Maximum noise (peak-peak)		50			mV_{PPmax}
vdda_hdmi	PLL_HDMI and HDMI analog power supply	1.71	1.80	1.836	1.89	V
	Maximum noise (peak-peak)		50			mV_{PPmax}
vdda_pcie	DPLL_PCIe_REF and PCIe analog power supply	1.71	1.80	1.836	1.89	V
	Maximum noise (peak-peak)		50			mV_{PPmax}
vdda_pcie0	PCIe ch0 RX/TX analog power supply	1.71	1.80		1.89	V
	Maximum noise (peak-peak)		50			mV_{PPmax}
vdda_sata	DPLL_SATA and SATA RX/TX analog power supply	1.71	1.80	1.836	1.89	V
	Maximum noise (peak-peak)		50			mV_{PPmax}
vdda_usb3	DPLL_USB_OTG_SS and USB3.0 RX/TX analog power supply	1.71	1.80	1.836	1.89	V
	Maximum noise (peak-peak)		50			mV_{PPmax}

Table 5-4. Recommended Operating Conditions (continued)

PARAMETER	DESCRIPTION		MIN [2]	NOM	MAX DC [3]	MAX [2]	UNIT
vdda_video	DPLL_VIDEO1 analog power supply		1.71	1.80	1.836	1.89	V
	Maximum noise (peak-peak)			50			mV_{PPmax}
vdds_mlbp	MLBP IO power supply		1.71	1.80		1.89	V
	Maximum noise (peak-peak)			50			mV_{PPmax}
vdda_mpu_abe	DPLL_MPU analog power supply		1.71	1.80	1.836	1.89	V
	Maximum noise (peak-peak)			50			mV_{PPmax}
vdda_osc	HFOSC analog power supply		1.71	1.80		1.89	V
	Maximum noise (peak-peak)			50			mV_{PPmax}
vdda_rtc	RTC bias and RTC LFOSC analog power supply		1.71	1.80		1.89	V
	Maximum noise (peak-peak)			50			mV_{PPmax}
vdda_csi	CSI Interface 1.8v Supply		1.71	1.80	1.836	1.89	V
	Maximum noise (peak-peak)			50			mV_{PPmax}
vdds18v	1.8V power supply		1.71	1.80	1.836	1.89	V
	Maximum noise (peak-peak)			50			mV_{PPmax}
vdds18v_ddr1	EMIF1 bias power supply		1.71	1.80	1.836	1.89	V
	Maximum noise (peak-peak)			50			mV_{PPmax}
vdds_ddr1	EMIF1 power supply (1.5V for DDR3 mode / 1.35V DDR3L mode)	1.35-V Mode	1.28	1.35	1.377	1.42	V
		1.5-V Mode	1.43	1.50	1.53	1.57	
	Maximum noise (peak-peak)	1.35-V Mode		50			mV_{PPmax}
		1.5-V Mode					
vddshv5	Dual Voltage (1.8V or 3.3V) power supply for the RTC Power Group pins	1.8-V Mode	1.71	1.80	1.836	1.89	V
		3.3-V Mode	3.135	3.30	3.366	3.465	
	Maximum noise (peak-peak)	1.8-V Mode		50			mV_{PPmax}
		3.3-V Mode					
vddshv1	Dual Voltage (1.8V or 3.3V) power supply for the VIN2 Power Group pins	1.8-V Mode	1.71	1.80	1.836	1.89	V
		3.3-V Mode	3.135	3.30	3.366	3.465	
	Maximum noise (peak-peak)	1.8-V Mode		50			mV_{PPmax}
		3.3-V Mode					
vddshv10	Dual Voltage (1.8V or 3.3V) power supply for the GPMC Power Group pins	1.8-V Mode	1.71	1.80	1.836	1.89	V
		3.3-V Mode	3.135	3.30	3.366	3.465	
	Maximum noise (peak-peak)	1.8-V Mode		50			mV_{PPmax}
		3.3-V Mode					
vddshv11	Dual Voltage (1.8V or 3.3V) power supply for the MMC2 Power Group pins	1.8-V Mode	1.71	1.80	1.836	1.89	V
		3.3-V Mode	3.135	3.30	3.366	3.465	
	Maximum noise (peak-peak)	1.8-V Mode		50			mV_{PPmax}
		3.3-V Mode					
vddshv2	Dual Voltage (1.8V or 3.3V) power supply for the VOUT Power Group pins	1.8-V Mode	1.71	1.80	1.836	1.89	V
		3.3-V Mode	3.135	3.30	3.366	3.465	
	Maximum noise (peak-peak)	1.8-V Mode		50			mV_{PPmax}
		3.3-V Mode					

Table 5-4. Recommended Operating Conditions (continued)

PARAMETER	DESCRIPTION		MIN [(2)]	NOM	MAX DC [(3)]	MAX [(2)]	UNIT
vddshv3	Dual Voltage (1.8V or 3.3V) power supply for the GENERAL Power Group pins	1.8-V Mode	1.71	1.80	1.836	1.89	V
		3.3-V Mode	3.135	3.30	3.366	3.465	
	Maximum noise (peak-peak)	1.8-V Mode		50			mV_{PPmax}
		3.3-V Mode					
vddshv4	Dual Voltage (1.8V or 3.3V) power supply for the MMC4 Power Group pins	1.8-V Mode	1.71	1.80	1.836	1.89	V
		3.3-V Mode	3.135	3.30	3.366	3.465	
	Maximum noise (peak-peak)	1.8-V Mode		50			mV_{PPmax}
		3.3-V Mode					
vddshv6	Dual Voltage (1.8V or 3.3V) power supply for the VIN1 Power Group pins	1.8-V Mode	1.71	1.80	1.836	1.89	V
		3.3-V Mode	3.135	3.30	3.366	3.465	
	Maximum noise (peak-peak)	1.8-V Mode		50			mV_{PPmax}
		3.3-V Mode					
vddshv7	Dual Voltage (1.8V or 3.3V) power supply for the WIFI Power Group pins	1.8-V Mode	1.71	1.80	1.836	1.89	V
		3.3-V Mode	3.135	3.30	3.366	3.465	
	Maximum noise (peak-peak)	1.8-V Mode		50			mV_{PPmax}
		3.3-V Mode					
vddshv8	Dual Voltage (1.8V or 3.3V) power supply for the MMC1 Power Group pins	1.8-V Mode	1.71	1.80	1.836	1.89	V
		3.3-V Mode	3.135	3.30	3.366	3.465	
	Maximum noise (peak-peak)	1.8-V Mode		50			mV_{PPmax}
		3.3-V Mode					
vddshv9	Dual Voltage (1.8V or 3.3V) power supply for the RGMII Power Group pins	1.8-V Mode	1.71	1.80	1.836	1.89	V
		3.3-V Mode	3.135	3.30	3.366	3.465	
	Maximum noise (peak-peak)	1.8-V Mode		50			mV_{PPmax}
		3.3-V Mode					
vss	Ground supply			0			V
vssa_hdmi	DPLL_HDMI and HDMI PHY analog ground			0			V
vssa_pcie	PCIe analog ground			0			V
vssa_usb	HS USB1 and HS USB2 analog ground			0			V
vssa_usb3	DPLL_USB and USB3.0 RX/TX analog ground			0			V
vssa_csi	CSI Interface 0v Supply			0			V
vssa_sata	SATA TX ground			0			V
vssa_video	DPLL_VIDEO1 analog ground			0			V
vssa_osc0	OSC0 analog ground			0			V
vssa_osc1	OSC1 analog ground			0			V
T_J [(1)]	Operating junction temperature range	Automotive	-40			125[(4)]	°C
ddr1_vref0	Reference Power Supply EMIF1			0.5*vdds_ddr1			V

(1) Refer to Power-On-Hour (POH) table Table 5-3 for limitations.
(2) The voltage at the device ball should never be below the MIN voltage or above the MAX voltage for any amount of time. This requirement includes dynamic voltage events such as AC ripple, voltage transients, voltage dips, etc.
(3) The DC voltage at the device ball should never be above the MAX DC voltage to avoid impact on device reliability and lifetime POH (Power-On-Hours). The MAX DC voltage is defined as the highest allowed DC regulated voltage, without transients, seen at the ball.
(4) The TSHUT feature of the SoC resets the device by default when one of the on-die temp sensors reports 123 °C. This is intended to protect the device from exceeding 125 °C. Though not recommended, the TSHUT temperature threshold can be modified in software if other mechanisms are in place to avoid exceeding 125 °C. Refer to the device TRM for details on the TSHUT feature.

5.5 Operating Performance Points

This section describes the operating conditions of the device. This section also contains the description of each Operating Performance Point (OPP) for processor clocks and device core clocks.

Table 5-5 describes the maximum supported frequency per speed grade for TDA2Ex devices.

Table 5-5. Speed Grade Maximum Frequency

DEVICE	MAXIMUM FREQUENCY (MHz)						
	MPU	DSP	IVA	GPU	IPU	L3	DDR3/DDR3L
TDA2ExxH	800	750	532	532	212.8	266	667 (DDR3-1333)
TDA2ExxD	500	500	430	500	212.8	266	667 (DDR3-1333)

(1) N/A stands for Not Applicable.

5.5.1 AVS and ABB Requirements

Adaptive Voltage Scaling (AVS) and Adaptive Body Biasing (ABB) are required on most of the vdd_* supplies as defined in Table 5-6.

Table 5-6. AVS and ABB Requirements per vdd_* Supply

SUPPLY	AVS REQUIRED?	ABB REQUIRED?
vdd_core	Yes, for all OPPs	No
vdd_mpu	Yes, for all OPPs	Yes, for all OPPs
vdd_iva	Yes, for all OPPs	Yes, for all OPPs
vdd_dsp	Yes, for all OPPs	Yes, for all OPPs
vdd_gpu	Yes, for all OPPs	Yes, for all OPPs

5.5.2 Voltage And Core Clock Specifications

Table 5-7 shows the recommended OPP per voltage domain.

Table 5-7. Voltage Domains Operating Performance Points [(1)]

DOMAIN	CONDITION	OPP_NOM			OPP_OD			OPP_HIGH			
		MIN [(3)]	NOM [(2)]	MAX [(3)]	MIN [(3)]	NOM [(2)]	MAX [(3)]	MIN [(3)]	NOM [(2)]	MAX DC [(4)]	MAX [(3)]
VD_CORE (V)	BOOT (Before AVS is enabled) [(5)]	1.11	1.15	1.2	Not Applicable			Not Applicable			
	After AVS is enabled [(5)]	AVS Voltage [(6)] – 3.5%	AVS Voltage [(6)]	1.2	Not Applicable			Not Applicable			

Table 5-7. Voltage Domains Operating Performance Points [(1)](#) (continued)

DOMAIN	CONDITION	OPP_NOM			OPP_OD			OPP_HIGH			
		MIN [(3)]	NOM [(2)]	MAX [(3)]	MIN [(3)]	NOM [(2)]	MAX [(3)]	MIN [(3)]	NOM [(2)]	MAX DC [(4)]	MAX [(3)]
VD_MPU (V)	BOOT (Before AVS is enabled) [(5)]	1.11	1.15	1.2	Not Applicable			Not Applicable			
	After AVS is enabled [(5)]	AVS Voltage [(6)] – 3.5%	AVS Voltage [(6)]	1.2	AVS Voltage [(6)] – 3.5%	AVS Voltage [(6)]	AVS Voltage [(6)] + 5%	AVS Voltage [(6)] – 3.5%	AVS Voltage [(6)]	AVS Voltage [(6)] +2%	AVS Voltage [(6)] + 5%
VD_RTC (V) [(7)]	-	0.84	0.88 to 1.06	1.2	Not Applicable			Not Applicable			
Others (V)	BOOT (Before AVS is enabled) [(5)]	1.02	1.06	1.2	Not Applicable			Not Applicable			
	After AVS is enabled [(5)]	AVS Voltage [(6)] – 3.5%	AVS Voltage [(6)]	1.2	AVS Voltage [(6)] – 3.5%	AVS Voltage [(6)]	AVS Voltage [(6)] + 5%	AVS Voltage [(6)] – 3.5%	AVS Voltage [(6)]	AVS Voltage [(6)] +2%	AVS Voltage [(6)] + 5%

(1) The voltage ranges in this table are preliminary, and final voltage ranges may be different than shown. Systems should be designed with the ability to modify the voltage to comply with future recommendations.

(2) In a typical implementation, the power supply should target the NOM voltage.

(3) The voltage at the device ball should never be below the MIN voltage or above the MAX voltage for any amount of time. This requirement includes dynamic voltage events such as AC ripple, voltage transients, voltage dips, etc.

(4) The DC voltage at the device ball should never be above the MAX DC voltage to avoid impact on device reliability and lifetime POH (Power-On-Hours). The MAX DC voltage is defined as the highest allowed DC regulated voltage, without transients, seen at the ball.

(5) For all OPPs, AVS must be enabled to avoid impact on device reliability, lifetime POH (Power-On-Hours), and device power.

(6) The AVS voltages are device-dependent, voltage domain-dependent, and OPP-dependent. They must be read from the STD_FUSE_OPP Registers. For information about STD_FUSE_OPP Registers address, please refer to the *Control Module* chapter of the device TRM. The power supply should be adjustable over the following ranges for each required OPP:

– OPP_NOM for MPU: 0.85 V – 1.15 V
– OPP_NOM for CORE and Others: 0.85 V - 1.15 V
– OPP_OD: 0.94 V - 1.15 V
– OPP_HIGH: 1.01 V - 1.25 V

The AVS voltages will be within the above specified ranges.

(7) VD_RTC can optionally be tied to VD_CORE and operate at the VD_CORE AVS voltages.

(8) The power supply must be programmed with the AVS voltages for the MPU and the CORE voltage domain, either just after the ROM boot or at the earliest possible time in the secondary boot loader before there is significant activity seen on these domains.

Table 5-8 describes the standard processor clocks speed characteristics vs OPP of the device.

Table 5-8. Supported OPP vs Max Frequency [(2)]

CLOCK	OPP_NOM	OPP_OD	OPP_HIGH
	MAXIMUM FREQUENCY (MHz)	MAXIMUM FREQUENCY (MHz)	MAXIMUM FREQUENCY (MHz)
VD_MPU			
MPU_CLK	800	800	800
VD_DSP			
DSP_CLK	600	700	750
VD_IVA			
IVA_GCLK	388.3	430	532
VD_GPU			
GPU_CLK	425.6	500	532
VD_CORE			
CORE_IPU1_CLK	212.8	N/A	N/A
L3_CLK	266	N/A	N/A

Table 5-8. Supported OPP vs Max Frequency (2) (continued)

CLOCK	OPP_NOM	OPP_OD	OPP_HIGH
	MAXIMUM FREQUENCY (MHz)	MAXIMUM FREQUENCY (MHz)	MAXIMUM FREQUENCY (MHz)
DDR3 / DDR3L	667 (DDR3-1333)	N/A	N/A
VD_RTC			
RTC_FCLK	0.034	N/A	N/A

(1) N/A stands for Not Applicable.

(2) Maximum supported frequency is limited to the device speed grade (see Table 5-5, Speed Grade Maximum Frequency).

5.5.3 Maximum Supported Frequency

Device modules either receive their clock directly from an external clock input, directly from a PLL, or from a PRCM. Table 5-9 lists the clock source options for each module on this device, along with the maximum frequency that module can accept. To ensure proper module functionality, the device PLLs and dividers must be programmed not to exceed the maximum frequencies listed in this table.

Table 5-9. Maximum Supported Frequency

MODULE				CLOCK SOURCE		
INSTANCE NAME	INPUT CLOCK NAME	CLOCK TYPE	MAX. CLOCK ALLOWED (MHz)	PRCM CLOCK NAME	PLL / OSC / SOURCE CLOCK NAME	PLL / OSC / SOURCE NAME
AES1	AES1_L3_CLK	Int	266	L4SEC_L3_GICLK	CORE_X2_CLK	DPLL_CORE
AES2	AES2_L3_CLK	Int	266	L4SEC_L3_GICLK	CORE_X2_CLK	DPLL_CORE
ATL	ATL_ICLK_L3	Int	266	ATL_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	ATLPCLK	Func	266	ATL_GFCLK	CORE_X2_CLK	DPLL_CORE
					PER_ABE_X1_GFCLK	DPLL_ABE
					FUNC_32K_CLK	OSC0
					HDMI_CLK	DPLL_HDMI
					VIDEO1_CLK	DPLL_VIDEO1
BB2D	BB2D_FCLK	Func	354.6	BB2D_GFCLK	BB2D_GFCLK	DPLL_CORE
	BB2D_ICLK	Int	266	DSS_L3_GICLK	CORE_X2_CLK	DPLL_CORE
COUNTER_32K	COUNTER_32K_FCLK	Func	0.032	FUNC_32K_CLK	SYS_CLK1/610	OSC0
	COUNTER_32K_ICLK	Int	38.4	WKUPAON_GICLK	SYS_CLK1	OSC0
					DPLL_ABE_X2_CLK	DPLL_ABE
CTRL_MODULE_BANDGAP	L3INSTR_TS_GCLK	Int	4.8	L3INSTR_TS_GCLK	SYS_CLK1	OSC0
					DPLL_ABE_X2_CLK	DPLL_ABE
CTRL_MODULE_CORE	L4CFG_L4_GICLK	Int	133	L4CFG_L4_GICLK	CORE_X2_CLK	DPLL_CORE
CTRL_MODULE_WKUP	WKUPAON_GICLK	Int	38.4	WKUPAON_GICLK	SYS_CLK1	OSC0
					DPLL_ABE_X2_CLK	DPLL_ABE
DCAN1	DCAN1_FCLK	Func	38.4	DCAN1_SYS_CLK	SYS_CLK1	OSC0
					SYS_CLK2	OSC1
	DCAN1_ICLK	Int	266	WKUPAON_GICLK	SYS_CLK1	OSC0
					DPLL_ABE_X2_CLK	DPLL_ABE
DCAN2	DCAN2_FCLK	Func	38.4	DCAN2_SYS_CLK	SYS_CLK1	OSC0
	DCAN2_ICLK	Int	266	L4PER2_L3_GICLK	CORE_X2_CLK	DPLL_CORE

Table 5-9. Maximum Supported Frequency (continued)

MODULE				CLOCK SOURCE		
INSTANCE NAME	**INPUT CLOCK NAME**	**CLOCK TYPE**	**MAX. CLOCK ALLOWED (MHz)**	**PRCM CLOCK NAME**	**PLL / OSC / SOURCE CLOCK NAME**	**PLL / OSC / SOURCE NAME**
DES3DES	DES_CLK_L3	Int	266	L4SEC_L3_GICLK	CORE_X2_CLK	DPLL_CORE
DLL	EMIF_DLL_FCLK	Func	EMIF_DLL_FCLK	EMIF_DLL_GCLK	EMIF_DLL_GCLK	DPLL_DDR
DLL_AGING	FCLK	Int	38.4	L3INSTR_DLL_AGING_GCLK	SYS_CLK1	OSC0
					DPLL_ABE_X2_CLK	DPLL_ABE
DMA_CRYPTO	DMA_CRYPTO_FCLK	Int & Func	266	L4SEC_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	DMA_CRYPTO_ICLK	Int	133	L4SEC_L4_GICLK	CORE_X2_CLK	DPLL_CORE
DMM	DMM_CLK	Int	266	EMIF_L3_GICLK	CORE_X2_CLK	DPLL_CORE
DPLL_DEBUG	SYSCLK	Int	38.4	EMU_SYS_CLK	SYS_CLK1	OSC0
DSP1	DSP1_FICLK	Int & Func	DSP_CLK	DSP1_GFCLK	DSP_GFCLK	DPLL_DSP
DSS	DSS_HDMI_CEC_CLK	Func	0.032	HDMI_CEC_GFCLK	SYS_CLK1/610	OSC0
	DSS_HDMI_PHY_CLK	Func	48	HDMI_PHY_GFCLK	FUNC_192M_CLK	DPLL_PER
	DSS_CLK	Func	192	DSS_GFCLK	DSS_CLK	DPLL_PER
	HDMI_CLKINP	Func	38.4	HDMI_DPLL_CLK	SYS_CLK1	OSC0
					SYS_CLK2	OSC1
	DSS_L3_ICLK	Int	266	DSS_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	VIDEO1_CLKINP	Func	38.4	VIDEO1_DPLL_CLK	SYS_CLK1	OSC0
					SYS_CLK2	OSC1
	VIDEO2_CLKINP	Func	38.4	VIDEO2_DPLL_CLK	SYS_CLK1	OSC0
					SYS_CLK2	OSC1
	DPLL_DSI1_A_CLK1	Func	209.3	N/A	HDMI_CLK	DPLL_HDMI
					VIDEO1_CLKOUT1	DPLL_VIDEO1
	DPLL_DSI1_B_CLK1	Func	209.3	N/A	VIDEO1_CLKOUT3	DPLL_VIDEO1
					HDMI_CLK	DPLL_HDMI
					DPLL_ABE_X2_CLK	DPLL_ABE
	DPLL_DSI1_C_CLK1	Func	209.3	N/A	HDMI_CLK	DPLL_HDMI
					VIDEO1_CLKOUT3	DPLL_VIDEO1
	DPLL_HDMI_CLK1	Func	185.6	N/A	HDMI_CLK	DPLL_HDMI

Table 5-9. Maximum Supported Frequency (continued)

MODULE				CLOCK SOURCE		
INSTANCE NAME	INPUT CLOCK NAME	CLOCK TYPE	MAX. CLOCK ALLOWED (MHz)	PRCM CLOCK NAME	PLL / OSC / SOURCE CLOCK NAME	PLL / OSC / SOURCE NAME
DSS DISPC	LCD1_CLK	Func	209.3	N/A	DPLL_DSI1_A_CLK1	See DSS data in the rows above
					DSS_CLK	
	LCD2_CLK	Func	209.3	N/A	DPLL_DSI1_B_CLK1	
					DSS_CLK	
	LCD3_CLK	Func	209.3	N/A	DPLL_DSI1_C_CLK1	
					DSS_CLK	
	F_CLK	Func	209.3	N/A	DPLL_DSI1_A_CLK1	
					DPLL_DSI1_B_CLK1	
					DPLL_DSI1_C_CLK1	
					DSS_CLK	
					DPLL_HDMI_CLK1	
EFUSE_CTRL_CUST	ocp_clk	Int	133	CUSTEFUSE_L4_GICLK	CORE_X2_CLK	DPLL_CORE
	sys_clk	Func	38.4	CUSTEFUSE_SYS_GFCLK	SYS_CLK1	OSC0
ELM	ELM_ICLK	Int	266	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE
EMIF_OCP_FW	L3_CLK	Int	266	EMIF_L3_GICLK	CORE_X2_CLK	DPLL_CORE
EMIF_PHY1	EMIF_PHY1_FCLK	Func	DDR	EMIF_PHY_GCLK	EMIF_PHY_GCLK	DPLL_DDR
EMIF1	EMIF1_ICLK	Int	266	EMIF_L3_GICLK	CORE_X2_CLK	DPLL_CORE
FPKA	PKA_CLK	Int & Func	266	L4SEC_L3_GICLK	CORE_X2_CLK	DPLL_CORE
GMAC_SW	CPTS_RFT_CLK	Func	266	GMAC_RFT_CLK	PER_ABE_X1_GFCLK	DPLL_ABE
					VIDEO1_CLK	DPLL_VIDEO1
					HDMI_CLK	DPLL_HDMI
					CORE_X2_CLK	DPLL_CORE
	MAIN_CLK	Int	125	GMAC_MAIN_CLK	GMAC_250M_CLK	DPLL_GMAC
	MHZ_250_CLK	Func	250	GMII_250MHZ_CLK	GMII_250MHZ_CLK	DPLL_GMAC
	MHZ_5_CLK	Func	5	RGMII_5MHZ_CLK	GMAC_RMII_HS_CLK	DPLL_GMAC
	MHZ_50_CLK	Func	50	RMII_50MHZ_CLK	GMAC_RMII_HS_CLK	DPLL_GMAC
	RMII1_MHZ_50_CLK	Func	50	RMII_50MHZ_CLK	GMAC_RMII_HS_CLK	DPLL_GMAC
	RMII2_MHZ_50_CLK	Func	50	RMII_50MHZ_CLK	GMAC_RMII_HS_CLK	DPLL_GMAC
GPIO1	GPIO1_ICLK	Int	38.4	WKUPAON_GICLK	SYS_CLK1	OSC0
					DPLL_ABE_X2_CLK	DPLL_ABE
	GPIO1_DBCLK	Func	0.032	WKUPAON_SYS_GFCLK	FUNC_32K_CLK	OSC0
GPIO2	GPIO2_ICLK	Int	266	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	GPIO2_DBCLK	Func	0.032	GPIO_GFCLK	FUNC_32K_CLK	OSC0

Table 5-9. Maximum Supported Frequency (continued)

MODULE				CLOCK SOURCE		
INSTANCE NAME	INPUT CLOCK NAME	CLOCK TYPE	MAX. CLOCK ALLOWED (MHz)	PRCM CLOCK NAME	PLL / OSC / SOURCE CLOCK NAME	PLL / OSC / SOURCE NAME
GPIO3	GPIO3_ICLK	Int	266	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	GPIO3_DBCLK	Func	0.032	GPIO_GFCLK	FUNC_32K_CLK	OSC0
GPIO4	GPIO4_ICLK	Int	266	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	GPIO4_DBCLK	Func	0.032	GPIO_GFCLK	FUNC_32K_CLK	OSC0
	PIDBCLK	Func	0.032	GPIO_GFCLK		
GPIO5	GPIO5_ICLK	Int	266	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	GPIO5_DBCLK	Func	0.032	GPIO_GFCLK	FUNC_32K_CLK	OSC0
	PIDBCLK	Func	0.032	GPIO_GFCLK		
GPIO6	GPIO6_ICLK	Int	266	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	GPIO6_DBCLK	Func	0.032	GPIO_GFCLK	FUNC_32K_CLK	OSC0
	PIDBCLK	Func	0.032	GPIO_GFCLK		
GPIO7	GPIO7_ICLK	Int	266	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	GPIO7_DBCLK	Func	0.032	GPIO_GFCLK	FUNC_32K_CLK	OSC0
	PIDBCLK	Func	0.032	GPIO_GFCLK		
GPIO8	GPIO8_ICLK	Int	266	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	GPIO8_DBCLK	Func	0.032	GPIO_GFCLK	FUNC_32K_CLK	OSC0
	PIDBCLK	Func	0.032	GPIO_GFCLK		
GPMC	GPMC_FCLK	Int	266	L3MAIN1_L3_GICLK	CORE_X2_CLK	DPLL_CORE
GPU	GPU_FCLK1	Func	GPU_CLK	GPU_CORE_GCLK	CORE_GPU_CLK	DPLL_CORE
					PER_GPU_CLK	DPLL_PER
					GPU_GCLK	DPLL_GPU
	GPU_FCLK2	Func	GPU_CLK	GPU_HYD_GCLK	CORE_GPU_CLK	DPLL_CORE
					PER_GPU_CLK	DPLL_PER
					GPU_GCLK	DPLL_GPU
	GPU_ICLK	Int	266	GPU_L3_GICLK	CORE_X2_CLK	DPLL_CORE
HDMI PHY	DSS_HDMI_PHY_CLK	Func	38.4	HDMI_PHY_GFCLK	FUNC_192M_CLK	DPLL_PER
HDQ1W	HDQ1W_ICLK	Int & Func	266	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	HDQ1W_FCLK	Func	12	PER_12M_GFCLK	FUNC_192M_CLK	DPLL_PER
I2C1	I2C1_ICLK	Int	266	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	I2C1_FCLK	Func	96	PER_96M_GFCLK	FUNC_192M_CLK	DPLL_PER
I2C2	I2C2_ICLK	Int	266	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	I2C2_FCLK	Func	96	PER_96M_GFCLK	FUNC_192M_CLK	DPLL_PER
I2C3	I2C3_ICLK	Int	266	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	I2C3_FCLK	Func	96	PER_96M_GFCLK	FUNC_192M_CLK	DPLL_PER
I2C4	I2C4_ICLK	Int	266	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	I2C4_FCLK	Func	96	PER_96M_GFCLK	FUNC_192M_CLK	DPLL_PER
I2C5	I2C5_ICLK	Int	266	IPU_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	I2C5_FCLK	Func	96	IPU_96M_GFCLK	FUNC_192M_CLK	DPLL_PER
I2C6	I2C6_ICLK	Int	266	L4PER2_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	I2C6_FCLK	Func	96	IPU_96M_GFCLK	FUNC_192M_CLK	DPLL_PER
IEEE1500_2_OCP	PI_L3CLK	Int & Func	266	L3INIT_L3_GICLK	CORE_X2_CLK	DPLL_CORE

Table 5-9. Maximum Supported Frequency (continued)

MODULE				CLOCK SOURCE		
INSTANCE NAME	INPUT CLOCK NAME	CLOCK TYPE	MAX. CLOCK ALLOWED (MHz)	PRCM CLOCK NAME	PLL / OSC / SOURCE CLOCK NAME	PLL / OSC / SOURCE NAME
IPU1	IPU1_GFCLK	Int & Func	425.6	IPU1_GFCLK	DPLL_ABE_X2_CLK	DPLL_ABE
					CORE_IPU_ISS_BOOST_CLK	DPLL_CORE
IPU2	IPU2_GFCLK	Int & Func	425.6	IPU2_GFCLK	CORE_IPU_ISS_BOOST_CLK	DPLL_CORE
IVA	IVA_GCLK	Int	IVA_GCLK	IVA_GCLK	IVA_GFCLK	DPLL_IVA
KBD	KBD_FCLK	Func	0.032	WKUPAON_SYS_GFCLK	FUNC_32K_CLK	OSC0
	PICLKKBD	Func	0.032	WKUPAON_SYS_GFCLK		
	KBD_ICLK	Int	38.4	WKUPAON_GICLK	SYS_CLK1	OSC0
	PICLKOCP	Int	38.4	WKUPAON_GICLK	DPLL_ABE_X2_CLK	DPLL_ABE
L3_INSTR	L3_CLK	Int	L3_CLK	L3INSTR_L3_GICLK	CORE_X2_CLK	DPLL_CORE
L3_MAIN	L3_CLK1	Int	L3_CLK	L3MAIN1_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	L3_CLK2	Int	L3_CLK	L3INSTR_L3_GICLK	CORE_X2_CLK	DPLL_CORE
L4_CFG	L4_CFG_CLK	Int	133	L4CFG_L3_GICLK	CORE_X2_CLK	DPLL_CORE
L4_PER1	L4_PER1_CLK	Int	133	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE
L4_PER2	L4_PER2_CLK	Int	133	L4PER2_L3_GICLK	CORE_X2_CLK	DPLL_CORE
L4_PER3	L4_PER3_CLK	Int	133	L4PER3_L3_GICLK	CORE_X2_CLK	DPLL_CORE
L4_WKUP	L4_WKUP_CLK	Int	38.4	WKUPAON_GICLK	SYS_CLK1	OSC0
					DPLL_ABE_X2_CLK	DPLL_ABE
MAILBOX1	MAILBOX1_FLCK	Int	266	L4CFG_L3_GICLK	CORE_X2_CLK	DPLL_CORE
MAILBOX2	MAILBOX2_FLCK	Int	266	L4CFG_L3_GICLK	CORE_X2_CLK	DPLL_CORE
MAILBOX3	MAILBOX3_FLCK	Int	266	L4CFG_L3_GICLK	CORE_X2_CLK	DPLL_CORE
MAILBOX4	MAILBOX4_FLCK	Int	266	L4CFG_L3_GICLK	CORE_X2_CLK	DPLL_CORE
MAILBOX5	MAILBOX5_FLCK	Int	266	L4CFG_L3_GICLK	CORE_X2_CLK	DPLL_CORE
MAILBOX6	MAILBOX6_FLCK	Int	266	L4CFG_L3_GICLK	CORE_X2_CLK	DPLL_CORE
MAILBOX7	MAILBOX7_FLCK	Int	266	L4CFG_L3_GICLK	CORE_X2_CLK	DPLL_CORE
MAILBOX8	MAILBOX8_FLCK	Int	266	L4CFG_L3_GICLK	CORE_X2_CLK	DPLL_CORE
MAILBOX9	MAILBOX9_FLCK	Int	266	L4CFG_L3_GICLK	CORE_X2_CLK	DPLL_CORE
MAILBOX10	MAILBOX10_FLCK	Int	266	L4CFG_L3_GICLK	CORE_X2_CLK	DPLL_CORE
MAILBOX11	MAILBOX11_FLCK	Int	266	L4CFG_L3_GICLK	CORE_X2_CLK	DPLL_CORE
MAILBOX12	MAILBOX12_FLCK	Int	266	L4CFG_L3_GICLK	CORE_X2_CLK	DPLL_CORE
MAILBOX13	MAILBOX13_FLCK	Int	266	L4CFG_L3_GICLK	CORE_X2_CLK	DPLL_CORE

Table 5-9. Maximum Supported Frequency (continued)

MODULE				CLOCK SOURCE		
INSTANCE NAME	INPUT CLOCK NAME	CLOCK TYPE	MAX. CLOCK ALLOWED (MHz)	PRCM CLOCK NAME	PLL / OSC / SOURCE CLOCK NAME	PLL / OSC / SOURCE NAME
MCASP1	MCASP1_AHCLKR	Func	100	MCASP1_AHCLKR	ABE_24M_GFCLK	DPLL_ABE
					ABE_SYS_CLK	OSC0
					FUNC_24M_GFCLK	DPLL_PER
					ATL_CLK0	Module ATL
					ATL_CLK1	Module ATL
					ATL_CLK2	Module ATL
					ATL_CLK3	Module ATL
					SYS_CLK2	OSC1
					XREF_CLK0	XREF_CLK0
					XREF_CLK1	XREF_CLK1
					XREF_CLK2	XREF_CLK2
					XREF_CLK3	XREF_CLK3
					MLB_CLK	Module MLB
					MLBP_CLK	Module MLB
	MCASP1_AHCLKX	Func	100	MCASP1_AHCLKX	ABE_24M_GFCLK	DPLL_ABE
					ABE_SYS_CLK	OSC0
					FUNC_24M_GFCLK	DPLL_PER
					ATL_CLK0	Module ATL
					ATL_CLK1	Module ATL
					ATL_CLK2	Module ATL
					ATL_CLK3	Module ATL
					SYS_CLK2	OSC1
					XREF_CLK0	XREF_CLK0
					XREF_CLK1	XREF_CLK1
					XREF_CLK2	XREF_CLK2
					XREF_CLK3	XREF_CLK3
					MLB_CLK	Module MLB
					MLBP_CLK	Module MLB
	MCASP1_FCLK	Func	192	MCASP1_AUX_GFCLK	PER_ABE_X1_GFCLK	DPLL_ABE
					VIDEO1_CLK	DPLL_VIDEO1
					HDMI_CLK	DPLL_HDMI
	MCASP1_ICLK	Int	266	IPU_L3_GICLK	CORE_X2_CLK	DPLL_CORE

Table 5-9. Maximum Supported Frequency (continued)

MODULE				CLOCK SOURCE		
INSTANCE NAME	INPUT CLOCK NAME	CLOCK TYPE	MAX. CLOCK ALLOWED (MHz)	PRCM CLOCK NAME	PLL / OSC / SOURCE CLOCK NAME	PLL / OSC / SOURCE NAME
MCASP2	MCASP2_AHCLKR	Func	100	MCASP2_AHCLKR	ABE_24M_GFCLK	DPLL_ABE
					ABE_SYS_CLK	OSC0
					FUNC_24M_GFCLK	DPLL_PER
					ATL_CLK3	Module ATL
					ATL_CLK2	Module ATL
					ATL_CLK1	Module ATL
					ATL_CLK0	Module ATL
					SYS_CLK2	OSC1
					XREF_CLK0	XREF_CLK0
					XREF_CLK1	XREF_CLK1
					XREF_CLK2	XREF_CLK2
					XREF_CLK3	XREF_CLK3
					MLB_CLK	Module MLB
					MLBP_CLK	Module MLB
	MCASP2_AHCLKX	Func	100	MCASP2_AHCLKX	ABE_24M_GFCLK	DPLL_ABE
					ABE_SYS_CLK	OSC0
					FUNC_24M_GFCLK	DPLL_PER
					ATL_CLK3	Module ATL
					ATL_CLK2	Module ATL
					ATL_CLK1	Module ATL
					ATL_CLK0	Module ATL
					SYS_CLK2	OSC1
					XREF_CLK0	XREF_CLK0
					XREF_CLK1	XREF_CLK1
					XREF_CLK2	XREF_CLK2
					XREF_CLK3	XREF_CLK3
					MLB_CLK	Module MLB
					MLBP_CLK	Module MLB
	MCASP2_FCLK	Func	192	MCASP2_AUX_GFCLK	PER_ABE_X1_GFCLK	DPLL_ABE
					VIDEO1_CLK	DPLL_VIDEO1
					HDMI_CLK	DPLL_HDMI
	MCASP2_ICLK	Int	266	L4PER2_L3_GICLK	CORE_X2_CLK	DPLL_CORE

Table 5-9. Maximum Supported Frequency (continued)

MODULE				CLOCK SOURCE		
INSTANCE NAME	INPUT CLOCK NAME	CLOCK TYPE	MAX. CLOCK ALLOWED (MHz)	PRCM CLOCK NAME	PLL / OSC / SOURCE CLOCK NAME	PLL / OSC / SOURCE NAME
MCASP3	MCASP3_AHCLKX	Func	100	MCASP3_AHCLKX	ABE_24M_GFCLK	DPLL_ABE
					ABE_SYS_CLK	OSC0
					FUNC_24M_GFCLK	DPLL_PER
					ATL_CLK3	Module ATL
					ATL_CLK2	Module ATL
					ATL_CLK1	Module ATL
					ATL_CLK0	Module ATL
					SYS_CLK2	OSC1
					XREF_CLK0	XREF_CLK0
					XREF_CLK1	XREF_CLK1
					XREF_CLK2	XREF_CLK2
					XREF_CLK3	XREF_CLK3
					MLB_CLK	Module MLB
					MLBP_CLK	Module MLB
	MCASP3_FCLK	Func	192	MCASP3_AUX_GFCLK	PER_ABE_X1_GFCLK	DPLL_ABE
					VIDEO1_CLK	DPLL_ABE
					HDMI_CLK	DPLL_HDMI
	MCASP3_ICLK	Int	266	L4PER2_L3_GICLK	CORE_X2_CLK	DPLL_CORE
MCASP4	MCASP4_AHCLKX	Func	100	MCASP4_AHCLKX	ABE_24M_GFCLK	DPLL_ABE
					ABE_SYS_CLK	OSC0
					FUNC_24M_GFCLK	DPLL_PER
					ATL_CLK3	Module ATL
					ATL_CLK2	Module ATL
					ATL_CLK1	Module ATL
					ATL_CLK0	Module ATL
					SYS_CLK2	OSC1
					XREF_CLK0	XREF_CLK0
					XREF_CLK1	XREF_CLK1
					XREF_CLK2	XREF_CLK2
					XREF_CLK3	XREF_CLK3
					MLB_CLK	Module MLB
					MLBP_CLK	Module MLB
	MCASP4_FCLK	Func	192	MCASP4_AUX_GFCLK	PER_ABE_X1_GFCLK	DPLL_ABE
					VIDEO1_CLK	DPLL_ABE
					HDMI_CLK	DPLL_HDMI
	MCASP4_ICLK	Int	266	L4PER2_L3_GICLK	CORE_X2_CLK	DPLL_CORE

Table 5-9. Maximum Supported Frequency (continued)

MODULE				CLOCK SOURCE		
INSTANCE NAME	INPUT CLOCK NAME	CLOCK TYPE	MAX. CLOCK ALLOWED (MHz)	PRCM CLOCK NAME	PLL / OSC / SOURCE CLOCK NAME	PLL / OSC / SOURCE NAME
MCASP5	MCASP5_AHCLKX	Func	100	MCASP5_AHCLKX	ABE_24M_GFCLK	DPLL_ABE
					ABE_SYS_CLK	OSC0
					FUNC_24M_GFCLK	DPLL_PER
					ATL_CLK3	Module ATL
					ATL_CLK2	Module ATL
					ATL_CLK1	Module ATL
					ATL_CLK0	Module ATL
					SYS_CLK2	OSC1
					XREF_CLK0	XREF_CLK0
					XREF_CLK1	XREF_CLK1
					XREF_CLK2	XREF_CLK2
					XREF_CLK3	XREF_CLK3
					MLB_CLK	Module MLB
					MLBP_CLK	Module MLB
	MCASP5_FCLK	Func	192	MCASP5_AUX_GFCLK	PER_ABE_X1_GFCLK	DPLL_ABE
					VIDEO1_CLK	DPLL_ABE
					HDMI_CLK	DPLL_HDMI
	MCASP5_ICLK	Int	266	L4PER2_L3_GICLK	CORE_X2_CLK	DPLL_CORE
MCASP6	MCASP6_AHCLKX	Func	100	MCASP6_AHCLKX	ABE_24M_GFCLK	DPLL_ABE
					FUNC_24M_GFCLK	DPLL_PER
					ATL_CLK3	Module ATL
					ATL_CLK2	Module ATL
					ATL_CLK1	Module ATL
					ATL_CLK0	Module ATL
					MLB_CLK	Module MLB
					MLBP_CLK	Module MLB
					ABE_SYS_CLK	OSC0
					SYS_CLK2	OSC1
					XREF_CLK0	XREF_CLK0
					XREF_CLK1	XREF_CLK1
					XREF_CLK2	XREF_CLK2
					XREF_CLK3	XREF_CLK3
	MCASP6_FCLK	Func	192	MCASP6_AUX_GFCLK	PER_ABE_X1_GFCLK	DPLL_ABE
					VIDEO1_CLK	DPLL_ABE
					HDMI_CLK	DPLL_HDMI
	MCASP6_ICLK	Int	266	L4PER2_L3_GICLK	CORE_X2_CLK	DPLL_CORE

Table 5-9. Maximum Supported Frequency (continued)

MODULE				CLOCK SOURCE		
INSTANCE NAME	INPUT CLOCK NAME	CLOCK TYPE	MAX. CLOCK ALLOWED (MHz)	PRCM CLOCK NAME	PLL / OSC / SOURCE CLOCK NAME	PLL / OSC / SOURCE NAME
MCASP7	MCASP7_AHCLKX	Func	100	MCASP7_AHCLKX	ABE_24M_GFCLK	DPLL_ABE
					ABE_SYS_CLK	OSC0
					FUNC_24M_GFCLK	DPLL_PER
					ATL_CLK3	Module ATL
					ATL_CLK2	Module ATL
					ATL_CLK1	Module ATL
					ATL_CLK0	Module ATL
					SYS_CLK2	OSC1
					XREF_CLK0	XREF_CLK0
					XREF_CLK1	XREF_CLK1
					XREF_CLK2	XREF_CLK2
					XREF_CLK3	XREF_CLK3
					MLB_CLK	Module MLB
					MLBP_CLK	Module MLB
	MCASP7_FCLK	Func	192	MCASP7_AUX_GFCLK	PER_ABE_X1_GFCLK	DPLL_ABE
					VIDEO1_CLK	DPLL_ABE
					HDMI_CLK	DPLL_HDMI
	MCASP7_ICLK	Int	266	L4PER2_L3_GICLK	CORE_X2_CLK	DPLL_CORE
MCASP8	MCASP8_AHCLKX	Func	100	MCASP8_AHCLKX	ABE_24M_GFCLK	DPLL_ABE
					ABE_SYS_CLK	OSC0
					FUNC_24M_GFCLK	DPLL_PER
					ATL_CLK3	Module ATL
					ATL_CLK2	Module ATL
					ATL_CLK1	Module ATL
					ATL_CLK0	Module ATL
					SYS_CLK2	OSC1
					XREF_CLK0	XREF_CLK0
					XREF_CLK1	XREF_CLK1
					XREF_CLK2	XREF_CLK2
					XREF_CLK3	XREF_CLK3
					MLB_CLK	Module MLB
					MLBP_CLK	Module MLB
	MCASP8_FCLK	Func	192	MCASP8_AUX_GFCLK	PER_ABE_X1_GFCLK	DPLL_ABE
					VIDEO1_CLK	DPLL_ABE
					HDMI_CLK	DPLL_HDMI
	MCASP8_ICLK	Int	266	L4PER2_L3_GICLK	CORE_X2_CLK	DPLL_CORE
MCSPI1	SPI1_ICLK	Int	266	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	SPI1_FCLK	Func	48	PER_48M_GFCLK	PER_48M_GFCLK	DPLL_PER
MCSPI2	SPI2_ICLK	Int	266	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	SPI2_FCLK	Func	48	PER_48M_GFCLK	PER_48M_GFCLK	DPLL_PER
MCSPI3	SPI3_ICLK	Int	266	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	SPI3_FCLK	Func	48	PER_48M_GFCLK	PER_48M_GFCLK	DPLL_PER

Table 5-9. Maximum Supported Frequency (continued)

MODULE				CLOCK SOURCE		
INSTANCE NAME	INPUT CLOCK NAME	CLOCK TYPE	MAX. CLOCK ALLOWED (MHz)	PRCM CLOCK NAME	PLL / OSC / SOURCE CLOCK NAME	PLL / OSC / SOURCE NAME
MCSPI4	SPI4_ICLK	Int	266	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	SPI4_FCLK	Func	48	PER_48M_GFCLK	PER_48M_GFCLK	DPLL_PER
MLB_SS	MLB_L3_ICLK	Int	266	MLB_SHB_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	MLB_L4_ICLK	Int	133	MLB_SPB_L4_GICLK	CORE_X2_CLK	DPLL_CORE
	MLB_FCLK	Func	266	MLB_SYS_L3_GFCLK	CORE_X2_CLK	DPLL_CORE
CSI2_0	CTRLCLK	Int & Func	96	LVDSRX_96M_GFCLK	FUNC_192M_CLK	DPLL_PER
	CAL_FCLK	Int & Func	266	CAL_GICLK	CORE_ISS_MAIN_CLK	DPLL_CORE
					L3_ICLK	CM_CORE_AON
CSI2_1	CTRLCLK	Int & Func	96	LVDSRX_96M_GFCLK	FUNC_192M_CLK	DPLL_PER
	CAL_FCLK	Int & Func	266	CAL_GICLK	CORE_ISS_MAIN_CLK	DPLL_CORE
					L3_ICLK	CM_CORE_AON
MMC1	MMC1_CLK_32K	Func	0.032	L3INIT_32K_GFCLK	FUNC_32K_CLK	OSC0
	MMC1_FCLK	Func	192	MMC1_GFCLK	FUNC_192M_CLK	DPLL_PER
			128		FUNC_256M_CLK	DPLL_PER
	MMC1_ICLK1	Int	266	L3INIT_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	MMC1_ICLK2	Int	133	L3INIT_L4_GICLK	CORE_X2_CLK	DPLL_CORE
MMC2	MMC2_CLK_32K	Func	0.032	L3INIT_32K_GFCLK	FUNC_32K_CLK	OSC0
	MMC2_FCLK	Func	192	MMC2_GFCLK	FUNC_192M_CLK	DPLL_PER
			128		FUNC_256M_CLK	DPLL_PER
	MMC2_ICLK1	Int	266	L3INIT_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	MMC2_ICLK2	Int	133	L3INIT_L4_GICLK	CORE_X2_CLK	DPLL_CORE
MMC3	MMC3_ICLK	Int	266	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	MMC3_CLK_32K	Func	0.032	L4PER_32K_GFCLK	FUNC_32K_CLK	OSC0
	MMC3_FCLK	Func	48	MMC3_GFCLK	FUNC_192M_CLK	DPLL_PER
			192			
MMC4	MMC4_ICLK	Int	266	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	MMC4_CLK_32K	Func	0.032	L4PER_32K_GFCLK	FUNC_32K_CLK	OSC0
	MMC4_FCLK	Func	48	MMC4_GFCLK	FUNC_192M_CLK	DPLL_PER
			192			
MMU_EDMA	MMU1_CLK	Int	266	L3MAIN1_L3_GICLK	CORE_X2_CLK	DPLL_CORE
MMU_PCIESS	MMU2_CLK	Int	266	L3MAIN1_L3_GICLK	CORE_X2_CLK	DPLL_CORE
MPU	MPU_CLK	Int & Func	MPU_CLK	MPU_GCLK	MPU_GCLK	DPLL_MPU
MPU_EMU_DBG	FCLK	Int	38.4	EMU_SYS_CLK	SYS_CLK1	OSC0
					MPU_GCLK	DPLL_MPU
OCMC_RAM1	OCMC1_L3_CLK	Int	266	L3MAIN1_L3_GICLK	CORE_X2_CLK	DPLL_CORE
OCMC_ROM	OCMC_L3_CLK	Int	266	L3MAIN1_L3_GICLK	CORE_X2_CLK	DPLL_CORE
OCP_WP_NOC	PICLKOCPL3	Int	266	L3INSTR_L3_GICLK	CORE_X2_CLK	DPLL_CORE
OCP2SCP1	L4CFG1_ADAPTER_CLKIN	Int	133	L3INIT_L4_GICLK	CORE_X2_CLK	DPLL_CORE
OCP2SCP2	L4CFG2_ADAPTER_CLKIN	Int	133	L4CFG_L4_GICLK	CORE_X2_CLK	DPLL_CORE

Table 5-9. Maximum Supported Frequency (continued)

MODULE				CLOCK SOURCE		
INSTANCE NAME	INPUT CLOCK NAME	CLOCK TYPE	MAX. CLOCK ALLOWED (MHz)	PRCM CLOCK NAME	PLL / OSC / SOURCE CLOCK NAME	PLL / OSC / SOURCE NAME
OCP2SCP3	L4CFG3_ADAPTER_CLKIN	Int	133	L3INIT_L4_GICLK	CORE_X2_CLK	DPLL_CORE
PCIESS1	PCIE1_PHY_WKUP_CLK	Func	0.032	PCIE_32K_GFCLK	FUNC_32K_CLK	OSC0
	PCIe_SS1_FICLK	Int & Func	266	PCIE_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	PCIEPHY_CLK	Func	2500	PCIE_PHY_GCLK	PCIE_PHY_GCLK	APLL_PCIE
	PCIEPHY_CLK_DIV	Func	1250	PCIE_PHY_DIV_GCLK	PCIE_PHY_DIV_GCLK	APLL_PCIE
	PCIE1_REF_CLKIN	Func	34.3	PCIE_REF_GFCLK	CORE_USB_OTG_SS_LFPS_TX_CLK	DPLL_CORE
	PCIE1_PWR_CLK	Func	38.4	PCIE_SYS_GFCLK	SYS_CLK1	OSC0
PCIESS2	PCIE2_PHY_WKUP_CLK	Func	0.032	PCIE_32K_GFCLK	FUNC_32K_CLK	OSC0
	PCIe_SS2_FICLK	Int & Func	266	PCIE_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	PCIEPHY_CLK	Func	2500	PCIE_PHY_GCLK	PCIE_PHY_GCLK	APLL_PCIE
	PCIEPHY_CLK_DIV	Func	1250	PCIE_PHY_DIV_GCLK	PCIE_PHY_DIV_GCLK	APLL_PCIE
	PCIE2_REF_CLKIN	Func	34.3	PCIE_REF_GFCLK	CORE_USB_OTG_SS_LFPS_TX_CLK	DPLL_CORE
	PCIE2_PWR_CLK	Func	38.4	PCIE_SYS_GFCLK	SYS_CLK1	OSC0
PRCM_MPU	32K_CLK	Func	0.032	FUNC_32K_CLK	SYS_CLK1/610	OSC0
	SYS_CLK	Func	38.4	WKUPAON_ICLK	SYS_CLK1	OSC0
					DPLL_ABE_X2_CLK	DPLL_ABE
PWMSS1	PWMSS1_GICLK	Int & Func	266	L4PER2_L3_GICLK	CORE_X2_CLK	DPLL_CORE
PWMSS2	PWMSS2_GICLK	Int & Func	266	L4PER2_L3_GICLK	CORE_X2_CLK	DPLL_CORE
PWMSS3	PWMSS3_GICLK	Int & Func	266	L4PER2_L3_GICLK	CORE_X2_CLK	DPLL_CORE
QSPI	QSPI_ICLK	Int	266	L4PER2_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	QSPI_FCLK	Func	128	QSPI_GFCLK	FUNC_256M_CLK	DPLL_PER
					PER_QSPI_CLK	DPLL_PER
RNG	RNG_ICLK	Int	266	L4SEC_L3_GICLK	CORE_X2_CLK	DPLL_CORE
RTC_SS	RTC_ICLK	Int	133	RTC_L4_GICLK	CORE_X2_CLK	DPLL_CORE
	RTC_FCLK	Func	RTC_FCLK	RTC_AUX_CLK	rtc_osc_xi_clkin32	RTC Oscillator
				FUNC_32K_CLK	SYS_CLK1/610	OSC0
SAR_ROM	PRCM_ROM_CLOCK	Int	266	L4CFG_L3_GICLK	CORE_X2_CLK	DPLL_CORE
SATA	SATA_FICLK	Int	266	L3INIT_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	SATA_PMALIVE_FCLK	Func	48	L3INIT_48M_GFCLK	FUNC_192M_CLK	DPLL_PER
	REF_CLK	Func	38	SATA_REF_GFCLK	SYS_CLK1	OSC0
SDMA	SDMA_FCLK	Int & Func	266	DMA_L3_GICLK	CORE_X2_CLK	DPLL_CORE
SHA2MD51	SHAM_1_CLK	Int	266	L4SEC_L3_GICLK	CORE_X2_CLK	DPLL_CORE
SHA2MD52	SHAM_2_CLK	Int	266	L4SEC_L3_GICLK	CORE_X2_CLK	DPLL_CORE
SL2	IVA_GCLK	Int	IVA_GCLK	IVA_GCLK	IVA_GFCLK	DPLL_IVA

Table 5-9. Maximum Supported Frequency (continued)

MODULE				CLOCK SOURCE		
INSTANCE NAME	INPUT CLOCK NAME	CLOCK TYPE	MAX. CLOCK ALLOWED (MHz)	PRCM CLOCK NAME	PLL / OSC / SOURCE CLOCK NAME	PLL / OSC / SOURCE NAME
SMARTREFLEX_CORE	MCLK	Int	133	COREAON_L4_GICLK	CORE_X2_CLK	DPLL_CORE
	SYSCLK	Func	38.4	WKUPAON_ICLK	SYS_CLK1	OSC0
					DPLL_ABE_X2_CLK	DPLL_ABE
SMARTREFLEX_DSP	MCLK	Int	133	COREAON_L4_GICLK	CORE_X2_CLK	DPLL_CORE
	SYSCLK	Func	38.4	WKUPAON_ICLK	SYS_CLK1	OSC0
					DPLL_ABE_X2_CLK	DPLL_ABE
SMARTREFLEX_GPU	MCLK	Int	133	COREAON_L4_GICLK	CORE_X2_CLK	DPLL_CORE
	SYSCLK	Func	38.4	WKUPAON_ICLK	SYS_CLK1	OSC0
					DPLL_ABE_X2_CLK	DPLL_ABE
SMARTREFLEX_IVAHD	MCLK	Int	133	COREAON_L4_GICLK	CORE_X2_CLK	DPLL_CORE
	SYSCLK	Func	38.4	WKUPAON_ICLK	SYS_CLK1	OSC0
					DPLL_ABE_X2_CLK	DPLL_ABE
SMARTREFLEX_MPU	MCLK	Int	133	COREAON_L4_GICLK	CORE_X2_CLK	DPLL_CORE
	SYSCLK	Func	38.4	WKUPAON_ICLK	SYS_CLK1	OSC0
					DPLL_ABE_X2_CLK	DPLL_ABE
SPINLOCK	SPINLOCK_ICLK	Int	266	L4CFG_L3_GICLK	CORE_X2_CLK	DPLL_CORE
TIMER1	TIMER1_ICLK	Int	38.4	WKUPAON_GICLK	SYS_CLK1	OSC0
					DPLL_ABE_X2_CLK	DPLL_ABE
	TIMER1_FCLK	Func	100	TIMER1_GFCLK	SYS_CLK1	OSC0
					FUNC_32K_CLK	OSC0
					SYS_CLK2	OSC1
					XREF_CLK0	XREF_CLK0
					XREF_CLK1	XREF_CLK1
					XREF_CLK2	XREF_CLK2
					XREF_CLK3	XREF_CLK3
					DPLL_ABE_X2_CLK	DPLL_ABE
					VIDEO1_CLK	DPLL_VIDEO1
					HDMI_CLK	DPLL_HDMI
TIMER2	TIMER2_ICLK	Int	266	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	TIMER2_FCLK	Func	100	TIMER2_GFCLK	SYS_CLK1	OSC0
					FUNC_32K_CLK	OSC0
					SYS_CLK2	OSC1
					XREF_CLK0	XREF_CLK0
					XREF_CLK1	XREF_CLK1
					XREF_CLK2	XREF_CLK2
					XREF_CLK3	XREF_CLK3
					DPLL_ABE_X2_CLK	DPLL_ABE
					VIDEO1_CLK	DPLL_VIDEO1
					HDMI_CLK	DPLL_HDMI

Table 5-9. Maximum Supported Frequency (continued)

MODULE				CLOCK SOURCE		
INSTANCE NAME	INPUT CLOCK NAME	CLOCK TYPE	MAX. CLOCK ALLOWED (MHz)	PRCM CLOCK NAME	PLL / OSC / SOURCE CLOCK NAME	PLL / OSC / SOURCE NAME
TIMER3	TIMER3_ICLK	Int	266	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	TIMER3_FCLK	Func	100	TIMER3_GFCLK	SYS_CLK1	OSC0
					FUNC_32K_CLK	OSC0
					SYS_CLK2	OSC1
					XREF_CLK0	XREF_CLK0
					XREF_CLK1	XREF_CLK1
					XREF_CLK2	XREF_CLK2
					XREF_CLK3	XREF_CLK3
					DPLL_ABE_X2_CLK	DPLL_ABE
					VIDEO1_CLK	DPLL_VIDEO1
					HDMI_CLK	DPLL_HDMI
TIMER4	TIMER4_ICLK	Int	266	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	TIMER4_FCLK	Func	100	TIMER4_GFCLK	SYS_CLK1	OSC0
					FUNC_32K_CLK	OSC0
					SYS_CLK2	OSC1
					XREF_CLK0	XREF_CLK0
					XREF_CLK1	XREF_CLK1
					XREF_CLK2	XREF_CLK2
					XREF_CLK3	XREF_CLK3
					DPLL_ABE_X2_CLK	DPLL_ABE
					VIDEO1_CLK	DPLL_VIDEO1
					HDMI_CLK	DPLL_HDMI
TIMER5	TIMER5_ICLK	Int	266	IPU_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	TIMER5_FCLK	Func	100	TIMER5_GFCLK	SYS_CLK1	OSC0
					FUNC_32K_CLK	OSC0
					SYS_CLK2	OSC1
					XREF_CLK0	XREF_CLK0
					XREF_CLK1	XREF_CLK1
					XREF_CLK2	XREF_CLK2
					XREF_CLK3	XREF_CLK3
					DPLL_ABE_X2_CLK	DPLL_ABE
					VIDEO1_CLK	DPLL_VIDEO1
					HDMI_CLK	DPLL_HDMI
					CLKOUTMUX[0]	CLKOUTMUX[0]

Table 5-9. Maximum Supported Frequency (continued)

MODULE				CLOCK SOURCE		
INSTANCE NAME	INPUT CLOCK NAME	CLOCK TYPE	MAX. CLOCK ALLOWED (MHz)	PRCM CLOCK NAME	PLL / OSC / SOURCE CLOCK NAME	PLL / OSC / SOURCE NAME
TIMER6	TIMER6_ICLK	Int	266	IPU_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	TIMER6_FCLK	Func	100	TIMER6_GFCLK	SYS_CLK1	OSC0
					FUNC_32K_CLK	OSC0
					SYS_CLK2	OSC1
					XREF_CLK0	XREF_CLK0
					XREF_CLK1	XREF_CLK1
					XREF_CLK2	XREF_CLK2
					XREF_CLK3	XREF_CLK3
					DPLL_ABE_X2_CLK	DPLL_ABE
					VIDEO1_CLK	DPLL_VIDEO1
					HDMI_CLK	DPLL_HDMI
					CLKOUTMUX[0]	CLKOUTMUX[0]
TIMER7	TIMER7_ICLK	Int	266	IPU_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	TIMER7_FCLK	Func	100	TIMER7_GFCLK	SYS_CLK1	OSC0
					FUNC_32K_CLK	OSC0
					SYS_CLK2	OSC1
					XREF_CLK0	XREF_CLK0
					XREF_CLK1	XREF_CLK1
					XREF_CLK2	XREF_CLK2
					XREF_CLK3	XREF_CLK3
					DPLL_ABE_X2_CLK	DPLL_ABE
					VIDEO1_CLK	DPLL_VIDEO1
					HDMI_CLK	DPLL_HDMI
					CLKOUTMUX[0]	CLKOUTMUX[0]
TIMER8	TIMER8_ICLK	Int	266	IPU_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	TIMER8_FCLK	Func	100	TIMER8_GFCLK	SYS_CLK1	OSC0
					FUNC_32K_CLK	OSC0
					SYS_CLK2	OSC1
					XREF_CLK0	XREF_CLK0
					XREF_CLK1	XREF_CLK1
					XREF_CLK2	XREF_CLK2
					XREF_CLK3	XREF_CLK3
					DPLL_ABE_X2_CLK	DPLL_ABE
					VIDEO1_CLK	DPLL_VIDEO1
					HDMI_CLK	DPLL_HDMI
					CLKOUTMUX[0]	CLKOUTMUX[0]

Table 5-9. Maximum Supported Frequency (continued)

MODULE				CLOCK SOURCE		
INSTANCE NAME	INPUT CLOCK NAME	CLOCK TYPE	MAX. CLOCK ALLOWED (MHz)	PRCM CLOCK NAME	PLL / OSC / SOURCE CLOCK NAME	PLL / OSC / SOURCE NAME
TIMER9	TIMER9_ICLK	Int	266	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	TIMER9_FCLK	Func	100	TIMER9_GFCLK	SYS_CLK1	OSC0
					FUNC_32K_CLK	OSC0
					SYS_CLK2	OSC1
					XREF_CLK0	XREF_CLK0
					XREF_CLK1	XREF_CLK1
					XREF_CLK2	XREF_CLK2
					XREF_CLK3	XREF_CLK3
					DPLL_ABE_X2_CLK	DPLL_ABE
					VIDEO1_CLK	DPLL_VIDEO1
					HDMI_CLK	DPLL_HDMI
TIMER10	TIMER10_ICLK	Int	266	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	TIMER10_FCLK	Func	100	TIMER10_GFCLK	SYS_CLK1	OSC0
					FUNC_32K_CLK	OSC0
					SYS_CLK2	OSC1
					XREF_CLK0	XREF_CLK0
					XREF_CLK1	XREF_CLK1
					XREF_CLK2	XREF_CLK2
					XREF_CLK3	XREF_CLK3
					DPLL_ABE_X2_CLK	DPLL_ABE
					VIDEO1_CLK	DPLL_VIDEO1
					HDMI_CLK	DPLL_HDMI
TIMER11	TIMER11_ICLK	Int	266	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	TIMER11_FCLK	Func	100	TIMER11_GFCLK	SYS_CLK1	OSC0
					FUNC_32K_CLK	OSC0
					SYS_CLK2	OSC1
					XREF_CLK0	XREF_CLK0
					XREF_CLK1	XREF_CLK1
					XREF_CLK2	XREF_CLK2
					XREF_CLK3	XREF_CLK3
					DPLL_ABE_X2_CLK	DPLL_ABE
					VIDEO1_CLK	DPLL_VIDEO1
					HDMI_CLK	DPLL_HDMI
TIMER12	TIMER12_ICLK	Int	38.4	WKUPAON_GICLK	SYS_CLK1	OSC0
					DPLL_ABE_X2_CLK	DPLL_ABE
	TIMER12_FCLK	Func	0.032	OSC_32K_CLK	RC_CLK	RC oscillator

Table 5-9. Maximum Supported Frequency (continued)

MODULE				CLOCK SOURCE		
INSTANCE NAME	**INPUT CLOCK NAME**	**CLOCK TYPE**	**MAX. CLOCK ALLOWED (MHz)**	**PRCM CLOCK NAME**	**PLL / OSC / SOURCE CLOCK NAME**	**PLL / OSC / SOURCE NAME**
TIMER13	TIMER13_ICLK	Int	266	L4PER3_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	TIMER13_FCLK	Func	100	TIMER13_GFCLK	SYS_CLK1	OSC0
					FUNC_32K_CLK	OSC0
					SYS_CLK2	OSC1
					XREF_CLK0	XREF_CLK0
					XREF_CLK1	XREF_CLK1
					XREF_CLK2	XREF_CLK2
					XREF_CLK3	XREF_CLK3
					DPLL_ABE_X2_CLK	DPLL_ABE
					VIDEO1_CLK	DPLL_VIDEO1
					HDMI_CLK	DPLL_HDMI
TIMER14	TIMER14_ICLK	Int	266	L4PER3_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	TIMER14_FCLK	Func	100	TIMER14_GFCLK	SYS_CLK1	OSC0
					FUNC_32K_CLK	OSC0
					SYS_CLK2	OSC1
					XREF_CLK0	XREF_CLK0
					XREF_CLK1	XREF_CLK1
					XREF_CLK2	XREF_CLK2
					XREF_CLK3	XREF_CLK3
					DPLL_ABE_X2_CLK	DPLL_ABE
					VIDEO1_CLK	DPLL_VIDEO1
					HDMI_CLK	DPLL_HDMI
TIMER15	TIMER15_ICLK	Int	266	L4PER3_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	TIMER15_FCLK	Func	100	TIMER15_GFCLK	SYS_CLK1	OSC0
					FUNC_32K_CLK	OSC0
					SYS_CLK2	OSC1
					XREF_CLK0	XREF_CLK0
					XREF_CLK1	XREF_CLK1
					XREF_CLK2	XREF_CLK2
					XREF_CLK3	XREF_CLK3
					DPLL_ABE_X2_CLK	DPLL_ABE
					VIDEO1_CLK	DPLL_VIDEO1
					HDMI_CLK	DPLL_HDMI

Table 5-9. Maximum Supported Frequency (continued)

MODULE				CLOCK SOURCE		
INSTANCE NAME	INPUT CLOCK NAME	CLOCK TYPE	MAX. CLOCK ALLOWED (MHz)	PRCM CLOCK NAME	PLL / OSC / SOURCE CLOCK NAME	PLL / OSC / SOURCE NAME
TIMER16	TIMER16_ICLK	Int	266	L4PER3_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	TIMER16_FCLK	Func	100	TIMER16_GFCLK	SYS_CLK1	OSC0
					FUNC_32K_CLK	OSC0
					SYS_CLK2	OSC1
					XREF_CLK0	XREF_CLK0
					XREF_CLK1	XREF_CLK1
					XREF_CLK2	XREF_CLK2
					XREF_CLK3	XREF_CLK3
					DPLL_ABE_X2_CLK	DPLL_ABE
					VIDEO1_CLK	DPLL_VIDEO1
					HDMI_CLK	DPLL_HDMI
TPCC	TPCC_GCLK	Int	266	L3MAIN1_L3_GICLK	CORE_X2_CLK	DPLL_CORE
TPTC1	TPTC0_GCLK	Int	266	L3MAIN1_L3_GICLK	CORE_X2_CLK	DPLL_CORE
TPTC2	TPTC1_GCLK	Int	266	L3MAIN1_L3_GICLK	CORE_X2_CLK	DPLL_CORE
UART1	UART1_FCLK	Func	48	UART1_GFCLK	FUNC_192M_CLK	DPLL_PER
	UART1_ICLK	Int	266	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE
UART2	UART2_FCLK	Func	48	UART2_GFCLK	FUNC_192M_CLK	DPLL_PER
	UART2_ICLK	Int	266	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE
UART3	UART3_FCLK	Func	48	UART3_GFCLK	FUNC_192M_CLK	DPLL_PER
	UART3_ICLK	Int	266	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE
UART4	UART4_FCLK	Func	48	UART4_GFCLK	FUNC_192M_CLK	DPLL_PER
	UART4_ICLK	Int	266	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE
UART5	UART5_FCLK	Func	48	UART5_GFCLK	FUNC_192M_CLK	DPLL_PER
	UART5_ICLK	Int	266	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE
UART6	UART6_FCLK	Func	48	UART6_GFCLK	FUNC_192M_CLK	DPLL_PER
	UART6_ICLK	Int	266	IPU_L3_GICLK	CORE_X2_CLK	DPLL_CORE
UART7	UART7_FCLK	Func	48	UART7_GFCLK	FUNC_192M_CLK	DPLL_PER
	UART7_ICLK	Int	266	L4PER2_L3_GICLK	CORE_X2_CLK	DPLL_CORE
UART8	UART8_FCLK	Func	48	UART8_GFCLK	FUNC_192M_CLK	DPLL_PER
	UART8_ICLK	Int	266	L4PER2_L3_GICLK	CORE_X2_CLK	DPLL_CORE
UART9	UART9_FCLK	Func	48	UART9_GFCLK	FUNC_192M_CLK	DPLL_PER
	UART9_ICLK	Int	266	L4PER2_L3_GICLK	CORE_X2_CLK	DPLL_CORE
UART10	UART10_FCLK	Func	48	UART10_GFCLK	FUNC_192M_CLK	DPLL_PER
	UART10_ICLK	Int	38.4	WKUPAON_GICLK	SYS_CLK1	OSC0
					DPLL_ABE_X2_CLK	DPLL_ABE
USB1	USB1_MICLK	Int	266	L3INIT_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	USB3PHY_REF_CLK	Func	34.3	USB_LFPS_TX_GFCLK	CORE_USB_OTG_SS_LFPS_TX_CLK	DPLL_CORE
	USB2PHY1_TREF_CLK	Func	38.4	USB_OTG_SS_REF_CLK	SYS_CLK1	OSC0
	USB2PHY1_REF_CLK	Func	960	L3INIT_960M_GFCLK	L3INIT_960_GFCLK	DPLL_USB

Table 5-9. Maximum Supported Frequency (continued)

MODULE				CLOCK SOURCE		
INSTANCE NAME	**INPUT CLOCK NAME**	**CLOCK TYPE**	**MAX. CLOCK ALLOWED (MHz)**	**PRCM CLOCK NAME**	**PLL / OSC / SOURCE CLOCK NAME**	**PLL / OSC / SOURCE NAME**
USB2	USB2_MICLK	Int	266	L3INIT_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	USB2PHY2_TREF_CLK	Func	38.4	USB_OTG_SS_REF_CLK	SYS_CLK1	OSC0
	USB2PHY2_REF_CLK	Func	960	L3INIT_960M_GFCLK	L3INIT_960_GFCLK	DPLL_USB
USB3	USB3_MICLK	Int	266	L3INIT_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	USB3PHY_PWRS_CLK	Func	38.4	USB_OTG_SS_REF_CLK	SYS_CLK1	OSC0
USB_PHY1_CORE	USB2PHY1_WKUP_CLK	Func	0.032	COREAON_32K_GFCLK	SYS_CLK1/610	OSC0
USB_PHY2_CORE	USB2PHY2_WKUP_CLK	Func	0.032	COREAON_32K_GFCLK	SYS_CLK1/610	OSC0
USB_PHY3_CORE	USB3PHY_WKUP_CLK	Func	0.032	COREAON_32K_GFCLK	SYS_CLK1/610	OSC0
VCP1	VCP1_CLK	Int	266	L3MAIN1_L3_GICLK	CORE_X2_CLK	DPLL_CORE
VCP2	VCP2_CLK	Int	266	L3MAIN1_L3_GICLK	CORE_X2_CLK	DPLL_CORE
VIP1	L3_CLK_PROC_CLK	Int & Func	266	VIP1_GCLK	CORE_X2_CLK	DPLL_CORE
					CORE_ISS_MAIN_CLK	DPLL_CORE
VPE	L3_CLK_PROC_CLK	Int & Func	300	VPE_GCLK	CORE_ISS_MAIN_CLK	DPLL_CORE
					VIDEO1_CLKOUT4	DPLL_VIDEO1
WD_TIMER1	PIOCPCLK	Int	38.4	WKUPAON_GICLK	SYS_CLK1	OSC0
					DPLL_ABE_X2_CLK	DPLL_ABE
	PITIMERCLK	Func	0.032	OSC_32K_CLK	RC_CLK	RC oscillator
WD_TIMER2	WD_TIMER2_ICLK	Int	38.4	WKUPAON_GICLK	SYS_CLK1	OSC0
					DPLL_ABE_X2_CLK	DPLL_ABE
	WD_TIMER2_FCLK	Func	0.032	WKUPAON_SYS_GFCLK	FUNC_32K_CLK	OSC0

5.6 Power Consumption Summary

NOTE

Maximum power consumption for this SoC depends on the specific use conditions for the end system. Contact your TI representative for assistance in estimating maximum power consumption for the end system use case.

5.7 Electrical Characteristics

NOTE

The data specified in Section 5.7.1 through Section 5.7.13 are subject to change.

NOTE

The interfaces or signals described in Section 5.7.1 through Section 5.7.13 correspond to the interfaces or signals available in multiplexing mode 0 (Function 1).

All interfaces or signals multiplexed on the balls described in these tables have the same DC electrical characteristics, unless multiplexing involves a PHY/GPIO combination in which case different DC electrical characteristics are specified for the different multiplexing modes (Functions).

5.7.1 LVCMOS DDR DC Electrical Characteristics

Table 5-10 summarizes the DC electrical characteristics for LVCMOS DDR Buffers.

NOTE

For more information on the I/O cell configurations (i[2:0], sr[1:0]), see *Control Module* chapter in the device TRM.

Table 5-10. LVCMOS DDR DC Electrical Characteristics

PARAMETER			MIN	NOM	MAX	UNIT
Signal Names in MUXMODE 0 (Single-Ended Signals): ddr1_d[31:0], ddr1_a[15:0], ddr1_dqm[3:0], ddr1_ba[2:0], ddr1_csn[1:0], ddr1_cke, ddr1_odt[1:0], ddr1_casn, ddr1_rasn, ddr1_wen, ddr1_rst, ddr1_ecc_d[7:0], ddr1_dqm_ecc;						
Balls: AH23 / AB16 / AG22 / AE20 / AC17 / AC18 / AF20 /AH21 / AG21 / AF17 / AE18 / AB18 / AD20 / AC19 / AC20 / AB19 / AF21 / AH22 / AG23 / AE21 / AF22 / AE22 / AD21 / AD22 / AC21 / AF18 / AE17 / AD18 / AF25 / AF26 / AG26 / AH26 / AF24 / AE24 / AF23 / AE23 / AC23 / AF27 / AG27 / AF28 / AE26 / AC25 / AC24 / AD25 / V20 / W20 / AB28 / AC28 / AC27 / Y19 / AB27 / Y20 / AA23 / Y22 / Y23 / AA24 / Y24 / AA26 / AA25 / AA28 / W22 / V23 / W19 / W23 / Y25 / V24 / V25 / Y26 / AD23 / AB23 / AC26 / AA27 / V26;						
Driver Mode						
V_{OH}	High-level output threshold (I_{OH} = 0.1 mA)		0.9*VDDS			V
V_{OL}	Low-level output threshold (I_{OL} = 0.1 mA)				0.1*VDDS	V
C_{PAD}	Pad capacitance (including package capacitance)				3	pF
Z_O	Output impedance (drive strength)	I[2:0] = 000 (Imp80)		80		Ω
		I[2:0] = 001 (Imp60)		60		
		I[2:0] = 010 (Imp48)		48		
		I[2:0] = 011 (Imp40)		40		
		I[2:0] = 100 (Imp34)		34		
Single-Ended Receiver Mode						
V_{IH}	High-level input threshold	DDR3/DDR3L	VREF+0.1		VDDS+0.2	V
V_{IL}	Low-level input threshold	DDR3/DDR3L	-0.2		VREF-0.1	V
V_{CM}	Input common-mode voltage		VREF -10%vdds		VREF+ 10%vdds	V
C_{PAD}	Pad capacitance (including package capacitance)				3	pF
Signal Names in MUXMODE 0 (Differential Signals): ddr1_dqs[3:0], ddr1_dqsn[3:0], ddr1_ck, ddr1_nck, ddr1_dqs_ecc, ddr1_dqsn_ecc						
Bottom Balls: AH25 / AG25 / AE27 / AE28 / AD27 / AD28 / Y28 / Y27 / V27 / V28 / AG24 / AH24						
Driver Mode						
V_{OH}	High-level output threshold (I_{OH} = 0.1 mA)		0.9*VDDS			V
V_{OL}	Low-level output threshold (I_{OL} = 0.1 mA)				0.1*VDDS	V
C_{PAD}	Pad capacitance (including package capacitance)				3	pF

Table 5-10. LVCMOS DDR DC Electrical Characteristics (continued)

PARAMETER			MIN	NOM	MAX	UNIT
Z_O	Output impedance (drive strength)	I[2:0] = 000 (Imp80)		80		Ω
		I[2:0] = 001 (Imp60)		60		
		I[2:0] = 010 (Imp48)		48		
		I[2:0] = 011 (Imp40)		40		
		I[2:0] = 100 (Imp34)		34		
Single-Ended Receiver Mode						
V_{IH}	High-level input threshold	DDR3/DDR3L	VREF+0.1		VDDS+0.2	V
V_{IL}	Low-level input threshold	DDR3/DDR3L	-0.2		VREF-0.1	V
V_{CM}	Input common-mode voltage		VREF -10%vdds		VREF+ 10%vdds	V
C_{PAD}	Pad capacitance (including package capacitance)				3	pF
Differential Receiver Mode						
V_{SWING}	Input voltage swing	DDR3/DDR3L	0.2		vdds+0.4	V
V_{CM}	Input common-mode voltage		VREF -10%vdds		VREF+ 10%vdds	V
C_{PAD}	Pad capacitance (including package capacitance)				3	pF

(1) VDDS stands for corresponding power supply (that is, vdds_ddr1). For more information on the power supply name and the corresponding ball, see Table 4-2, POWER [10] column.

(2) VREF stands for corresponding Reference Power Supply (that is, ddr1_vref0). For more information on the power supply name and the corresponding ball, see Table 4-2, POWER [10] column.

(3) For more information on the I/O cell configurations (i[2:0], sr[1:0]), see the *Control Module* chapter in the device TRM.

5.7.2 HDMIPHY DC Electrical Characteristics

The HDMIPHY DC Electrical Characteristics are compliant with the HDMI 1.4a specification and are not reproduced here.

5.7.3 Dual Voltage LVCMOS I2C DC Electrical Characteristics

Table 5-11 summarizes the DC electrical characteristics for Dual Voltage LVCMOS I2C Buffers.

NOTE

For more information on the IO cell configurations, see *Control Module* section in the device TRM.

Table 5-11. Dual Voltage LVCMOS I2C DC Electrical Characteristics

PARAMETER		MIN	NOM	MAX	UNIT
Signal Names in MUXMODE 0: i2c2_scl; i2c1_scl; i2c1_sda; i2c2_sda;					
Balls: F17 / C20 / C21 / C25					
I2C Standard Mode – 1.8 V					
V_{IH}	Input high-level threshold	0.7*VDDS			V
V_{IL}	Input low-level threshold			0.3*VDDS	V
V_{hys}	Hysteresis	0.1*VDDS			V
I_{IN}	Input current at each I/O pin with an input voltage between 0.1*VDDS to 0.9*VDDS			12	µA

Table 5-11. Dual Voltage LVCMOS I2C DC Electrical Characteristics (continued)

PARAMETER		MIN	NOM	MAX	UNIT
I_{OZ}	I_{OZ}(I_{PAD} Current) for BIDI cell. This current is contributed by the tristated driver leakage + input current of the Rx + weak pullup/pulldown leakage. PAD is swept from 0 to VDDS and the Max($I_{(PAD)}$) is measured and is reported as I_{OZ}			12	µA
C_{IN}	Input capacitance			10	pF
V_{OL3}	Output low-level threshold open-drain at 3-mA sink current			0.2*VDDS	V
I_{OLmin}	Low-level output current @V_{OL}=0.2*VDDS	3			mA
t_{OF}	Output fall time from V_{IHmin} to V_{ILmax} with a bus capacitance CB from 5 pF to 400 pF			250	ns
I2C Fast Mode – 1.8 V					
V_{IH}	Input high-level threshold	0.7*VDDS			V
V_{IL}	Input low-level threshold			0.3*VDDS	V
V_{hys}	Hysteresis	0.1*VDDS			V
I_{IN}	Input current at each I/O pin with an input voltage between 0.1*VDDS to 0.9*VDDS			12	µA
I_{OZ}	I_{OZ}(I_{PAD} Current) for BIDI cell. This current is contributed by the tristated driver leakage + input current of the Rx + weak pullup/pulldown leakage. PAD is swept from 0 to VDDS and the Max($I_{(PAD)}$) is measured and is reported as I_{OZ}			12	µA
C_{IN}	Input capacitance			10	pF
V_{OL3}	Output low-level threshold open-drain at 3-mA sink current			0.2*VDDS	V
I_{OLmin}	Low-level output current @V_{OL}=0.2*VDDS	3			mA
t_{OF}	Output fall time from V_{IHmin} to V_{ILmax} with a bus capacitance CB from 10 pF to 400 pF	20+0.1*Cb		250	ns
I2C Standard Mode – 3.3 V					
V_{IH}	Input high-level threshold	0.7*VDDS			V
V_{IL}	Input low-level threshold			0.3*VDDS	V
V_{hys}	Hysteresis	0.05*VDDS			V
I_{IN}	Input current at each I/O pin with an input voltage between 0.1*VDDS to 0.9*VDDS	31		80	µA
I_{OZ}	I_{OZ}(I_{PAD} Current) for BIDI cell. This current is contributed by the tristated driver leakage + input current of the Rx + weak pullup/pulldown leakage. PAD is swept from 0 to VDDS and the Max($I_{(PAD)}$) is measured and is reported as I_{OZ}	31		80	µA
C_{IN}	Input capacitance			10	pF
V_{OL3}	Output low-level threshold open-drain at 3-mA sink current			0.4	V
I_{OLmin}	Low-level output current @V_{OL}=0.4V	3			mA
I_{OLmin}	Low-level output current @V_{OL}=0.6V for full drive load (400pF/400KHz)	6			mA
t_{OF}	Output fall time from V_{IHmin} to V_{ILmax} with a bus capacitance CB from 5 pF to 400 pF			250	ns
I2C Fast Mode – 3.3 V					
V_{IH}	Input high-level threshold	0.7*VDDS			V
V_{IL}	Input low-level threshold			0.3*VDDS	V
V_{hys}	Hysteresis	0.05*VDDS			V
I_{IN}	Input current at each I/O pin with an input voltage between 0.1*VDDS to 0.9*VDDSS	31		80	µA

Table 5-11. Dual Voltage LVCMOS I2C DC Electrical Characteristics (continued)

PARAMETER		MIN	NOM	MAX	UNIT
I_{OZ}	I_{OZ}(I_{PAD} Current) for BIDI cell. This current is contributed by the tristated driver leakage + input current of the Rx + weak pullup/pulldown leakage. PAD is swept from 0 to VDDS and the Max($I_{(PAD)}$) is measured and is reported as I_{OZ}	31		80	µA
C_{IN}	Input capacitance			10	pF
V_{OL3}	Output low-level threshold open-drain at 3-mA sink current			0.4	V
I_{OLmin}	Low-level output current @V_{OL}=0.4V	3			mA
I_{OLmin}	Low-level output current @V_{OL}=0.6V for full drive load (400pF/400KHz)	6			mA
t_{OF}	Output fall time from V_{IHmin} to V_{ILmax} with a bus capacitance CB from 10 pF to 200 pF (Proper External Resistor Value should be used as per I2C spec)	20+0.1*Cb		250	ns
	Output fall time from V_{IHmin} to V_{ILmax} with a bus capacitance CB from 300 pF to 400 pF (Proper External Resistor Value should be used as per I2C spec)	40		290	ns

(1) VDDS stands for corresponding power supply (that is, vddshv3). For more information on the power supply name and the corresponding ball, see Table 4-2, POWER [10] column.

5.7.4 IQ1833 Buffers DC Electrical Characteristics

Table 5-12 summarizes the DC electrical characteristics for IQ1833 Buffers.

Table 5-12. IQ1833 Buffers DC Electrical Characteristics

PARAMETER		MIN	NOM	MAX	UNIT
Signal Names in MUXMODE 0: tclk;					
Balls: E20;					
1.8-V Mode					
V_{IH}	Input high-level threshold (Does not meet JEDEC V_{IH})	0.75 * VDDS			V
V_{IL}	Input low-level threshold (Does not meet JEDEC V_{IL})			0.25 * VDDS	V
V_{HYS}	Input hysteresis voltage	100			mV
I_{IN}	Input current at each I/O pin	2		11	µA
C_{PAD}	Pad capacitance (including package capacitance)			1	pF
3.3-V Mode					
V_{IH}	Input high-level threshold (Does not meet JEDEC V_{IH})	2.0			V
V_{IL}	Input low-level threshold (Does not meet JEDEC V_{IL})			0.6	V
V_{HYS}	Input hysteresis voltage	400			mV
I_{IN}	Input current at each I/O pin	5		11	µA
C_{PAD}	Pad capacitance (including package capacitance)			1	pF

(1) VDDS stands for corresponding power supply (that is, vddshv3). For more information on the power supply name and the corresponding ball, see Table 4-2, POWER [10] column.

5.7.5 IHHV1833 Buffers DC Electrical Characteristics

Table 5-13 summarizes the DC electrical characteristics for IHHV1833 Buffers.

Table 5-13. IHHV1833 Buffers DC Electrical Characteristics

PARAMETER		MIN	NOM	MAX	UNIT
Signal Names in MUXMODE 0: porz / rtc_porz / wakeup3 / wakeup0;					
Balls: F22 / AB17 / AD17 / AC16;					
1.8-V Mode					
V_{IH}	Input high-level threshold	1.2			V
V_{IL}	Input low-level threshold			0.4	V
V_{HYS}	Input hysteresis voltage	40			mV
I_{IN}	Input current at each I/O pin	0.02		1	µA
C_{PAD}	Pad capacitance (including package capacitance)			1	pF
3.3-V Mode					
V_{IH}	Input high-level threshold	1.2			V
V_{IL}	Input low-level threshold			0.4	V
V_{HYS}	Input hysteresis voltage	40			mV
I_{IN}	Input current at each I/O pin	5		8	µA
C_{PAD}	Pad capacitance (including package capacitance)			1	pF

5.7.6 LVCMOS OSC Buffers DC Electrical Characteristics

Table 5-14 summarizes the DC electrical characteristics for LVCMOS OSC Buffers.

Table 5-14. LVCMOS OSC Buffers DC Electrical Characteristics

PARAMETER		MIN	NOM	MAX	UNIT
Signal Names in MUXMODE 0: rtc_osc_xi_clkin32 / rtc_osc_xo;					
Balls: AE14 / AD14;					
1.8-V Mode					
V_{IH}	Input high-level threshold	0.65 * VDDS			V
V_{IL}	Input low-level threshold			0.35 * VDDS	V
V_{HYS}	Input hysteresis voltage	150			mV
C_{PAD}	Pad capacitance (including package capacitance)			3	pF

(1) VDDS stands for corresponding power supply (that is, vdda_rtc). For more information on the power supply name and the\corresponding ball, see Table 4-2, POWER [10] column.

5.7.7 LVCMOS CSI2 DC Electrical Characteristics

Table 5-15 summarizes the DC electrical characteristics for LVCMOS CSI2 Buffers.

Table 5-15. LVCMOS CSI2 DC Electrical Characteristics

PARAMETER		MIN	NOM	MAX	UNIT
Signals MUXMODE0 : csi2_0_dx[4:0]; csi2_0_dy[4:0]; csi2_1_dx[2:0]; csi2_1_dy[2:0];					
Bottom Balls: AE1 / AD2 / AF1 / AE2 / AF2 / AF3 / AH4 / AG4 / AH3 / AG3 / AG5 / AH5 / AG6 / AH6 / AH7 / AG7					
MIPI D-PHY Mode Low-Power Receiver (LP-RX)					
V_{IH}	Input high-level voltage	880		1350	mV
V_{IL}	Input low-level voltage			550	mV
V_{ITH}	Input high-level threshold (1)			880	mV
V_{ITL}	Input low-level threshold (2)	550			mV
V_{HYS}	Input hysteresis (3)	25			mV
MIPI D-PHY Mode Ultralow Power Receiver (ULP-RX)					

Table 5-15. LVCMOS CSI2 DC Electrical Characteristics (continued)

PARAMETER		MIN	NOM	MAX	UNIT
V_{IL}	Input low-level voltage			300	mV
V_{ITL}	Input low-level threshold (4)	300			mV
V_{HYS}	Input hysteresis (3)	25			mV
MIPI D-PHY Mode High Speed Receiver (HS-RX)					
V_{IDTH}	Differential input high-level threshold	70			mV
V_{IDTL}	Differential input low-level threshold			–70	mV
V_{IDMAX}	Maximum differential input voltage (7)			270	mV
V_{IHHS}	Single-ended input high voltage (5)			460	mV
V_{ILHS}	Single-ended input low voltage (5)	–40			mV
V_{CMRXDC}	Differential input common-mode voltage (5) (6)	70		330	mV
Z_{ID}	Differential input impedance	80	100	125	Ω

(1) V_{ITH} is the voltage at which the receiver is required to detect a high state in the input signal.

(2) V_{ITL} is the voltage at which the receiver is required to detect a low state in the input signal. V_{ITL} is larger than the maximum single-ended line high voltage during HS transmission. Therefore, both low-power (LP) receivers will detect low during HS signaling.

(3) To reduce noise sensitivity on the received signal, the LP receiver is required to incorporate a hysteresis, V_{HYST}. V_{HYST} is the difference between the V_{ITH} threshold and the V_{ITL} threshold.

(4) V_{ITL} is the voltage at which the receiver is required to detect a low state in the input signal. Specification is relaxed for detecting 0 during ultralow power (ULP) state. The LP receiver is not required to detect HS single-ended voltage as 0 in this state.

(5) Excluding possible additional RF interference of 200 mV_{PP} beyond 450 MHz.

(6) This value includes a ground difference of 50 mV between the transmitter and the receiver, the static common-mode level tolerance and variations below 450 MHz.

(7) This number corresponds to the VOD_{MAX} transmitter.

(8) Common mode is defined as the average voltage level of X and Y: $V_{CMRX} = (V_X + V_Y) / 2$.

(9) Common mode ripple may be due to t_R or t_F and transmission line impairments in the PCB.

(10) For more information regarding the pin name (or ball name) and corresponding signal name, see Table 4-7 ,*CSI 2 Signal Descriptions*.

5.7.8 *BC1833IHHV Buffers DC Electrical Characteristics*

Table 5-16 summarizes the DC electrical characteristics for BC1833IHHV Buffers.

Table 5-16. BC1833IHHV Buffers DC Electrical Characteristics

PARAMETER		MIN	NOM	MAX	UNIT
Signal Names in MUXMODE 0: on_off;					
Balls: Y11;					
1.8-V Mode					
V_{OH}	Output high-level threshold (I_{OH} = 2 mA)	VDDS-0.45			V
V_{OL}	Output low-level threshold (I_{OL} = 2 mA)			0.45	V
I_{DRIVE}	Pin Drive strength at PAD Voltage = 0.45V or VDDS-0.45V	6			mA
I_{IN}	Input current at each I/O pin	6		12	µA
I_{OZ}	I_{OZ}(I_{PAD} Current) for BIDI cell. This current is contributed by the tristated driver leakage + input current of the Rx + weak pullup/pulldown leakage. PAD is swept from 0 to VDDS and the Max($I_{(PAD)}$) is measured and is reported as I_{OZ}			6	µA
C_{PAD}	Pad capacitance (including package capacitance)			4	pF
3.3-V Mode					
V_{OH}	Output high-level threshold (I_{OH} = 100 µA)	VDDS-0.2			V
V_{OL}	Output low-level threshold (I_{OL} = 100 µA)			0.2	V
I_{DRIVE}	Pin Drive strength at PAD Voltage = 0.45V or VDDS-0.45V	6			mA
I_{IN}	Input current at each I/O pin			60	µA

Table 5-16. BC1833IHHV Buffers DC Electrical Characteristics (continued)

PARAMETER		MIN	NOM	MAX	UNIT
I_{OZ}	I_{OZ}(I_{PAD} Current) for BIDI cell. This current is contributed by the tristated driver leakage + input current of the Rx + weak pullup/pulldown leakage. PAD is swept from 0 to VDDS and the Max($I_{(PAD)}$) is measured and is reported as I_{OZ}			60	µA
C_{PAD}	Pad capacitance (including package capacitance)			4	pF

(1) VDDS stands for corresponding power supply (that is, vddshv5). For more information on the power supply name and the corresponding ball, see Table 4-2, POWER [10] column.

5.7.9 USBPHY DC Electrical Characteristics

NOTE

USB1 instance is compliant with the USB3.0 SuperSpeed Transmitter and Receiver Normative Electrical Parameters as defined in the USB3.0 Specification Rev 1.0 dated Jun 6, 2011.

NOTE

USB1 and USB2 Electrical Characteristics are compliant with USB2.0 Specification Rev 2.0 dated April 27, 2000 including ECNs and Errata as applicable.

5.7.10 Dual Voltage SDIO1833 DC Electrical Characteristics

Table 5-17 summarizes the DC electrical characteristics for Dual Voltage SDIO1833 Buffers.

Table 5-17. Dual Voltage SDIO1833 DC Electrical Characteristics

PARAMETER		MIN	NOM	MAX	UNIT
Signal Names in Mode 0: mmc1_clk, mmc1_cmd, mmc1_data[3:0]					
Bottom Balls: W6 / Y6 / AA6 / Y4 / AA5 / Y3					
1.8-V Mode					
V_{IH}	Input high-level threshold	1.27			V
V_{IL}	Input low-level threshold			0.58	V
V_{HYS}	Input hysteresis voltage	50 (2)			mV
I_{IN}	Input current at each I/O pin			30	µA
I_{OZ}	I_{OZ}(I_{PAD} Current) for BIDI cell. This current is contributed by the tristated driver leakage + input current of the Rx + weak pullup/pulldown leakage. PAD is swept from 0 to VDDS and the Max(I(PAD)) is measured and is reported as I_{OZ}			30	µA
I_{IN} with pulldown enabled	Input current at each I/O pin with weak pulldown enabled measured when PAD = VDDS	50	120	210	µA
I_{IN} with pullup enabled	Input current at each I/O pin with weak pullup enabled measured when PAD = 0	60	120	200	µA
C_{PAD}	Pad capacitance (including package capacitance)			5	pF
V_{OH}	Output high-level threshold (I_{OH} = 2 mA)	1.4			V
V_{OL}	Output low-level threshold (I_{OL} = 2 mA)			0.45	V
3.3-V Mode					
V_{IH}	Input high-level threshold	0.625 × VDDS			V
V_{IL}	Input low-level threshold			0.25 × VDDS	V
V_{HYS}	Input hysteresis voltage	40 (2)			mV
I_{IN}	Input current at each I/O pin			110	µA
I_{OZ}	I_{OZ}(I_{PAD} Current) for BIDI cell. This current is contributed by the tristated driver leakage + input current of the Rx + weak pullup/pulldown leakage. PAD is swept from 0 to VDDS and the Max(I(PAD)) is measured and is reported as I_{OZ}			110	µA
I_{IN} with pulldown enabled	Input current at each I/O pin with weak pulldown enabled measured when PAD = VDDS	40	100	290	µA
I_{IN} with pullup enabled	Input current at each I/O pin with weak pullup enabled measured when PAD = 0	10	100	290	µA
C_{PAD}	Pad capacitance (including package capacitance)			5	pF
V_{OH}	Output high-level threshold (I_{OH} = 2 mA)	0.75 × VDDS			V
V_{OL}	Output low-level threshold (I_{OL} = 2 mA)			0.125 × VDDS	V

(1) VDDS stands for corresponding power supply (that is, vddshv8). For more information on the power supply name and the corresponding ball, see Table 4-2, POWER [10] column.

(2) Hysteresis is enabled/disabled with CTRL_CORE_CONTROL_HYST_1.SDCARD_HYST register.

5.7.11 Dual Voltage LVCMOS DC Electrical Characteristics

Table 5-18 summarizes the DC electrical characteristics for Dual Voltage LVCMOS Buffers.

Table 5-18. Dual Voltage LVCMOS DC Electrical Characteristics

PARAMETER		MIN	NOM	MAX	UNIT
1.8-V Mode					
V_{IH}	Input high-level threshold	0.65*VDDS			V
V_{IL}	Input low-level threshold			0.35*VDDS	V
V_{HYS}	Input hysteresis voltage	100			mV
V_{OH}	Output high-level threshold (I_{OH} = 2 mA)	VDDS-0.45			V
V_{OL}	Output low-level threshold (I_{OL} = 2 mA)			0.45	V
I_{DRIVE}	Pin Drive strength at PAD Voltage = 0.45V or VDDS-0.45V	6			mA
I_{IN}	Input current at each I/O pin			16	µA
I_{OZ}	I_{OZ}(I_{PAD} Current) for BIDI cell. This current is contributed by the tristated driver leakage + input current of the Rx + weak pullup/pulldown leakage. PAD is swept from 0 to VDDS and the Max($I_{(PAD)}$) is measured and is reported as I_{OZ}			16	µA
$I_{IN\ with\ pulldown\ enabled}$	Input current at each I/O pin with weak pulldown enabled measured when PAD = VDDS	50	120	210	µA
$I_{IN\ with\ pullup\ enabled}$	Input current at each I/O pin with weak pullup enabled measured when PAD = 0	60	120	200	µA
C_{PAD}	Pad capacitance (including package capacitance)			4	pF
Z_O	Output impedance (drive strength)		40		Ω
3.3-V Mode					
V_{IH}	Input high-level threshold	2			V
V_{IL}	Input low-level threshold			0.8	V
V_{HYS}	Input hysteresis voltage	200			mV
V_{OH}	Output high-level threshold (I_{OH} = 100 µA)	VDDS-0.2			V
V_{OL}	Output low-level threshold (I_{OL} = 100 µA)			0.2	V
I_{DRIVE}	Pin Drive strength at PAD Voltage = 0.45V or VDDS-0.45V	6			mA
I_{IN}	Input current at each I/O pin			65	µA
I_{OZ}	I_{OZ}(I_{PAD} Current) for BIDI cell. This current is contributed by the tristated driver leakage + input current of the Rx + weak pullup/pulldown leakage. PAD is swept from 0 to VDDS and the Max($I_{(PAD)}$) is measured and is reported as I_{OZ}			65	µA
$I_{IN\ with\ pulldown\ enabled}$	Input current at each I/O pin with weak pulldown enabled measured when PAD = VDDS	40	100	200	µA
$I_{IN\ with\ pullup\ enabled}$	Input current at each I/O pin with weak pullup enabled measured when PAD = 0	10	100	290	µA
C_{PAD}	Pad capacitance (including package capacitance)			4	pF
Z_O	Output impedance (drive strength)		40		Ω

(1) VDDS stands for corresponding power supply. For more information on the power supply name and the corresponding ball, see Table 4-2, POWER [10] column.

5.7.12 SATAPHY DC Electrical Characteristics

NOTE

The SATA module is compliant with the electrical parameters specified in the *SATA-IO SATA Specification*, Revision 3.2, August 7, 2013.

5.7.13 PCIEPHY DC Electrical Characteristics

NOTE

The PCIe interfaces are compliant with the electrical parameters specified in PCI-Express® Base Specification Revision 3.0.

5.8 VPP Specifications for One-Time Programmable (OTP) eFuses

NOTE

This functionality is available only for Silicon Revision 2.1.

This section specifies the operating conditions required for programming the OTP eFuses and is applicable only for High-Security Devices.

Table 5-19. Recommended Operating Conditions for OTP eFuse Programming

over operating free-air temperature range (unless otherwise noted)

PARAMETER	DESCRIPTION	MIN	NOM	MAX	UNIT
vdd	Supply voltage range for the core domain during OTP operation	1.11	1.15	1.2	V
vpp	Supply voltage range for the eFuse ROM domain during normal operation		NC		V
	Supply voltage range for the eFuse ROM domain during OTP programming(1)(2)		1.8		V
I(vpp)				100	mA
Temperature (junction)		0	25	85	ºC

(1) Supply voltage range includes DC errors and peak-to-peak noise. TI power management solutions TLV70718 from the TLV707x family meet the supply voltage range needed for vpp.

(2) During normal operation, no voltage should be applied to vpp. This can be typically achieved by disabling the regulator attached to the vpp terminal. For more details, see TLV707, TLV707P 200-mA, Low-I_Q, Low-Noise, Low-Dropout Regulator for Portable Devices.

5.8.1 Hardware Requirements

The following hardware requirements must be met when programming keys in the OTP eFuses:

- The vpp power supply must be disabled when not programming OTP registers.
- The vpp power supply must be ramped up after the proper device power-up sequence (for more details, see Section 5.10).

5.8.2 Programming Sequence

Programming sequence for OTP eFuses:

1. Power on the board per the power-up sequencing. No voltage should be applied on the vpp terminal during power up and normal operation.
2. Load the OTP write software required to program the eFuse (contact your local TI representative for the OTP software package).
3. Apply the voltage on the vpp terminal according to the specification in Table 5-19.
4. Run the software that programs the OTP registers.
5. After validating the content of the OTP registers, remove the voltage from the vpp terminal.

5.8.3 Impact to Your Hardware Warranty

You accept that e-Fusing the TI Devices with security keys permanently alters them. You acknowledge that the e-Fuse can fail, for example, due to incorrect or aborted program sequence or if you omit a sequence step. Further the TI Device may fail to secure boot if the error code correction check fails for the Production Keys or if the image is not signed and optionally encrypted with the current active Production Keys. These types of situations will render the TI Device inoperable and TI will be unable to confirm whether the TI Devices conformed to their specifications prior to the attempted e-Fuse. CONSEQUENTLY, TI WILL HAVE NO LIABILITY (WARRANTY OR OTHERWISE) FOR ANY TI DEVICES THAT HAVE BEEN e-FUSED WITH SECURITY KEYS.

5.9 Thermal Characteristics

For reliability and operability concerns, the maximum junction temperature of the Device has to be at or below the T_J value identified in Table 5-4, *Recommended Operating Conditions*.

A BCI compact thermal model for this Device is available and recommended for use when modeling thermal performance in a system.

Therefore, it is recommended to perform thermal simulations at the system level with the worst case device power consumption.

5.9.1 Package Thermal Characteristics

Table 5-20 provides the thermal resistance characteristics for the package used on this device.

NOTE

Power dissipation of 1.9 W and an ambient temperature of 85ºC is assumed for ABC package.

Table 5-20. Thermal Resistance Characteristics

NO.	PARAMETER	DESCRIPTION	°C/W(1)	AIR FLOW (m/s)(2)
T1	$R\Theta_{JC}$	Junction-to-case	0.41	N/A
T2	$R\Theta_{JB}$	Junction-to-board	4.74	N/A
T3	$R\Theta_{JA}$	Junction-to-free air	11.9	0
T4		Junction-to-moving air	8.9	1
T5			8.0	2
T6			7.4	3
T7	Ψ_{JT}	Junction-to-package top	0.22	0
T8			0.22	1
T9			0.22	2
T10			0.23	3
T11	Ψ_{JB}	Junction-to-board	4.12	0
T12			3.73	1
T13			3.59	2
T14			3.48	3

(1) These measurements were conducted in a JEDEC defined 2S2P system (with the exception of the Theta JC [$R\Theta_{JC}$] measurement, which was conducted in a JEDEC defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:

– JESD51-2, *Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air)*
– JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
– JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
– JESD51-9, *Test Boards for Area Array Surface Mount Packages*

(2) m/s = meters per second

5.10 Power Supply Sequences

This section describes the power-up and power-down sequence required to ensure proper device operation. The power supply names described in this section comprise a superset of a family of compatible devices. Some members of this family will not include a subset of these power supplies and their associated device modules. Refer to the Section 4.2, *Ball Characteristics* of the Section 4, *Terminal Configuration and Functions* to determine which power supplies are applicable.

Figure 5-2 and Figure 5-3 describe the device Power Sequencing.

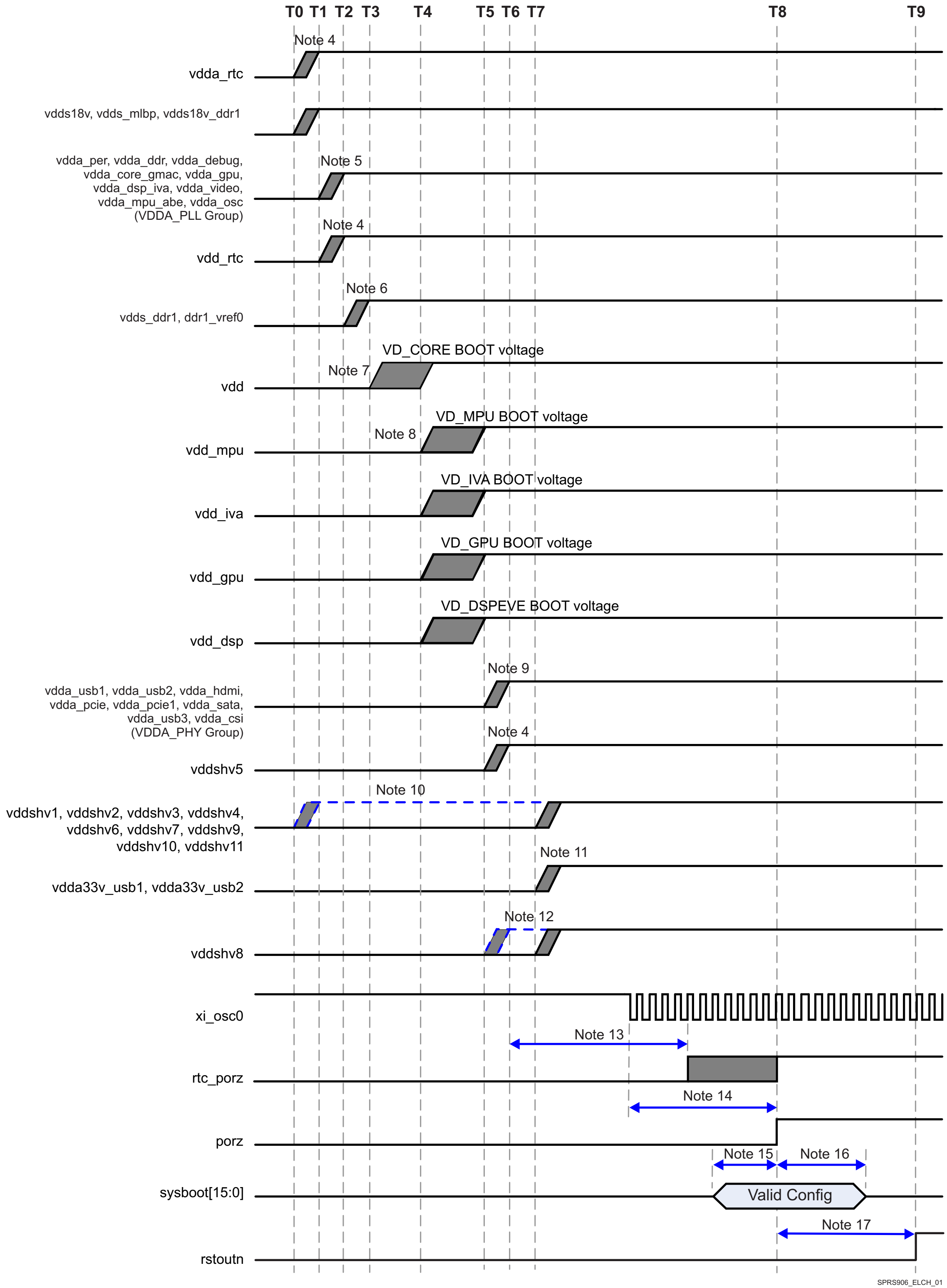


Figure 5-2. Recommended Power-Up Sequencing

(1) Time stamps:

– T0 = 0 ms; T1 = 0.55 ms; T2 = 1.1 ms; T3 = 1.65 ms; T4 = 2.2 ms; T5 = 2.75 ms; T6 = 3.3 ms; T7 = 5.85 ms; T8 = 6.4 ms; T9 = 8.4

ms. All “Tn” markers show total elapsed time from T0.

(2) Terminology:
- $V_{OPR\ MIN}$ = Minimum Operational Voltage level that ensures device functionality and specified performance per Section 5.4, *Recommended Operating Conditions*.
- Ramp Up = transition time from V_{OFF} to $V_{OPR\ MIN}$.

(3) General timing diagram items:
- Grey shaded areas show valid transition times for supplies between $V_{OPR\ MIN}$ and V_{OFF}.
- Dashed horizontal lines are not valid ramp times but show alternate transition times based upon common sources and clarified in associated note.
- Dashed vertical lines show approximate elapse times based upon TI recommended PMIC power sequencer circuit performance.

(4) vddshv5, vdd_rtc, and vdda_rtc domains:
- If RTC mode is used, then vdda_rtc, vdd_rtc and vddshv5 must be individually powered with separate power supplies and cannot be combined with other rails.
- If RTC-mode is not supported then the following combinations are approved:
  - vdda_rtc can be combined with vdds18v
  - vdd_rtc can be combined with vdd
  - vddshv5 can be combined with other 1.8 V or 3.3 V vddshvn rails

  If combinations listed above are not followed then sequencing for these 3 voltage rails should follow the RTC mode timing requirements.

(5) vdda_* rails should not be combined with vdds18v_* for best performance to avoid transient switching noise impacts on analog domains. vdda_* should not ramp-up before vdds18v_* but could ramp concurrently if design ensures final operational voltage will not be reached until after vdds18v. The preferred sequence is to follow all vdds18v_* to ensure circuit components and PCB design do not cause an inadvertent violation.

(6) vdds_ddr* should not ramp-up before vdds18v_*. The preferred sequence has vdds_ddr1 following vdds18v_* to ensure circuit components and PCB design do not cause an inadvertent violation. vdds_ddr1 can ramp-up before, concurrently or after vdda_*, there are no dependencies between vdds_ddr1 and vdda_* domains.

(7) vdd should not ramp-up before vdds18v_* or vdds_ddr* domains have reached $V_{OPR\ MIN}$.

(8) vdd_mpu, vdd_iva, vdd_gpu, vdd_dsp domains should follow vdd core supply as preferred sequence. If vdd_mpu, vdd_iva, vdd_gpu, vdd_dsp domains ramp concurrently or quicker than vdd core, then vdd core must remain at least 150 mV greater than vdd_mpu, vdd_iva, vdd_gpu, vdd_dsp domains during ramp. Circuit design (components and PCB) must ensure vdd reaches final operational voltage before any of the vdd_mpu, vdd_iva, vdd_gpu, vdd_dsp domains.

(9) VDDA_PHY group should not be combined with VDDA_PLL group to avoid transient switching noise impacts.

(10) vddshv[1-7, 9-11] domains:
- If 1.8 V I/O signaling is needed, then 1.8 V must be sourced from common vdds18v supply and ramp up concurrently with vdds18v.
- If 3.3 V I/O signaling is needed, then 3.3 V vddshvx rails must ramp up after vdd_mpu, vdd_iva, vdd_gpu, vdd_dsp, and VDDA_PHY group domains.

(11) vdda33v_usb[1-2] domain:
- If USB1 and USB2 interfaces are used, should be supplied from independent analog supply.
- If USB1/USB2 interface is not used, could be connected to VSS/GND if both conditions are met:
  - USB1/USB2 diff pair (usb1_dm/usb1_dp; usb2_dm/usb2_dp) pins are left unconnected
  - vdda_usb1 and/or vdda_usb2 PHY is not energized

(12) vddshv8 shows two ramp up options for 1.8 V I/O or 3.3 V I/O or SD Card operation:
- If 1.8 V I/O signaling is needed, then vddshv8 must ramp up after vdd and before or concurrently with 3.3 V vddshv* rails.
- If 3.3 V I/O signaling is needed, then vddshv8 must be combined with other 3.3 V vddshv* rails.
- If SD Card operation is needed, then vddshv8 must be sourced from a dual voltage (3.3 V / 1.8 V) power source per SDIO specifications and ramp up concurrently with 3.3 V vddshv* rails.

(13) Pulse duration: rtc_porz must remain low 1 ms after vdda_rtc, vddshv5, and vdd_rtc are ramped and stable or can be de-asserted before but no later than porz. The FUNK_32K_CLK source must be stable and at a valid frequency 1 ms prior to de-asserting rtc_porz high.

(14) porz must remain asserted low until both of the following conditions are met:
- Minimum of 12P, where P = 1 / (SYS_CLK1 / 610), units in ns.
- All device supply rails reach stable operational levels.

(15) Setup time: sysboot[15:0] pins must be valid 2P[14] before porz is de-asserted high.

(16) Hold time: sysboot[15:0] pins must be valid 15P[14] after porz is de-asserted high.

(17) rstoutn will be set high after global reset, due to porz, is de-asserted following an internal 2 ms delay. rstoutn is only valid after vddshv3 reaches an operational level. If used as a peripheral component reset, it should be AND gated with porz to avoid possible reset glitches during power up.

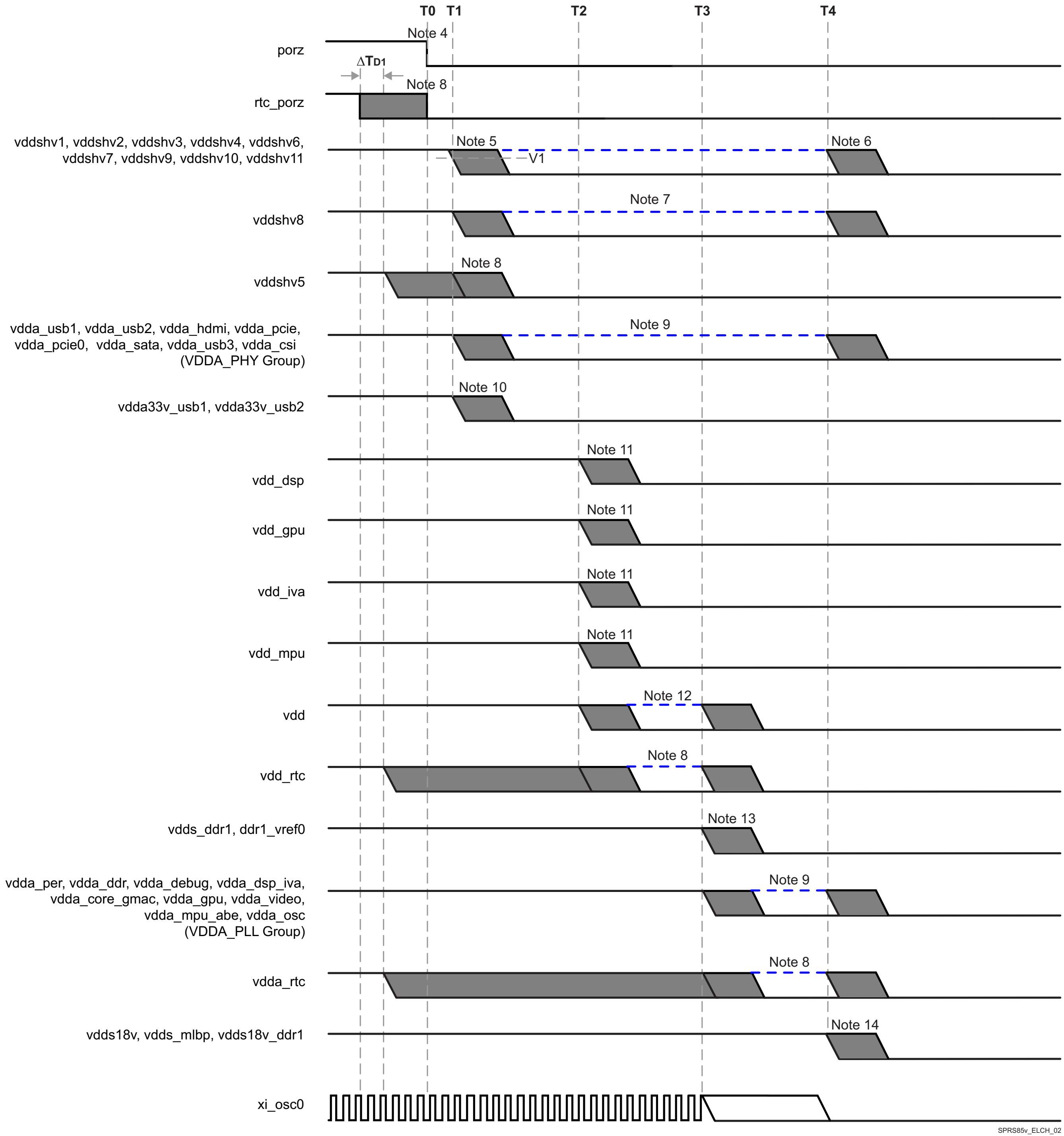


Figure 5-3. Recommended Power-Down Sequencing

(1) Time stamps:

– T0 = 0 ms, T1 > 100 µs, T2 = 0.5 ms, T3 = 1.0 ms, T4 = 1.5 ms; V1 = 2.7 V. All "Tn" markers are intended to show elapsed times from T0. Delta time: Δ T_{D1} > 100 µs.

(2) Terminology:

– $V_{OPR\ MIN}$ = Minimum Operational Voltage level that ensures device functionality and specified performance per Section 5.4, *Recommended Operating Conditions*.
– V_{OFF} = OFF Voltage level is defined to be less than 0.6 V where any current draw has no impact to POH.
– Ramp Down = transition time from $V_{OPR\ MIN}$ to V_{OFF} and is slew rate independent.

(3) General timing diagram items:

- Grey shaded areas show valid transition times for supplies between $V_{OPR\ MIN}$ and V_{OFF}.
- Dashed horizontal lines are not valid ramp times but show alternate transition times based upon common sources and clarified in associated note.
- Dashed vertical lines show approximate elapse times based upon TI recommended PMIC power-down sequencer circuit performance.

(4) porz signals must be asserted low for 100 µs min to ensure SoC is set to a safe functional state before any voltage begins to ramp down.

(5) vddshv* domains supplied by 3.3 V:

- must remain greater than 2.7 V to enable Dual Voltage GPIO selector circuit operation for 100 µs min after porz is asserted low.
- must be in first group of supplies ramping down after porz has been asserted low for 100 µs min.
- must not exceed vdds18v by more than 2 V during ramp down, see Figure 5-7 “vdds18v and vdda_* Discharge Relationship”.

(6) vddshv* domains supplied by 1.8 V:

- must ramp down concurrently with vdds18v and be sourced from the same vdds18v supply.

(7) vddshv8 domain:

- must be in first group of supplies to ramp down after porz has been asserted low for 100 µs min.
- if SDIO operation is needed, must be sourced from independent power resource that can provide dual voltage (3.3 V / 1.8 V) operation as required to be compliant to SDIO specification
- if SDIO operation is not needed, must be grouped and ramped down with other vddshv* domains as noted above.

(8) RTC domains (vddshv5, vdd_rtc, and vdda_rtc):

- If RTC mode is used:
  - rtc_porz can be asserted low before porz and RTC domains can be ramped down after 100 µs elapsed time.
  - must be sourced from independent supplies and must not be combined with other rails.
  - timing diagram shows this mode of operation.
- If RTC mode is not used, then:
  - rtc_porz must be connected to porz signal.
  - vddshv5 must be grouped and ramped down with other vddshv* domains as noted above.
  - vdd_rtc must be grouped and ramped down with vdd.
  - vdda_rtc must be grouped and ramped down with either VDDA_PHY group or vdds18v.

(9) vdda_* domains:

- should not be combined with vdds18v for best performance to avoid transient switching noise impacts on analog domains.
- can ramp down before or concurrently with vdds18v.
- must satisfy the vdds18v and vdda_* Discharge Relationship (see Figure 5-7) if vdda_* disable point is later or discharge rate is slower than vdds18v.
- can ramp down before, concurrently or after vdds_ddr*, there is no dependency between these supplies.

(10) vdda33v_usb* domains:

- can start ramping down 100 µs after low assertion of porz
- can ramp down concurrently or before VDDA_PHY group

(11) vdd_dsp, vdd_gpu, vdd_iva, vdd_mpu domains can ramp down before or concurrently with vdd.

(12) vdd can ramp down concurrently or after with vdd_dsp, vdd_gpu, vdd_iva, vdd_mpu domains.

(13) vdds_ddr* domains:

- should ramp down after vdd begins ramping down.

(14) vdds18v domain:

- should maintain $V_{OPR\ MIN}$ (V_{NOM} -5% = 1.71 V) until all other supplies start to ramp down.
- must satisfy the vdds18v versus vddshv[1-7, 9-11] Discharge Relationship (see Figure 5-5) if vddshv* is operating at 3.3 V
- must satisfy the vdds18v and vdds_ddr* Discharge Relationship (see Figure 5-6) if vdds_ddr* discharge rate is slower than vdds18v.

Figure 5-4 describes the RTC-mode Power Sequencing.

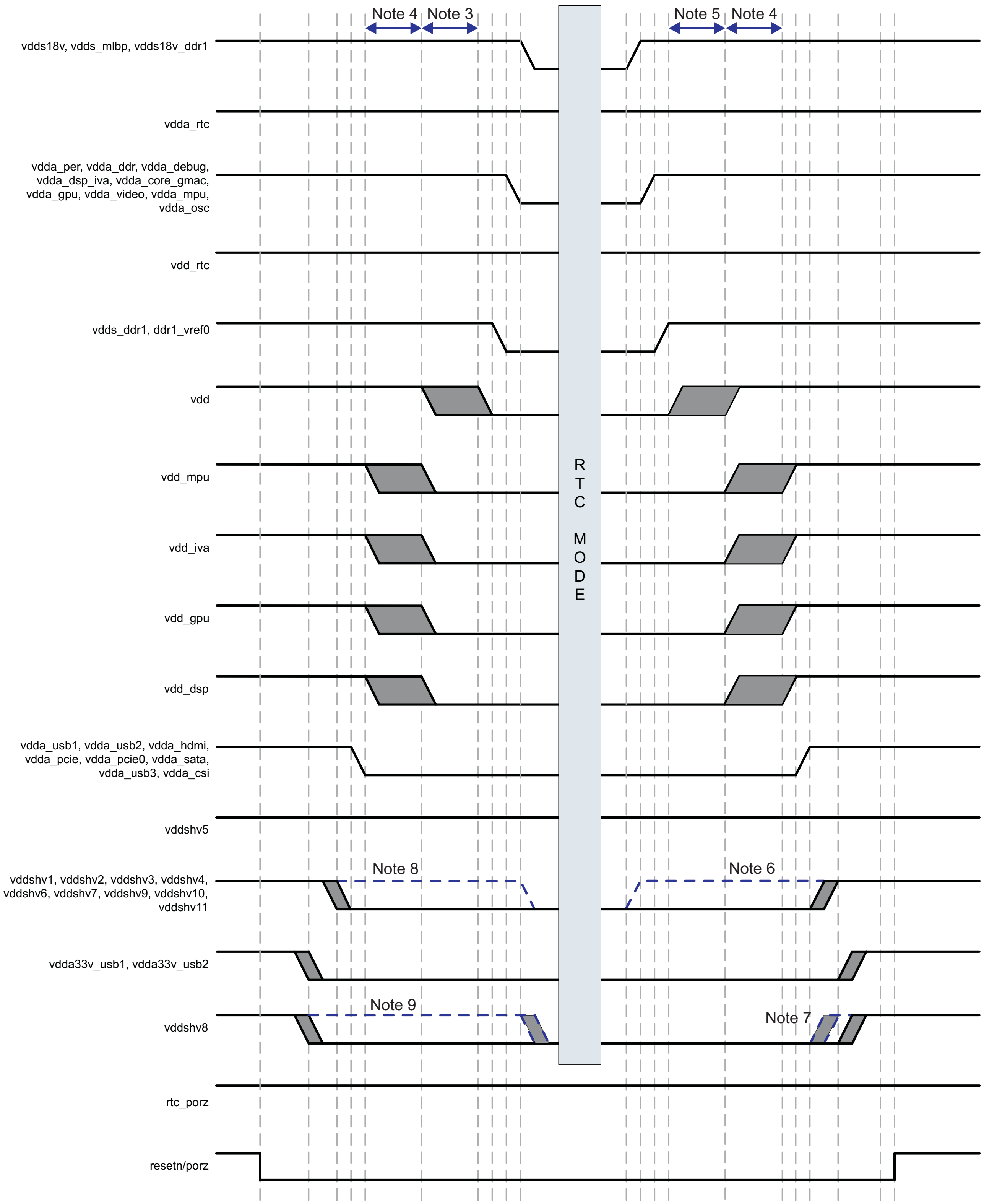


Figure 5-4. RTC Mode Sequencing

(1) Grey shaded areas are windows where it is valid to ramp the voltage rail.

(2) Blue dashed lines are not valid windows but show alternate ramp possibilities based on the associated note.
(3) vdd must ramp down after or at the same time as vdd_mpu, vdd_gpu, vdd_dsp and vdd_iva.
(4) vdd_mpu, vdd_gpu, vdd_dsp, vdd_iva can be ramped at the same time or can be staggered.
(5) vdd must ramp up before or at the same time as vdd_mpu, vdd_gpu, vdd_dsp and vdd_iva.
(6) If any of the vddshv[1-7,9-11] rails (not including vddshv8) are used as 1.8V only, then these rails can be combined with vdds18v.
(7) vddshv8 is separated out to show support for dual voltage. If single voltage is used then vddshv8 can be combined with other vddshvn rails but vddshv8 must ramp down before vdd and must ramp up after vdd.
(8) If any of the vddshv[1-7,9-11] rails (not including vddshv8) are used as 1.8V only, then these rails can be combined with vdds18v. vddshv[1-7,9-11] is allowed to ramp down at either of the two points shown in the timing diagram in either 1.8V mode or in 3.3V mode. If vddshv[1-7,9-11] ramps down at the later time in the diagram then the board design must ensure that the vddshvn rail is never higher than 2.0 V above the vdds18v rail.
(9) vddshv8 is separated out to show support for dual voltage. If a dedicated LDO/supply source is used for vddshv8, then vddshv8 ramp down should occur at one of the two earliest points in the timing diagram. If vddshv8 is powered by the same supply source as the other vddshvn rails, then it is allowed to ramp down at either of the last two points in the timing diagram.

Figure 5-5 describes vddshv[1-7,9-11] Supplies Falling Before vdds18v Supplies Delta.

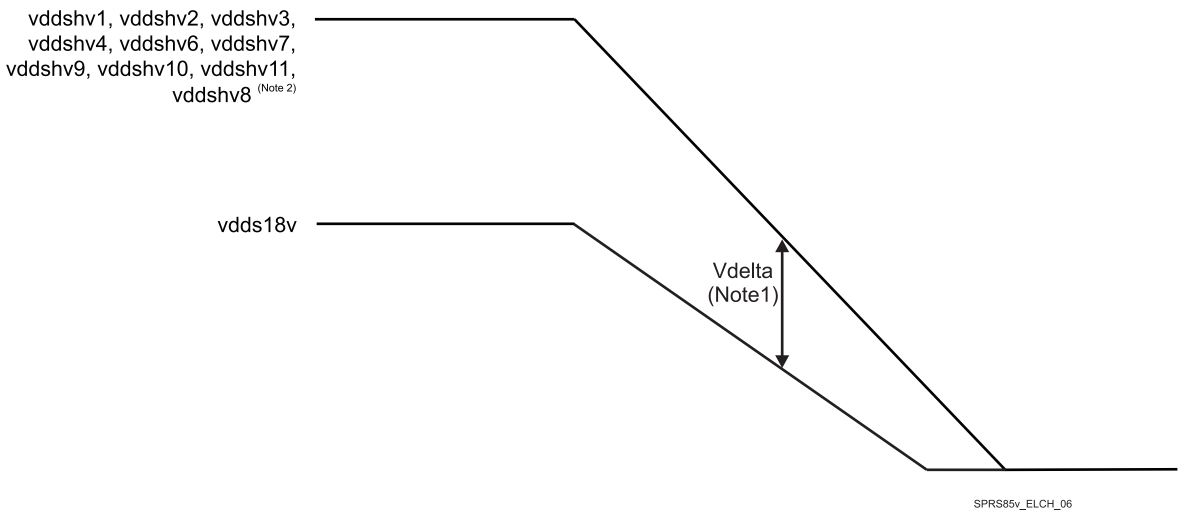


Figure 5-5. vdds18v versus vddshv[1-7, 9-11] Discharge Relationship

(1) Vdelta MAX = 2 V
(2) If vddshv8 is powered by the same supply source as the other vddshv[1-7,9-11] rails.

If vdds18v and vdds_ddr* are disabled at the same time due to a loss of input power event or if vdds_ddr* discharges more slowly than vdds18v, analysis has shown no reliability impacts when the elapsed time period beginning with vdds18v dropping below 1.0 V and ending with vdds_ddr* dropping below 0.6 V is less than 10 ms (Figure 5-6).

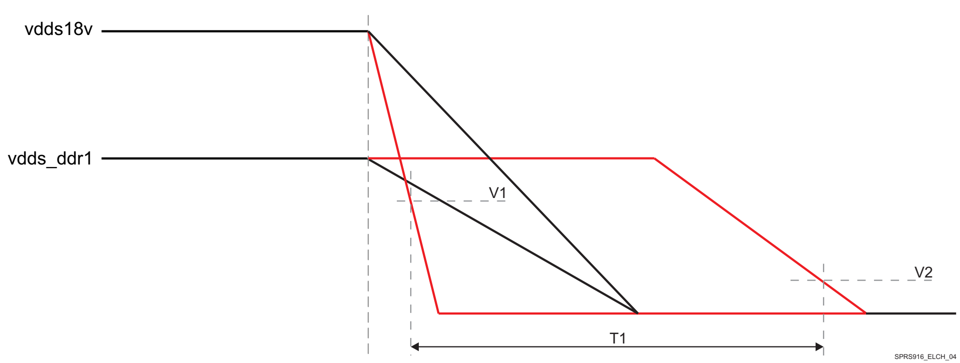


Figure 5-6. vdds18v and vdds_ddr* Discharge Relationship(1)

(1) V1 > 1.0 V; V2 < 0.6V; T1 < 10 ms.

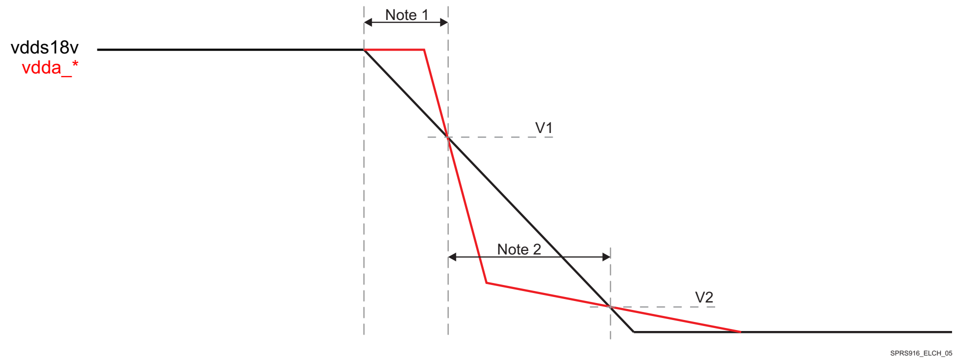


Figure 5-7. vdds18v and vdda_* Discharge Relationship(3)

(1) vdda_* can be ≥ vdds18v, until vdds18v drops below 1.62 V.

(2) vdds18v must be ≥ vdda_*, until vdds18v reaches 0.6 V.

(3) V1 = 1.62 V; V2 < 0.6 V.

Figure 5-5 through Figure 5-8 and associated notes described the device abrupt power down sequence.

A ”loss of input power event” occurs when the system’s input power is unexpectedly removed. Normally, the recommended power-down sequence should be followed and can be accomplished within 1.5-2 ms of elapsed time. This is the typical range of elapsed time available following a loss of power event, see Section 8.3.7 for design recommendations. If sufficient elapse time is not provided, then an “abrupt” power down sequence can be supported without impacting POH reliability if all of the following conditions are met (Figure 5-8).

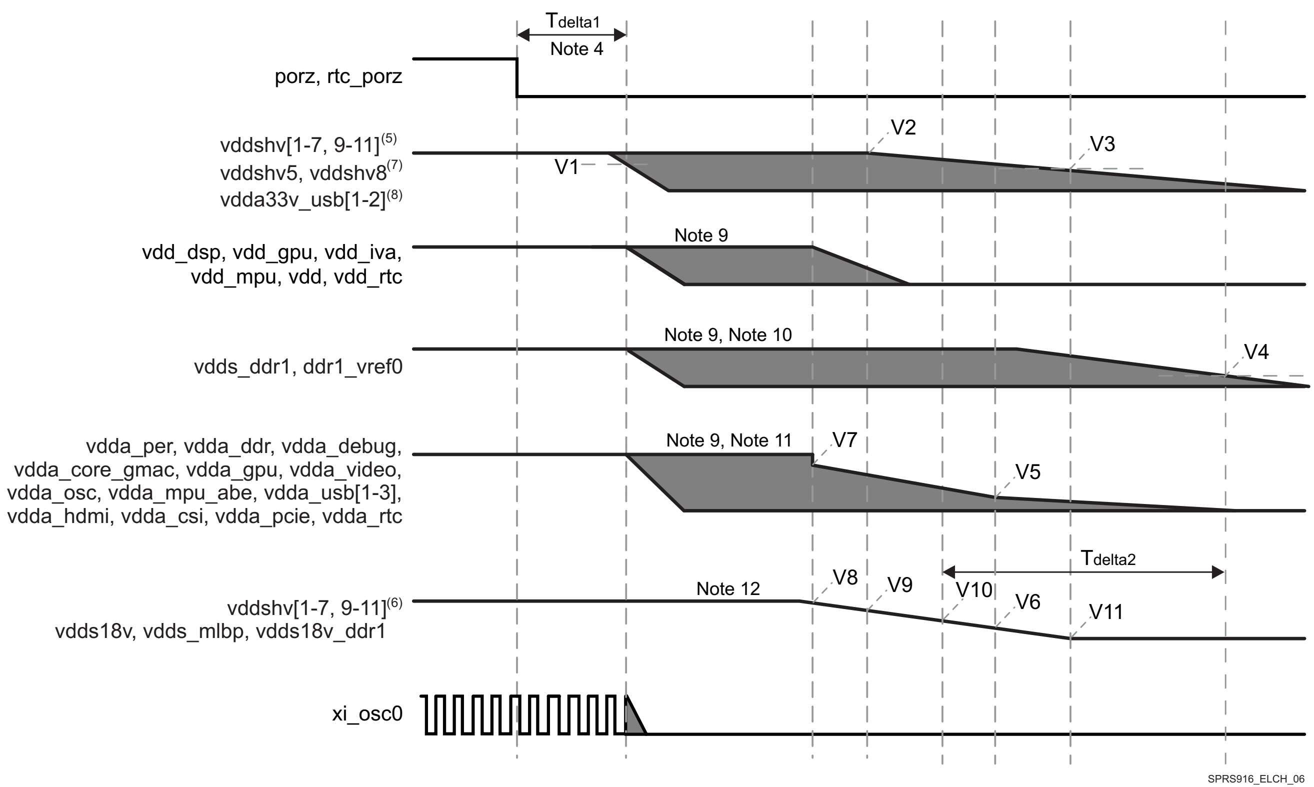


Figure 5-8. Abrupt Power-Down Sequencing(1)

(1) Time stamps:

– V1 = 2.7 V; V2 = 3.3 V; V3 = 2.0 V; V4 = V5 = V6 = 0.6 V; V7 = V8 = 1.62 V; V9 = 1.3 V; V10 = 1.0 V; V11 = 0.0 V; T_{delta1} > 100 µs; T_{delta2} < 10 ms.

(2) Terminology:

- $V_{OPR\ MIN}$ = Minimum Operational Voltage level that ensures device functionality and specified performance in Section 5.4, *Recommended Operating Conditions table*.
- V_{OFF} = OFF Voltage level is defined to be less than 0.6 V, where any current draw has no impact to POH.
- Ramp Down = transition time from $V_{OPR\ MIN}$ to V_{OFF} and is slew rate independent.

(3) General timing diagram items:

- Grey shaded areas show valid transition times for supplies between $V_{OPR\ MIN}$ and V_{OFF}.
- Dashed vertical lines show approximate elapse times based upon TI recommended PMIC power-down sequencer circuit performance.

(4) porz and rtc_porz must be asserted low for 100 µs min to ensure SoC is set to a safe functional state before any voltage begins to ramp down.

- Only if using RTC-mode with an independent RTC input power source, then rtc_porz can remain high and RTC-domains (vdd_rtc, vdda_rtc, and vddshv5) can remain energized while all other domains sourced from the system input power are powered down.

(5) vddshv[1-7, 9-11] domains supplied by 3.3 V:

- must remain greater than 2.7 V to enable Dual Voltage GPIO selector circuit operation for 100 µs min, after porz is asserted low.
- must not exceed vdds18v voltage level by more than 2 V during ramp down, until vdds18v drops below V_{OFF} (0.6 V).

(6) vddshv[1-7, 9-11] domains supplied by 1.8 V must ramp down concurrently with vdds18v and be sourced from common vdds18v supply.

(7) vddshv8 supporting SD Card:

- must be in first group of supplies to ramp down after porz has been asserted low for 100 µs min.
- must be sourced from independent power resource that can provide dual voltage (3.3 V / 1.8 V) operation as required to be compliant to SDIO specification.
- if SDIO operation is not needed, must be grouped with other vddshv[1-7, 9-11] domains.

(8) vdda33v_usb[1-2] domains must be in first group of supplies to ramp down after porz has been asserted low for 100 µs min.

(9) vdd_dsp, vdd_gpu, vdd_iva, vdd_mpu, vdd, vdd_rtc, vdds_ddr1, vdda_* domains can all start to ramp down in any order after 100 µs low assertion of porz.

(10) vdds_ddr1 domains:

- can remain at $V_{OPR\ MIN}$ or a level greater than vdds18v during ramp down.
- elapsed time from vdds18v dropping below 1.0 V to vdds_ddr[1-3] dropping below 0.6 V must not exceed 10 ms.

(11) vdda_* domains:

- can start to ramp down before or concurrently with vdds18v.
- must not exceed vdds18v voltage level after vdds18v drops below 1.62 V until vdds18v drops below V_{OFF} (0.6 V).

(12) vdds18v domain should maintain a minimum level of 1.62 V (V_{NOM} – 10%) until vdd_dsp and vdd start to ramp down.

6 Clock Specifications

NOTE

For more information, see *Power, Reset, and Clock Management* chapter in the device TRM.

NOTE

Audio Back End (ABE) module is not supported for this family of devices, but “ABE” name is still present in some clock or DPLL names.

The device operation requires the following clocks:

- The 32 kHz frequency is used for low frequency operation. It supplies the wake-up domain for operation in lowest power mode. This is an optional clock and will be supplied by on chip divider + mux (FUNC_32K_CLK) incase it is not available on external pin.
- The system clocks, SYS_CLK1 (Mandatory) and SYS_CLK2 (Optional) are the main clock sources of the device. They supply the reference clock to the DPLLs as well as functional clock to several modules.

The Device also embeds an internal free-running 32-kHz oscillator that is always active as long as the the wake-up (WKUP) domain is supplied.

Figure 6-1 shows the external input clock sources and the output clocks to peripherals.

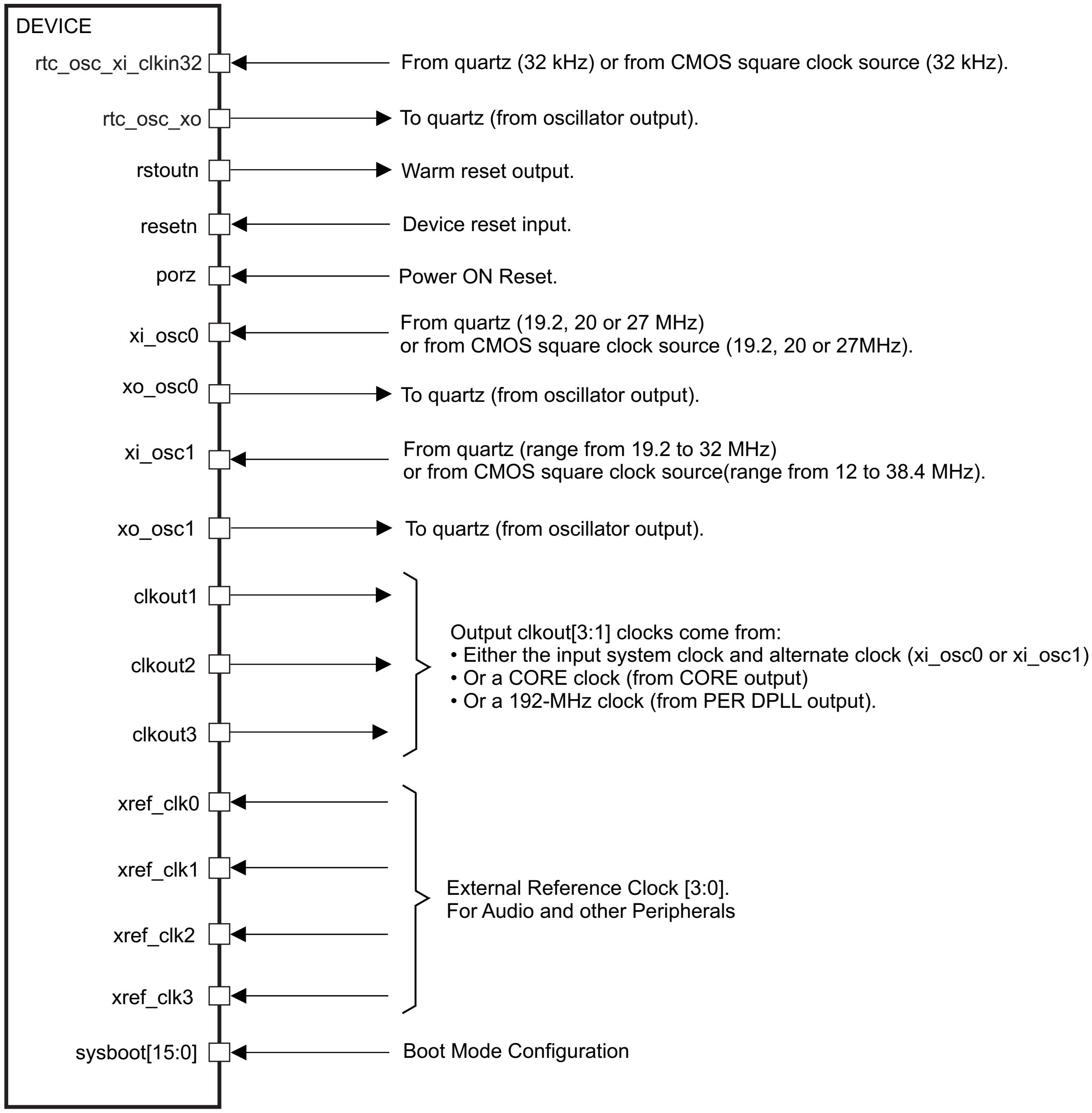


Figure 6-1. Clock Interface

6.1 Input Clock Specifications

6.1.1 Input Clock Requirements

- The source of the internal system clock (SYS_CLK1) could be either:
  - A CMOS clock that enters on the xi_osc0 ball (with xo_osc0 left unconnected on the CMOS clock case).
  - A crystal oscillator clock managed by xi_osc0 and xo_osc0.
- The source of the internal system clock (SYS_CLK2) could be either:
  - A CMOS clock that enters on the xi_osc1 ball (with xo_osc1 left unconnected on the CMOS clock case).
  - A crystal oscillator clock managed by xi_osc1 and xo_osc1.
- The source of the internal system clock (FUNC_32K_CLK) could be either:
  - A CMOS clock that enters on the rtc_osc_xi_clkin32 ball and supports external LVCMOS clock generators
  - A crystal oscillator clock managed by rtc_osc_xi_clkin32 and rtc_osc_xo.

6.1.2 System Oscillator OSC0 Input Clock

SYS_CLK1 is received directly from oscillator OSC0. For more information about SYS_CLK1, see *Power, Reset, and Clock Management* chapter in the device TRM.

6.1.2.1 OSC0 External Crystal

An external crystal is connected to the device pins. Figure 6-2 describes the crystal implementation.

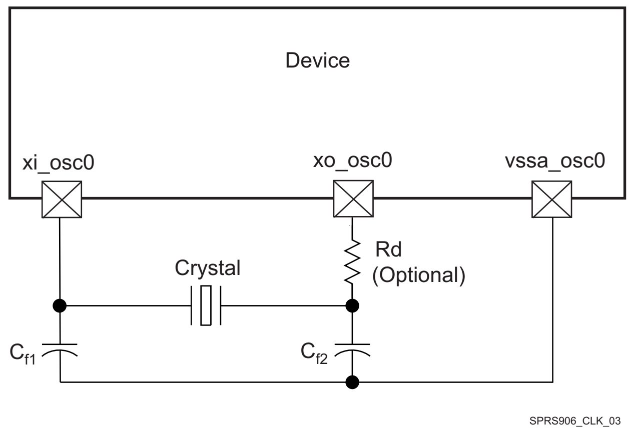


Figure 6-2. OSC0 Crystal Implementation

NOTE

The load capacitors, C_{f1} and C_{f2} in Figure 6-2, should be chosen such that the below equation is satisfied. C_L in the equation is the load specified by the crystal manufacturer. All discrete components used to implement the oscillator circuit should be placed as close as possible to the associated oscillator xi_osc0, xo_osc0, and vssa_osc0 pins.

$$C_L = \frac{C_{f1}C_{f2}}{(C_{f1}+C_{f2})}$$

Figure 6-3. Load Capacitance Equation

The crystal must be in the fundamental mode of operation and parallel resonant. Table 6-1 summarizes the required electrical constraints.

Table 6-1. OSC0 Crystal Electrical Characteristics

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
f_p	Parallel resonance crystal frequency		19.2, 20, 27		MHz
C_{f1}	C_{f1} load capacitance for crystal parallel resonance with $C_{f1} = C_{f2}$	12		24	pF
C_{f2}	C_{f2} load capacitance for crystal parallel resonance with $C_{f1} = C_{f2}$	12		24	pF
ESR(C_{f1},C_{f2}) (1)	Crystal ESR			100	Ω

Table 6-1. OSC0 Crystal Electrical Characteristics (continued)

NAME	DESCRIPTION			MIN	TYP	MAX	UNIT
C_O	Crystal shunt capacitance	ESR = 30 Ω ESR = 40 Ω	19.2 MHz, 20 MHz, 27 MHz			7	pF
		ESR = 50 Ω	19.2 MHz, 20 MHz			7	pF
			27 MHz			5	pF
		ESR = 60 Ω	19.2 MHz, 20 MHz			7	pF
			27 MHz		Not Supported		-
		ESR = 80 Ω	19.2 MHz, 20 MHz			5	pF
			27 MHz		Not Supported		-
		ESR = 100 Ω	19.2 MHz, 20 MHz			3	pF
			27 MHz		Not Supported		-
L_M	Crystal motional inductance for f_p = 20 MHz				10.16		mH
C_M	Crystal motional capacitance				3.42		fF
$t_{j(xiosc0)}$	Frequency accuracy(1), xi_osc0		Ethernet and MLB not used			±200	ppm
			Ethernet RGMII and RMII using derived clock			±50	ppm
			Ethernet MII using derived clock			±100	ppm
			MLB using derived clock			±50	ppm

(1) Crystal characteristics should account for tolerance+stability+aging.

When selecting a crystal, the system design must take into account the temperature and aging characteristics of a crystal versus the user environment and expected lifetime of the system.

Table 6-2 details the switching characteristics of the oscillator and the requirements of the input clock.

Table 6-2. Oscillator Switching Characteristics—Crystal Mode

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
f_p	Oscillation frequency		19.2, 20, 27 MHz		MHz
t_{sX}	Start-up time			4	ms

6.1.2.2 OSC0 Input Clock

A 1.8-V LVCMOS-Compatible Clock Input can be used instead of the internal oscillator to provide the SYS_CLK1 clock input to the system. The external connections to support this are shown in Figure 6-4. The xi_osc0 pin is connected to the 1.8-V LVCMOS-Compatible clock source. The xi_osc0 pin is left unconnected. The vssa_osc0 pin is connected to board ground (VSS).

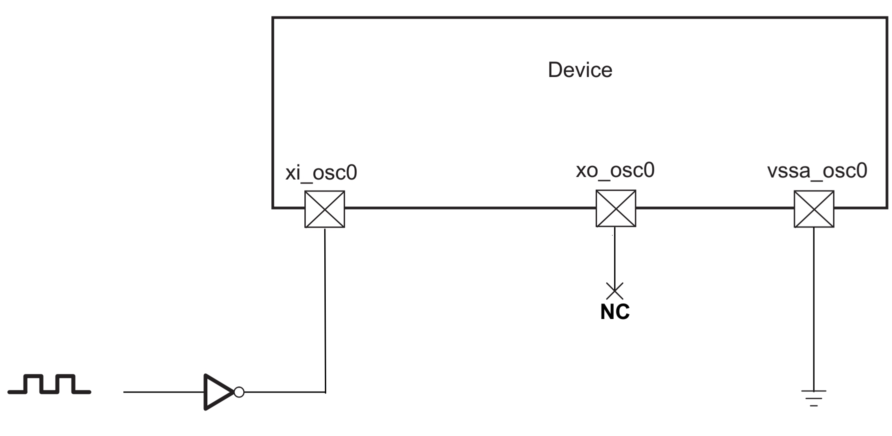


Figure 6-4. 1.8-V LVCMOS-Compatible Clock Input

Table 6-3 summarizes the OSC0 input clock electrical characteristics.

Table 6-3. OSC0 Input Clock Electrical Characteristics—Bypass Mode

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
f	Frequency		19.2, 20, 27		MHz
C_{IN}	Input capacitance	2.184	2.384	2.584	pF
I_{IN}	Input current (3.3V mode)	4	6	10	µA

Table 6-4 details the OSC0 input clock timing requirements.

Table 6-4. OSC0 Input Clock Timing Requirements

NAME		DESCRIPTION		MIN	TYP	MAX	UNIT
CK0	$1 / t_{c(xiosc0)}$	Frequency, xi_osc0			19.2, 20, 27		MHz
CK1	$t_{w(xiosc0)}$	Pulse duration, xi_osc0 low or high		$0.45 * t_{c(xiosc0)}$		$0.55 * t_{c(xiosc0)}$	ns
	$t_{j(xiosc0)}$	Period jitter[1], xi_osc0				$0.01 \times t_{c(xiosc0)}$	ns
	$t_{R(xiosc0)}$	Rise time, xi_osc0				5	ns
	$t_{F(xiosc0)}$	Fall time, xi_osc0				5	ns
	$t_{j(xiosc0)}$	Frequency accuracy[2], xi_osc0	Ethernet and MLB not used			±200	ppm
			Ethernet RGMII and RMII using derived clock			±50	
			Ethernet MII using derived clock			±100	
			MLB using derived clock			±50	

(1) Period jitter is meant here as follows:
– The maximum value is the difference between the longest measured clock period and the expected clock period
– The minimum value is the difference between the shortest measured clock period and the expected clock period
(2) Crystal characteristics should account for tolerance+stability+aging.

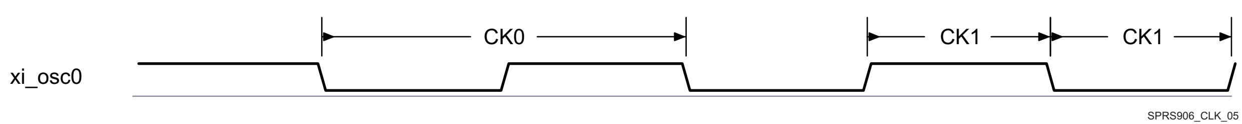


Figure 6-5. xi_osc0 Input Clock

6.1.3 Auxiliary Oscillator OSC1 Input Clock

SYS_CLK2 is received directly from oscillator OSC1. For more information about SYS_CLK2, see *Power, Reset, and Clock Management* chapter in the device TRM.

6.1.3.1 OSC1 External Crystal

An external crystal is connected to the device pins. Figure 6-6 describes the crystal implementation.

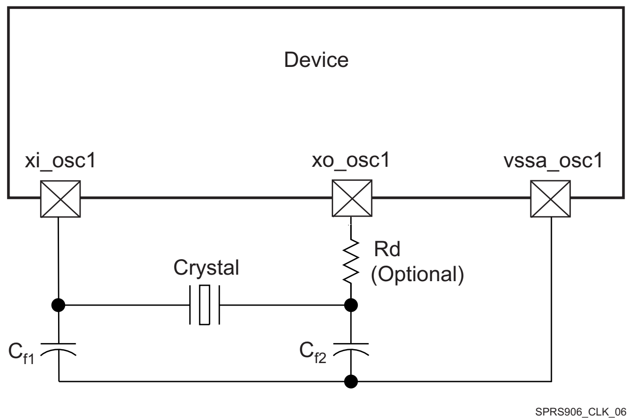


Figure 6-6. Crystal Implementation

NOTE

The load capacitors, C_{f1} and C_{f2} in Figure 6-6, should be chosen such that the below equation is satisfied. C_L in the equation is the load specified by the crystal manufacturer. All discrete components used to implement the oscillator circuit should be placed as close as possible to the associated oscillator xi_osc1, xo_osc1, and vssa_osc1 pins.

$$C_L = \frac{C_{f1} C_{f2}}{(C_{f1} + C_{f2})}$$

Figure 6-7. Load Capacitance Equation

The crystal must be in the fundamental mode of operation and parallel resonant. Table 6-5 summarizes the required electrical constraints.

Table 6-5. OSC1 Crystal Electrical Characteristics

NAME	DESCRIPTION			MIN	TYP	MAX	UNIT
f_p	Parallel resonance crystal frequency				Range from 19.2 to 32		MHz
C_{f1}	C_{f1} load capacitance for crystal parallel resonance with $C_{f1} = C_{f2}$			12		24	pF
C_{f2}	C_{f2} load capacitance for crystal parallel resonance with $C_{f1} = C_{f2}$			12		24	pF
ESR(C_{f1},C_{f2})	Crystal ESR					100	Ω
C_O	Crystal shunt capacitance	ESR = 30 Ω	19.2 MHz ≤ f_p ≤ 32 MHz			7	pF
		ESR = 40 Ω	19.2 MHz ≤ f_p ≤ 32 MHz			5	pF
		ESR = 50 Ω	19.2 MHz ≤ f_p ≤ 25 MHz			7	pF
			25 MHz < f_p ≤ 27 MHz			5	pF
			27 MHz < f_p ≤ 32 MHz		Not Supported		-
		ESR = 60 Ω	19.2 MHz ≤ f_p ≤ 23 MHz			7	pF
			23 MHz < f_p ≤ 25 MHz			5	pF
			25 MHz < f_p ≤ 32 MHz		Not Supported		-
		ESR = 80 Ω	19.2 MHz ≤ f_p ≤ 23 MHz			5	pF
			23 MHz ≤ f_p ≤ 25 MHz			3	pF
			25 MHz < f_p ≤ 32 MHz		Not Supported		-
		ESR = 100 Ω	19.2 MHz ≤ f_p ≤ 20 MHz			3	pF
			20 MHz < f_p ≤ 32 MHz		Not Supported		-
L_M	Crystal motional inductance for f_p = 20 MHz				10.16		mH
C_M	Crystal motional capacitance				3.42		fF

Table 6-5. OSC1 Crystal Electrical Characteristics (continued)

NAME	DESCRIPTION		MIN	TYP	MAX	UNIT
$t_{j(xiosc1)}$	Frequency accuracy(1), xi_osc1	Ethernet and MLB not used			±200	ppm
		Ethernet RGMII and RMII using derived clock			±50	
		Ethernet MII using derived clock			±100	
		MLB using derived clock			±50	

(1) Crystal characteristics should account for tolerance+stability+aging.

When selecting a crystal, the system design must take into account the temperature and aging characteristics of a crystal versus the user environment and expected lifetime of the system.

Table 6-6 details the switching characteristics of the oscillator and the requirements of the input clock.

Table 6-6. Oscillator Switching Characteristics—Crystal Mode

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
f_p	Oscillation frequency	Range from 19.2 to 32			MHz
t_{sX}	Start-up time			4	ms

6.1.3.2 OSC1 Input Clock

A 1.8-V LVCMOS-Compatible Clock Input can be used instead of the internal oscillator to provide the SYS_CLK2 clock input to the system. The external connections to support this are shown in, Figure 6-8. The xi_osc1 pin is connected to the 1.8-V LVCMOS-Compatible clock sources. The xo_osc1 pin is left unconnected. The vssa_osc1 pin is connected to board ground (vss).

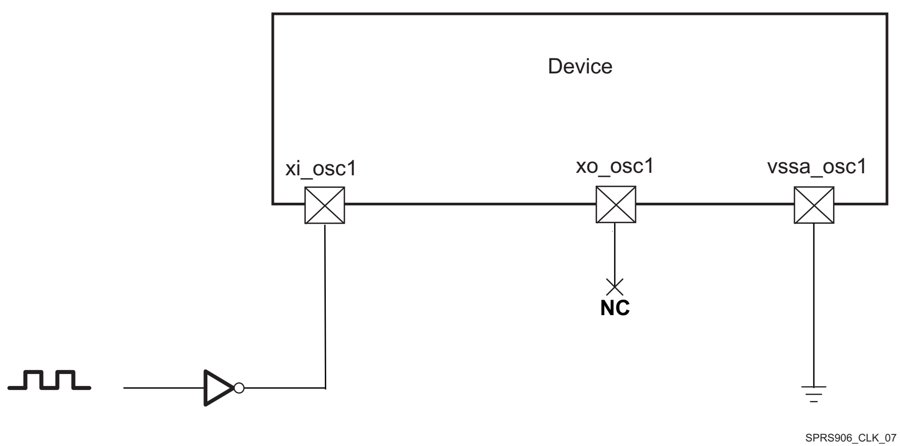


Figure 6-8. 1.8-V LVCMOS-Compatible Clock Input

Table 6-7 summarizes the OSC1 input clock electrical characteristics.

Table 6-7. OSC1 Input Clock Electrical Characteristics—Bypass Mode

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
f	Frequency	Range from 12 to 38.4			MHz
C_{IN}	Input capacitance	2.819	3.019	3.219	pF
I_{IN}	Input current (3.3V mode)	4	6	10	µA
t_{sX}	Start-up time(1)	See(2)			ms

(1) To switch from bypass mode to crystal or from crystal mode to bypass mode, there is a waiting time about 100 µs; however, if the chip comes from bypass mode to crystal mode the crystal will start-up after time mentioned in Table 6-6, t_{sX} parameter.

(2) Before the processor boots up and the oscillator is set to bypass mode, there is a waiting time when the internal oscillator is in application mode and receives a wave. The switching time in this case is about 100 µs.

Table 6-8 details the OSC1 input clock timing requirements.

Table 6-8. OSC1 Input Clock Timing Requirements

NAME	DESCRIPTION			MIN	TYP	MAX	UNIT
CK0	1 / $t_{c(xiosc1)}$	Frequency, xi_osc1		Range from 12 to 38.4			MHz
CK1	$t_{w(xiosc1)}$	Pulse duration, xi_osc1 low or high		0.45 * $t_{c(xiosc1)}$		0.55 * $t_{c(xiosc1)}$	ns
	$t_{j(xiosc1)}$	Period jitter[1], xi_osc1				0.01 × $t_{c(xiosc1)}$[3]	ns
	$t_{R(xiosc1)}$	Rise time, xi_osc1				5	ns
	$t_{F(xiosc1)}$	Fall time, xi_osc1				5	ns
	$t_{j(xiosc1)}$	Frequency accuracy[2], xi_osc1	Ethernet and MLB not used			±200	ppm
			Ethernet RGMII and RMII using derived clock			±50	
			Ethernet MII using derived clock			±100	
			MLB using derived clock			±50	

(1) Period jitter is meant here as follows:
- The maximum value is the difference between the longest measured clock period and the expected clock period
- The minimum value is the difference between the shortest measured clock period and the expected clock period

(2) Crystal characteristics should account for tolerance+stability+aging.

(3) The Period jitter requirement for osc1 can be relaxed to 0.02*tc(xiosc1) under the following constraints:
a.The osc1/SYS_CLK2 clock bypasses all device PLLs
b.The osc1/SYS_CLK2 clock is only used to source the DSS pixel clock outputs

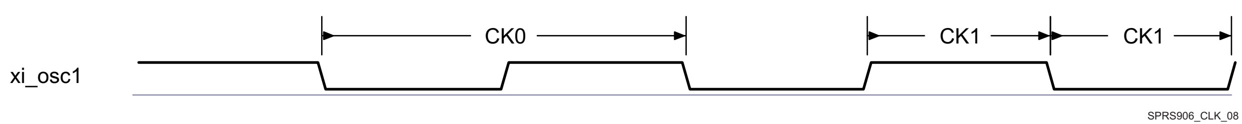


Figure 6-9. xi_osc1 Input Clock

6.1.4 RTC Oscillator Input Clock

FUNC_32K_CLK is received directly from RTC oscillator. For more information about FUNC_32K_CLK, see *Power, Reset, and Clock Management* chapter in the device TRM.

6.1.4.1 RTC Oscillator External Crystal

An external crystal is connected to the device pins. Figure 6-10 describes the crystal implementation.

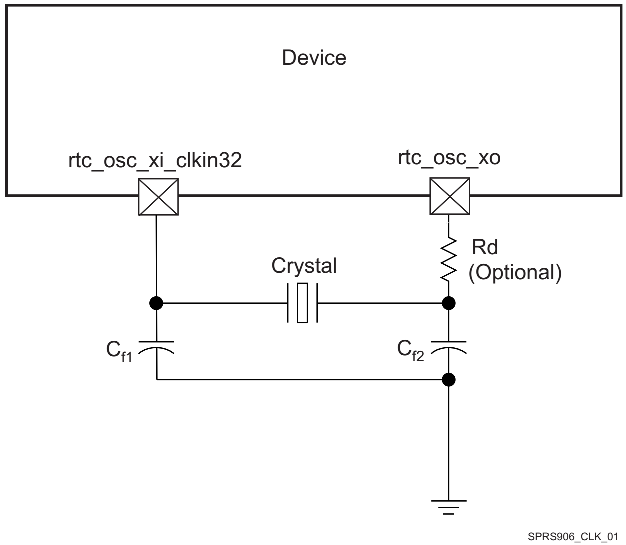


Figure 6-10. Crystal Implementation

NOTE

The load capacitors, C_{f1} and C_{f2} in Figure 6-10, should be chosen such that the below equation is satisfied. C_L in the equation is the load specified by the crystal manufacturer. All discrete components used to implement the oscillator circuit should be placed as close as possible to the associated oscillator rtc_osc_xi_clkin32 and rtc_osc_xo pins.

$$C_L = \frac{C_{f1} C_{f2}}{(C_{f1} + C_{f2})}$$

Figure 6-11. Load Capacitance Equation

The crystal must be in the fundamental mode of operation and parallel resonant. Table 6-9 summarizes the required electrical constraints.

Table 6-9. RTC Crystal Electrical Characteristics

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
f_p	Parallel resonance crystal frequency		32.768		kHz
C_{f1}	C_{f1} load capacitance for crystal parallel resonance with $C_{f1} = C_{f2}$	12		24	pF
C_{f2}	C_{f2} load capacitance for crystal parallel resonance with $C_{f1} = C_{f2}$	12		24	pF
$ESR(C_{f1},C_{f2})$	Crystal ESR			80	kΩ
C_O	Crystal shunt capacitance			5	pF
L_M	Crystal motional inductance for f_p = 32,768 kHz		10.7		mH
C_M	Crystal motional capacitance		2.2		fF
$t_{j(rtc\_osc\_xi\_clkin32)}$	Frequency accuracy, rtc_osc_xi_clkin32			±200	ppm

When selecting a crystal, the system design must take into account the temperature and aging characteristics of a crystal versus the user environment and expected lifetime of the system.

Table 6-10 details the switching characteristics of the oscillator and the requirements of the input clock.

Table 6-10. Oscillator Switching Characteristics—Crystal Mode

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
f_p	Oscillation frequency		32.768		kHz

Table 6-10. Oscillator Switching Characteristics—Crystal Mode (continued)

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
t_{sX}	Start-up time			4	ms

6.1.4.2 RTC Oscillator Input Clock

A 1.8-V LVCMOS-Compatible Clock Input can be used instead of the internal oscillator to provide the FUNC_32K_CLK clock input to the system. The external connections to support this are shown in Figure 6-12. The rtc_osc_xi_clkin32 pin is connected to the 1.8-V LVCMOS-Compatible clock sources. The rtc_osc_xo pin is left unconnected.

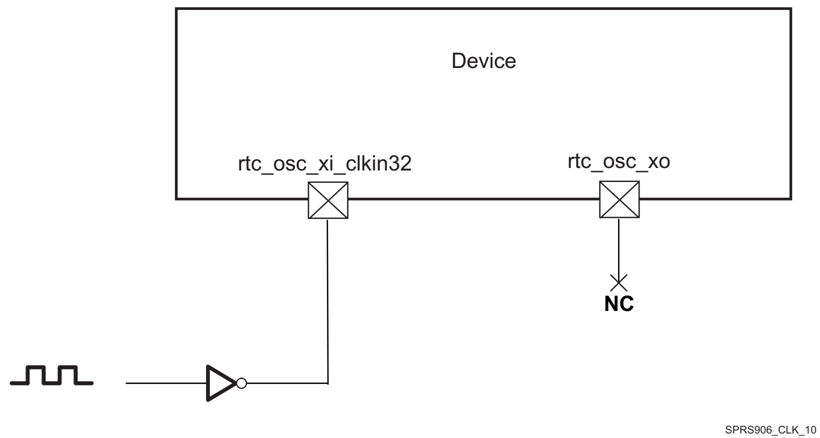


Figure 6-12. LVCMOS-Compatible Clock Input

Table 6-11 summarizes the RTC Oscillator input clock electrical characteristics.

Table 6-11. RTC Oscillator Input Clock Electrical Characteristics—Bypass Mode

NAME		DESCRIPTION	MIN	TYP	MAX	UNIT
CK0	$1/t_{c(rtc\_osc\_xi\_clkin32)}$	Frequency, rtc_osc_xi_clkin32		32.768		kHz
CK1	$t_{w(rtc\_osc\_xi\_clkin32)}$	Pulse duration, rtc_osc_xi_clkin32 low or high	0.45 * $t_{c(rtc\_osc\_xi\_clkin32)}$		0.55 * $t_{c(rtc\_osc\_xi\_clkin32)}$	ns
	C_{IN}	Input capacitance	2.178	2.378	2.578	pF
	I_{IN}	Input current (3.3V mode)	4	6	10	µA
	t_{sX}	Start-up time		See (1)		ms

(1) Before the processor boots up and the oscillator is set to bypass mode, there is a waiting time when the internal oscillator is inapplication mode and receives a wave. The switching time in this case is about 100 µs.

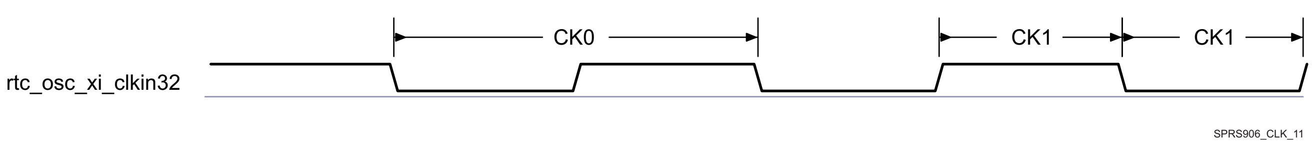


Figure 6-13. rtc_osc_xi_clkin32 Input Clock

6.1.4.3 RC On-die Oscillator Clock

NOTE

The OSC_32K_CLK clock, provided by the On-die 32K RC oscillator, inside of the SoC, is not accurate 32kHz clock.

The frequency may significantly vary with temperature and silicon characteristics.

For more information about OSC_32K_CLK, see *Power, Reset, and Clock Management* chapter in the device TRM.

6.2 DPLLs, DLLs Specifications

NOTE

For more information, see *Power, Reset, and Clock Management* and *Display Subsystem* chapters in the device TRM.

To generate high-frequency clocks, the device supports multiple on-chip DPLLs controlled directly by the PRCM module. They are of two types: type A and type B DPLLs.

- They have their own independent power domain (each one embeds its own switch and can be controlled as an independent functional power domain)
- They are fed with ALWAYS ON system clock, with independent control per DPLL.

The different DPLLs managed by the PRCM are listed below:

- DPLL_MPU: It supplies the MPU subsystem clocking internally.
- DPLL_IVA: It feeds the IVA subsystem clocking.
- DPLL_CORE: It supplies all interface clocks and also few module functional clocks.
- DPLL_PER: It supplies several clock sources: a 192-MHz clock for the display functional clock, a 96-MHz functional clock to subsystems and peripherals.
- DPLL_ABE: It provides clocks to various modules within the device.
- DPLL_USB: It provides 960M clock for USB modules (USB1/2/3/4).
- DPLL_GMAC: It supplies several clocks for the Gigabit Ethernet Switch (GMAC_SW).
- DPLL_DSP: It feeds the DSP Subsystem clocking.
- DPLL_GPU: It supplies clock for the GPU Subsystem.
- DPLL_DDR: It generates clocks for the two External Memory Interface (EMIF) controllers and their associated EMIF PHYs.
- DPLL_PCIE_REF: It provides reference clock for the APLL_PCIE in PCIE Subsystem.
- APLL_PCIE: It feeds clocks for the device Peripheral Component Interconnect Express (PCIe) controllers.

NOTE

The following DPLLs are controlled by the clock manager located in the always-on Core power domain (CM_CORE_AON):

- DPLL_MPU, DPLL_IVA, DPLL_CORE, DPLL_ABE, DPLL_DDR, DPLL_GMAC, DPLL_PCIE_REF, DPLL_PER, DPLL_USB, DPLL_DSP, DPLL_GPU, APLL_PCIE_REF.

For more information on CM_CORE_AON and CM_CORE or PRCM DPLLs, see *Power, Reset, and Clock Management* chapter in the device TRM.

The following DPLLs are not managed by the PRCM:

- DPLL_VIDEO1; (It is controlled from DSS)
- DPLL_HDMI; (It is controlled from DSS)
- DPLL_SATA; (It is controlled from SATA)
- DPLL_DEBUG; (It is controlled from DEBUGSS)
- DPLL_USB_OTG_SS; (It is controlled from OCP2SCP1)

NOTE

For more information for not controlled from PRCM DPLL's see the related chapters in TRM.

6.2.1 DPLL Characteristics

The DPLL has three relevant input clocks. One of them is the reference clock (CLKINP) used to generated the synthesized clock but can also be used as the bypass clock whenever the DPLL enters a bypass mode. It is therefore mandatory. The second one is a fast bypass clock (CLKINPULOW) used when selected as the bypass clock and is optional. The third clock (CLKINPHIF) is explained in the next paragraph.

The DPLL has three output clocks (namely CLKOUT, CLKOUTX2, and CLKOUTHIF). CLKOUT and CLKOUTX2 run at the bypass frequency whenever the DPLL enters a bypass mode. Both of them are generated from the lock frequency divided by a post-divider (namely M2 post-divider). The third clock, CLKOUTHIF, has no automatic bypass capability. It is an output of a post-divider (M3 post-divider) with the input clock selectable between the internal lock clock (Fdpll) and CLKINPHIF input of the PLL through an asynchronous multplexing.

For more information, see *Power, Reset, and Clock Management* chapter in the device TRM.

Table 6-12 summarizes DPLL type described in Section 6.2, *DPLLs, DLLs Specifications* introduction.

Table 6-12. DPLL Control Type

DPLL NAME	TYPE	CONTROLLED BY PRCM
DPLL_ABE	Table 6-13 (Type A)	Yes(1)
DPLL_CORE	Table 6-13 (Type A)	Yes(1)
DPLL_DEBUGSS	Table 6-13 (Type A)	No
DPLL_DSP	Table 6-13 (Type A)	Yes(1)
DPLL_GMAC	Table 6-13 (Type A)	Yes(1)
DPLL_HDMI	Table 6-14 (Type B)	No
DPLL_IVA	Table 6-13 (Type A)	Yes(1)
DPLL_MPU	Table 6-13 (Type A)	Yes(1)
DPLL_PER	Table 6-13 (Type A)	Yes(1)
APLL_PCIE	Table 6-13 (Type A)	Yes(1)
DPLL_PCIE_REF	Table 6-14 (Type B)	Yes(1)
DPLL_SATA	Table 6-14 (Type B)	No
DPLL_USB	Table 6-14 (Type B)	Yes(1)
DPLL_USB_OTG_SS	Table 6-14 (Type B)	No
DPLL_VIDEO1	Table 6-13 (Type A)	No
DPLL_DDR	Table 6-13 (Type A)	Yes(1)
DPLL_GPU	Table 6-13 (Type A)	Yes(1)

(1) DPLL is in the always-on domain.

Table 6-13 and Table 6-14 summarize the DPLL characteristics and assume testing over recommended operating conditions.

Table 6-13. DPLL Type A Characteristics

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT	COMMENTS
f_{input}	CLKINP input frequency	0.032		52	MHz	F_{INP}
$f_{internal}$	Internal reference frequency	0.15		52	MHz	REFCLK
$f_{CLKINPHIF}$	CLKINPHIF input frequency	10		1400	MHz	F_{INPHIF}

Table 6-13. DPLL Type A Characteristics (continued)

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT	COMMENTS
$f_{CLKINPULOW}$	CLKINPULOW input frequency	0.001		600	MHz	Bypass mode: f_{CLKOUT} = $f_{CLKINPULOW}$ / (M1 + 1) if ulowclken = 1[6]
f_{CLKOUT}	CLKOUT output frequency	20[1]		1800[2]	MHz	[M / (N + 1)] × F_{INP} × [1 / M2] (in locked condition)
$f_{CLKOUTx2}$	CLKOUTx2 output frequency	40[1]		2200[2]	MHz	2 × [M / (N + 1)] × F_{INP} × [1 / M2] (in locked condition)
$f_{CLKOUTHIF}$	CLKOUTHIF output frequency	20[3]		1400[4]	MHz	F_{INPHIF} / M3 if clkinphifsel = 1
		40[3]		2200[4]	MHz	2 × [M / (N + 1)] × F_{INP} × [1 / M3] if clkinphifsel = 0
$f_{CLKDCOLDO}$	DCOCLKLDO output frequency	40		2800	MHz	2 × [M / (N + 1)] × F_{INP} (in locked condition)
t_{lock}	Frequency lock time			6 + 350 × REFCLK	µs	
p_{lock}	Phase lock time			6 + 500 × REFCLK	µs	
$t_{relock-L}$	Relock time—Frequency lock[5] (LP relock time from bypass)			6 + 70 × REFCLK	µs	DPLL in LP relock time: lowcurrstdby = 1
$p_{relock-L}$	Relock time—Phase lock[5] (LP relock time from bypass)			6 + 120 × REFCLK	µs	DPLL in LP relock time: lowcurrstdby = 1
$t_{relock-F}$	Relock time—Frequency lock[5] (fast relock time from bypass)			3.55 + 70 × REFCLK	µs	DPLL in fast relock time: lowcurrstdby = 0
$p_{relock-F}$	Relock time—Phase lock[5] (fast relock time from bypass)			3.55 + 120 × REFCLK	µs	DPLL in fast relock time: lowcurrstdby = 0

(1) The minimum frequencies on CLKOUT and CLKOUTX2 are assuming M2 = 1.

For M2 > 1, the minimum frequency on these clocks will further scale down by factor of M2.

(2) The maximum frequencies on CLKOUT and CLKOUTX2 are assuming M2 = 1.

(3) The minimum frequency on CLKOUTHIF is assuming M3 = 1. For M3 > 1, the minimum frequency on this clock will further scale down by factor of M3.

(4) The maximum frequency on CLKOUTHIF is assuming M3 = 1.

(5) Relock time assumes typical operating conditions, 10°C maximum temperature drift.

(6) Bypass mode: f_{CLKOUT} = F_{INP} if ulowclken = 0. For more information, see the device TRM.

Table 6-14. DPLL Type B Characteristics

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT	COMMENTS
f_{input}	CLKINP input clock frequency	0.62		60	MHz	F_{INP}
$f_{internal}$	REFCLK internal reference clock frequency	0.62		2.5	MHz	[1 / (N + 1)] × F_{INP}
$f_{CLKINPULOW}$	CLKINPULOW bypass input clock frequency	0.001		600	MHz	Bypass mode: f_{CLKOUT} = $f_{CLKINPULOW}$ / (M1 + 1) If ulowclken = 1[4]
$f_{CLKLDOOUT}$	CLKOUTLDO output clock frequency	20[1][5]		2500[2][5]	MHz	M / (N + 1)] × F_{INP} × [1 / M2] (in locked condition)
f_{CLKOUT}	CLKOUT output clock frequency	20[1][5]		1450[2][5]	MHz	[M / (N + 1)] × F_{INP} × [1 / M2] (in locked condition)
$f_{CLKDCOLDO}$	Internal oscillator (DCO) output clock frequency	750[5]		1500[5]	MHz	[M / (N + 1)] × F_{INP} (in locked condition)
		1250[5]		2500[5]	MHz	
t_J	CLKOUTLDO period jitter	–2.5%		2.5%		The period jitter at the output clocks is ± 2.5% peak to peak
	CLKOUT period jitter					
	CLKDCOLDO period jitter					
t_{lock}	Frequency lock time			350 × REFCLKs	µs	

Table 6-14. DPLL Type B Characteristics (continued)

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT	COMMENTS
p_{lock}	Phase lock time			500 × REFCLKs	µs	
$t_{relock-L}$	Relock time—Frequency lock(3) (LP relock time from bypass)			9 + 30 × REFCLKs	µs	
$p_{relock-L}$	Relock time—Phase lock(3) (LP relock time from bypass)			9 + 125 × REFCLKs	µs	

(1) The minimum frequency on CLKOUT is assuming M2 = 1.

For M2 > 1, the minimum frequency on this clock will further scale down by factor of M2.

(2) The maximum frequency on CLKOUT is assuming M2 = 1.

(3) Relock time assumes typical operating conditions, 10°C maximum temperature drift.

(4) Bypass mode: $f_{CLKOUT} = F_{INP}$ if ULOWCLKEN = 0. For more information, see the device TRM.

(5) For output clocks, there are two frequency ranges according to the SELFREQDCO setting. For more information, see the device TRM.

6.2.2 DLL Characteristics

Table 6-15 summarizes the DLL characteristics and assumes testing over recommended operating conditions.

Table 6-15. DLL Characteristics

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
f_{input}	Input clock frequency (EMIF_DLL_FCLK)			333	MHz
t_{lock}	Lock time			50k	cycles
t_{relock}	Relock time (a change of the DLL frequency implies that DLL must relock)			50k	cycles

6.2.3 DPLL and DLL Noise Isolation

NOTE

For more information on DPLL and DLL decoupling capacitor requirements, see *Core Power Domains* section.

7 Timing Requirements and Switching Characteristics

7.1 Timing Test Conditions

All timing requirements and switching characteristics are valid over the recommended operating conditions unless otherwise specified.

7.2 Interface Clock Specifications

7.2.1 Interface Clock Terminology

The interface clock is used at the system level to sequence the data and/or to control transfers accordingly with the interface protocol.

7.2.2 Interface Clock Frequency

The two interface clock characteristics are:

- The maximum clock frequency
- The maximum operating frequency

The interface clock frequency documented in this document is the maximum clock frequency, which corresponds to the maximum frequency programmable on this output clock. This frequency defines the maximum limit supported by the Device IC and does not take into account any system consideration (PCB, peripherals).

The system designer will have to consider these system considerations and the Device IC timing characteristics as well to define properly the maximum operating frequency that corresponds to the maximum frequency supported to transfer the data on this interface.

7.3 Timing Parameters and Information

The timing parameter symbols used in the timing requirement and switching characteristic tables are created in accordance with JEDEC Standard 100. To shorten the symbols, some of pin names and other related terminologies have been abbreviated as follows:

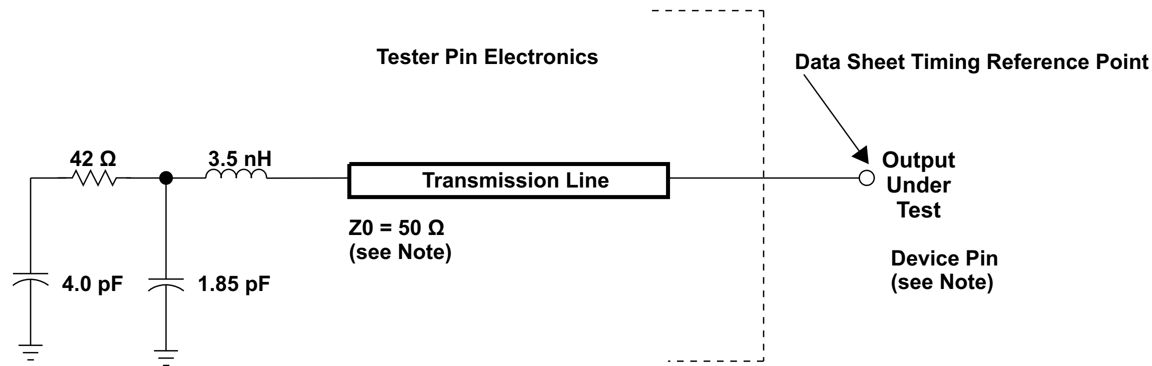
Table 7-1. Timing Parameters

SUBSCRIPTS	
SYMBOL	**PARAMETER**
c	Cycle time (period)
d	Delay time
dis	Disable time
en	Enable time
h	Hold time
su	Setup time
START	Start bit
t	Transition time
v	Valid time
w	Pulse duration (width)
X	Unknown, changing, or don't care level
F	Fall time
H	High
L	Low
R	Rise time
V	Valid
IV	Invalid

Table 7-1. Timing Parameters (continued)

SUBSCRIPTS	
SYMBOL	PARAMETER
AE	Active Edge
FE	First Edge
LE	Last Edge
Z	High impedance

7.3.1 Parameter Information



NOTE: The data sheet provides timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account. A transmission line with a delay of 2 ns can be used to produce the desired transmission line effect. The transmission line is intended as a load only. It is not necessary to add or subtract the transmission line delay (2 ns) from the data sheet timings.

Input requirements in this data sheet are tested with an input slew rate of < 4 Volts per nanosecond (4 V/ns) at the device pin.

pm_tstcirc_prs403

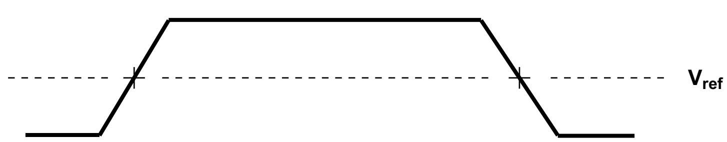
Figure 7-1. Test Load Circuit for AC Timing Measurements

The load capacitance value stated is only for characterization and measurement of AC timing signals.

This load capacitance value does not indicate the maximum load the device is capable of driving.

7.3.1.1 1.8V and 3.3V Signal Transition Levels

All input and output timing parameters are referenced to V_{ref} for both "0" and "1" logic levels. V_{ref} = (VDD I/O)/2.



pm_io_volt_prs403

Figure 7-2. Input and Output Voltage Reference Levels for AC Timing Measurements

All rise and fall transition timing parameters are referenced to V_{IL} MAX and V_{IH} MIN for input clocks, V_{OL} MAX and V_{OH} MIN for output clocks.

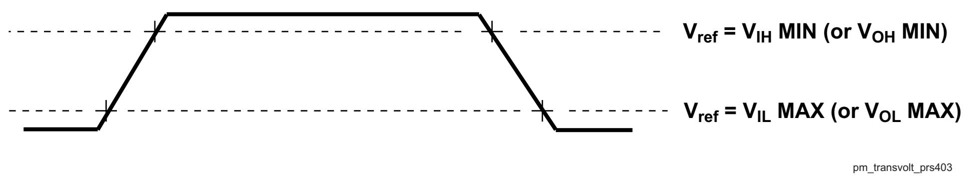


Figure 7-3. Rise and Fall Transition Time Voltage Reference Levels

7.3.1.2 1.8V and 3.3V Signal Transition Rates

The default SLEWCONTROL settings in each pad configuration register must be used to ensure timings, unless specific instructions otherwise are given in the individual timing sub-sections of the datasheet.

All timings are tested with an input edge rate of 4 volts per nanosecond (4 V/ns).

7.3.1.3 Timing Parameters and Board Routing Analysis

The timing parameter values specified in this data manual do not include delays by board routes. As a good board design practice, such delays must *always* be taken into account. Timing values may be adjusted by increasing/decreasing such delays. TI recommends using the available I/O buffer information specification (IBIS) models to analyze the timing characteristics correctly. To properly use IBIS models to attain accurate timing analysis for a given system, see the Using IBIS Models for timing Analysis. If needed, external logic hardware such as buffers may be used to compensate any timing differences.

7.4 Recommended Clock and Control Signal Transition Behavior

All clocks and control signals ***must*** transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner. Monotonic transitions are more easily ensure with faster switching signals. Slower input transitions are more susceptible to glitches due to noise and special care should be taken for slow input clocks.

7.5 Virtual and Manual I/O Timing Modes

Some of the timings described in the following sections require the use of Virtual or Manual I/O Timing Modes. Table 7-2 provides a summary of the Virtual and Manual I/O Timing Modes across all device interfaces. The individual interface timing sections found later in this document provide the full description of each applicable Virtual and Manual I/O Timing Mode. Refer to the "Pad Configuration" section of the TRM for the procedure on implementing the Virtual and Manual Timing Modes in a system.

Table 7-2. Modes Summary

VIRTUAL OR MANUAL IO MODE NAME	DATA MANUAL TIMING MODE
DPI VIDEO OUTPUT	
No Virtual or Manual IO Timing Mode Required	DPI1/3 Video Output Default Timings - Rising-edge Clock Reference
DSS_VIRTUAL1	DPI1/3 Video Output Default Timings - Falling-edge Clock Reference
VOUT1_MANUAL1	DPI1 Video Output Alternate Timings
VOUT1_MANUAL4	DPI1 Video Output MANUAL4 Timings
VOUT1_MANUAL5	DPI1 Video Output MANUAL5 Timings
VOUT2_IOSET1_MANUAL1	DPI2 Video Output IOSET1 Alternate Timings
VOUT2_IOSET1_MANUAL2	DPI2 Video Output IOSET1 Default Timings - Rising-edge Clock Reference
VOUT2_IOSET1_MANUAL3	DPI2 Video Output IOSET1 Default Timings - Falling-edge Clock Reference
VOUT2_IOSET1_MANUAL4	DPI2 Video Output IOSET1 MANUAL4 Timings
VOUT2_IOSET1_MANUAL5	DPI2 Video Output IOSET1 MANUAL5 Timings
VOUT2_IOSET2_MANUAL1	DPI2 Video Output IOSET2 Alternate Timings
VOUT2_IOSET2_MANUAL2	DPI2 Video Output IOSET2 Default Timings - Rising-edge Clock Reference
VOUT2_IOSET2_MANUAL3	DPI2 Video Output IOSET2 Default Timings - Falling-edge Clock Reference
VOUT2_IOSET2_MANUAL4	DPI2 Video Output IOSET2 MANUAL4 Timings

Table 7-2. Modes Summary (continued)

VIRTUAL OR MANUAL IO MODE NAME	DATA MANUAL TIMING MODE
VOUT2_IOSET2_MANUAL5	DPI2 Video Output IOSET2 MANUAL5 Timings
VOUT3_MANUAL1	DPI3 Video Output Alternate Timings
VOUT3_MANUAL4	DPI3 Video Output MANUAL4 Timings
VOUT3_MANUAL5	DPI3 Video Output MANUAL5 Timings
GPMC	
No Virtual or Manual IO Timing Mode Required	GPMC Asynchronous Mode Timings and Synchronous Mode - Default Timings
GPMC_VIRTUAL1	GPMC Synchronous Mode - Alternate Timings
McASP	
No Virtual or Manual IO Timing Mode Required	McASP1 Asynchronous and Synchronous Transmit Timings
MCASP1_VIRTUAL1_SYNC_RX	See Table 7-50
MCASP1_VIRTUAL2_ASYNC_RX	See Table 7-50
No Virtual or Manual IO Timing Mode Required	McASP2 Asynchronous and Synchronous Transmit Timings
MCASP2_VIRTUAL1_SYNC_RX_80M	See Table 7-51
MCASP2_VIRTUAL2_ASYNC_RX	See Table 7-51
MCASP2_VIRTUAL3_SYNC_RX	See Table 7-51
MCASP2_VIRTUAL4_ASYNC_RX_80M	See Table 7-51
No Virtual or Manual IO Timing Mode Required	McASP3 Synchronous Transmit Timings
MCASP3_VIRTUAL2_SYNC_RX	See Table 7-52
No Virtual or Manual IO Timing Mode Required	McASP4 Synchronous Transmit Timings
MCASP4_VIRTUAL1_SYNC_RX	See Table 7-53
No Virtual or Manual IO Timing Mode Required	McASP5 Synchronous Transmit Timings
MCASP5_VIRTUAL1_SYNC_RX	See Table 7-54
No Virtual or Manual IO Timing Mode Required	McASP6 Synchronous Transmit Timings
MCASP6_VIRTUAL1_SYNC_RX	See Table 7-55
No Virtual or Manual IO Timing Mode Required	McASP7 Synchronous Transmit Timings
MCASP7_VIRTUAL2_SYNC_RX	See Table 7-56
No Virtual or Manual IO Timing Mode Required	McASP8 Synchronous Transmit Timings
MCASP8_VIRTUAL1_SYNC_RX	See Table 7-57
eMMC/SD/SDIO	
No Virtual or Manual IO Timing Mode Required	MMC1 DS (Pad Loopback), HS (Internal Loopback and Pad Loopback), SDR12 (Internal Loopback and Pad Loopback), and SDR25 Timings (Internal Loopback and Pad Loopback) Timings
MMC1_VIRTUAL1	MMC1 SDR50 (Pad Loopback) Timings
MMC1_VIRTUAL4	MMC1 DS (Internal Loopback) Timings
MMC1_VIRTUAL5	MMC1 SDR50 (Internal Loopback) Timings
MMC1_VIRTUAL6	MMC1 DDR50 (Internal Loopback) Timings
MMC1_MANUAL1	MMC1 DDR50 (Pad Loopback) Timings
MMC1_MANUAL2	MMC1 SDR104 Timings
No Virtual or Manual IO Timing Mode Required	MMC2 Standard (Pad Loopback), High Speed (Pad Loopback) Timings
MMC2_VIRTUAL2	MMC2 Standard (Internal Loopback), High Speed (Internal Loopback) Timings
MMC2_MANUAL1	MMC2 DDR (Pad Loopback) Timings
MMC2_MANUAL2	MMC2 DDR (Internal Loopback Manual) Timings
MMC2_MANUAL3	MMC2 HS200 Timings
No Virtual or Manual IO Timing Mode Required	MMC3 DS, SDR12, HS, SDR25 Timings
MMC3_MANUAL1	MMC3 SDR50 Timings
No Virtual or Manual IO Timing Mode Required	MMC4 DS, SDR12, HS, SDR25 Timings
QSPI	
No Virtual or Manual IO Timing Mode Required	QSPI Mode 3 Timings

Table 7-2. Modes Summary (continued)

VIRTUAL OR MANUAL IO MODE NAME	DATA MANUAL TIMING MODE
QSPI1_MANUAL1	QSPI Mode 0 Timings
GMAC	
No Virtual or Manual IO Timing Mode Required	GMAC MII0/1 Timings
GMAC_RGMII0_MANUAL1	GMAC RGMII0 with Transmit Clock Internal Delay Enabled
GMAC_RGMII1_MANUAL1	GMAC RGMII1 with Transmit Clock Internal Delay Enabled
GMAC_RMII0_MANUAL1	GMAC RMII0 Timings
GMAC_RMII1_MANUAL1	GMAC RMII1 Timings
VIP	
VIP_MANUAL1	VIN1A (IOSET7) and VIN2A (IOSET10) Rise-Edge Capture Mode Timings
VIP_MANUAL2	VIN1A (IOSET7) and VIN2A (IOSET10) Fall-Edge Capture Mode Timings
VIP_MANUAL3	VIN2A (IOSET4/5/6) Rise-Edge Capture Mode Timings
VIP_MANUAL4	VIN2B (IOSET7/8/9) Rise-Edge Capture Mode Timings
VIP_MANUAL5	VIN2A (IOSET4/5/6) Fall-Edge Capture Mode Timings
VIP_MANUAL6	VIN2B (IOSET7/8/9) Fall-Edge Capture Mode Timings
VIP_MANUAL7	VIN1A (IOSET2/3/4) and VIN1B (IOSET4/7) and VIN2B (IOSET1/10) Rise-Edge Capture Mode Timings
VIP_MANUAL8	VIN1A (IOSET5/6) and VIN2A (IOSET7/8/9) Rise-Edge Capture Mode Timings
VIP_MANUAL9	VIN1B (IOSET6/7) Rise-Edge Capture Mode Timings
VIP_MANUAL10	VIN1B (IOSET5) and VIN2B (IOSET2/11) Rise-Edge Capture Mode Timings
VIP_MANUAL11	VIN1B (IOSET5) and VIN2B (IOSET2/11) Fall-Edge Capture Mode Timings
VIP_MANUAL12	VIN1A (IOSET2/3/4) and VIN1B (IOSET4/7) and VIN2B (IOSET1/10) Fall-Edge Capture Mode Timings
VIP_MANUAL13	VIN1A (IOSET5/6) and VIN2A (IOSET7/8/9) Fall-Edge Capture Mode Timings
VIP_MANUAL14	VIN1B (IOSET6/7) Fall-Edge Capture Mode Timings
VIP_MANUAL15	VIN1A (IOSET8/9/10) Rise-Edge Capture Mode Timings
VIP_MANUAL16	VIN1A (IOSET8/9/10) Fall-Edge Capture Mode Timings
HDMI, EMIF, Timers, I2C, HDQ/1-Wire, UART, McSPI, USB, SATA, PCIe, DCAN, GPIO, KBD, PWM, ATL, JTAG, TPIU, RTC, SDMA, INTC, MLB	
No Virtual or Manual IO Timing Mode Required	All Modes

7.6 Video Input Ports (VIP)

The Device includes 1 Video Input Ports (VIP).

Table 7-3, Figure 7-4 and Figure 7-5 present timings and switching characteristics of the VIPs.

> **CAUTION**
>
> The I/O timings provided in this section are valid only for VIN1 and VIN2 if signals within a single IOSET are used. The IOSETs are defined in Table 7-4 and Table 7-5.

Table 7-3. Timing Requirements for VIP (3)(4)(5)

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
V1	$t_{c(CLK)}$	Cycle time, vinx_clki (3) (5)	6.06 (2)		ns
V2	$t_{w(CLKH)}$	Pulse duration, vinx_clki high (3) (5)	0.45*P (2)		ns
V3	$t_{w(CLKL)}$	Pulse duration, vinx_clki low (3) (5)	0.45*P (2)		ns
V4	$t_{su(CTL/DATA-CLK)}$	Input setup time, Control (vinx_dei, vinx_vsynci, vinx_fldi, vinx_hsynci) and Data (vinx_dn) valid to vinx_clki transition (3) (4) (5)	3.11 (2)		ns

Table 7-3. Timing Requirements for VIP [(3)(4)(5)] (continued)

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
V6	$t_{h(CLK-CTL/DATA)}$	Input hold time, Control (vinx_dei, vinx_vsynci, vinx_fldi, vinx_hsynci) and Data (vinx_dn) valid from vinx_clki transition [(3)(4)(5)]	-0.05 [(2)]		ns

(1) For maximum frequency of 165 MHz.

(2) P = vinx_clki period.

(3) x in vinx = 1a, 1b, 2a, 2b.

(4) n in dn = 0 to 7 when x = 1b, 2b.
n = 0 to 23 when x = 1a, 2a.

(5) i in clki, dei, vsynci, hsynci and fldi = 0 or 1.

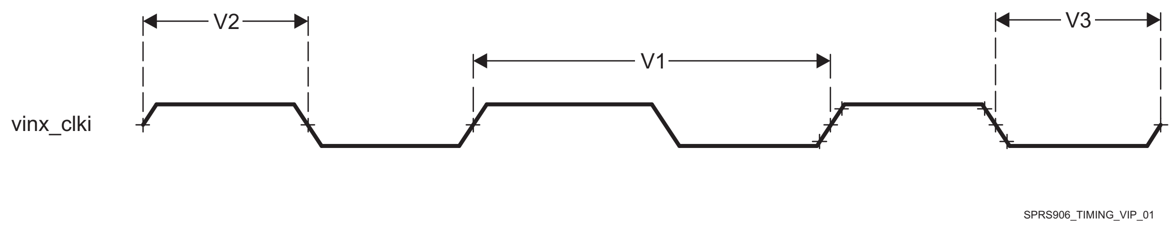


Figure 7-4. Video Input Ports clock signal

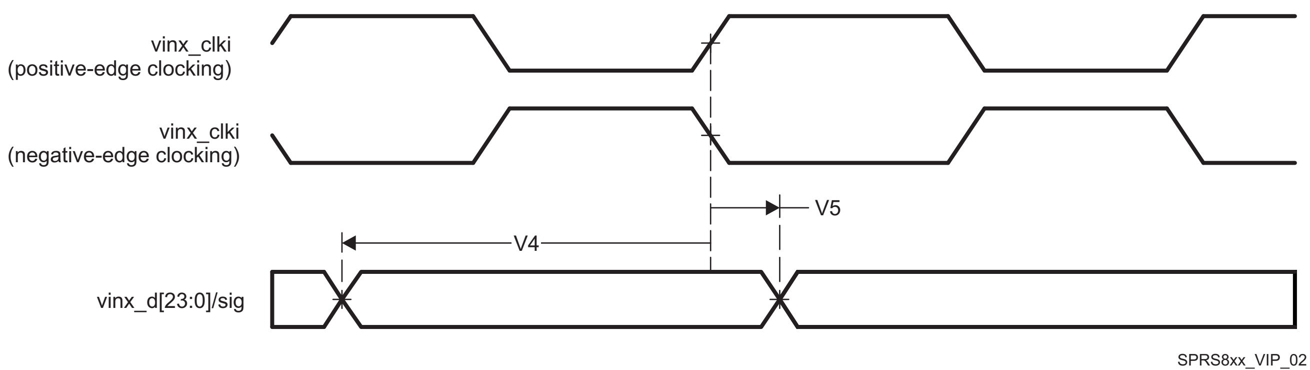


Figure 7-5. Video Input Ports timings

In Table 7-4 and Table 7-5 are presented the specific groupings of signals (IOSET) for use with vin1 and vin2.

Table 7-4. VIN1 IOSETs

SIGNALS	IOSET2		IOSET3		IOSET4 (1)		IOSET5 (1)		IOSET6 (1)		IOSET7 (1)		IOSET8		IOSET9		IOSET10	
	BALL	MUX	BALL	MUX	BALL	MUX	BALL	MUX	BALL	MUX	BALL	MUX	BALL	MUX	BALL	MUX	BALL	MUX
vin1a																		
vin1a_clk0	P1	2	B11	4	B11	3	P4	4	P4	4	B26	8	AC5	9	E17	7	E17	7
vin1a_hsync0	N7	2	C11	4	C11	3	R3	4	P7	4	E21	8	AB8	9	F12	7	F12	7
vin1a_vsync0	R4	2	E11	4	E11	3	T2	4	N1	4	F20	8	AB5	9	G12	7	G12	7
vin1a_fld0	P9	2	D11	4	D11	3	P9	4	J7	4	F21	8	C17	9	C14	7	C14	7
vin1a_de0	N9	2	B10	4	B10	3	P7	5	H6	4	C23	8	AB4	9	D14	7	D14	7
vin1a_d0	M6	2	B7	4	B7	3	R6	4	R6	4	B14	8	AD6	9	D18	7	C17	7
vin1a_d1	M2	2	B8	4	B8	3	T9	4	T9	4	J14	8	AC8	9	B19	7	B19	7
vin1a_d2	L5	2	A7	4	A7	3	T6	4	T6	4	G13	8	AC3	9	F15	7	F15	7
vin1a_d3	M1	2	A8	4	A8	3	T7	4	T7	4	J11	8	AC9	9	B18	7	B18	7
vin1a_d4	L6	2	C9	4	C9	3	P6	4	P6	4	E12	8	AC6	9	A16	7	A16	7
vin1a_d5	L4	2	A9	4	A9	3	R9	4	R9	4	F13	8	AC7	9	C15	7	C15	7
vin1a_d6	L3	2	B9	4	B9	3	R5	4	R5	4	C12	8	AC4	9	A18	7	A18	7
vin1a_d7	L2	2	A10	4	A10	3	P5	4	P5	4	D12	8	AD4	9	A19	7	A19	7
vin1a_d8	L1	2	E8	4	E8	3	U2	4	U2	4	E15	8	AA4	9	F14	7	F14	7
vin1a_d9	K2	2	D9	4	D9	3	U1	4	U1	4	A20	8	AB3	9	G14	7	G14	7
vin1a_d10	J1	2	D7	4	D7	3	P3	4	P3	4	B15	8	AB9	9	A13	7	A13	7
vin1a_d11	J2	2	D8	4	D8	3	R2	4	R2	4	A15	8	AA3	9	E14	7	E14	7
vin1a_d12	H1	2	A5	4	A5	3	K7	4	K7	4	D15	8	D17	9	A12	7	A12	7
vin1a_d13	J3	2	C6	4	C6	3	M7	4	M7	4	B16	8	G16	9	B13	7	B13	7
vin1a_d14	H2	2	C8	4	C8	3	J5	4	J5	4	B17	8	A21	9	A11	7	A11	7
vin1a_d15	H3	2	C7	4	C7	3	K6	4	K6	4	A17	8	C18	9	B12	7	B12	7
vin1a_d16	R6	2	F11	4	F11	3					C18	8						
vin1a_d17	T9	2	G10	4	G10	3					A21	8						
vin1a_d18	T6	2	F10	4	F10	3					G16	8						
vin1a_d19	T7	2	G11	4	G11	3					D17	8						
vin1a_d20	P6	2	E9	4	E9	3					AA3	8						
vin1a_d21	R9	2	F9	4	F9	3					AB9	8						
vin1a_d22	R5	2	F8	4	F8	3					AB3	8						
vin1a_d23	P5	2	E7	4	E7	3					AA4	8						

Table 7-4. VIN1 IOSETs (continued)

SIGNALS	IOSET2		IOSET3		IOSET4 [(1)]		IOSET5 [(1)]		IOSET6 [(1)]		IOSET7 [(1)]		IOSET8		IOSET9		IOSET10	
	BALL	MUX	BALL	MUX	BALL	MUX	BALL	MUX	BALL	MUX	BALL	MUX	BALL	MUX	BALL	MUX	BALL	MUX
vin1b																		
vin1b_clk1					P7	6	M4	4	V1	5	N9	6						
vin1b_hsync1					H5	6	H5	6	U7	5	N7	6						
vin1b_vsync1					H6	6	H6	6	V6	5	R4	6						
vin1b_fld1					M4	6			W2	5	P4	6						
vin1b_de1					N6	6	N6	6	V7	5	P9	6						
vin1b_d0					K7	6	K7	6	U4	5	R6	6						
vin1b_d1					M7	6	M7	6	V2	5	T9	6						
vin1b_d2					J5	6	J5	6	Y1	5	T6	6						
vin1b_d3					K6	6	K6	6	W9	5	T7	6						
vin1b_d4					J7	6	J7	6	V9	5	P6	6						
vin1b_d5					J4	6	J4	6	U5	5	R9	6						
vin1b_d6					J6	6	J6	6	V5	5	R5	6						
vin1b_d7					H4	6	H4	6	V4	5	P5	6						

(1) The IOSET under this column is only applicable for pins with alternate functionality which allows either VIN1 or VIN2 signals to be mapped to the pins. These alternate functions are controlled via CTRL_CORE_VIP_MUX_SELECT register. For more information on how to use these options, see *Pad Configuration Registers* section, *Control Module* chapter in the device TRM.

Table 7-5. VIN2 IOSETs

SIGNALS	IOSET1		IOSET2		IOSET4		IOSET5		IOSET6		IOSET7 [(1)]		IOSET8 [(1)]		IOSET9 [(1)]		IOSET10 [(1)]	
	BALL	MUX	BALL	MUX	BALL	MUX	BALL	MUX	BALL	MUX	BALL	MUX	BALL	MUX	BALL	MUX	BALL	MUX
vin2a																		
vin2a_clk0					E1	0	E1	0	V1	4	B11	3	P4	4	P4	4	B26	8
vin2a_hsync0					G1	0	G1	0	U7	4	C11	3	R3	4	P7	4	E21	8
vin2a_vsync0					G6	0	G6	0	V6	4	E11	3	T2	4	N1	4	F20	8
vin2a_fld0					H7	0	G2	1	W2	4	D11	3	P9	4	J7	4	F21	8
vin2a_de0					G2	0			V7	4	B10	3	P7	5	H6	4	C23	8
vin2a_d0					F2	0	F2	0	U4	4	B7	3	R6	4	R6	4	B14	8
vin2a_d1					F3	0	F3	0	V2	4	B8	3	T9	4	T9	4	J14	8
vin2a_d2					D1	0	D1	0	Y1	4	A7	3	T6	4	T6	4	G13	8
vin2a_d3					E2	0	E2	0	W9	4	A8	3	T7	4	T7	4	J11	8
vin2a_d4					D2	0	D2	0	V9	4	C9	3	P6	4	P6	4	E12	8

Table 7-5. VIN2 IOSETs (continued)

SIGNALS	IOSET1		IOSET2		IOSET4		IOSET5		IOSET6		IOSET7 (1)		IOSET8 (1)		IOSET9 (1)		IOSET10 (1)	
	BALL	MUX	BALL	MUX	BALL	MUX	BALL	MUX	BALL	MUX	BALL	MUX	BALL	MUX	BALL	MUX	BALL	MUX
vin2a_d5					F4	0	F4	0	U5	4	A9	3	R9	4	R9	4	F13	8
vin2a_d6					C1	0	C1	0	V5	4	B9	3	R5	4	R5	4	C12	8
vin2a_d7					E4	0	E4	0	V4	4	A10	3	P5	4	P5	4	D12	8
vin2a_d8					F5	0	F5	0	V3	4	E8	3	U2	4	U2	4	E15	8
vin2a_d9					E6	0	E6	0	Y2	4	D9	3	U1	4	U1	4	A20	8
vin2a_d10					D3	0	D3	0	U6	4	D7	3	P3	4	P3	4	B15	8
vin2a_d11					F6	0	F6	0	U3	4	D8	3	R2	4	R2	4	A15	8
vin2a_d12					D5	0	D5	0			A5	3	K7	4	K7	4	D15	8
vin2a_d13					C2	0	C2	0			C6	3	M7	4	M7	4	B16	8
vin2a_d14					C3	0	C3	0			C8	3	J5	4	J5	4	B17	8
vin2a_d15					C4	0	C4	0			C7	3	K6	4	K6	4	A17	8
vin2a_d16					B2	0	B2	0			F11	3					C18	8
vin2a_d17					D6	0	D6	0			G10	3					A21	8
vin2a_d18					C5	0	C5	0			F10	3					G16	8
vin2a_d19					A3	0	A3	0			G11	3					D17	8
vin2a_d20					B3	0	B3	0			E9	3					AA3	8
vin2a_d21					B4	0	B4	0			F9	3					AB9	8
vin2a_d22					B5	0	B5	0			F8	3					AB3	8
vin2a_d23					A4	0	A4	0			E7	3					AA4	8
vin2b																		
vin2b_clk1	P7	6	M4	4							H7	2	H7	2	AB5	4		
vin2b_hsync1	H5	6	H5	6							G1	3	G1	3	AC5	4		
vin2b_vsync1	H6	6	H6	6							G6	3	G6	3	AB4	4		
vin2b_fld1	M4	6											G2	2				
vin2b_de1	N6	6	N6	6							G2	3			AB8	4		
vin2b_d0	K7	6	K7	6							A4	2	A4	2	AD6	4		
vin2b_d1	M7	6	M7	6							B5	2	B5	2	AC8	4		
vin2b_d2	J5	6	J5	6							B4	2	B4	2	AC3	4		
vin2b_d3	K6	6	K6	6							B3	2	B3	2	AC9	4		
vin2b_d4	J7	6	J7	6							A3	2	A3	2	AC6	4		
vin2b_d5	J4	6	J4	6							C5	2	C5	2	AC7	4		
vin2b_d6	J6	6	J6	6							D6	2	D6	2	AC4	4		

Table 7-5. VIN2 IOSETs (continued)

SIGNALS	IOSET1		IOSET2		IOSET4		IOSET5		IOSET6		IOSET7 (1)		IOSET8 (1)		IOSET9 (1)		IOSET10 (1)	
	BALL	MUX	BALL	MUX	BALL	MUX	BALL	MUX	BALL	MUX	BALL	MUX	BALL	MUX	BALL	MUX	BALL	MUX
vin2b_d7	H4	6	H4	6							B2	2	B2	2	AD4	4		

(1) The IOSET under this column is only applicable for pins with alternate functionality which allows either VIN1 or VIN2 signals to be mapped to the pins. These alternate functions are controlled via CTRL_CORE_VIP_MUX_SELECT register. For more information on how to use these options, see *Pad Configuration Registers* section, *Control Module* chapter in the device TRM.

NOTE

To configure the desired Manual IO Timing Mode the user must follow the steps described in section "*Manual IO Timing Modes*" in the device TRM.

The associated registers to configure are listed in the **CFG REGISTER** column. For more information, see *Control Module* chapter in the device TRM.

Manual IO Timings Modes must be used to ensure some IO timings for VIP1. See Table 7-2 *Modes Summary* for a list of IO timings requiring the use of Manual IO Timings Modes. See *Manual Functions Mapping for VIP1 1A IOSET7 and 2A IOSET10* for a definition of the Manual modes.

Table 7-6 lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.

Table 7-6. Manual Functions Mapping for VIP1 1A IOSET7 and 2A IOSET10

BALL	BALL NAME	VIP_MANUAL1		VIP_MANUAL2		CFG REGISTER	MUXMODE	
		A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)		8	8(1)
E21	gpio6_14	1400	240	1767	0	CFG_GPIO6_14_IN	vin2a_hsync0	vin1a_hsync0
F20	gpio6_15	1170	240	1522	0	CFG_GPIO6_15_IN	vin2a_vsync0	vin1a_vsync0
F21	gpio6_16	1470	0	1600	0	CFG_GPIO6_16_IN	vin2a_fld0	vin1a_fld0
B14	mcasp1_aclkr	2145	200	2509	0	CFG_MCASP1_ACLKR_IN	vin2a_d0	vin1a_d0
G13	mcasp1_axr2	2740	900	2680	1180	CFG_MCASP1_AXR2_IN	vin2a_d2	vin1a_d2
J11	mcasp1_axr3	2933	200	2700	600	CFG_MCASP1_AXR3_IN	vin2a_d3	vin1a_d3
E12	mcasp1_axr4	2901	240	2660	700	CFG_MCASP1_AXR4_IN	vin2a_d4	vin1a_d4
F13	mcasp1_axr5	2600	840	2640	920	CFG_MCASP1_AXR5_IN	vin2a_d5	vin1a_d5
C12	mcasp1_axr6	2718	240	3081	0	CFG_MCASP1_AXR6_IN	vin2a_d6	vin1a_d6
D12	mcasp1_axr7	2983	240	2540	800	CFG_MCASP1_AXR7_IN	vin2a_d7	vin1a_d7
J14	mcasp1_fsr	2203	240	2566	0	CFG_MCASP1_FSR_IN	vin2a_d1	vin1a_d1
E15	mcasp2_aclkr	2143	240	2492	0	CFG_MCASP2_ACLKR_IN	vin2a_d8	vin1a_d8
B15	mcasp2_axr0	2543	240	2905	0	CFG_MCASP2_AXR0_IN	vin2a_d10	vin1a_d10
A15	mcasp2_axr1	2664	240	2730	400	CFG_MCASP2_AXR1_IN	vin2a_d11	vin1a_d11

Table 7-6. Manual Functions Mapping for VIP1 1A IOSET7 and 2A IOSET10 (continued)

BALL	BALL NAME	VIP_MANUAL1		VIP_MANUAL2		CFG REGISTER	MUXMODE	
		A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)		8	8(1)
D15	mcasp2_axr4	2792	240	2750	400	CFG_MCASP2_AXR4_IN	vin2a_d12	vin1a_d12
B16	mcasp2_axr5	2621	300	2983	0	CFG_MCASP2_AXR5_IN	vin2a_d13	vin1a_d13
B17	mcasp2_axr6	1903	100	2086	0	CFG_MCASP2_AXR6_IN	vin2a_d14	vin1a_d14
A17	mcasp2_axr7	2928	200	2670	700	CFG_MCASP2_AXR7_IN	vin2a_d15	vin1a_d15
A20	mcasp2_fsr	2291	200	2654	0	CFG_MCASP2_FSR_IN	vin2a_d9	vin1a_d9
C18	mcasp4_aclkx	1433	0	1540	0	CFG_MCASP4_ACLKX_IN	vin2a_d16	vin1a_d16
G16	mcasp4_axr0	2500	0	2560	0	CFG_MCASP4_AXR0_IN	vin2a_d18	vin1a_d18
D17	mcasp4_axr1	2379	100	2599	0	CFG_MCASP4_AXR1_IN	vin2a_d19	vin1a_d19
A21	mcasp4_fsx	1500	1400	1900	1040	CFG_MCASP4_FSX_IN	vin2a_d17	vin1a_d17
AA3	mcasp5_aclkx	3740	1850	3900	1700	CFG_MCASP5_ACLKX_IN	vin2a_d20	vin1a_d20
AB3	mcasp5_axr0	3800	2760	3800	2800	CFG_MCASP5_AXR0_IN	vin2a_d22	vin1a_d22
AA4	mcasp5_axr1	4099	2500	3900	2870	CFG_MCASP5_AXR1_IN	vin2a_d23	vin1a_d23
AB9	mcasp5_fsx	3740	2100	3860	2060	CFG_MCASP5_FSX_IN	vin2a_d21	vin1a_d21
B26	xref_clk2	0	0	0	0	CFG_XREF_CLK2_IN	vin2a_clk0	vin1a_clk0
C23	xref_clk3	1440	0	1623	0	CFG_XREF_CLK3_IN	vin2a_de0	vin1a_de0

(1) Some signals listed are manual functions that present alternate multiplexing options. These manual functions are controlled via CTRL_CORE_ALT_SELECT_MUX or CTRL_CORE_VIP_MUX_SELECT registers. For more information on how to use these options, see *Pad Configuration Registers* section, *Control Module* chapter in the device TRM.

Manual IO Timings Modes must be used to ensure some IO timings for VIP1. See Table 7-2 *Modes Summary* for a list of IO timings requiring the use of Manual IO Timings Modes. See Table 7-7 *Manual Functions Mapping for VIN2A (IOSET4/5/6)* for a definition of the Manual modes.

Table 7-7 lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.

Table 7-7. Manual Functions Mapping for VIN2A (IOSET4/5/6)

BALL	BALL NAME	VIP_MANUAL3		VIP_MANUAL5		CFG REGISTER	MUXMODE				
		A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)		0	1	2	3	4
U3	RMII_MHZ_50_CLK	2616	1379	2798	1294	CFG_RMII_MHZ_50_CLK_IN	-	-	-	-	vin2a_d11
U4	mdio_d	2558	1105	2790	954	CFG_MDIO_D_IN	-	-	-	-	vin2a_d0
V1	mdio_mclk	998	463	1029	431	CFG_MDIO_MCLK_IN	-	-	-	-	vin2a_clk0
U5	rgmii0_rxc	2658	862	2896	651	CFG_RGMII0_RXC_IN	-	-	-	-	vin2a_d5
V5	rgmii0_rxctl	2658	1628	2844	1518	CFG_RGMII0_RXCTL_IN	-	-	-	-	vin2a_d6
W2	rgmii0_rxd0	2638	1123	2856	888	CFG_RGMII0_RXD0_IN	-	-	-	-	vin2a_fld0
Y2	rgmii0_rxd1	2641	1737	2804	1702	CFG_RGMII0_RXD1_IN	-	-	-	-	vin2a_d9

Table 7-7. Manual Functions Mapping for VIN2A (IOSET4/5/6) (continued)

BALL	BALL NAME	VIP_MANUAL3		VIP_MANUAL5		CFG REGISTER	MUXMODE				
		A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)		0	1	2	3	4
V3	rgmii0_rxd2	2641	1676	2801	1652	CFG_RGMII0_RXD2_IN	-	-	-	-	vin2a_d8
V4	rgmii0_rxd3	2644	1828	2807	1790	CFG_RGMII0_RXD3_IN	-	-	-	-	vin2a_d7
W9	rgmii0_txc	2638	1454	2835	1396	CFG_RGMII0_TXC_IN	-	-	-	-	vin2a_d3
V9	rgmii0_txctl	2672	1663	2831	1640	CFG_RGMII0_TXCTL_IN	-	-	-	-	vin2a_d4
U6	rgmii0_txd0	2604	1442	2764	1417	CFG_RGMII0_TXD0_IN	-	-	-	-	vin2a_d10
V6	rgmii0_txd1	2683	1598	2843	1600	CFG_RGMII0_TXD1_IN	-	-	-	-	vin2a_vsync0
U7	rgmii0_txd2	2563	1483	2816	1344	CFG_RGMII0_TXD2_IN	-	-	-	-	vin2a_hsync0
V7	rgmii0_txd3	2717	1461	2913	1310	CFG_RGMII0_TXD3_IN	-	-	-	-	vin2a_de0
V2	uart3_rxd	2445	1145	2743	923	CFG_UART3_RXD_IN	-	-	-	-	vin2a_d1
Y1	uart3_txd	2650	1197	2842	1080	CFG_UART3_TXD_IN	-	-	-	-	vin2a_d2
E1	vin2a_clk0	0	0	0	0	CFG_VIN2A_CLK0_IN	vin2a_clk0	-	-	-	-
F2	vin2a_d0	1812	102	1936	0	CFG_VIN2A_D0_IN	vin2a_d0	-	-	-	-
F3	vin2a_d1	1701	439	2229	10	CFG_VIN2A_D1_IN	vin2a_d1	-	-	-	-
D3	vin2a_d10	1720	215	2031	0	CFG_VIN2A_D10_IN	vin2a_d10	-	-	-	-
F6	vin2a_d11	1622	0	1702	0	CFG_VIN2A_D11_IN	vin2a_d11	-	-	-	-
D5	vin2a_d12	1350	412	1819	0	CFG_VIN2A_D12_IN	vin2a_d12	-	-	-	-
C2	vin2a_d13	1613	147	1476	260	CFG_VIN2A_D13_IN	vin2a_d13	-	-	-	-
C3	vin2a_d14	1149	516	1701	0	CFG_VIN2A_D14_IN	vin2a_d14	-	-	-	-
C4	vin2a_d15	1530	450	2021	0	CFG_VIN2A_D15_IN	vin2a_d15	-	-	-	-
B2	vin2a_d16	1512	449	2044	11	CFG_VIN2A_D16_IN	vin2a_d16	-	vin2b_d7	-	-
D6	vin2a_d17	1293	488	1839	5	CFG_VIN2A_D17_IN	vin2a_d17	-	vin2b_d6	-	-
C5	vin2a_d18	2140	371	2494	0	CFG_VIN2A_D18_IN	vin2a_d18	-	vin2b_d5	-	-
A3	vin2a_d19	2041	275	1699	611	CFG_VIN2A_D19_IN	vin2a_d19	-	vin2b_d4	-	-
D1	vin2a_d2	1675	35	1736	0	CFG_VIN2A_D2_IN	vin2a_d2	-	-	-	-
B3	vin2a_d20	1972	441	2412	88	CFG_VIN2A_D20_IN	vin2a_d20	-	vin2b_d3	-	-
B4	vin2a_d21	1957	556	2391	161	CFG_VIN2A_D21_IN	vin2a_d21	-	vin2b_d2	-	-
B5	vin2a_d22	2011	433	2446	102	CFG_VIN2A_D22_IN	vin2a_d22	-	vin2b_d1	-	-
A4	vin2a_d23	1962	523	2395	145	CFG_VIN2A_D23_IN	vin2a_d23	-	vin2b_d0	-	-
E2	vin2a_d3	1457	361	1943	0	CFG_VIN2A_D3_IN	vin2a_d3	-	-	-	-
D2	vin2a_d4	1535	0	1601	0	CFG_VIN2A_D4_IN	vin2a_d4	-	-	-	-

Table 7-7. Manual Functions Mapping for VIN2A (IOSET4/5/6) (continued)

BALL	BALL NAME	VIP_MANUAL3		VIP_MANUAL5		CFG REGISTER	MUXMODE				
		A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)		0	1	2	3	4
F4	vin2a_d5	1676	271	2052	0	CFG_VIN2A_D5_IN	vin2a_d5	-	-	-	-
C1	vin2a_d6	1513	0	1571	0	CFG_VIN2A_D6_IN	vin2a_d6	-	-	-	-
E4	vin2a_d7	1616	141	1855	0	CFG_VIN2A_D7_IN	vin2a_d7	-	-	-	-
F5	vin2a_d8	1286	437	1224	618	CFG_VIN2A_D8_IN	vin2a_d8	-	-	-	-
E6	vin2a_d9	1544	265	1373	509	CFG_VIN2A_D9_IN	vin2a_d9	-	-	-	-
G2	vin2a_de0	1732	208	1949	0	CFG_VIN2A_DE0_IN	vin2a_de0	vin2a_fld0	vin2b_fld1	vin2b_de1	-
H7	vin2a_fld0	1461	562	1983	151	CFG_VIN2A_FLD0_IN	vin2a_fld0	-	vin2b_clk1	-	-
G1	vin2a_hsync0	1877	0	1943	0	CFG_VIN2A_HSYNC0_IN	vin2a_hsync0	-	-	vin2b_hsync1	-
G6	vin2a_vsync0	1566	0	1612	0	CFG_VIN2A_VSYNC0_IN	vin2a_vsync0	-	-	vin2b_vsync1	-

Manual IO Timings Modes must be used to ensure some IO timings for VIP1. See Table 7-2 *Modes Summary* for a list of IO timings requiring the use of Manual IO Timings Modes. See Table 7-8 *Manual Functions Mapping for VIN2B (IOSET7/8/9)* for a definition of the Manual modes.

Table 7-8 lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.

Table 7-8. Manual Functions Mapping for VIN2B (IOSET7/8/9)

BALL	BALL NAME	VIP_MANUAL4		VIP_MANUAL6		CFG REGISTER	MUXMODE		
		A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)		2	3	4
AC5	gpio6_10	2829	884	3009	892	CFG_GPIO6_10_IN	-	-	vin2b_hsync1
AB4	gpio6_11	2648	1033	2890	1096	CFG_GPIO6_11_IN	-	-	vin2b_vsync1
AD4	mmc3_clk	2794	1074	2997	1089	CFG_MMC3_CLK_IN	-	-	vin2b_d7
AC4	mmc3_cmd	2789	1162	2959	1210	CFG_MMC3_CMD_IN	-	-	vin2b_d6
AC7	mmc3_dat0	2689	1180	2897	1269	CFG_MMC3_DAT0_IN	-	-	vin2b_d5
AC6	mmc3_dat1	2605	1219	2891	1219	CFG_MMC3_DAT1_IN	-	-	vin2b_d4
AC9	mmc3_dat2	2616	703	2947	590	CFG_MMC3_DAT2_IN	-	-	vin2b_d3
AC3	mmc3_dat3	2760	1235	2931	1342	CFG_MMC3_DAT3_IN	-	-	vin2b_d2
AC8	mmc3_dat4	2757	880	2979	891	CFG_MMC3_DAT4_IN	-	-	vin2b_d1
AD6	mmc3_dat5	2688	1177	2894	1262	CFG_MMC3_DAT5_IN	-	-	vin2b_d0
AB8	mmc3_dat6	2638	1165	2894	1187	CFG_MMC3_DAT6_IN	-	-	vin2b_de1
AB5	mmc3_dat7	995	182	1202	107	CFG_MMC3_DAT7_IN	-	-	vin2b_clk1
B2	vin2a_d16	1423	0	1739	0	CFG_VIN2A_D16_IN	vin2b_d7	-	-

Table 7-8. Manual Functions Mapping for VIN2B (IOSET7/8/9) (continued)

BALL	BALL NAME	VIP_MANUAL4		VIP_MANUAL6		CFG REGISTER	MUXMODE		
		A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)		2	3	4
D6	vin2a_d17	1253	0	1568	0	CFG_VIN2A_D17_IN	vin2b_d6	-	-
C5	vin2a_d18	2080	0	2217	0	CFG_VIN2A_D18_IN	vin2b_d5	-	-
A3	vin2a_d19	1849	0	2029	0	CFG_VIN2A_D19_IN	vin2b_d4	-	-
B3	vin2a_d20	1881	50	2202	0	CFG_VIN2A_D20_IN	vin2b_d3	-	-
B4	vin2a_d21	1917	167	2313	0	CFG_VIN2A_D21_IN	vin2b_d2	-	-
B5	vin2a_d22	1955	79	2334	0	CFG_VIN2A_D22_IN	vin2b_d1	-	-
A4	vin2a_d23	1899	145	2288	0	CFG_VIN2A_D23_IN	vin2b_d0	-	-
G2	vin2a_de0	1568	261	2048	0	CFG_VIN2A_DE0_IN	vin2b_fld1	vin2b_de1	-
H7	vin2a_fld0	0	0	0	0	CFG_VIN2A_FLD0_IN	vin2b_clk1	-	-
G1	vin2a_hsync0	1793	0	2011	0	CFG_VIN2A_HSYNC0_IN	-	vin2b_hsync1	-
G6	vin2a_vsync0	1382	0	1632	0	CFG_VIN2A_VSYNC0_IN	-	vin2b_vsync1	-

Manual IO Timings Modes must be used to ensure some IO timings for VIP1. See Table 7-2 *Modes Summary* for a list of IO timings requiring the use of Manual IO Timings Modes. See Table 7-9 *Manual Functions Mapping for VIN1A (IOSET2/3/4) and VIN1B (IOSET4/7) and VIN2B (IOSET1/10)* for a definition of the Manual modes.

Table 7-9 lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.

Table 7-9. Manual Functions Mapping for VIN1A (IOSET2/3/4) and VIN1B (IOSET4/7) and VIN2B (IOSET1/10)

BALL	BALL NAME	VIP_MANUAL7		VIP_MANUAL12		CFG REGISTER	MUXMODE							
		A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)		2	3(1)	3(1)	4(1)	4(1)	5	6(1)	6(1)
R6	gpmc_a0	3080	1792	3376	1632	CFG_GPMC_A0_IN	vin1a_d16	-	-	vin2a_d0	-	-	vin1b_d0	-
T9	gpmc_a1	2958	1890	3249	1749	CFG_GPMC_A1_IN	vin1a_d17	-	-	vin2a_d1	-	-	vin1b_d1	-
N9	gpmc_a10	3073	1653	3388	1433	CFG_GPMC_A10_IN	vin1a_de0	-	-	-	-	-	vin1b_clk1	-
P9	gpmc_a11	3014	1784	3290	1693	CFG_GPMC_A11_IN	vin1a_fld0	-	-	vin2a_fld0	vin1a_fld0	-	vin1b_de1	-
K7	gpmc_a19	1385	0	1246	0	CFG_GPMC_A19_IN	-	-	-	vin2a_d12	-	-	vin2b_d0	vin1b_d0
T6	gpmc_a2	3041	1960	3322	1850	CFG_GPMC_A2_IN	vin1a_d18	-	-	vin2a_d2	-	-	vin1b_d2	-
M7	gpmc_a20	859	0	720	0	CFG_GPMC_A20_IN	-	-	-	vin2a_d13	-	-	vin2b_d1	vin1b_d1

Table 7-9. Manual Functions Mapping for VIN1A (IOSET2/3/4) and VIN1B (IOSET4/7) and VIN2B (IOSET1/10) (continued)

BALL	BALL NAME	VIP_MANUAL7		VIP_MANUAL12		CFG REGISTER	MUXMODE							
		A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)		2	3(1)	3(1)	4(1)	4(1)	5	6(1)	6(1)
J5	gpmc_a21	1465	0	1334	0	CFG_GPMC_A21_IN	-	-	-	vin2a_d14	-	-	vin2b_d2	vin1b_d2
K6	gpmc_a22	1210	0	1064	0	CFG_GPMC_A22_IN	-	-	-	vin2a_d15	-	-	vin2b_d3	vin1b_d3
J7	gpmc_a23	1111	0	954	0	CFG_GPMC_A23_IN	-	-	-	vin2a_fld0	-	-	vin2b_d4	vin1b_d4
J4	gpmc_a24	1137	0	1051	0	CFG_GPMC_A24_IN	-	-	-	-	-	-	vin2b_d5	vin1b_d5
J6	gpmc_a25	1402	0	1283	0	CFG_GPMC_A25_IN	-	-	-	-	-	-	vin2b_d6	vin1b_d6
H4	gpmc_a26	1298	0	1153	0	CFG_GPMC_A26_IN	-	-	-	-	-	-	vin2b_d7	vin1b_d7
H5	gpmc_a27	934	0	870	0	CFG_GPMC_A27_IN	-	-	-	-	-	-	vin2b_hsync1	vin1b_hsync1
T7	gpmc_a3	3019	2145	3296	2050	CFG_GPMC_A3_IN	vin1a_d19	-	-	vin2a_d3	-	-	vin1b_d3	-
P6	gpmc_a4	3063	1981	3357	1829	CFG_GPMC_A4_IN	vin1a_d20	-	-	vin2a_d4	-	-	vin1b_d4	-
R9	gpmc_a5	3021	1954	3304	1840	CFG_GPMC_A5_IN	vin1a_d21	-	-	vin2a_d5	-	-	vin1b_d5	-
R5	gpmc_a6	3062	1716	3348	1592	CFG_GPMC_A6_IN	vin1a_d22	-	-	vin2a_d6	-	-	vin1b_d6	-
P5	gpmc_a7	3260	1889	3583	1631	CFG_GPMC_A7_IN	vin1a_d23	-	-	vin2a_d7	-	-	vin1b_d7	-
N7	gpmc_a8	3033	1702	3328	1547	CFG_GPMC_A8_IN	vin1a_hsync0	-	-	-	-	-	vin1b_hsync1	-
R4	gpmc_a9	2991	1905	3281	1766	CFG_GPMC_A9_IN	vin1a_vsync0	-	-	-	-	-	vin1b_vsync1	-
M6	gpmc_ad0	2907	1342	3181	1255	CFG_GPMC_AD0_IN	vin1a_d0	-	-	-	-	-	-	-
M2	gpmc_ad1	2858	1321	3132	1234	CFG_GPMC_AD1_IN	vin1a_d1	-	-	-	-	-	-	-
J1	gpmc_ad10	2920	1384	3223	1204	CFG_GPMC_AD10_IN	vin1a_d10	-	-	-	-	-	-	-
J2	gpmc_ad11	2719	1310	3019	1198	CFG_GPMC_AD11_IN	vin1a_d11	-	-	-	-	-	-	-
H1	gpmc_ad12	2845	1135	3160	917	CFG_GPMC_AD12_IN	vin1a_d12	-	-	-	-	-	-	-
J3	gpmc_ad13	2765	1225	3045	1119	CFG_GPMC_AD13_IN	vin1a_d13	-	-	-	-	-	-	-
H2	gpmc_ad14	2845	1150	3153	952	CFG_GPMC_AD14_IN	vin1a_d14	-	-	-	-	-	-	-

Table 7-9. Manual Functions Mapping for VIN1A (IOSET2/3/4) and VIN1B (IOSET4/7) and VIN2B (IOSET1/10) (continued)

BALL	BALL NAME	VIP_MANUAL7		VIP_MANUAL12		CFG REGISTER	MUXMODE							
		A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)		2	3(1)	3(1)	4(1)	4(1)	5	6(1)	6(1)
H3	gpmc_ad15	2766	1453	3044	1355	CFG_GPMC_AD15_IN	vin1a_d15	-	-	-	-	-	-	-
L5	gpmc_ad2	2951	1296	3226	1209	CFG_GPMC_AD2_IN	vin1a_d2	-	-	-	-	-	-	-
M1	gpmc_ad3	2825	1154	3121	997	CFG_GPMC_AD3_IN	vin1a_d3	-	-	-	-	-	-	-
L6	gpmc_ad4	2927	1245	3246	1014	CFG_GPMC_AD4_IN	vin1a_d4	-	-	-	-	-	-	-
L4	gpmc_ad5	2923	1251	3217	1098	CFG_GPMC_AD5_IN	vin1a_d5	-	-	-	-	-	-	-
L3	gpmc_ad6	2958	1342	3238	1239	CFG_GPMC_AD6_IN	vin1a_d6	-	-	-	-	-	-	-
L2	gpmc_ad7	2900	1244	3174	1157	CFG_GPMC_AD7_IN	vin1a_d7	-	-	-	-	-	-	-
L1	gpmc_ad8	2845	1585	3125	1482	CFG_GPMC_AD8_IN	vin1a_d8	-	-	-	-	-	-	-
K2	gpmc_ad9	2779	1343	3086	1223	CFG_GPMC_AD9_IN	vin1a_d9	-	-	-	-	-	-	-
N6	gpmc_ben0	1555	0	1425	0	CFG_GPMC_BEN0_IN	-	-	-	-	-	-	vin2b_de1	vin1b_de1
M4	gpmc_ben1	1501	0	1397	0	CFG_GPMC_BEN1_IN	-	-	-	vin2b_clk1	-	-	vin2b_fld1	vin1b_fld1
P7	gpmc_clk	0	0	0	0	CFG_GPMC_CLK_IN	-	-	-	vin2a_hsync0	-	vin2a_de0	vin2b_clk1	vin1b_clk1
H6	gpmc_cs1	1192	0	1102	0	CFG_GPMC_CS1_IN	-	-	-	vin2a_de0	-	-	vin2b_vsync1	vin1b_vsync1
P1	gpmc_cs3	1324	374	1466	353	CFG_GPMC_CS3_IN	vin1a_clk0	-	-	-	-	-	-	-
D11	vout1_clk	1648	885	1762	928	CFG_VOUT1_CLK_IN	-	vin2a_fld0	vin1a_fld0	vin1a_fld0	-	-	-	-
F11	vout1_d0	2197	565	2734	215	CFG_VOUT1_D0_IN	-	vin2a_d16	vin1a_d16	vin1a_d16	-	-	-	-
G10	vout1_d1	2221	576	2750	230	CFG_VOUT1_D1_IN	-	vin2a_d17	vin1a_d17	vin1a_d17	-	-	-	-
D7	vout1_d10	1800	863	1910	916	CFG_VOUT1_D10_IN	-	vin2a_d10	vin1a_d10	vin1a_d10	-	-	-	-
D8	vout1_d11	1656	931	1780	945	CFG_VOUT1_D11_IN	-	vin2a_d11	vin1a_d11	vin1a_d11	-	-	-	-
A5	vout1_d12	1719	1086	1866	1041	CFG_VOUT1_D12_IN	-	vin2a_d12	vin1a_d12	vin1a_d12	-	-	-	-
C6	vout1_d13	1757	928	1851	1022	CFG_VOUT1_D13_IN	-	vin2a_d13	vin1a_d13	vin1a_d13	-	-	-	-
C8	vout1_d14	2279	345	2788	0	CFG_VOUT1_D14_IN	-	vin2a_d14	vin1a_d14	vin1a_d14	-	-	-	-

Table 7-9. Manual Functions Mapping for VIN1A (IOSET2/3/4) and VIN1B (IOSET4/7) and VIN2B (IOSET1/10) (continued)

BALL	BALL NAME	VIP_MANUAL7		VIP_MANUAL12		CFG REGISTER	MUXMODE							
		A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)		2	3(1)	3(1)	4(1)	4(1)	5	6(1)	6(1)
C7	vout1_d15	1810	874	2786	69	CFG_VOUT1_D15_IN	-	vin2a_d15	vin1a_d15	vin1a_d15	-	-	-	-
B7	vout1_d16	1763	774	1880	807	CFG_VOUT1_D16_IN	-	vin2a_d0	vin1a_d0	vin1a_d0	-	-	-	-
B8	vout1_d17	1695	788	1805	838	CFG_VOUT1_D17_IN	-	vin2a_d1	vin1a_d1	vin1a_d1	-	-	-	-
A7	vout1_d18	1777	590	1871	684	CFG_VOUT1_D18_IN	-	vin2a_d2	vin1a_d2	vin1a_d2	-	-	-	-
A8	vout1_d19	2047	22	2196	0	CFG_VOUT1_D19_IN	-	vin2a_d3	vin1a_d3	vin1a_d3	-	-	-	-
F10	vout1_d2	1809	941	2759	178	CFG_VOUT1_D2_IN	-	vin2a_d18	vin1a_d18	vin1a_d18	-	-	-	-
C9	vout1_d20	1676	944	1795	973	CFG_VOUT1_D20_IN	-	vin2a_d4	vin1a_d4	vin1a_d4	-	-	-	-
A9	vout1_d21	1712	688	1848	670	CFG_VOUT1_D21_IN	-	vin2a_d5	vin1a_d5	vin1a_d5	-	-	-	-
B9	vout1_d22	1698	557	2443	0	CFG_VOUT1_D22_IN	-	vin2a_d6	vin1a_d6	vin1a_d6	-	-	-	-
A10	vout1_d23	1627	1035	1726	1116	CFG_VOUT1_D23_IN	-	vin2a_d7	vin1a_d7	vin1a_d7	-	-	-	-
G11	vout1_d3	2427	429	2853	167	CFG_VOUT1_D3_IN	-	vin2a_d19	vin1a_d19	vin1a_d19	-	-	-	-
E9	vout1_d4	2351	412	2845	85	CFG_VOUT1_D4_IN	-	vin2a_d20	vin1a_d20	vin1a_d20	-	-	-	-
F9	vout1_d5	1634	983	1729	1076	CFG_VOUT1_D5_IN	-	vin2a_d21	vin1a_d21	vin1a_d21	-	-	-	-
F8	vout1_d6	1776	880	2736	107	CFG_VOUT1_D6_IN	-	vin2a_d22	vin1a_d22	vin1a_d22	-	-	-	-
E7	vout1_d7	2272	351	2757	53	CFG_VOUT1_D7_IN	-	vin2a_d23	vin1a_d23	vin1a_d23	-	-	-	-
E8	vout1_d8	1724	898	1819	990	CFG_VOUT1_D8_IN	-	vin2a_d8	vin1a_d8	vin1a_d8	-	-	-	-
D9	vout1_d9	2281	566	2804	195	CFG_VOUT1_D9_IN	-	vin2a_d9	vin1a_d9	vin1a_d9	-	-	-	-
B10	vout1_de	1734	749	1828	842	CFG_VOUT1_DE_IN	-	vin2a_de0	vin1a_de0	vin1a_de0	-	-	-	-
B11	vout1_fld	0	0	0	0	CFG_VOUT1_FLD_IN	-	vin2a_clk0	vin1a_clk0	vin1a_clk0	-	-	-	-
C11	vout1_hsync	1634	606	2399	0	CFG_VOUT1_HSYNC_IN	-	vin2a_hsync0	vin1a_hsync0	vin1a_hsync0	-	-	-	-
E11	vout1_vsync	1887	0	2068	0	CFG_VOUT1_VSYNC_IN	-	vin2a_vsync0	vin1a_vsync0	vin1a_vsync0	-	-	-	-

(1) Some signals listed are manual functions that present alternate multiplexing options. These manual functions are controlled via CTRL_CORE_ALT_SELECT_MUX or CTRL_CORE_VIP_MUX_SELECT registers. For more information on how to use these options, see *Pad Configuration Registers* section, *Control Module* chapter in the device TRM.

Manual IO Timings Modes must be used to ensure some IO timings for VIP1. See Table 7-2 *Modes Summary* for a list of IO timings requiring the use of Manual IO Timings Modes. See Table 7-10 *Manual Functions Mapping for VIN1A (IOSET5/6) and VIN2A (IOSET7/8/9)* for a definition of the Manual modes.

Table 7-10 lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.

Table 7-10. Manual Functions Mapping for VIN1A (IOSET5/6) and VIN2A (IOSET7/8/9)

BALL	BALL NAME	VIP_MANUAL8		VIP_MANUAL13		CFG REGISTER	MUXMODE				
		A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)		3	4[(1)]	4[(1)]	5[(1)]	5[(1)]
R6	gpmc_a0	1891	427	2176	0	CFG_GPMC_A0_IN	-	vin2a_d0	vin1a_d0	-	-
T9	gpmc_a1	1713	513	2109	0	CFG_GPMC_A1_IN	-	vin2a_d1	vin1a_d1	-	-
P9	gpmc_a11	1797	317	2036	0	CFG_GPMC_A11_IN	-	vin2a_fld0	vin1a_fld0	-	-
P4	gpmc_a12	0	0	0	0	CFG_GPMC_A12_IN	-	vin2a_clk0	vin1a_clk0	-	-
R3	gpmc_a13	1876	391	2144	0	CFG_GPMC_A13_IN	-	vin2a_hsync0	vin1a_hsync0	-	-
T2	gpmc_a14	1720	756	2384	38	CFG_GPMC_A14_IN	-	vin2a_vsync0	vin1a_vsync0	-	-
U2	gpmc_a15	1502	368	1804	0	CFG_GPMC_A15_IN	-	vin2a_d8	vin1a_d8	-	-
U1	gpmc_a16	1651	355	1902	0	CFG_GPMC_A16_IN	-	vin2a_d9	vin1a_d9	-	-
P3	gpmc_a17	1642	338	1862	0	CFG_GPMC_A17_IN	-	vin2a_d10	vin1a_d10	-	-
R2	gpmc_a18	1612	0	1406	0	CFG_GPMC_A18_IN	-	vin2a_d11	vin1a_d11	-	-
K7	gpmc_a19	1463	152	1418	0	CFG_GPMC_A19_IN	-	vin2a_d12	vin1a_d12	-	-
T6	gpmc_a2	1789	646	2310	0	CFG_GPMC_A2_IN	-	vin2a_d2	vin1a_d2	-	-
M7	gpmc_a20	1124	0	933	0	CFG_GPMC_A20_IN	-	vin2a_d13	vin1a_d13	-	-
J5	gpmc_a21	1491	206	1483	0	CFG_GPMC_A21_IN	-	vin2a_d14	vin1a_d14	-	-
K6	gpmc_a22	1218	245	1254	0	CFG_GPMC_A22_IN	-	vin2a_d15	vin1a_d15	-	-
J7	gpmc_a23	1216	0	1021	0	CFG_GPMC_A23_IN	-	vin2a_fld0	vin1a_fld0	-	-
T7	gpmc_a3	1789	766	2451	8	CFG_GPMC_A3_IN	-	vin2a_d3	vin1a_d3	-	-
P6	gpmc_a4	1842	646	2329	0	CFG_GPMC_A4_IN	-	vin2a_d4	vin1a_d4	-	-
R9	gpmc_a5	1778	556	2215	0	CFG_GPMC_A5_IN	-	vin2a_d5	vin1a_d5	-	-
R5	gpmc_a6	1783	443	2088	0	CFG_GPMC_A6_IN	-	vin2a_d6	vin1a_d6	-	-
P5	gpmc_a7	2207	370	2393	0	CFG_GPMC_A7_IN	-	vin2a_d7	vin1a_d7	-	-
N1	gpmc_advn_ale	1755	116	1745	0	CFG_GPMC_ADVN_ALE_IN	-	vin2a_vsync0	vin1a_vsync0	-	-

Table 7-10. Manual Functions Mapping for VIN1A (IOSET5/6) and VIN2A (IOSET7/8/9) (continued)

BALL	BALL NAME	VIP_MANUAL8		VIP_MANUAL13		CFG REGISTER	MUXMODE				
		A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)		3	4(1)	4(1)	5(1)	5(1)
P7	gpmc_clk	1896	351	2152	0	CFG_GPMC_CLK_IN	-	vin2a_hsync0	vin1a_hsync0	vin2a_de0	vin1a_de0
H6	gpmc_cs1	1337	74	1288	0	CFG_GPMC_CS1_IN	-	vin2a_de0	vin1a_de0	-	-
D11	vout1_clk	1939	332	2486	0	CFG_VOUT1_CLK_IN	vin2a_fld0	-	-	-	-
F11	vout1_d0	2140	647	2617	386	CFG_VOUT1_D0_IN	vin2a_d16	-	-	-	-
G10	vout1_d1	2104	615	2620	314	CFG_VOUT1_D1_IN	vin2a_d17	-	-	-	-
D7	vout1_d10	2139	406	2675	85	CFG_VOUT1_D10_IN	vin2a_d10	-	-	-	-
D8	vout1_d11	1944	534	2569	125	CFG_VOUT1_D11_IN	vin2a_d11	-	-	-	-
A5	vout1_d12	1966	659	2646	154	CFG_VOUT1_D12_IN	vin2a_d12	-	-	-	-
C6	vout1_d13	2048	447	2624	87	CFG_VOUT1_D13_IN	vin2a_d13	-	-	-	-
C8	vout1_d14	2222	548	2700	286	CFG_VOUT1_D14_IN	vin2a_d14	-	-	-	-
C7	vout1_d15	2072	443	2664	67	CFG_VOUT1_D15_IN	vin2a_d15	-	-	-	-
B7	vout1_d16	2044	455	2634	82	CFG_VOUT1_D16_IN	vin2a_d0	-	-	-	-
B8	vout1_d17	1971	246	2433	0	CFG_VOUT1_D17_IN	vin2a_d1	-	-	-	-
A7	vout1_d18	2104	120	2440	0	CFG_VOUT1_D18_IN	vin2a_d2	-	-	-	-
A8	vout1_d19	1888	0	2105	0	CFG_VOUT1_D19_IN	vin2a_d3	-	-	-	-
F10	vout1_d2	2170	237	2624	0	CFG_VOUT1_D2_IN	vin2a_d18	-	-	-	-
C9	vout1_d20	1942	512	2579	91	CFG_VOUT1_D20_IN	vin2a_d4	-	-	-	-
A9	vout1_d21	1997	141	2324	0	CFG_VOUT1_D21_IN	vin2a_d5	-	-	-	-
B9	vout1_d22	1949	0	2165	0	CFG_VOUT1_D22_IN	vin2a_d6	-	-	-	-
A10	vout1_d23	1871	704	2522	269	CFG_VOUT1_D23_IN	vin2a_d7	-	-	-	-
G11	vout1_d3	2319	417	2740	191	CFG_VOUT1_D3_IN	vin2a_d19	-	-	-	-
E9	vout1_d4	2300	369	2739	137	CFG_VOUT1_D4_IN	vin2a_d20	-	-	-	-
F9	vout1_d5	1923	579	2527	191	CFG_VOUT1_D5_IN	vin2a_d21	-	-	-	-
F8	vout1_d6	2148	396	2622	138	CFG_VOUT1_D6_IN	vin2a_d22	-	-	-	-
E7	vout1_d7	2212	335	2653	110	CFG_VOUT1_D7_IN	vin2a_d23	-	-	-	-
E8	vout1_d8	1962	573	2573	178	CFG_VOUT1_D8_IN	vin2a_d8	-	-	-	-
D9	vout1_d9	2312	335	2725	138	CFG_VOUT1_D9_IN	vin2a_d9	-	-	-	-
B10	vout1_de	1973	414	2551	52	CFG_VOUT1_DE_IN	vin2a_de0	-	-	-	-
B11	vout1_fld	0	0	0	0	CFG_VOUT1_FLD_IN	vin2a_clk0	-	-	-	-
C11	vout1_hsync	1813	261	2277	0	CFG_VOUT1_HSYNC_IN	vin2a_hsync0	-	-	-	-

Table 7-10. Manual Functions Mapping for VIN1A (IOSET5/6) and VIN2A (IOSET7/8/9) (continued)

BALL	BALL NAME	VIP_MANUAL8		VIP_MANUAL13		CFG REGISTER	MUXMODE				
		A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)		3	4(1)	4(1)	5(1)	5(1)
E11	vout1_vsync	1665	0	1881	0	CFG_VOUT1_VSYNC_IN	vin2a_vsync0	-	-	-	-

(1) Some signals listed are manual functions that present alternate multiplexing options. These manual functions are controlled via CTRL_CORE_ALT_SELECT_MUX or CTRL_CORE_VIP_MUX_SELECT registers. For more information on how to use these options, see *Pad Configuration Registers* section, *Control Module* chapter in the device TRM.

Manual IO Timings Modes must be used to ensure some IO timings for VIP1. See Table 7-2 *Modes Summary* for a list of IO timings requiring the use of Manual IO Timings Modes. See Table 7-11 *Manual Functions Mapping for VIN1B (IOSET6/7)* for a definition of the Manual modes.

Table 7-11 lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.

Table 7-11. Manual Functions Mapping for VIN1B (IOSET6/7)

BALL	BALL NAME	VIP_MANUAL9		VIP_MANUAL14		CFG REGISTER	MUXMODE	
		A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)		5	6
R6	gpmc_a0	1873	702	2202	441	CFG_GPMC_A0_IN	-	vin1b_d0
T9	gpmc_a1	1629	772	2057	413	CFG_GPMC_A1_IN	-	vin1b_d1
N9	gpmc_a10	0	0	0	0	CFG_GPMC_A10_IN	-	vin1b_clk1
P9	gpmc_a11	1851	1011	2126	856	CFG_GPMC_A11_IN	-	vin1b_de1
P4	gpmc_a12	2009	601	2289	327	CFG_GPMC_A12_IN	-	vin1b_fld1
T6	gpmc_a2	1734	898	2131	573	CFG_GPMC_A2_IN	-	vin1b_d2
T7	gpmc_a3	1757	1076	2106	812	CFG_GPMC_A3_IN	-	vin1b_d3
P6	gpmc_a4	1794	893	2164	559	CFG_GPMC_A4_IN	-	vin1b_d4
R9	gpmc_a5	1726	853	2120	523	CFG_GPMC_A5_IN	-	vin1b_d5
R5	gpmc_a6	1792	612	2153	338	CFG_GPMC_A6_IN	-	vin1b_d6
P5	gpmc_a7	2117	610	2389	304	CFG_GPMC_A7_IN	-	vin1b_d7
N7	gpmc_a8	1758	653	2140	308	CFG_GPMC_A8_IN	-	vin1b_hsync1
R4	gpmc_a9	1705	899	2067	646	CFG_GPMC_A9_IN	-	vin1b_vsync1
U4	mdio_d	1945	671	2265	414	CFG_MDIO_D_IN	vin1b_d0	-
V1	mdio_mclk	255	119	337	0	CFG_MDIO_MCLK_IN	vin1b_clk1	-
U5	rgmii0_rxc	2057	909	2341	646	CFG_RGMII0_RXC_IN	vin1b_d5	-
V5	rgmii0_rxctl	2121	1139	2323	988	CFG_RGMII0_RXCTL_IN	vin1b_d6	-
W2	rgmii0_rxd0	2070	655	2336	340	CFG_RGMII0_RXD0_IN	vin1b_fld1	-
V4	rgmii0_rxd3	2092	1357	2306	1216	CFG_RGMII0_RXD3_IN	vin1b_d7	-
W9	rgmii0_txc	2088	1205	2328	1079	CFG_RGMII0_TXC_IN	vin1b_d3	-
V9	rgmii0_txctl	2143	1383	2312	1311	CFG_RGMII0_TXCTL_IN	vin1b_d4	-

Table 7-11. Manual Functions Mapping for VIN1B (IOSET6/7) (continued)

BALL	BALL NAME	VIP_MANUAL9		VIP_MANUAL14		CFG REGISTER	MUXMODE	
		A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)		5	6
V6	rgmii0_txd1	2078	1189	2324	1065	CFG_RGMII0_TXD1_IN	vin1b_vsync1	-
U7	rgmii0_txd2	1928	1125	2306	763	CFG_RGMII0_TXD2_IN	vin1b_hsync1	-
V7	rgmii0_txd3	2255	971	2401	846	CFG_RGMII0_TXD3_IN	vin1b_de1	-
V2	uart3_rxd	1829	747	2220	400	CFG_UART3_RXD_IN	vin1b_d1	-
Y1	uart3_txd	2030	837	2324	568	CFG_UART3_TXD_IN	vin1b_d2	-

Manual IO Timings Modes must be used to ensure some IO timings for VIP1. See Table 7-2 *Modes Summary* for a list of IO timings requiring the use of Manual IO Timings Modes. See Table 7-12 *Manual Functions Mapping for VIN1B (IOSET5) and VIN2B (IOSET2/11)* for a definition of the Manual modes.

Table 7-12 lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.

Table 7-12. Manual Functions Mapping for VIN1B (IOSET5) and VIN2B (IOSET2/11)

BALL	BALL NAME	VIP_MANUAL10		VIP_MANUAL11		CFG REGISTER	MUXMODE			
		A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)		4(1)	4(1)	6(1)	6(1)
K7	gpmc_a19	1600	943	2023	477	CFG_GPMC_A19_IN	-	-	vin2b_d0	vin1b_d0
M7	gpmc_a20	1440	621	1875	136	CFG_GPMC_A20_IN	-	-	vin2b_d1	vin1b_d1
J5	gpmc_a21	1602	1066	2021	604	CFG_GPMC_A21_IN	-	-	vin2b_d2	vin1b_d2
K6	gpmc_a22	1395	983	1822	519	CFG_GPMC_A22_IN	-	-	vin2b_d3	vin1b_d3
J7	gpmc_a23	1571	716	2045	200	CFG_GPMC_A23_IN	-	-	vin2b_d4	vin1b_d4
J4	gpmc_a24	1463	832	1893	396	CFG_GPMC_A24_IN	-	-	vin2b_d5	vin1b_d5
J6	gpmc_a25	1426	1166	1842	732	CFG_GPMC_A25_IN	-	-	vin2b_d6	vin1b_d6
H4	gpmc_a26	1362	1094	1797	584	CFG_GPMC_A26_IN	-	-	vin2b_d7	vin1b_d7
H5	gpmc_a27	1283	809	1760	338	CFG_GPMC_A27_IN	-	-	vin2b_hsync1	vin1b_hsync1
N6	gpmc_ben0	1978	780	2327	389	CFG_GPMC_BEN0_IN	-	-	vin2b_de1	vin1b_de1
M4	gpmc_ben1	0	0	0	0	CFG_GPMC_BEN1_IN	vin2b_clk1	vin1b_clk1	vin2b_fld1	vin1b_fld1
H6	gpmc_cs1	1411	982	1857	536	CFG_GPMC_CS1_IN	-	-	vin2b_vsync1	vin1b_vsync1

(1) Some signals listed are manual functions that present alternate multiplexing options. These manual functions are controlled via CTRL_CORE_ALT_SELECT_MUX or CTRL_CORE_VIP_MUX_SELECT registers. For more information on how to use these options, see *Pad Configuration Registers* section, *Control Module* chapter in the device TRM.

Manual IO Timings Modes must be used to ensure some IO timings for VIP1. See Table 7-2 *Modes Summary* for a list of IO timings requiring the use of Manual IO Timings Modes. See Table 7-13 *Manual Functions Mapping for VIN1A (IOSET8/9/10)* for a definition of the Manual modes.

Table 7-13 lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.

Table 7-13. Manual Functions Mapping for VIN1A (IOSET8/9/10)

BALL	BALL NAME	VIP_MANUAL15		VIP_MANUAL16		CFG REGISTER	MUXMODE	
		A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)		7	9
AC5	gpio6_10	2131	2198	2170	2180	CFG_GPIO6_10_IN	-	vin1a_clk0
AB4	gpio6_11	3720	2732	4106	2448	CFG_GPIO6_11_IN	-	vin1a_de0
C14	mcasp1_aclkx	2447	0	3042	0	CFG_MCASP1_ACLKX_IN	vin1a_fld0	-
G12	mcasp1_axr0	3061	0	3380	292	CFG_MCASP1_AXR0_IN	vin1a_vsync0	-
F12	mcasp1_axr1	3113	0	3396	304	CFG_MCASP1_AXR1_IN	vin1a_hsync0	-
B13	mcasp1_axr10	2803	0	3362	0	CFG_MCASP1_AXR10_IN	vin1a_d13	-
A12	mcasp1_axr11	3292	0	3357	546	CFG_MCASP1_AXR11_IN	vin1a_d12	-
E14	mcasp1_axr12	2854	0	3145	320	CFG_MCASP1_AXR12_IN	vin1a_d11	-
A13	mcasp1_axr13	2813	0	3229	196	CFG_MCASP1_AXR13_IN	vin1a_d10	-
G14	mcasp1_axr14	2471	0	3053	0	CFG_MCASP1_AXR14_IN	vin1a_d9	-
F14	mcasp1_axr15	2815	0	3225	201	CFG_MCASP1_AXR15_IN	vin1a_d8	-
B12	mcasp1_axr8	2965	0	3427	83	CFG_MCASP1_AXR8_IN	vin1a_d15	-
A11	mcasp1_axr9	3082	0	3253	440	CFG_MCASP1_AXR9_IN	vin1a_d14	-
D14	mcasp1_fsx	2898	0	3368	139	CFG_MCASP1_FSX_IN	vin1a_de0	-
A19	mcasp2_aclkx	2413	0	2972	0	CFG_MCASP2_ACLKX_IN	vin1a_d7	-
C15	mcasp2_axr2	2478	0	3062	0	CFG_MCASP2_AXR2_IN	vin1a_d5	-
A16	mcasp2_axr3	2806	0	3175	242	CFG_MCASP2_AXR3_IN	vin1a_d4	-
A18	mcasp2_fsx	2861	78	2936	599	CFG_MCASP2_FSX_IN	vin1a_d6	-
B18	mcasp3_aclkx	1583	0	1878	0	CFG_MCASP3_ACLKX_IN	vin1a_d3	-
B19	mcasp3_axr0	2873	0	3109	375	CFG_MCASP3_AXR0_IN	vin1a_d1	-
C17	mcasp3_axr1	1625	1400	2072	1023	CFG_MCASP3_AXR1_IN	vin1a_d0	vin1a_fld0
F15	mcasp3_fsx	2792	0	3146	257	CFG_MCASP3_FSX_IN	vin1a_d2	-
C18	mcasp4_aclkx	1547	268	1776	0	CFG_MCASP4_ACLKX_IN	-	vin1a_d15
G16	mcasp4_axr0	2362	587	2815	193	CFG_MCASP4_AXR0_IN	-	vin1a_d13
D17	mcasp4_axr1	2326	667	2769	304	CFG_MCASP4_AXR1_IN	-	vin1a_d12
A21	mcasp4_fsx	924	2573	1338	2219	CFG_MCASP4_FSX_IN	-	vin1a_d14
AA3	mcasp5_aclkx	3731	2106	4130	1708	CFG_MCASP5_ACLKX_IN	-	vin1a_d11
AB3	mcasp5_axr0	3800	3013	4159	2776	CFG_MCASP5_AXR0_IN	-	vin1a_d9
AA4	mcasp5_axr1	3828	2951	4179	2733	CFG_MCASP5_AXR1_IN	-	vin1a_d8
AB9	mcasp5_fsx	3675	2447	4074	2142	CFG_MCASP5_FSX_IN	-	vin1a_d10
AD4	mmc3_clk	3907	2744	4260	2450	CFG_MMC3_CLK_IN	-	vin1a_d7
AC4	mmc3_cmd	3892	2768	4242	2470	CFG_MMC3_CMD_IN	-	vin1a_d6

Table 7-13. Manual Functions Mapping for VIN1A (IOSET8/9/10) (continued)

BALL	BALL NAME	VIP_MANUAL15		VIP_MANUAL16		CFG REGISTER	MUXMODE	
		A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)		7	9
AC7	mmc3_dat0	3786	2765	4156	2522	CFG_MMC3_DAT0_IN	-	vin1a_d5
AC6	mmc3_dat1	3673	2961	4053	2667	CFG_MMC3_DAT1_IN	-	vin1a_d4
AC9	mmc3_dat2	3818	2447	4209	2096	CFG_MMC3_DAT2_IN	-	vin1a_d3
AC3	mmc3_dat3	3902	2903	4259	2672	CFG_MMC3_DAT3_IN	-	vin1a_d2
AC8	mmc3_dat4	3905	2622	4259	2342	CFG_MMC3_DAT4_IN	-	vin1a_d1
AD6	mmc3_dat5	3807	2824	4167	2595	CFG_MMC3_DAT5_IN	-	vin1a_d0
AB8	mmc3_dat6	3724	2818	4123	2491	CFG_MMC3_DAT6_IN	-	vin1a_hsync0
AB5	mmc3_dat7	3775	2481	4159	2161	CFG_MMC3_DAT7_IN	-	vin1a_vsync0
D18	xref_clk0	1971	0	2472	0	CFG_XREF_CLK0_IN	vin1a_d0	-
E17	xref_clk1	0	192	0	603	CFG_XREF_CLK1_IN	vin1a_clk0	-

7.7 Display Subsystem - Video Output Ports

Three Display Parallel Interfaces (DPI) channels are available in DSS named DPI Video Output 1, DPI Video Output 2 and DPI Video Output 3.

NOTE

The DPI Video Output i (i = 1 to 3) interface is also referred to as VOUTi.

Every VOUT interface consists of:

- 24-bit data bus (data[23:0])
- Horizontal synchronization signal (HSYNC)
- Vertical synchronization signal (VSYNC)
- Data enable (DE)
- Field ID (FID)
- Pixel clock (CLK)

NOTE

For more information, see *Display Subsystem* chapter in the device TRM.

CAUTION

The I/O Timings provided in this section are valid only if signals within a single IOSET are used. The IOSETs are defined in Table 7-18 .

CAUTION

The I/O Timings provided in this section are valid only for some DSS usage modes when the corresponding Virtual I/O Timings or Manual I/O Timings are configured as described in the tables found in this section.

CAUTION

All pads/balls configured as vouti_* signals must be programmed to use slow slew rate by setting the corresponding CTRL_CORE_PAD_*[SLEWCONTROL] register field to SLOW (0b1).

Table 7-14 through Table 7-17, and Figure 7-6 assume testing over the recommended operating conditions and electrical characteristic conditions.

Table 7-14. DPI Video Output i (i = 1..3) Default Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
D1	$t_{c(clk)}$	Cycle time, output pixel clock vouti_clk	DPI1/2/3 in 1.8V mode DPI2 in 3.3V mode	11.76 (3)		ns
			DPI1/3 in 3.3V mode	13.33 (3)		ns
D2	$t_{w(clkL)}$	Pulse duration, output pixel clock vouti_clk low		P*0.5-1 (1)		ns
D3	$t_{w(clkH)}$	Pulse duration, output pixel clock vouti_clk high		P*0.5-1 (1)		ns

Table 7-14. DPI Video Output i (i = 1..3) Default Switching Characteristics (continued)

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
D5	$t_{d(clk-ctlV)}$	Delay time, output pixel clock vouti_clk transition to output data vouti_d[23:0] valid	DPI1	-2.5	2.5	ns
D6	$t_{d(clk-dV)}$	Delay time, output pixel clock vouti_clk transition to output control signals vouti_vsync, vouti_hsync, vouti_de, and vouti_fld valid	DPI1	-2.5	2.5	ns
D5	$t_{d(clk-ctlV)}$	Delay time, output pixel clock vouti_clk transition to output data vouti_d[23:0] valid	DPI2 (vin2a_fld0 clock reference)	-2.5	2.5	ns
D6	$t_{d(clk-dV)}$	Delay time, output pixel clock vouti_clk transition to output control signals vouti_vsync, vouti_hsync, vouti_de, and vouti_fld valid	DPI2 (vin2a_fld0 clock reference)	-2.5	2.5	ns
D5	$t_{d(clk-ctlV)}$	Delay time, output pixel clock vouti_clk transition to output data vouti_d[23:0] valid	DPI2 (xref_clk2 clock reference)	-2.5	2.5	ns
D6	$t_{d(clk-dV)}$	Delay time, output pixel clock vouti_clk transition to output control signals vouti_vsync, vouti_hsync, vouti_de, and vouti_fld valid	DPI2 (xref_clk2 clock reference)	-2.5	2.5	ns
D5	$t_{d(clk-ctlV)}$	Delay time, output pixel clock vouti_clk transition to output data vouti_d[23:0] valid	DPI3	-2.5	2.5	ns
D6	$t_{d(clk-dV)}$	Delay time, output pixel clock vouti_clk transition to output control signals vouti_vsync, vouti_hsync, vouti_de, and vouti_fld valid	DPI3	-2.5	2.5	ns

(1) P = output vouti_clk period in ns.

(2) All pads/balls configured as vouti_* signals must be programmed to use slow slew rate by setting the corresponding CTRL_CORE_PAD_*[SLEWCONTROL] register field to SLOW (0b1).

(3) SERDES transceivers may be sensitive to the jitter profile of vouti_clk. See Application Note **SPRAC62** for additional guidance.

Table 7-15. DPI Video Output i (i = 1..3) Alternate Switching Characteristics[(2)]

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
D1	$t_{c(clk)}$	Cycle time, output pixel clock vouti_clk	DPI1/2/3 in 1.8V mode DPI2 in 3.3V mode	6.06[(3)]		ns
			DPI1/3 in 3.3V mode	13.33[(3)]		ns
D2	$t_{w(clkL)}$	Pulse duration, output pixel clock vouti_clk low		P*0.5-1 [(1)]		ns
D3	$t_{w(clkH)}$	Pulse duration, output pixel clock vouti_clk high		P*0.5-1 [(1)]		ns
D5	$t_{d(clk-ctlV)}$	Delay time, output pixel clock vouti_clk transition to output data vouti_d[23:0] valid	DPI1	1.51	4.55	ns
D6	$t_{d(clk-dV)}$	Delay time, output pixel clock vouti_clk transition to output control signals vouti_vsync, vouti_hsync, vouti_de, and vouti_fld valid	DPI1	1.51	4.55	ns
D5	$t_{d(clk-ctlV)}$	Delay time, output pixel clock vouti_clk transition to output data vouti_d[23:0] valid	DPI2 (vin2a_fld0 clock reference)	1.51	4.55	ns
D6	$t_{d(clk-dV)}$	Delay time, output pixel clock vouti_clk transition to output control signals vouti_vsync, vouti_hsync, vouti_de, and vouti_fld valid	DPI2 (vin2a_fld0 clock reference)	1.51	4.55	ns
D5	$t_{d(clk-ctlV)}$	Delay time, output pixel clock vouti_clk transition to output data vouti_d[23:0] valid	DPI2 (xref_clk2 clock reference)	1.51	4.55	ns
D6	$t_{d(clk-dV)}$	Delay time, output pixel clock vouti_clk transition to output control signals vouti_vsync, vouti_hsync, vouti_de, and vouti_fld valid	DPI2 (xref_clk2 clock reference)	1.51	4.55	ns
D5	$t_{d(clk-ctlV)}$	Delay time, output pixel clock vouti_clk transition to output data vouti_d[23:0] valid	DPI3	1.51	4.55	ns
D6	$t_{d(clk-dV)}$	Delay time, output pixel clock vouti_clk transition to output control signals vouti_vsync, vouti_hsync, vouti_de, and vouti_fld valid	DPI3	1.51	4.55	ns

(1) P = output vouti_clk period in ns.

(2) All pads/balls configured as vouti_* signals must be programmed to use slow slew rate by setting the corresponding CTRL_CORE_PAD_*[SLEWCONTROL] register field to SLOW (0b1).

(3) SERDES transceivers may be sensitive to the jitter profile of vouti_clk. See Application Note **SPRAC62** for additional guidance.

Table 7-16. DPI Video Output i (i = 1..3) MANUAL4 Switching Characteristics (2)

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
D1	$t_{c(clk)}$	Cycle time, output pixel clock vouti_clk	DPI1/2/3 in 1.8V mode DPI2 in 3.3V mode	6.06 (3)		ns
			DPI1/3 in 3.3V mode	13.33 (3)		ns
D2	$t_{w(clkL)}$	Pulse duration, output pixel clock vouti_clk low		P*0.5-1 (1)		ns
D3	$t_{w(clkH)}$	Pulse duration, output pixel clock vouti_clk high		P*0.5-1 (1)		ns
D5	$t_{d(clk-ctlV)}$	Delay time, output pixel clock vouti_clk transition to output data vouti_d[23:0] valid	DPI1	2.85	5.56	ns
D6	$t_{d(clk-dV)}$	Delay time, output pixel clock vouti_clk transition to output control signals vouti_vsync, vouti_hsync, vouti_de, and vouti_fld valid	DPI1	2.85	5.56	ns
D5	$t_{d(clk-ctlV)}$	Delay time, output pixel clock vouti_clk transition to output data vouti_d[23:0] valid	DPI2 (vin2a_fld0 clock reference)	2.85	5.56	ns
D6	$t_{d(clk-dV)}$	Delay time, output pixel clock vouti_clk transition to output control signals vouti_vsync, vouti_hsync, vouti_de, and vouti_fld valid	DPI2 (vin2a_fld0 clock reference)	2.85	5.56	ns
D5	$t_{d(clk-ctlV)}$	Delay time, output pixel clock vouti_clk transition to output data vouti_d[23:0] valid	DPI2 (xref_clk2 clock reference)	2.85	5.56	ns
D6	$t_{d(clk-dV)}$	Delay time, output pixel clock vouti_clk transition to output control signals vouti_vsync, vouti_hsync, vouti_de, and vouti_fld valid	DPI2 (xref_clk2 clock reference)	2.85	5.56	ns
D5	$t_{d(clk-ctlV)}$	Delay time, output pixel clock vouti_clk transition to output data vouti_d[23:0] valid	DPI3	2.85	5.56	ns
D6	$t_{d(clk-dV)}$	Delay time, output pixel clock vouti_clk transition to output control signals vouti_vsync, vouti_hsync, vouti_de, and vouti_fld valid	DPI3	2.85	5.56	ns

(1) P = output vouti_clk period in ns.

(2) All pads/balls configured as vouti_* signals must be programmed to use slow slew rate by setting the corresponding CTRL_CORE_PAD_*[SLEWCONTROL] register field to SLOW (0b1).

(3) SERDES transceivers may be sensitive to the jitter profile of vouti_clk. See Application Note **SPRAC62** for additional guidance.

Table 7-17. DPI Video Output i (i = 1..3) MANUAL5 Switching Characteristics (2)

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
D1	$t_{c(clk)}$	Cycle time, output pixel clock vouti_clk	DPI1/2/3 in 1.8V mode DPI2 in 3.3V mode	6.06 (3)		ns
			DPI1/3 in 3.3V mode	13.33 (3)		ns
D2	$t_{w(clkL)}$	Pulse duration, output pixel clock vouti_clk low		P*0.5-1 (1)		ns
D3	$t_{w(clkH)}$	Pulse duration, output pixel clock vouti_clk high		P*0.5-1 (1)		ns
D5	$t_{d(clk-ctlV)}$	Delay time, output pixel clock vouti_clk transition to output data vouti_d[23:0] valid	DPI1	3.55	6.61	ns
D6	$t_{d(clk-dV)}$	Delay time, output pixel clock vouti_clk transition to output control signals vouti_vsync, vouti_hsync, vouti_de, and vouti_fld valid	DPI1	3.55	6.61	ns
D5	$t_{d(clk-ctlV)}$	Delay time, output pixel clock vouti_clk transition to output data vouti_d[23:0] valid	DPI2 (vin2a_fld0 clock reference)	3.55	6.61	ns

Table 7-17. DPI Video Output i (i = 1..3) MANUAL5 Switching Characteristics [(2)] (continued)

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
D6	$t_{d(clk-dV)}$	Delay time, output pixel clock vouti_clk transition to output control signals vouti_vsync, vouti_hsync, vouti_de, and vouti_fld valid	DPI2 (vin2a_fld0 clock reference)	3.55	6.61	ns
D5	$t_{d(clk-ctlV)}$	Delay time, output pixel clock vouti_clk transition to output data vouti_d[23:0] valid	DPI2 (xref_clk2 clock reference)	3.55	6.61	ns
D6	$t_{d(clk-dV)}$	Delay time, output pixel clock vouti_clk transition to output control signals vouti_vsync, vouti_hsync, vouti_de, and vouti_fld valid	DPI2 (xref_clk2 clock reference)	3.55	6.61	ns
D5	$t_{d(clk-ctlV)}$	Delay time, output pixel clock vouti_clk transition to output data vouti_d[23:0] valid	DPI3	3.55	6.61	ns
D6	$t_{d(clk-dV)}$	Delay time, output pixel clock vouti_clk transition to output control signals vouti_vsync, vouti_hsync, vouti_de, and vouti_fld valid	DPI3	3.55	6.61	ns

(1) P = output vouti_clk period in ns.

(2) All pads/balls configured as vouti_* signals must be programmed to use slow slew rate by setting the corresponding CTRL_CORE_PAD_*[SLEWCONTROL] register field to SLOW (0b1).

(3) SERDES transceivers may be sensitive to the jitter profile of vouti_clk. See Application Note **SPRAC62** for additional guidance.

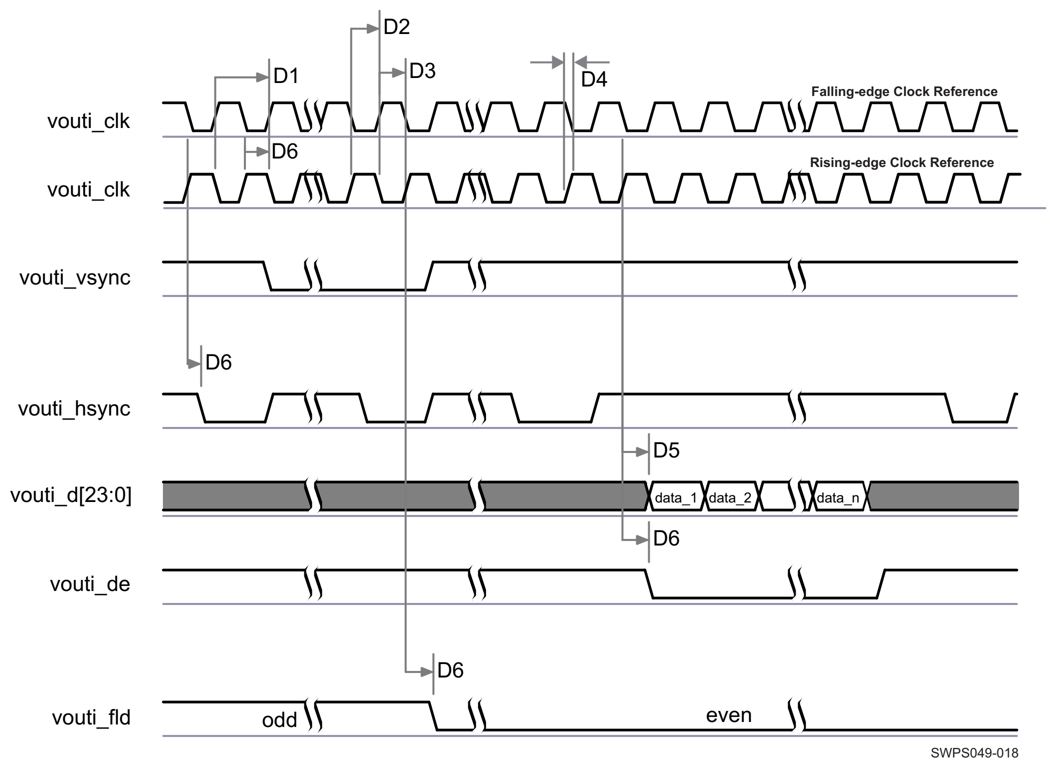


Figure 7-6. DPI Video Output[(1)(2)(3)]

(1) The configuration of assertion of the data can be programmed on the falling or rising edge of the pixel clock.

(2) The polarity and the pulse width of vouti_hsync and vouti_vsync are programmable, refer to the DSS section of the device TRM.

(3) The vouti_clk frequency can be configured, refer to the DSS section of the device TRM.

In Table 7-18 are presented the specific groupings of signals (IOSET) for use with VOUT2.

Table 7-18. VOUT2 IOSETs

SIGNALS	IOSET1		IOSET2	
	BALL	MUX	BALL	MUX
vout2_d23	F2	4	AA4	6

Table 7-18. VOUT2 IOSETs (continued)

SIGNALS	IOSET1		IOSET2	
	BALL	MUX	BALL	MUX
vout2_d22	F3	4	AB3	6
vout2_d21	D1	4	AB9	6
vout2_d20	E2	4	AA3	6
vout2_d19	D2	4	D17	6
vout2_d18	F4	4	G16	6
vout2_d17	C1	4	A21	6
vout2_d16	E4	4	C18	6
vout2_d15	F5	4	A17	6
vout2_d14	E6	4	B17	6
vout2_d13	D3	4	B16	6
vout2_d12	F6	4	D15	6
vout2_d11	D5	4	A15	6
vout2_d10	C2	4	B15	6
vout2_d9	C3	4	A20	6
vout2_d8	C4	4	E15	6
vout2_d7	B2	4	D12	6
vout2_d6	D6	4	C12	6
vout2_d5	C5	4	F13	6
vout2_d4	A3	4	E12	6
vout2_d3	B3	4	J11	6
vout2_d2	B4	4	G13	6
vout2_d1	B5	4	J14	6
vout2_d0	A4	4	B14	6
vout2_vsync	G6	4	F20	6
vout2_hsync	G1	4	E21	6
vout2_clk	H7	4	B26	6
vout2_fld	E1	4	F21	6
vout2_de	G2	4	C23	6

NOTE

To configure the desired virtual mode the user must set MODESELECT bit and DELAYMODE bit field for each corresponding pad control register.

The pad control registers are presented in Table 4-3 and described in Device TRM, *Control Module Chapter*.

Virtual IO Timings Modes must be used to ensure some IO timings for VOUT1. See Table 7-2 *Modes Summary* for a list of IO timings requiring the use of Virtual IO Timings Modes. See Table 7-19 *Virtual Functions Mapping for VOUT1* for a definition of the Virtual modes.

Table 7-19 presents the values for DELAYMODE bit field.

Table 7-19. Virtual Functions Mapping for DSS VOUT1

BALL	BALL NAME	Delay Mode Value	MUXMODE	
		DSS_VIRTUAL1	0	3
H3	gpmc_ad15	14		vout3_d15
D9	vout1_d9	15	vout1_d9	
N7	gpmc_a8	15		vout3_hsync

Table 7-19. Virtual Functions Mapping for DSS VOUT1 (continued)

BALL	BALL NAME	Delay Mode Value	MUXMODE	
		DSS_VIRTUAL1	0	3
L6	gpmc_ad4	14		vout3_d4
E8	vout1_d8	15	vout1_d8	
M6	gpmc_ad0	14		vout3_d0
F9	vout1_d5	15	vout1_d5	
J3	gpmc_ad13	14		vout3_d13
T6	gpmc_a2	15		vout3_d18
M2	gpmc_ad1	14		vout3_d1
P6	gpmc_a4	15		vout3_d20
B10	vout1_de	15	vout1_de	
B7	vout1_d16	15	vout1_d16	
R5	gpmc_a6	15		vout3_d22
A9	vout1_d21	15	vout1_d21	
H2	gpmc_ad14	14		vout3_d14
T9	gpmc_a1	15		vout3_d17
E7	vout1_d7	15	vout1_d7	
C11	vout1_hsync	15	vout1_hsync	
D11	vout1_clk	15	vout1_clk	
P1	gpmc_cs3	15		vout3_clk
B9	vout1_d22	15	vout1_d22	
G11	vout1_d3	15	vout1_d3	
R4	gpmc_a9	15		vout3_vsync
D8	vout1_d11	15	vout1_d11	
J2	gpmc_ad11	14		vout3_d11
L3	gpmc_ad6	14		vout3_d6
D7	vout1_d10	15	vout1_d10	
L5	gpmc_ad2	14		vout3_d2
F10	vout1_d2	15	vout1_d2	
M1	gpmc_ad3	14		vout3_d3
P5	gpmc_a7	15		vout3_d23
T7	gpmc_a3	15		vout3_d19
A7	vout1_d18	15	vout1_d18	
C7	vout1_d15	15	vout1_d15	
J1	gpmc_ad10	14		vout3_d10
L2	gpmc_ad7	14		vout3_d7
N9	gpmc_a10	15		vout3_de
F11	vout1_d0	15	vout1_d0	
G10	vout1_d1	15	vout1_d1	
R9	gpmc_a5	15		vout3_d21
L1	gpmc_ad8	14		vout3_d8
F8	vout1_d6	15	vout1_d6	
L4	gpmc_ad5	14		vout3_d5
A10	vout1_d23	15	vout1_d23	
E11	vout1_vsync	15	vout1_vsync	
C9	vout1_d20	15	vout1_d20	
R6	gpmc_a0	15		vout3_d16
A8	vout1_d19	15	vout1_d19	

Table 7-19. Virtual Functions Mapping for DSS VOUT1 (continued)

BALL	BALL NAME	Delay Mode Value	MUXMODE	
		DSS_VIRTUAL1	0	3
E9	vout1_d4	15	vout1_d4	
H1	gpmc_ad12	14		vout3_d12
B11	vout1_fld	15	vout1_fld	
P9	gpmc_a11	15		vout3_fld
K2	gpmc_ad9	14		vout3_d9
C6	vout1_d13	15	vout1_d13	
B8	vout1_d17	15	vout1_d17	
A5	vout1_d12	15	vout1_d12	
C8	vout1_d14	15	vout1_d14	

NOTE

To configure the desired Manual IO Timing Mode the user must follow the steps described in section "*Manual IO Timing Modes*" in the device TRM.

The associated registers to configure are listed in the **CFG REGISTER** column. For more information, see *Control Module* chapter in the device TRM.

Manual IO Timings Modes must be used to ensure some IO timings for VOUT1. See Table 7-2 *Modes Summary* for a list of IO timings requiring the use of Manual IO Timings Modes. See Table 7-20 *Manual Functions Mapping for DSS VOUT1* for a definition of the Manual modes.

Table 7-20 lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.

Table 7-20. Manual Functions Mapping for DSS VOUT1

BALL	BALL NAME	VOUT1_MANUAL1		VOUT1_MANUAL4		VOUT1_MANUAL5		CFG REGISTER	MUXMODE
		A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)		0
D11	vout1_clk	0	212	0	249	0	249	CFG_VOUT1_CLK_OUT	vout1_clk
F11	vout1_d0	2502	0	3778	0	4648	0	CFG_VOUT1_D0_OUT	vout1_d0
G10	vout1_d1	2402	0	3650	0	4520	0	CFG_VOUT1_D1_OUT	vout1_d1
D7	vout1_d10	2147	0	3353	0	4223	0	CFG_VOUT1_D10_OUT	vout1_d10
D8	vout1_d11	2249	0	3588	0	4458	0	CFG_VOUT1_D11_OUT	vout1_d11
A5	vout1_d12	2410	0	3733	0	4603	0	CFG_VOUT1_D12_OUT	vout1_d12
C6	vout1_d13	2129	0	3427	0	4297	0	CFG_VOUT1_D13_OUT	vout1_d13
C8	vout1_d14	2279	0	3485	0	4355	0	CFG_VOUT1_D14_OUT	vout1_d14
C7	vout1_d15	2266	23	3573	0	4443	0	CFG_VOUT1_D15_OUT	vout1_d15
B7	vout1_d16	1798	0	3069	0	3939	0	CFG_VOUT1_D16_OUT	vout1_d16
B8	vout1_d17	2243	0	3492	0	4362	0	CFG_VOUT1_D17_OUT	vout1_d17
A7	vout1_d18	2127	0	3319	0	4189	0	CFG_VOUT1_D18_OUT	vout1_d18
A8	vout1_d19	2096	0	3455	0	4225	0	CFG_VOUT1_D19_OUT	vout1_d19
F10	vout1_d2	2375	0	3788	0	4658	0	CFG_VOUT1_D2_OUT	vout1_d2
C9	vout1_d20	2105	0	3402	0	4272	0	CFG_VOUT1_D20_OUT	vout1_d20
A9	vout1_d21	2120	0	3477	0	4347	0	CFG_VOUT1_D21_OUT	vout1_d21
B9	vout1_d22	2013	65	3395	0	4265	0	CFG_VOUT1_D22_OUT	vout1_d22
A10	vout1_d23	1887	0	3213	0	3983	0	CFG_VOUT1_D23_OUT	vout1_d23
G11	vout1_d3	2429	0	3753	0	4623	0	CFG_VOUT1_D3_OUT	vout1_d3
E9	vout1_d4	2639	0	3728	0	4598	0	CFG_VOUT1_D4_OUT	vout1_d4
F9	vout1_d5	2319	0	3643	0	4363	0	CFG_VOUT1_D5_OUT	vout1_d5

Table 7-20. Manual Functions Mapping for DSS VOUT1 (continued)

BALL	BALL NAME	VOUT1_MANUAL1		VOUT1_MANUAL4		VOUT1_MANUAL5		CFG REGISTER	MUXMODE
		A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)		0
F8	vout1_d6	2227	0	3544	0	4264	0	CFG_VOUT1_D6_OUT	vout1_d6
E7	vout1_d7	2309	0	3707	0	4427	0	CFG_VOUT1_D7_OUT	vout1_d7
E8	vout1_d8	1999	0	3315	0	4185	0	CFG_VOUT1_D8_OUT	vout1_d8
D9	vout1_d9	2276	0	3539	0	4409	0	CFG_VOUT1_D9_OUT	vout1_d9
B10	vout1_de	1933	0	3507	0	4177	0	CFG_VOUT1_DE_OUT	vout1_de
B11	vout1_fld	1825	0	3382	0	4052	0	CFG_VOUT1_FLD_OUT	vout1_fld
C11	vout1_hsync	1741	13	3408	0	4278	0	CFG_VOUT1_HSYNC_OUT	vout1_hsync
E11	vout1_vsync	2338	0	3718	0	4588	0	CFG_VOUT1_VSYNC_OUT	vout1_vsync

Manual IO Timings Modes must be used to ensure some IO timings for VOUT2. See Table 7-2 *Modes Summary* for a list of IO timings requiring the use of Manual IO Timings Modes. See Table 7-21 *Manual Functions Mapping for DSS VOUT2 IOSET1* for a definition of the Manual modes.

Table 7-21 lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.

Table 7-21. Manual Functions Mapping for DSS VOUT2 IOSET1

BALL	BALL NAME	VOUT2_IOSET1_MANUAL1		VOUT2_IOSET1_MANUAL2		VOUT2_IOSET1_MANUAL3		VOUT2_IOSET1_MANUAL4		VOUT2_IOSET1_MANUAL5		CFG REGISTER	MUXMODE
		A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)		4
E1	vin2a_clk0	2571	0	1059	0	1025	0	4110	0	4980	0	CFG_VIN2A_CLK0_OUT	vout2_fld
F2	vin2a_d0	2124	0	589	0	577	0	3613	0	4483	0	CFG_VIN2A_D0_OUT	vout2_d23
F3	vin2a_d1	2103	0	568	0	557	0	3442	0	4312	0	CFG_VIN2A_D1_OUT	vout2_d22
D3	vin2a_d10	2091	0	557	0	545	0	3430	0	4200	0	CFG_VIN2A_D10_OUT	vout2_d13
F6	vin2a_d11	2142	0	608	0	596	0	3481	0	4251	0	CFG_VIN2A_D11_OUT	vout2_d12
D5	vin2a_d12	2920	385	1816	255	1783	276	3943	601	4713	601	CFG_VIN2A_D12_OUT	vout2_d11
C2	vin2a_d13	2776	322	1872	192	1838	213	3799	538	4669	538	CFG_VIN2A_D13_OUT	vout2_d10
C3	vin2a_d14	2904	0	1769	0	1757	0	3869	174	4739	174	CFG_VIN2A_D14_OUT	vout2_d9
C4	vin2a_d15	2670	257	1665	127	1632	148	3792	473	4662	473	CFG_VIN2A_D15_OUT	vout2_d8
B2	vin2a_d16	2814	155	1908	31	1878	43	3837	371	4707	371	CFG_VIN2A_D16_OUT	vout2_d7
D6	vin2a_d17	3002	199	1897	69	1865	89	4024	415	4894	415	CFG_VIN2A_D17_OUT	vout2_d6
C5	vin2a_d18	1893	0	358	0	347	0	3432	0	4302	0	CFG_VIN2A_D18_OUT	vout2_d5
A3	vin2a_d19	1698	0	163	0	151	0	3237	0	4007	0	CFG_VIN2A_D19_OUT	vout2_d4
D1	vin2a_d2	2193	0	658	0	646	0	3531	0	4401	0	CFG_VIN2A_D2_OUT	vout2_d21
B3	vin2a_d20	1736	0	202	0	190	0	3075	0	3945	0	CFG_VIN2A_D20_OUT	vout2_d3
B4	vin2a_d21	1636	0	101	0	89	0	3074	0	3944	0	CFG_VIN2A_D21_OUT	vout2_d2
B5	vin2a_d22	1628	0	93	0	81	0	3266	0	4036	0	CFG_VIN2A_D22_OUT	vout2_d1
A4	vin2a_d23	1538	0	0	0	0	0	2968	0	3838	0	CFG_VIN2A_D23_OUT	vout2_d0
E2	vin2a_d3	1997	0	462	0	450	0	3335	0	4205	0	CFG_VIN2A_D3_OUT	vout2_d20
D2	vin2a_d4	2528	0	993	0	982	0	3867	0	4537	0	CFG_VIN2A_D4_OUT	vout2_d19
F4	vin2a_d5	2038	0	503	0	492	0	3577	0	4347	0	CFG_VIN2A_D5_OUT	vout2_d18
C1	vin2a_d6	1746	0	211	0	200	0	3285	0	4055	0	CFG_VIN2A_D6_OUT	vout2_d17
E4	vin2a_d7	2213	0	678	0	666	0	3552	0	4272	0	CFG_VIN2A_D7_OUT	vout2_d16
F5	vin2a_d8	2268	0	733	0	721	0	3607	0	4277	0	CFG_VIN2A_D8_OUT	vout2_d15
E6	vin2a_d9	2170	0	635	0	623	0	3509	0	4379	0	CFG_VIN2A_D9_OUT	vout2_d14
G2	vin2a_de0	2102	0	568	0	556	0	3841	0	4611	0	CFG_VIN2A_DE0_OUT	vout2_de
H7	vin2a_fld0	0	983	1398	1185	1385	1202	0	994	0	994	CFG_VIN2A_FLD0_OUT	vout2_clk
G1	vin2a_hsync0	2482	0	974	0	936	0	4021	0	4891	0	CFG_VIN2A_HSYNC0_OUT	vout2_hsync

Table 7-21. Manual Functions Mapping for DSS VOUT2 IOSET1 (continued)

BALL	BALL NAME	VOUT2_IOSET1_MANUAL1		VOUT2_IOSET1_MANUAL2		VOUT2_IOSET1_MANUAL3		VOUT2_IOSET1_MANUAL4		VOUT2_IOSET1_MANUAL5		CFG REGISTER	MUXMODE
		A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)		4
G6	vin2a_vsync0	2296	0	784	0	750	0	3935	0	4805	0	CFG_VIN2A_VSYNC0_OUT	vout2_vsync

Manual IO Timings Modes must be used to ensure some IO timings for VOUT2. See Table 7-2 *Modes Summary* for a list of IO timings requiring the use of Manual IO Timings Modes. See Table 7-22 *Manual Functions Mapping for DSS VOUT2 IOSET2* for a definition of the Manual modes.

Table 7-22 lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.

Table 7-22. Manual Functions Mapping for DSS VOUT2 IOSET2

BALL	BALL NAME	VOUT2_IOSET2_MANUAL1		VOUT2_IOSET2_MANUAL2		VOUT2_IOSET2_MANUAL3		VOUT2_IOSET2_MANUAL4		VOUT2_IOSET2_MANUAL5		CFG REGISTER	MUXMODE
		A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)		6
E21	gpio6_14	1983	0	79	0	68	0	3513	0	4383	0	CFG_GPIO6_14_OUT	vout2_hsync
F20	gpio6_15	2159	0	158	0	148	0	3689	0	4559	0	CFG_GPIO6_15_OUT	vout2_vsync
F21	gpio6_16	1864	0	0	0	0	0	3394	0	4264	0	CFG_GPIO6_16_OUT	vout2_fld
B14	mcasp1_aclkr	2614	0	1255	0	1270	0	4353	0	5223	0	CFG_MCASP1_ACLKR_OUT	vout2_d0
G13	mcasp1_axr2	2705	0	1350	0	1360	0	4444	0	5314	0	CFG_MCASP1_AXR2_OUT	vout2_d2
J11	mcasp1_axr3	2865	0	1210	0	1219	0	4504	0	5374	0	CFG_MCASP1_AXR3_OUT	vout2_d3
E12	mcasp1_axr4	2759	0	1404	0	1413	0	4498	0	5368	0	CFG_MCASP1_AXR4_OUT	vout2_d4
F13	mcasp1_axr5	2980	0	1325	0	1335	0	4419	0	5289	0	CFG_MCASP1_AXR5_OUT	vout2_d5
C12	mcasp1_axr6	2634	0	1275	0	1289	0	4373	0	5243	0	CFG_MCASP1_AXR6_OUT	vout2_d6
D12	mcasp1_axr7	2658	0	1302	0	1311	0	4396	0	5266	0	CFG_MCASP1_AXR7_OUT	vout2_d7
J14	mcasp1_fsr	2818	0	1163	0	1172	0	4456	0	5326	0	CFG_MCASP1_FSR_OUT	vout2_d1
E15	mcasp2_aclkr	2728	0	1373	0	1382	0	4367	0	5237	0	CFG_MCASP2_ACLKR_OUT	vout2_d8
B15	mcasp2_axr0	2513	0	319	534	308	560	4151	0	5021	0	CFG_MCASP2_AXR0_OUT	vout2_d10

Table 7-22. Manual Functions Mapping for DSS VOUT2 IOSET2 (continued)

BALL	BALL NAME	VOUT2_IOSET2_MANUAL1		VOUT2_IOSET2_MANUAL2		VOUT2_IOSET2_MANUAL3		VOUT2_IOSET2_MANUAL4		VOUT2_IOSET2_MANUAL5		CFG REGISTER	MUXMODE
		A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)		6
A15	mcasp2_axr1	2712	0	1357	0	1366	0	4351	0	5221	0	CFG_MCASP2_AXR1_OUT	vout2_d11
D15	mcasp2_axr4	2529	0	1169	0	1184	0	4267	0	5137	0	CFG_MCASP2_AXR4_OUT	vout2_d12
B16	mcasp2_axr5	2376	0	543	478	1029	0	4114	0	4984	0	CFG_MCASP2_AXR5_OUT	vout2_d13
B17	mcasp2_axr6	2620	0	1265	0	1274	0	4359	0	5229	0	CFG_MCASP2_AXR6_OUT	vout2_d14
A17	mcasp2_axr7	2492	0	354	483	845	0	4130	0	5000	0	CFG_MCASP2_AXR7_OUT	vout2_d15
A20	mcasp2_fsr	2358	0	12	487	513	0	3797	0	4667	0	CFG_MCASP2_FSR_OUT	vout2_d9
C18	mcasp4_aclkx	2524	0	1165	0	1179	0	3863	0	4733	0	CFG_MCASP4_ACLKX_OUT	vout2_d16
G16	mcasp4_axr0	2578	0	797	0	806	0	4208	0	5078	0	CFG_MCASP4_AXR0_OUT	vout2_d18
D17	mcasp4_axr1	2253	0	750	0	759	0	3983	0	4853	0	CFG_MCASP4_AXR1_OUT	vout2_d19
A21	mcasp4_fsx	2478	0	823	0	832	0	4117	0	4987	0	CFG_MCASP4_FSX_OUT	vout2_d17
AA3	mcasp5_aclkx	4672	1737	3256	1798	3226	1837	5900	1949	6770	1949	CFG_MCASP5_ACLKX_OUT	vout2_d20
AB3	mcasp5_axr0	4642	1286	3226	1347	3196	1386	5870	1497	6740	1497	CFG_MCASP5_AXR0_OUT	vout2_d22
AA4	mcasp5_axr1	4625	725	3209	786	3179	825	6153	935	7023	935	CFG_MCASP5_AXR1_OUT	vout2_d23
AB9	mcasp5_fsx	4565	1062	3149	1123	3119	1162	6093	1273	6963	1273	CFG_MCASP5_FSX_OUT	vout2_d21
B26	xref_clk2	0	49	1359	466	1341	512	0	60	0	60	CFG_XREF_CLK2_OUT	vout2_clk
C23	xref_clk3	1947	0	36	0	45	0	3378	0	4248	0	CFG_XREF_CLK3_OUT	vout2_de

Manual IO Timings Modes must be used to ensure some IO timings for VOUT3. See Table 7-2 *Modes Summary* for a list of IO timings requiring the use of Manual IO Timings Modes. See Table 7-23 *Manual Functions Mapping for DSS VOUT3* for a definition of the Manual modes.

Table 7-23 lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.

Table 7-23. Manual Functions Mapping for DSS VOUT3

BALL	BALL NAME	VOUT3_MANUAL1		VOUT3_MANUAL4		VOUT3_MANUAL5		CFG REGISTER	MUXMODE
		A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)		3
R6	gpmc_a0	2395	0	3909	0	4779	0	CFG_GPMC_A0_OUT	vout3_d16
T9	gpmc_a1	2412	0	3957	0	4827	0	CFG_GPMC_A1_OUT	vout3_d17
N9	gpmc_a10	2473	0	3980	0	4850	0	CFG_GPMC_A10_OUT	vout3_de
P9	gpmc_a11	2906	0	4253	0	5123	0	CFG_GPMC_A11_OUT	vout3_fld
T6	gpmc_a2	2360	0	3873	0	4743	0	CFG_GPMC_A2_OUT	vout3_d18
T7	gpmc_a3	2391	0	4112	0	4982	0	CFG_GPMC_A3_OUT	vout3_d19
P6	gpmc_a4	2626	0	4336	0	5206	0	CFG_GPMC_A4_OUT	vout3_d20
R9	gpmc_a5	2338	0	3840	0	4710	0	CFG_GPMC_A5_OUT	vout3_d21
R5	gpmc_a6	2374	0	3913	0	4783	0	CFG_GPMC_A6_OUT	vout3_d22
P5	gpmc_a7	2432	0	3947	0	4817	0	CFG_GPMC_A7_OUT	vout3_d23
N7	gpmc_a8	3155	0	4309	105	5179	105	CFG_GPMC_A8_OUT	vout3_hsync
R4	gpmc_a9	2309	0	3842	0	4712	0	CFG_GPMC_A9_OUT	vout3_vsync
M6	gpmc_ad0	2360	0	3652	0	4522	0	CFG_GPMC_AD0_OUT	vout3_d0
M2	gpmc_ad1	2420	0	3762	0	4632	0	CFG_GPMC_AD1_OUT	vout3_d1
J1	gpmc_ad10	2235	0	3456	0	4326	0	CFG_GPMC_AD10_OUT	vout3_d10
J2	gpmc_ad11	2253	0	3584	0	4454	0	CFG_GPMC_AD11_OUT	vout3_d11
H1	gpmc_ad12	1949	427	3589	0	4459	0	CFG_GPMC_AD12_OUT	vout3_d12
J3	gpmc_ad13	2318	0	3547	0	4417	0	CFG_GPMC_AD13_OUT	vout3_d13
H2	gpmc_ad14	2123	0	3302	0	4172	0	CFG_GPMC_AD14_OUT	vout3_d14
H3	gpmc_ad15	2195	29	3532	0	4402	0	CFG_GPMC_AD15_OUT	vout3_d15
L5	gpmc_ad2	2617	0	3859	0	4729	0	CFG_GPMC_AD2_OUT	vout3_d2
M1	gpmc_ad3	2350	0	3590	0	4460	0	CFG_GPMC_AD3_OUT	vout3_d3
L6	gpmc_ad4	2324	0	3534	0	4404	0	CFG_GPMC_AD4_OUT	vout3_d4
L4	gpmc_ad5	2371	0	3609	0	4479	0	CFG_GPMC_AD5_OUT	vout3_d5
L3	gpmc_ad6	2231	0	3416	0	4286	0	CFG_GPMC_AD6_OUT	vout3_d6
L2	gpmc_ad7	2440	0	3661	0	4531	0	CFG_GPMC_AD7_OUT	vout3_d7
L1	gpmc_ad8	2479	0	3714	0	4584	0	CFG_GPMC_AD8_OUT	vout3_d8
K2	gpmc_ad9	2355	0	3593	0	4463	0	CFG_GPMC_AD9_OUT	vout3_d9
P1	gpmc_cs3	0	641	0	905	0	905	CFG_GPMC_CS3_OUT	vout3_clk

7.8 Display Subsystem - High-Definition Multimedia Interface (HDMI)

The High-Definition Multimedia Interface is provided for transmitting digital television audiovisual signals from DVD players, set-top boxes and other audiovisual sources to television sets, projectors and other video displays. The HDMI interface is aligned with the HDMI TMDS single stream standard v1.4a (720p @60Hz to 1080p @24Hz) and the HDMI v1.3 (1080p @60Hz): 3 data channels, plus 1 clock channel is supported (differential).

NOTE

For more information, see *High-Definition Multimedia Interface* section in the device TRM.

7.9 Camera Serial Interface 2 CAL bridge (CSI2)

NOTE

For more information, see *Camera Interface Subsystem* chapter in the device TRM.

The camera adaptation layer (CAL) deals with the processing of the pixel data coming from an external image sensor, data from memory. The CAL is a key component for the following multimedia applications: camera viewfinder, video record, and still image capture. The CAL has two serial camera interfaces (primary and secondary):

- The primary serial interface (CSI2 Port A) is compliant with MIPI CSI-2 protocol with four data lanes.
- The secondary serial interface (CSI2 Port B) is compliant with MIPI CSI-2 protocol with two data lanes.

7.9.1 CSI-2 MIPI D-PHY

The CSI-2 port A is compliant with the MIPI D-PHY RX specification v1.00.00 and the MIPI CSI-2 specification v1.00, with 4 data differential lanes plus 1 clock differential lane in synchronous mode, double data rate:

- 1.5 Gbps (750 MHz) @OPP_NOM for each lane.

The CSI-2 port B is compliant with the MIPI D-PHY RX specification v1.00.00 and the MIPI CSI-2 specification v1.00, with 2 data lanes plus 1 clock lane (differential) in synchronous mode, double data rate:

- 1.5 Gbps (750 MHz) @OPP_NOM for each lane, in synchronous mode.

7.10 External Memory Interface (EMIF)

The device has a dedicated interface to DDR3 and DDR3L SDRAM. It supports JEDEC standard compliant DDR3 and DDR3L SDRAM devices with the following features:

- 16-bit or 32-bit data path to external SDRAM memory
- Memory device capacity: 128Mb, 256Mb, 512Mb, 1Gb, 2Gb, 4Gb and 8Gb devices
- One interface with associated DDR3/DDR3L PHYs

NOTE

For more information, see *EMIF Controller* section in the device TRM.

7.11 General-Purpose Memory Controller (GPMC)

The GPMC is the unified memory controller that interfaces external memory devices such as:

- Asynchronous SRAM-like memories and ASIC devices
- Asynchronous page mode and synchronous burst NOR flash
- NAND flash

NOTE

For more information, see *General-Purpose Memory Controller* section in the device TRM.

7.11.1 GPMC/NOR Flash Interface Synchronous Timing

CAUTION

The I/O Timings provided in this section are valid only for some GPMC usage modes when the corresponding Virtual I/O Timings or Manual I/O Timings are configured as described in the tables found in this section.

Table 7-24 and Table 7-25 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 7-7, Figure 7-8, Figure 7-9, Figure 7-10, Figure 7-11 and Figure 7-12).

Table 7-24. GPMC/NOR Flash Interface Timing Requirements - Synchronous Mode - Default

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
F12	$t_{su(dV-clkH)}$	Setup time, read gpmc_ad[15:0] valid before gpmc_clk high	3		ns
F13	$t_{h(clkH-dV)}$	Hold time, read gpmc_ad[15:0] valid after gpmc_clk high	1.1		ns
F21	$t_{su(waitV-clkH)}$	Setup time, gpmc_wait[1:0] valid before gpmc_clk high	2.5		ns
F22	$t_{h(clkH-waitV)}$	Hold Time, gpmc_wait[1:0] valid after gpmc_clk high	1.3		ns

NOTE

Wait monitoring support is limited to a WaitMonitoringTime value > 0. For a full description of wait monitoring feature, see the Device TRM.

Table 7-25. GPMC/NOR Flash Interface Switching Characteristics - Synchronous Mode - Default

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
F0	$t_{c(clk)}$	Cycle time, output clock gpmc_clk period	11.3		ns
F2	$t_{d(clkH-nCSV)}$	Delay time, gpmc_clk rising edge to gpmc_cs[7:0] transition	F-1.7 (7)	F+4.3 (7)	ns
F3	$t_{d(clkH-nCSIV)}$	Delay time, gpmc_clk rising edge to gpmc_cs[7:0] invalid	E-1.7 (6)	E+4.2 (6)	ns
F4	$t_{d(ADDV-clk)}$	Delay time, gpmc_a[27:0] address bus valid to gpmc_clk first edge	B-1.8 (3)	B+4.3 (3)	ns
F5	$t_{d(clkH-ADDIV)}$	Delay time, gpmc_clk rising edge to gpmc_a[27:0] gpmc address bus invalid	-1.8		ns
F6	$t_{d(nBEV-clk)}$	Delay time, gpmc_ben[1:0] valid to gpmc_clk rising edge	B-4.3(3)	B+1.5(3)	ns
F7	$t_{d(clkH-nBEIV)}$	Delay time, gpmc_clk rising edge to gpmc_ben[1:0] invalid	D-1.5(5)	D+4.3(5)	ns
F8	$t_{d(clkH-nADV)}$	Delay time, gpmc_clk rising edge to gpmc_advn_ale transition	G-1.3 (8)	G+4.2 (8)	ns
F9	$t_{d(clkH-nADVIV)}$	Delay time, gpmc_clk rising edge to gpmc_advn_ale invalid	D-1.3 (5)	G+4.2 (5)	ns
F10	$t_{d(clkH-nOE)}$	Delay time, gpmc_clk rising edge to gpmc_oen_ren transition	H-1.0 (9)	H+3.2 (9)	ns
F11	$t_{d(clkH-nOEIV)}$	Delay time, gpmc_clk rising edge to gpmc_oen_ren invalid	E-1.0 (6)	E+3.2 (6)	ns
F14	$t_{d(clkH-nWE)}$	Delay time, gpmc_clk rising edge to gpmc_wen transition	I-0.9 (10)	I+4.2 (10)	ns
F15	$t_{d(clkH-Data)}$	Delay time, gpmc_clk rising edge to gpmc_ad[15:0] data bus transition	J-2.1 (11)	J+4.6 (11)	ns
F17	$t_{d(clkH-nBE)}$	Delay time, gpmc_clk rising edge to gpmc_ben[1:0] transition	J-1.5 (11)	J+4.3 (11)	ns
F18	$t_{w(nCSV)}$	Pulse duration, gpmc_cs[7:0] low	A (2)		ns
F19	$t_{w(nBEV)}$	Pulse duration, gpmc_ben[1:0] low	C (4)		ns
F20	$t_{w(nADVV)}$	Pulse duration, gpmc_advn_ale low	K (12)		ns
F23	$t_{d(CLK-GPIO)}$	Delay time, gpmc_clk transition to gpio6_16 transition (14)	0.5	7.5	ns

Table 7-26. GPMC/NOR Flash Interface Timing Requirements - Synchronous Mode - Alternate

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
F12	$t_{su(dV-clkH)}$	Setup time, read gpmc_ad[15:0] valid before gpmc_clk high	2.9		ns

Table 7-26. GPMC/NOR Flash Interface Timing Requirements - Synchronous Mode - Alternate (continued)

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
F13	$t_{h(clkH-dV)}$	Hold time, read gpmc_ad[15:0] valid after gpmc_clk high	2		ns
F21	$t_{su(waitV-clkH)}$	Setup time, gpmc_wait[1:0] valid before gpmc_clk high	2.5		ns
F22	$t_{h(clkH-waitV)}$	Hold Time, gpmc_wait[1:0] valid after gpmc_clk high	2.1		ns

Table 7-27. GPMC/NOR Flash Interface Switching Characteristics - Synchronous Mode - Alternate

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
F0	$t_{c(clk)}$	Cycle time, output clock gpmc_clk period (13)	15.04		ns
F2	$t_{d(clkH-nCSV)}$	Delay time, gpmc_clk rising edge to gpmc_cs[7:0] transition	F+0.6 (7)	F+7.0 (7)	ns
F3	$t_{d(clkH-nCSIV)}$	Delay time, gpmc_clk rising edge to gpmc_cs[7:0] invalid	E+0.6 (6)	E+7.0 (6)	ns
F4	$t_{d(ADDV-clk)}$	Delay time, gpmc_a[27:0] address bus valid to gpmc_clk first edge	B-0.7 (3)	B+7.0 (3)	ns
F5	$t_{d(clkH-ADDIV)}$	Delay time, gpmc_clk rising edge to gpmc_a[27:0] gpmc address bus invalid	-0.7		ns
F6	$t_{d(nBEV-clk)}$	Delay time, gpmc_ben[1:0] valid to gpmc_clk rising edge	B-7.0	B+0.4	ns
F7	$t_{d(clkH-nBEIV)}$	Delay time, gpmc_clk rising edge to gpmc_ben[1:0] invalid	D-0.4	D+7.0	ns
F8	$t_{d(clkH-nADV)}$	Delay time, gpmc_clk rising edge to gpmc_advn_ale transition	G+0.7 (8)	G+6.1 (8)	ns
F9	$t_{d(clkH-nADVIV)}$	Delay time, gpmc_clk rising edge to gpmc_advn_ale invalid	D+0.7 (5)	D+6.1 (5)	ns
F10	$t_{d(clkH-nOE)}$	Delay time, gpmc_clk rising edge to gpmc_oen_ren transition	H+0.7 (9)	H+5.1 (9)	ns
F11	$t_{d(clkH-nOEIV)}$	Delay time, gpmc_clk rising edge to gpmc_oen_ren invalid	E+0.7 (6)	E+5.1 (6)	ns
F14	$t_{d(clkH-nWE)}$	Delay time, gpmc_clk rising edge to gpmc_wen transition	I+0.7 (10)	I+6.1 (10)	ns
F15	$t_{d(clkH-Data)}$	Delay time, gpmc_clk rising edge to gpmc_ad[15:0] data bus transition	J-0.4 (11)	J+4.9 (11)	ns
F17	$t_{d(clkH-nBE)}$	Delay time, gpmc_clk rising edge to gpmc_ben[1:0] transition	J-0.4 (11)	J+4.9 (11)	ns
F18	$t_{w(nCSV)}$	Pulse duration, gpmc_cs[7:0] low	A (2)		ns
F19	$t_{w(nBEV)}$	Pulse duration, gpmc_ben[1:0] low	C (4)		ns
F20	$t_{w(nADVV)}$	Pulse duration, gpmc_advn_ale low	K (12)		ns
F23	$t_{d(CLK-GPIO)}$	Delay time, gpmc_clk transition to gpio6_16.clkout1 transition (14)	0.5	7.5	ns

(1) Total GPMC load on any signal at 3.3V must not exceed 10pF.

(2) For single read: A = (CSRdOffTime - CSOnTime) * (TimeParaGranularity + 1) * GPMC_FCLK period
For burst read: A = (CSRdOffTime - CSOnTime + (n - 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK period
For burst write: A = (CSWrOffTime - CSOnTime + (n - 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK period
with n the page burst access number.

(3) B = ClkActivationTime * GPMC_FCLK

(4) For single read: C = RdCycleTime * (TimeParaGranularity + 1) * GPMC_FCLK
For burst read: C = (RdCycleTime + (n - 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK
For Burst write: C = (WrCycleTime + (n - 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK with n the page burst access number.

(5) For single read: D = (RdCycleTime - AccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK
For burst read: D = (RdCycleTime - AccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK
For burst write: D = (WrCycleTime - AccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK

(6) For single read: E = (CSRdOffTime - AccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK
For burst read: E = (CSRdOffTime - AccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK
For burst write: E = (CSWrOffTime - AccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK

(7) For nCS falling edge (CS activated):
Case GpmcFCLKDivider = 0 :
F = 0.5 * CSExtraDelay * GPMC_FCLK
Case GpmcFCLKDivider = 1:
F = 0.5 * CSExtraDelay * GPMC_FCLK if (ClkActivationTime and CSOnTime are odd) or (ClkActivationTime and CSOnTime are even)
F = (1 + 0.5 * CSExtraDelay) * GPMC_FCLK otherwise
Case GpmcFCLKDivider = 2:
F = 0.5 * CSExtraDelay * GPMC_FCLK if ((CSOnTime - ClkActivationTime) is a multiple of 3)
F = (1 + 0.5 * CSExtraDelay) * GPMC_FCLK if ((CSOnTime - ClkActivationTime - 1) is a multiple of 3)
F = (2 + 0.5 * CSExtraDelay) * GPMC_FCLK if ((CSOnTime - ClkActivationTime - 2) is a multiple of 3)
Case GpmcFCLKDivider = 3:
F = 0.5 * CSExtraDelay * GPMC_FCLK if ((CSOnTime - ClkActivationTime) is a multiple of 4)
F = (1 + 0.5 * CSExtraDelay) * GPMC_FCLK if ((CSOnTime - ClkActivationTime - 1) is a multiple of 4)

F = (2 + 0.5 * CSExtraDelay) * GPMC_FCLK if ((CSOnTime - ClkActivationTime - 2) is a multiple of 4)
F = (3 + 0.5 * CSExtraDelay) * GPMC_FCLK if ((CSOnTime - ClkActivationTime - 3) is a multiple of 4)

(8) For ADV falling edge (ADV activated):
Case GpmcFCLKDivider = 0 :
G = 0.5 * ADVExtraDelay * GPMC_FCLK
Case GpmcFCLKDivider = 1:
G = 0.5 * ADVExtraDelay * GPMC_FCLK if (ClkActivationTime and ADVOnTime are odd) or (ClkActivationTime and ADVOnTime are even)
G = (1 + 0.5 * ADVExtraDelay) * GPMC_FCLK otherwise
Case GpmcFCLKDivider = 2:
G = 0.5 * ADVExtraDelay * GPMC_FCLK if ((ADVOnTime - ClkActivationTime) is a multiple of 3)
G = (1 + 0.5 * ADVExtraDelay) * GPMC_FCLK if ((ADVOnTime - ClkActivationTime - 1) is a multiple of 3)
G = (2 + 0.5 * ADVExtraDelay) * GPMC_FCLK if ((ADVOnTime - ClkActivationTime - 2) is a multiple of 3)
For ADV rising edge (ADV desactivated) in Reading mode:
Case GpmcFCLKDivider = 0:
G = 0.5 * ADVExtraDelay * GPMC_FCLK
Case GpmcFCLKDivider = 1:
G = 0.5 * ADVExtraDelay * GPMC_FCLK if (ClkActivationTime and ADVRdOffTime are odd) or (ClkActivationTime and ADVRdOffTime are even)
G = (1 + 0.5 * ADVExtraDelay) * GPMC_FCLK otherwise
Case GpmcFCLKDivider = 2:
G = 0.5 * ADVExtraDelay * GPMC_FCLK if ((ADVRdOffTime - ClkActivationTime) is a multiple of 3)
G = (1 + 0.5 * ADVExtraDelay) * GPMC_FCLK if ((ADVRdOffTime - ClkActivationTime - 1) is a multiple of 3)
G = (2 + 0.5 * ADVExtraDelay) * GPMC_FCLK if ((ADVRdOffTime - ClkActivationTime - 2) is a multiple of 3)
Case GpmcFCLKDivider = 3:
G = 0.5 * ADVExtraDelay * GPMC_FCLK if ((ADVRdOffTime - ClkActivationTime) is a multiple of 4)
G = (1 + 0.5 * ADVExtraDelay) * GPMC_FCLK if ((ADVRdOffTime - ClkActivationTime - 1) is a multiple of 4)
G = (2 + 0.5 * ADVExtraDelay) * GPMC_FCLK if ((ADVRdOffTime - ClkActivationTime - 2) is a multiple of 4)
G = (3 + 0.5 * ADVExtraDelay) * GPMC_FCLK if ((ADVRdOffTime - ClkActivationTime - 3) is a multiple of 4)
For ADV rising edge (ADV desactivated) in Writing mode:
Case GpmcFCLKDivider = 0:
G = 0.5 * ADVExtraDelay * GPMC_FCLK
Case GpmcFCLKDivider = 1:
G = 0.5 * ADVExtraDelay * GPMC_FCLK if (ClkActivationTime and ADVWrOffTime are odd) or (ClkActivationTime and ADVWrOffTime are even)
G = (1 + 0.5 * ADVExtraDelay) * GPMC_FCLK otherwise
Case GpmcFCLKDivider = 2:
G = 0.5 * ADVExtraDelay * GPMC_FCLK if ((ADVWrOffTime - ClkActivationTime) is a multiple of 3)
G = (1 + 0.5 * ADVExtraDelay) * GPMC_FCLK if ((ADVWrOffTime - ClkActivationTime - 1) is a multiple of 3)
G = (2 + 0.5 * ADVExtraDelay) * GPMC_FCLK if ((ADVWrOffTime - ClkActivationTime - 2) is a multiple of 3)
Case GpmcFCLKDivider = 3:
G = 0.5 * ADVExtraDelay * GPMC_FCLK if ((ADVWrOffTime - ClkActivationTime) is a multiple of 4)
G = (1 + 0.5 * ADVExtraDelay) * GPMC_FCLK if ((ADVWrOffTime - ClkActivationTime - 1) is a multiple of 4)
G = (2 + 0.5 * ADVExtraDelay) * GPMC_FCLK if ((ADVWrOffTime - ClkActivationTime - 2) is a multiple of 4)
G = (3 + 0.5 * ADVExtraDelay) * GPMC_FCLK if ((ADVWrOffTime - ClkActivationTime - 3) is a multiple of 4)

(9) For OE falling edge (OE activated):
Case GpmcFCLKDivider = 0:
- H = 0.5 * OEExtraDelay * GPMC_FCLK
Case GpmcFCLKDivider = 1:
- H = 0.5 * OEExtraDelay * GPMC_FCLK if (ClkActivationTime and OEOnTime are odd) or (ClkActivationTime and OEOnTime are even)
- H = (1 + 0.5 * OEExtraDelay) * GPMC_FCLK otherwise
Case GpmcFCLKDivider = 2:
- H = 0.5 * OEExtraDelay * GPMC_FCLK if ((OEOnTime - ClkActivationTime) is a multiple of 3)
- H = (1 + 0.5 * OEExtraDelay) * GPMC_FCLK if ((OEOnTime - ClkActivationTime - 1) is a multiple of 3)
- H = (2 + 0.5 * OEExtraDelay) * GPMC_FCLK if ((OEOnTime - ClkActivationTime - 2) is a multiple of 3)
Case GpmcFCLKDivider = 3:
- H = 0.5 * OEExtraDelay * GPMC_FCLK if ((OEOnTime - ClkActivationTime) is a multiple of 4)
- H = (1 + 0.5 * OEExtraDelay) * GPMC_FCLK if ((OEOnTime - ClkActivationTime - 1) is a multiple of 4)
- H = (2 + 0.5 * OEExtraDelay) * GPMC_FCLK if ((OEOnTime - ClkActivationTime - 2) is a multiple of 4)
- H = (3 + 0.5 * OEExtraDelay)) * GPMC_FCLK if ((OEOnTime - ClkActivationTime - 3) is a multiple of 4)
For OE rising edge (OE desactivated):
Case GpmcFCLKDivider = 0:
- H = 0.5 * OEExtraDelay * GPMC_FCLK
Case GpmcFCLKDivider = 1:
- H = 0.5 * OEExtraDelay * GPMC_FCLK if (ClkActivationTime and OEOffTime are odd) or (ClkActivationTime and OEOffTime are even)
- H = (1 + 0.5 * OEExtraDelay) * GPMC_FCLK otherwise
Case GpmcFCLKDivider = 2:
- H = 0.5 * OEExtraDelay * GPMC_FCLK if ((OEOffTime - ClkActivationTime) is a multiple of 3)
- H = (1 + 0.5 * OEExtraDelay) * GPMC_FCLK if ((OEOffTime - ClkActivationTime - 1) is a multiple of 3)
- H = (2 + 0.5 * OEExtraDelay) * GPMC_FCLK if ((OEOffTime - ClkActivationTime - 2) is a multiple of 3)
Case GpmcFCLKDivider = 3:
- H = 0.5 * OEExtraDelay * GPMC_FCLK if ((OEOffTime - ClkActivationTime) is a multiple of 4)

- H = (1 + 0.5 * OEExtraDelay) * GPMC_FCLK if ((OEOffTime - ClkActivationTime - 1) is a multiple of 4)
- H = (2 + 0.5 * OEExtraDelay) * GPMC_FCLK if ((OEOffTime - ClkActivationTime - 2) is a multiple of 4)
- H = (3 + 0.5 * OEExtraDelay) * GPMC_FCLK if ((OEOffTime - ClkActivationTime - 3) is a multiple of 4)

(10) For WE falling edge (WE activated):
Case GpmcFCLKDivider = 0:
- I = 0.5 * WEExtraDelay * GPMC_FCLK
Case GpmcFCLKDivider = 1:
- I = 0.5 * WEExtraDelay * GPMC_FCLK if (ClkActivationTime and WEOnTime are odd) or (ClkActivationTime and WEOnTime are even)
- I = (1 + 0.5 * WEExtraDelay) * GPMC_FCLK otherwise
Case GpmcFCLKDivider = 2:
- I = 0.5 * WEExtraDelay * GPMC_FCLK if ((WEOnTime - ClkActivationTime) is a multiple of 3)
- I = (1 + 0.5 * WEExtraDelay) * GPMC_FCLK if ((WEOnTime - ClkActivationTime - 1) is a multiple of 3)
- I = (2 + 0.5 * WEExtraDelay) * GPMC_FCLK if ((WEOnTime - ClkActivationTime - 2) is a multiple of 3)
Case GpmcFCLKDivider = 3:
- I = 0.5 * WEExtraDelay * GPMC_FCLK if ((WEOnTime - ClkActivationTime) is a multiple of 4)
- I = (1 + 0.5 * WEExtraDelay) * GPMC_FCLK if ((WEOnTime - ClkActivationTime - 1) is a multiple of 4)
- I = (2 + 0.5 * WEExtraDelay) * GPMC_FCLK if ((WEOnTime - ClkActivationTime - 2) is a multiple of 4)
- I = (3 + 0.5 * WEExtraDelay) * GPMC_FCLK if ((WEOnTime - ClkActivationTime - 3) is a multiple of 4)
For WE rising edge (WE desactivated):
Case GpmcFCLKDivider = 0:
- I = 0.5 * WEExtraDelay * GPMC_FCLK
Case GpmcFCLKDivider = 1:
- I = 0.5 * WEExtraDelay * GPMC_FCLK if (ClkActivationTime and WEOffTime are odd) or (ClkActivationTime and WEOffTime are even)
- I = (1 + 0.5 * WEExtraDelay) * GPMC_FCLK otherwise
Case GpmcFCLKDivider = 2:
- I = 0.5 * WEExtraDelay * GPMC_FCLK if ((WEOffTime - ClkActivationTime) is a multiple of 3)
- I = (1 + 0.5 * WEExtraDelay) * GPMC_FCLK if ((WEOffTime - ClkActivationTime - 1) is a multiple of 3)
- I = (2 + 0.5 * WEExtraDelay) * GPMC_FCLK if ((WEOffTime - ClkActivationTime - 2) is a multiple of 3)
Case GpmcFCLKDivider = 3:
- I = 0.5 * WEExtraDelay * GPMC_FCLK if ((WEOffTime - ClkActivationTime) is a multiple of 4)
- I = (1 + 0.5 * WEExtraDelay) * GPMC_FCLK if ((WEOffTime - ClkActivationTime - 1) is a multiple of 4)
- I = (2 + 0.5 * WEExtraDelay) * GPMC_FCLK if ((WEOffTime - ClkActivationTime - 2) is a multiple of 4)
- I = (3 + 0.5 * WEExtraDelay) * GPMC_FCLK if ((WEOffTime - ClkActivationTime - 3) is a multiple of 4)

(11) J = GPMC_FCLK period, where GPMC_FCLK is the General Purpose Memory Controller internal functional clock

(12) For read:
K = (ADVRdOffTime - ADVOnTime) * (TimeParaGranularity + 1) * GPMC_FCLK
For write: K = (ADVWrOffTime - ADVOnTime) * (TimeParaGranularity + 1) * GPMC_FCLK

(13) The gpmc_clk output clock maximum and minimum frequency is programmable in the I/F module by setting the GPMC_CONFIG1_CSx configuration register bit fields GpmcFCLKDivider

(14) gpio6_16 programmed to MUXMODE=9 (clkout1), CM_CLKSEL_CLKOUTMUX1 programmed to 7 (CORE_DPLL_OUT_DCLK), CM_CLKSEL_CORE_DPLL_OUT_CLK_CLKOUTMUX programmed to 1.

(15) CSEXTRADELAY = 0, ADVEXTRADELAY = 0, WEEXTRADELAY = 0, OEEXTRADELAY = 0. Extra half-GPMC_FCLK cycle delay mode is not timed.

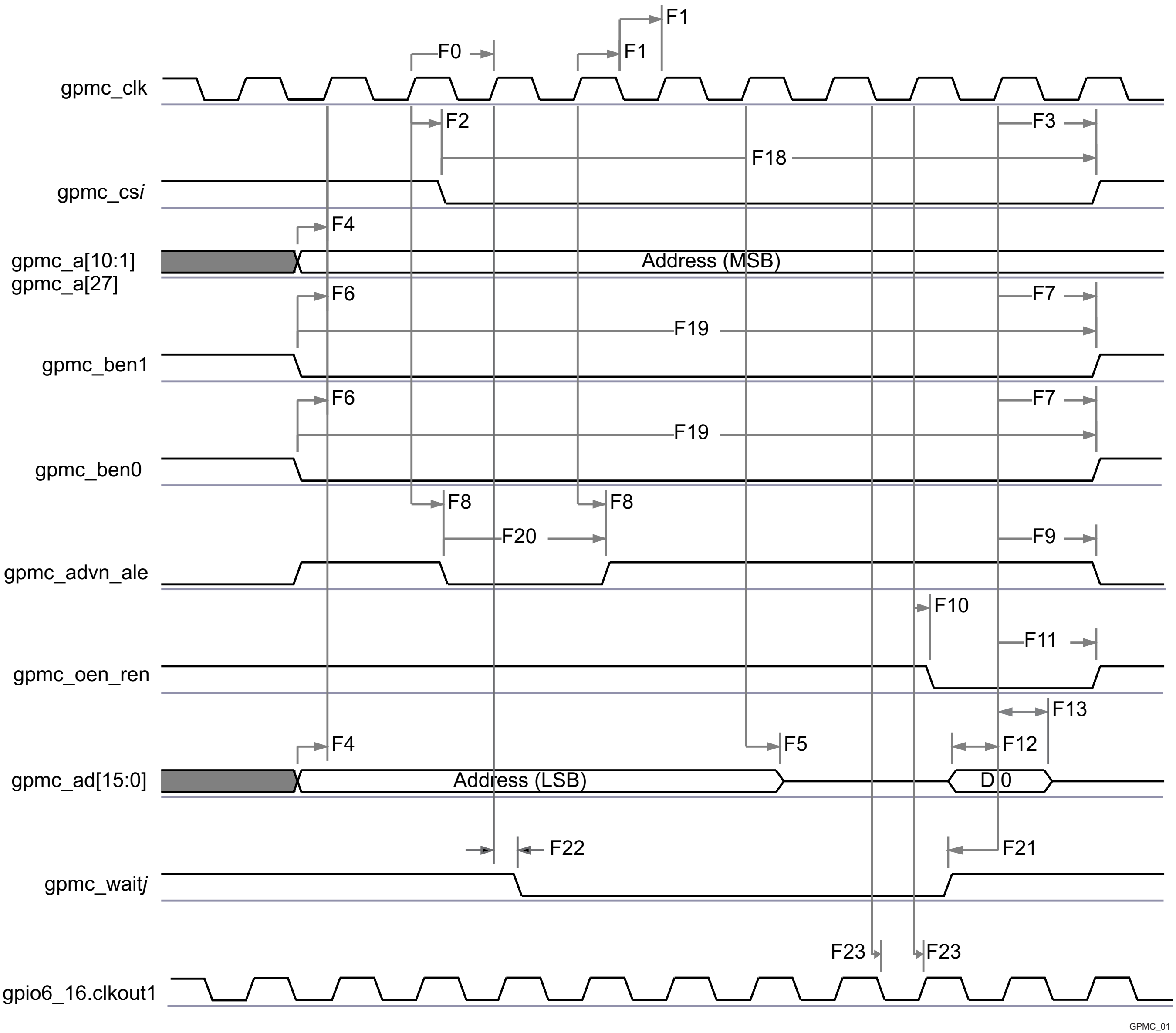


Figure 7-7. GPMC / Multiplexed 16bits NOR Flash - Synchronous Single Read - (GpmcFCLKDivider = 0)[(1)(2)]

(1) In gpmc_csi, i = 0 to 7.

(2) In gpmc_waitj, j = 0 to 1.

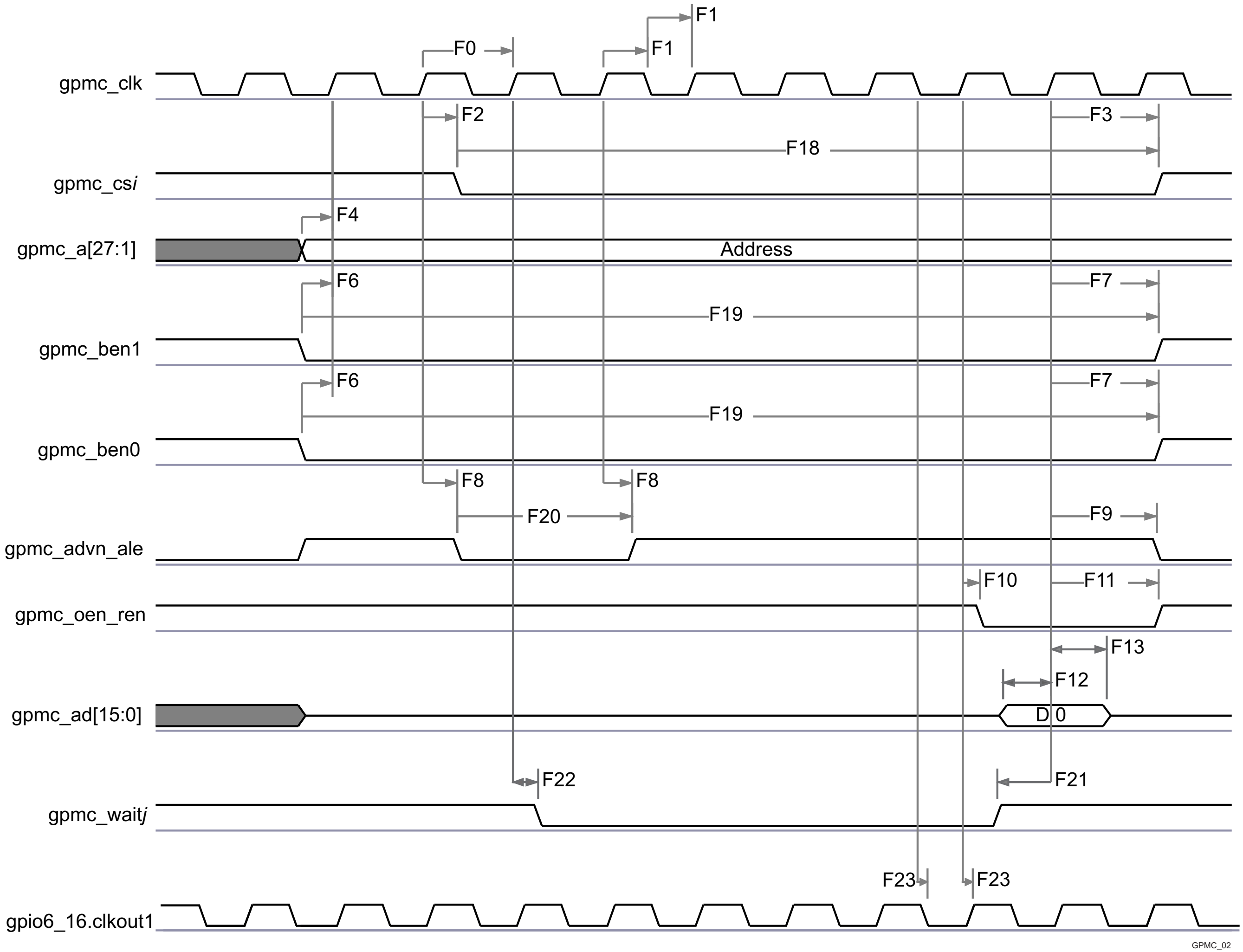


Figure 7-8. GPMC / Nonmultiplexed 16bits NOR Flash - Synchronous Single Read - (GpmcFCLKDivider = 0)[(1)(2)]

(1) In gpmc_cs*i*, i = 0 to 7.

(2) In gpmc_waitj, j = 0 to 1.

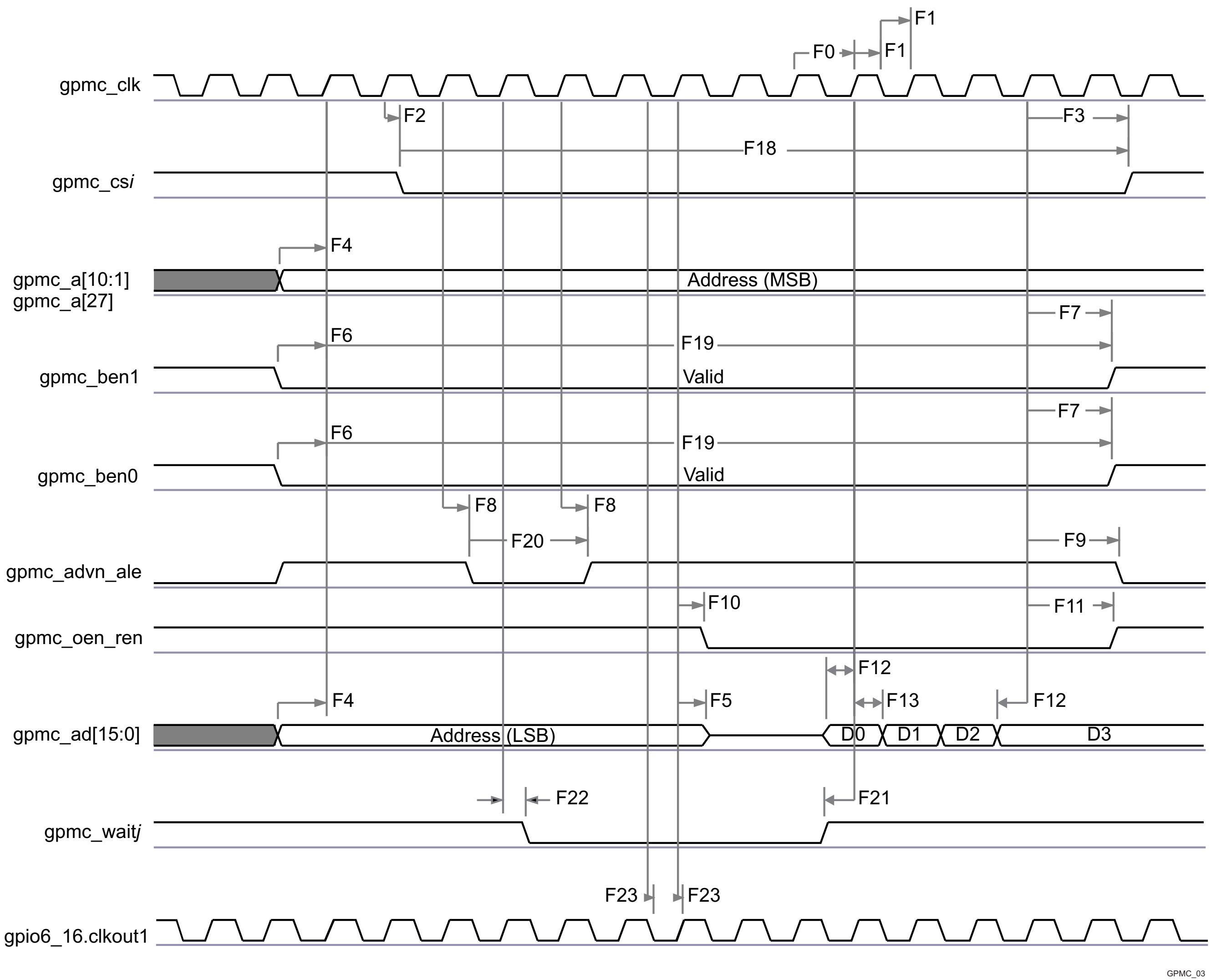


Figure 7-9. GPMC / Multiplexed 16bits NOR Flash - Synchronous Burst Read 4x16 bits - (GpmcFCLKDivider = 0)[(1)(2)]

(1) In gpmc_cs*i*, i= 0 to 7.

(2) In gpmc_waitj, j = 0 to 1.

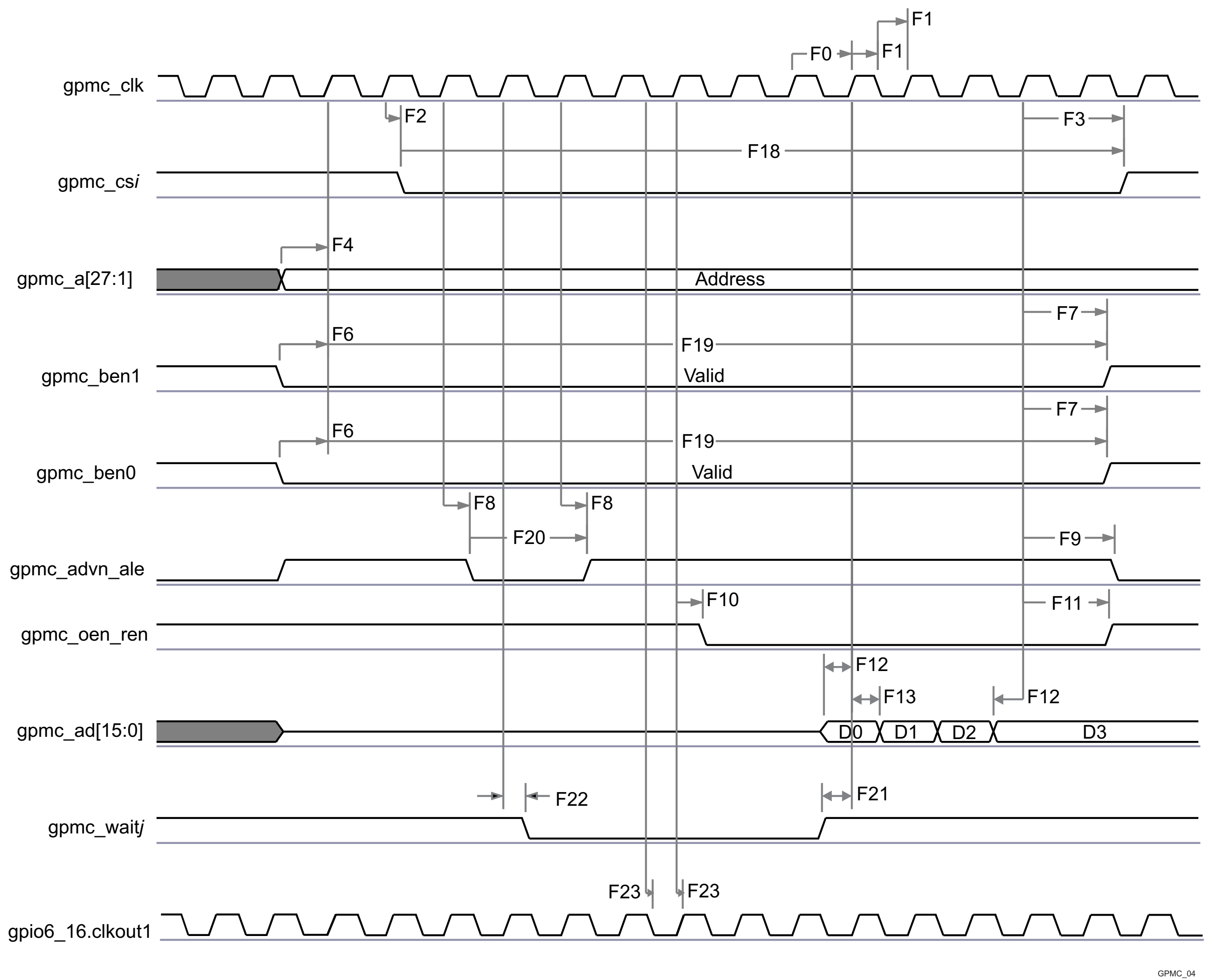


Figure 7-10. GPMC / Nonmultiplexed 16bits NOR Flash - Synchronous Burst Read 4x16 bits - (GpmcFCLKDivider = 0)(1)(2)

(1) In gpmc_cs*i*, i = 0 to 7.

(2) In gpmc_waitj, j = 0 to 1.

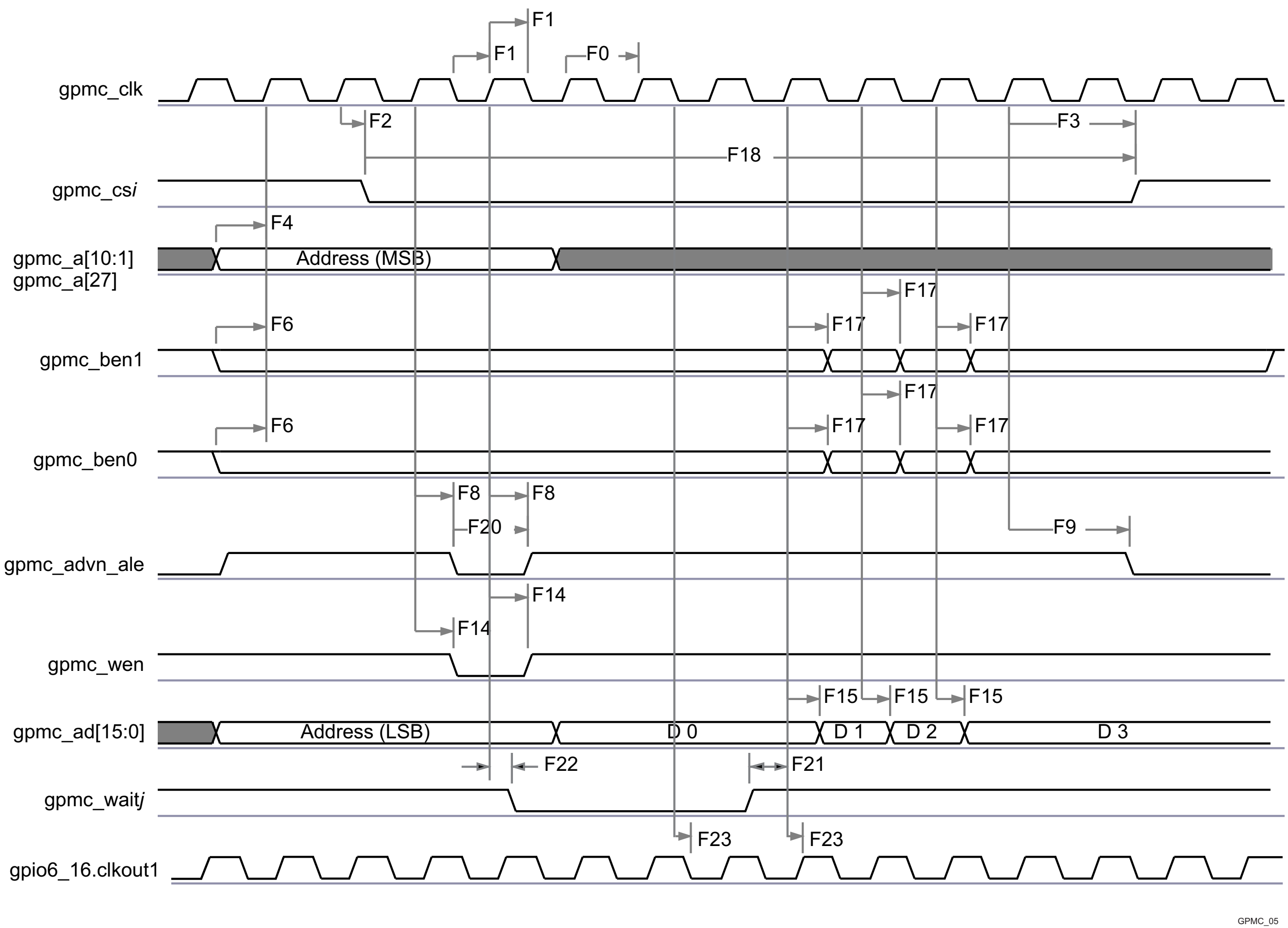


Figure 7-11. GPMC / Multiplexed 16bits NOR Flash - Synchronous Burst Write 4x16bits - (GpmcFCLKDivider = 0)(1)(2)

(1) In “gpmc_csi”, i = 0 to 7.

(2) In “gpmc_waitj”, j = 0 to 1.

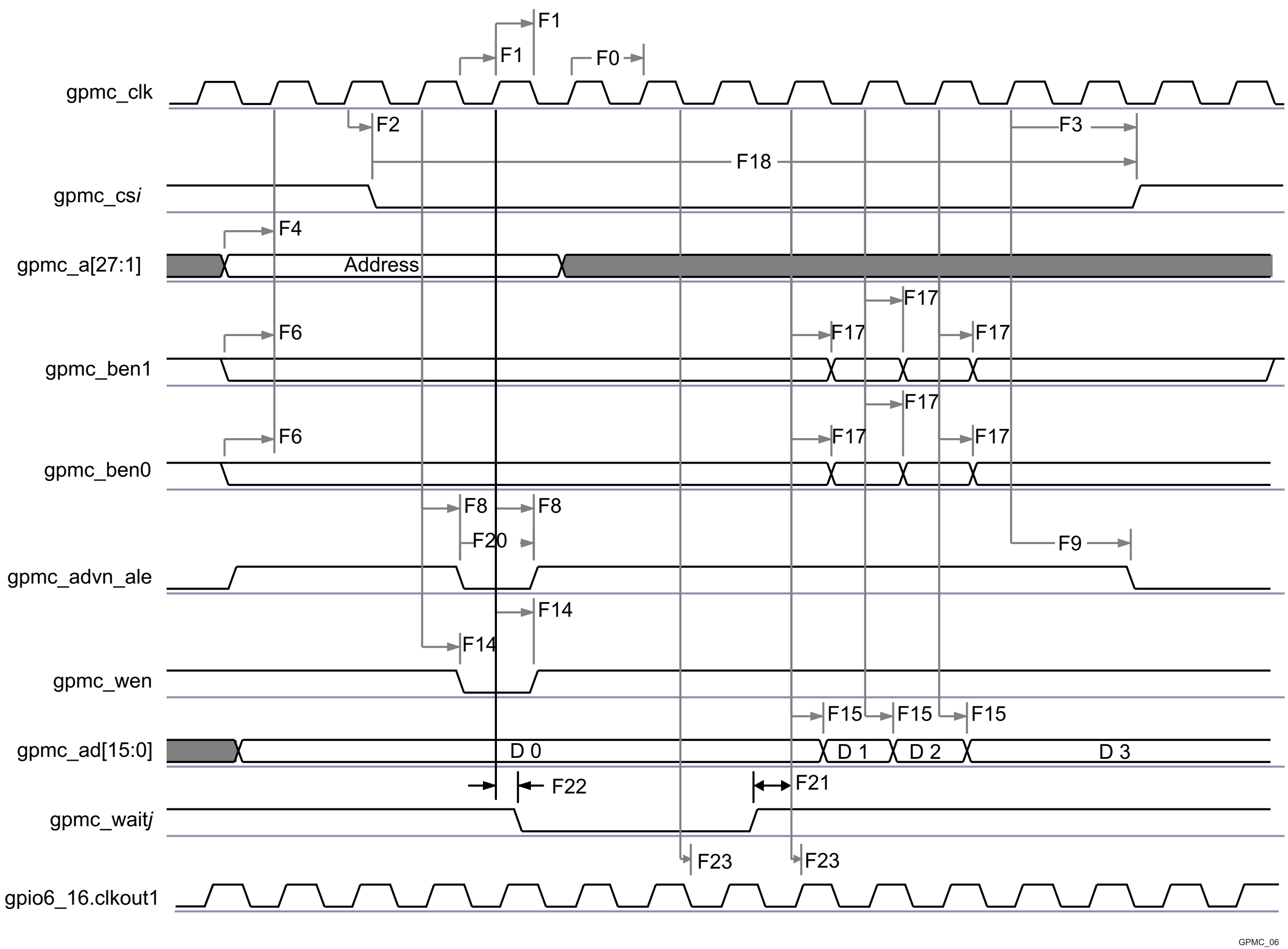


Figure 7-12. GPMC / Nonmultiplexed 16bits NOR Flash - Synchronous Burst Write 4x16bits - (GpmcFCLKDivider = 0)[(1)(2)]

(1) In “gpmc_csi”, i = 1 to 7.

(2) In “gpmc_waitj”, j = 0 to 1.

7.11.2 GPMC/NOR Flash Interface Asynchronous Timing

CAUTION

The I/O Timings provided in this section are valid only for some GPMC usage modes when the corresponding Virtual I/O Timings or Manual I/O Timings are configured as described in the tables found in this section.

Table 7-28 and Table 7-29 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 7-13, Figure 7-14, Figure 7-15, Figure 7-16, Figure 7-17 and Figure 7-18).

Table 7-28. GPMC/NOR Flash Interface Timing Requirements - Asynchronous Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
FA5	$t_{acc(DAT)}$	Data Maximum Access Time (GPMC_FCLK cycles)		H [(1)]	cycles

Table 7-28. GPMC/NOR Flash Interface Timing Requirements - Asynchronous Mode (continued)

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
FA20	$t_{acc1-pgmode(DAT)}$	Page Mode Successive Data Maximum Access Time (GPMC_FCLK cycles)		P (2)	cycles
FA21	$t_{acc2-pgmode(DAT)}$	Page Mode First Data Maximum Access Time (GPMC_FCLK cycles)		H (1)	cycles
-	$t_{su(DV-OEH)}$	Setup time, read gpmc_ad[15:0] valid before gpmc_oen_ren high	1.9		ns
-	$t_{h(OEH-DV)}$	Hold time, read gpmc_ad[15:0] valid after gpmc_oen_ren high	1		ns

(1) H = Access Time * (TimeParaGranularity + 1)

(2) P = PageBurstAccessTime * (TimeParaGranularity + 1)

Table 7-29. GPMC/NOR Flash Interface Switching Characteristics - Asynchronous Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
-	$t_{r(DO)}$	Rising time, gpmc_ad[15:0] output data	0.447	4.067	ns
-	$t_{f(DO)}$	Fallling time, gpmc_ad[15:0] output data	0.43	4.463	ns
FA0	$t_{w(nBEV)}$	Pulse duration, gpmc_ben[1:0] valid time		N (1)	ns
FA1	$t_{w(nCSV)}$	Pulse duration, gpmc_cs[7:0] low		A (2)	ns
FA3	$t_{d(nCSV-nADVIV)}$	Delay time, gpmc_cs[7:0] valid to gpmc_advn_ale invalid	B - 2 (3)	B + 4 (3)	ns
FA4	$t_{d(nCSV-nOEIV)}$	Delay time, gpmc_cs[7:0] valid to gpmc_oen_ren invalid (Single read)	C - 2 (4)	C + 4 (4)	ns
FA9	$t_{d(AV-nCSV)}$	Delay time, address bus valid to gpmc_cs[7:0] valid	J - 2 (5)	J + 4 (5)	ns
FA10	$t_{d(nBEV-nCSV)}$	Delay time, gpmc_ben[1:0] valid to gpmc_cs[7:0] valid	J - 2 (5)	J + 4 (5)	ns
FA12	$t_{d(nCSV-nADVV)}$	Delay time, gpmc_cs[7:0] valid to gpmc_advn_ale valid	K - 2 (6)	K + 4 (6)	ns
FA13	$t_{d(nCSV-nOEV)}$	Delay time, gpmc_cs[7:0] valid to gpmc_oen_ren valid	L - 2 (7)	L + 4 (7)	ns
FA16	$t_{w(AIV)}$	Pulse duration, address invalid between 2 successive R/W accesses	G (8)		ns
FA18	$t_{d(nCSV-nOEIV)}$	Delay time, gpmc_cs[7:0] valid to gpmc_oen_ren invalid (Burst read)	I - 2 (9)	I + 4 (9)	ns
FA20	$t_{w(AV)}$	Pulse duration, address valid : 2nd, 3rd and 4th accesses	D (10)		ns
FA25	$t_{d(nCSV-nWEV)}$	Delay time, gpmc_cs[7:0] valid to gpmc_wen valid	E - 2 (11)	E + 4 (11)	ns
FA27	$t_{d(nCSV-nWEIV)}$	Delay time, gpmc_cs[7:0] valid to gpmc_wen invalid	F - 2 (12)	F + 4 (12)	ns
FA28	$t_{d(nWEV-DV)}$	Delay time, gpmc_ wen valid to data bus valid		2	ns
FA29	$t_{d(DV-nCSV)}$	Delay time, data bus valid to gpmc_cs[7:0] valid	J - 2 (5)	J + 4 (5)	ns
FA37	$t_{d(nOEV-AIV)}$	Delay time, gpmc_oen_ren valid to gpmc_ad[15:0] multiplexed address bus phase end		2	ns

(1) For single read: N = RdCycleTime * (TimeParaGranularity + 1) * GPMC_FCLK
For single write: N = WrCycleTime * (TimeParaGranularity + 1) * GPMC_FCLK
For burst read: N = (RdCycleTime + (n - 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK
For burst write: N = (WrCycleTime + (n - 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK

(2) For single read: A = (CSRdOffTime - CSOnTime) * (TimeParaGranularity + 1) * GPMC_FCLK
For single write: A = (CSWrOffTime - CSOnTime) * (TimeParaGranularity + 1) * GPMC_FCLK
For burst read: A = (CSRdOffTime - CSOnTime + (n - 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK
For burst write: A = (CSWrOffTime - CSOnTime + (n - 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK

(3) For reading: B = ((ADVRdOffTime - CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (ADVExtraDelay - CSExtraDelay)) * GPMC_FCLK
For writing: B = ((ADVWrOffTime - CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (ADVExtraDelay - CSExtraDelay)) * GPMC_FCLK

(4) C = ((OEOffTime - CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (OEExtraDelay - CSExtraDelay)) * GPMC_FCLK

(5) J = (CSOnTime * (TimeParaGranularity + 1) + 0.5 * CSExtraDelay) * GPMC_FCLK

(6) K = ((ADVOnTime - CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (ADVExtraDelay - CSExtraDelay)) * GPMC_FCLK

(7) L = ((OEOnTime - CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (OEExtraDelay - CSExtraDelay)) * GPMC_FCLK

(8) G = Cycle2CycleDelay * GPMC_FCLK * (TimeParaGranularity +1)

(9) I = ((OEOffTime + (n - 1) * PageBurstAccessTime - CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (OEExtraDelay - CSExtraDelay)) * GPMC_FCLK

(10) D = PageBurstAccessTime * (TimeParaGranularity + 1) * GPMC_FCLK

(11) E = ((WEOnTime - CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (WEExtraDelay - CSExtraDelay)) * GPMC_FCLK

(12) F = ((WEOffTime - CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (WEExtraDelay - CSExtraDelay)) * GPMC_FCLK

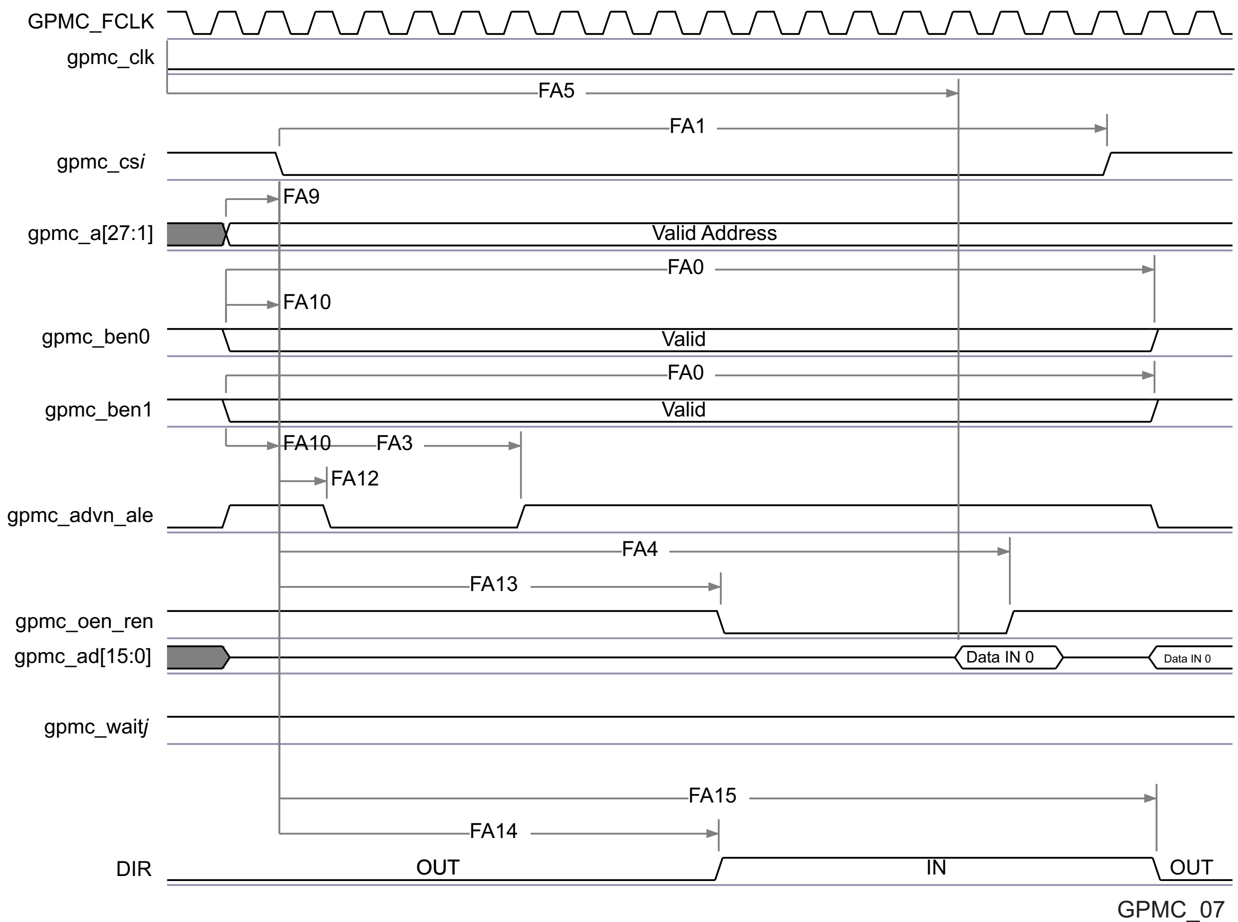


Figure 7-13. GPMC / NOR Flash - Asynchronous Read - Single Word Timing(1)(2)(3)

(1) In gpmc_cs*i*, i = 0 to 7. In gpmc_waitj, j = 0 to 1.

(2) FA5 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input Data will be internally sampled by active functional clock edge. FA5 value must be stored inside AccessTime register bits field.

(3) GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.

(4) The "DIR" (direction control) output signal is NOT pinned out on any of the device pads. It is an internal signal only representing a signal direction on the GPMC data bus.

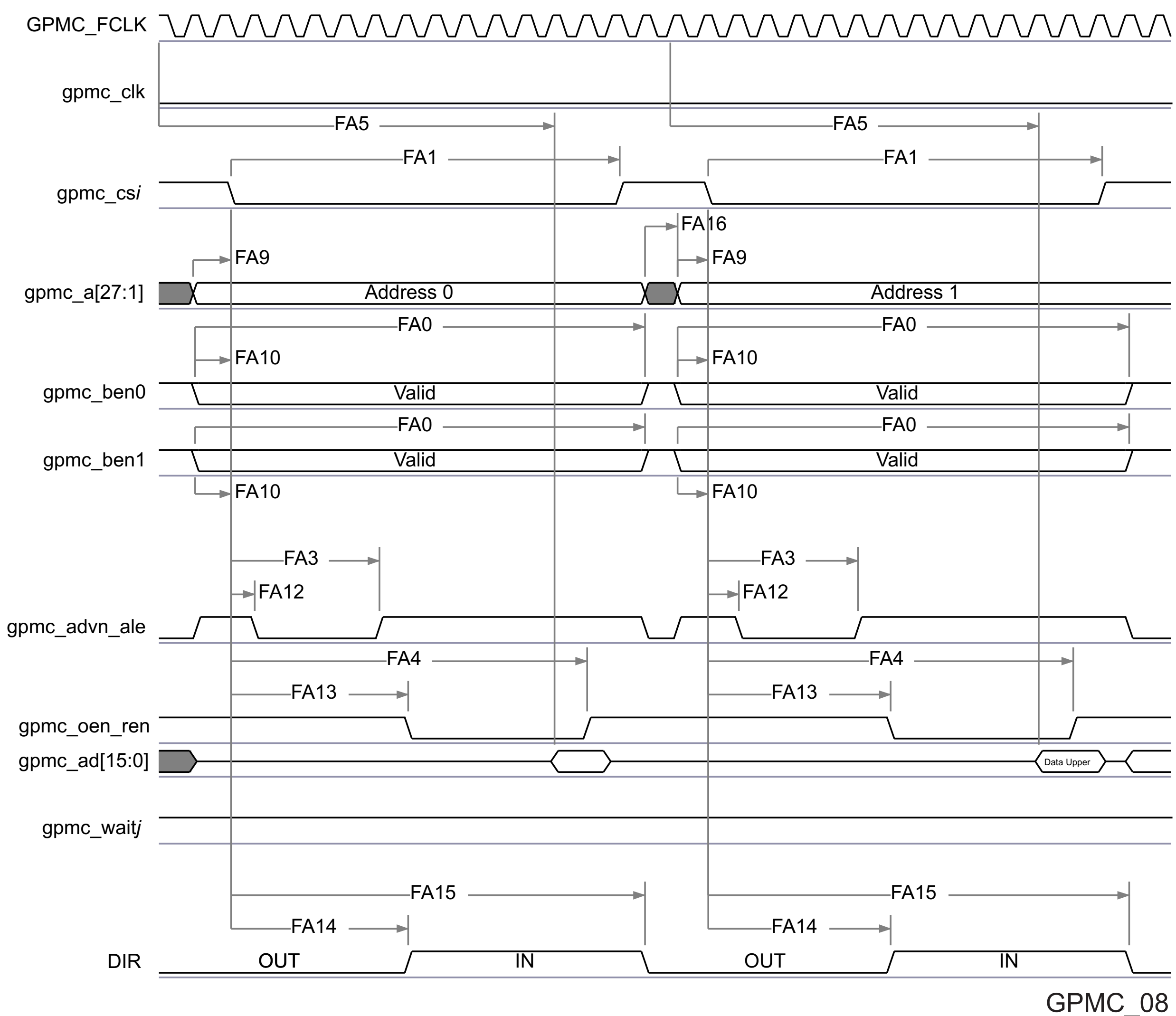


Figure 7-14. GPMC / NOR Flash - Asynchronous Read - 32-bit Timing(1)(2)(3)

(1) In "gpmc_csi", i = 0 to 7. In "gpmc_waitj", j = 0 to 1.

(2) FA5 parameter illustrates amount of time required to internally sample input Data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input Data will be internally sampled by active functional clock edge. FA5 value should be stored inside AccessTime register bits field

(3) GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally

(4) The "DIR" (direction control) output signal is NOT pinned out on any of the device pads. It is an internal signal only representing a signal direction on the GPMC data bus.

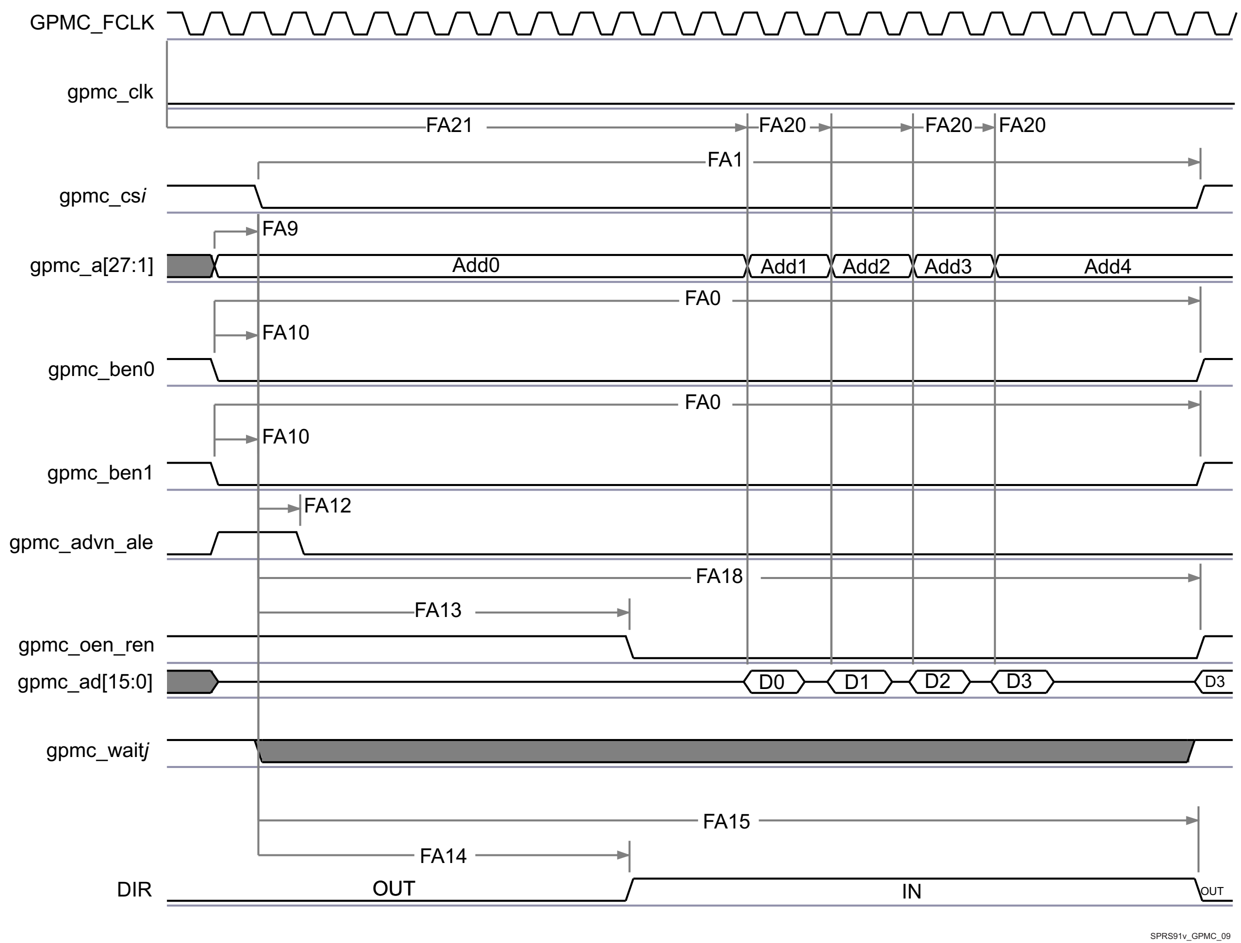


Figure 7-15. GPMC / NOR Flash - Asynchronous Read - Page Mode 4x16-bit Timing(1)(2)(3)(4)

(1) In “gpmc_csi”, i = 0 to 7. In “gpmc_waitj”, j = 0 to 1

(2) FA21 parameter illustrates amount of time required to internally sample first input Page Data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA21 functional clock cycles, First input Page Data will be internally sampled by active functional clock edge. FA21 calculation is detailled in a separated application note and should be stored inside AccessTime register bits field.

(3) FA20 parameter illustrates amount of time required to internally sample successive input Page Data. It is expressed in number of GPMC functional clock cycles. After each access to input Page Data, next input Page Data will be internally sampled by active functional clock edge after FA20 functional clock cycles. FA20 is also the duration of address phases for successive input Page Data (excluding first input Page Data). FA20 value should be stored in PageBurstAccessTime register bits field.

(4) GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally

(5) The "DIR" (direction control) output signal is NOT pinned out on any of the device pads. It is an internal signal only representing a signal direction on the GPMC data bus.

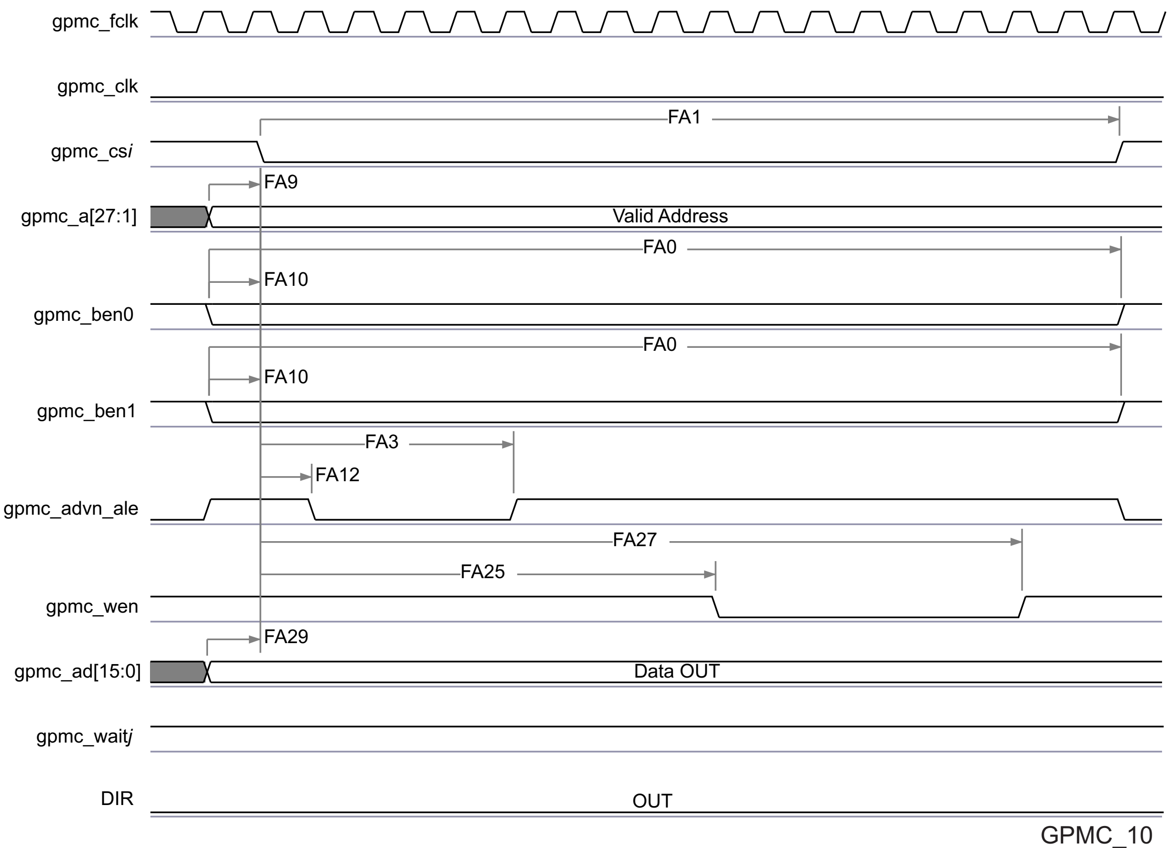


Figure 7-16. GPMC / NOR Flash - Asynchronous Write - Single Word Timing(1)

(1) In “gpmc_cs*i*”, i = 0 to 7. In “gpmc_waitj”, j = 0 to 1.

(2) The "DIR" (direction control) output signal is NOT pinned out on any of the device pads. It is an internal signal only representing a signal direction on the GPMC data bus.

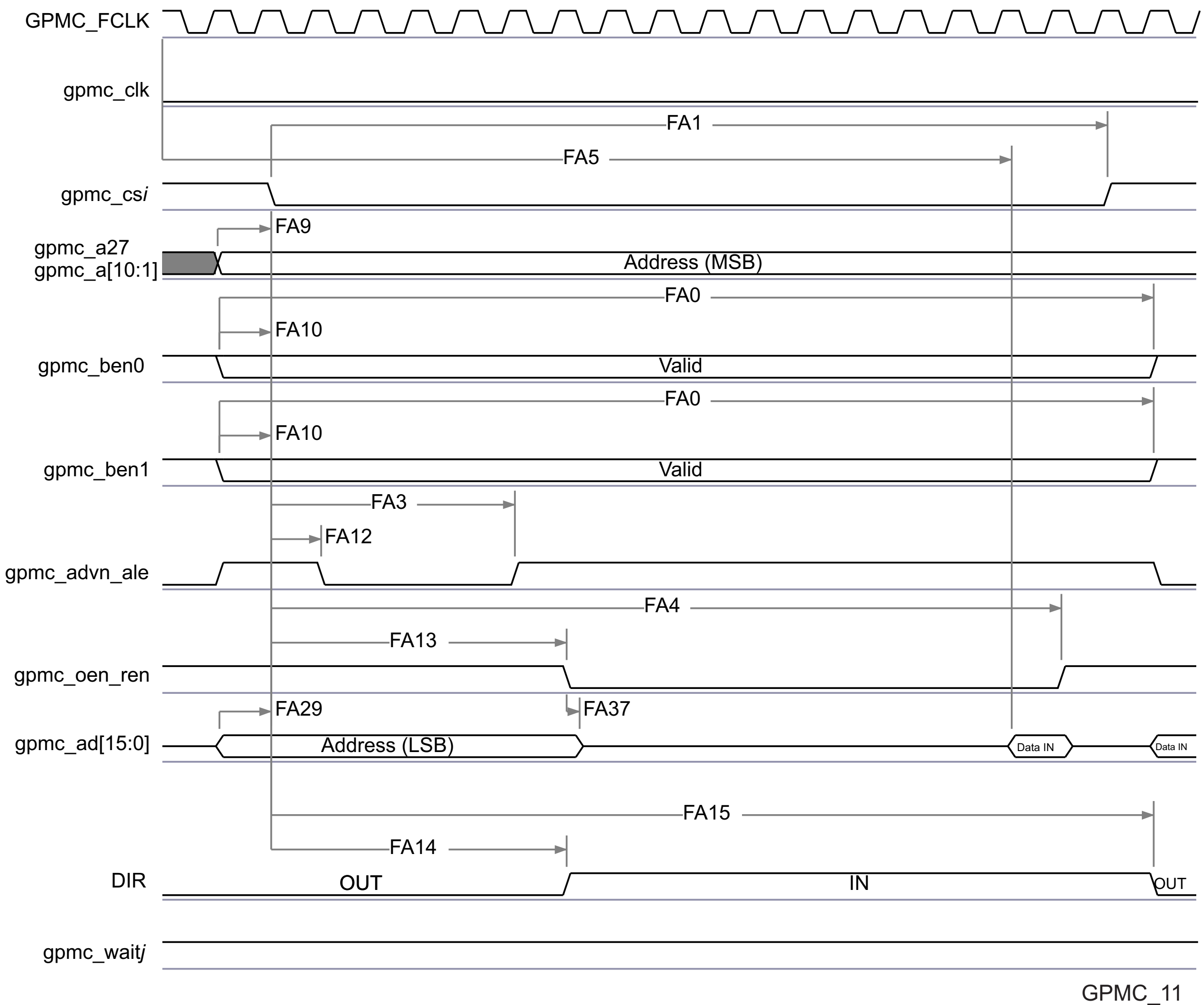


Figure 7-17. GPMC / Multiplexed NOR Flash - Asynchronous Read - Single Word Timing(1)(2)(3)

(1) In “gpmc_cs*i*”, i = 0 to 7. In “gpmc_waitj”, j = 0 to 1

(2) FA5 parameter illustrates amount of time required to internally sample input Data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input Data will be internally sampled by active functional clock edge. FA5 value should be stored inside AccessTime register bits field.

(3) GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally

(4) The "DIR" (direction control) output signal is NOT pinned out on any of the device pads. It is an internal signal only representing a signal direction on the GPMC data bus.

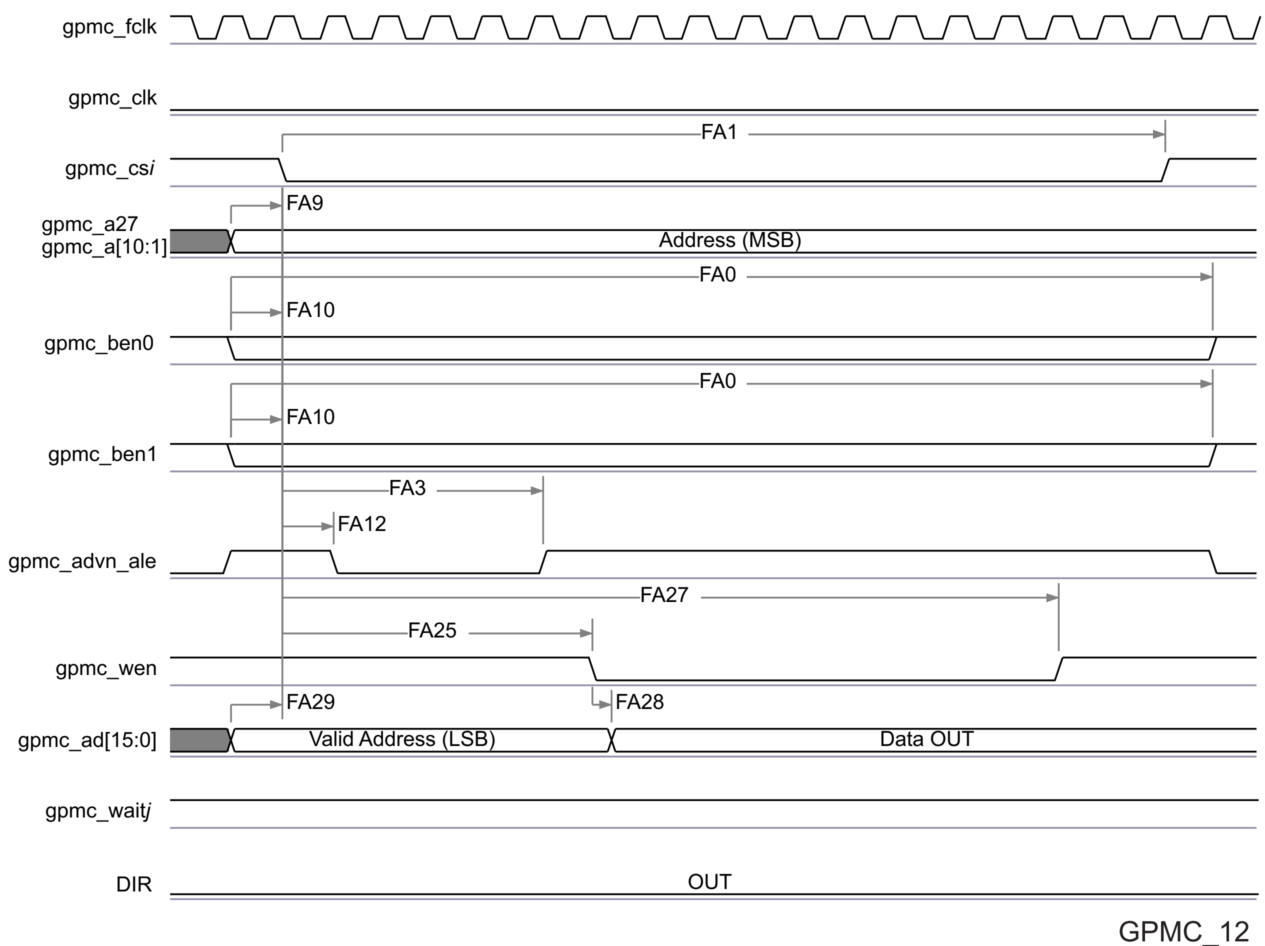


Figure 7-18. GPMC / Multiplexed NOR Flash - Asynchronous Write - Single Word Timing[(1)]

(1) In “gpmc_cs*i*”, i = 0 to 7. In “gpmc_waitj”, j = 0 to 1.

(2) The "DIR" (direction control) output signal is NOT pinned out on any of the device pads. It is an internal signal only representing a signal direction on the GPMC data bus.

7.11.3 GPMC/NAND Flash Interface Asynchronous Timing

CAUTION

The I/O Timings provided in this section are valid only for some GPMC usage modes when the corresponding Virtual I/O Timings or Manual I/O Timings are configured as described in the tables found in this section.

Table 7-30 and Table 7-31 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 7-19, Figure 7-20, Figure 7-21 and Figure 7-22).

Table 7-30. GPMC/NAND Flash Interface Timing Requirements

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
GNF12	$t_{acc(DAT)}$	Data maximum access time (GPMC_FCLK Cycles)		J [(1)]	cycles
-	$t_{su(DV-OEH)}$	Setup time, read gpmc_ad[15:0] valid before gpmc_oen_ren high	1.9		ns
-	$t_{h(OEH-DV)}$	Hold time, read gpmc_ad[15:0] valid after gpmc_oen_ren high	1		ns

(1) J = AccessTime * (TimeParaGranularity + 1)

Table 7-31. GPMC/NAND Flash Interface Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
-	$t_{r(DO)}$	Rising time, gpmc_ad[15:0] output data	0.447	4.067	ns
-	$t_{f(DO)}$	Fallling time, gpmc_ad[15:0] output data	0.43	4.463	ns
GNF0	$t_{w(nWEV)}$	Pulse duration, gpmc_wen valid time		A (1)	ns
GNF1	$t_{d(nCSV-nWEV)}$	Delay time, gpmc_cs[7:0] valid to gpmc_wen valid	B - 2 (2)	B + 4 (2)	ns
GNF2	$t_{d(CLEH-nWEV)}$	Delay time, gpmc_ben[1:0] high to gpmc_wen valid	C - 2 (3)	C + 4 (3)	ns
GNF3	$t_{d(nWEV-DV)}$	Delay time, gpmc_ad[15:0] valid to gpmc_wen valid	D - 2 (4)	D + 4 (4)	ns
GNF4	$t_{d(nWEIV-DIV)}$	Delay time, gpmc_wen invalid to gpmc_ad[15:0] invalid	E - 2 (5)	E + 4 (5)	ns
GNF5	$t_{d(nWEIV-CLEIV)}$	Delay time, gpmc_wen invalid to gpmc_ben[1:0] invalid	F - 2 (6)	F + 4 (6)	ns
GNF6	$t_{d(nWEIV-nCSIV)}$	Delay time, gpmc_wen invalid to gpmc_cs[7:0] invalid	G - 2 (7)	G + 4 (7)	ns
GNF7	$t_{d(ALEH-nWEV)}$	Delay time, gpmc_advn_ale high to gpmc_wen valid	C - 2 (3)	C + 4 (3)	ns
GNF8	$t_{d(nWEIV-ALEIV)}$	Delay time, gpmc_wen invalid to gpmc_advn_ale invalid	F - 2 (6)	F + 4 (6)	ns
GNF9	$t_{c(nWE)}$	Cycle time, write cycle time		H (8)	ns
GNF10	$t_{d(nCSV-nOEV)}$	Delay time, gpmc_cs[7:0] valid to gpmc_oen_ren valid	I - 2 (9)	I + 4 (9)	ns
GNF13	$t_{w(nOEV)}$	Pulse duration, gpmc_oen_ren valid time		K (10)	ns
GNF14	$t_{c(nOE)}$	Cycle time, read cycle time		L (11)	ns
GNF15	$t_{d(nOEIV-nCSIV)}$	Delay time, gpmc_oen_ren invalid to gpmc_cs[7:0] invalid	M - 2 (12)	M + 4 (12)	ns

(1) A = (WEOffTime - WEOnTime) * (TimeParaGranularity + 1) * GPMC_FCLK
(2) B = ((WEOnTime - CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (WEExtraDelay - CSExtraDelay)) * GPMC_FCLK
(3) C = ((WEOnTime - ADVOnTime) * (TimeParaGranularity + 1) + 0.5 * (WEExtraDelay - ADVExtraDelay)) * GPMC_FCLK
(4) D = (WEOnTime * (TimeParaGranularity + 1) + 0.5 * WEExtraDelay) * GPMC_FCLK
(5) E = (WrCycleTime - WEOffTime * (TimeParaGranularity + 1) - 0.5 * WEExtraDelay) * GPMC_FCLK
(6) F = (ADVWrOffTime - WEOffTime * (TimeParaGranularity + 1) + 0.5 * (ADVExtraDelay - WEExtraDelay) * GPMC_FCLK
(7) G = (CSWrOffTime - WEOffTime * (TimeParaGranularity + 1) + 0.5 * (CSExtraDelay - WEExtraDelay) * GPMC_FCLK
(8) H = WrCycleTime * (1 + TimeParaGranularity) * GPMC_FCLK
(9) I = ((OEOffTime + (n - 1) * PageBurstAccessTime - CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (OEExtraDelay - CSExtraDelay)) * GPMC_FCLK
(10) K = (OEOffTime - OEOnTime) * (1 + TimeParaGranularity) * GPMC_FCLK
(11) L = RdCycleTime * (1 + TimeParaGranularity) * GPMC_FCLK
(12) M = (CSRdOffTime - OEOffTime * (TimeParaGranularity + 1) + 0.5 * (CSExtraDelay - OEExtraDelay) * GPMC_FCLK

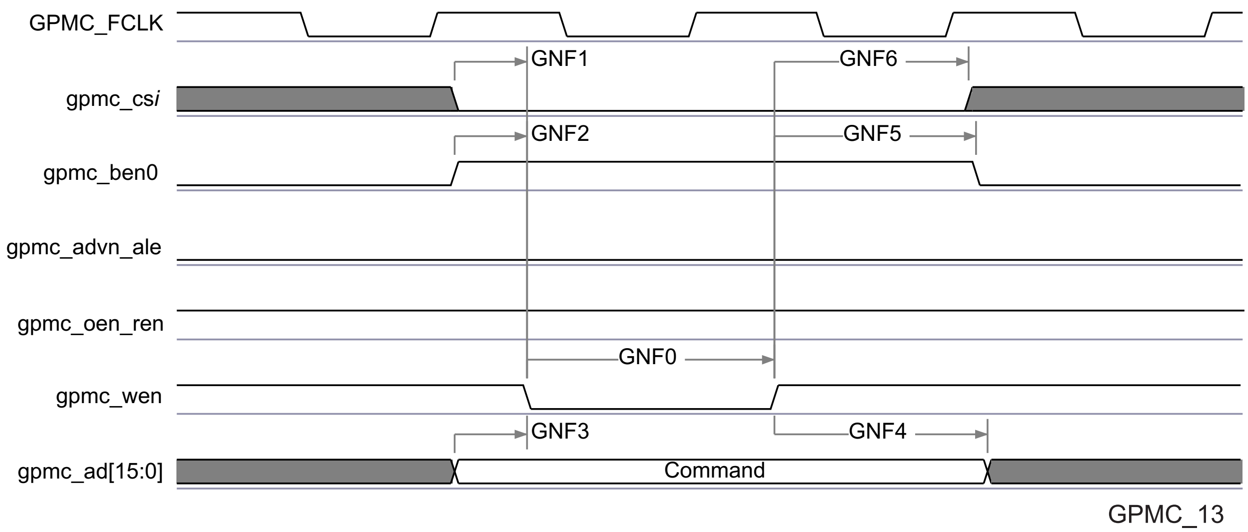


Figure 7-19. GPMC / NAND Flash - Command Latch Cycle Timing[(1)]

(1) In gpmc_cs*i*, i = 0 to 7.

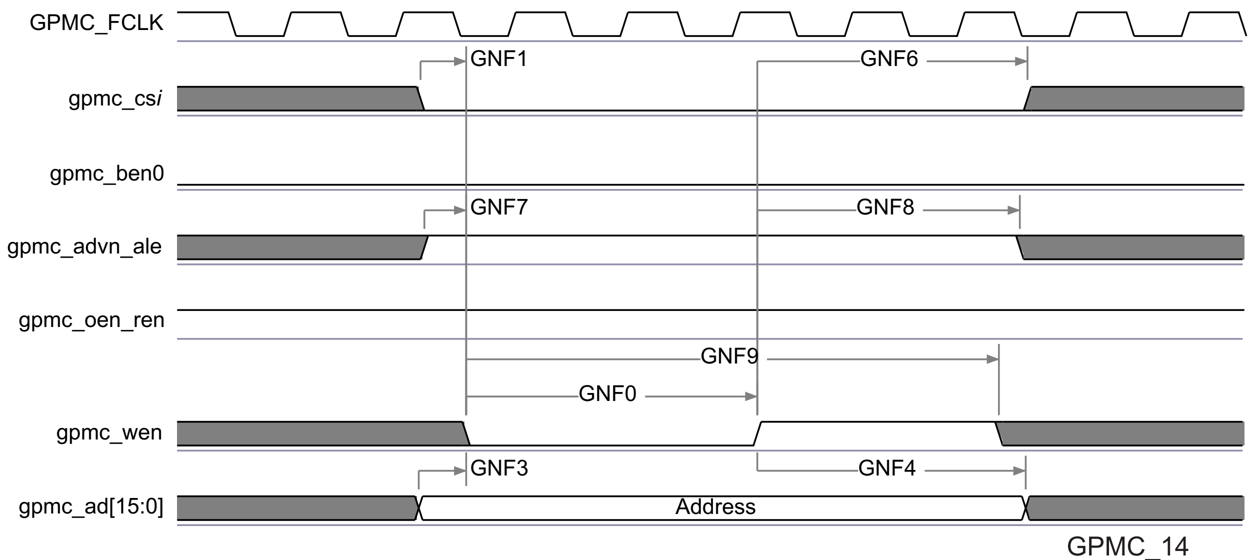


Figure 7-20. GPMC / NAND Flash - Address Latch Cycle Timing[(1)]

(1) In gpmc_cs*i*, i = 0 to 7.

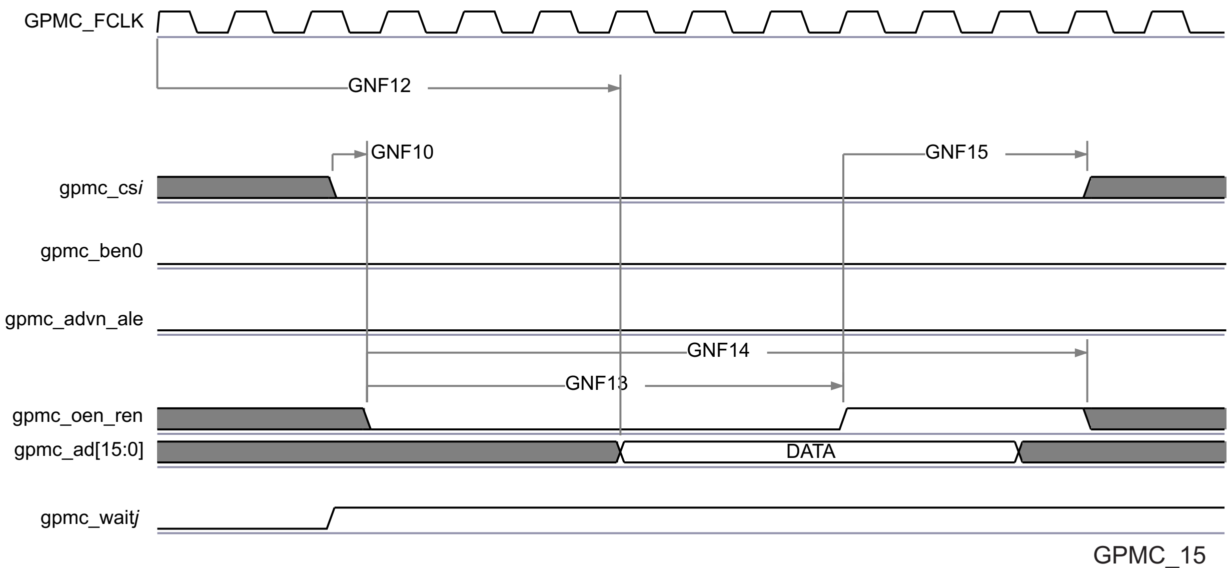


Figure 7-21. GPMC / NAND Flash - Data Read Cycle Timing[(1)(2)(3)]

(1) GNF12 parameter illustrates amount of time required to internally sample input Data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after GNF12 functional clock cycles, input data will be internally sampled by active functional clock edge. GNF12 value must be stored inside AccessTime register bits field.

(2) GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.

(3) In gpmc_cs*i*, i = 0 to 7. In gpmc_waitj, j = 0 to 1.

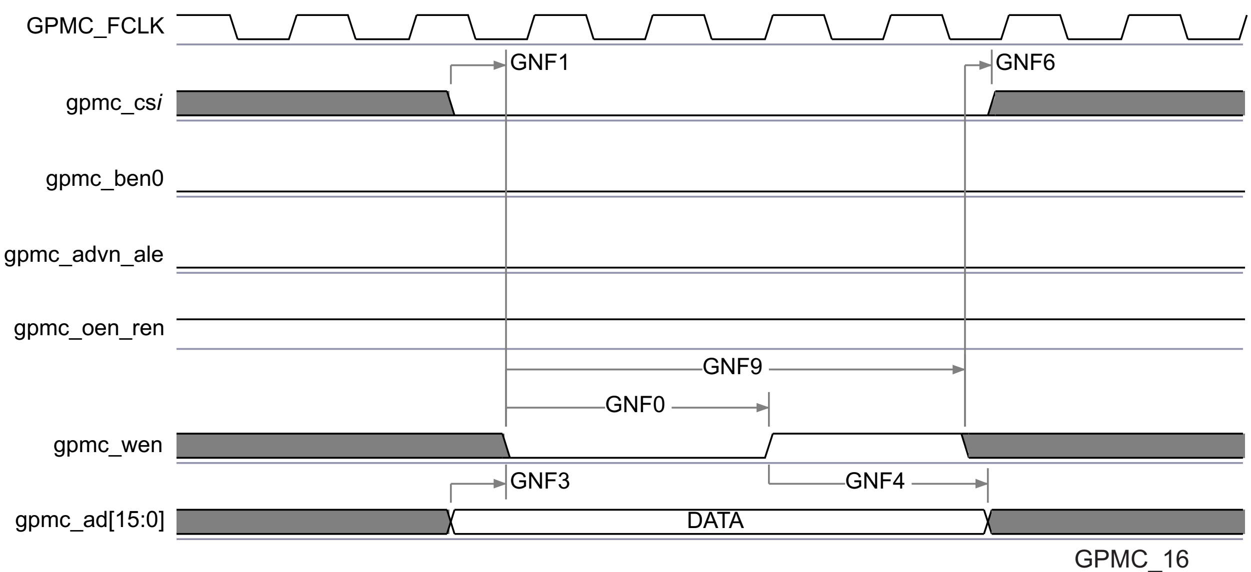


Figure 7-22. GPMC / NAND Flash - Data Write Cycle Timing[(1)]

(1) In gpmc_cs*i*, i = 0 to 7.

NOTE

To configure the desired virtual mode the user must set MODESELECT bit and DELAYMODE bit field for each corresponding pad control register.

The pad control registers are presented in Table 4-3 and described in Device TRM, *Control Module Chapter*.

Virtual IO Timings Modes must be used to ensure some IO timings for GPMC. See Table 7-2 *Modes Summary* for a list of IO timings requiring the use of Virtual IO Timings Modes. See Table 7-32 *Virtual Functions Mapping for GPMC* for a definition of the Virtual modes.

Table 7-32 presents the values for DELAYMODE bit field.

Table 7-32. Virtual Functions Mapping for GPMC

BALL	BALL NAME	Delay Mode Value	MUXMODE							
		GPMC_VIRTUAL1	0	1	2	3	5	6	14[(1)]	14[(1)]
N1	gpmc_advn_ale	15	gpmc_advn_ale	gpmc_cs6		gpmc_wait1	gpmc_a2	gpmc_a23		
H3	gpmc_ad15	13	gpmc_ad15							
L3	gpmc_ad6	13	gpmc_ad6							
L5	gpmc_ad2	13	gpmc_ad2							
E6	vin2a_d9	9							gpmc_a25	
M3	gpmc_wen	15	gpmc_wen							
H2	gpmc_ad14	13	gpmc_ad14							
R3	gpmc_a13	15	gpmc_a13							
N7	gpmc_a8	14	gpmc_a8							
T2	gpmc_a14	15	gpmc_a14							
L6	gpmc_ad4	13	gpmc_ad4							
H4	gpmc_a26	15	gpmc_a26		gpmc_a20					
M6	gpmc_ad0	13	gpmc_ad0							
N2	gpmc_wait0	15	gpmc_wait0							
F6	vin2a_d11	9							gpmc_a23	
M2	gpmc_ad1	13	gpmc_ad1							
J3	gpmc_ad13	13	gpmc_ad13							
T6	gpmc_a2	14	gpmc_a2							
L4	gpmc_ad5	13	gpmc_ad5							
F5	vin2a_d8	9							gpmc_a26	
T1	gpmc_cs0	15	gpmc_cs0							
G1	vin2a_hsync0	9							gpmc_a27	
P6	gpmc_a4	14	gpmc_a4							
N6	gpmc_ben0	15	gpmc_ben0	gpmc_cs4						
R5	gpmc_a6	14	gpmc_a6							
U2	gpmc_a15	15	gpmc_a15							
J2	gpmc_ad11	13	gpmc_ad11							

Table 7-32. Virtual Functions Mapping for GPMC (continued)

BALL	BALL NAME	Delay Mode Value	MUXMODE							
		GPMC_VIRTUAL1	0	1	2	3	5	6	14[(1)]	14[(1)]
U1	gpmc_a16	15	gpmc_a16							
T9	gpmc_a1	14	gpmc_a1							
J4	gpmc_a24	15	gpmc_a24		gpmc_a18					
J7	gpmc_a23	15	gpmc_a23		gpmc_a17					
L1	gpmc_ad8	13	gpmc_ad8							
J1	gpmc_ad10	13	gpmc_ad10							
H1	gpmc_ad12	13	gpmc_ad12							
M7	gpmc_a20	15	gpmc_a20		gpmc_a14					
D3	vin2a_d10	9							gpmc_a24	
P1	gpmc_cs3	14	gpmc_cs3				gpmc_a1			
M5	gpmc_oen_ren	15	gpmc_oen_ren							
R4	gpmc_a9	14	gpmc_a9							
H6	gpmc_cs1	15	gpmc_cs1		gpmc_a22					
M1	gpmc_ad3	13	gpmc_ad3							
L2	gpmc_ad7	13	gpmc_ad7							
P5	gpmc_a7	14	gpmc_a7							
T7	gpmc_a3	14	gpmc_a3							
M4	gpmc_ben1	15	gpmc_ben1	gpmc_cs5			gpmc_a3			
P7	gpmc_clk	15	gpmc_clk	gpmc_cs7		gpmc_wait1				
K6	gpmc_a22	15	gpmc_a22		gpmc_a16					
P2	gpmc_cs2	15	gpmc_cs2							
H7	vin2a_fld0	11							gpmc_a27	gpmc_a18
N9	gpmc_a10	14	gpmc_a10							
P4	gpmc_a12	15	gpmc_a12				gpmc_a0			
P3	gpmc_a17	15	gpmc_a17							
R9	gpmc_a5	14	gpmc_a5							
J5	gpmc_a21	15	gpmc_a21		gpmc_a15					
H5	gpmc_a27	15	gpmc_a27		gpmc_a21					
K2	gpmc_ad9	13	gpmc_ad9							
K7	gpmc_a19	15	gpmc_a19		gpmc_a13					
J6	gpmc_a25	15	gpmc_a25		gpmc_a19					
R6	gpmc_a0	14	gpmc_a0							

Table 7-32. Virtual Functions Mapping for GPMC (continued)

BALL	BALL NAME	Delay Mode Value	MUXMODE							
		GPMC_VIRTUAL1	0	1	2	3	5	6	14[(1)]	14[(1)]
E1	vin2a_clk0	11							gpmc_a27	gpmc_a17
R2	gpmc_a18	15	gpmc_a18							
P9	gpmc_a11	14	gpmc_a11							

(1) Some signals listed are virtual functions that present alternate multiplexing options. These virtual functions are controlled via CTRL_CORE_ALT_SELECT_MUX or CTRL_CORE_VIP_MUX_SELECT registers. For more information on how to use these options, see *Pad Configuration Registers* section, *Control Module* chapter in the device TRM.

7.12 Timers

The device has 16 general-purpose (GP) timers (TIMER1 - TIMER16), two watchdog timers, and a 32-kHz synchronized timer (COUNTER_32K) that have the following features:

- Dedicated input trigger for capture mode and dedicated output trigger/pulse width modulation (PWM) signal
- Interrupts generated on overflow, compare, and capture
- Free-running 32-bit upward counter
- Supported modes:
  - Compare and capture modes
  - Auto-reload mode
  - Start-stop mode
- On-the-fly read/write register (while counting)

The device has two system watchdog timer (WD_TIMER1 and WD_TIMER2) that have the following features:

- Free-running 32-bit upward counter
- On-the-fly read/write register (while counting)
- Reset upon occurrence of a timer overflow condition

WD_TIMER2 is available in all devices as a system watchdog timer. WD_TIMER1 is only supported in security enabled devices.

The watchdog timer is used to provide a recovery mechanism for the device in the event of a fault condition, such as a non-exiting code loop.

NOTE

For additional information on the Timer Module, see the Device TRM.

7.13 Inter-Integrated Circuit Interface (I2C)

The device includes 6 inter-integrated circuit (I2C) modules which provide an interface to other devices compliant with Philips Semiconductors Inter-IC bus (I2C) specification version 2.1. External components attached to this 2-wire serial bus can transmit/receive 8-bit data to/from the device through the I2C module.

NOTE

Note that, on I2C1 and I2C2, due to characteristics of the open drain IO cells, HS mode is not supported.

NOTE

Inter-integrated circuit i (i=1 to 6) module is also referred to as I2Ci.

NOTE

For more information, see *Multimaster High Speed I2C Controller* section in the device TRM.

Table 7-33, Table 7-34 and Figure 7-23 assume testing over the recommended operating conditions and electrical characteristic conditions below.

Table 7-33. Timing Requirements for I2C Input Timings(1)

NO.	PARAMETER	DESCRIPTION	STANDARD MODE		FAST MODE		UNIT
			MIN	MAX	MIN	MAX	
1	$t_{c(SCL)}$	Cycle time, SCL	10		2.5		µs
2	$t_{su(SCLH-SDAL)}$	Setup time, SCL high before SDA low (for a repeated START condition)	4.7		0.6		µs
3	$t_{h(SDAL-SCLL)}$	Hold time, SCL low after SDA low (for a START and a repeated START condition)	4		0.6		µs
4	$t_{w(SCLL)}$	Pulse duration, SCL low	4.7		1.3		µs
5	$t_{w(SCLH)}$	Pulse duration, SCL high	4		0.6		µs
6	$t_{su(SDAV-SCLH)}$	Setup time, SDA valid before SCL high	250		100(2)		ns
7	$t_{h(SCLL-SDAV)}$	Hold time, SDA valid after SCL low	0(3)	3.45(4)	0(3)	0.9(4)	µs
8	$t_{w(SDAH)}$	Pulse duration, SDA high between STOP and START conditions	4.7		1.3		µs
9	$t_{r(SDA)}$	Rise time, SDA		1000	$20 + 0.1C_b$ (5)	300(3)	ns
10	$t_{r(SCL)}$	Rise time, SCL		1000	$20 + 0.1C_b$ (5)	300(3)	ns
11	$t_{f(SDA)}$	Fall time, SDA		300	$20 + 0.1C_b$ (5)	300(3)	ns
12	$t_{f(SCL)}$	Fall time, SCL		300	$20 + 0.1C_b$ (5)	300(3)	ns
13	$t_{su(SCLH-SDAH)}$	Setup time, SCL high before SDA high (for STOP condition)	4		0.6		µs
14	$t_{w(SP)}$	Pulse duration, spike (must be suppressed)			0	50	ns
15	C_b (5)	Capacitive load for each bus line		400		400	pF

(1) The I2C pins SDA and SCL do not feature fail-safe I/O buffers. These pins could potentially draw current when the device is powered down.

(2) A Fast-mode I2C device can be used in a Standard-mode I2C system, but the requirement $t_{su(SDA-SCLH)} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t_r max + $t_{su(SDA-SCLH)}$= 1000 + 250 = 1250 ns (according to the Standard-mode I2C Specification) before the SCL line is released.

(3) A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL.

(4) The maximum $t_{h(SDA-SCLL)}$ has only to be met if the device does not stretch the low period [$t_{w(SCLL)}$] of the SCL signal.

(5) C_b = total capacitance of one bus line in pF. If mixed with HS-mode devices, faster fall-times are allowed.

Table 7-34. Timing Requirements for I2C HS-Mode (I2C3/4/5/6 Only)(1)

NO.	PARAMETER	DESCRIPTION	C_b = 100 pF MAX		C_b = 400 pF (2)		UNIT
			MIN	MAX	MIN	MAX	
1	$t_{c(SCL)}$	Cycle time, SCL	0.294		0.588		µs
2	$t_{su(SCLH-SDAL)}$	Set-up time, SCL high before SDA low (for a repeated START condition)	160		160		ns
3	$t_{h(SDAL-SCLL)}$	Hold time, SCL low after SDA low (for a repeated START condition)	160		160		ns
4	$t_{w(SCLL)}$	LOW period of the SCLH clock	160		320		ns
5	$t_{w(SCLH)}$	HIGH period of the SCLH clock	60		120		ns
6	$t_{su(SDAV-SCLH)}$	Setup time, SDA valid vefore SCL high	10		10		ns

Table 7-34. Timing Requirements for I2C HS-Mode (I2C3/4/5/6 Only)(1) (continued)

NO.	PARAMETER	DESCRIPTION	C_b = 100 pF MAX		C_b = 400 pF (2)		UNIT
			MIN	MAX	MIN	MAX	
7	$t_{h(SCLL-SDAV)}$	Hold time, SDA valid after SCL low	0 (3)	70	0 (3)	150	ns
13	$t_{su(SCLH-SDAH)}$	Setup time, SCL high before SDA high (for a STOP condition)	160		160		ns
14	$t_{w(SP)}$	Pulse duration, spike (must be suppressed)	0	10	0	10	ns
15	C_b (2)	Capacitive load for SDAH and SCLH lines		100		400	pF
16	C_b	Capacitive load for SDAH + SDA line and SCLH + SCL line		400		400	pF

(1) I2C HS-Mode is only supported on I2C3/4/5/6. I2C HS-Mode is not supported on I2C1/2.

(2) For bus line loads C_b between 100 and 400 pF the timing parameters must be linearly interpolated.

(3) A device must internally provide a Data hold time to bridge the undefined part between V_{IH} and V_{IL} of the falling edge of the SCLH signal. An input circuit with a threshold as low as possible for the falling edge of the SCLH signal minimizes this hold time.

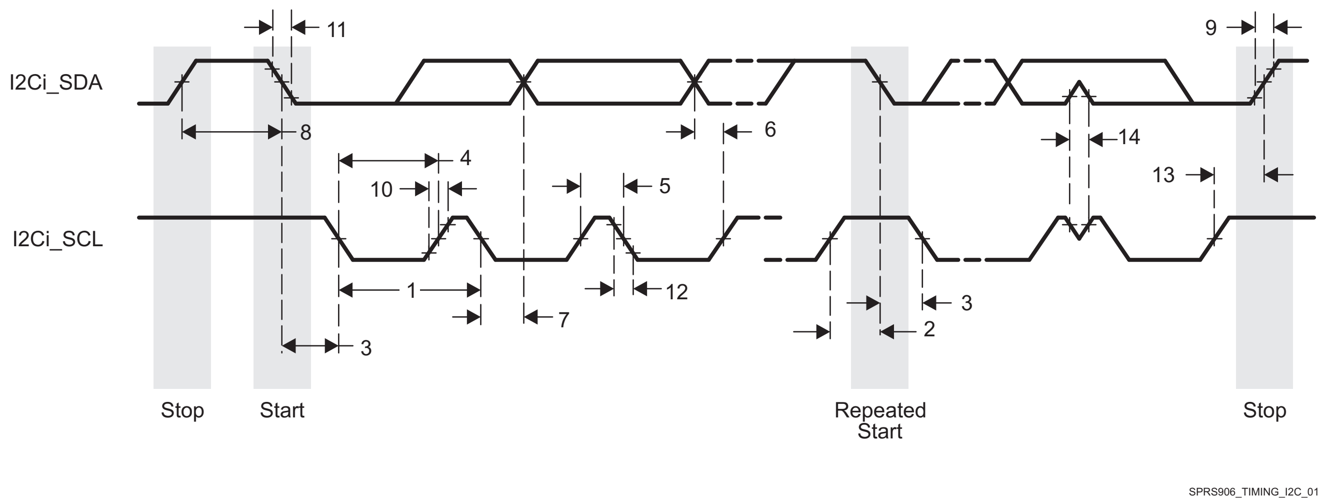


Figure 7-23. I2C Receive Timing

Table 7-35 and Figure 7-24 assume testing over the recommended operating conditions and electrical characteristic conditions below.

Table 7-35. Switching Characteristics Over Recommended Operating Conditions for I2C Output Timings(2)

NO.	PARAMETER	DESCRIPTION	STANDARD MODE		FAST MODE		UNIT
			MIN	MAX	MIN	MAX	
16	$t_{c(SCL)}$	Cycle time, SCL	10		2.5		µs
17	$t_{su(SCLH-SDAL)}$	Setup time, SCL high before SDA low (for a repeated START condition)	4.7		0.6		µs
18	$t_{h(SDAL-SCLL)}$	Hold time, SCL low after SDA low (for a START and a repeated START condition)	4		0.6		µs
19	$t_{w(SCLL)}$	Pulse duration, SCL low	4.7		1.3		µs
20	$t_{w(SCLH)}$	Pulse duration, SCL high	4		0.6		µs
21	$t_{su(SDAV-SCLH)}$	Setup time, SDA valid before SCL high	250		100		ns
22	$t_{h(SCLL-SDAV)}$	Hold time, SDA valid after SCL low (for I2C bus devices)	0	3.45	0	0.9	µs
23	$t_{w(SDAH)}$	Pulse duration, SDA high between STOP and START conditions	4.7		1.3		µs

Table 7-35. Switching Characteristics Over Recommended Operating Conditions for I2C Output Timings[(2)] (continued)

NO.	PARAMETER	DESCRIPTION	STANDARD MODE		FAST MODE		UNIT
			MIN	MAX	MIN	MAX	
24	$t_{r(SDA)}$	Rise time, SDA		1000	20 + 0.1C_b [(1)] [(3)]	300[(3)]	ns
25	$t_{r(SCL)}$	Rise time, SCL		1000	20 + 0.1C_b [(1)] [(3)]	300[(3)]	ns
26	$t_{f(SDA)}$	Fall time, SDA		300	20 + 0.1C_b [(1)] [(3)]	300[(3)]	ns
27	$t_{f(SCL)}$	Fall time, SCL		300	20 + 0.1C_b [(1)] [(3)]	300[(3)]	ns
28	$t_{su(SCLH-SDAH)}$	Setup time, SCL high before SDA high (for STOP condition)	4		0.6		µs
29	C_p	Capacitance for each I2C pin		10		10	pF

(1) C_b = total capacitance of one bus line in pF. If mixed with HS-mode devices, faster fall-times are allowed.

(2) Software must properly configure the I2C module registers to achieve the required timing parameters. For more information, see *Multimaster High Speed I2C Controller* section in the device TRM.

(3) These timings apply only to I2C1 and I2C2. I2C3, I2C4, I2C5 and I2C6 use standard LVCMOS buffers to emulate open-drain buffers and their rise/fall times should be referenced in the device IBIS model.

NOTE

I2C emulation is achieved by configuring the LVCMOS buffers to output Hi-Z instead of driving high when transmitting logic-1.

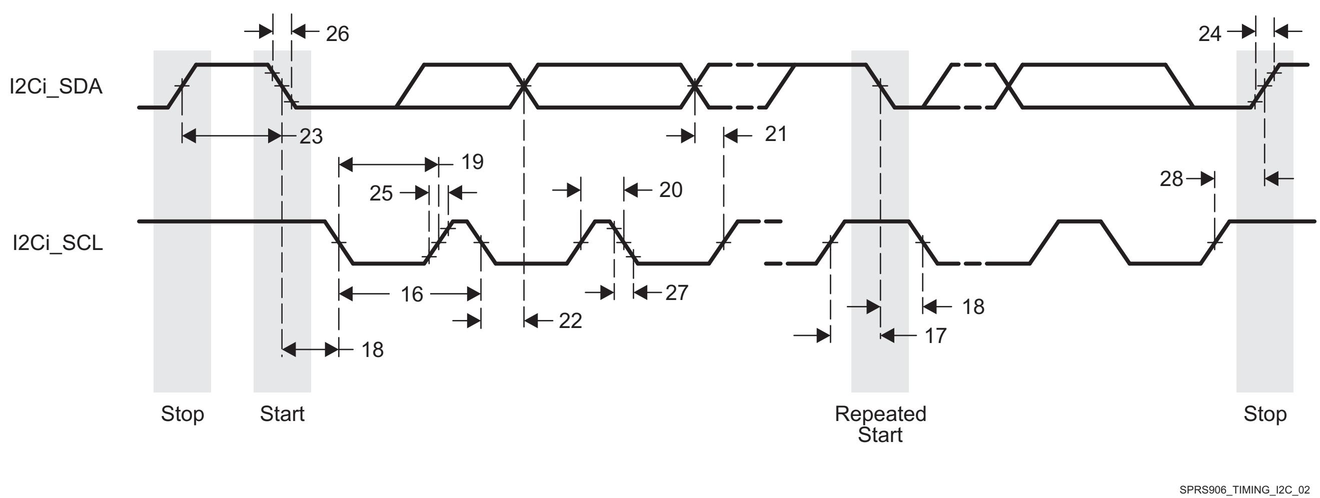


Figure 7-24. I2C Transmit Timing

7.14 Universal Asynchronous Receiver Transmitter (UART)

The UART performs serial-to-parallel conversions on data received from a peripheral device and parallel-to-serial conversion on data received from the CPU. There are 10 UART modules in the device. Only one UART supports IrDA features. Each UART can be used for configuration and data exchange with a number of external peripheral devices or interprocessor communication between devices

The UARTi (where i = 1 to 10) include the following features:

- 16C750 compatibility
- 64-byte FIFO buffer for receiver and 64-byte FIFO for transmitter
- Baud generation based on programmable divisors N (where N = 1…16 384) operating from a fixed functional clock of 48 MHz or 192 MHz

- Break character detection and generation
- Configurable data format:
  - Data bit: 5, 6, 7, or 8 bits
  - Parity bit: Even, odd, none
  - Stop-bit: 1, 1.5, 2 bit(s)
- Flow control: Hardware (RTS/CTS) or software (XON/XOFF)
- Only UART1 module has extended modem control signals (CD, RI, DTR, DSR)
- Only UART3 supports IrDA

NOTE

For more information, see *UART/IrDA/CIR* section in the device TRM.

Table 7-36, Table 7-37 and Figure 7-25 assume testing over the recommended operating conditions and electrical characteristic conditions below.

Table 7-36. Timing Requirements for UART

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
4	$t_{w(RX)}$	Pulse width, receive data bit, 15/30/100pF high or low	0.96U(1)	1.05U(1)	ns
5	$t_{w(CTS)}$	Pulse width, receive start bit, 15/30/100pF high or low	0.96U(1)	1.05U(1)	ns
	$t_{d(RTS-TX)}$	Delay time, transmit start bit to transmit data	P(2)		ns
	$t_{d(CTS-TX)}$	Delay time, receive start bit to transmit data	P(2)		ns

(1) U = UART baud time = 1/programmed baud rate

(2) P = Clock period of the reference clock (FCLK, usually 48 MHz or 192MHz).

Table 7-37. Switching Characteristics Over Recommended Operating Conditions for UART

NO.	PARAMETER	DESCRIPTION		MIN	MAX	UNIT
	$f_{(baud)}$	Maximum programmable baud rate	15 pF		12	MHz
			30 pF		0.23	
			100 pF		0.115	
2	$t_{w(TX)}$	Pulse width, transmit data bit, 15/30/100 pF high or low		U - 2(1)	U + 2(1)	ns
3	$t_{w(RTS)}$	Pulse width, transmit start bit, 15/30/100 pF high or low		U - 2(1)	U + 2(1)	ns

(1) U = UART baud time = 1/programmed baud rate

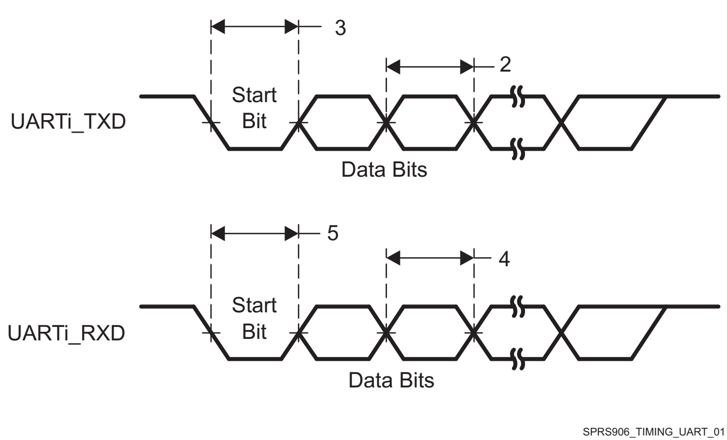


Figure 7-25. UART Timing

7.15 Multichannel Serial Peripheral Interface (McSPI)

The McSPI is a master/slave synchronous serial bus. There are four separate McSPI modules (SPI1, SPI2, SPI3, and SPI4) in the device. All these four modules support up to four external devices (four chip selects) and are able to work as both master and slave.

The McSPI modules include the following main features:

- Serial clock with programmable frequency, polarity, and phase for each channel
- Wide selection of SPI word lengths, ranging from 4 to 32 bits
- Up to four master channels, or single channel in slave mode
- Master multichannel mode:
  - Full duplex/half duplex
  - Transmit-only/receive-only/transmit-and-receive modes
  - Flexible input/output (I/O) port controls per channel
  - Programmable clock granularity
  - SPI configuration per channel. This means, clock definition, polarity enabling and word width
- Power management through wake-up capabilities
- Programmable timing control between chip select and external clock generation
- Built-in FIFO available for a single channel.
- Each SPI module supports multiple chip select pins spim_cs[i], where i = 1 to 4.

NOTE

For more information, see *Multichannel Serial Peripheral Interface* section in the device TRM.

NOTE

The McSPIm module (m = 1 to 4) is also referred to as SPIm.

CAUTION

The I/O timings provided in this section are applicable for all combinations of signals for SPI1 and SPI2. However, the timings are valid only for SPI3 and SPI4 if signals within a single IOSET are used. The IOSETS are defined in Table 7-40.

Table 7-38, Figure 7-26 and Figure 7-27 present Timing Requirements for McSPI - Master Mode.

Table 7-38. Timing Requirements for SPI - Master Mode [(1)]

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
SM1	$t_{c(SPICLK)}$	Cycle time, spi_sclk [(1)] [(2)]	SPI1/2/3/4	20.8 [(3)]		ns
SM2	$t_{w(SPICLKL)}$	Typical Pulse duration, spi_sclk low [(1)]		0.5*P-1 [(4)]		ns
SM3	$t_{w(SPICLKH)}$	Typical Pulse duration, spi_sclk high [(1)]		0.5*P-1 [(4)]		ns
SM4	$t_{su(MISO-SPICLK)}$	Setup time, spi_d[x] valid before spi_sclk active edge [(1)]		3.5		ns
SM5	$t_{h(SPICLK-MISO)}$	Hold time, spi_d[x] valid after spi_sclk active edge [(1)]		3.7		ns

Table 7-38. Timing Requirements for SPI - Master Mode [(1)] (continued)

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
SM6	$t_{d(SPICLK-SIMO)}$	Delay time, spi_sclk active edge to spi_d[x] transition [(1)]	SPI1	-3.57	4.1	ns
			SPI2	-3.9	3.6	ns
			SPI3	-4.9	4.7	ns
			SPI4	-4.3	4.5	ns
SM7	$t_{d(CS-SIMO)}$	Delay time, spi_cs[x] active edge to spi_d[x] transition			5	ns
SM8	$t_{d(CS-SPICLK)}$	Delay time, spi_cs[x] active to spi_sclk first edge [(1)]	MASTER_PHA0 [(5)]	B-4.2 [(6)]		ns
			MASTER_PHA1 [(5)]	A-4.2 [(7)]		ns
SM9	$t_{d(SPICLK-CS)}$	Delay time, spi_sclk last edge to spi_cs[x] inactive [(1)]	MASTER_PHA0 [(5)]	A-4.2 [(7)]		ns
			MASTER_PHA1 [(5)]	B-4.2 [(6)]		ns

(1) This timing applies to all configurations regardless of SPI_CLK polarity and which clock edges are used to drive output data and capture input data.

(2) Related to the SPI_CLK maximum frequency.

(3) 20.8ns cycle time = 48MHz

(4) P = SPICLK period.

(5) SPI_CLK phase is programmable with the PHA bit of the SPI_CH(i)CONF register.

(6) B = (TCS + 0.5) * TSPICLKREF * Fratio, where TCS is a bit field of the SPI_CH(i)CONF register and Fratio = Even ≥2.

(7) When P = 20.8 ns, A = (TCS + 1) * TSPICLKREF, where TCS is a bit field of the SPI_CH(i)CONF register. When P > 20.8 ns, A = (TCS + 0.5) * Fratio * TSPICLKREF, where TCS is a bit field of the SPI_CH(i)CONF register.

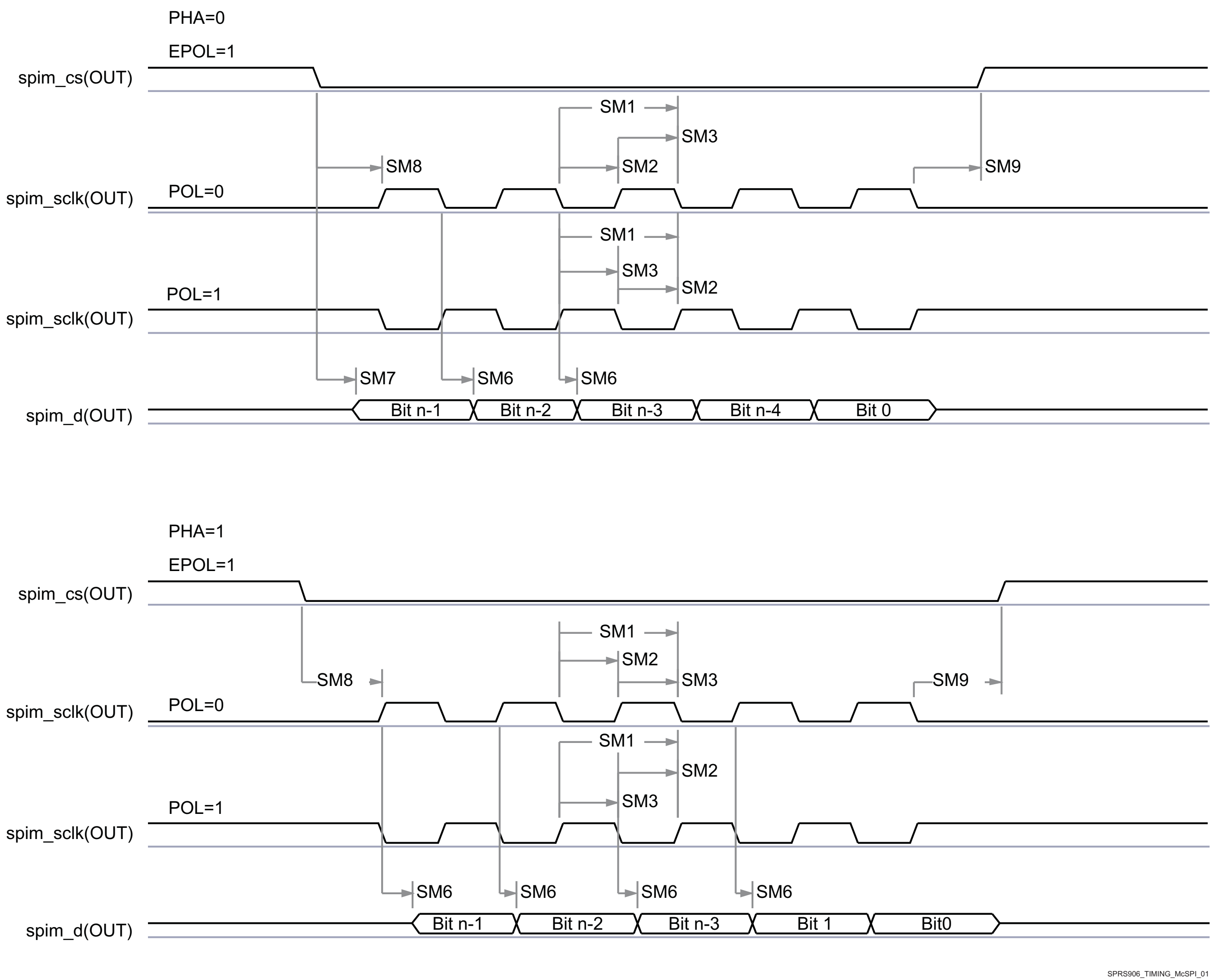


Figure 7-26. McSPI - Master Mode Transmit

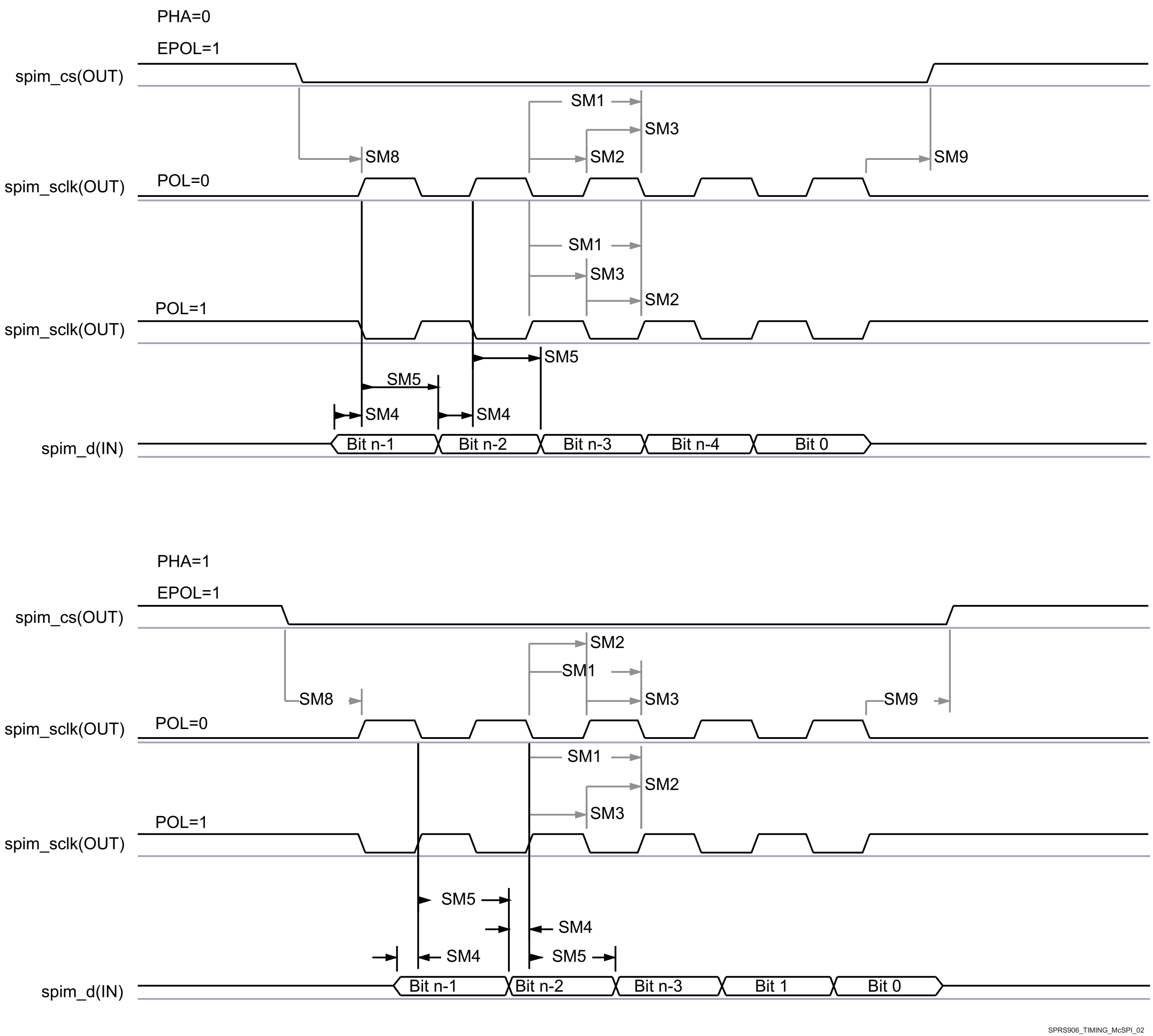


Figure 7-27. McSPI - Master Mode Receive

Table 7-39, Figure 7-28 and Figure 7-29 present Timing Requirements for McSPI - Slave Mode.

Table 7-39. Timing Requirements for SPI - Slave Mode

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
SS1 (1)	$t_{c(SPICLK)}$	Cycle time, spi_sclk		62.5 (2) (3)		ns
SS2 (1)	$t_{w(SPICLKL)}$	Typical Pulse duration, spi_sclk low		0.45*P (4)		ns
SS3 (1)	$t_{w(SPICLKH)}$	Typical Pulse duration, spi_sclk high		0.45*P (4)		ns
SS4 (1)	$t_{su(SIMO-SPICLK)}$	Setup time, spi_d[x] valid before spi_sclk active edge		5		ns
SS5 (1)	$t_{h(SPICLK-SIMO)}$	Hold time, spi_d[x] valid after spi_sclk active edge		5		ns
SS6 (1)	$t_{d(SPICLK-SOMI)}$	Delay time, spi_sclk active edge to mcspi_somi transition	SPI1/2/3	2	26.6	ns
			SPI4	2	20.1	ns
SS7 (5)	$t_{d(CS-SOMI)}$	Delay time, spi_cs[x] active edge to mcspi_somi transition			20.95	ns

Table 7-39. Timing Requirements for SPI - Slave Mode (continued)

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
SS8 (1)	$t_{su(CS-SPICLK)}$	Setup time, spi_cs[x] valid before spi_sclk first edge		5		ns
SS9 (1)	$t_{h(SPICLK-CS)}$	Hold time, spi_cs[x] valid after spi_sclk last edge	SPI1/2	5		ns
			SPI3	7.5		ns
			SPI4	6		ns

(1) This timing applies to all configurations regardless of SPI_CLK polarity and which clock edges are used to drive output data and capture input data.

(2) When operating the SPI interface in RX-only mode, the minimum Cycle time is 26ns (38.4MHz)

(3) 62.5ns Cycle time = 16 MHz

(4) P = SPICLK period.

(5) PHA = 0; SPI_CLK phase is programmable with the PHA bit of the SPI_CH(i)CONF register.

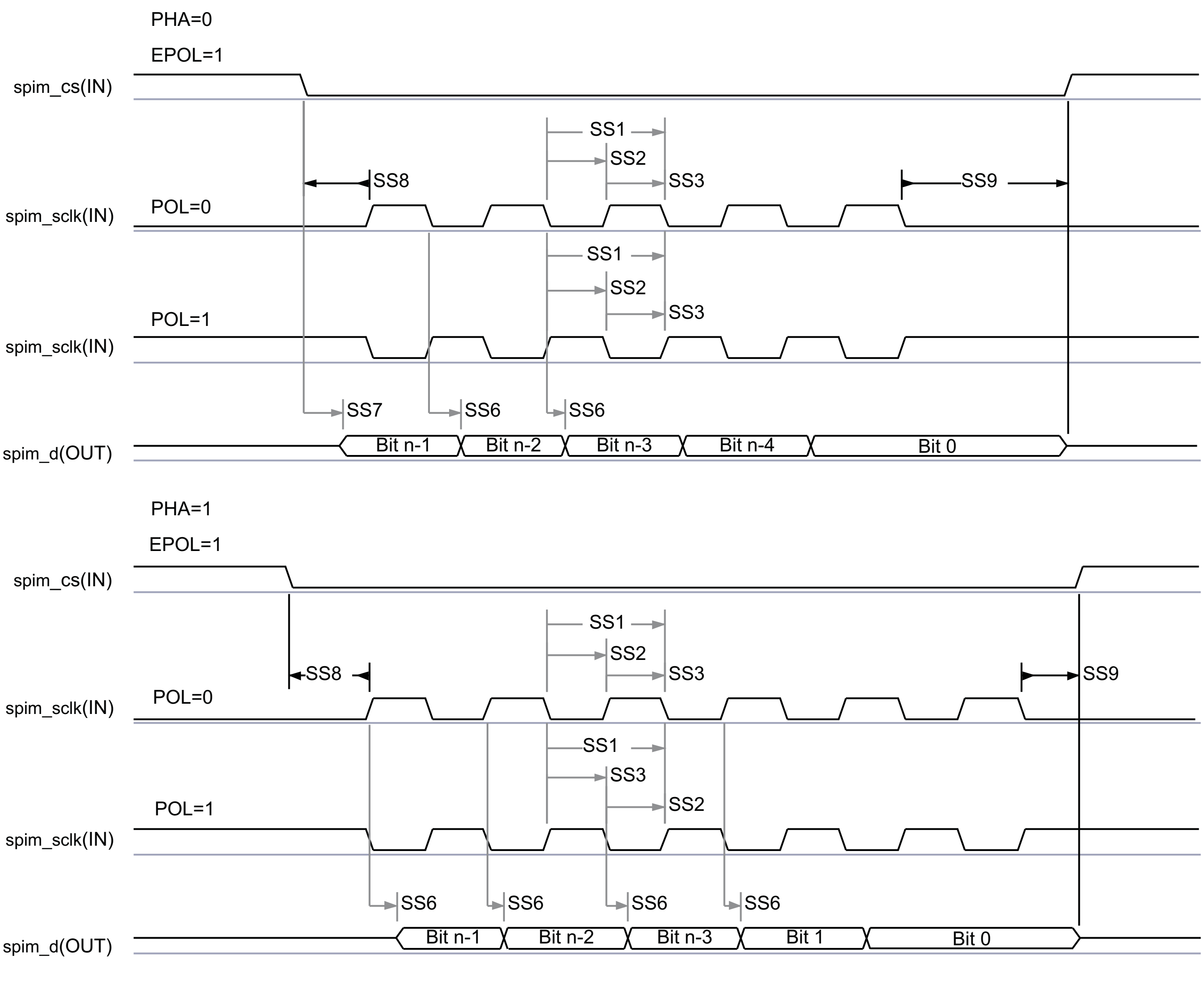


Figure 7-28. McSPI - Slave Mode Transmit

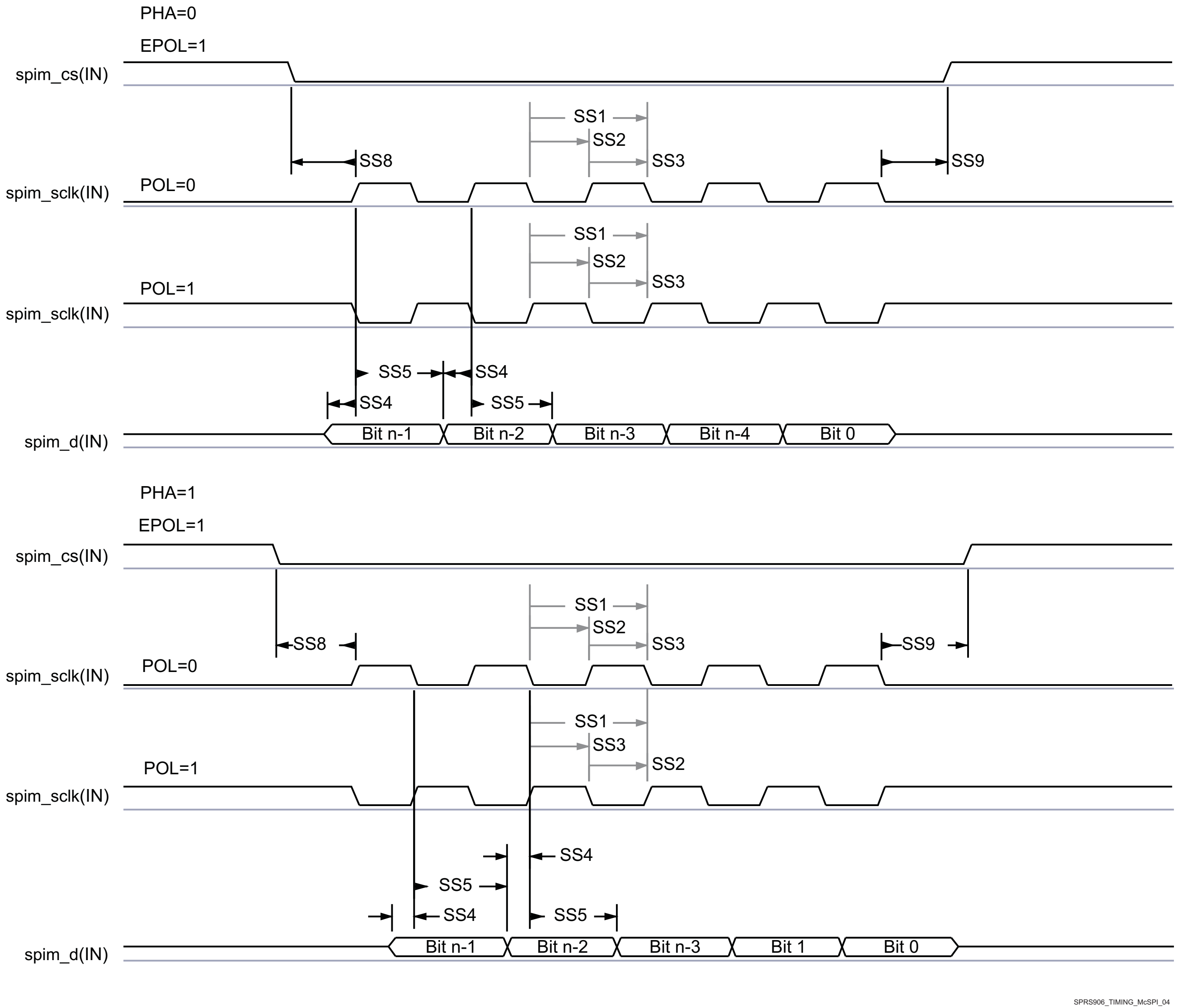


Figure 7-29. McSPI - Slave Mode Receive

In Table 7-40 are presented the specific groupings of signals (IOSET) for use with SPI3 and SPI4.

Table 7-40. McSPI3/4 IOSETs

SIGNALS	IOSET1		IOSET2		IOSET3		IOSET4		IOSET5	
	BALL	MUX	BALL	MUX	BALL	MUX	BALL	MUX	BALL	MUX
McSPI3										
spi3_cs0	D11	8	V9	7	A12	3	D17	2	AC9	1
spi3_cs1	B11	8	AC3	1	E14	3	B11	8	AC3	1
spi3_cs2	F11	8			F11	8	F11	8		
spi3_cs3	A10	8			A10	8	A10	8		
spi3_d0	C11	8	W9	7	B13	3	G16	2	AC6	1
spi3_d1	B10	8	Y1	7	A11	3	A21	2	AC7	1
spi3_sclk	E11	8	V2	7	B12	3	C18	2	AC4	1
McSPI4										
spi4_cs0	P9	8	F3	8	U6	7	AA4	2	AB5	1

Table 7-40. McSPI3/4 IOSETs (continued)

SIGNALS	IOSET1		IOSET2		IOSET3		IOSET4		IOSET5	
	BALL	MUX	BALL	MUX	BALL	MUX	BALL	MUX	BALL	MUX
spi4_cs1	P4	8	P4	8	Y1	8	Y1	8	Y1	8
spi4_cs2	R3	8	R3	8	W9	8	W9	8	W9	8
spi4_cs3	T2	8	T2	8	V9	8	V9	8	V9	8
spi4_d0	N9	8	F2	8	V6	7	AB3	2	AB8	1
spi4_d1	R4	8	G6	8	U7	7	AB9	2	AD6	1
spi4_sclk	N7	8	G1	8	V7	7	AA3	2	AC8	1

7.16 Quad Serial Peripheral Interface (QSPI)

The Quad SPI (QSPI) module is a type of SPI module that allows single, dual or quad read access to external SPI devices. This module has a memory mapped register interface, which provides a direct interface for accessing data from external SPI devices and thus simplifying software requirements. It works as a master only. There is one QSPI module in the device and it is primary intended for fast booting from quad-SPI flash memories.

General SPI features:

- Programmable clock divider
- Six pin interface (DCLK, CS_N, DOUT, DIN, QDIN1, QDIN2)
- 4 external chip select signals
- Support for 3-, 4- or 6-pin SPI interface
- Programmable CS_N to DOUT delay from 0 to 3 DCLKs
- Programmable signal polarities
- Programmable active clock edge
- Software controllable interface allowing for any type of SPI transfer

NOTE

For more information, see *Quad Serial Peripheral Interface* section in the device TRM.

CAUTION

The I/O Timings provided in this section are only valid when all QSPI Chip Selects used in a system are configured to use the same Clock Mode (either Clock Mode 0 or Clock Mode 3).

CAUTION

The I/O Timings provided in this section are valid only for some QSPI usage modes when the corresponding Virtual I/O Timings or Manual I/O Timings are configured as described in the tables found in this section.

Table 7-41 and Table 7-42 Present Timing and Switching Characteristics for Quad SPI Interface.

Table 7-41. Switching Characteristics for QSPI

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
Q1	$t_{c(SCLK)}$	Cycle time, sclk	Default Timing Mode, Clock Mode 0	11.71		ns
			Default Timing Mode, Clock Mode 3	20.8		ns
Q2	$t_{w(SCLKL)}$	Pulse duration, sclk low		Y*P-1 (1)		ns
Q3	$t_{w(SCLKH)}$	Pulse duration, sclk high		Y*P-1 (1)		ns
Q4	$t_{d(CS-SCLK)}$	Delay time, sclk falling edge to cs active edge, CS3:0	Default Timing Mode	-M*P-1.6 (2) (3)	-M*P+2.6 (2) (3)	ns
Q5	$t_{d(SCLK-CS)}$	Delay time, sclk falling edge to cs inactive edge, CS3:0	Default Timing Mode	N*P-1.6 (2) (3)	N*P+2.6 (2) (3)	ns
Q6	$t_{d(SCLK-D0)}$	Delay time, sclk falling edge to d[0] transition	Default Timing Mode	-1.6	2.6	ns
Q7	$t_{ena(CS-D0LZ)}$	Enable time, cs active edge to d[0] driven (lo-z)		-P-3.5	-P+2.5	ns
Q8	$t_{dis(CS-D0Z)}$	Disable time, cs active edge to d[0] tri-stated (hi-z)		-P-2.5	-P+2.0	ns
Q9	$t_{d(SCLK-D0)}$	Delay time, sclk first falling edge to first d[0] transition	PHA=0 Only, Default Timing Mode	-1.6 - P (2)	2.6 - P (2)	ns

(1) The Y parameter is defined as follows:
If DCLK_DIV is 0 or ODD then, Y equals 0.5.
If DCLK_DIV is EVEN then, Y equals (DCLK_DIV/2) / (DCLK_DIV+1).
For best performance, it is recommended to use a DCLK_DIV of 0 or ODD to minimize the duty cycle distortion. The HSDIVIDER on CLKOUTX2_H13 output of DPLL_PER can be used to achieve the desired clock divider ratio. All required details about clock division factor DCLK_DIV can be found in the device-specific Technical Reference Manual.

(2) P = SCLK period.

(3) M=QSPI_SPI_DC_REG.DDx + 1 when Clock Mode 0.
M=QSPI_SPI_DC_REG.DDx when Clock Mode 3.
N = 2 when Clock Mode 0.
N = 3 when Clock Mode 3.

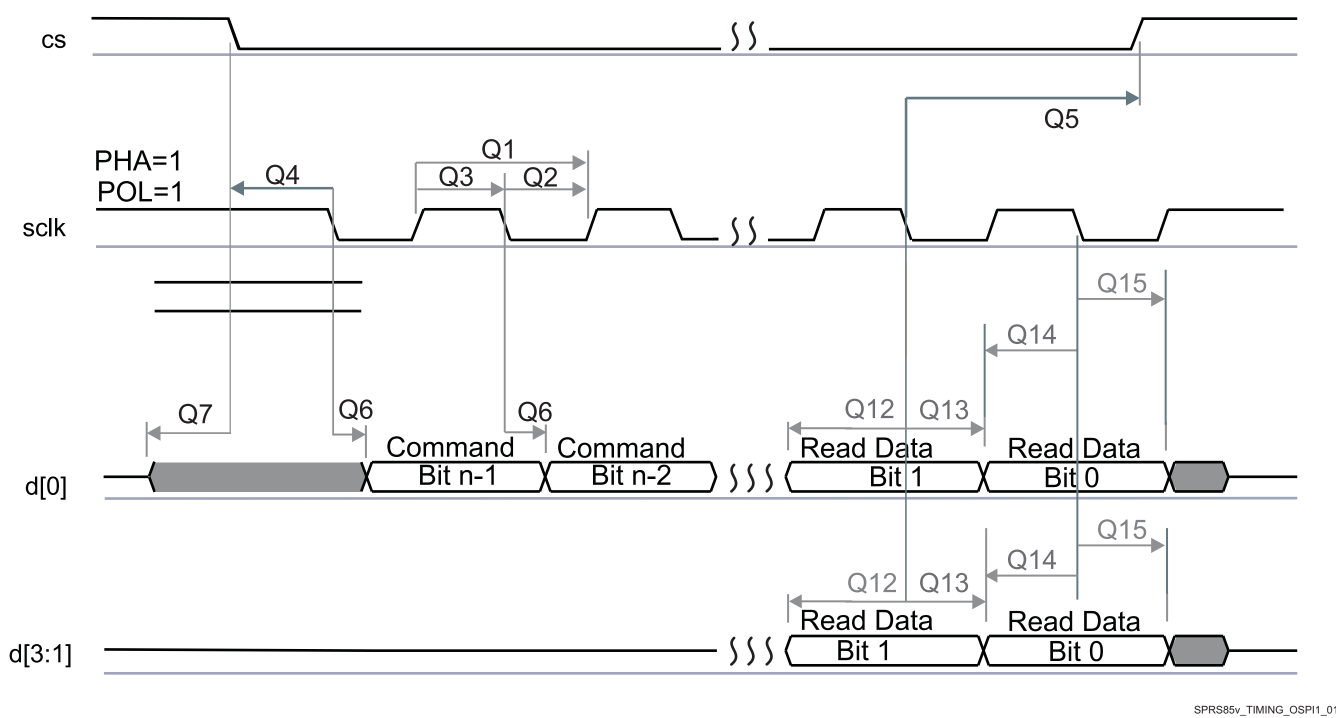


Figure 7-30. QSPI Read (Clock Mode 3)

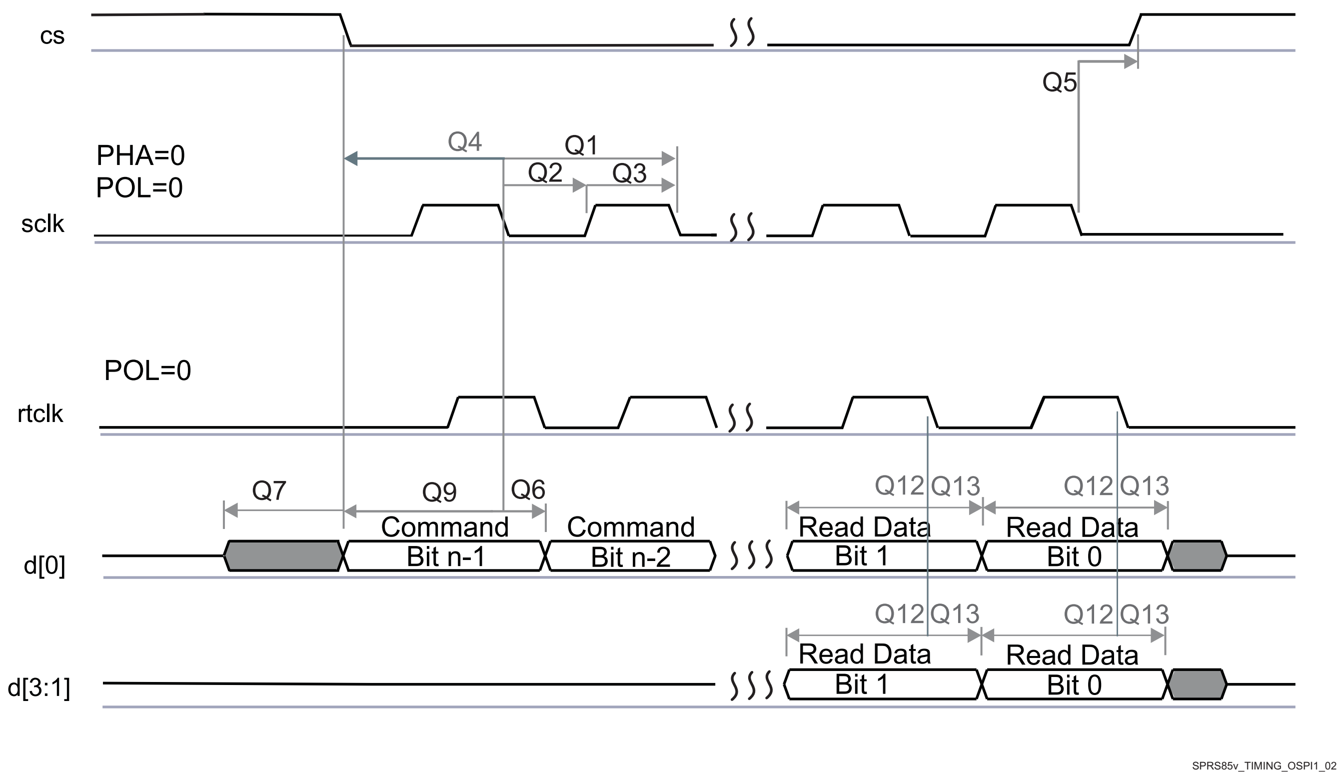


Figure 7-31. QSPI Read (Clock Mode 0)

> **CAUTION**
>
> The I/O Timings provided in this section are valid only for some QSPI usage modes when the corresponding Virtual I/O Timings or Manual I/O Timings are configured as described in the tables found in this section.

Table 7-42. Timing Requirements for QSPI(3)(2)

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
Q12	$t_{su(D-RTCLK)}$	Setup time, d[3:0] valid before falling rtclk edge	Default Timing Mode, Clock Mode 0	4.6		ns
	$t_{su(D-SCLK)}$	Setup time, d[3:0] valid before falling sclk edge	Default Timing Mode, Clock Mode 3	12.3		ns
Q13	$t_{h(RTCLK-D)}$	Hold time, d[3:0] valid after falling rtclk edge	Default Timing Mode, Clock Mode 0	-0.1		ns
	$t_{h(SCLK-D)}$	Hold time, d[3:0] valid after falling sclk edge	Default Timing Mode, Clock Mode 3	0.1		ns
Q14	$t_{su(D-SCLK)}$	Setup time, final d[3:0] bit valid before final falling sclk edge	Default Timing Mode, Clock Mode 3	12.3-P (1)		ns
Q15	$t_{h(SCLK-D)}$	Hold time, final d[3:0] bit valid after final falling sclk edge	Default Timing Mode, Clock Mode 3	0.1+P (1)		ns

(1) P = SCLK period.

(2) Clock Modes 1 and 2 are not supported.

(3) The Device captures data on the falling clock edge in Clock Mode 0 and 3, as opposed to the traditional rising clock edge. Although non-standard, the falling-edge-based setup and hold time timings have been designed to be compatible with standard SPI devices that launch data on the falling edge in Clock Modes 0 and 3.

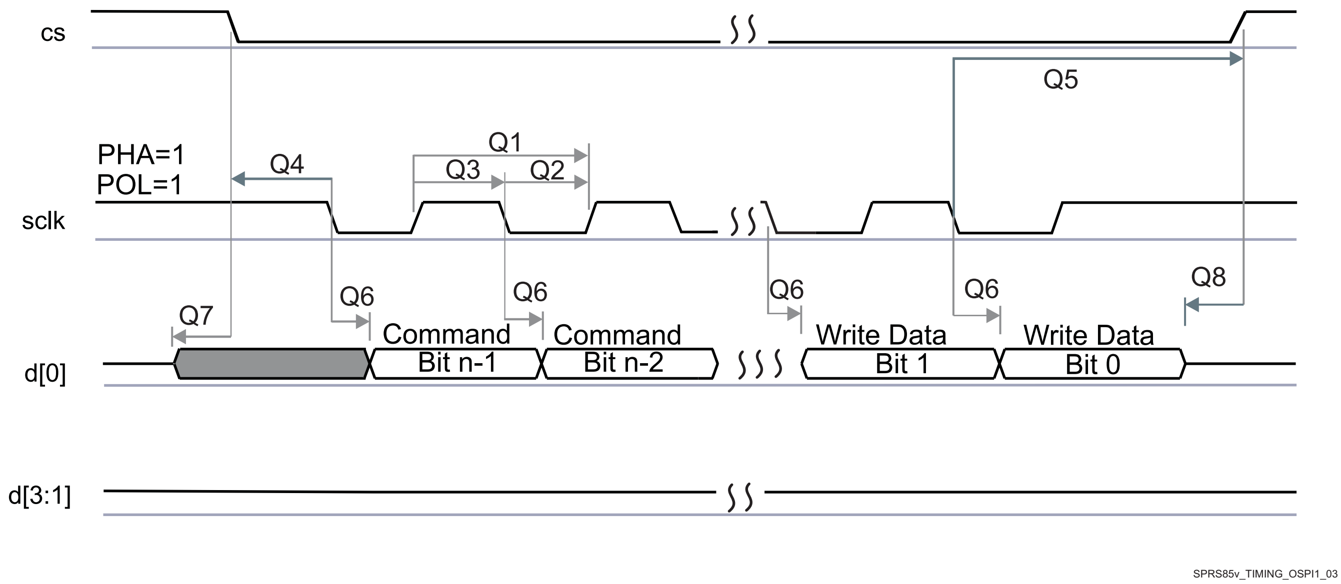


Figure 7-32. QSPI Write (Clock Mode 3)

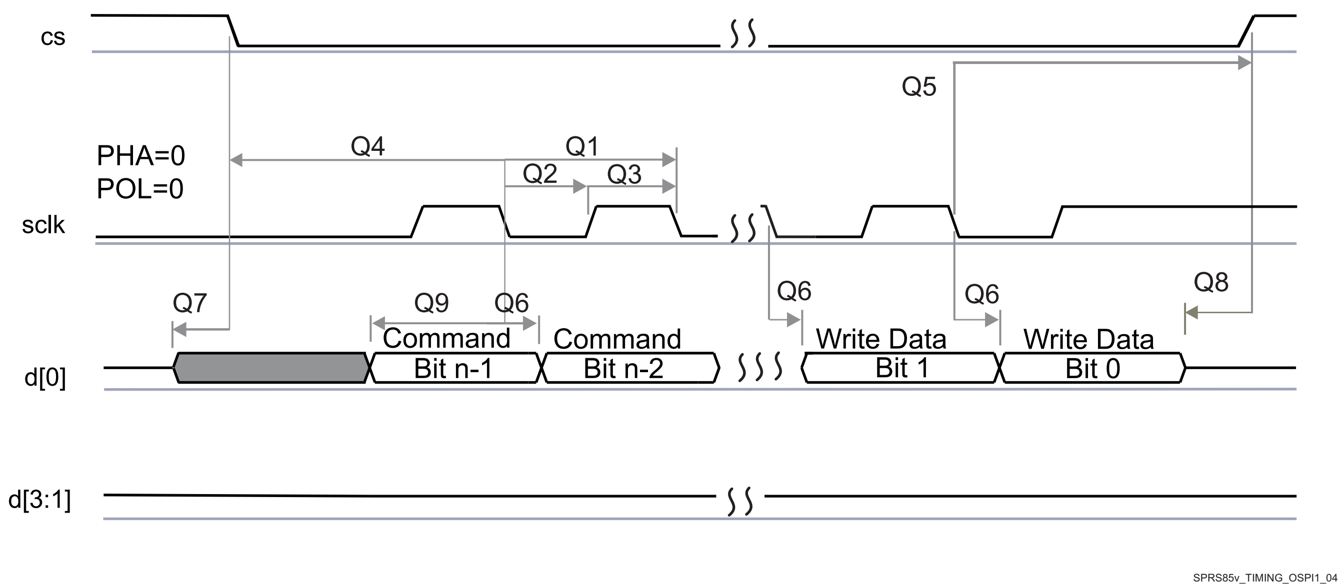


Figure 7-33. QSPI Write (Clock Mode 0)

CAUTION

The I/O Timings provided in this section are valid only for some QSPI usage modes when the corresponding Virtual I/O Timings or Manual I/O Timings are configured as described in the tables found in this section.

NOTE

To configure the desired Manual IO Timing Mode the user must follow the steps described in section Manual IO Timing Modes of the Device TRM.

The associated registers to configure are listed in the **CFG REGISTER** column. For more information see *Control Module* chapter in the device TRM.

Manual IO Timings Modes must be used to ensure some IO timings for QSPI. See Table 7-2 *Modes Summary* for a list of IO timings requiring the use of Manual IO Timings Modes. See Table 7-43 *Manual Functions Mapping for QSPI* for a definition of the Manual modes.

Table 7-43 lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.

Table 7-43. Manual Functions Mapping for QSPI

BALL	BALL NAME	QSPI1_MANUAL1		CFG REGISTER	MUXMODE
		A_DELAY (ps)	G_DELAY (ps)		1
T7	gpmc_a3	0	0	CFG_GPMC_A3_OUT	qspi1_cs2
P6	gpmc_a4	0	0	CFG_GPMC_A4_OUT	qspi1_cs3
R3	gpmc_a13	0	0	CFG_GPMC_A13_IN	qspi1_rtclk
T2	gpmc_a14	2247	1186	CFG_GPMC_A14_IN	qspi1_d3
U2	gpmc_a15	2176	1197	CFG_GPMC_A15_IN	qspi1_d2
U1	gpmc_a16	2229	1268	CFG_GPMC_A16_IN	qspi1_d0
U1	gpmc_a16	0	0	CFG_GPMC_A16_OUT	qspi1_d0
P3	gpmc_a17	2251	1217	CFG_GPMC_A17_IN	qspi1_d1
R2	gpmc_a18	0	0	CFG_GPMC_A18_OUT	qspi1_sclk
P2	gpmc_cs2	0	0	CFG_GPMC_CS2_OUT	qspi1_cs0
P1	gpmc_cs3	0	0	CFG_GPMC_CS3_OUT	qspi1_cs1

7.17 Multichannel Audio Serial Port (McASP)

The multichannel audio serial port (McASP) functions as a general-purpose audio serial port optimized for the needs of multichannel audio applications. The McASP is useful for time-division multiplexed (TDM) stream, Inter-Integrated Sound (I2S) protocols, and intercomponent digital audio interface transmission (DIT).

The device have integrated 8 McASP modules (McASP1-McASP8) with:

- McASP1 and McASP2 modules supporting 16 channels with independent TX/RX clock/sync domain
- McASP3 through McASP8 modules supporting 4 channels with independent TX/RX clock/sync domain

NOTE

For more information, see *Multichannel Audio Serial Port* section in the device TRM.

CAUTION

The I/O Timings provided in this section are valid only for some McASP usage modes when the corresponding Virtual I/O Timings or Manual I/O Timings are configured as described in the tables found in this section.

Table 7-44, Table 7-45, Table 7-46 and Figure 7-34 present Timing Requirements for McASP1 to 8
.

Table 7-44. Timing Requirements for McASP1[(1)]

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
1	$t_{c(AHCLKX)}$	Cycle time, AHCLKX		20		ns
2	$t_{w(AHCLKX)}$	Pulse duration, AHCLKX high or low		0.35P [(2)]		ns
3	$t_{c(ACLKRX)}$	Cycle time, ACLKR/X		20		ns
4	$t_{w(ACLKRX)}$	Pulse duration, ACLKR/X high or low		0.5R - 3 [(3)]		ns
5	$t_{su(AFSRX-ACLK)}$	Setup time, AFSR/X input valid before ACLKR/X	ACLKR/X int	20.5		ns
			ACLKR/X ext in ACLKR/X ext out	4		ns
6	$t_{h(ACLK-AFSRX)}$	Hold time, AFSR/X input valid after ACLKR/X	ACLKR/X int	-1		ns
			ACLKR/X ext in ACLKR/X ext out	1.7		ns
7	$t_{su(AXR-ACLK)}$	Setup time, AXR input valid before ACLKR/X	ACLKR/X int	21.6		ns
			ACLKR/X ext in ACLKR/X ext out	11.5		ns
8	$t_{h(ACLK-AXR)}$	Hold time, AXR input valid after ACLKR/X	ACLKR/X int	-1		ns
			ACLKR/X ext in ACLKR/X ext out	1.8		ns

(1) ACLKR internal: ACLKRCTL.CLKRM=1, PDIR.ACLKR = 1
ACLKR external input: ACLKRCTL.CLKRM=0, PDIR.ACLKR=0
ACLKR external output: ACLKRCTL.CLKRM=0, PDIR.ACLKR=1
ACLKX internal: ACLKXCTL.CLKXM=1, PDIR.ACLKX = 1
ACLKX external input: ACLKXCTL.CLKXM=0, PDIR.ACLKX=0
ACLKX external output: ACLKXCTL.CLKXM=0, PDIR.ACLKX=1

(2) P = AHCLKX period in ns.

(3) R = ACLKR/X period in ns.

Table 7-45. Timing Requirements for McASP2[(1)]

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
1	$t_{c(AHCLKX)}$	Cycle time, AHCLKX		20		ns
2	$t_{w(AHCLKX)}$	Pulse duration, AHCLKX high or low		0.35P [(2)]		ns
3	$t_{c(ACLKRX)}$	Cycle time, ACLKR/X	Any Other Conditions	20		ns
			ACLKX/AFSX (In Sync Mode), ACLKR/AFSR (In Async Mode), and AXR are all inputs "80M" Virtual IO Timing Modes	12.5		ns
4	$t_{w(ACLKRX)}$	Pulse duration, ACLKR/X high or low	Any Other Conditions	0.5R - 3 [(3)]		ns
			ACLKX/AFSX (In Sync Mode), ACLKR/AFSR (In Async Mode), and AXR are all inputs "80M" Virtual IO Timing Modes	0.38R [(3)]		ns
5	$t_{su(AFSRX-ACLK)}$	Setup time, AFSR/X input valid before ACLKR/X	ACLKR/X int	20.3		ns
			ACLKR/X ext in ACLKR/X ext out	4.5		ns
			ACLKR/X ext in ACLKR/X ext out "80M" Virtual IO Timing Modes	3		ns

Table 7-45. Timing Requirements for McASP2(1) (continued)

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
6	$t_{h(ACLK-AFSRX)}$	Hold time, AFSR/X input valid after ACLKR/X	ACLKR/X int	-1		ns
			ACLKR/X ext in ACLKR/X ext out	1.8		ns
			ACLKR/X ext in ACLKR/X ext out "80M" Virtual IO Timing Modes	3		ns
7	$t_{su(AXR-ACLK)}$	Setup time, AXR input valid before ACLKR/X	ACLKR/X int	21.1		ns
			ACLKR/X ext in ACLKR/X ext out	4.5		ns
			ACLKR/X ext in ACLKR/X ext out "80M" Virtual IO Timing Modes	3		ns
8	$t_{h(ACLK-AXR)}$	Hold time, AXR input valid after ACLKR/X	ACLKR/X int	-1		ns
			ACLKR/X ext in ACLKR/X ext out	1.8		ns
			ACLKR/X ext in ACLKR/X ext out "80M" Virtual IO Timing Modes	3		ns

(1) ACLKR internal: ACLKRCTL.CLKRM=1, PDIR.ACLKR = 1
ACLKR external input: ACLKRCTL.CLKRM=0, PDIR.ACLKR=0
ACLKR external output: ACLKRCTL.CLKRM=0, PDIR.ACLKR=1
ACLKX internal: ACLKXCTL.CLKXM=1, PDIR.ACLKX = 1
ACLKX external input: ACLKXCTL.CLKXM=0, PDIR.ACLKX=0
ACLKX external output: ACLKXCTL.CLKXM=0, PDIR.ACLKX=1

(2) P = AHCLKX period in ns.

(3) R = ACLKR/X period in ns.

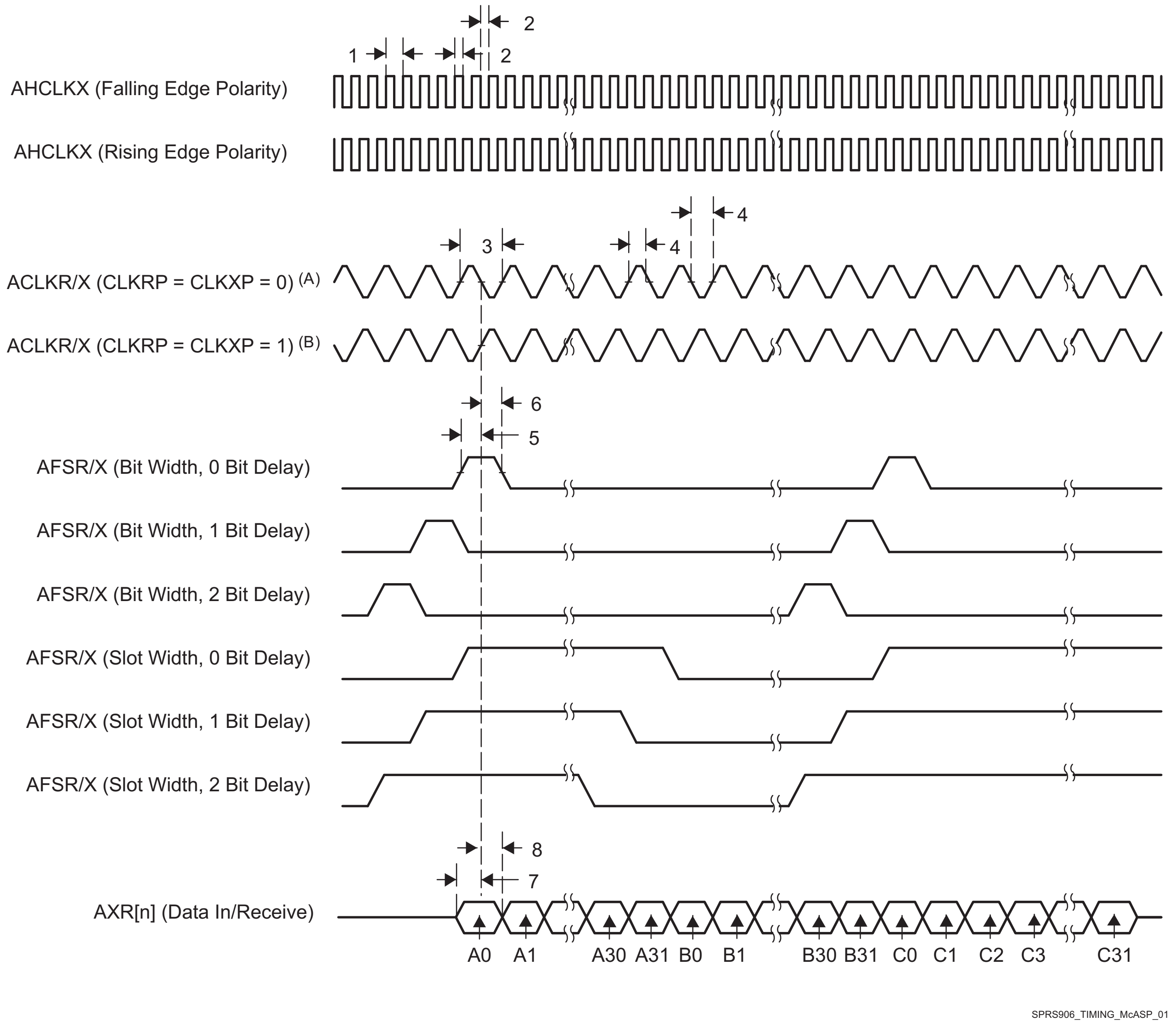
Table 7-46. Timing Requirements for McASP3/4/5/6/7/8(1)

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
1	$t_{c(AHCLKX)}$	Cycle time, AHCLKX		20		ns
2	$t_{w(AHCLKX)}$	Pulse duration, AHCLKX high or low		0.35P (2)		ns
3	$t_{c(ACLKRX)}$	Cycle time, ACLKR/X		20		ns
4	$t_{w(ACLKRX)}$	Pulse duration, ACLKR/X high or low		0.5R - 3 (3)		ns
5	$t_{su(AFSRX-ACLK)}$	Setup time, AFSR/X input valid before ACLKR/X	ACLKR/X int	19.7		ns
			ACLKR/X ext in ACLKR/X ext out	5.6		ns
6	$t_{h(ACLK-AFSRX)}$	Hold time, AFSR/X input valid after ACLKR/X	ACLKR/X int	-1.1		ns
			ACLKR/X ext in ACLKR/X ext out	2.5		ns
	$t_{su(AXR-ACLK)}$	Setup time, AXR input valid before ACLKX	ACLKX int (ASYNC=0)	20.3		ns
			ACLKR/X ext in ACLKR/X ext out	5.1		ns
8	$t_{h(ACLK-AXR)}$	Hold time, AXR input valid after ACLKX	ACLKX int (ASYNC=0)	-0.8		ns
			ACLKR/X ext in ACLKR/X ext out	2.5		ns

(1) ACLKR internal: ACLKRCTL.CLKRM=1, PDIR.ACLKR = 1 (NOT SUPPORTED)
ACLKR external input: ACLKRCTL.CLKRM=0, PDIR.ACLKR=0
ACLKR external output: ACLKRCTL.CLKRM=0, PDIR.ACLKR=1
ACLKX internal: ACLKXCTL.CLKXM=1, PDIR.ACLKX = 1
ACLKX external input: ACLKXCTL.CLKXM=0, PDIR.ACLKX=0
ACLKX external output: ACLKXCTL.CLKXM=0, PDIR.ACLKX=1

(2) P = AHCLKX period in ns.

(3) R = ACLKR/X period in ns.



A. For CLKRP = CLKXP = 0, the McASP transmitter is configured for rising edge (to shift data out) and the McASP receiver is configured for falling edge (to shift data in).

B. For CLKRP = CLKXP = 1, the McASP transmitter is configured for falling edge (to shift data out) and the McASP receiver is configured for rising edge (to shift data in).

Figure 7-34. McASP Input Timing

Table 7-47, Table 7-48, Table 7-49 and Figure 7-35 present Switching Characteristics Over Recommended Operating Conditions for McASP1 to 8.

Table 7-47. Switching Characteristics Over Recommended Operating Conditions for McASP1[(1)]

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
9	$t_{c(AHCLKX)}$	Cycle time, AHCLKX		20		ns
10	$t_{w(AHCLKX)}$	Pulse duration, AHCLKX high or low		0.5P - 2.5 [(2)]		ns
11	$t_{c(ACLKRX)}$	Cycle time, ACLKR/X		20		ns

Table 7-47. Switching Characteristics Over Recommended Operating Conditions for McASP1[(1)] (continued)

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
12	$t_{w(ACLKRX)}$	Pulse duration, ACLKR/X high or low		0.5P - 2.5 [(3)]		ns
13	$t_{d(ACLK-AFSXR)}$	Delay time, ACLKR/X transmit edge to AFSX/R output valid	ACLKR/X int	-0.9	6	ns
			ACLKR/X ext in ACLKR/X ext out	2	23.1	ns
14	$t_{d(ACLK-AXR)}$	Delay time, ACLKR/X transmit edge to AXR output valid	ACLKR/X int	-1.4	6	ns
			ACLKR/X ext in ACLKR/X ext out	2	24.2	ns

(1) ACLKR internal: ACLKRCTL.CLKRM=1, PDIR.ACLKR = 1
ACLKR external input: ACLKRCTL.CLKRM=0, PDIR.ACLKR=0
ACLKR external output: ACLKRCTL.CLKRM=0, PDIR.ACLKR=1
ACLKX internal: ACLKXCTL.CLKXM=1, PDIR.ACLKX = 1
ACLKX external input: ACLKXCTL.CLKXM=0, PDIR.ACLKX=0
ACLKX external output: ACLKXCTL.CLKXM=0, PDIR.ACLKX=1

(2) P = AHCLKX period in ns.

(3) R = ACLKR/X period in ns.

Table 7-48. Switching Characteristics Over Recommended Operating Conditions for McASP2 [(1)]

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
9	$t_{c(AHCLKX)}$	Cycle time, AHCLKX		20		ns
10	$t_{w(AHCLKX)}$	Pulse duration, AHCLKX high or low		0.5P - 2.5 [(2)]		ns
11	$t_{c(ACLKRX)}$	Cycle time, ACLKR/X		20		ns
12	$t_{w(ACLKRX)}$	Pulse duration, ACLKR/X high or low		0.5P - 2.5 [(3)]		ns
13	$t_{d(ACLK-AFSXR)}$	Delay time, ACLKR/X transmit edge to AFSX/R output valid	ACLKR/X int	-1	6	ns
			ACLKR/X ext in ACLKR/X ext out	2	23.2	ns
14	$t_{d(ACLK-AXR)}$	Delay time, ACLKR/X transmit edge to AXR output valid	ACLKR/X int	-1.3	6	ns
			ACLKR/X ext in ACLKR/X ext out	2	23.7	ns

(1) ACLKR internal: ACLKRCTL.CLKRM=1, PDIR.ACLKR = 1
ACLKR external input: ACLKRCTL.CLKRM=0, PDIR.ACLKR=0
ACLKR external output: ACLKRCTL.CLKRM=0, PDIR.ACLKR=1
ACLKX internal: ACLKXCTL.CLKXM=1, PDIR.ACLKX = 1
ACLKX external input: ACLKXCTL.CLKXM=0, PDIR.ACLKX=0
ACLKX external output: ACLKXCTL.CLKXM=0, PDIR.ACLKX=1

(2) P = AHCLKX period in ns.

(3) R = ACLKR/X period in ns.

Table 7-49. Switching Characteristics Over Recommended Operating Conditions for McASP3/4/5/6/7/8[(1)]

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
9	$t_{c(AHCLKX)}$	Cycle time, AHCLKX		20		ns
10	$t_{w(AHCLKX)}$	Pulse duration, AHCLKX high or low		0.5P - 2.5 [(2)]		ns
11	$t_{c(ACLKRX)}$	Cycle time, ACLKR/X		20		ns
12	$t_{w(ACLKRX)}$	Pulse duration, ACLKR/X high or low		0.5P - 2.5 [(3)]		ns

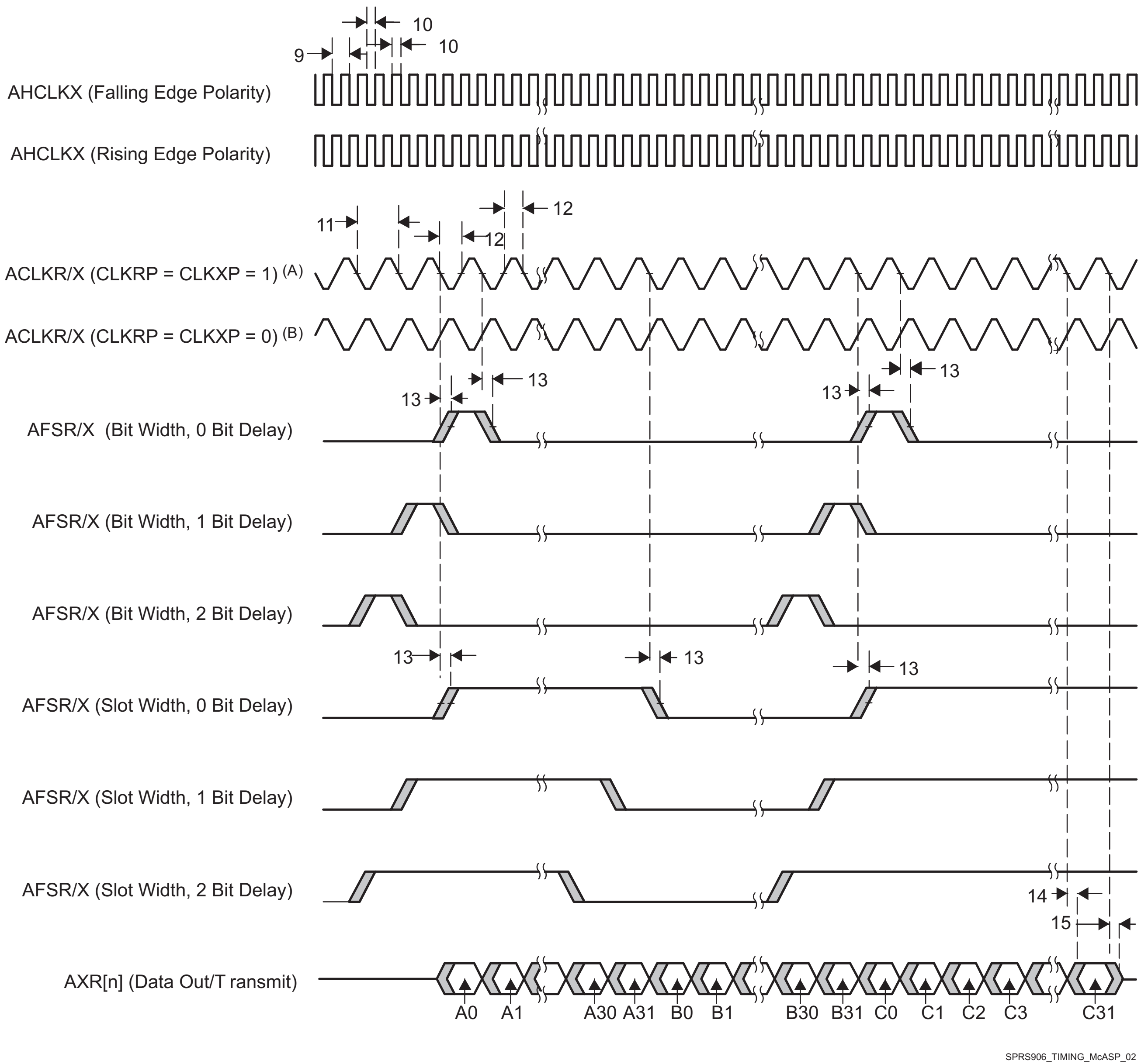
Table 7-49. Switching Characteristics Over Recommended Operating Conditions for McASP3/4/5/6/7/8(1) (continued)

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
13	$t_{d(ACLK-AFSXR)}$	Delay time, ACLKR/X transmit edge to AFSX/R output valid	ACLKR/X int	-0.5	6	ns
			ACLKR/X ext in ACLKR/X ext out	1.9	24.5	ns
14	$t_{d(ACLK-AXR)}$	Delay time, ACLKR/X transmit edge to AXR output valid	ACLKR/X int	-1.4	7.1	ns
			ACLKR/X ext in ACLKR/X ext out	1.1	24.2	ns

(1) ACLKR internal: ACLKRCTL.CLKRM=1, PDIR.ACLKR = 1
ACLKR external input: ACLKRCTL.CLKRM=0, PDIR.ACLKR=0
ACLKR external output: ACLKRCTL.CLKRM=0, PDIR.ACLKR=1
ACLKX internal: ACLKXCTL.CLKXM=1, PDIR.ACLKX = 1
ACLKX external input: ACLKXCTL.CLKXM=0, PDIR.ACLKX=0
ACLKX external output: ACLKXCTL.CLKXM=0, PDIR.ACLKX=1

(2) P = AHCLKX period in ns.

(3) R = ACLKR/X period in ns.



A. For CLKRP = CLKXP = 1, the McASP transmitter is configured for falling edge (to shift data out) and the McASP receiver is configured for rising edge (to shift data in).

B. For CLKRP = CLKXP = 0, the McASP transmitter is configured for rising edge (to shift data out) and the McASP receiver is configured for falling edge (to shift data in).

Figure 7-35. McASP Output Timing

Table 7-50 through Table 7-57 explain all cases with Virtual Mode Details for McASP1/2/3/4/5/6/7/8 (see Figure 7-36 through Figure 7-43).

Table 7-50. Virtual Mode Case Details for McASP1

No.	CASE	CASE Description	Virtual Mode Settings		Notes
			Signals	Virtual Mode Value	
IP Mode : ASYNC					
1	COIFOI	CLKX / FSX: Output CLKR / FSR: Input	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 7-36
			AXR(Inputs)/CLKR/FSR	MCASP1_VIRTUAL2_ASYNC_RX	

Table 7-50. Virtual Mode Case Details for McASP1 (continued)

No.	CASE	CASE Description	Virtual Mode Settings		Notes
			Signals	Virtual Mode Value	
2	COIFIO	CLKX / FSR: Output CLKR / FSX: Input	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 7-37
			AXR(Inputs)/CLKR/FSR	MCASP1_VIRTUAL2_ASYNC_RX	
3	CIOFIO	CLKR / FSR: Output CLKX / FSX: Input	AXR(Outputs)/CLKX/FSX	MCASP1_VIRTUAL2_ASYNC_RX	See Figure 7-38
			AXR(Inputs)/CLKR/FSR	Default (No Virtual Mode)	
4	CIOFOI	CLKR / FSX: Output CLKX / FSR: Input	AXR(Outputs)/CLKX/FSX	MCASP1_VIRTUAL2_ASYNC_RX	See Figure 7-39
			AXR(Inputs)/CLKR/FSR	Default (No Virtual Mode)	
IP Mode : SYNC (CLKR / FSR internally generated from CLKX / FSX)					
5	CO-FO-	CLKX / FSX: Output	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 7-40
			AXR(Inputs)/CLKX/FSX	Default (No Virtual Mode)	
6	CI-FO-	FSX: Output CLKX: Input	AXR(Outputs)/CLKX/FSX	MCASP1_VIRTUAL1_SYNC_RX	See Figure 7-41
			AXR(Inputs)/CLKX/FSX	MCASP1_VIRTUAL1_SYNC_RX	
7	CI-FI-	CLKX / FSX: Input	AXR(Outputs)/CLKX/FSX	MCASP1_VIRTUAL1_SYNC_RX	See Figure 7-42
			AXR(Inputs)/CLKX/FSX	MCASP1_VIRTUAL1_SYNC_RX	
8	CO-FI-	CLKX: Output FSX: Input	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 7-43
			AXR(Inputs)/CLKX/FSX	Default (No Virtual Mode)	

Table 7-51. Virtual Mode Case Details for McASP2

No.	CASE	CASE Description	Virtual Mode Settings		Notes
			Signals	Virtual Mode Value	
IP Mode : ASYNC					
1	COIFOI	CLKX / FSX: Output CLKR / FSR: Input	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)(1)	See Figure 7-36
			AXR(Inputs)/CLKR/FSR	Default (No Virtual Mode)(1)	
			AXR(Inputs)/CLKR/FSR	MCASP2_VIRTUAL4_ASYNC_RX_80M (2)	
2	COIFIO	CLKX / FSR: Output CLKR / FSX: Input	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 7-37
			AXR(Inputs)/CLKR/FSR	MCASP2_VIRTUAL2_ASYNC_RX	
3	CIOFIO	CLKR / FSR: Output CLKX / FSX: Input	AXR(Outputs)/CLKX/FSX	MCASP2_VIRTUAL2_ASYNC_RX	See Figure 7-38
			AXR(Inputs)/CLKR/FSR	Default (No Virtual Mode)	
4	CIOFOI	CLKR / FSX: Output CLKX / FSR: Input	AXR(Outputs)/CLKX/FSX	MCASP2_VIRTUAL2_ASYNC_RX	See Figure 7-39
			AXR(Inputs)/CLKR/FSR	Default (No Virtual Mode)	
IP Mode : SYNC (CLKR / FSR internally generated from CLKX / FSX)					
5	CO-FO-	CLKX / FSX: Output	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 7-40
			AXR(Inputs)/CLKX/FSX	Default (No Virtual Mode)	
6	CI-FO-	FSX: Output CLKX: Input	AXR(Outputs)/CLKX/FSX	MCASP2_VIRTUAL3_SYNC_RX	See Figure 7-41
			AXR(Inputs)/CLKX/FSX	MCASP2_VIRTUAL3_SYNC_RX	
7	CI-FI-	CLKX / FSX: Input	AXR(Outputs)/CLKX/FSX	MCASP2_VIRTUAL3_SYNC_RX(1)	See Figure 7-42
			AXR(Inputs)/CLKX/FSX	MCASP2_VIRTUAL3_SYNC_RX(1)	
			AXR(Inputs)/CLKX/FSX	MCASP2_VIRTUAL1_SYNC_RX_80M(2)	
8	CO-FI-	CLKX: Output FSX: Input	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 7-43
			AXR(Inputs)/CLKX/FSX	Default (No Virtual Mode)	

(1) Used up to 50MHz. Should also be used in a CI-FI- mixed case where AXR operate as both inputs and outputs (that is, AXR are bidirectional).

(2) Used in 80MHz input only mode when AXR, CLKX and FSX are all inputs.

Table 7-52. Virtual Mode Case Details for McASP3

No.	CASE	CASE Description	Virtual Mode Settings		Notes
			Signals	Virtual Mode Value	
IP Mode : ASYNC					
1	COIFOI	CLKX / FSX: Output CLKR / FSR: Input	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 7-36
			AXR(Inputs)/CLKR/FSR	MCASP3_VIRTUAL2_SYNC_RX	
2	COIFIO	CLKX / FSR: Output CLKR / FSX: Input	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 7-37
			AXR(Inputs)/CLKR/FSR	MCASP3_VIRTUAL2_SYNC_RX	
3	CIOFIO	CLKR / FSR: Output CLKX / FSX: Input	AXR(Outputs)/CLKX/FSX	MCASP3_VIRTUAL2_SYNC_RX	See Figure 7-38
			AXR(Inputs)/CLKR/FSR	MCASP3_VIRTUAL2_SYNC_RX	
4	CIOFOI	CLKR / FSX: Output CLKX / FSR: Input	AXR(Outputs)/CLKX/FSX	MCASP3_VIRTUAL2_SYNC_RX	See Figure 7-39
			AXR(Inputs)/CLKR/FSR	MCASP3_VIRTUAL2_SYNC_RX	
IP Mode : SYNC (CLKR / FSR internally generated from CLKX / FSX)					
5	CO-FO-	CLKX / FSX: Output	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 7-40
			AXR(Inputs)/CLKX/FSX	Default (No Virtual Mode)	
6	CI-FO-	FSX: Output CLKX: Input	AXR(Outputs)/CLKX/FSX	MCASP3_VIRTUAL2_SYNC_RX	See Figure 7-41
			AXR(Inputs)/CLKX/FSX	MCASP3_VIRTUAL2_SYNC_RX	
7	CI-FI-	CLKX / FSX: Input	AXR(Outputs)/CLKX/FSX	MCASP3_VIRTUAL2_SYNC_RX	See Figure 7-42
			AXR(Inputs)/CLKX/FSX	MCASP3_VIRTUAL2_SYNC_RX	
8	CO-FI-	CLKX: Output FSX: Input	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 7-43
			AXR(Inputs)/CLKX/FSX	Default (No Virtual Mode)	

Table 7-53. Virtual Mode Case Details for McASP4

No.	CASE	CASE Description	Virtual Mode Settings		Notes
			Signals	Virtual Mode Value	
IP Mode : ASYNC					
1	COIFOI	CLKX / FSX: Output CLKR / FSR: Input	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 7-36
			AXR(Inputs)/CLKR/FSR	MCASP4_VIRTUAL1_SYNC_RX	
2	COIFIO	CLKX / FSR: Output CLKR / FSX: Input	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 7-37
			AXR(Inputs)/CLKR/FSR	MCASP4_VIRTUAL1_SYNC_RX	
3	CIOFIO	CLKR / FSR: Output CLKX / FSX: Input	AXR(Outputs)/CLKX/FSX	MCASP4_VIRTUAL1_SYNC_RX	See Figure 7-38
			AXR(Inputs)/CLKR/FSR	MCASP4_VIRTUAL1_SYNC_RX	
4	CIOFOI	CLKR / FSX: Output CLKX / FSR: Input	AXR(Outputs)/CLKX/FSX	MCASP4_VIRTUAL1_SYNC_RX	See Figure 7-39
			AXR(Inputs)/CLKR/FSR	MCASP4_VIRTUAL1_SYNC_RX	
IP Mode : SYNC (CLKR / FSR internally generated from CLKX / FSX)					
5	CO-FO-	CLKX / FSX: Output	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 7-40
			AXR(Inputs)/CLKX/FSX	Default (No Virtual Mode)	
6	CI-FO-	FSX: Output CLKX: Input	AXR(Outputs)/CLKX/FSX	MCASP4_VIRTUAL1_SYNC_RX	See Figure 7-41
			AXR(Inputs)/CLKX/FSX	MCASP4_VIRTUAL1_SYNC_RX	
7	CI-FI-	CLKX / FSX: Input	AXR(Outputs)/CLKX/FSX	MCASP4_VIRTUAL1_SYNC_RX	See Figure 7-42
			AXR(Inputs)/CLKX/FSX	MCASP4_VIRTUAL1_SYNC_RX	

Table 7-53. Virtual Mode Case Details for McASP4 (continued)

No.	CASE	CASE Description	Virtual Mode Settings		Notes
			Signals	Virtual Mode Value	
8	CO-FI-	CLKX: Output FSX: Input	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 7-43
			AXR(Inputs)/CLKX/FSX	Default (No Virtual Mode)	

Table 7-54. Virtual Mode Case Details for McASP5

No.	CASE	CASE Description	Virtual Mode Settings		Notes
			Signals	Virtual Mode Value	
IP Mode : ASYNC					
1	COIFOI	CLKX / FSX: Output CLKR / FSR: Input	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 7-36
			AXR(Inputs)/CLKR/FSR	MCASP5_VIRTUAL1_SYNC_RX	
2	COIFIO	CLKX / FSR: Output CLKR / FSX: Input	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 7-37
			AXR(Inputs)/CLKR/FSR	MCASP5_VIRTUAL1_SYNC_RX	
3	CIOFIO	CLKR / FSR: Output CLKX / FSX: Input	AXR(Outputs)/CLKX/FSX	MCASP5_VIRTUAL1_SYNC_RX	See Figure 7-38
			AXR(Inputs)/CLKR/FSR	MCASP5_VIRTUAL1_SYNC_RX	
4	CIOFOI	CLKR / FSX: Output CLKX / FSR: Input	AXR(Outputs)/CLKX/FSX	MCASP5_VIRTUAL1_SYNC_RX	See Figure 7-39
			AXR(Inputs)/CLKR/FSR	MCASP5_VIRTUAL1_SYNC_RX	
IP Mode : SYNC (CLKR / FSR internally generated from CLKX / FSX)					
5	CO-FO-	CLKX / FSX: Output	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 7-40
			AXR(Inputs)/CLKX/FSX	Default (No Virtual Mode)	
6	CI-FO-	FSX: Output CLKX: Input	AXR(Outputs)/CLKX/FSX	MCASP5_VIRTUAL1_SYNC_RX	See Figure 7-41
			AXR(Inputs)/CLKX/FSX	MCASP5_VIRTUAL1_SYNC_RX	
7	CI-FI-	CLKX / FSX: Input	AXR(Outputs)/CLKX/FSX	MCASP5_VIRTUAL1_SYNC_RX	See Figure 7-42
			AXR(Inputs)/CLKX/FSX	MCASP5_VIRTUAL1_SYNC_RX	
8	CO-FI-	CLKX: Output FSX: Input	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 7-43
			AXR(Inputs)/CLKX/FSX	Default (No Virtual Mode)	

Table 7-55. Virtual Mode Case Details for McASP6

No.	CASE	CASE Description	Virtual Mode Settings		Notes
			Signals	Virtual Mode Value	
IP Mode : ASYNC					
1	COIFOI	CLKX / FSX: Output CLKR / FSR: Input	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 7-36
			AXR(Inputs)/CLKR/FSR	MCASP6_VIRTUAL1_SYNC_RX	
2	COIFIO	CLKX / FSR: Output CLKR / FSX: Input	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 7-37
			AXR(Inputs)/CLKR/FSR	MCASP6_VIRTUAL1_SYNC_RX	
3	CIOFIO	CLKR / FSR: Output CLKX / FSX: Input	AXR(Outputs)/CLKX/FSX	MCASP6_VIRTUAL1_SYNC_RX	See Figure 7-38
			AXR(Inputs)/CLKR/FSR	MCASP6_VIRTUAL1_SYNC_RX	
4	CIOFOI	CLKR / FSX: Output CLKX / FSR: Input	AXR(Outputs)/CLKX/FSX	MCASP6_VIRTUAL1_SYNC_RX	See Figure 7-39
			AXR(Inputs)/CLKR/FSR	MCASP6_VIRTUAL1_SYNC_RX	
IP Mode : SYNC (CLKR / FSR internally generated from CLKX / FSX)					
5	CO-FO-	CLKX / FSX: Output	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 7-40
			AXR(Inputs)/CLKX/FSX	Default (No Virtual Mode)	

Table 7-55. Virtual Mode Case Details for McASP6 (continued)

No.	CASE	CASE Description	Virtual Mode Settings		Notes
			Signals	Virtual Mode Value	
6	CI-FO-	FSX: Output CLKX: Input	AXR(Outputs)/CLKX/FSX	MCASP6_VIRTUAL1_SYNC_RX	See Figure 7-41
			AXR(Inputs)/CLKX/FSX	MCASP6_VIRTUAL1_SYNC_RX	
7	CI-FI-	CLKX / FSX: Input	AXR(Outputs)/CLKX/FSX	MCASP6_VIRTUAL1_SYNC_RX	See Figure 7-42
			AXR(Inputs)/CLKX/FSX	MCASP6_VIRTUAL1_SYNC_RX	
8	CO-FI-	CLKX: Output FSX: Input	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 7-43
			AXR(Inputs)/CLKX/FSX	Default (No Virtual Mode)	

Table 7-56. Virtual Mode Case Details for McASP7

No.	CASE	CASE Description	Virtual Mode Settings		Notes
			Signals	Virtual Mode Value	
IP Mode : ASYNC					
1	COIFOI	CLKX / FSX: Output CLKR / FSR: Input	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 7-36
			AXR(Inputs)/CLKR/FSR	MCASP7_VIRTUAL2_SYNC_RX	
2	COIFIO	CLKX / FSR: Output CLKR / FSX: Input	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 7-37
			AXR(Inputs)/CLKR/FSR	MCASP7_VIRTUAL2_SYNC_RX	
3	CIOFIO	CLKR / FSR: Output CLKX / FSX: Input	AXR(Outputs)/CLKX/FSX	MCASP7_VIRTUAL2_SYNC_RX	See Figure 7-38
			AXR(Inputs)/CLKR/FSR	MCASP7_VIRTUAL2_SYNC_RX	
4	CIOFOI	CLKR / FSX: Output CLKX / FSR: Input	AXR(Outputs)/CLKX/FSX	MCASP7_VIRTUAL2_SYNC_RX	See Figure 7-39
			AXR(Inputs)/CLKR/FSR	MCASP7_VIRTUAL2_SYNC_RX	
IP Mode : SYNC (CLKR / FSR internally generated from CLKX / FSX)					
5	CO-FO-	CLKX / FSX: Output	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 7-40
			AXR(Inputs)/CLKX/FSX	Default (No Virtual Mode)	
6	CI-FO-	FSX: Output CLKX: Input	AXR(Outputs)/CLKX/FSX	MCASP7_VIRTUAL2_SYNC_RX	See Figure 7-41
			AXR(Inputs)/CLKX/FSX	MCASP7_VIRTUAL2_SYNC_RX	
7	CI-FI-	CLKX / FSX: Input	AXR(Outputs)/CLKX/FSX	MCASP7_VIRTUAL2_SYNC_RX	See Figure 7-42
			AXR(Inputs)/CLKX/FSX	MCASP7_VIRTUAL2_SYNC_RX	
8	CO-FI-	CLKX: Output FSX: Input	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 7-43
			AXR(Inputs)/CLKX/FSX	Default (No Virtual Mode)	

Table 7-57. Virtual Mode Case Details for McASP8

No.	CASE	CASE Description	Virtual Mode Settings		Notes
			Signals	Virtual Mode Value	
IP Mode : ASYNC					
1	COIFOI	CLKX / FSX: Output CLKR / FSR: Input	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 7-36
			AXR(Inputs)/CLKR/FSR	MCASP8_VIRTUAL1_SYNC_RX	
2	COIFIO	CLKX / FSR: Output CLKR / FSX: Input	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 7-37
			AXR(Inputs)/CLKR/FSR	MCASP8_VIRTUAL1_SYNC_RX	
3	CIOFIO	CLKR / FSR: Output CLKX / FSX: Input	AXR(Outputs)/CLKX/FSX	MCASP8_VIRTUAL1_SYNC_RX	See Figure 7-38
			AXR(Inputs)/CLKR/FSR	MCASP8_VIRTUAL1_SYNC_RX	

Table 7-57. Virtual Mode Case Details for McASP8 (continued)

No.	CASE	CASE Description	Virtual Mode Settings		Notes
			Signals	Virtual Mode Value	
4	CIOFOI	CLKR / FSX: Output CLKX / FSR: Input	AXR(Outputs)/CLKX/FSX	MCASP8_VIRTUAL1_SYNC_RX	See Figure 7-39
			AXR(Inputs)/CLKR/FSR	MCASP8_VIRTUAL1_SYNC_RX	
IP Mode : SYNC (CLKR / FSR internally generated from CLKX / FSX)					
5	CO-FO-	CLKX / FSX: Output	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 7-40
			AXR(Inputs)/CLKX/FSX	Default (No Virtual Mode)	
6	CI-FO-	FSX: Output CLKX: Input	AXR(Outputs)/CLKX/FSX	MCASP8_VIRTUAL1_SYNC_RX	See Figure 7-41
			AXR(Inputs)/CLKX/FSX	MCASP8_VIRTUAL1_SYNC_RX	
7	CI-FI-	CLKX / FSX: Input	AXR(Outputs)/CLKX/FSX	MCASP8_VIRTUAL1_SYNC_RX	See Figure 7-42
			AXR(Inputs)/CLKX/FSX	MCASP8_VIRTUAL1_SYNC_RX	
8	CO-FI-	CLKX: Output FSX: Input	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 7-43
			AXR(Inputs)/CLKX/FSX	Default (No Virtual Mode)	

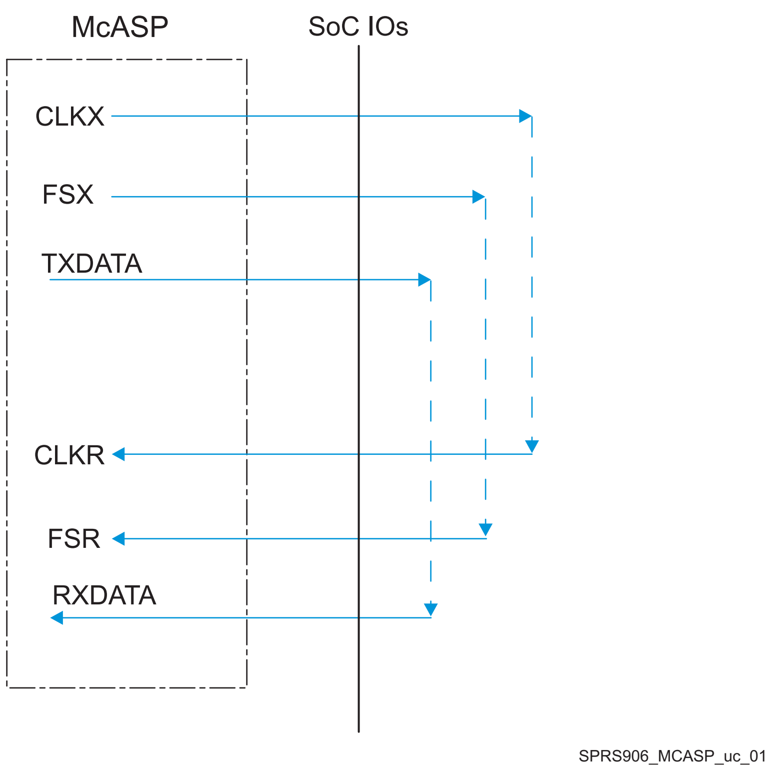


Figure 7-36. McASP1-8 COIFOI - ASYNC Mode

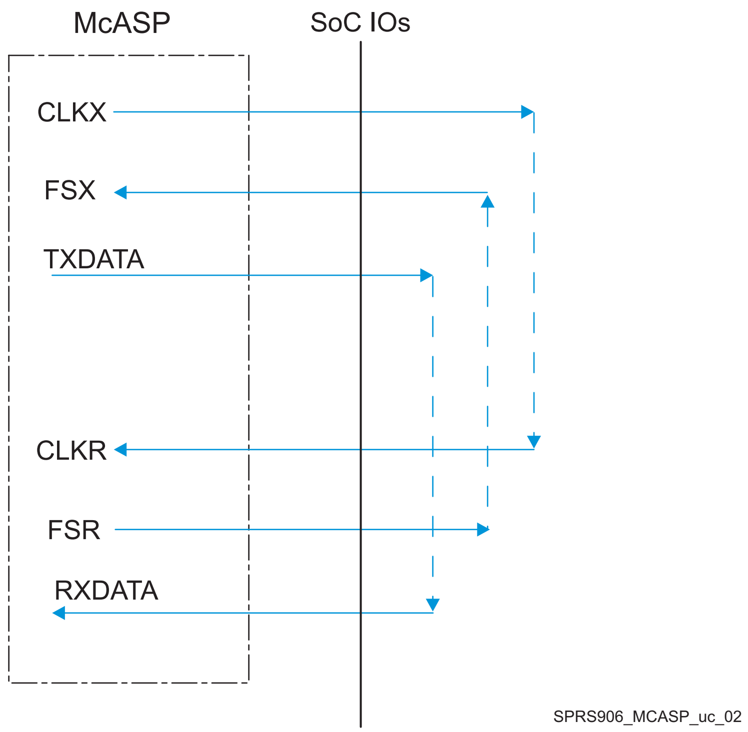


Figure 7-37. McASP1-8 COIFIO - ASYNC Mode

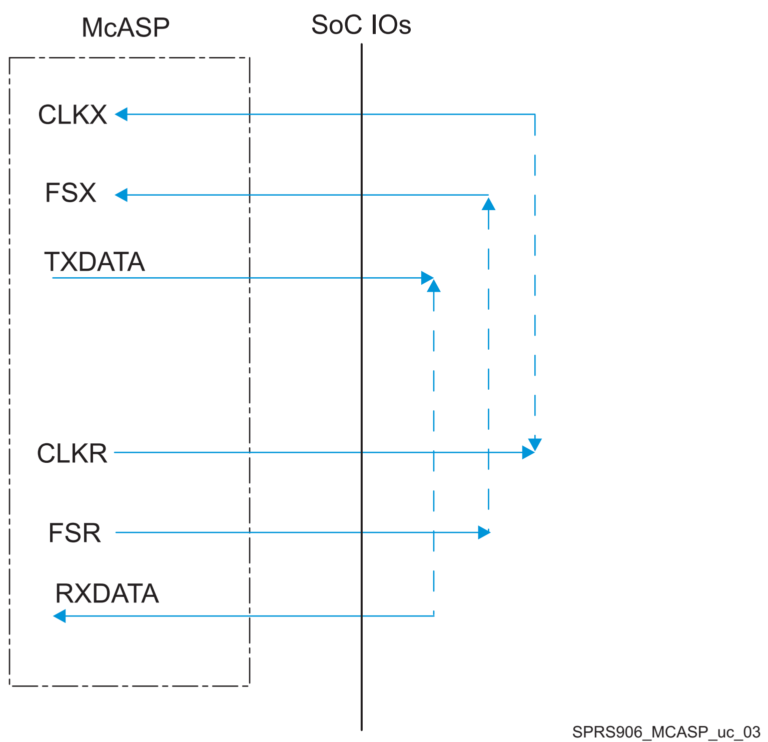


Figure 7-38. McASP1-8 CIOFIO - ASYNC Mode

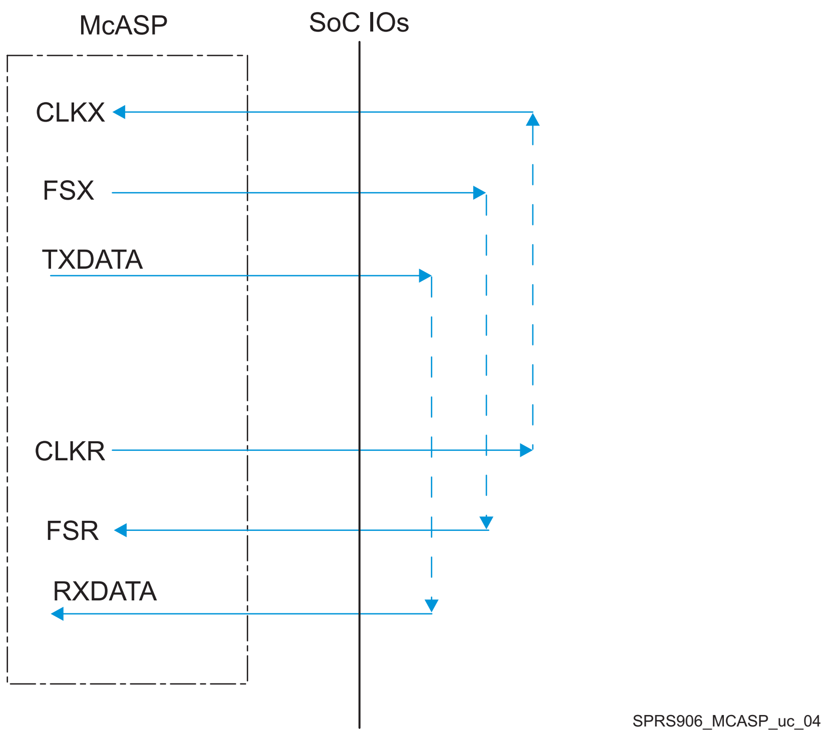


Figure 7-39. McASP1-8 CIOFOI - ASYNC Mode

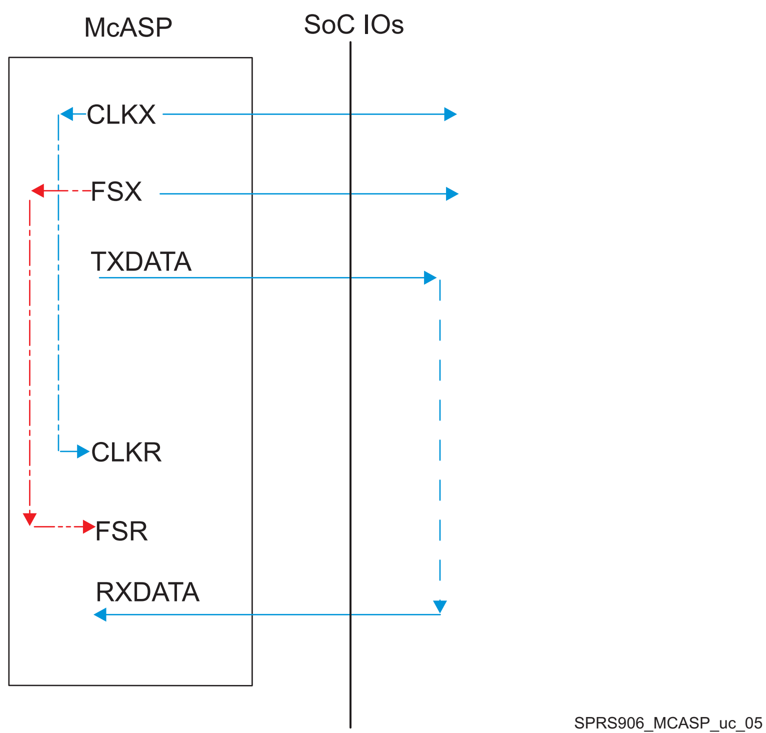


Figure 7-40. McASP1-8 CO-FO- - SYNC Mode

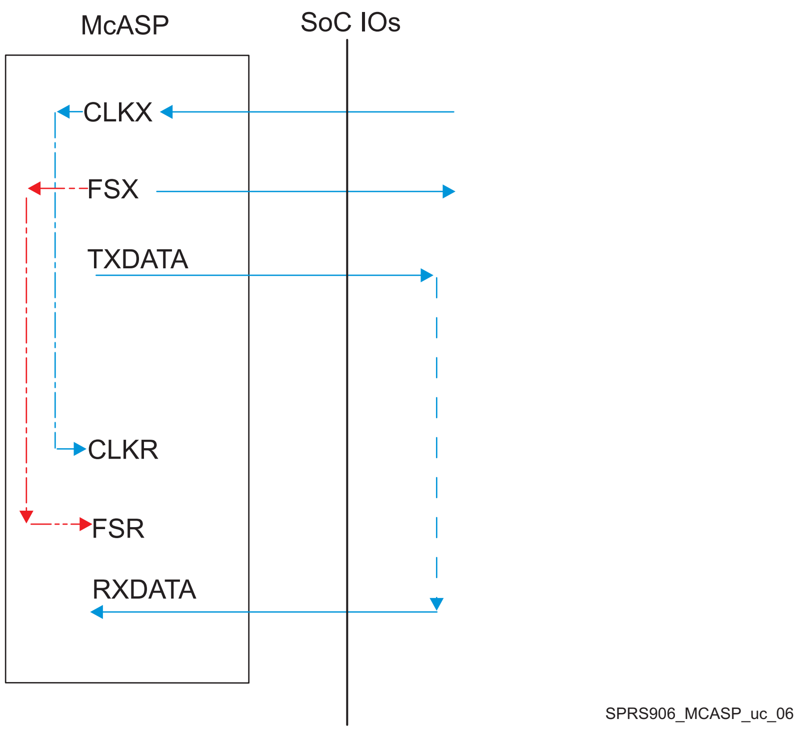


Figure 7-41. McASP1-8 CI-FO- - SYNC Mode

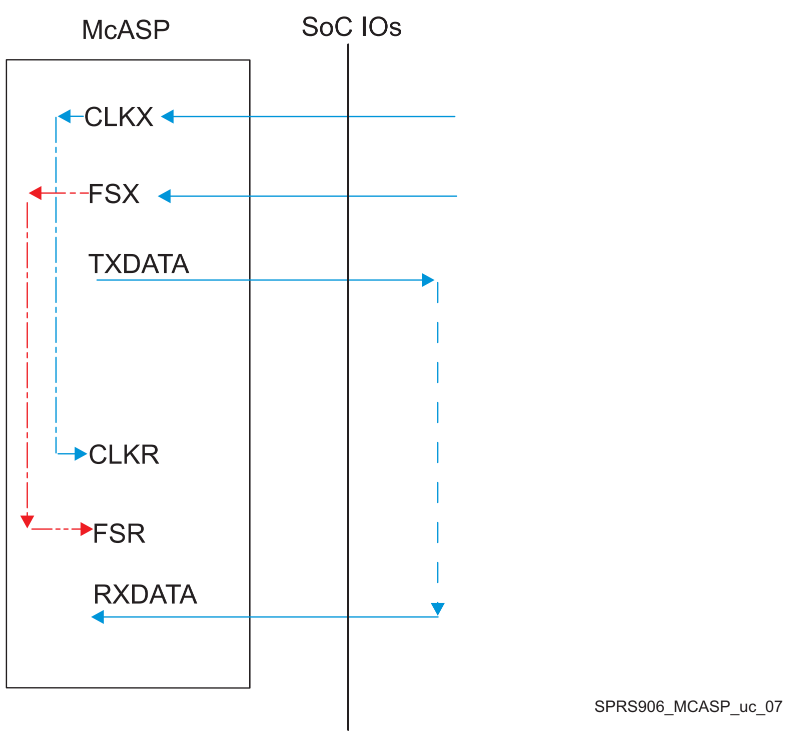


Figure 7-42. McASP1-8 CI-FI- - SYNC Mode

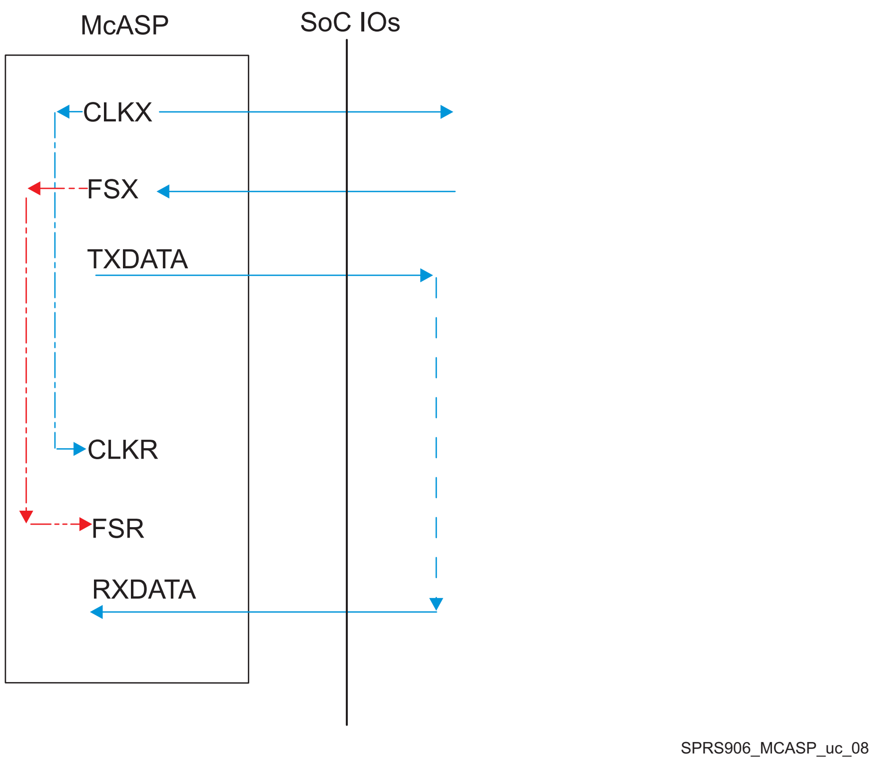


Figure 7-43. McASP1-8 CO-FI- - SYNC Mode

NOTE

To configure the desired virtual mode the user must set MODESELECT bit and DELAYMODE bit field for each corresponding pad control register.

The pad control registers are presented in Table 4-3 and described in Device TRM, *Control Module Chapter*.

CAUTION

The I/O Timings provided in this section are valid only for some McASP usage modes when the corresponding Virtual I/O Timings or Manual I/O Timings are configured as described in the tables found in this section.

Virtual IO Timings Modes must be used to ensure some IO timings for McASP1. See Table 7-2 *Modes Summary* for a list of IO timings requiring the use of Virtual IO Timings Modes. See Table 7-58 *Virtual Functions Mapping for McASP1* for a definition of the Virtual modes.

Table 7-58 presents the values for DELAYMODE bit field.

Table 7-58. Virtual Functions Mapping for McASP1

BALL	BALL NAME	Delay Mode Value		MUXMODE		
		MCASP1_VIRTUAL1_SYNC_RX	MCASP1_VIRTUAL2_ASYNC_RX	0	1	2
C14	mcasp1_aclkx	15	14	mcasp1_aclkx		
E21	gpio6_14	14	13		mcasp1_axr8	
A13	mcasp1_axr13	15	14	mcasp1_axr13		
E12	mcasp1_axr4	14	13	mcasp1_axr4		
B26	xref_clk2	14	13			mcasp1_axr6
A11	mcasp1_axr9	15	14	mcasp1_axr9		
D12	mcasp1_axr7	14	13	mcasp1_axr7		
E14	mcasp1_axr12	15	14	mcasp1_axr12		
F21	gpio6_16	14	13		mcasp1_axr10	
F20	gpio6_15	14	13		mcasp1_axr9	
C23	xref_clk3	14	13			mcasp1_axr7
C12	mcasp1_axr6	14	13	mcasp1_axr6		
B13	mcasp1_axr10	15	14	mcasp1_axr10		
J14	mcasp1_fsr	N/A	14	mcasp1_fsr		
B12	mcasp1_axr8	15	14	mcasp1_axr8		
A12	mcasp1_axr11	15	14	mcasp1_axr11		
G13	mcasp1_axr2	14	13	mcasp1_axr2		
D14	mcasp1_fsx	15	14	mcasp1_fsx		
G14	mcasp1_axr14	15	14	mcasp1_axr14		
F14	mcasp1_axr15	15	14	mcasp1_axr15		
F12	mcasp1_axr1	15	14	mcasp1_axr1		
B14	mcasp1_aclkr	N/A	14	mcasp1_aclkr		
F13	mcasp1_axr5	14	13	mcasp1_axr5		
E17	xref_clk1	15	14			mcasp1_axr5
G12	mcasp1_axr0	15	14	mcasp1_axr0		
J11	mcasp1_axr3	14	13	mcasp1_axr3		
D18	xref_clk0	15	14			mcasp1_axr4

Virtual IO Timings Modes must be used to ensure some IO timings for McASP2. See Table 7-2 *Modes Summary* for a list of IO timings requiring the use of Virtual IO Timings Modes. See Table 7-59 *Virtual Functions Mapping for McASP2* for a definition of the Virtual modes.

Table 7-59 presents the values for DELAYMODE bit field.

Table 7-59. Virtual Functions Mapping for McASP2

BALL	BALL NAME	Delay Mode Value				MUXMODE		
		MCASP2_VIRTUAL1_SYNC_RX_80M	MCASP2_VIRTUAL2_ASYNC_RX	MCASP2_VIRTUAL3_SYNC_RX	MCASP2_VIRTUAL4_ASYNC_RX_80M	0	1	2
B19	mcasp3_axr0	15	14	10	9			mcasp2_axr14
B17	mcasp2_axr6	14	13	12	11	mcasp2_axr6		
B16	mcasp2_axr5	14	13	12	11	mcasp2_axr5		
A18	mcasp2_fsx	15	14	10	9	mcasp2_fsx		
B26	xref_clk2	12	11	10	9		mcasp2_axr10	
A16	mcasp2_axr3	15	14	10	9	mcasp2_axr3		
E15	mcasp2_aclkr	N/A	14	N/A	13	mcasp2_aclkr		
B18	mcasp3_aclkx	15	14	10	9			mcasp2_axr12
A19	mcasp2_aclkx	15	14	10	9	mcasp2_aclkx		
A17	mcasp2_axr7	14	13	12	11	mcasp2_axr7		
C23	xref_clk3	12	11	10	9		mcasp2_axr11	
C17	mcasp3_axr1	15	14	10	8			mcasp2_axr15
F15	mcasp3_fsx	15	14	10	9			mcasp2_axr13
C15	mcasp2_axr2	15	14	10	9	mcasp2_axr2		
D15	mcasp2_axr4	14	13	12	11	mcasp2_axr4		
A20	mcasp2_fsr	N/A	14	N/A	13	mcasp2_fsr		
E17	xref_clk1	10	9	8	6		mcasp2_axr9	
A15	mcasp2_axr1	14	13	12	11	mcasp2_axr1		
B15	mcasp2_axr0	14	13	12	11	mcasp2_axr0		
D18	xref_clk0	10	9	8	6		mcasp2_axr8	

Virtual IO Timings Modes must be used to ensure some IO timings for McASP3/4/5/6/7/8. See Table 7-2 *Modes Summary* for a list of IO timings requiring the use of Virtual IO Timings Modes. See Table 7-60 *Virtual Functions Mapping for McASP3/4/5/6/7/8* for a definition of the Virtual modes.

Table 7-60 presents the values for DELAYMODE bit field.

Table 7-60. Virtual Functions Mapping for McASP3/4/5/6/7/8

BALL	BALL NAME	Delay Mode Value	MUXMODE		
			0	1	2
MCASP3_VIRTUAL2_SYNC_RX					
A16	mcasp2_axr3	8		mcasp3_axr3	
B18	mcasp3_aclkx	8	mcasp3_aclkx	mcasp3_aclkr	
B19	mcasp3_axr0	8	mcasp3_axr0		
C17	mcasp3_axr1	6	mcasp3_axr1		
F15	mcasp3_fsx	8	mcasp3_fsx	mcasp3_fsr	
C15	mcasp2_axr2	8		mcasp3_axr2	
MCASP4_VIRTUAL1_SYNC_RX					
A21	mcasp4_fsx	14	mcasp4_fsx	mcasp4_fsr	
C18	mcasp4_aclkx	14	mcasp4_aclkx	mcasp4_aclkr	
G16	mcasp4_axr0	14	mcasp4_axr0		
D17	mcasp4_axr1	14	mcasp4_axr1		
F13	mcasp1_axr5	12		mcasp4_axr3	
E12	mcasp1_axr4	12		mcasp4_axr2	
MCASP5_VIRTUAL1_SYNC_RX					
AA3	mcasp5_aclkx	14	mcasp5_aclkx	mcasp5_aclkr	
AB9	mcasp5_fsx	14	mcasp5_fsx	mcasp5_fsr	
AA4	mcasp5_axr1	14	mcasp5_axr1		
C12	mcasp1_axr6	12		mcasp5_axr2	
AB3	mcasp5_axr0	14	mcasp5_axr0		
D12	mcasp1_axr7	12		mcasp5_axr3	
MCASP6_VIRTUAL1_SYNC_RX					
G13	mcasp1_axr2	12		mcasp6_axr2	
J11	mcasp1_axr3	12		mcasp6_axr3	
B13	mcasp1_axr10	10		mcasp6_aclkx	mcasp6_aclkr
A11	mcasp1_axr9	10		mcasp6_axr1	
B12	mcasp1_axr8	10		mcasp6_axr0	
A12	mcasp1_axr11	10		mcasp6_fsx	mcasp6_fsr
MCASP7_VIRTUAL2_SYNC_RX					
E14	mcasp1_axr12	10		mcasp7_axr0	
F14	mcasp1_axr15	10		mcasp7_fsx	mcasp7_fsr
G14	mcasp1_axr14	10		mcasp7_aclkx	mcasp7_aclkr

Table 7-60. Virtual Functions Mapping for McASP3/4/5/6/7/8 (continued)

BALL	BALL NAME	Delay Mode Value	MUXMODE		
			0	1	2
A13	mcasp1_axr13	10		mcasp7_axr1	
B14	mcasp1_aclkr	13		mcasp7_axr2	
J14	mcasp1_fsr	13		mcasp7_axr3	
MCASP8_VIRTUAL1_SYNC_RX					
D15	mcasp2_axr4	10		mcasp8_axr0	
A17	mcasp2_axr7	10		mcasp8_fsx	mcasp8_fsr
B17	mcasp2_axr6	10		mcasp8_aclkx	mcasp8_aclkr
A20	mcasp2_fsr	12		mcasp8_axr3	
B16	mcasp2_axr5	10		mcasp8_axr1	
E15	mcasp2_aclkr	12		mcasp8_axr2	

7.18 Universal Serial Bus (USB)

SuperSpeed USB DRD Subsystem has four instances in the device providing the following functions:

- USB1: SuperSpeed (SS) USB 3.0 Dual-Role-Device (DRD) subsystem with integrated SS (USB3.0) PHY and HS/FS (USB2.0) PHY.
- USB2: High Speed (HS) USB 2.0 Dual-Role-Device (DRD) subsystem with integrated HS/FS PHY.
- USB3: HS USB 2.0 Dual-Role-Device (DRD) subsystem with ULPI (SDR) interface to external HS/FS PHYs.

NOTE

For more information, see *SuperSpeed USB DRD* section in the device TRM.

7.18.1 USB1 DRD PHY

The USB1 DRD interface supports the following applications:

- USB2.0 High Speed PHY port (1.8 V and 3.3 V): this asynchronous high speed interface is compliant with the USB2.0 PHY standard with an internal transceiver (USB2.0 standard v2.0), for a maximum data rate of 480 Mbps.
- USB3.0 SuperSpeed PHY port (1.8 V): this asynchronous differential super speed interface is compliant with the USB3.0 RX/TX PHY standard (USB3.0 standard v1.0) for a maximum data bit rate of 5Gbps.

7.18.2 USB2 PHY

The USB2 interface supports the following applications:

- USB2.0 High Speed PHY port (1.8 V and 3.3 V): this asynchronous high speed interface is compliant with the USB2.0 PHY standard with an internal transceiver (USB2.0 standard v2.0), for a maximum data rate of 480 Mbps.

7.18.3 USB3 DRD ULPI-SDR-Slave Mode-12-pin Mode

TheUSB3 DRD interfaces support the following application:

- USB ULPI port: this synchronous interface is compliant with the USB2.0 ULPI SDR standard (UTMI+ v1.22), for alternative off-chip USB2.0 PHY interface; that is, with external transceiver with a maximum frequency of 60 MHz (synchronous slave mode, SDR, 12-pin, 8-data-bit).

NOTE

The Universal Serial Bus k ULPI modules are also refered as USBk where k = 3, 4.

Table 7-61, Table 7-62 and Figure 7-44 assume testing over the recommended operating conditions and electrical characteristic conditions.

Table 7-61. Timing Requirements for ULPI SDR Slave Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
US1	$t_{c(clk)}$	Cycle time, usb_ulpi_clk period	16.66		ns
US5	$t_{su(ctrlV-clkH)}$	Setup time, usb_ulpi_dir/usb_ulpi_nxt valid before usb_ulpi_clk rising edge	6.73		ns
US6	$t_{h(clkH-ctrlV)}$	Hold time, usb_ulpi_dir/usb_ulpi_nxt valid after usb_ulpi_clk rising edge	-0.41		ns
US7	$t_{su(dV-clkH)}$	Setup time, usb_ulpi_d[7:0] valid before usb_ulpi_clk rising edge	6.73		ns
US8	$t_{h(clkH-dV)}$	Hold time, usb_ulpi_d[7:0] valid after usb_ulpi_clk rising edge	-0.41		ns

Table 7-62. Switching Characteristics for ULPI SDR Slave Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
US4	$t_{d(clkH-stpV)}$	Delay time, usb_ulpi_clk rising edge high to output usb_ulpi_stp valid	0.44	8.35	ns
US9	$t_{d(clkL-doV)}$	Delay time, usb_ulpi_clk rising edge high to output usb_ulpi_d[7:0] valid	0.44	8.35	ns

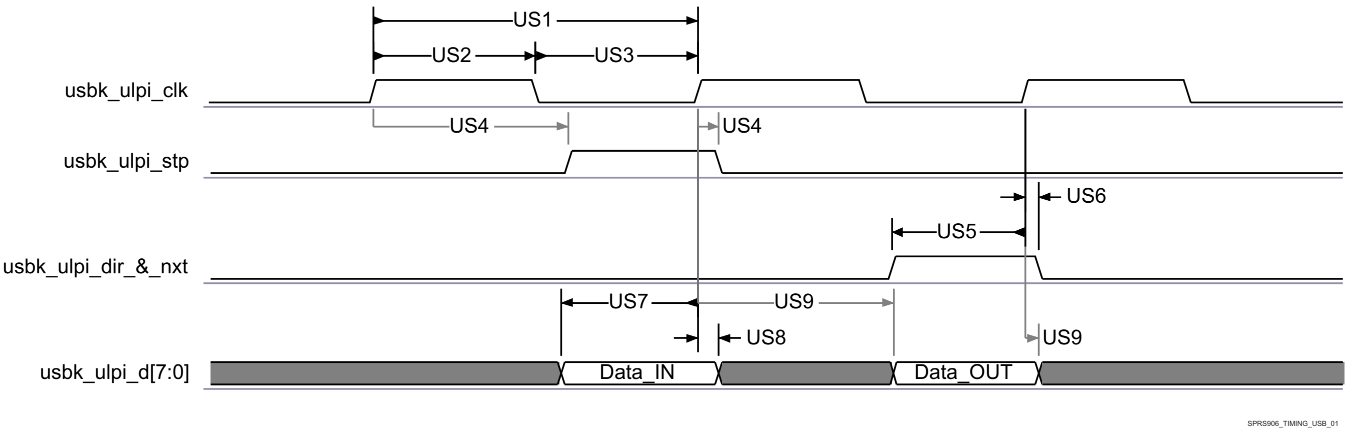


Figure 7-44. HS USB3 ULPI -SDR-Slave Mode-12-pin Mode

In Table 7-63 are presented the specific groupings of signals (IOSET) for use with USB3 signals.

Table 7-63. USB3 IOSETs

SIGNALS	IOSET2		IOSET3	
	BALL	MUX	BALL	MUX
usb3_ulpi_d7	AC5	3	W2	6
usb3_ulpi_d6	AB4	3	Y2	6
usb3_ulpi_d5	AD4	3	V3	6
usb3_ulpi_d4	AC4	3	V4	6
usb3_ulpi_d3	AC7	3	V5	6
usb3_ulpi_d2	AC6	3	U5	6
usb3_ulpi_d1	AC9	3	U6	6
usb3_ulpi_d0	AC3	3	V6	6
usb3_ulpi_nxt	AC8	3	U7	6
usb3_ulpi_dir	AD6	3	V7	6
usb3_ulpi_stp	AB8	3	V9	6
usb3_ulpi_clk	AB5	3	W9	6

7.19 Serial Advanced Technology Attachment (SATA)

The SATA RX/TX PHY interface is compliant with the SATA standard v2.6 for a maximum data rate:

- Gen2i, Gen2m, Gen2x: 3Gbps.
- Gen1i, Gen1m, Gen1x: 1.5Gbps.

NOTE

For more information, see *SATA Controller* section in the device TRM.

7.20 Peripheral Component Interconnect Express (PCIe)

The device supports connections to PCIe-compliant devices via the integrated PCIe master/slave bus interface. The PCIe module is comprised of a dual-mode PCIe core and a SerDes PHY. Each PCIe subsystem controller has support for PCIe Gen-II mode (5.0 Gbps /lane) and Gen-I mode (2.5 Gbps/lane) (Single Lane and Flexible dual lane configuration).

The device PCIe supports the following features:

- 16-bit operation @250 MHz on PIPE interface (per 16-bit lane)
- Supports 2 ports x 1 lane or 1 port x 2 lanes configuration
- Single virtual channel (VC0), single traffic class (TC0)
- Single function in end-point mode
- Automatic width and speed negotiation
- Max payload: 128 byte outbound, 256 byte inbound
- Automatic credit management
- ECRC generation and checking
- Configurable BAR filtering
- Legacy interrupt reception (RC) and generation (EP)
- MSI generation and reception
- PCI-Express Active State Power Management (ASPM) state L0s and L1 (with exceptions)
- All PCI Device Power Management D-states with the exception of $D3_{cold}$ / L2 state

The PCIe controller on this device conforms to the PCI-Express Base 3.0 Specification, revision 1.0 and the PCI Local Bus Specification, revision 3.0

NOTE

For more information, see *PCIe Controller* section in the device TRM.

7.21 Controller Area Network Interface (DCAN)

The device provides two DCAN interfaces for supporting distributed realtime control with a high level of security. The DCAN interfaces implement the following features:

- Supports CAN protocol version 2.0 part A, B
- Bit rates up to 1 MBit/s
- 64 message objects
- Individual identifier mask for each message object
- Programmable FIFO mode for message objects
- Programmable loop-back modes for self-test operation
- Suspend mode for debug support
- Software module reset
- Automatic bus on after Bus-Off state by a programmable 32-bit timer
- Direct access to Message RAM during test mode
- CAN Rx/Tx pins are configurable as general-purpose IO pins
- Two interrupt lines (plus additional parity-error interrupts line)
- RAM initialization
- DMA support

NOTE

For more information, see *DCAN* section in the device TRM.

NOTE
The Controller Area Network Interface x (x = 1 to 2) is also referred to as DCANx.

NOTE
Refer to the CAN Specification for calculations necessary to validate timing compliance. Jitter tolerance calculations must be performed to validate the implementation.

Table 7-64 and Table 7-65 present timing and switching characteristics for DCANx Interface.

Table 7-64. Timing Requirements for DCANx Receive

NO.	PARAMETER	DESCRIPTION	MIN	NOM	MAX	UNIT
-	$f_{(baud)}$	Maximum programmable baud rate			1	Mbps
-	$t_{d(DCANRX)}$	Delay time, DCANx_RX pin to receive shift register			15	ns

Table 7-65. Switching Characteristics Over Recommended Operating Conditions for DCANx Transmit

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
-	f(baud)	Maximum programmable baud rate		1	Mbps
-	$t_{d(DCANTX)}$	Delay time, Transmit shift register to DCANx_TX pin(1)		23	ns

(1) These values do not include rise/fall times of the output buffer.

7.22 Ethernet Interface (GMAC_SW)

The three-port gigabit ethernet switch subsystem (GMAC_SW) provides ethernet packet communication and can be configured as an ethernet switch. It provides the Gigabit Media Independent Interface (G/MII) in MII mode, Reduced Gigabit Media Independent Interface (RGMII), Reduced Media Independent Interface (RMII), and the Management Data Input/Output (MDIO) for physical layer device (PHY) management.

NOTE
For more information, see *Gigabit Ethernet Switch (GMAC_SW)* section in the device TRM.

NOTE
The Gigabit, Reduced and Media Independent Interface n (n = 0 to 1) are also referred to as MIIn, RMIIn and RGMIIn.

CAUTION

The I/O timings provided in this section are valid only if signals within a single IOSET are used. The IOSETs are defined in Table 7-70, Table 7-73, Table 7-78 and Table 7-85.

CAUTION

The I/O Timings provided in this section are valid only for some GMAC usage modes when the corresponding Virtual I/O Timings or Manual I/O Timings are configured as described in the tables found in this section.

Table 7-66 and Figure 7-45 present timing requirements for MIIn in receive operation.

7.22.1 GMAC MII Timings

Table 7-66. Timing Requirements for miin_rxclk - MII Operation

NO.	PARAMETER	DESCRIPTION	SPEED	MIN	MAX	UNIT
1	$t_{c(RX\_CLK)}$	Cycle time, miin_rxclk	10 Mbps	400		ns
			100 Mbps	40		ns
2	$t_{w(RX\_CLKH)}$	Pulse duration, miin_rxclk high	10 Mbps	140	260	ns
			100 Mbps	14	26	ns
3	$t_{w(RX\_CLKL)}$	Pulse duration, miin_rxclk low	10 Mbps	140	260	ns
			100 Mbps	14	26	ns
4	$t_{t(RX\_CLK)}$	Transition time, miin_rxclk	10 Mbps		3	ns
			100 Mbps		3	ns

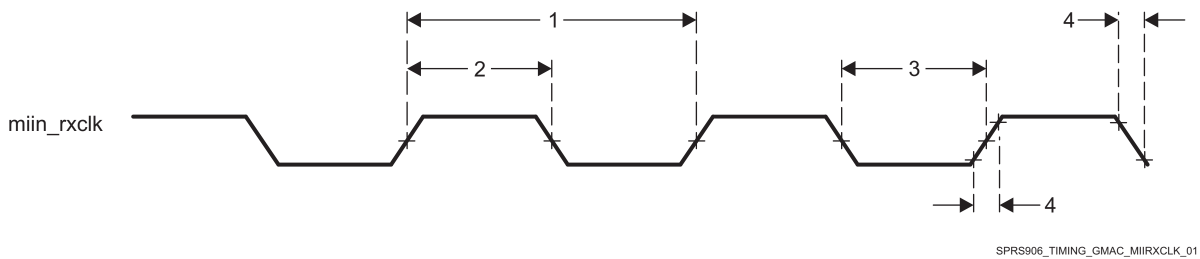


Figure 7-45. Clock Timing (GMAC Receive) - MIIn operation

Table 7-67 and Figure 7-46 present timing requirements for MIIn in transmit operation.

Table 7-67. Timing Requirements for miin_txclk - MII Operation

NO.	PARAMETER	DESCRIPTION	SPEED	MIN	MAX	UNIT
1	$t_{c(TX\_CLK)}$	Cycle time, miin_txclk	10 Mbps	400		ns
			100 Mbps	40		ns
2	$t_{w(TX\_CLKH)}$	Pulse duration, miin_txclk high	10 Mbps	140	260	ns
			100 Mbps	14	26	ns
3	$t_{w(TX\_CLKL)}$	Pulse duration, miin_txclk low	10 Mbps	140	260	ns
			100 Mbps	14	26	ns
4	$t_{t(TX\_CLK)}$	Transition time, miin_txclk	10 Mbps		3	ns
			100 Mbps		3	ns

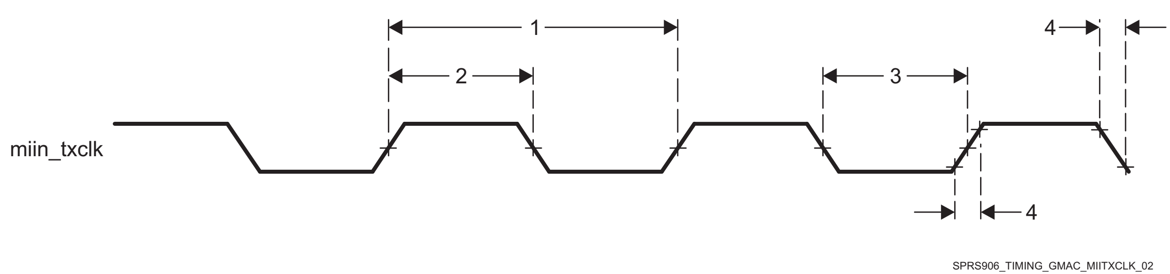


Figure 7-46. Clock Timing (GMAC Transmit) - MIIn operation

Table 7-68 and Figure 7-47 present timing requirements for GMAC MIIn Receive 10/100Mbit/s.

Table 7-68. Timing Requirements for GMAC MIIn Receive 10/100 Mbit/s

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
1	$t_{su(RXD-RX\_CLK)}$ $t_{su(RX\_DV-RX\_CLK)}$ $t_{su(RX\_ER-RX\_CLK)}$	Setup time, receive selected signals valid before miin_rxclk	8		ns
2	$t_{h(RX\_CLK-RXD)}$ $t_{h(RX\_CLK-RX\_DV)}$ $t_{h(RX\_CLK-RX\_ER)}$	Hold time, receive selected signals valid after miin_rxclk	8		ns

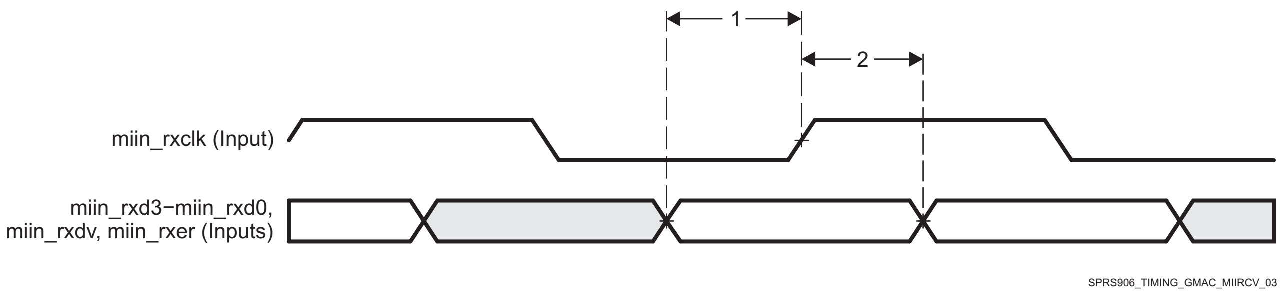


Figure 7-47. GMAC Receive Interface Timing MIIn operation

Table 7-69 and Figure 7-48 present timing requirements for GMAC MIIn Transmit 10/100Mbit/s.

Table 7-69. Switching Characteristics Over Recommended Operating Conditions for GMAC MIIn Transmit 10/100 Mbits/s

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
1	$t_{d(TX\_CLK-TXD)}$ $t_{d(TX\_CLK-TX\_EN)}$ $t_{d(TX\_CLK-TX\_ER)}$	Delay time, miin_txclk to transmit selected signals valid	0	25	ns

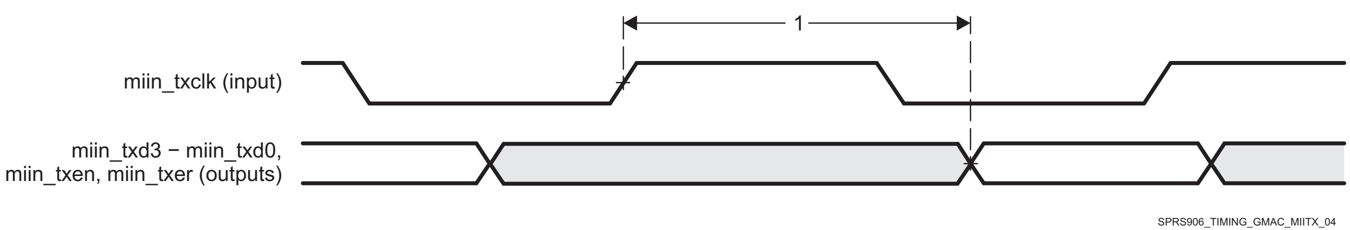


Figure 7-48. GMAC Transmit Interface Timing MIIn operation

In Table 7-70 are presented the specific groupings of signals (IOSET) for use with GMAC MII signals.

Table 7-70. GMAC MII IOSETs

SIGNALS	IOSET5		IOSET6	
	BALL	MUX	BALL	MUX
GMAC MII1				
mii1_txd3	C5	8		
mii1_txd2	D6	8		
mii1_txd1	B2	8		
mii1_txd0	C4	8		
mii1_rxd3	F5	8		
mii1_rxd2	E4	8		
mii1_rxd1	C1	8		

Table 7-70. GMAC MII IOSETs (continued)

SIGNALS	IOSET5		IOSET6	
	BALL	MUX	BALL	MUX
mii1_rxd0	E6	8		
mii1_col	B4	8		
mii1_rxer	B3	8		
mii1_txer	A3	8		
mii1_txen	A4	8		
mii1_crs	B5	8		
mii1_rxclk	D5	8		
mii1_txclk	C3	8		
mii1_rxdv	C2	8		
GMAC MII0				
mii0_txd3			V5	3
mii0_txd2			V4	3
mii0_txd1			Y2	3
mii0_txd0			W2	3
mii0_rxd3			W9	3
mii0_rxd2			V9	3
mii0_rxd1			V6	3
mii0_rxd0			U6	3
mii0_txclk			U5	3
mii0_txer			U4	3
mii0_rxer			U7	3
mii0_rxdv			V2	3
mii0_crs			V7	3
mii0_col			V1	3
mii0_rxclk			Y1	3
mii0_txen			V3	3

7.22.2 GMAC MDIO Interface Timings

CAUTION

The I/O Timings provided in this section are valid only for some GMAC usage modes when the corresponding Virtual I/O Timings or Manual I/O Timings are configured as described in the tables found in this section.

Table 7-71, Table 7-71 and Figure 7-49 present timing requirements for MDIO.

Table 7-71. Timing Requirements for MDIO Input

No	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
MDIO1	$t_{c(MDC)}$	Cycle time, MDC	400		ns
MDIO2	$t_{w(MDCH)}$	Pulse Duration, MDC High	160		ns
MDIO3	$t_{w(MDCL)}$	Pulse Duration, MDC Low	160		ns
MDIO4	$t_{su(MDIO-MDC)}$	Setup time, MDIO valid before MDC High	90		ns
MDIO5	$t_{h(MDIO\_MDC)}$	Hold time, MDIO valid from MDC High	0		ns

Table 7-72. Switching Characteristics Over Recommended Operating Conditions for MDIO Output

NO	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
MDIO6	$t_{t(MDC)}$	Transition time, MDC		5	ns
MDIO7	$t_{d(MDC-MDIO)}$	Delay time, MDC low to MDIO valid	-150	150	ns

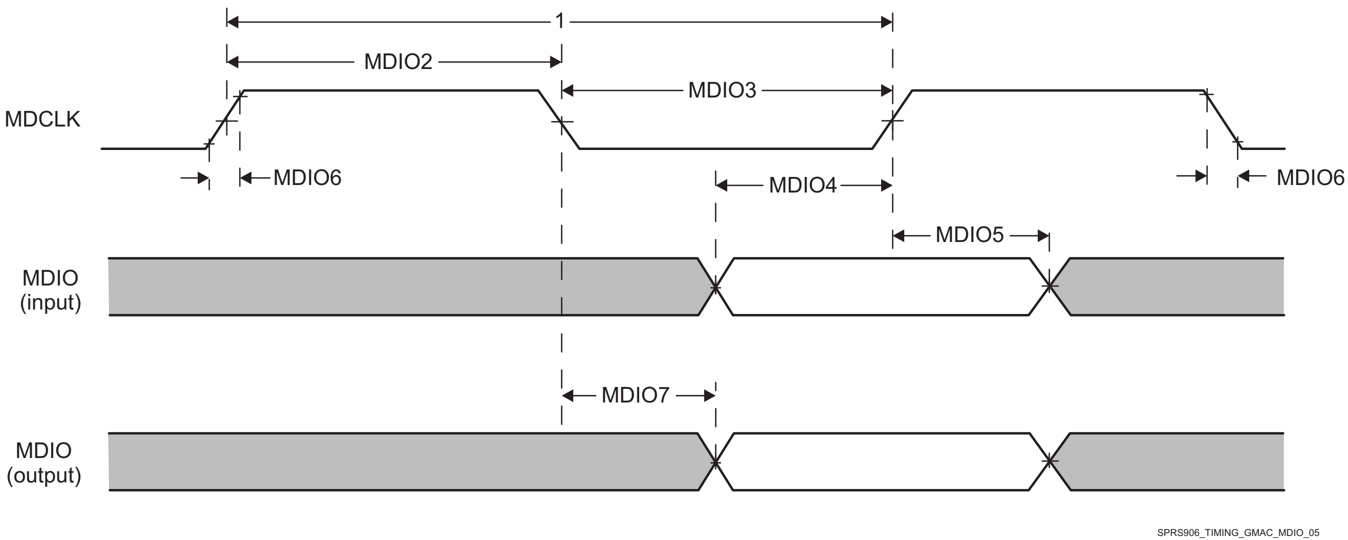


Figure 7-49. GMAC MDIO diagrams

In Table 7-73 are presented the specific groupings of signals (IOSET) for use with GMAC MDIO signals.

Table 7-73. GMAC MDIO IOSETs

SIGNALS	IOSET7		IOSET8		IOSET9		IOSET10	
	BALL	MUX	BALL	MUX	BALL	MUX	BALL	MUX
mdio_d	F6	3	U4	0	AB4	1	B20	5
mdio_mclk	D3	3	V1	0	AC5	1	B21	5

7.22.3 GMAC RMII Timings

The main reference clock REF_CLK (RMII_50MHZ_CLK) of RMII interface is internally supplied from PRCM. The source of this clock could be either externally sourced from the RMII_MHZ_50_CLK pin of the device or internally generated from DPLL_GMAC output clock GMAC_RMII_HS_CLK. Please see the PRCM chapter of the device TRM for full details about RMII reference clock.

CAUTION

The I/O Timings provided in this section are valid only for some GMAC usage modes when the corresponding Virtual I/O Timings or Manual I/O Timings are configured as described in the tables found in this section.

Table 7-74, Table 7-75 and Figure 7-50 present timing requirements for GMAC RMIIn Receive.

Table 7-74. Timing Requirements for GMAC REF_CLK - RMII Operation

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
RMII1	$t_{c(REF\_CLK)}$	Cycle time, REF_CLK	20		ns
RMII2	$t_{w(REF\_CLKH)}$	Pulse duration, REF_CLK high	7	13	ns
RMII3	$t_{w(REF\_CLKL)}$	Pulse duration, REF_CLK low	7	13	ns

Table 7-74. Timing Requirements for GMAC REF_CLK - RMII Operation (continued)

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
RMII4	$t_{tt(REF\_CLK)}$	Transistion time, REF_CLK		3	ns

Table 7-75. Timing Requirements for GMAC RMIIn Receive

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
RMII5	$t_{su(RXD-REF\_CLK)}$	Setup time, receive selected signals valid before REF_CLK	4		ns
	$t_{su(CRS\_DV-REF\_CLK)}$				
	$t_{su(RX\_ER-REF\_CLK)}$				
RMII6	$t_{h(REF\_CLK-RXD)}$	Hold time, receive selected signals valid after REF_CLK	2		ns
	$t_{h(REF\_CLK-CRS\_DV)}$				
	$t_{h(REF\_CLK-RX\_ER)}$				

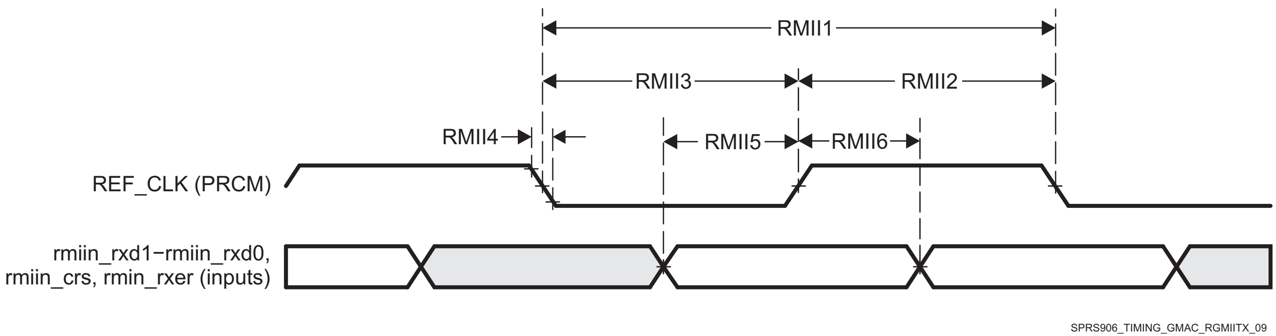


Figure 7-50. GMAC Receive Interface Timing RMIIn operation

Table 7-76, Table 7-76 and Figure 7-51 present switching characteristics for GMAC RMIIn Transmit 10/100Mbit/s.

Table 7-76. Switching Characteristics Over Recommended Operating Conditions for GMAC REF_CLK - RMII Operation

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
RMII7	$t_{c(REF\_CLK)}$	Cycle time, REF_CLK	20		ns
RMII8	$t_{w(REF\_CLKH)}$	Pulse duration, REF_CLK high	7	13	ns
RMII9	$t_{w(REF\_CLKL)}$	Pulse duration, REF_CLK low	7	13	ns
RMII10	$t_{t(REF\_CLK)}$	Transistion time, REF_CLK		3	ns

Table 7-77. Switching Characteristics Over Recommended Operating Conditions for GMAC RMIIn Transmit 10/100 Mbits/s

NO.	PARAMETER	DESCRIPTION	RMIIn	MIN	MAX	UNIT
RMII11	$t_{d(REF\_CLK-TXD)}$	Delay time, REF_CLK high to selected transmit signals valid	RMII0	2	13.5	ns
	$t_{dd(REF\_CLK-TXEN)}$					
	$t_{d(REF\_CLK-TXD)}$		RMII1	2	13.8	ns
	$t_{dd(REF\_CLK-TXEN)}$					

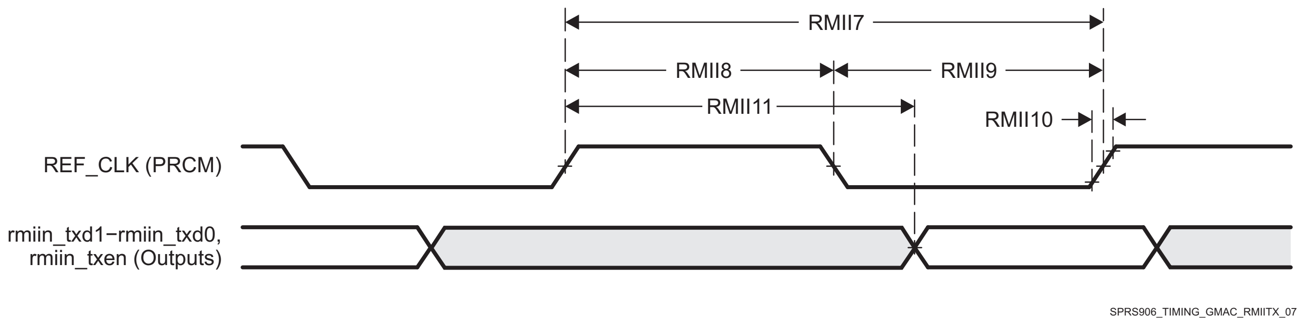


Figure 7-51. GMAC Transmit Interface Timing RMIIn Operation

In Table 7-78 are presented the specific groupings of signals (IOSET) for use with GMAC RMII signals.

Table 7-78. GMAC RMII IOSETs

SIGNALS	IOSET1		IOSET2	
	BALL	MUX	BALL	MUX
GMAC RMII1				
RMII_MHZ_50_CLK	U3	0		
rmii1_txd1	V5	2		
rmii1_txd0	V4	2		
rmii1_rxd1	W9	2		
rmii1_rxd0	V9	2		
rmii1_rxer	Y1	2		
rmii1_txen	U5	2		
rmii1_crs	V2	2		
GMAC RMII0				
RMII_MHZ_50_CLK			U3	0
rmii0_txd1			Y2	1
rmii0_txd0			W2	1
rmii0_rxd1			V6	1
rmii0_rxd0			U6	1
rmii0_txen			V3	1
rmii0_rxer			U7	1
rmii0_crs			V7	1

Manual IO Timings Modes must be used to ensure some IO timings for GMAC. See Table 7-2 *Modes Summary* for a list of IO timings requiring the use of Manual IO Timings Modes. See Table 7-79 *Manual Functions Mapping for GMAC RMII0* for a definition of the Manual modes.

Table 7-79 lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.

Table 7-79. Manual Functions Mapping for GMAC RMII0

BALL	BALL NAME	GMAC_RMII0_MANUAL1		CFG REGISTER	MUXMODE	
		A_DELAY (ps)	G_DELAY (ps)		0	1
U3	RMII_MHZ_50_CLK	0	0	CFG_RMII_MHZ_50_CLK_IN	RMII_MHZ_50_CLK	
U6	rgmii0_txd0	2444	804	CFG_RGMII0_TXD0_IN		rmii0_rxd0
V6	rgmii0_txd1	2453	981	CFG_RGMII0_TXD1_IN		rmii0_rxd1
U7	rgmii0_txd2	2356	847	CFG_RGMII0_TXD2_IN		rmii0_rxer
V7	rgmii0_txd3	2415	993	CFG_RGMII0_TXD3_IN		rmii0_crs

Manual IO Timings Modes must be used to ensure some IO timings for GMAC. See Table 7-2 *Modes Summary* for a list of IO timings requiring the use of Manual IO Timings Modes. See Table 7-80 *Manual Functions Mapping for GMAC RMII1* for a definition of the Manual modes.

Table 7-80 list the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.

Table 7-80. Manual Functions Mapping for GMAC RMII1

BALL	BALL NAME	GMAC_RMII1_MANUAL1		CFG REGISTER	MUXMODE	
		A_DELAY (ps)	G_DELAY (ps)		0	2
U3	RMII_MHZ_50_CLK	0	0	CFG_RMII_MHZ_50_CLK_IN	RMII_MHZ_50_CLK	
V9	rgmii0_txctl	2450	909	CFG_RGMII0_TXCTL_IN		rmii1_rxd0
W9	rgmii0_txc	2327	926	CFG_RGMII0_TXC_IN		rmii1_rxd1
Y1	uart3_txd	2553	443	CFG_UART3_TXD_IN		rmii1_rxer
V2	uart3_rxd	1943	1110	CFG_UART3_RXD_IN		rmii1_crs

7.22.4 GMAC RGMII Timings

CAUTION

The I/O Timings provided in this section are valid only for some GMAC usage modes when the corresponding Virtual I/O Timings or Manual I/O Timings are configured as described in the tables found in this section.

Table 7-81, Table 7-82 and Figure 7-52 present timing requirements for receive RGMIIn operation.

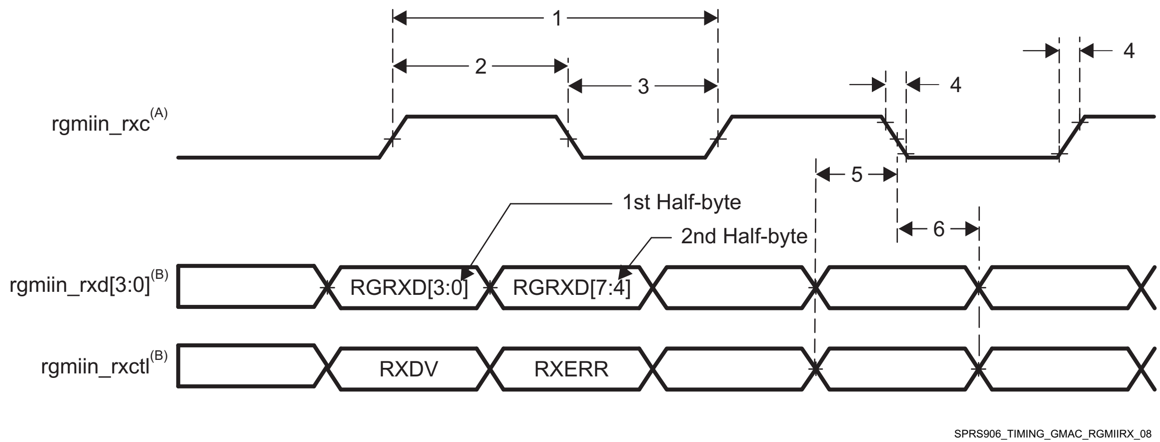
Table 7-81. Timing Requirements for rgmiin_rxc - RGMIIn Operation

NO.	PARAMETER	DESCRIPTION	SPEED	MIN	MAX	UNIT
1	$t_{c(TXC)}$	Cycle time, rgmiin_txc	10 Mbps	360	440	ns
			100 Mbps	36	44	ns
			1000 Mbps	7.2	8.8	ns
2	$t_{w(TXCH)}$	Pulse duration, rgmiin_txc high	10 Mbps	160	240	ns
			100 Mbps	16	24	ns
			1000 Mbps	3.6	4.4	ns
3	$t_{w(TXCL)}$	Pulse duration, rgmiin_txc low	10 Mbps	160	240	ns
			100 Mbps	16	24	ns
			1000 Mbps	3.6	4.4	ns
4	$t_{t(TXC)}$	Transition time, rgmiin_txc	10 Mbps		0.75	ns
			100 Mbps		0.75	ns
			1000 Mbps		0.75	ns

Table 7-82. Timing Requirements for GMAC RGMIIn Input Receive for 10/100/1000 Mbps (1)

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
5	$t_{su(RXD-RXCH)}$	Setup time, receive selected signals valid before rgmiin_rxc high/low	RGMII0/1	1		ns
6	$t_{h(RXCH-RXD)}$	Hold time, receive selected signals valid after rgmiin_rxc high/low	RGMII0/1	1		ns

(1) For RGMII, receive selected signals include: rgmiin_rxd[3:0] and rgmiin_rxctl.



A. rgmiin_rxc must be externally delayed relative to the data and control pins.
B. Data and control information is received using both edges of the clocks. rgmiin_rxd[3:0] carries data bits 3-0 on the rising edge of rgmiin_rxc and data bits 7-4 on the falling edge ofrgmiin_rxc. Similarly, rgmiin_rxctl carries RXDV on rising edge of rgmiin_rxc and RXERR on falling edge of rgmiin_rxc.

Figure 7-52. GMAC Receive Interface Timing, RGMIIn operation

Table 7-83, Table 7-84 and Figure 7-53 present switching characteristics for transmit - RGMIIn for 10/100/1000Mbit/s.

Table 7-83. Switching Characteristics Over Recommended Operating Conditions for rgmiin_txctl - RGMIIn Operation for 10/100/1000 Mbit/s

NO.	PARAMETER	DESCRIPTION	SPEED	MIN	MAX	UNIT
1	$t_{c(TXC)}$	Cycle time, rgmiin_txc	10 Mbps	360	440	ns
			100 Mbps	36	44	ns
			1000 Mbps	7.2	8.8	ns
2	$t_{w(TXCH)}$	Pulse duration, rgmiin_txc high	10 Mbps	160	240	ns
			100 Mbps	16	24	ns
			1000 Mbps	3.6	4.4	ns
3	$t_{w(TXCL)}$	Pulse duration, rgmiin_txc low	10 Mbps	160	240	ns
			100 Mbps	16	24	ns
			1000 Mbps	3.6	4.4	ns
4	$t_{t(TXC)}$	Transition time, rgmiin_txc	10 Mbps		0.75	ns
			100 Mbps		0.75	ns
			1000 Mbps		0.75	ns

Table 7-84. Switching Characteristics for GMAC RGMIIn Output Transmit for 10/100/1000 Mbps (1)

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
5	$t_{osu(TXD-TXC)}$	Output Setup time, transmit selected signals valid to rgmiin_txc high/low	RGMII0, Internal Delay Enabled, 1000 Mbps	1.05 (2)		ns
			RGMII0, Internal Delay Enabled, 10/100 Mbps	1.2		ns
			RGMII1, Internal Delay Enabled, 1000 Mbps	1.05 (3)		ns
			RGMII1, Internal Delay Enabled, 10/100 Mbps	1.2		ns

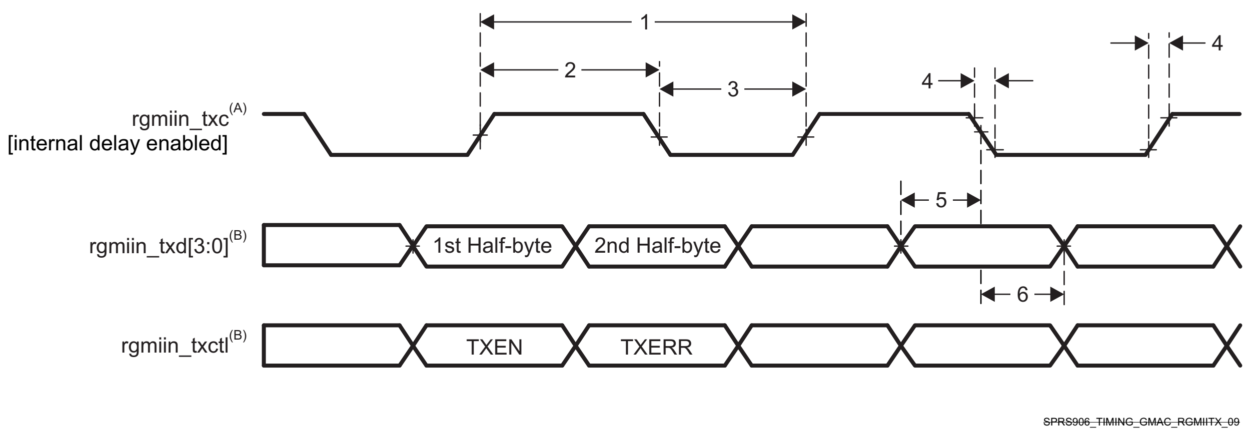
Table 7-84. Switching Characteristics for GMAC RGMIIn Output Transmit for 10/100/1000 Mbps (1) (continued)

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
6	$t_{oh(TXC-TXD)}$	Output Hold time, transmit selected signals valid after rgmiin_txc high/low	RGMII0, Internal Delay Enabled, 1000 Mbps	1.05 (2)		ns
			RGMII0, Internal Delay Enabled, 10/100 Mbps	1.2		ns
			RGMII1, Internal Delay Enabled, 1000 Mbps	1.05 (3)		ns
			RGMII1, Internal Delay Enabled, 10/100 Mbps	1.2		ns

(1) For RGMII, transmit selected signals include: rgmiin_txd[3:0] and rgmiin_txctl.

(2) RGMII0 requires that the 4 data pins rgmii0_txd[3:0] and rgmii0_txctl have their board propagation delays matched within 50pS of rgmii0_txc.

(3) RGMII1 requires that the 4 data pins rgmii1_txd[3:0] and rgmii1_txctl have their board propagation delays matched within 50pS of rgmii1_txc.



A. TXC is delayed internally before being driven to the rgmiin_txc pin. This internal delay is always enabled.

B. Data and control information is transmitted using both edges of the clocks. rgmiin_txd[3:0] carries data bits 3-0 on the rising edge of rgmiin_txc and data bits 7-4 on the falling edge of rgmiin_txc. Similarly, rgmiin_txctl carries TXEN on rising edge of rgmiin_txc and TXERR of falling edge of rgmiin_txc.

Figure 7-53. GMAC Transmit Interface Timing RGMIIn operation

In Table 7-85 are presented the specific groupings of signals (IOSET) for use with GMAC RGMII signals.

Table 7-85. GMAC RGMII IOSETs

SIGNALS	IOSET3		IOSET4	
	BALL	MUX	BALL	MUX
GMAC RGMII1				
rgmii1_txd3	C3	3		
rgmii1_txd2	C4	3		
rgmii1_txd1	B2	3		
rgmii1_txd0	D6	3		
rgmii1_rxd3	B3	3		
rgmii1_rxd2	B4	3		
rgmii1_rxd1	B5	3		
rgmii1_rxd0	A4	3		
rgmii1_rxctl	A3	3		
rgmii1_txc	D5	3		
rgmii1_txctl	C2	3		

Table 7-85. GMAC RGMII IOSETs (continued)

SIGNALS	IOSET3		IOSET4	
	BALL	MUX	BALL	MUX
rgmii1_rxc	C5	3		
GMAC RGMII0				
rgmii0_txd3			V7	0
rgmii0_txd2			U7	0
rgmii0_txd1			V6	0
rgmii0_txd0			U6	0
rgmii0_rxd3			V4	0
rgmii0_rxd2			V3	0
rgmii0_rxd1			Y2	0
rgmii0_rxd0			W2	0
rgmii0_txc			W9	0
rgmii0_rxctl			V5	0
rgmii0_rxc			U5	0
rgmii0_txctl			V9	0

NOTE

To configure the desired Manual IO Timing Mode the user must follow the steps described in section "*Manual IO Timing Modes*" of the Device TRM.

The associated registers to configure are listed in the **CFG REGISTER** column. For more information, see *Control Module* chapter in the device TRM.

Manual IO Timings Modes must be used to ensure some IO timings for GMAC. See Table 7-2 *Modes Summary* for a list of IO timings requiring the use of Manual IO Timings Modes. See Table 7-86 *Manual Functions Mapping for GMAC RGMII0* for a definition of the Manual modes.

Table 7-86 lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.

Table 7-86. Manual Functions Mapping for GMAC RGMII0

BALL	BALL NAME	GMAC_RGMII0_MANUAL1		CFG REGISTER	MUXMODE
		A_DELAY (ps)	G_DELAY (ps)		0
U5	rgmii0_rxc	413	0	CFG_RGMII0_RXC_IN	rgmii0_rxc
V5	rgmii0_rxctl	27	2296	CFG_RGMII0_RXCTL_IN	rgmii0_rxctl
W2	rgmii0_rxd0	3	1721	CFG_RGMII0_RXD0_IN	rgmii0_rxd0
Y2	rgmii0_rxd1	134	1786	CFG_RGMII0_RXD1_IN	rgmii0_rxd1
V3	rgmii0_rxd2	40	1966	CFG_RGMII0_RXD2_IN	rgmii0_rxd2
V4	rgmii0_rxd3	0	2057	CFG_RGMII0_RXD3_IN	rgmii0_rxd3
W9	rgmii0_txc	0	60	CFG_RGMII0_TXC_OUT	rgmii0_txc
V9	rgmii0_txctl	0	60	CFG_RGMII0_TXCTL_OUT	rgmii0_txctl
U6	rgmii0_txd0	0	60	CFG_RGMII0_TXD0_OUT	rgmii0_txd0
V6	rgmii0_txd1	0	0	CFG_RGMII0_TXD1_OUT	rgmii0_txd1
U7	rgmii0_txd2	0	60	CFG_RGMII0_TXD2_OUT	rgmii0_txd2
V7	rgmii0_txd3	0	120	CFG_RGMII0_TXD3_OUT	rgmii0_txd3

Manual IO Timings Modes must be used to ensure some IO timings for GMAC. See Table 7-2 *Modes Summary* for a list of IO timings requiring the use of Manual IO Timings Modes. See Table 7-87 *Manual Functions Mapping for GMAC RGMII1* for a definition of the Manual modes.

Table 7-87 lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.

Table 7-87. Manual Functions Mapping for GMAC RGMII1

BALL	BALL NAME	GMAC_RGMII1_MANUAL1		CFG REGISTER	MUXMODE
		A_DELAY (ps)	G_DELAY (ps)		3
C5	vin2a_d18	530	0	CFG_VIN2A_D18_IN	rgmii1_rxc
A3	vin2a_d19	71	1099	CFG_VIN2A_D19_IN	rgmii1_rxctl
B3	vin2a_d20	142	1337	CFG_VIN2A_D20_IN	rgmii1_rxd3
B4	vin2a_d21	114	1517	CFG_VIN2A_D21_IN	rgmii1_rxd2
B5	vin2a_d22	171	1331	CFG_VIN2A_D22_IN	rgmii1_rxd1
A4	vin2a_d23	0	1328	CFG_VIN2A_D23_IN	rgmii1_rxd0
D5	vin2a_d12	0	0	CFG_VIN2A_D12_OUT	rgmii1_txc
C2	vin2a_d13	170	0	CFG_VIN2A_D13_OUT	rgmii1_txctl
C3	vin2a_d14	150	0	CFG_VIN2A_D14_OUT	rgmii1_txd3
C4	vin2a_d15	0	0	CFG_VIN2A_D15_OUT	rgmii1_txd2
B2	vin2a_d16	60	0	CFG_VIN2A_D16_OUT	rgmii1_txd1
D6	vin2a_d17	60	0	CFG_VIN2A_D17_OUT	rgmii1_txd0

7.23 eMMC/SD/SDIO

The Device includes the following external memory interfaces 4 MultiMedia Card/Secure Digital/Secure Digital Input Output Interface (MMC/SD/SDIO).

NOTE

The eMMC/SD/SDIOi (i = 1 to 4) controller is also referred to as MMCi.

7.23.1 MMC1-SD Card Interface

MMC1 interface is compliant with the SD Standard v3.01 and it supports the following SD Card applications:

- Default speed, 4-bit data, SDR, half-cycle
- High speed, 4-bit data, SDR, half-cycle
- SDR12, 4-bit data, half-cycle
- SDR25, 4-bit data, half-cycle
- UHS-I SDR50, 4-bit data, half-cycle
- UHS-I SDR104, 4-bit data, half-cycle
- UHS-I DDR50, 4-bit data

NOTE

For more information, see *eMMC/SD/SDIO* chapter in the device TRM.

7.23.1.1 Default speed, 4-bit data, SDR, half-cycle

Table 7-88 and Table 7-89 present Timing requirements and Switching characteristics for MMC1 - Default Speed in receiver and transmitter mode (see Figure 7-54 and Figure 7-55).

Table 7-88. Timing Requirements for MMC1 - SD Card Default Speed Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
DSSD5	$t_{su(cmdV-clkH)}$	Setup time, mmc1_cmd valid before mmc1_clk rising clock edge	5.11		ns
DSSD6	$t_{h(clkH-cmdV)}$	Hold time, mmc1_cmd valid after mmc1_clk rising clock edge	20.46		ns
DSSD7	$t_{su(dV-clkH)}$	Setup time, mmc1_dat[3:0] valid before mmc1_clk rising clock edge	5.11		ns
DSSD8	$t_{h(clkH-dV)}$	Hold time, mmc1_dat[3:0] valid after mmc1_clk rising clock edge	20.46		ns

Table 7-89. Switching Characteristics for MMC1 - SD Card Default Speed Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
DSSD0	fop(clk)	Operating frequency, mmc1_clk		24	MHz
DSSD1	$t_{w(clkH)}$	Pulse duration, mmc1_clk high	0.5*P-0.185 (1)		ns
DSSD2	$t_{w(clkL)}$	Pulse duration, mmc1_clk low	0.5*P-0.185 (1)		ns
DSSD3	$t_{d(clkL-cmdV)}$	Delay time, mmc1_clk falling clock edge to mmc1_cmd transition	-14.93	14.93	ns
DSSD4	$t_{d(clkL-dV)}$	Delay time, mmc1_clk falling clock edge to mmc1_dat[3:0] transition	-14.93	14.93	ns

(1) P = output mmc1_clk period in ns

Figure 7-54. MMC/SD/SDIO in - Default Speed - Receiver Mode

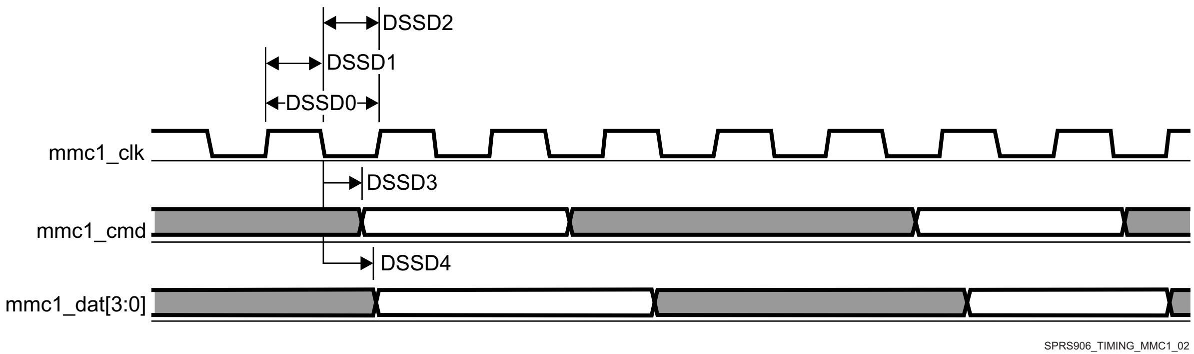


Figure 7-55. MMC/SD/SDIO in - Default Speed - Transmitter Mode

7.23.1.2 High speed, 4-bit data, SDR, half-cycle

Table 7-90 and Table 7-91 present Timing requirements and Switching characteristics for MMC1 - High Speed in receiver and transmitter mode (see Figure 7-56 and Figure 7-57).

Table 7-90. Timing Requirements for MMC1 - SD Card High Speed

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
HSSD3	$t_{su(cmdV-clkH)}$	Setup time, mmc1_cmd valid before mmc1_clk rising clock edge	5.3		ns
HSSD4	$t_{h(clkH-cmdV)}$	Hold time, mmc1_cmd valid after mmc1_clk rising clock edge	2.6		ns
HSSD7	$t_{su(dV-clkH)}$	Setup time, mmc1_dat[3:0] valid before mmc1_clk rising clock edge	5.3		ns
HSSD8	$t_{h(clkH-dV)}$	Hold time, mmc1_dat[3:0] valid after mmc1_clk rising clock edge	2.6		ns

Table 7-91. Switching Characteristics for MMC1 - SD Card High Speed

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
HSSD1	fop(clk)	Operating frequency, mmc1_clk		48	MHz
HSSD2H	$t_{w(clkH)}$	Pulse duration, mmc1_clk high	0.5*P-0.185 [(1)]		ns
HSSD2L	$t_{w(clkL)}$	Pulse duration, mmc1_clk low	0.5*P-0.185 [(1)]		ns
HSSD5	$t_{d(clkL-cmdV)}$	Delay time, mmc1_clk falling clock edge to mmc1_cmd transition	-7.6	3.6	ns
HSSD6	$t_{d(clkL-dV)}$	Delay time, mmc1_clk falling clock edge to mmc1_dat[3:0] transition	-7.6	3.6	ns

(1) P = output mmc1_clk period in ns

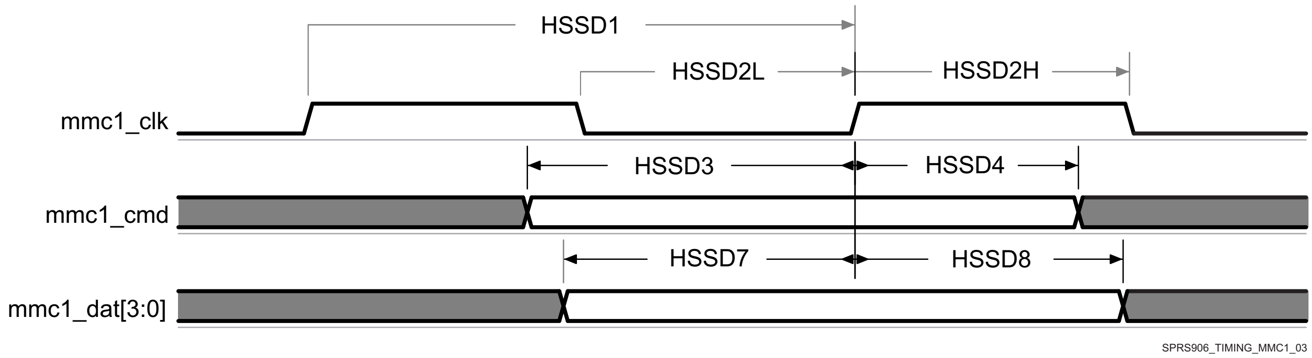


Figure 7-56. MMC/SD/SDIO in - High Speed - Receiver Mode

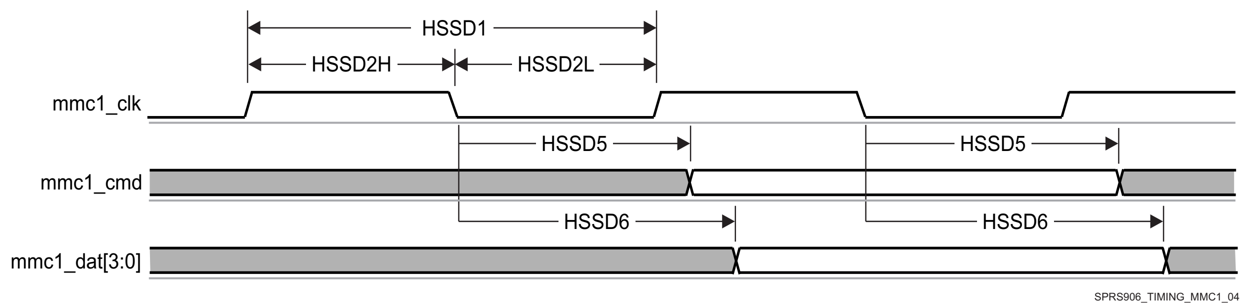


Figure 7-57. MMC/SD/SDIO in - High Speed - Transmitter Mode

7.23.1.3 SDR12, 4-bit data, half-cycle

Table 7-92 and Table 7-93 present Timing requirements and Switching characteristics for MMC1 - SDR12 in receiver and transmitter mode (see Figure 7-58 and Figure 7-59).

Table 7-92. Timing Requirements for MMC1 - SD Card SDR12 Mode

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
SDR125	$t_{su(cmdV-clkH)}$	Setup time, mmc1_cmd valid before mmc1_clk rising clock edge		25.99		ns
SDR126	$t_{h(clkH-cmdV)}$	Hold time, mmc1_cmd valid after mmc1_clk rising clock edge	Pad Loopback Clock	1.6		ns
			Internal Loopback Clock	1.6		ns
SDR127	$t_{su(dV-clkH)}$	Setup time, mmc1_dat[3:0] valid before mmc1_clk rising clock edge		25.99		ns
SDR128	$t_{h(clkH-dV)}$	Hold time, mmc1_dat[3:0] valid after mmc1_clk rising clock edge	Pad Loopback Clock	1.6		ns
			Internal Loopback Clock	1.6		ns

Table 7-93. Switching Characteristics for MMC1 - SD Card SDR12 Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
SDR120	fop(clk)	Operating frequency, mmc1_clk		24	MHz
SDR121	$t_{w(clkH)}$	Pulse duration, mmc1_clk high	0.5*P-0.185 (1)		ns
SDR122	$t_{w(clkL)}$	Pulse duration, mmc1_clk low	0.5*P-0.185(1)		ns
SDR123	$t_{d(clkL-cmdV)}$	Delay time, mmc1_clk falling clock edge to mmc1_cmd transition	-19.13	16.93	ns
SDR124	$t_{d(clkL-dV)}$	Delay time, mmc1_clk falling clock edge to mmc1_dat[3:0] transition	-19.13	16.93	ns

(1) P = output mmc1_clk period in ns

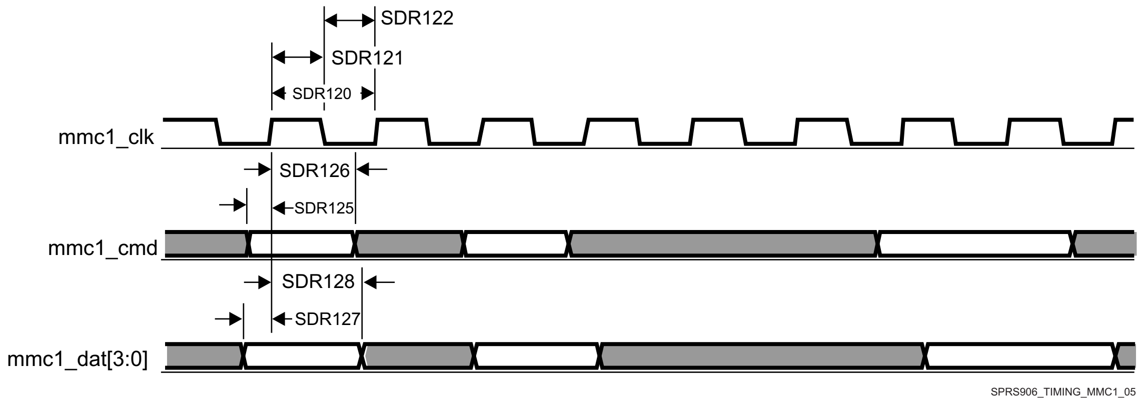


Figure 7-58. MMC/SD/SDIO in - High Speed SDR12 - Receiver Mode

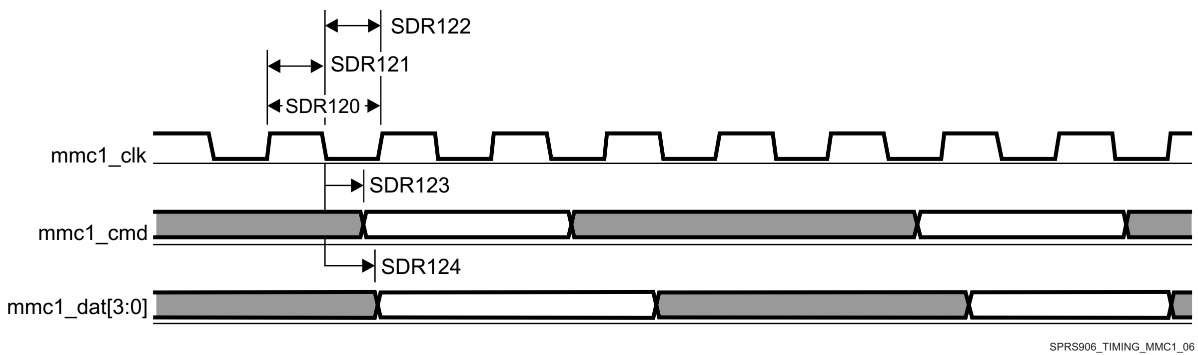


Figure 7-59. MMC/SD/SDIO in - High Speed SDR12 - Transmitter Mode

7.23.1.4 SDR25, 4-bit data, half-cycle

Table 7-94 and Table 7-95 present Timing requirements and Switching characteristics for MMC1 - SDR25 in receiver and transmitter mode (see Figure 7-60 and Figure 7-61).

Table 7-94. Timing Requirements for MMC1 - SD Card SDR25 Mode

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
SDR253	$t_{su(cmdV-clkH)}$	Setup time, mmc1_cmd valid before mmc1_clk rising clock edge		5.3		ns
SDR254	$t_{h(clkH-cmdV)}$	Hold time, mmc1_cmd valid after mmc1_clk rising clock edge		1.6		ns
SDR257	$t_{su(dV-clkH)}$	Setup time, mmc1_dat[3:0] valid before mmc1_clk rising clock edge		5.3		ns
SDR258	$t_{h(clkH-dV)}$	Hold time, mmc1_dat[3:0] valid after mmc1_clk rising clock edge	Pad Loopback Clock	1.6		ns
			Internal Loopback Clock	1.6		ns

Table 7-95. Switching Characteristics for MMC1 - SD Card SDR25 Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
SDR251	fop(clk)	Operating frequency, mmc1_clk		48	MHz
SDR252H	$t_{w(clkH)}$	Pulse duration, mmc1_clk high	0.5*P-0.185 (1)		ns
SDR252L	$t_{w(clkL)}$	Pulse duration, mmc1_clk low	0.5*P-0.185 (1)		ns
SDR255	$t_{d(clkL-cmdV)}$	Delay time, mmc1_clk falling clock edge to mmc1_cmd transition	-8.8	6.6	ns

Table 7-95. Switching Characteristics for MMC1 - SD Card SDR25 Mode (continued)

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
SDR256	$t_{d(clkL-dV)}$	Delay time, mmc1_clk falling clock edge to mmc1_dat[3:0] transition	-8.8	6.6	ns

(1) P = output mmc1_clk period in ns

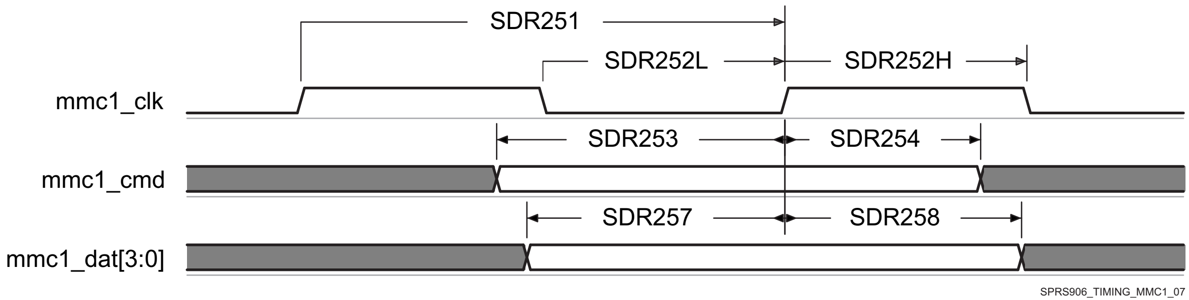


Figure 7-60. MMC/SD/SDIO in - High Speed SDR25 - Receiver Mode

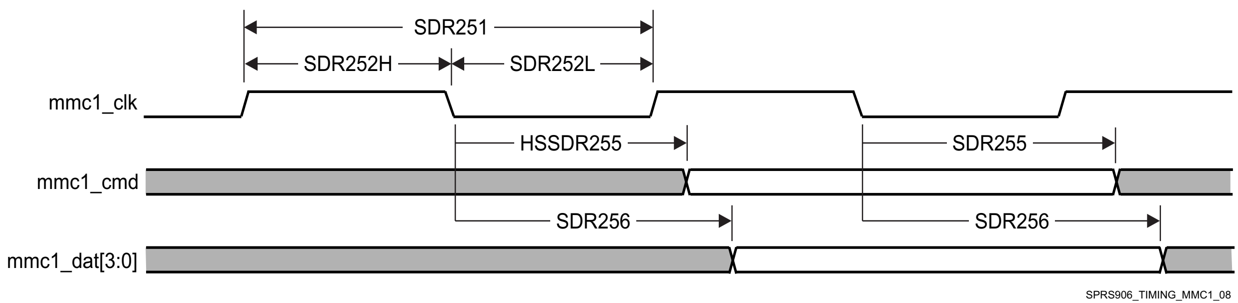


Figure 7-61. MMC/SD/SDIO in - High Speed SDR25 - Transmitter Mode

7.23.1.5 UHS-I SDR50, 4-bit data, half-cycle

Table 7-96 and Table 7-97 present Timing requirements and Switching characteristics for MMC1 - SDR50 in receiver and transmitter mode (see Figure 7-62 and Figure 7-63).

Table 7-96. Timing Requirements for MMC1 - SD Card SDR50 Mode

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
SDR503	$t_{su(cmdV-clkH)}$	Setup time, mmc1_cmd valid before mmc1_clk rising clock edge		1.48		ns
SDR504	$t_{h(clkH-cmdV)}$	Hold time, mmc1_cmd valid after mmc1_clk rising clock edge		1.6		ns
SDR507	$t_{su(dV-clkH)}$	Setup time, mmc1_dat[3:0] valid before mmc1_clk rising clock edge		1.48		ns
SDR508	$t_{h(clkH-dV)}$	Hold time, mmc1_dat[3:0] valid after mmc1_clk rising clock edge	Pad Loopback Clock	1.6		ns
			Internal Loopback Clock	1.6		ns

Table 7-97. Switching Characteristics for MMC1 - SD Card SDR50 Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
SDR501	fop(clk)	Operating frequency, mmc1_clk		96	MHz
SDR502H	$t_{w(clkH)}$	Pulse duration, mmc1_clk high	0.5 × P - 0.185 (1)		ns
SDR502L	$t_{w(clkL)}$	Pulse duration, mmc1_clk low	0.5 × P - 0.185 (1)		ns
SDR505	$t_{d(clkL-cmdV)}$	Delay time, mmc1_clk falling clock edge to mmc1_cmd transition	-3.66	1.46	ns
SDR506	$t_{d(clkL-dV)}$	Delay time, mmc1_clk falling clock edge to mmc1_dat[3:0] transition	-3.66	1.46	ns

(1) P = output mmc1_clk period in ns

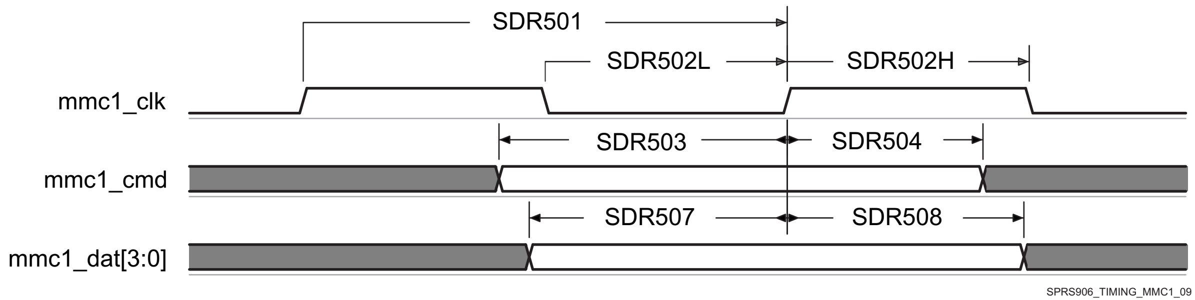


Figure 7-62. MMC/SD/SDIO in - High Speed SDR50 - Receiver Mode

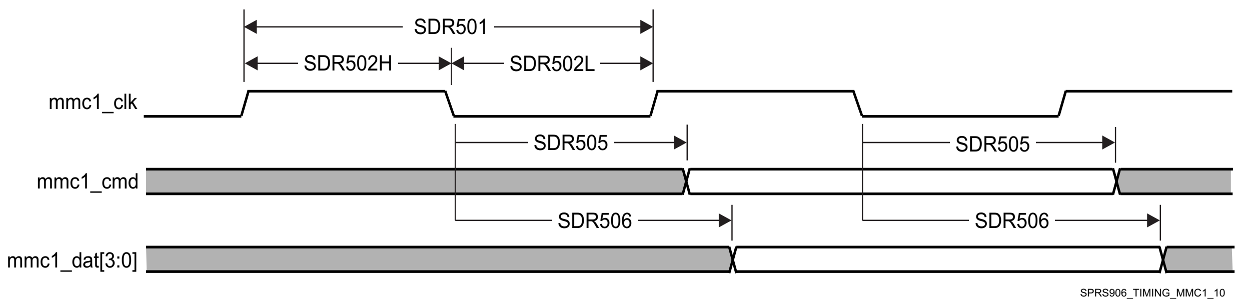


Figure 7-63. MMC/SD/SDIO in - High Speed SDR50 - Transmitter Mode

7.23.1.6 UHS-I SDR104, 4-bit data, half-cycle

Table 7-98 presents Timing requirements and Switching characteristics for MMC1 - SDR104 in receiver and transmitter mode (see Figure 7-64 and Figure 7-65).

Table 7-98. Switching Characteristics for MMC1 - SD Card SDR104 Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
SDR1041	fop(clk)	Operating frequency, mmc1_clk		192	MHz
SDR1042 H	$t_{w(clkH)}$	Pulse duration, mmc1_clk high	0.5*P-0.185 (1)		ns
SDR1042 L	$t_{w(clkL)}$	Pulse duration, mmc1_clk low	0.5*P-0.185 (1)		ns
SDR1045	$t_{d(clkL-cmdV)}$	Delay time, mmc1_clk falling clock edge to mmc1_cmd transition	-1.09	0.49	ns
SDR1046	$t_{d(clkL-dV)}$	Delay time, mmc1_clk falling clock edge to mmc1_dat[3:0] transition	-1.09	0.49	ns

(1) P = output mmc1_clk period in ns

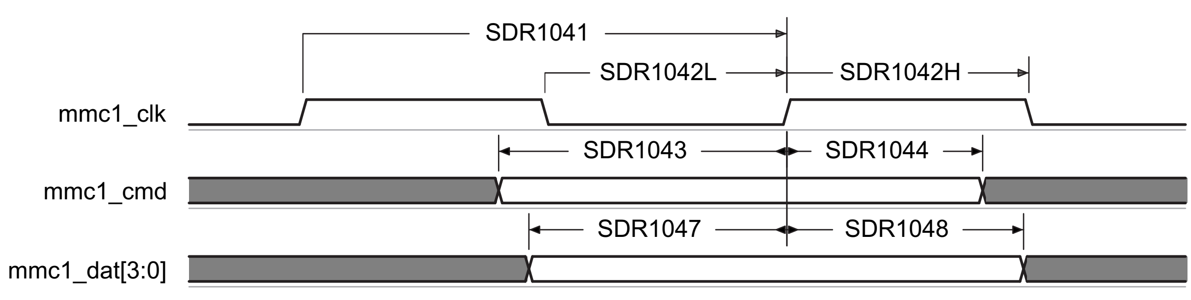


Figure 7-64. MMC/SD/SDIO in - High Speed SDR104 - Receiver Mode

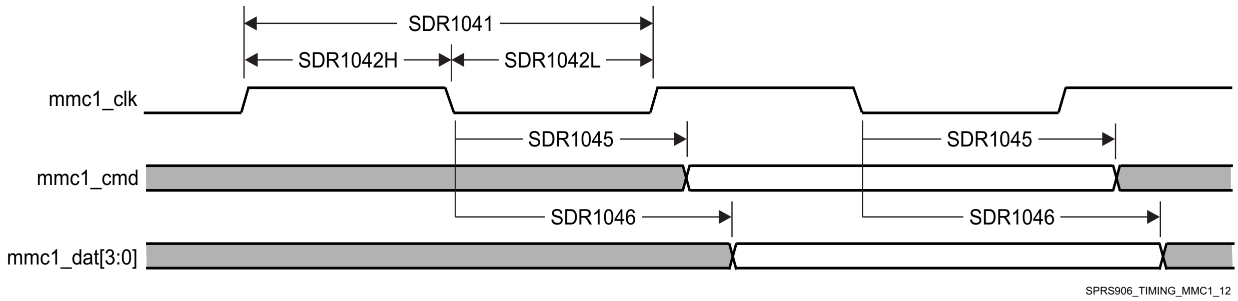


Figure 7-65. MMC/SD/SDIO in - High Speed SDR104 - Transmitter Mode

7.23.1.7 UHS-I DDR50, 4-bit data

Table 7-99 and Table 7-100 present Timing requirements and Switching characteristics for MMC1 - DDR50 in receiver and transmitter mode (see Figure 7-66 and Figure 7-67).

Table 7-99. Timing Requirements for MMC1 - SD Card DDR50 Mode

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
DDR505	$t_{su(cmdV-clk)}$	Setup time, mmc1_cmd valid before mmc1_clk transition		1.79		ns
DDR506	$t_{h(clk-cmdV)}$	Hold time, mmc1_cmd valid after mmc1_clk transition		1.6		ns
DDR507	$t_{su(dV-clk)}$	Setup time, mmc1_dat[3:0] valid before mmc1_clk transition	Pad Loopback	1.79		ns
			Internal Loopback	1.79		ns
DDR508	$t_{h(clk-dV)}$	Hold time, mmc1_dat[3:0] valid after mmc1_clk transition	Pad Loopback	1.6		ns
			Internal Loopback	1.6		ns

Table 7-100. Switching Characteristics for MMC1 - SD Card DDR50 Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
DDR500	fop(clk)	Operating frequency, mmc1_clk		48	MHz
DDR501	$t_{w(clkH)}$	Pulse duration, mmc1_clk high	0.5*P-0.185 (1)		ns
DDR502	$t_{w(clkL)}$	Pulse duration, mmc1_clk low	0.5*P-0.185 (1)		ns
DDR503	$t_{d(clk-cmdV)}$	Delay time, mmc1_clk transition to mmc1_cmd transition	1.225	6.6	ns
DDR504	$t_{d(clk-dV)}$	Delay time, mmc1_clk transition to mmc1_dat[3:0] transition	1.225	6.6	ns

(1) P = output mmc1_clk period in ns

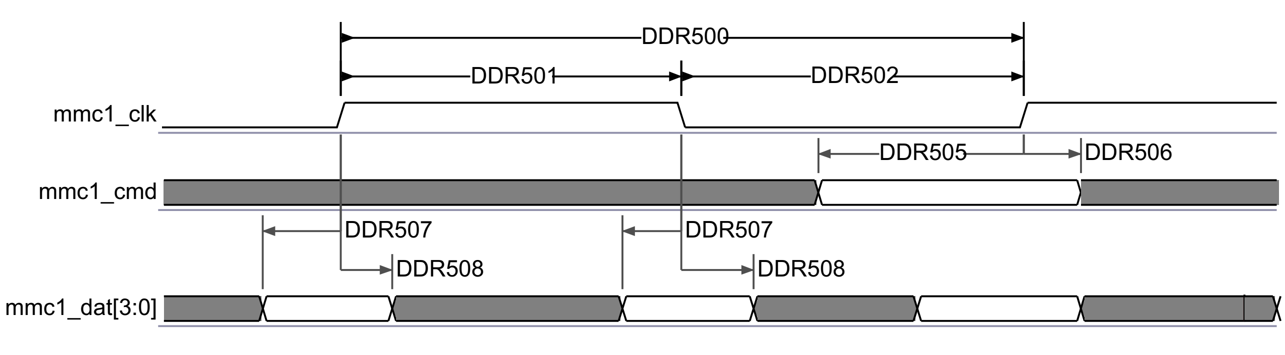


Figure 7-66. SDMMC - High Speed SD - DDR - Data/Command Receive

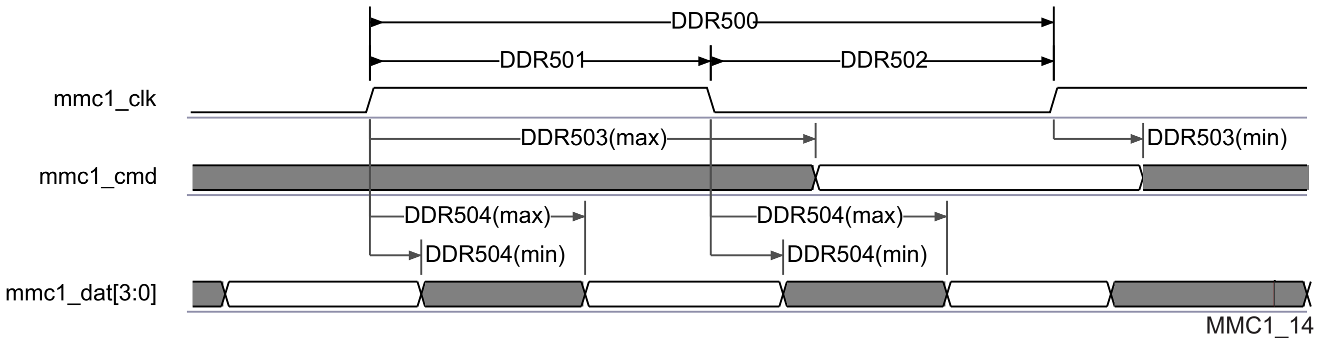


Figure 7-67. SDMMC - High Speed SD - DDR - Data/Command Transmit

NOTE

To configure the desired virtual mode the user must set MODESELECT bit and DELAYMODE bit field for each corresponding pad control register.

The pad control registers are presented in Table 4-3 and described in Device TRM, *Control Module Chapter*.

Virtual IO Timings Modes must be used to ensure some IO timings for MMC1. See Table 7-2 *Modes Summary* for a list of IO timings requiring the use of Virtual IO Timings Modes. See Table 7-101 *Virtual Functions Mapping for MMC1* for a definition of the Virtual modes.

Table 7-101 presents the values for DELAYMODE bit field.

Table 7-101. Virtual Functions Mapping for MMC1

BALL	BALL NAME	Delay Mode Value				MUXMODE
		MMC1_ VIRTUAL1	MMC1_ VIRTUAL4	MMC1_ VIRTUAL5	MMC1_ VIRTUAL6	0
W6	mmc1_clk	15	12	11	10	mmc1_clk
Y6	mmc1_cmd	15	12	11	10	mmc1_cmd
AA6	mmc1_dat0	15	12	11	10	mmc1_dat0
Y4	mmc1_dat1	15	12	11	10	mmc1_dat1
AA5	mmc1_dat2	15	12	11	10	mmc1_dat2
Y3	mmc1_dat3	15	12	11	10	mmc1_dat3

NOTE

To configure the desired Manual IO Timing Mode the user must follow the steps described in section Manual IO Timing Modes of the Device TRM.

The associated registers to configure are listed in the **CFG REGISTER** column. For more information, see *Control Module* chapter in the device TRM.

Manual IO Timings Modes must be used to ensure some IO timings for MMC1. See Table 7-2 *Modes Summary* for a list of IO timings requiring the use of Manual IO Timings Modes. See Table 7-102 *Manual Functions Mapping for MMC1* for a definition of the Manual modes.

Table 7-102 lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.

Table 7-102. Manual Functions Mapping for MMC1

BALL	BALL NAME	MMC1_MANUAL1		MMC1_MANUAL2		CFG REGISTER	MUXMODE
		A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)		0
W6	mmc1_clk	588	0	-	-	CFG_MMC1_CLK_IN	mmc1_clk
Y6	mmc1_cmd	1000	0	-	-	CFG_MMC1_CMD_IN	mmc1_cmd
AA6	mmc1_dat0	1375	0	-	-	CFG_MMC1_DAT0_IN	mmc1_dat0
Y4	mmc1_dat1	1000	0	-	-	CFG_MMC1_DAT1_IN	mmc1_dat1
AA5	mmc1_dat2	1000	0	-	-	CFG_MMC1_DAT2_IN	mmc1_dat2
Y3	mmc1_dat3	1000	0	-	-	CFG_MMC1_DAT3_IN	mmc1_dat3
W6	mmc1_clk	1230	0	520	320	CFG_MMC1_CLK_OUT	mmc1_clk
Y6	mmc1_cmd	0	0	0	0	CFG_MMC1_CMD_OUT	mmc1_cmd
AA6	mmc1_dat0	56	0	40	0	CFG_MMC1_DAT0_OUT	mmc1_dat0
Y4	mmc1_dat1	76	0	83	0	CFG_MMC1_DAT1_OUT	mmc1_dat1
AA5	mmc1_dat2	91	0	98	0	CFG_MMC1_DAT2_OUT	mmc1_dat2
Y3	mmc1_dat3	99	0	106	0	CFG_MMC1_DAT3_OUT	mmc1_dat3
Y6	mmc1_cmd	0	0	51	0	CFG_MMC1_CMD_OEN	mmc1_cmd
AA6	mmc1_dat0	0	0	0	0	CFG_MMC1_DAT0_OEN	mmc1_dat0
Y4	mmc1_dat1	0	0	363	0	CFG_MMC1_DAT1_OEN	mmc1_dat1
AA5	mmc1_dat2	0	0	199	0	CFG_MMC1_DAT2_OEN	mmc1_dat2
Y3	mmc1_dat3	0	0	273	0	CFG_MMC1_DAT3_OEN	mmc1_dat3

7.23.2 MMC2 - eMMC

MMC2 interface is compliant with the JC64 eMMC Standard v4.5 and it supports the following eMMC applications:

- Standard JC64 SDR, 8-bit data, half cycle
- High Speed JC64 SDR, 8-bit data, half cycle
- High Speed HS200 JEDS84, 8-bit data, half cycle
- High Speed JC64 DDR, 8-bit data

NOTE

For more information, see *eMMC/SD/SDIO* chapter in the device TRM.

7.23.2.1 Standard JC64 SDR, 8-bit data, half cycle

Table 7-103 and Table 7-104 present Timing requirements and Switching characteristics for MMC2 - Standart SDR in receiver and transmitter mode (see Figure 7-68 and Figure 7-69).

Table 7-103. Timing Requirements for MMC2 - JC64 Standard SDR Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
SSDR5	$t_{su(cmdV-clkH)}$	Setup time, mmc2_cmd valid before mmc2_clk rising clock edge	13.19		ns
SSDR6	$t_{h(clkH-cmdV)}$	Hold time, mmc2_cmd valid after mmc2_clk rising clock edge	8.4		ns
SSDR7	$t_{su(dV-clkH)}$	Setup time, mmc2_dat[7:0] valid before mmc2_clk rising clock edge	13.19		ns
SSDR8	$t_{h(clkH-dV)}$	Hold time, mmc2_dat[7:0] valid after mmc2_clk rising clock edge	8.4		ns

Table 7-104. Switching Characteristics for MMC2 - JC64 Standard SDR Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
SSDR1	fop(clk)	Operating frequency, mmc2_clk		24	MHz
SSDR2H	$t_{w(clkH)}$	Pulse duration, mmc2_clk high	0.5*P-0.172 (1)		ns
SSDR2L	$t_{w(clkL)}$	Pulse duration, mmc2_clk low	0.5*P-0.172 (1)		ns
SSDR3	$t_{d(clkL-cmdV)}$	Delay time, mmc2_clk falling clock edge to mmc2_cmd transition	-16.96	16.96	ns
SSDR4	$t_{d(clkL-dV)}$	Delay time, mmc2_clk falling clock edge to mmc2_dat[7:0] transition	-16.96	16.96	ns

(1) P = output mmc2_clk period in ns

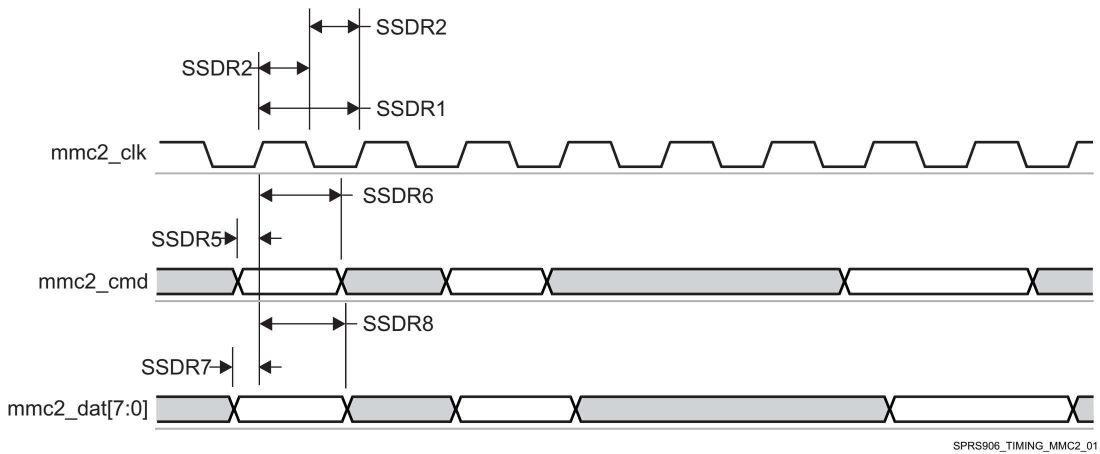


Figure 7-68. MMC/SD/SDIO in - Standard JC64 - Receiver Mode

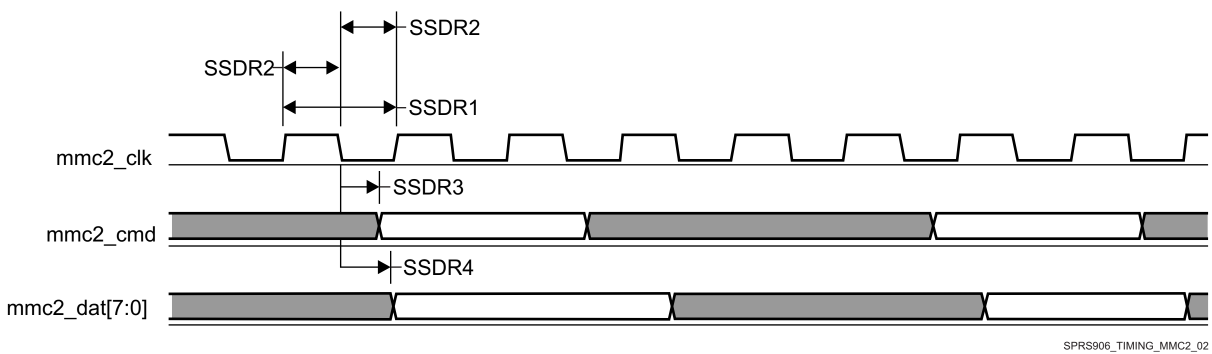


Figure 7-69. MMC/SD/SDIO in - Standard JC64 - Transmitter Mode

7.23.2.2 High Speed JC64 SDR, 8-bit data, half cycle

Table 7-105 and Table 7-106 present Timing requirements and Switching characteristics for MMC2 - High speed SDR in receiver and transmitter mode (see Figure 7-70 and Figure 7-71).

Table 7-105. Timing Requirements for MMC2 - JC64 High Speed SDR Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
JC643	$t_{su(cmdV-clkH)}$	Setup time, mmc2_cmd valid before mmc2_clk rising clock edge	5.6		ns
JC644	$t_{h(clkH-cmdV)}$	Hold time, mmc2_cmd valid after mmc2_clk rising clock edge	2.6		ns
JC647	$t_{su(dV-clkH)}$	Setup time, mmc2_dat[7:0] valid before mmc2_clk rising clock edge	5.6		ns
JC648	$t_{h(clkH-dV)}$	Hold time, mmc2_dat[7:0] valid after mmc2_clk rising clock edge	2.6		ns

Table 7-106. Switching Characteristics for MMC2 - JC64 High Speed SDR Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
JC641	fop(clk)	Operating frequency, mmc2_clk		48	MHz
JC642H	$t_{w(clkH)}$	Pulse duration, mmc2_clk high	0.5*P-0.172 (1)		ns
JC642L	$t_{w(clkL)}$	Pulse duration, mmc2_clk low	0.5*P-0.172 (1)		ns
JC645	$t_{d(clkL-cmdV)}$	Delay time, mmc2_clk falling clock edge to mmc2_cmd transition	-6.64	6.64	ns
JC646	$t_{d(clkL-dV)}$	Delay time, mmc2_clk falling clock edge to mmc2_dat[7:0] transition	-6.64	6.64	ns

(1) P = output mmc2_clk period in ns

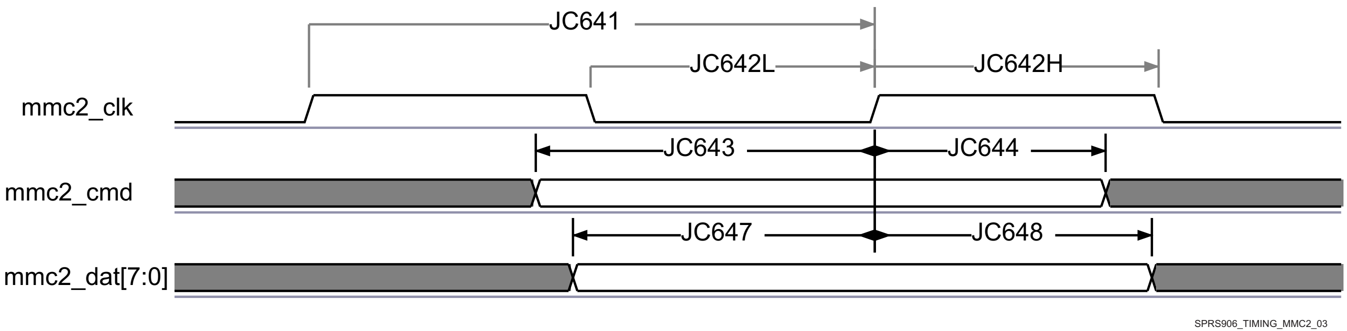


Figure 7-70. MMC/SD/SDIO in - High Speed JC64 - Receiver Mode

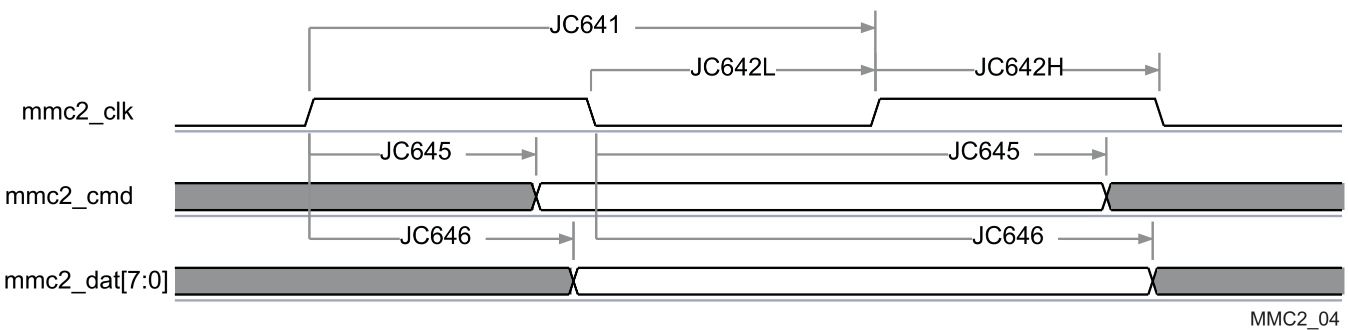


Figure 7-71. MMC/SD/SDIO in - High Speed JC64 - Transmitter Mode

7.23.2.3 High Speed HS200 JEDS84, 8-bit data, half cycle

Table 7-107 presents Switching characteristics for MMC2 - HS200 in transmitter mode (see Figure 7-72).

Table 7-107. Switching Characteristics for MMC2 - JEDS84 HS200 Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
HS2001	fop(clk)	Operating frequency, mmc2_clk		192	MHz
HS2002H	$t_{w(clkH)}$	Pulse duration, mmc2_clk high	0.5*P-0.172 (1)		ns
HS2002L	$t_{w(clkL)}$	Pulse duration, mmc2_clk low	0.5*P-0.172 (1)		ns
HS2005	$t_{d(clkL-cmdV)}$	Delay time, mmc2_clk falling clock edge to mmc2_cmd transition	-1.136	0.536	ns
HS2006	$t_{d(clkL-dV)}$	Delay time, mmc2_clk falling clock edge to mmc2_dat[7:0] transition	-1.136	0.536	ns

(1) P = output mmc2_clk period in ns

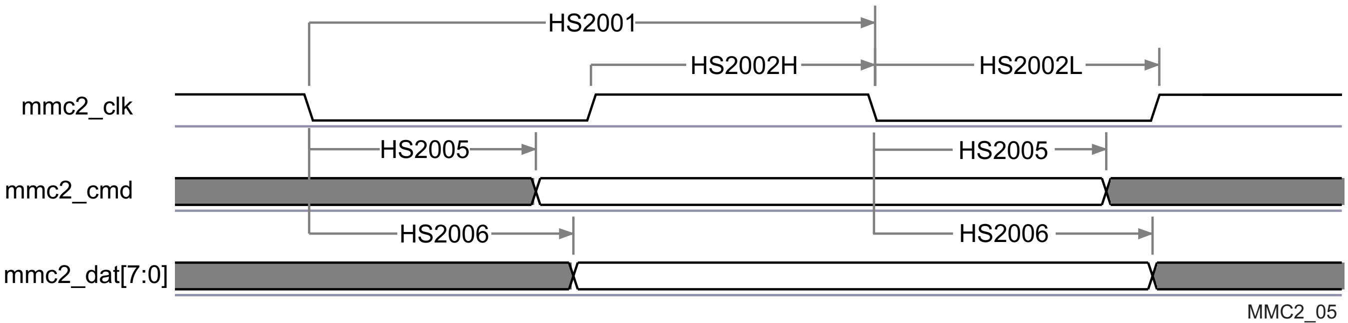


Figure 7-72. eMMC in - HS200 SDR - Transmitter Mode

7.23.2.4 High Speed JC64 DDR, 8-bit data

Table 7-108 and Table 7-109 present Timing requirements and Switching characteristics for MMC2 - High speed DDR in receiver and transmitter mode (see Figure 7-73 and Figure 7-74).

Table 7-108. Timing Requirements for MMC2 - JC64 High Speed DDR Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
DDR3	$t_{su(cmdV-clk)}$	Setup time, mmc2_cmd valid before mmc2_clk transition	1.8		ns
DDR4	$t_{h(clk-cmdV)}$	Hold time, mmc2_cmd valid after mmc2_clk transition	1.6		ns
DDR7	$t_{su(dV-clk)}$	Setup time, mmc2_dat[7:0] valid before mmc2_clk transition	1.8		ns
DDR8	$t_{h(clk-dV)}$	Hold time, mmc2_dat[7:0] valid after mmc2_clk transition	1.6		ns

Table 7-109. Switching Characteristics for MMC2 - JC64 High Speed DDR Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
DDR1	fop(clk)	Operating frequency, mmc2_clk		48	MHz
DDR2H	$t_{w(clkH)}$	Pulse duration, mmc2_clk high	0.5 × P - 0.172	(1)	ns
DDR2L	$t_{w(clkL)}$	Pulse duration, mmc2_clk low	0.5 × P - 0.172	(1)	ns
DDR5	$t_{d(clk-cmdV)}$	Delay time, mmc2_clk transition to mmc2_cmd transition	3.4	7.14	ns
DDR6	$t_{d(clk-dV)}$	Delay time, mmc2_clk transition to mmc2_dat[7:0] transition	2.9	7.14	ns

(1) P = output mmc2_clk period in ns

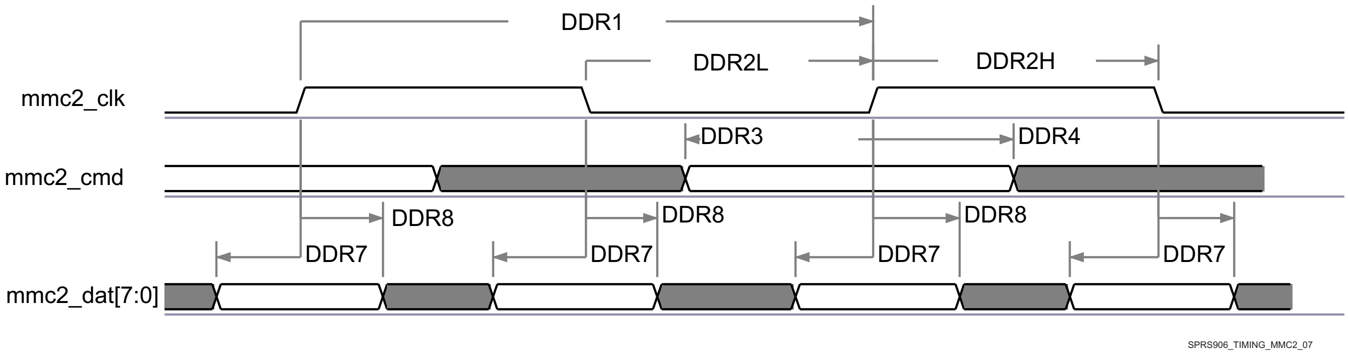


Figure 7-73. MMC/SD/SDIO in - High Speed DDR JC64 - Receiver Mode

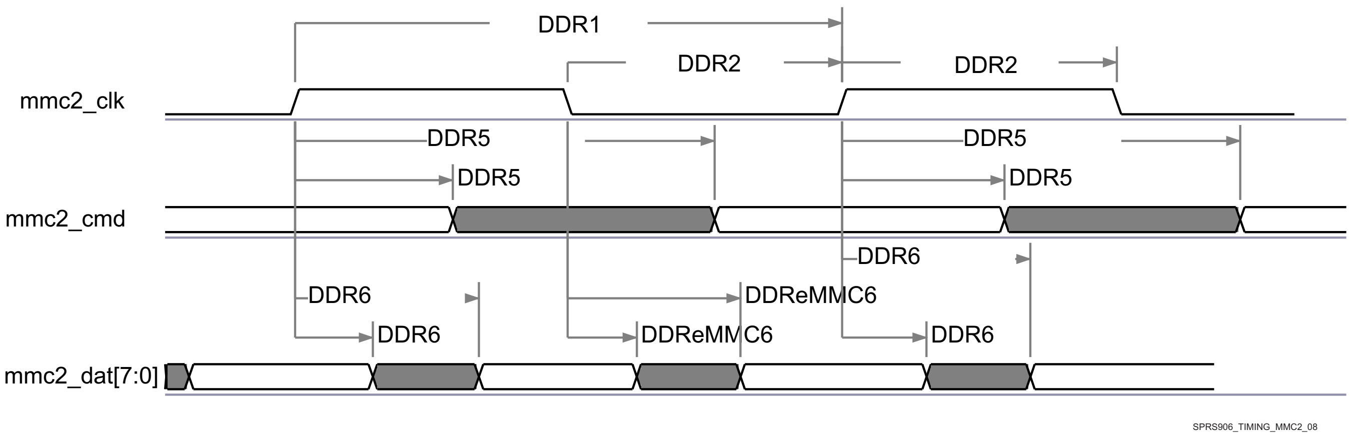


Figure 7-74. MMC/SD/SDIO in - High Speed DDR JC64 - Transmitter Mode

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NOTE

To configure the desired virtual mode the user must set MODESELECT bit and DELAYMODE bit field for each corresponding pad control register.

The pad control registers are presented in Table 4-3 and described in Device TRM, *Control Module Chapter*.

Virtual IO Timings Modes must be used to ensure some IO timings for MMC2. See Table 7-2 *Modes Summary* for a list of IO timings requiring the use of Virtual IO Timings Modes. See Table 7-110 *Virtual Functions Mapping for MMC2* for a definition of the Virtual modes.

Table 7-110 presents the values for DELAYMODE bit field.

Table 7-110. Virtual Functions Mapping for MMC2

BALL	BALL NAME	Delay Mode Value	MUXMODE
		MMC2_VIRTUAL2	1
H6	gpmc_cs1	13	mmc2_cmd
K7	gpmc_a19	13	mmc2_dat4
M7	gpmc_a20	13	mmc2_dat5
J5	gpmc_a21	13	mmc2_dat6
K6	gpmc_a22	13	mmc2_dat7
J7	gpmc_a23	13	mmc2_clk

Table 7-110. Virtual Functions Mapping for MMC2 (continued)

BALL	BALL NAME	Delay Mode Value	MUXMODE
		MMC2_VIRTUAL2	1
J4	gpmc_a24	13	mmc2_dat0
J6	gpmc_a25	13	mmc2_dat1
H4	gpmc_a26	13	mmc2_dat2
H5	gpmc_a27	13	mmc2_dat3

NOTE

To configure the desired Manual IO Timing Mode the user must follow the steps described in section Manual IO Timing Modes of the Device TRM.

The associated registers to configure are listed in the **CFG REGISTER** column. For more information, see *Control Module* chapter in the device TRM.

Manual IO Timings Modes must be used to ensure some IO timings for MMC2. See Table 7-2 *Modes Summary* for a list of IO timings requiring the use of Manual IO Timings Modes. See Table 7-111 *Manual Functions Mapping for MMC2* for a definition of the Manual modes.

Table 7-111 lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.

Table 7-111. Manual Functions Mapping for MMC2

BALL	BALL NAME	MMC2_MANUAL1		MMC2_MANUAL2		MMC2_MANUAL3		CFG REGISTER	MUXMODE
		A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)		1
K7	gpmc_a19	0	0	0	14	-	-	CFG_GPMC_A19_IN	mmc2_dat4
M7	gpmc_a20	119	0	127	0	-	-	CFG_GPMC_A20_IN	mmc2_dat5
J5	gpmc_a21	0	0	22	0	-	-	CFG_GPMC_A21_IN	mmc2_dat6
K6	gpmc_a22	18	0	72	0	-	-	CFG_GPMC_A22_IN	mmc2_dat7
J7	gpmc_a23	894	0	410	4000	-	-	CFG_GPMC_A23_IN	mmc2_clk
J4	gpmc_a24	30	0	82	0	-	-	CFG_GPMC_A24_IN	mmc2_dat0
J6	gpmc_a25	0	0	0	0	-	-	CFG_GPMC_A25_IN	mmc2_dat1
H4	gpmc_a26	23	0	77	0	-	-	CFG_GPMC_A26_IN	mmc2_dat2
H5	gpmc_a27	0	0	0	0	-	-	CFG_GPMC_A27_IN	mmc2_dat3
H6	gpmc_cs1	0	0	0	0	-	-	CFG_GPMC_CS1_IN	mmc2_cmd
K7	gpmc_a19	152	0	152	0	285	0	CFG_GPMC_A19_OUT	mmc2_dat4
M7	gpmc_a20	206	0	206	0	189	0	CFG_GPMC_A20_OUT	mmc2_dat5
J5	gpmc_a21	78	0	78	0	0	120	CFG_GPMC_A21_OUT	mmc2_dat6
K6	gpmc_a22	2	0	2	0	0	70	CFG_GPMC_A22_OUT	mmc2_dat7
J7	gpmc_a23	266	0	266	0	730	360	CFG_GPMC_A23_OUT	mmc2_clk
J4	gpmc_a24	0	0	0	0	0	0	CFG_GPMC_A24_OUT	mmc2_dat0
J6	gpmc_a25	0	0	0	0	0	0	CFG_GPMC_A25_OUT	mmc2_dat1
H4	gpmc_a26	43	0	43	0	70	0	CFG_GPMC_A26_OUT	mmc2_dat2
H5	gpmc_a27	0	0	0	0	0	0	CFG_GPMC_A27_OUT	mmc2_dat3
H6	gpmc_cs1	0	0	0	0	0	120	CFG_GPMC_CS1_OUT	mmc2_cmd
K7	gpmc_a19	0	0	0	0	0	0	CFG_GPMC_A19_OEN	mmc2_dat4
M7	gpmc_a20	0	0	0	0	231	0	CFG_GPMC_A20_OEN	mmc2_dat5
J5	gpmc_a21	0	0	0	0	39	0	CFG_GPMC_A21_OEN	mmc2_dat6
K6	gpmc_a22	0	0	0	0	91	0	CFG_GPMC_A22_OEN	mmc2_dat7
J4	gpmc_a24	0	0	0	0	176	0	CFG_GPMC_A24_OEN	mmc2_dat0

Table 7-111. Manual Functions Mapping for MMC2 (continued)

BALL	BALL NAME	MMC2_MANUAL1		MMC2_MANUAL2		MMC2_MANUAL3		CFG REGISTER	MUXMODE
		A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)		1
J6	gpmc_a25	0	0	0	0	0	0	CFG_GPMC_A25_OEN	mmc2_dat1
H4	gpmc_a26	0	0	0	0	101	0	CFG_GPMC_A26_OEN	mmc2_dat2
H5	gpmc_a27	0	0	0	0	0	0	CFG_GPMC_A27_OEN	mmc2_dat3
H6	gpmc_cs1	0	0	0	0	360	0	CFG_GPMC_CS1_OEN	mmc2_cmd

7.23.3 MMC3 and MMC4-SDIO/SD

MMC3 and MMC4 interfaces are compliant with the SDIO3.0 standard v1.0, SD Part E1 and for generic SDIO devices, it supports the following applications:

- MMC3 8-bit data and MMC4 4-bit data, SD Default speed, SDR
- MMC3 8-bit data and MMC4 4-bit data, SD High speed, SDR
- MMC3 8-bit data and MMC4 4-bit data, UHS-1 SDR12 (SD Standard v3.01), 4-bit data, SDR, half cycle
- MMC3 8-bit data and MMC4 4-bit data, UHS-I SDR25 (SD Standard v3.01), 4-bit data, SDR, half cycle
- MMC3 8-bit data, UHS-I SDR50

NOTE

The eMMC/SD/SDIOj (j = 3 to 4) controller is also referred to as MMCj.

NOTE

For more information, see *eMMC/SD/SDIO* chapter in the device TRM.

7.23.3.1 MMC3 and MMC4, SD Default Speed

Figure 7-75, Figure 7-76, and Table 7-112 through Table 7-115 present Timing requirements and Switching characteristics for MMC3 and MMC4 - SD Default speed in receiver and transmitter mode.

Table 7-112. Timing Requirements for MMC3 - Default Speed Mode [(1)]

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
DS5	$t_{su(cmdV-clkH)}$	Setup time, mmc3_cmd valid before mmc3_clk rising clock edge	5.11		ns
DS6	$t_{h(clkH-cmdV)}$	Hold time, mmc3_cmd valid after mmc3_clk rising clock edge	20.46		ns
DS7	$t_{su(dV-clkH)}$	Setup time, mmc3_dat[i:0] valid before mmc3_clk rising clock edge	5.11		ns
DS8	$t_{h(clkH-dV)}$	Hold time, mmc3_dat[i:0] valid after mmc3_clk rising clock edge	20.46		ns

(1) i in [i:0] = 7

Table 7-113. Switching Characteristics for MMC3 - SD/SDIO Default Speed Mode [(2)]

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
DS0	fop(clk)	Operating frequency, mmc3_clk		24	MHz
DS1	$t_{w(clkH)}$	Pulse duration, mmc3_clk high	0.5*P-0.270 [(1)]		ns
DS2	$t_{w(clkL)}$	Pulse duration, mmc3_clk low	0.5*P-0.270 [(1)]		ns
DS3	$t_{d(clkL-cmdV)}$	Delay time, mmc3_clk falling clock edge to mmc3_cmd transition	-14.93	14.93	ns
DS4	$t_{d(clkL-dV)}$	Delay time, mmc3_clk falling clock edge to mmc3_dat[i:0] transition	-14.93	14.93	ns

(1) P = output mmc3_clk period in ns
(2) i in [i:0] = 7

Table 7-114. Timing Requirements for MMC4 - Default Speed Mode (1)

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
DS5	$t_{su(cmdV-clkH)}$	Setup time, mmc4_cmd valid before mmc4_clk rising clock edge	5.11		ns
DS6	$t_{h(clkH-cmdV)}$	Hold time, mmc4_cmd valid after mmc4_clk rising clock edge	20.46		ns
DS7	$t_{su(dV-clkH)}$	Setup time, mmc4_dat[i:0] valid before mmc4_clk rising clock edge	5.11		ns
DS8	$t_{h(clkH-dV)}$	Hold time, mmc4_dat[i:0] valid after mmc4_clk rising clock edge	20.46		ns

(1) i in [i:0] = 3

Table 7-115. Switching Characteristics for MMC4 - Default Speed Mode (2)

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
DS0	fop(clk)	Operating frequency, mmc4_clk		24	MHz
DS1	$t_{w(clkH)}$	Pulse duration, mmc4_clk high	0.5*P-0.270 (1)		ns
DS2	$t_{w(clkL)}$	Pulse duration, mmc4_clk low	0.5*P-0.270 (1)		ns
DS3	$t_{d(clkL-cmdV)}$	Delay time, mmc4_clk falling clock edge to mmc4_cmd transition	-14.93	14.93	ns
DS4	$t_{d(clkL-dV)}$	Delay time, mmc4_clk falling clock edge to mmc4_dat[i:0] transition	-14.93	14.93	ns

(1) P = output mmc4_clk period in ns
(2) i in [i:0] = 3

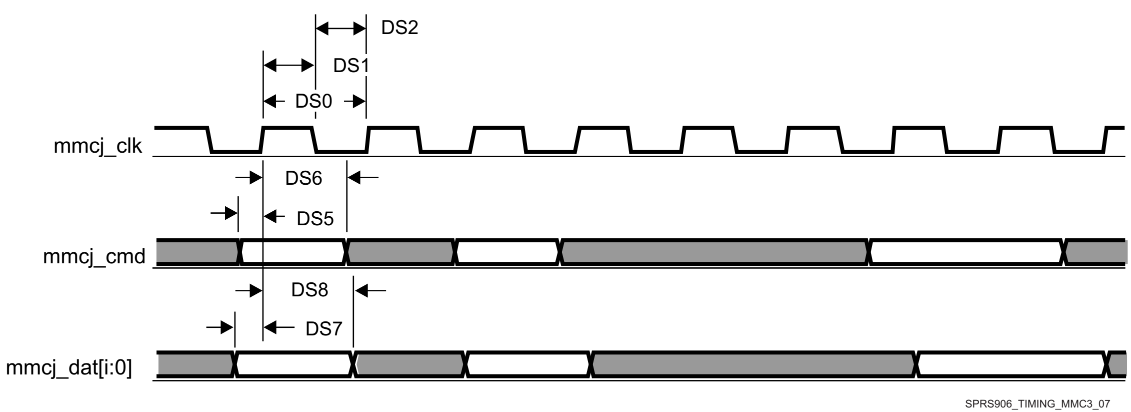


Figure 7-75. MMC/SD/SDIOj in - Default Speed - Receiver Mode

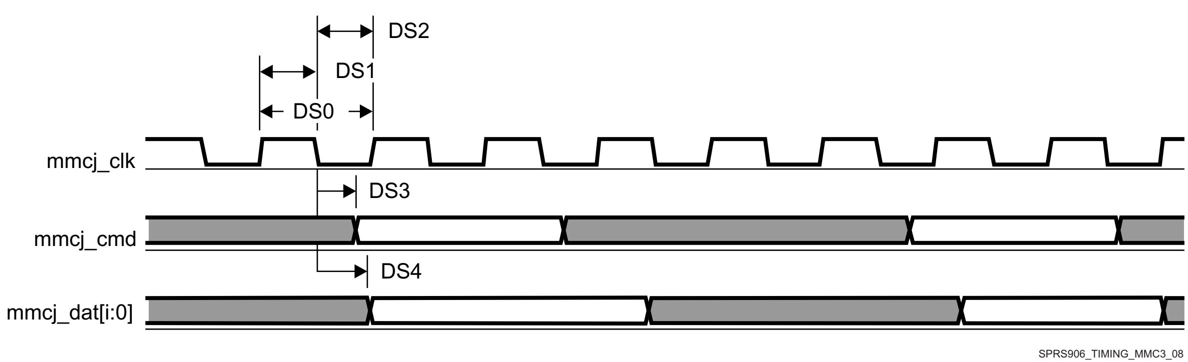


Figure 7-76. MMC/SD/SDIOj in - Default Speed - Transmitter Mode

7.23.3.2 MMC3 and MMC4, SD High Speed

Figure 7-77, Figure 7-78, and Table 7-116 through Table 7-119 present Timing requirements and Switching characteristics for MMC3 and MMC4 - SD and SDIO High speed in receiver and transmitter mode.

Table 7-116. Timing Requirements for MMC3 - SD/SDIO High Speed Mode (1)

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
HS3	$t_{su(cmdV-clkH)}$	Setup time, mmc3_cmd valid before mmc3_clk rising clock edge	5.3		ns
HS4	$t_{h(clkH-cmdV)}$	Hold time, mmc3_cmd valid after mmc3_clk rising clock edge	2.6		ns
HS7	$t_{su(dV-clkH)}$	Setup time, mmc3_dat[i:0] valid before mmc3_clk rising clock edge	5.3		ns
HS8	$t_{h(clkH-dV)}$	Hold time, mmc3_dat[i:0] valid after mmc3_clk rising clock edge	2.6		ns

(1) i in [i:0] = 7

Table 7-117. Switching Characteristics for MMC3 - SD/SDIO High Speed Mode (2)

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
HS1	fop(clk)	Operating frequency, mmc3_clk		48	MHz
HS2H	$t_{w(clkH)}$	Pulse duration, mmc3_clk high	0.5*P-0.270 (1)		ns
HS2L	$t_{w(clkL)}$	Pulse duration, mmc3_clk low	0.5*P-0.270 (1)		ns
HS5	$t_{d(clkL-cmdV)}$	Delay time, mmc3_clk falling clock edge to mmc3_cmd transition	-7.6	3.6	ns
HS6	$t_{d(clkL-dV)}$	Delay time, mmc3_clk falling clock edge to mmc3_dat[i:0] transition	-7.6	3.6	ns

(1) P = output mmc3_clk period in ns

(2) i in [i:0] = 7

Table 7-118. Timing Requirements for MMC4 - High Speed Mode (1)

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
HS3	$t_{su(cmdV-clkH)}$	Setup time, mmc4_cmd valid before mmc4_clk rising clock edge	5.3		ns
HS4	$t_{h(clkH-cmdV)}$	Hold time, mmc4_cmd valid after mmc4_clk rising clock edge	1.6		ns
HS7	$t_{su(dV-clkH)}$	Setup time, mmc4_dat[i:0] valid before mmc4_clk rising clock edge	5.3		ns
HS8	$t_{h(clkH-dV)}$	Hold time, mmc4_dat[i:0] valid after mmc4_clk rising clock edge	1.6		ns

(1) i in [i:0] = 3

Table 7-119. Switching Characteristics for MMC4 - High Speed Mode (2)

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
HS1	fop(clk)	Operating frequency, mmc4_clk		48	MHz
HS2H	$t_{w(clkH)}$	Pulse duration, mmc4_clk high	0.5*P-0.270 (1)		ns
HS2L	$t_{w(clkL)}$	Pulse duration, mmc4_clk low	0.5*P-0.270 (1)		ns
HS5	$t_{d(clkL-cmdV)}$	Delay time, mmc4_clk falling clock edge to mmc4_cmd transition	-8.8	6.6	ns
HS6	$t_{d(clkL-dV)}$	Delay time, mmc4_clk falling clock edge to mmc4_dat[i:0] transition	-8.8	6.6	ns

(1) P = output mmc4_clk period in ns
(2) i in [i:0] = 3

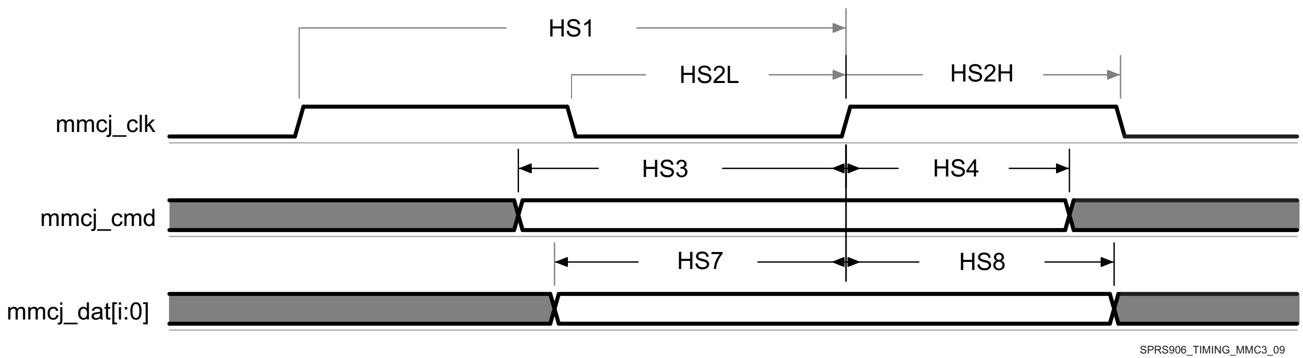


Figure 7-77. MMC/SD/SDIOj in - High Speed - Receiver Mode

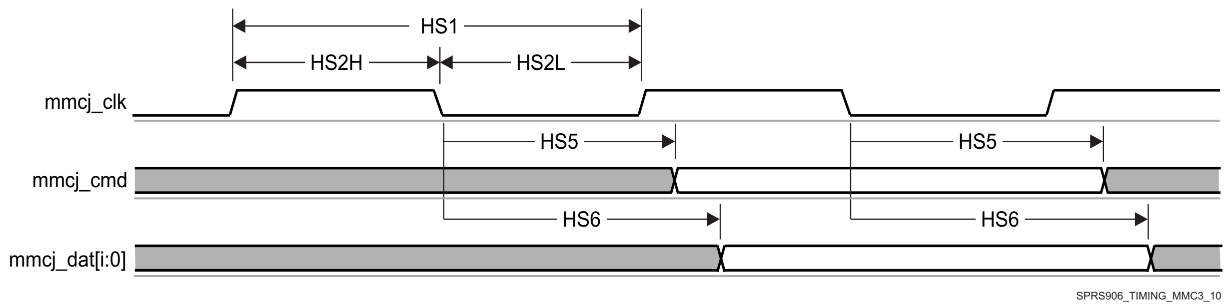


Figure 7-78. MMC/SD/SDIOj in - High Speed - Transmitter Mode

7.23.3.3 MMC3 and MMC4, SD and SDIO SDR12 Mode

Figure 7-79, Figure 7-80, and Table 7-120, through Table 7-123 present Timing requirements and Switching characteristics for MMC3 and MMC4 - SD and SDIO SDR12 in receiver and transmitter mode.

Table 7-120. Timing Requirements for MMC3 - SDR12 Mode (1)

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
SDR125	$t_{su(cmdV-clkH)}$	Setup time, mmc3_cmd valid before mmc3_clk rising clock edge	25.99		ns
SDR126	$t_{h(clkH-cmdV)}$	Hold time, mmc3_cmd valid after mmc3_clk rising clock edge	1.6		ns
SDR127	$t_{su(dV-clkH)}$	Setup time, mmc3_dat[i:0] valid before mmc3_clk rising clock edge	25.99		ns
SDR128	$t_{h(clkH-dV)}$	Hold time, mmc3_dat[i:0] valid after mmc3_clk rising clock edge	1.6		ns

(1) i in [i:0] = 7

Table 7-121. Switching Characteristics for MMC3 - SDR12 Mode (2)

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
SDR120	fop(clk)	Operating frequency, mmc3_clk		24	MHz
SDR121	$t_{w(clkH)}$	Pulse duration, mmc3_clk high	0.5*P-0.270 (1)		ns
SDR122	$t_{w(clkL)}$	Pulse duration, mmc3_clk low	0.5*P-0.270 (1)		ns
SDR123	$t_{d(clkL-cmdV)}$	Delay time, mmc3_clk falling clock edge to mmc3_cmd transition	-19.13	16.93	ns
SDR124	$t_{d(clkL-dV)}$	Delay time, mmc3_clk falling clock edge to mmc3_dat[i:0] transition	-19.13	16.93	ns

(1) P = output mmc3_clk period in ns

(2) i in [i:0] = 7

Table 7-122. Timing Requirements for MMC4 - SDR12 Mode [(1)]

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
SDR125	$t_{su(cmdV-clkH)}$	Setup time, mmc4_cmd valid before mmc4_clk rising clock edge	25.99		ns
SDR126	$t_{h(clkH-cmdV)}$	Hold time, mmc4_cmd valid after mmc4_clk rising clock edge	1.6		ns
SDR127	$t_{su(dV-clkH)}$	Setup time, mmc4_dat[i:0] valid before mmc4_clk rising clock edge	25.99		ns
SDR128	$t_{h(clkH-dV)}$	Hold time, mmc4_dat[i:0] valid after mmc4_clk rising clock edge	1.6		ns

(1) j in [i:0] = 3

Table 7-123. Switching Characteristics for MMC4 - SDR12 Mode [(2)]

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
SDR120	fop(clk)	Operating frequency, mmc4_clk		24	MHz
SDR121	$t_{w(clkH)}$	Pulse duration, mmc4_clk high	0.5*P-0.270 [(1)]		ns
SDR122	$t_{w(clkL)}$	Pulse duration, mmc4_clk low	0.5*P-0.270 [(1)]		ns
SDR125	$t_{d(clkL-cmdV)}$	Delay time, mmc4_clk falling clock edge to mmc4_cmd transition	-19.13	16.93	ns
SDR126	$t_{d(clkL-dV)}$	Delay time, mmc4_clk falling clock edge to mmc4_dat[i:0] transition	-19.13	16.93	ns

(1) P = output mmc4_clk period in ns

(2) j in [i:0] = 3

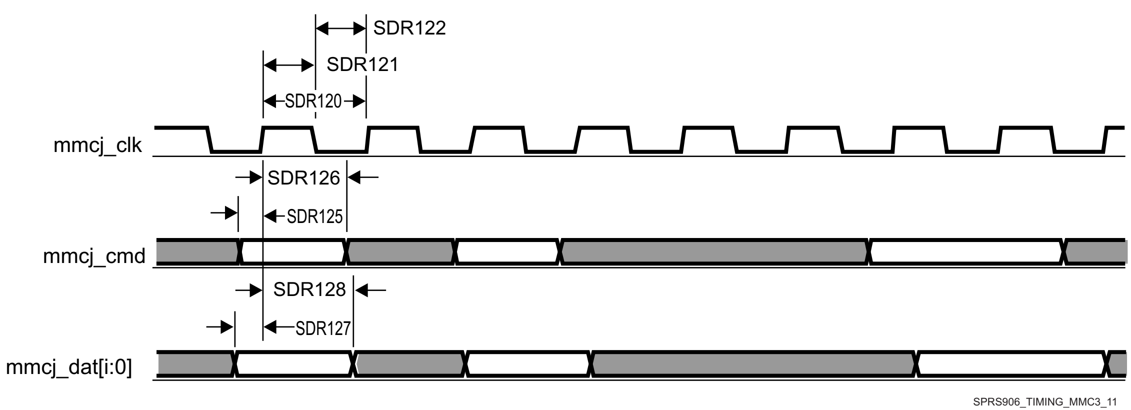


Figure 7-79. MMC/SD/SDIOj in - SDR12 - Receiver Mode

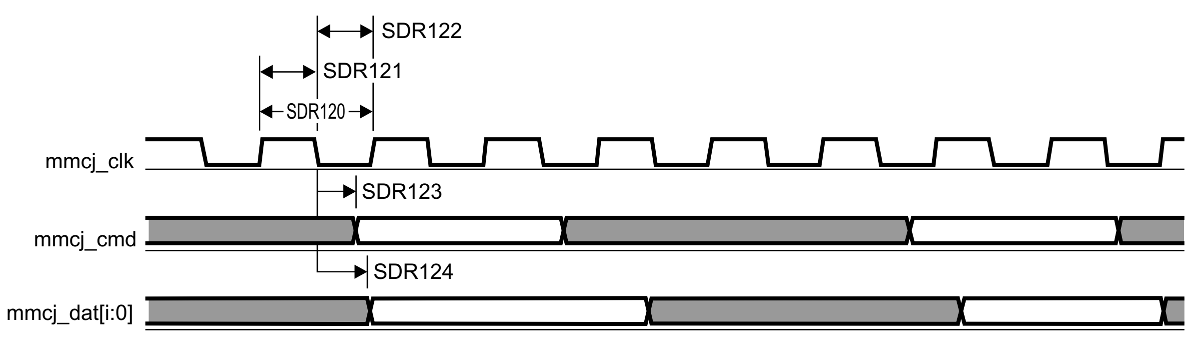


Figure 7-80. MMC/SD/SDIOj in - SDR12 - Transmitter Mode

7.23.3.4 MMC3 and MMC4, SD SDR25 Mode

Figure 7-81, Figure 7-82, and Table 7-124, through Table 7-127 present Timing requirements and Switching characteristics for MMC3 and MMC4 - SD and SDIO SDR25 in receiver and transmitter mode.

Table 7-124. Timing Requirements for MMC3 - SDR25 Mode (1)

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
SDR253	$t_{su(cmdV-clkH)}$	Setup time, mmc3_cmd valid before mmc3_clk rising clock edge	5.3		ns
SDR254	$t_{h(clkH-cmdV)}$	Hold time, mmc3_cmd valid after mmc3_clk rising clock edge	1.6		ns
SDR257	$t_{su(dV-clkH)}$	Setup time, mmc3_dat[i:0] valid before mmc3_clk rising clock edge	5.3		ns
SDR258	$t_{h(clkH-dV)}$	Hold time, mmc3_dat[i:0] valid after mmc3_clk rising clock edge	1.6		ns

(1) i in [i:0] = 7

Table 7-125. Switching Characteristics for MMC3 - SDR25 Mode (2)

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
SDR251	fop(clk)	Operating frequency, mmc3_clk		48	MHz
SDR252H	$t_{w(clkH)}$	Pulse duration, mmc3_clk high	0.5*P-0.270 (1)		ns
SDR252L	$t_{w(clkL)}$	Pulse duration, mmc3_clk low	0.5*P-0.270 (1)		ns
SDR255	$t_{d(clkL-cmdV)}$	Delay time, mmc3_clk falling clock edge to mmc3_cmd transition	-8.8	6.6	ns
SDR256	$t_{d(clkL-dV)}$	Delay time, mmc3_clk falling clock edge to mmc3_dat[i:0] transition	-8.8	6.6	ns

(1) P = output mmc3_clk period in ns

(2) i in [i:0] = 7

Table 7-126. Timing Requirements for MMC4 - SDR25 Mode (1)

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
SDR255	$t_{su(cmdV-clkH)}$	Setup time, mmc4_cmd valid before mmc4_clk rising clock edge	5.3		ns
SDR256	$t_{h(clkH-cmdV)}$	Hold time, mmc4_cmd valid after mmc4_clk rising clock edge	1.6		ns
SDR257	$t_{su(dV-clkH)}$	Setup time, mmc4_dat[i:0] valid before mmc4_clk rising clock edge	5.3		ns
SDR258	$t_{h(clkH-dV)}$	Hold time, mmc4_dat[i:0] valid after mmc4_clk rising clock edge	1.6		ns

(1) i in [i:0] = 3

Table 7-127. Switching Characteristics for MMC4 - SDR25 Mode (2)

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
SDR251	fop(clk)	Operating frequency, mmc4_clk		48	MHz
SDR252H	$t_{w(clkH)}$	Pulse duration, mmc4_clk high	0.5*P-0.270 (1)		ns
SDR252L	$t_{w(clkL)}$	Pulse duration, mmc4_clk low	0.5*P-0.270 (1)		ns
SDR255	$t_{d(clkL-cmdV)}$	Delay time, mmc4_clk falling clock edge to mmc4_cmd transition	-8.8	6.6	ns
SDR256	$t_{d(clkL-dV)}$	Delay time, mmc4_clk falling clock edge to mmc4_dat[i:0] transition	-8.8	6.6	ns

(1) P = output mmc4_clk period in ns
(2) i in [i:0] = 3

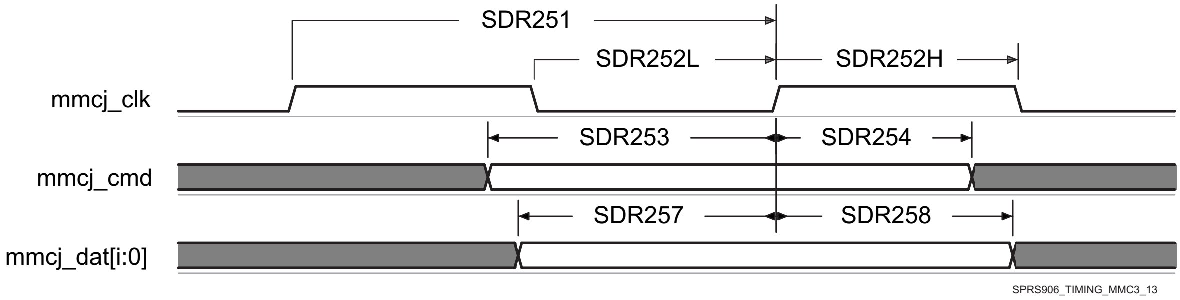


Figure 7-81. MMC/SD/SDIOj in - SDR25 - Receiver Mode

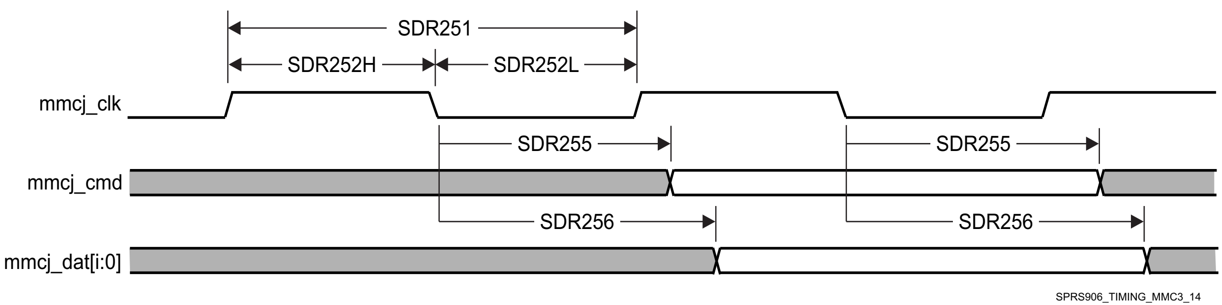


Figure 7-82. MMC/SD/SDIOj in - SDR25 - Transmitter Mode

7.23.3.5 MMC3 SDIO High Speed UHS-I SDR50 Mode, Half Cycle

Figure 7-83, Figure 7-84, Table 7-128, and Table 7-129 present Timing requirements and Switching characteristics for MMC3 - SDIO High speed SDR50 in receiver and transmitter mode.

Table 7-128. Timing Requirements for MMC3 - SDR50 Mode (1)

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
SDR503	$t_{su(cmdV-clkH)}$	Setup time, mmc3_cmd valid before mmc3_clk rising clock edge	1.48		ns
SDR504	$t_{h(clkH-cmdV)}$	Hold time, mmc3_cmd valid after mmc3_clk rising clock edge	1.6		ns
SDR507	$t_{su(dV-clkH)}$	Setup time, mmc3_dat[i:0] valid before mmc3_clk rising clock edge	1.48		ns
SDR508	$t_{h(clkH-dV)}$	Hold time, mmc3_dat[i:0] valid after mmc3_clk rising clock edge	1.6		ns

(1) i in [i:0] = 7

Table 7-129. Switching Characteristics for MMC3 - SDR50 Mode (2)

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
SDR501	fop(clk)	Operating frequency, mmc3_clk		96	MHz
SDR502H	$t_{w(clkH)}$	Pulse duration, mmc3_clk high	0.5*P-0.270 (1)		ns
SDR502L	$t_{w(clkL)}$	Pulse duration, mmc3_clk low	0.5*P-0.270 (1)		ns
SDR505	$t_{d(clkL-cmdV)}$	Delay time, mmc3_clk falling clock edge to mmc3_cmd transition	-3.66	1.46	ns
SDR506	$t_{d(clkL-dV)}$	Delay time, mmc3_clk falling clock edge to mmc3_dat[i:0] transition	-3.66	1.46	ns

(1) P = output mmc3_clk period in ns
(2) i in [i:0] = 7

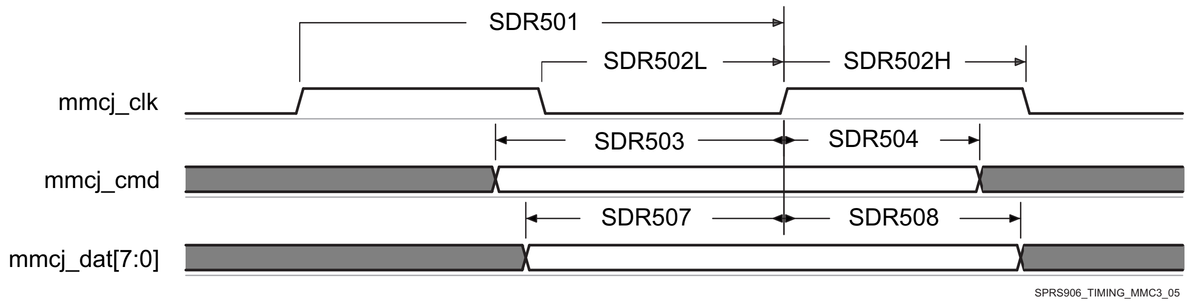


Figure 7-83. MMC/SD/SDIOj in - High Speed SDR50 - Receiver Mode

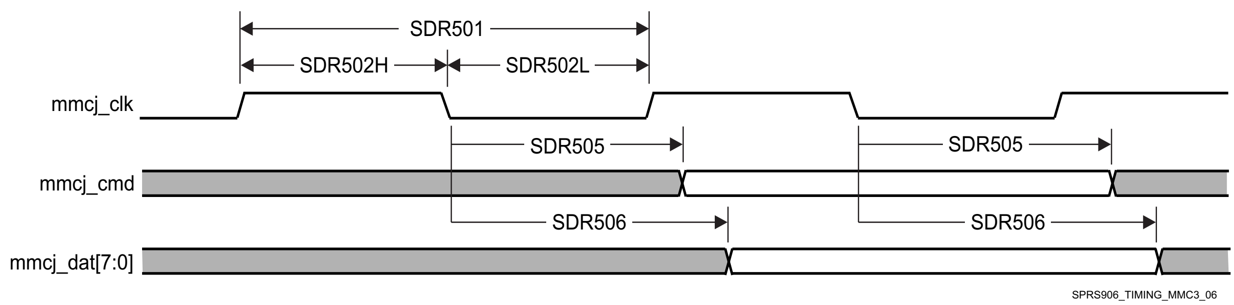


Figure 7-84. MMC/SD/SDIOj in - High Speed SDR50 - Transmitter Mode

NOTE

To configure the desired Manual IO Timing Mode the user must follow the steps described in section Manual IO Timing Modes of the Device TRM.

The associated registers to configure are listed in the **CFG REGISTER** column. For more information, see *Control Module* chapter in the device TRM.

Manual IO Timings Modes must be used to ensure some IO timings for MMC3. See Table 7-2 *Modes Summary* for a list of IO timings requiring the use of Manual IO Timings Modes. See Table 7-130 *Manual Functions Mapping for MMC3* for a definition of the Manual modes.

Table 7-130 lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.

Table 7-130. Manual Functions Mapping for MMC3

BALL	BALL NAME	MMC3_MANUAL1		CFG REGISTER	MUXMODE
		A_DELAY (ps)	G_DELAY (ps)		0
AD4	mmc3_clk	1085	21	CFG_MMC3_CLK_IN	mmc3_clk
AD4	mmc3_clk	1269	0	CFG_MMC3_CLK_OUT	mmc3_clk
AC4	mmc3_cmd	0	0	CFG_MMC3_CMD_IN	mmc3_cmd
AC4	mmc3_cmd	128	0	CFG_MMC3_CMD_OEN	mmc3_cmd
AC4	mmc3_cmd	98	0	CFG_MMC3_CMD_OUT	mmc3_cmd
AC7	mmc3_dat0	0	0	CFG_MMC3_DAT0_IN	mmc3_dat0
AC7	mmc3_dat0	362	0	CFG_MMC3_DAT0_OEN	mmc3_dat0
AC7	mmc3_dat0	0	0	CFG_MMC3_DAT0_OUT	mmc3_dat0
AC6	mmc3_dat1	7	0	CFG_MMC3_DAT1_IN	mmc3_dat1
AC6	mmc3_dat1	333	0	CFG_MMC3_DAT1_OEN	mmc3_dat1

Table 7-130. Manual Functions Mapping for MMC3 (continued)

BALL	BALL NAME	MMC3_MANUAL1		CFG REGISTER	MUXMODE
		A_DELAY (ps)	G_DELAY (ps)		0
AC6	mmc3_dat1	0	0	CFG_MMC3_DAT1_OUT	mmc3_dat1
AC9	mmc3_dat2	0	0	CFG_MMC3_DAT2_IN	mmc3_dat2
AC9	mmc3_dat2	402	0	CFG_MMC3_DAT2_OEN	mmc3_dat2
AC9	mmc3_dat2	0	0	CFG_MMC3_DAT2_OUT	mmc3_dat2
AC3	mmc3_dat3	203	0	CFG_MMC3_DAT3_IN	mmc3_dat3
AC3	mmc3_dat3	549	0	CFG_MMC3_DAT3_OEN	mmc3_dat3
AC3	mmc3_dat3	1	0	CFG_MMC3_DAT3_OUT	mmc3_dat3
AC8	mmc3_dat4	121	0	CFG_MMC3_DAT4_IN	mmc3_dat4
AC8	mmc3_dat4	440	0	CFG_MMC3_DAT4_OEN	mmc3_dat4
AC8	mmc3_dat4	206	0	CFG_MMC3_DAT4_OUT	mmc3_dat4
AD6	mmc3_dat5	336	0	CFG_MMC3_DAT5_IN	mmc3_dat5
AD6	mmc3_dat5	283	0	CFG_MMC3_DAT5_OEN	mmc3_dat5
AD6	mmc3_dat5	174	0	CFG_MMC3_DAT5_OUT	mmc3_dat5
AB8	mmc3_dat6	320	0	CFG_MMC3_DAT6_IN	mmc3_dat6
AB8	mmc3_dat6	443	0	CFG_MMC3_DAT6_OEN	mmc3_dat6
AB8	mmc3_dat6	0	0	CFG_MMC3_DAT6_OUT	mmc3_dat6
AB5	mmc3_dat7	2	0	CFG_MMC3_DAT7_IN	mmc3_dat7
AB5	mmc3_dat7	344	0	CFG_MMC3_DAT7_OEN	mmc3_dat7
AB5	mmc3_dat7	0	0	CFG_MMC3_DAT7_OUT	mmc3_dat7

NOTE

To configure the desired virtual mode the user must set MODESELECT bit and DELAYMODE bit field for each corresponding pad control register.

The pad control registers are presented in Table 4-3 and described in Device TRM, *Control Module Chapter*.

7.24 General-Purpose Interface (GPIO)

The general-purpose interface combines eight general-purpose input/output (GPIO) banks. Each GPIO module provides up to 32 dedicated general-purpose pins with input and output capabilities; thus, the general-purpose interface supports up to 215 pins.

These pins can be configured for the following applications:

- Data input (capture)/output (drive)
- Keyboard interface with a debounce cell
- Interrupt generation in active mode upon the detection of external events. Detected events are processed by two parallel independent interrupt-generation submodules to support biprocessor operations
- Wake-up request generation in idle mode upon the detection of external events

NOTE

For more information, see *General-Purpose Interface* chapter in the device TRM.

NOTE

The general-purpose input/output i (i = 1 to 8) bank is also referred to as GPIOi.

7.25 System and Miscellaneous interfaces

The Device includes the following System and Miscellaneous interfaces:

- Sysboot Interface
- System DMA Interface
- Interrupt Controllers (INTC) Interface
- Observability Signal (OBS) Interface

7.26 Test Interfaces

The Device includes the following Test interfaces:

- IEEE 1149.1 Standard-Test-Access Port (JTAG)
- Trace Port Interface Unit (TPIU)
- Advanced Event Triggering Interface (AET)

7.26.1 IEEE 1149.1 Standard-Test-Access Port (JTAG)

The JTAG (IEEE Standard 1149.1-1990 Standard-Test-Access Port and Boundary Scan Architecture) interface is used for BSDL testing and emulation of the device. The trstn pin only needs to be released when it is necessary to use a JTAG controller to debug the device or exercise the device's boundary scan functionality. For maximum reliability, the device includes an internal Pulldown (IPD) on the trstn pin to ensure that trstn is always asserted upon power up and the device's internal emulation logic is always properly initialized. JTAG controllers from Texas Instruments actively drive trstn high. However, some third-party JTAG controllers may not drive trstn high but expect the use of a Pullup resistor on trstn. When using this type of JTAG controller, assert trstn to initialize the device after powerup and externally drive trstn high before attempting any emulation or boundary-scan operations.

The main JTAG features include:

- 32KB embedded trace buffer (ETB)
- 5-pin system trace interface for debug
- Supports Advanced Event Triggering (AET)
- All processors can be emulated via JTAG ports
- All functions on EMU pins of the device:
  - EMU[1:0] - cross-triggering, boot mode (WIR), STM trace
  - EMU[4:2] - STM trace only (single direction)

7.26.1.1 JTAG Electrical Data/Timing

Table 7-131, Table 7-132 and Figure 7-85 assume testing over the recommended operating conditions and electrical characteristic conditions below.

Table 7-131. Timing Requirements for IEEE 1149.1 JTAG

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
1	$t_{c(TCK)}$	Cycle time, TCK	62.29		ns
1a	$t_{w(TCKH)}$	Pulse duration, TCK high (40% of t_c)	24.92		ns
1b	$t_{w(TCKL)}$	Pulse duration, TCK low (40% of t_c)	24.92		ns
3	$t_{su(TDI-TCK)}$	Input setup time, TDI valid to TCK high	6.23		ns
	$t_{su(TMS-TCK)}$	Input setup time, TMS valid to TCK high	6.23		ns
4	$t_{h(TCK-TDI)}$	Input hold time, TDI valid from TCK high	31.15		ns
	$t_{h(TCK-TMS)}$	Input hold time, TMS valid from TCK high	31.15		ns

Table 7-132. Switching Characteristics Over Recommended Operating Conditions for IEEE 1149.1 JTAG

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
2	$t_{d(TCKL-TDOV)}$	Delay time, TCK low to TDO valid	0	30.5	ns

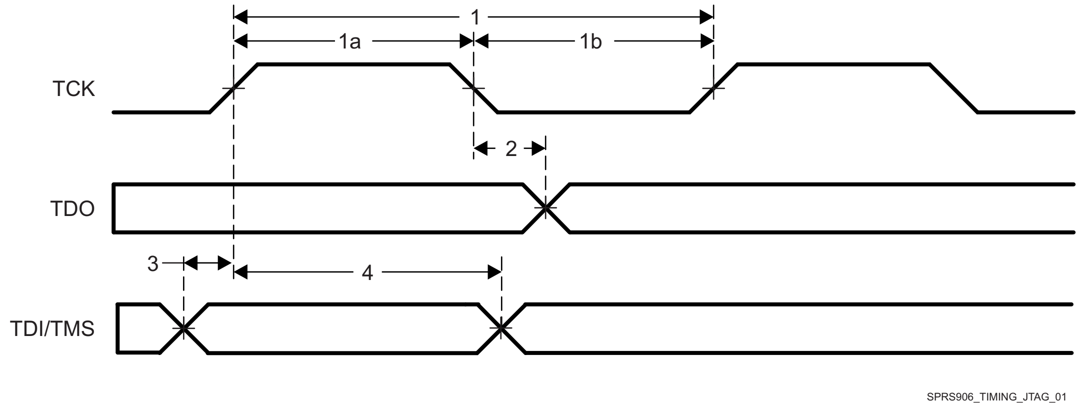


Figure 7-85. JTAG Timing

Table 7-133, Table 7-134 and Figure 7-86 assume testing over the recommended operating conditions and electrical characteristic conditions below.

Table 7-133. Timing Requirements for IEEE 1149.1 JTAG With RTCK

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
1	$t_{c(TCK)}$	Cycle time, TCK	62.29		ns
1a	$t_{w(TCKH)}$	Pulse duration, TCK high (40% of t_c)	24.92		ns
1b	$t_{w(TCKL)}$	Pulse duration, TCK low (40% of t_c)	24.92		ns
3	$t_{su(TDI-TCK)}$	Input setup time, TDI valid to TCK high	6.23		ns
	$t_{su(TMS-TCK)}$	Input setup time, TMS valid to TCK high	6.23		ns
4	$t_{h(TCK-TDI)}$	Input hold time, TDI valid from TCK high	31.15		ns
	$t_{h(TCK-TMS)}$	Input hold time, TMS valid from TCK high	31.15		ns

Table 7-134. Switching Characteristics Over Recommended Operating Conditions for IEEE 1149.1 JTAG With RTCK

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
5	$t_{d(TCK-RTCK)}$	Delay time, TCK to RTCK with no selected subpaths (that is, ICEPick is the only tap selected - when the Arm is in the scan chain, the delay time is a function of the Arm functional clock).	0	27	ns
6	$t_{c(RTCK)}$	Cycle time, RTCK	62.29		ns
7	$t_{w(RTCKH)}$	Pulse duration, RTCK high (40% of t_c)	24.92		ns
8	$t_{w(RTCKL)}$	Pulse duration, RTCK low (40% of t_c)	24.92		ns

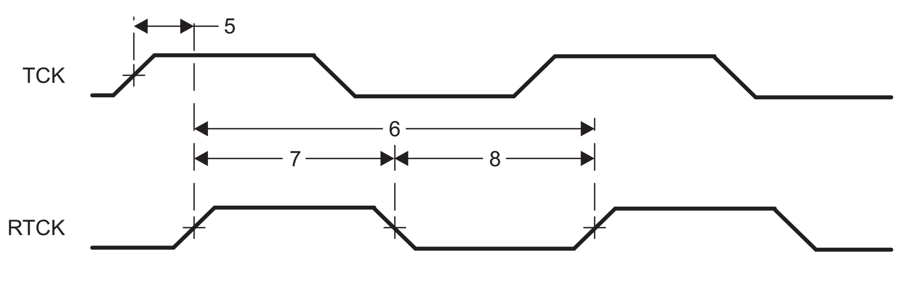


Figure 7-86. JTAG With RTCK Timing

7.26.2 Trace Port Interface Unit (TPIU)

CAUTION

The I/O timings provided in this section are valid only if signals within a single IOSET are used. The IOSETs are defined in Table 7-136.

7.26.2.1 TPIU PLL DDR Mode

Table 7-135 and Figure 7-87 assume testing over the recommended operating conditions and electrical characteristic conditions below.

Table 7-135. Switching Characteristics for TPIU

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
TPIU1	$t_{c(clk)}$	Cycle time, TRACECLK period	5.56		ns
TPIU4	$t_{d(clk-ctlV)}$	Skew time, TRACECLK transition to TRACECTL transition	-1.61	1.98	ns
TPIU5	$t_{d(clk-dataV)}$	Skew time, TRACECLK transition to TRACEDATA[17:0]	-1.61	1.98	ns

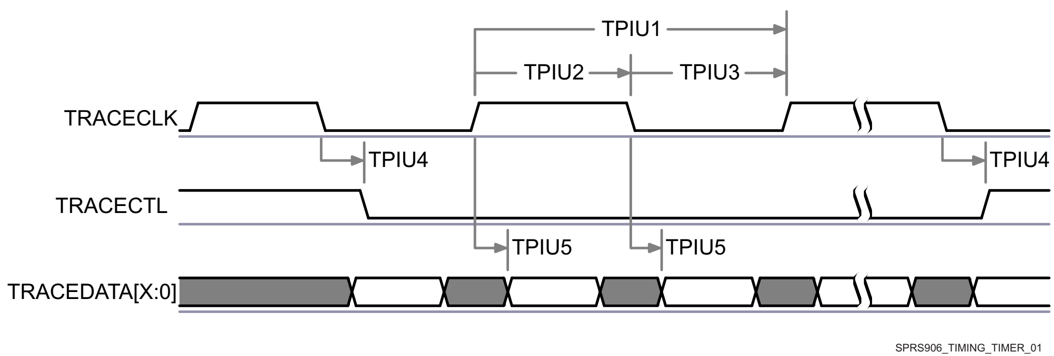


Figure 7-87. TPIU-PLL DDR Transmit Mode(1)

(1) In d[X:0], X is equal to 15 or 17.

In Table 7-136 are presented the specific groupings of signals (IOSET) for use with TPIU signals.

Table 7-136. TPIU IOSETs

SIGNALS	IOSET1		IOSET2	
	BALL	MUX	BALL	MUX
emu19	E6	5	A10	2
emu18	F5	5	B9	2
emu17	E4	5	A9	2
emu16	C1	5	C9	2
emu15	F4	5	A8	2
emu14	D2	5	C7	2
emu13	E2	5	C8	2
emu12	D1	5	C6	2
emu11	F3	5	A5	2
emu10	F2	5	D8	2
emu9	G6	5	E7	2
emu8	G1	5	F8	2
emu7	H7	5	F9	2
emu6	G2	5	E9	2

Table 7-136. TPIU IOSETs (continued)

SIGNALS	IOSET1		IOSET2	
	BALL	MUX	BALL	MUX
emu5	E1	5	G11	2
emu4	A7	2	A7	2
emu3	D7	2	D7	2
emu2	F10	2	F10	2
emu1	D24	0	D24	0
emu0	G21	0	G21	0

8 Applications, Implementation, and Layout

NOTE

Information in the following Applications section is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Introduction

This chapter is intended to communicate, guide and illustrate a PCB design strategy resulting in a PCB that can support TI's latest Application Processor. This Processor is a high-performance processor designed for automotive Infotainment based on enhanced OMAP™ architecture integrated on a 28-nm CMOS process technology.

These guidelines first focus on designing a robust Power Delivery Network (PDN) which is essential to achieve the desirable high performance processing available on Device. The general principles and step-by-step approach for implementing good power integrity (PI) with specific requirements will be described for the key Device power domains.

TI strongly believes that simulating a PCB's proposed PDN is required for first pass PCB design success. Key Device processor high-current power domains need to be evaluated for Power Rail IR Drop, Decoupling Capacitor Loop-Inductance and Power Rail Target Impedance. Only then can a PCB's PDN performance be truly accessed by comparing these model PI parameters vs. TI's recommended values. Ultimately for any high-volume product, TI recommends conducting a "Processor PDN Validation" test on prototype PCBs across processor "split lots" to verify PDN robustness meets desired performance goals for each customer's worst-case scenario. Please contact your TI representative to receive guidance on PDN PI modeling and validation testing.

Likewise, the methodology and requirements needed to route Device high speed, differential interfaces (that is, USB2.0, USB3.0, HDMI, PCIe, SATA), single-ended interfaces (that is, DDR3, QSPI) and general purpose interfaces using LVCMOS drivers that meet timing requirements while minimizing signal integrity (SI) distortions on the PCB's signaling traces. Signal trace lengths and flight times are aligned with FR-4 standard specification for PCBs.

Several different PCB layout stack-up examples have been presented to illustrate a typical number of layers, signal assignments and controlled impedance requirements. Different Device interface signals demand more or less complexity for routing and controlled impedance stack-ups. Optimizing the PCB's PDN stack-up needs with all of these different types of signal interfaces will ultimately determine the final layer count and layer assignments in each customer's PCB design.

This guideline must be used as a supplement in complement to TI's Application Processor, Power Management IC (PMIC) and Audio Companion components along with other TI component technical documentation (that is, Technical Reference Manual, Data Manual, Data Sheets, Silicon Errata, Pin-Out Spreadsheet, Application Notes, etc.).

NOTE

Notwithstanding any provision to the contrary, TI makes no warranty expressed, implied, or statutory, including any implied warranty of merchantability of fitness for a specific purpose, for customer boards. The data described in this appendix are intended as guidelines only.

NOTE

These PCB guidelines are in a draft maturity and consequently, are subject to change depending on design verification testing conducted during IC development and validation.

8.1.1 Initial Requirements and Guidelines

Unless otherwise specified, the characteristic impedance for single-ended interfaces is recommended to be between 35 Ω and 65 Ω to minimize the overshoot or undershoot on far-end loads.

Characteristic impedance for differential interfaces must be routed as differential traces on the same layer. The trace width and spacing must be chosen to yield the recommended differential impedance. For more information see Section 8.5.1.

The PDN must be optimized for low trace resistance and low trace inductance for all high-current power nets from PMIC to the device.

An external interface using a connector must be protected following the IEC61000-4-2 level 4 system ESD.

8.2 Power Optimizations

This section describes the necessary steps for designing a robust Power Distribution Network (PDN):

- **Section 8.2.1, Step 1:** PCB Stack-up
- **Section 8.2.2, Step 2:** Physical Placement
- **Section 8.2.3, Step 3:** Static Analysis
- **Section 8.2.4, Step 4:** Frequency Analysis

8.2.1 Step 1: PCB Stack-up

The PCB stack-up (layer assignment) is an important factor in determining the optimal performance of the power distribution system. An optimized PCB stack-up for higher power integrity performance can be achieved by following these recommendations:

- Power and ground plane pairs must be closely coupled together. The capacitance formed between the planes can decouple the power supply at high frequencies. Whenever possible, the power and ground planes must be solid to provide continuous return path for return current.
- Use a thin dielectric between the power and ground plane pair. Capacitance is inversely proportional to the separation of the plane pair. Minimizing the separation distance (the dielectric thickness) maximizes the capacitance.
- Optimize the power and ground plane pair carrying high current supplies to key component power domains as close as possible to the same surface where these components are placed (see Figure 8-1). This will help to minimize "loop inductance" encountered between supply decoupling capacitors and component supply inputs and between power and ground plane pairs.

NOTE

1-2oz Cu weight for power / ground plane is preferred to enable better PCB heat spreading, helping to reduce Processor junction temperatures. In addition, it is preferable to have the power / ground planes be adjacent to the PCB surface on which the Processor is mounted.

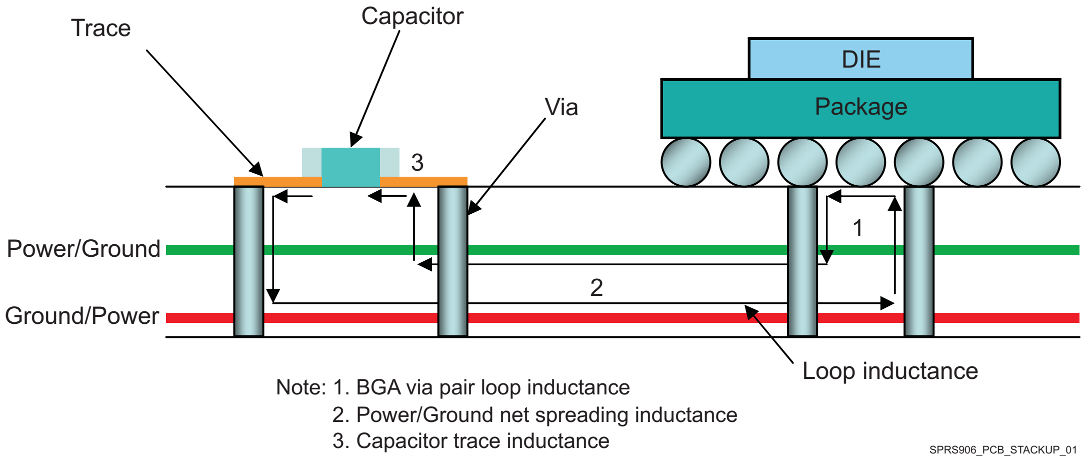


Figure 8-1. Minimize Loop Inductance With Proper Layer Assignment

The placement of power and ground planes in the PCB stackup (determined by layer assignment) has a significant impact on the parasitic inductances of power current path as shown in Figure 8-1. For this reason, it is recommended to consider layer order in the early stages of the PCB PDN design cycle, putting high-priority supplies in the top half of the stackup (assuming high load and priority components are mounted on the top-side of PCB) and low-priority supplies in the bottom half of the stackup as shown in the examples below (vias have parasitic inductances which impact the bottom layers more, so it is advised to put the sensitive and high-priority power supplies on the top/same layers).

8.2.2 Step 2: Physical Placement

A critical step in designing an optimized PDN is that proper care must be taken to making sure that the initial floor planning of the PCB layout is done with good power integrity design guidelines in mind. The following points are important for optimizing a PCB's PDN:

- Minimizing the physical distance between power sources and key high load components is the first step toward optimization. Placing source and load components on the same side of the PCB is desirable. This will minimize via inductance impact for high current loads and steps
- External trace routing between components must be as wide as possible. The wider the traces, the lower the DC resistance and consequently the lower the static IR drop.
- Whenever possible for the internal layers (routing and plane), wide traces and copper area fills are preferred for PDN layout. The routing of power nets in plane provide for more interplane capacitance and improved high frequency performance of the PDN.
- Whenever possible, use a via to component pin/pad ratio of 1:1 or better (that is, especially decoupling capacitors, power inductors and current sensing resistors). Do not share vias among multiple capacitors for connecting power supply and ground planes.
- Placement of vias must be as close as possible or even within a component's solder pad if the PCB technology you are using provides this capability.
- To avoid any "ampacity" issue – maximum current-carrying capacity of each transitional via should be evaluated to determine the appropriate number of vias required to connect components.

  Adding vias to bring the "via-to-pad" ratio to 1:1 will improve PDN performance.
- For noise sensitive power supplies (that is, Phase Lock-Loops, analog signals like audio and video), a Gnd shield can be used to isolate coplanar supplies that may have high step currents or high frequency switching transitions from coupling into low-noise supplies.

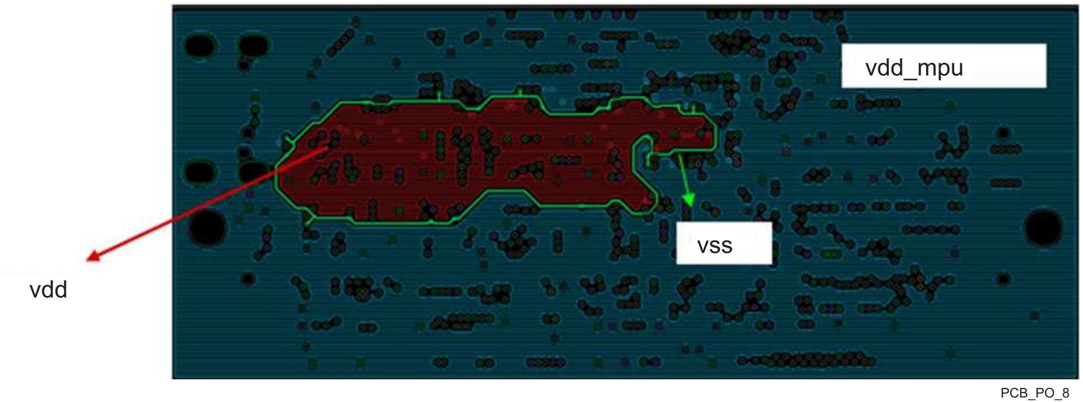


Figure 8-2. Coplanar Shielding of Power Net Using Ground Guard-band

8.2.3 Step 3: Static Analysis

Delivering reliable power to circuits is always of critical importance because voltage drops (also known as IR drops) can happen at every level within an electronic system, on-chip, within a package, and across the board. Robust system performance can only be ensured by understanding how the system elements will perform under typical stressful Use Cases. Therefore, it is a good practice to perform a Static or DC Analysis.

Static or DC analysis and design methodology results in a PDN design that minimizes voltage or IR drops across power and ground planes, traces and vias. This ensures the application processor's internal transistors will be operating within their specified voltage ranges for proper functionality. The amount of IR drop that will be encounter is based upon amount power drawn for a desired Use Case and PCB trace (widths, geometry and number of parallel traces) and via (size, type and number) characteristics.

Components that are distant from their power source are particularly susceptible to IR drop. Designs that rely on battery power must minimize voltage drops to avoid unacceptable power loss that can negatively impact system performance. Early assessments a PDN's static (DC) performance helps to determine basic power distribution parameters such as best system input power point, optimal PCB layer stackup, and copper area needed for load currents.

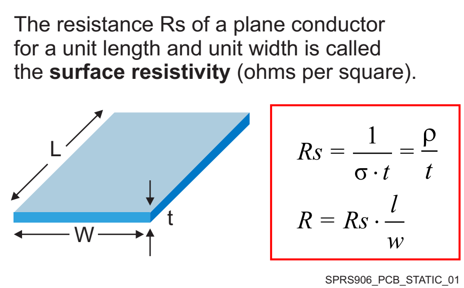


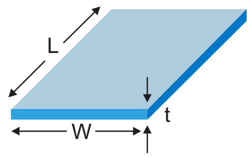
Figure 8-3. Depiction of Sheet Resistivity and Resistance

Ohm's Law (V = I × R) relates conduction current to voltage drop. At DC, the relation coefficient is a constant and represents the resistance of the conductor. Even current carrying conductors will dissipate power at high currents even though their resistance may be very small. Both voltage drop and power dissipation are proportional to the resistance of the conductor.

Figure 8-4 shows a PCB-level static IR drop budget defined between the power management device (PMIC) pins and the application processor's balls when the PMIC is supplying power.

- It is highly recommended to physically place the PMIC as close as possible to the processor and on the same side. The orientation of the PMIC vs. processor should be aligned to minimize distance for the highest current rail.

The resistance Rs of a plane conductor for a unit length and unit width is called the **surface resistivity** (ohms per square).



$$Rs = \frac{1}{\sigma \cdot t} = \frac{\rho}{t}$$

$$R = Rs \cdot \frac{l}{w}$$

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Figure 8-4. Static IR Drop Budget for PCB Only

The system-level IR drop budget is made up of three portions: on-chip, package, and PCB board. Static IR or DC analysis/design methodology consists of designing the PDN such that the voltage drop (under DC operating conditions) across power and ground pads of the transistors of the application processor device is within a specified value of the nominal voltage for proper functionality of the device.

A PCB system-level voltage drop budget for proper device functionality is typically 1.5% of nominal voltage. For a 1.35-V supply, this would be ≤20 mV.

To accurately analyze PCB static IR drop, the actual geometry of the PDN must be modeled properly and simulated to accurately characterize long distribution paths, copper weight impacts, electro-migration violations of current-carrying vias, and “Swiss-cheese” effects via placement has on power rails. It is recommended to perform the following analyses:

- Lumped resistance/IR drop analysis
- Distributed resistance/IR drop analysis

NOTE

The PMIC companion device supporting this processor has been designed with voltage sensing feedback loop capabilities that enable a remote sense of the SMPS output voltage at the point of use.

The NOTE above means the SMPS feedback signals and returns must be routed across PCB and connected to the Device input power ball for which a particular SMPS is supplying power. This feedback loop provides compensation for some of the voltage drop encountered across the PDN within limits. As such, the effective resistance of the PDN within this loop should be determined in order to optimize voltage compensation loop performance. The resistance of two PDN segments are of interest: one from the power inductor/bulk power filtering capacitor node to the Processor’s input power and second is the entire PDN route from SMPS output pin/ball to the Processor input power.

In the following sections each methodology is described in detail and an example has been provided of analysis flow that can be used by the PCB designer to validate compliance to the requirements on their PCB PDN design.

8.2.3.1 PDN Resistance and IR Drop

Lumped methodology consists of grouping all of the power pins on both the PMIC (voltage source) and processor (current sink) devices. Then the PMIC source is set to an expected Use Case voltage level and the processor load has its Use Case current sink value set as well. Now the lumped/effective resistance for the power rail trace/plane routes can be determine based upon the actual layout’s power rail etch wide, shape, length, via count and placement Figure 8-5 illustrates the pin-grouping/lumped concept.

The lumped methodology consists of importing the PCB layout database (from Cadence Allegro tool or any other layout design tool) into the static IR drop modeling and simulation tool of preference for the PCB designer. This is followed by applying the correct PCB stack-up information (thickness, material properties) of the PCB dielectric and metallization layers. The material properties of dielectric consist of permittivity (Dk) and loss tangent (Df).

For the conductor layers, the correct conductivity needs to be programmed into the simulation tool. This is followed by pin-grouping of the power and ground nets, and applying appropriate voltage/current sources. The current and voltage information can be obtained from the power and voltage specifications of the device under different operating conditions / Use Cases.

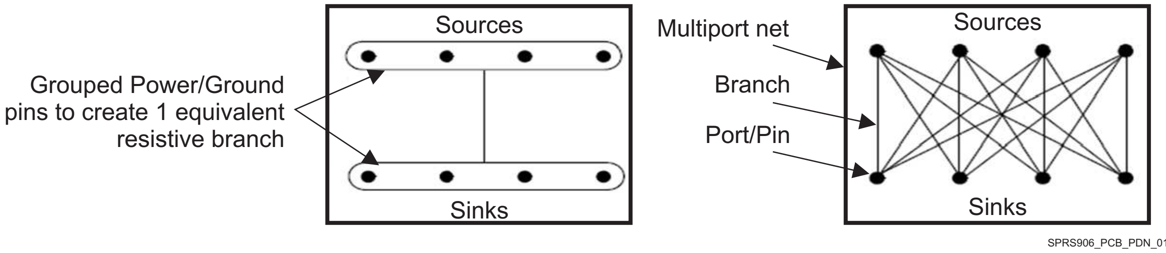

Figure 8-5. Pin-grouping concept: Lumped and Distributed Methodologies

8.2.4 Step 4: Frequency Analysis

Delivering low noise voltage sources are very important to allowing a system to operate at the lowest possible Operational Performance Point (OPP) for any one Use Case. An OPP is a combination of the supply voltage level and clocking rate for key internal processor domains. A SCH and PCB designed to provide low noise voltage supplies will then enable the processor to enter optimal OPPs for each Use Case that in turn will minimize power dissipation and junction temperatures on-die. Therefore, it is a good engineering practice to perform a Frequency Analysis over the key power domains.

Frequency analysis and design methodology results in a PDN design that minimizes transient noise voltages at the processor's input power balls. This allows the processor's internal transistors to operate near the minimum specified operating supply voltage levels. To accomplish this one must evaluate how a voltage supply will change due to impedance variations over frequency. This analysis will focus on the decoupling capacitor network (VDD_xxx and VSS/Gnd rails) at the load. Sufficient capacitance with a distribution of self-resonant points will provide for an overall lower impedance vs frequency response for each power domain.

Decoupling components that are distant from their load's input power are susceptible to encountering spreading loop inductance from the PCB design. Early analysis of each key power domain's frequency response helps to determine basic decoupling capacitor placement, optimal footprint, layer assignment, and types needed for minimizing supply voltage noise/fluctuations due to switching and load current transients.

NOTE

Evaluation of loop inductance values for decoupling capacitors placed ~300mils closer to the load's input power balls has shown an 18% reduction in loop inductance due to reduced distance.

- Decoupling capacitors must be carefully placed in order to minimize loop inductance impact on supply voltage transients. A real capacitor has characteristics not only of capacitance but also inductance and resistance.

  Figure 8-6 shows the parasitic model of a real capacitor. A real capacitor must be treated as an RLC circuit with effective series resistance (ESR) and effective series inductance (ESL).

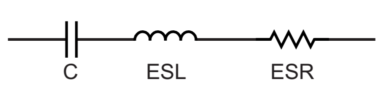

Figure 8-6. Characteristics of a Real Capacitor With ESL and ESR

The magnitude of the impedance of this series model is given as:

$$|Z| = \sqrt{ESR^2 + \left(\omega ESL - \frac{1}{\omega C}\right)^2}$$

$$\text{where: } \omega = 2\pi f$$

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Figure 8-7. Series Model Impedance Equation

Figure 8-8 shows the resonant frequency response of a typical capacitor with a self-resonant frequency of 55 MHz. The impedance of the capacitor is a combination of its series resistance and reactive capacitance and inductance as shown in the equation above.

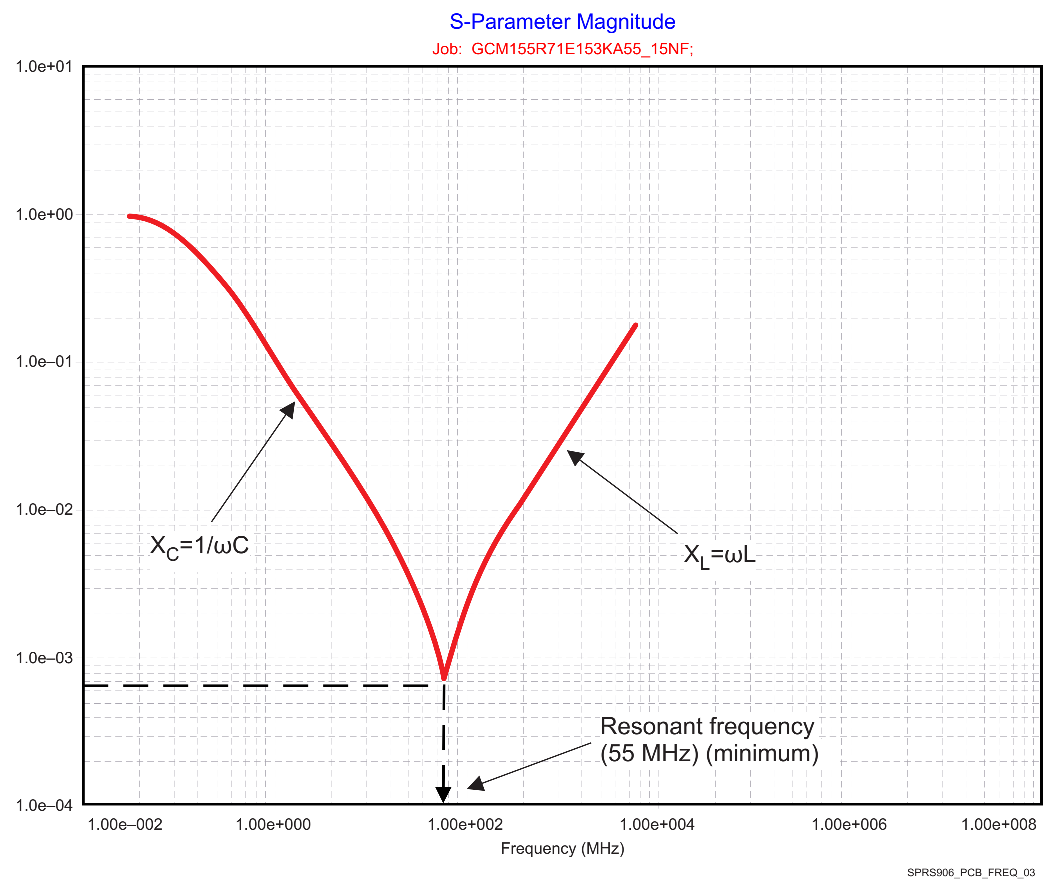

Figure 8-8. Typical Impedance Profile of a Capacitor

Because a capacitor has series inductance and resistance that impacts its effectiveness, it is important that the following recommendations are adopted in placing capacitors on the PDN.

Wherever possible, mount the capacitor with the geometry that minimizes the mounting inductance and resistance. This was shown earlier in Figure 8-1. The capacitor mounting inductance and resistance values include the inductance and resistance of the pads, trace, and vias. Whenever possible, use footprints that have the lowest inductance configuration as shown in Figure 8-9

The length of a trace used to connect a capacitor has a big impact on parasitic inductance and resistance of the mounting. This trace must be as short and as wide as possible. wherever possible, minimize distance to supply and Gnd vias by locating vias nearby or within the capacitor's solder pad landing. Further improvements can be made to the mounting by placing vias to the side of capacitor lands or doubling the number of vias as shown in Figure 8-9. If the PCB manufacturing processes allow it and if cost-effective, via-in-pad (VIP) geometries are strongly recommended.

In addition to mounting inductance and resistance associated with placing a capacitor on the PCB, the effectiveness of a decoupling capacitor also depends on the spreading inductance and resistance that the capacitor sees with respect to the load. The spreading inductance and resistance is strongly dependent on the layer assignment in the PCB stack-up. Therefore, try to minimize X, Y and Z dimensions where the Z is due to PCB thickness (as shown in Figure 8-9).

From left (highest inductance) to right (lowest inductance) the capacitor footprint types shown in Figure 8-9 are known as:

- 2-via, Skinny End Exit (2vSEE)
- 2-via, Wide End Exit (2vWEE)
- 2-via, Wide Side Exit (2vWSE)
- 4-via, Wide Side Exit (4vWSE)
- 2-via, In-Pad (2vIP)

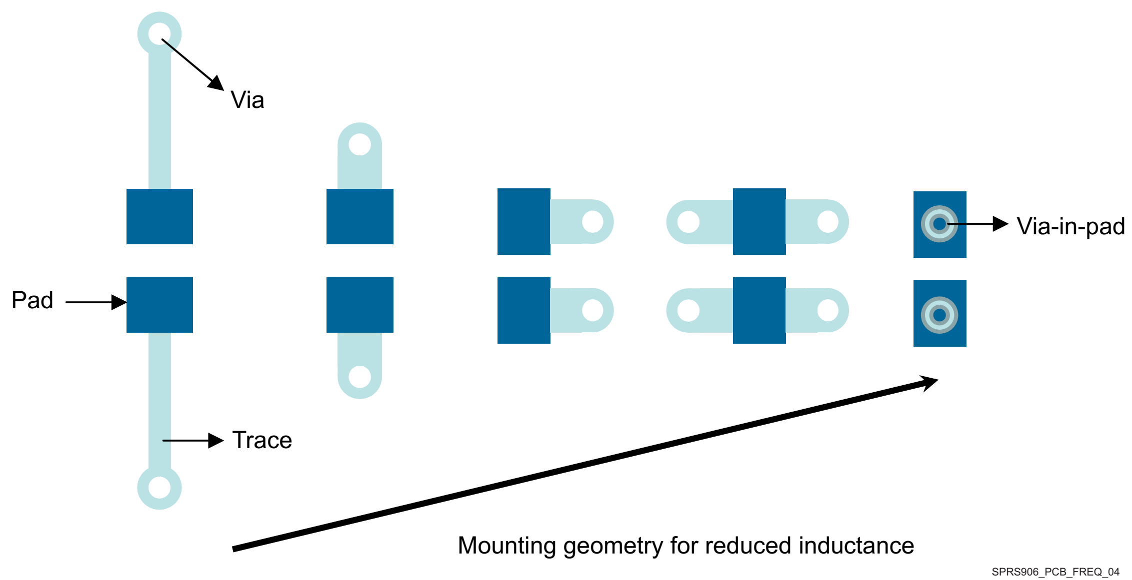

Figure 8-9. Capacitor Placement Geometry for Improved Mounting Inductance

NOTE

Evaluation of loop inductance values for decoupling capacitor footprints 2vSEE (worst case) vs 4vWSE (2nd best) has shown a 30% reduction in inductance when 4vWSE footprint was used in place of 2vSEE.

Decoupling Capacitor (Dcap) Strategy:

1. Use lowest inductance footprint and trace connection scheme possible for given PCB technology and layout area in order to minimize Dcap loop inductance to power pin as much as possible (see Figure 8-9).
2. Place Dcaps on “same-side” as component within their power plane outline to minimize “decoupling loop inductance”. Target distance to power pin should be less than ~500mils depending upon PCB layout characteristics (plane's layer assignment and solid nature). Use PI modeling CAD tool to verify minimum inductance for top vs bottom-side placement.
3. Place Dcaps on “opposite-side” as component within their power plane outline if “same-side” is not feasible or if distance to power pin is greater than ~500mils for top-side location. Use PI modeling CAD tool to verify minimum inductance for top vs bottom-side placement.
4. Use minimum 10mil trace width for all voltage and gnd planes connections (that is, Dcap pads, component power pins, etc.).

5. Place all voltage and gnd plane vias "as close as possible" to point of use (that is, Dcap pads, component power pins, etc.).
6. Use a "Power/Gnd pad/pin to via" ratio of 1:1 whenever possible. Do not exceed 2:1 ratio for small number of vias within restricted PCB areas (that is, underneath BGA components).

Frequency analysis for the CORE power domain has yielded the vdd Impedance vs Frequency response shown in Section 8.3.8.2, vdd Example Analysis. As the example shows the overall CORE PDN R_{eff} meets the maximum recommended PDN resistance of 10mΩ.

8.2.5 System ESD Generic Guidelines

8.2.5.1 System ESD Generic PCB Guideline

Protection devices must be placed close to the ESD source which means close to the connector. This allows the device to subtract the energy associated with an ESD strike before it reaches the internal circuitry of the application board.

To help minimize the residual voltage pulse that will be built-up at the protection device due to its nonzero turn-on impedance, it is mandatory to route the ESD device with minimum stub length so that the low-resistive, low-inductive path from the signal to the ground is granted and not increasing the impedance between signal and ground.

For ESD protection array being railed to a power supply when no decoupling capacitor is available in close vicinity, consider using a decoupling capacitor (≥ 0.1 µF) tight to the VCC pin of the ESD protection. A positive strike will be partially diverted to this capacitance resulting in a lower residual voltage pulse.

Ensure that there is sufficient metallization for the supply of signals at the interconnect side (VCC and GND in Figure 8-10) from connector to external protection because the interconnect may see between 15-A to 30-A current in a short period of time during the ESD event.

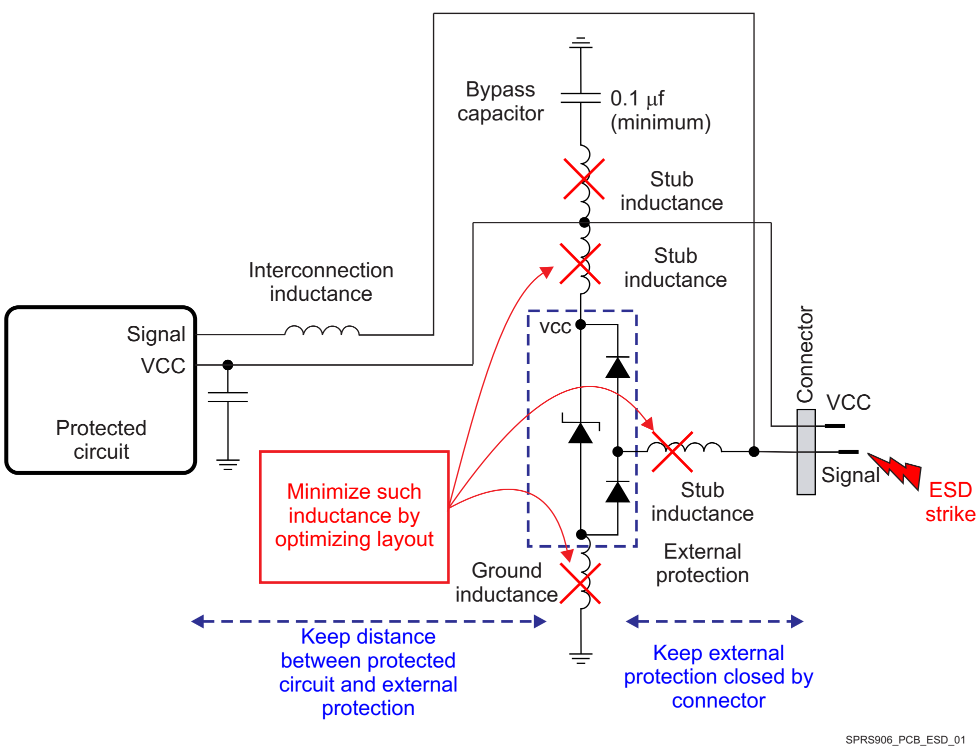

Figure 8-10. Placement Recommendation for an ESD External Protection

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NOTE

To ensure normal behavior of the ESD protection (unwanted leakage), it is better to ground the ESD protection to the board ground rather than any local ground (example isolated shield or audio ground).

8.2.5.2 Miscellaneous EMC Guidelines to Mitigate ESD Immunity

- Avoid running critical signal traces (clocks, resets, interrupts, control signals, and so forth) near PCB edges.
- Add high frequency filtering: Decoupling capacitors close to the receivers rather than close to the drivers to minimize ESD coupling.
- Put a ground (guard) ring around the entire periphery of the PCB to act as a lightning rod.
- Connect the guard ring to the PCB ground plane to provide a low impedance path for ESD-coupled current on the ring.
- Fill unused portions of the PCB with ground plane.
- Minimize circuit loops between power and ground by using multilayer PCB with dedicated power and ground planes.
- Shield long line length (strip lines) to minimize radiated ESD.
- Avoid running traces over split ground planes. It is better to use a bridge connecting the two planes in one area.

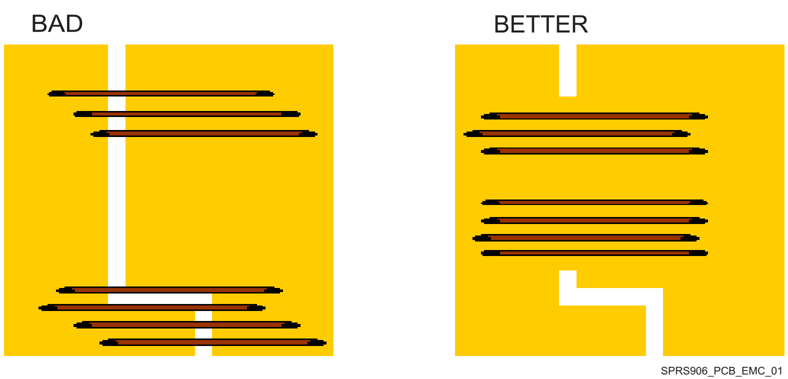


Figure 8-11. Trace Examples

- Always route signal traces and their associated ground returns as close to one another as possible to minimize the loop area enclosed by current flow:
  - At high frequencies current follows the path of least inductance.
  - At low frequencies current flows through the path of least resistance.

8.2.5.3 ESD Protection System Design Consideration

ESD protection system design consideration is covered in Section 8.5.2.2 of this document. The following are additional considerations for ESD protection in a system.

- Metallic shielding for both ESD and EMI
- Chassis GND isolation from the board GND
- Air gap designed on board to absorb ESD energy
- Clamping diodes to absorb ESD energy
- Capacitors to divert ESD energy
- The use of external ESD components on the DP/DM lines may affect signal quality and are not recommended.

8.2.6 EMI / EMC Issues Prevention

All high speed digital integrated circuits can be sources of unwanted radiation, which can affect nearby sensitive circuitry and cause the final product to have radiated emissions levels above the limits allowed by the EMC regulations if some preventative steps are not taken.

Likewise, analog and digital circuits can be susceptible to interference from the outside world and picked up by the circuitry interconnections.

To minimize the potential for EMI/EMC issues, the following guidelines are recommended to be followed.

8.2.6.1 Signal Bandwidth

To evaluate the frequency of a digital signal, an estimated rule of thumb is to consider its bandwidth f_{BW} with respect to its rise time, t_R:

$f_{BW} \approx 0.35 / t_R$

This frequency actually corresponds to the break point in the signal spectrum, where the harmonics start to decay at 40 dB per decade instead of 20 dB per decade.

8.2.6.2 Signal Routing

8.2.6.2.1 Signal Routing—Sensitive Signals and Shielding

Keep radio frequency (RF) sensitive circuitry (like GPS receivers, GSM/WCDMA, Bluetooth/WLAN transceivers, frequency modulation (FM) radio) away from high speed ICs (the device, power and audio manager, chargers, memories, and so forth) and ideally on the opposite side of the PCB. For improved protection it is recommended to place these emission sources in a shield can. If the shield can have a removable lid (two-piece shield), ensure there is low contact impedance between the fence and the lid. Leave some space between the lid and the components under it to limit the high-frequency currents induced in the lid. Limit the shield size to put any potential shield resonances above the frequencies of interest; see Figure 8-8, *Typical Impedance Profile of a Capacitor*.

8.2.6.2.2 Signal Routing—Outer Layer Routing

In case there is a need to use the outer layers for routing outside of shielded areas, it is recommended to route only static signals and ensure that these static signals do not carry any high-frequency components (due to parasitic coupling with other signals). In case of long traces, make provision for a bypass capacitor near the signal source.

Routing of high-frequency clock signals on outer layers, even for a short distance, is discouraged, because their emissions energy is concentrated at the discrete harmonics and can become significant even with poor radiators.

Coplanar shielding of traces on outer layers (placing ground near the sides of a track along its length) is effective only if the distance between the trace sides and the ground is smaller that the trace height above the ground reference plane. For modern multilayer PCBs this is often not possible, so coplanar shielding will not be effective. Do not route high-frequency traces near the periphery of the PCB, as the lack of a ground reference near the trace edges can increase EMI: see Section 8.2.6.3, *Ground Guidelines*.

8.2.6.3 Ground Guidelines

8.2.6.3.1 PCB Outer Layers

Ideally the areas on the top and bottom layers of the PCB that are not enclosed by a shield should be filled with ground after the routing is completed and connected with an adequate number of vias to the ground on the inner ground planes.

8.2.6.3.2 Metallic Frames

Ensure that all metallic parts are well connected to the PCB ground (like LCD screens metallic frames, antennas reference planes, connector cages, flex cables grounds, and so forth). If using flex PCB ribbon cables to bring high-frequency signals off the PCB, ensure they are adequately shielded (coaxial cables or flex ribbons with a solid reference ground).

8.2.6.3.3 Connectors

For high-frequency signals going to connectors choose a fully shielded connector, if possible (for example, SD card connectors). For signals going to external connectors or which are routed over long distances, it is recommended to reduce their bandwidth by using low-pass filters (resistor, capacitor (RC) combinations or lossy ferrite inductors). These filters will help to prevent emissions from the board and can also improve the immunity from external disturbances.

8.2.6.3.4 Guard Ring on PCB Edges

The major advantage of a multilayer PCB with ground-plane is the ground return path below each and every signal or power trace.

As shown in Figure 8-12 the field lines of the signal return to PCB ground as long as an infinite ground is available.

Traces near the PCB-edges do not have this infinite ground and therefore may radiate more than the others. Thus, signals (clocks) or power traces (core power) identified to be critical must not be routed in the vicinity of PCB edges, or, if not avoidable, must be accompanied by a guard ring on the PCB edge.

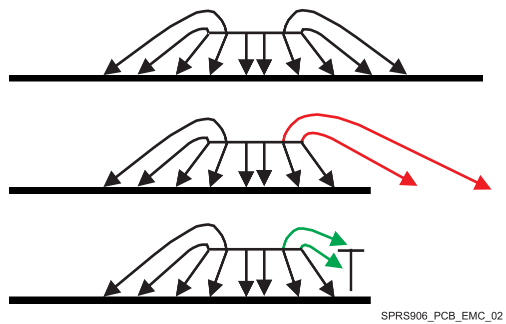


Figure 8-12. Field Lines of a Signal Above Ground

Figure 8-13. Guard Ring Routing

The intention of the guard ring is that HF-energy, that otherwise would have been emitted from the PCB edge, is reflected back into the board where it partially will be absorbed. For this purpose ground traces on the borders of all layers (including power layer) must be applied as shown in Figure 8-13.

As these traces must have the same (HF–) potential as the ground plane they must be connected to the ground plane at least every 10 mm.

8.2.6.3.5 Analog and Digital Ground

For the optimum solution, the AGND and the DGND planes must be connected together at the power supply source in a same point. This ensures that both planes are at the same potential, while the transfer of noise from the digital to the analog domain is minimized.

8.3 Core Power Domains

This section provides boundary conditions and theoretical background to be applied as a guide for optimizing a PCB design. The decoupling capacitor and PDN characteristics tables shown below give recommended capacitors and PCB parameters to be followed for schematic and PCB designs. Board designs that meet the static and dynamic PDN characteristics shown in tables below will be aligned to the expected PDN performance needed to optimize SoC performance.

8.3.1 General Constraints and Theory

- Max PCB static/DC voltage drop (IRd) budget of **1.5% of supply voltage** when using PMICs **without remote sensing** as measured from PMIC's power inductor and filter capacitor node to Processor input including any ground return losses.
- Max PCB static/DC voltage drop (IRd) budget can be relaxed to **5% of supply voltage** when using PMICs **with remote sensing at the load** as measured from PMIC's power inductor and filter capacitor node to Device's supply input including any ground return losses.
- PMIC component DM and guidelines should be referenced for the following:
  – Routing remote feedback sensing to optimize per each SMPS's implementation
  – Selecting power filtering capacitor values and PCB placement.
- Max Effective Resistance (Reff) budget can range from **4 – 50mΩ** for key Device power rails not including ground returns depending upon maximum load currents and maximum DC voltage drop budget (as discussed above).
- Max Device supply input voltage difference budget of **5mV** under max current loading shall be maintained across all balls connected to a common power rail. This represents any voltage difference that may exist between a remote sense point to any power input.
- Max PCB Loop Inductance (LL) budget between Device's power inputs and local bulk and high frequency decoupling capacitors including ground returns should range from **0.4 – 2.5nH depending upon maximum transient load currents.**
- Max PCB dynamic/AC peak-to-peak transient noise voltage budgets between PMIC and Device including ground returns are as follows:
  – **+/-3% of nominal supply voltage** for frequencies below the PMIC bandwidth (typ Fpmic ~ 200kHz)
  – **+/-5% of nominal supply voltage** for frequencies between Fpmic to Fpcb (typ 20 – 100MHz)

- Max PCB Impedance (Z) vs Frequency (F) budget between Device's power inputs and PMIC's output power filter node including ground return is determined by applying the Frequency Domain Target Impedance Method to determine the PCB's maximum frequency of interest (Fpcb). Ideally a properly designed and decoupled PDN will exhibit smoothly increasing Z vs. F curve. There are 2 general regions of interest as can be seen in Figure 8-14.
  – 1^{st} area is from DC (0Hz) up to Fpmic (typ a few 100 kHz) where a PMIC's transient response characteristic (that is, Switching Freq, Compensation Loop BW) dominate. A PDN's Z is typically very low due to power filtering & bulk capacitor values when PDN has very low trace resistance (that is, good Reff performance). The goal is to maintain a smoothly increasing Z that is less than Zt1 over this low frequency range. This will ensure that a max transient current event will not cause a voltage drop more than the PMIC's current step response can support (typ 3%).
  – 2^{nd} area is from Fpmic up to Fpcb (typ 20-100MHz) where a PCB's inherent characteristics (that is, parasitic capacitance, planar spreading inductances) dominate. A PDN's Z will naturally increase with frequency. At frequencies between Fpmic up to Fpcb, the goal is to maintain a smoothly increasing Z to be less than Zt2. This will ensue that the high frequency content of a max transient current event will not cause a voltage drop to be more than 5% of the min supply voltage.

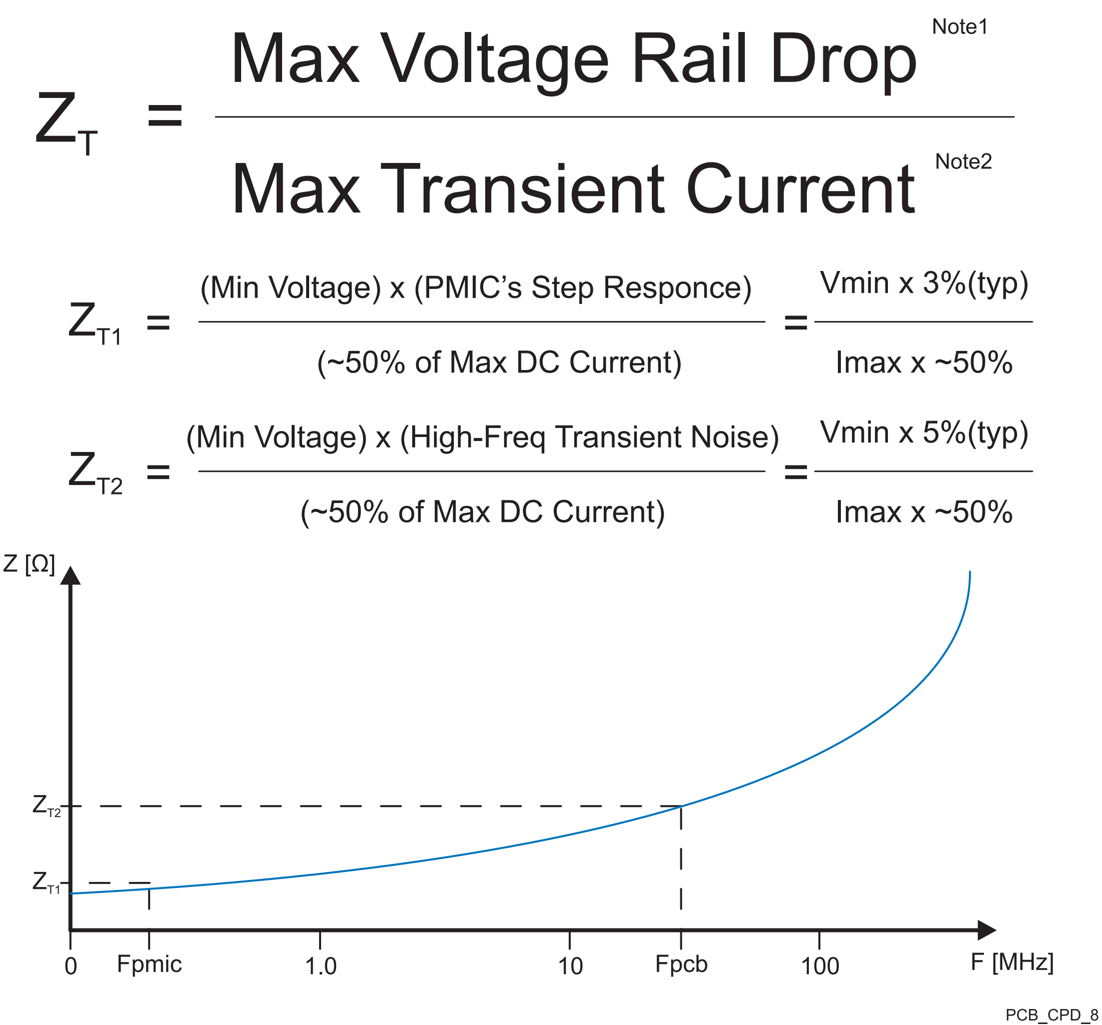


Figure 8-14. PDN's Target impedance

1.Voltage Rail Drop includes regulation accuracy, voltage distribution drops, and all dynamic events such as transient noise, AC ripple, voltage dips etc.

2.Typical max transient current is defined as 50% of max current draw possible.

8.3.2 Voltage Decoupling

Recommended power supply decoupling capacitors main characteristics for commercial products whose ambient temperature is not to exceed +85C are shown in table below:

Table 8-1. Commercial Applications Recommended Decoupling Capacitors Characteristics(1)(2)(3)

Value	Voltage [V]	Package	Stability	Dielectric	Capacitance Tolerance	Temp Range [°C]	Temp Sensitivity [%]	REFERENCE
22µF	6,3	0603	Class 2	X5R	- / + 20%	-55 to + 85	- / + 15	GRM188R60J226MEA0L
10µF	4,0	0402	Class 2	X5R	- / + 20%	-55 to + 85	- / + 15	GRM155R60G106ME44
4.7µF	6,3	0402	Class 2	X5R	- / + 20%	-55 to + 85	- / + 15	GRM155R60J475ME95
2.2µF	6,3	0402	Class 2	X5R	- / + 20%	-55 to + 85	- / + 15	GRM155R60J225ME95
1µF	6,3	0201	Class 2	X5R	- / + 20%	-55 to + 85	- / + 15	GRM033R60J105MEA2
470nF	6,3	0201	Class 2	X5R	- / + 20%	-55 to + 85	- / + 15	GRM033R60G474ME90
220nF	6,3	0201	Class 2	X5R	- / + 20%	-55 to + 85	- / + 15	GRM033R60J224ME90
100nF	6,3	0201	Class 2	X5R	- / + 20%	-55 to + 85	- / + 15	GRM033R60J104ME19

(1) Minimum value for each PCB capacitor: 100 nF.

(2) Among the different capacitors, 470 nF is recommended (not required) to filter at 5-MHz to 10-MHz frequency range.

(3) In comparison with the EIA Class 1 dielectrics, Class 2 dielectric capacitors tend to have severe temperature drift, high dependence of capacitance on applied voltage, high voltage coefficient of dissipation factor, high frequency coefficient of dissipation, and problems with aging due to gradual change of crystal structure. Aging causes gradual exponential loss of capacitance and decrease of dissipation factor.

Recommended power supply decoupling capacitors main characteristics for automotive products are shown in table below:

Table 8-2. Automotive Applications Recommended Decoupling Capacitors Characteristics (1)(2)

Value	Voltage [V]	Package	Stability	Dielectric	Capacitance Tolerance	Temp Range [°C]	Temp Sensitivity [%]	REFERENCE
22µF	6,3	1206	Class 2	X7R	- / + 20%	-55 to + 125	- / + 15	GCM31CR70J226ME23
10µF	6,3	0805	Class 2	X7R	- / + 20%	-55 to + 125	- / + 15	GCM21BR70J106ME22
4.7µF	10	0805	Class 2	X7R	- / + 20%	-55 to + 125	- / + 15	GCM21BC71A475MA73
2.2µF	6,3	0603	Class 2	X7R	- / + 20%	-55 to + 125	- / + 15	GCM188R70J225ME22
1µF	16	0603	Class 2	X7R	- / + 20%	-55 to + 125	- / + 15	GCM188R71C105MA64
470nF	16	0603	Class 2	X7R	- / + 20%	-55 to + 125	- / + 15	GCM188R71C474MA55
220nF	25	0603	Class 2	X7R	- / + 20%	-55 to + 125	- / + 15	GCM188L81C224MA37
100nF	16	0402	Class 2	X7R	- / + 20%	-55 to + 125	- / + 15	GCM155R71C104MA55

(1) Minimum value for each PCB capacitor: 100 nF.

(2) Among the different capacitors, 470 nF is recommended (not required) to filter at 5-MHz to 10-MHz frequency range.

8.3.3 Static PDN Analysis

One power net parameter derived from a PCB's PDN static analysis is the Effective Resistance (Reff). This is the total PCB power net routing resistance that is the sum of all the individual power net segments used to deliver a supply voltage to the point of load and includes any series resistive elements (that is, current sensing resistor) that may be installed between the PMIC outputs and Processor inputs.

8.3.4 Dynamic PDN Analysis

Three power net parameters derived from a PCB's PDN dynamic analysis are the Loop Inductance (LL), Impedance (Z) and PCB Frequency of Interest (Fpcb).

- LL values shown are the recommended max PCB trace inductance between a decoupling capacitor's power supply and ground reference terminals when viewed from the decoupling capacitor with a "theoretical shorted" applied across the Processor's supply inputs to ground reference.
- Z values shown are the recommended max PCB trace impedances allowed between Fpmic up to Fpcb frequency range that limits transient noise drops to no more than 5% of min supply voltage during max transient current events.
- Fpcb (Frequency of Interest) is defined to be a power rail's max frequency after which adding a reasonable number of decoupling capacitors no longer significantly reduces the power rail impedance below the desired impedance target (Zt2). This is due to the dominance of the PCB's parasitic planar spreading and internal package inductances.

Table 8-3. Recommended PDN and Decoupling Characteristics (1)(2)(3)(4)(5)

PDN Analysis:	Static	Dynamic			Number of Recommended Decoupling Capacitors per Supply							
Supply	**Max R_{eff} (7) [mΩ]**	**Dec. Cap. Max LL(8) (6) [nH]**	**Max Impedance [mΩ]**	**Frequency range of Interest [MHz]**	**100 nF(6)**	**220 nF**	**470 nF**	**1µF**	**2.2 µF**	**4.7 µF**	**10 µF**	**22 µF**
vdd_mpu	10	2	57	≤20	8	1	1	1	1	1		1
vdd_dsp, vdd_gpu, vdd_iva	13	2.5	54	≤20	8	1	1	1	1	1	1	1
vdd	27	2	87	≤50	6	1	1	1	1	1		
vdds_ddr1	10	2.5	200	≤100	8	4		2		2		1
cap_vbbldo_dsp	N/A	6	N/A	N/A				1				
cap_vbbldo_gpu	N/A	6	N/A	N/A				1				
cap_vbbldo_iva	N/A	6	N/A	N/A				1				
cap_vbbldo_mpu	N/A	6	N/A	N/A				1				
cap_vddram_core1	N/A	6	N/A	N/A				1				
cap_vddram_core3	N/A	6	N/A	N/A				1				
cap_vddram_core4	N/A	6	N/A	N/A				1				
cap_vddram_dsp	N/A	6	N/A	N/A				1				
cap_vddram_gpu	N/A	6	N/A	N/A				1				
cap_vddram_iva	N/A	6	N/A	N/A				1				
cap_vddram_mpu	N/A	6	N/A	N/A				1				

(1) For more information on peak-to-peak noise values, see the Recommended Operating Conditions table of the Specifications chapter.

(2) ESL must be as low as possible and must not exceed 0.5 nH.

(3) The PDN (Power Delivery Network) impedance characteristics are defined versus the device activity (that runs at different frequency) based on the Recommended Operating Conditions table of the Specifications chapter.

(4) The static drop requirement drives the maximum acceptable PCB resistance between the PMIC or the external SMPS and the processor power balls.

(5) Assuming that the external SMPS (power IC) feedback sense is taken close to processor power balls.

(6) High-frequency (30 to 70MHz) PCB decoupling capacitors

(7) Maximum R_{eff} from SMPS to Processor.

(8) Maximum Loop Inductance for decoupling capacitor.

8.3.5 *Power Supply Mapping*

TPS65917 or TPS659039 are the Power Management ICs (PMICs) that should be used for the Device designs. TI requires use of these PMICs for the following reasons:

- TI has validated their use with the Device
- Board level margins including transient response and output accuracy are analyzed and optimized for the entire system
- Support for power sequencing requirements (refer to Section 5.10 *Power Supply Sequences*)
- Support for Adaptive Voltage Scaling (AVS) Class 0 requirements, including TI provided software

Whenever we allow for combining of rails mapped on any of the SMPSes, the PDN guidelines that are the most stringent of the rails combined should be implemented for the particular supply rail.

It is possible that some voltage domains on the device are unused in some systems. In such cases, to ensure device reliability, it is still required that the supply pins for the specific voltage domains are connected to some core power supply output.

These unused supplies though can be combined with any of the core supplies that are used (active) in the system. For example if IVA and GPU domains are not used, they can be combined with the CORE domain, thereby having a single power supply driving the combined CORE, IVA and GPU domains.

For the combined rail, the following relaxations do apply:

- The AVS voltage of active rail in the combined rail needs to be used to set the power supply
- The decoupling capacitance should be set according to the active rail in the combined rail

Table 8-4 illustrates the approved and validated power supply connections to the Device for the SMPS outputs of the TPS659039 PMIC.

Table 8-4. TPS659039 Power Supply Connections(1)

SMPS	Valid Combination 1: Reference Platform	Valid Combination 2: MPU Centric	TPS659039 Current Rating Limitation(3) (4)
SMPS1/2/3(2)	vdd_mpu	vdd_mpu	SMPS1/2: 6A SMPS1/2/3: 9A
SMPS3(2)	vdds_ddr1	vdds_ddr1	SMPS3: 3A
SMPS4/5	vdd_dsp	vdd_dsp, vdd_gpu, vdd_iva	SMPS4/5: 4A
SMPS6	vdd_gpu	vdd	SMPS6: 2-3A (BOOST_CURRENT=0/1)
SMPS7	vdd	Free	2A
SMPS8	vdd_iva	Free	1A
SMPS9	vdds18v	vdds18v	1A

(1) Power consumption is highly application-specific. Separate analysis must be performed to ensure output current ratings (average and peak) is within the limits of the PMIC for all rails of the device.

(2) Dual phase (SMPS1/2) can be used as long as the peak power consumption is maintained below the SMPS1/2 capacity

a. For the latest rated output current specifications for the TPS659039 device, please refer to the PMIC data manual.

b. MPU power consumption is highly system dependent. A detailed power consumption estimate must be performed to confirm compatibility. Example: Single vs Dual MPU, OPP_NOM vs OPP_OD vs OPP_HIGH, TPS659039 configured with $V_I \geq 3V$ vs $V_I < 3V$, etc. Contact your TI representative for details.

(3) Refer to the PMIC data manual for the latest TPS659039 specifications.

(4) A product's maximum ambient temperature, thermal system design & heat spreading performance could limit the maximum power dissipation below the full PMIC capacity in order to not exceed recommended SoC max Tj.

Table 8-5 illustrates the approved and validated power supply connections to the Device for the SMPS outputs of the TPS65917 PMIC.

Table 8-5. TPS65917 Power Supply Connections

TPS65917	Valid Combination 1:	Valid Combination 2:	TPS65917 Current Rating Limitation (1) (3)
SMPS1	vdd_mpu	vdd_mpu	3.5A
SMPS2 (2)	vdd_dsp, vdd_gpu, vdd_iva	vdd	3.5A
SMPS3 (2)	vdd	vdd_dspeve, vdd_gpu, vdd_iva	3A
SMPS4 (3)	vdds18v	vdds18v	1.5A
SMPS5 (4)	vdds_ddr1	vdds_ddr1	2A

(1) Refer to the TPS65917 Data Manual for exact current rating limitations, including assumed V_{IN} and other parameters. Values provided in this table are for comparison purposes.

(2) DSP, EVE, GPU, and IVAHD power consumption is highly application-specific. Separate analysis must be performed to ensure output current ratings (average and peak) is within the limits of the PMIC. VDD only supports OPP_NOM.

(3) Highly application-specific. Separate analysis must be performed to ensure average and peak power is within the limits of the PMIC.

(4) Furthermore, if SMPS5 is used for DDR power, both total memory + SoC power must be within the PMIC limits.

8.3.6 DPLL Voltage Requirement

The voltage input to the DPLLs has a low noise requirement. Board designs should supply these voltage inputs with a low noise LDO to ensure they are isolated from any potential digital switching noise. The TPS65917 PMIC LDOLN output is specifically designed to meet this low noise requirement.

NOTE

For more information about Input Voltage Sources, see Section 6.2 *DPLLs, DLLs Specifications*.

Table 8-4 present the voltage inputs that supply the DPLLs.

Table 8-6. Input Voltage Power Supplies for the DPLLs

POWER SUPPLY	DPLLs
vdda_per	DPLL_PER and PER HSDIVIDER analog power supply
vdda_ddr	DPLL_DDR and DDR HSDIVIDER analog power supply
vdda_debug	DPLL_DEBUG analog power supply
vdda_dsp_iva	DPLL_DSP and DPLL_IVA analog power supply
vdda_core_gmac	DPLL_CORE and HSDIVIDER analog power supply
vdda_gpu	DPLL_GPU analog power supply
vdda_video	DPLL_VIDEO1 analog power supply
vdda_mpu_abe	DPLL_MPU and DPLL_ABE analog power supply
vdda_osc	not DPLL input but is required to be supplied by low noise input voltage
vdda_pll_spare	DPLL_SPARE analog power supply

8.3.7 Loss of Input Power Event

A few key PDN design items needed to enable a controlled and compliant SoC power down sequence for a “Loss of Input Power” event are:

- “Loss of Input Power” early warning.
  - TI EVM and Reference Design Study SCHs and PDNs achieve this by using the First Stage Converter’s (that is, LM536033-Q1) Power Good status output to enable and disable the Second Stage PMIC devices (that is, TPS65917/919, LP8733, and LP8732). If a different First Stage Converter is used, care must be taken to ensure an adequate “PG_Status” or “Vbatt_Status” signal is provided that can disable Second Stage PMIC to begin a controlled and compliant SoC power down sequence. The total elapsed time from asserting “PG_Status” low until SoC’s PMIC input voltage reaches minimum level of 2.75 V should be minimum of 1.5 ms and 2 ms preferred.
- Maximize discharge time of First Stage Vout (VSYS_3V3 power rail = input voltage to SoC PMIC).
  - TI EVM and Reference Design Study SCHs and PDNs achieve this by opening an in-line load switch immediately upon “PG_Status” low assertion in order to remove the SoC’s 3.3 V IO load current from VSYS_3V3. This will extend the VSYS_3V3 power rail’s discharge time in order to maximize elapsed time for allowing SoC PMIC to execute a controlled and compliant power down sequence. Care should be taken to either disable or isolate any additional peripheral components that may be loading the VSYS_3V3 rail as well.
- Sufficient bulk decoupling capacitance on the First Stage Vout (VSYS_3V3 per PDN) that allows for desired 1.5 – 2 ms elapsed time as described above.
  - TI EVM and Reference Design Study SCHs and PDNs achieve this by using 200 μF of total capacitance on VSYS_3V3. The First Stage Converter (that is, LM536033-Q1) can typically drive a max of 400 μF to help extend VSYS_3V3 discharge time for a compliant SoC power down sequence.
- Optimizing the Second Stage SoC PMIC’s OTP settings that determines SoC power up and down sequences and total elapsed time needed for a controlled sequence.
  - TI EVM and Reference Design Study SCHs and PDNs achieve this by using optimized OTPs per the SCH and components used. The definition of these OTPs is captured in the detailed timing diagrams for both power up and down sequences. The PDN diagram typically shows a recommended PMIC OTP ID based upon the SoC and DDR memory types.

8.3.8 Example PCB Design

The following sections describe an example PCB design and its resulting PDN performance for the vdd_mpu key processor power domain.

NOTE

Materials presented in this section are based on generic PDN analysis on PCB boards and are not specific to systems integrating the Device.

8.3.8.1 Example Stack-up

Layer Assignments:

- Layer Top: Signal and Segmented Power Plane
  - Processor and PMIC components placed on Top-side
- Layer 2: Gnd Plane1
- Layer 3: Signals
- Layer n: Power Plane1
- Layer n+1: Power Plane 2
- Layer n+2: Signal
- Layer n+3: Gnd Plane2
- Layer Bottom: Signal and Segmented Power Planes
  - Decoupling caps, etc.

Via Technology: Through-hole

Copper Weight:

- ½ oz for all signal layers.
- 1-2oz for all power plane for improved PCB heat spreading.

8.3.8.2 vdd Example Analysis

Maximum acceptable PCB resistance (R_{eff}) between the PMIC and Processor input power balls should not exceed 10mΩ.

Maximum decoupling capacitance loop inductance (LL) between Processor input power balls and decoupling capacitances should not exceed 2.0nH (ESL NOT included)

Impedance target for key frequency of interest between Processor input power balls and PMIC's SMPS output power balls should not exceed 57mΩ at 20MHz.

Table 8-7. Example PCB vdd PI Analysis Summary

Parameter	Recommendation	Example PCB
OPP	OPP_NOM	
Clocking Rate	266 MHz	
Voltage Level	1 V	1 V
Max Current Draw	1 A	1 A
Max Effective Resistance: Power Inductor Segment Total R_{eff}	10mΩ	9.7 mΩ
Max Loop Inductance	2.0nH	0.97 –1.75nH
Impedance Target	57mΩ F<20Mhz	57mΩ F<20Mhz

Figure 8-15 show a PCB layout example and the resulting PI analysis results.

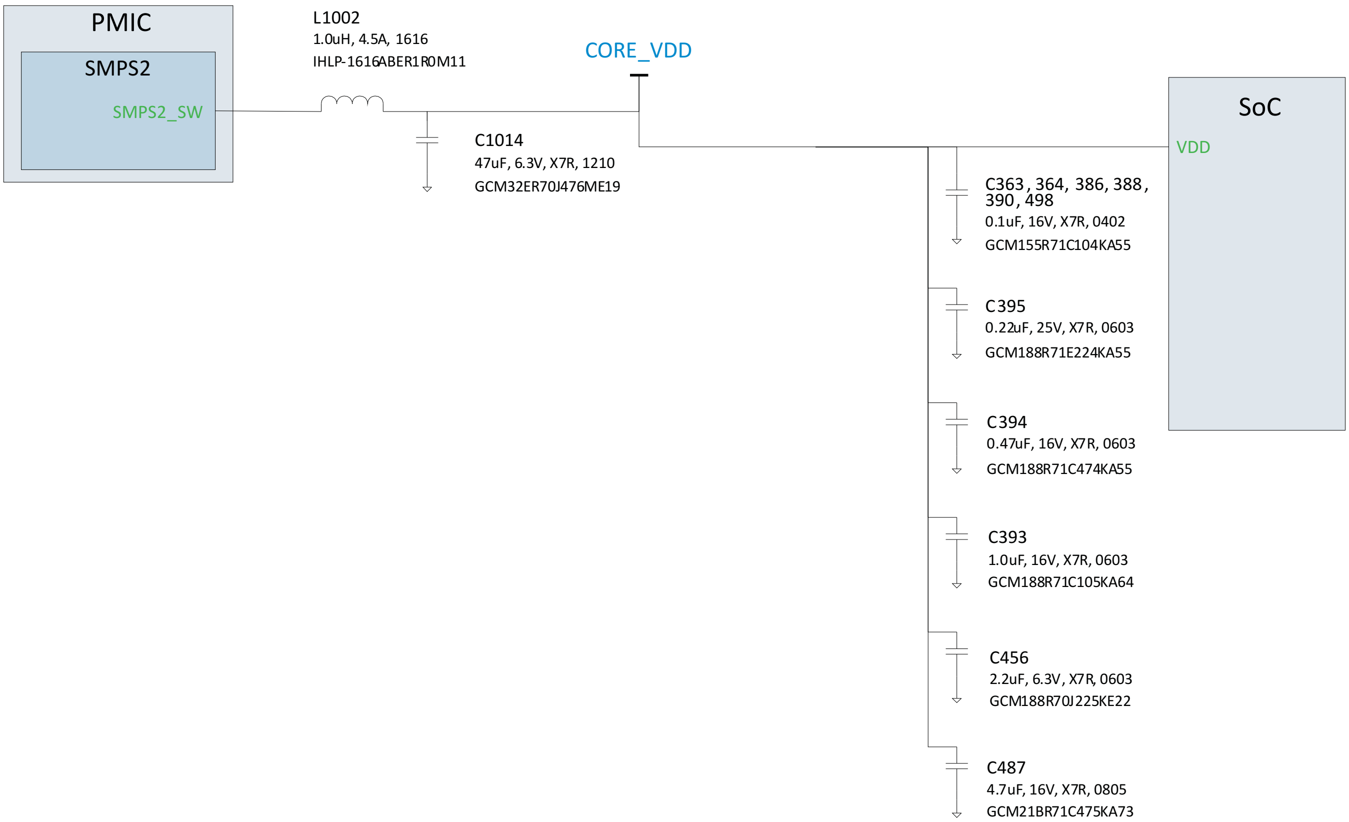


Figure 8-15. vdd Simplified SCH Diagram

NOTE

PCB Etch Resistance Breakdown, PDN Effective Resistance, and vdd routings are UNDER DEVELOPMENT!

IR Drop: vdd (PCB Rev Oct25, CAD sPSI v13.1.1)

- Source Conditions: 1V @ 1A
- Power Plane/Trace Effective Resistances
  – From PMIC SMPS to SoC load = 9.7mohm
  – From Power Inductor to SoC load = 6mohm
  – "Open-Loop" Voltage/IR Drop for 1A = 6mV

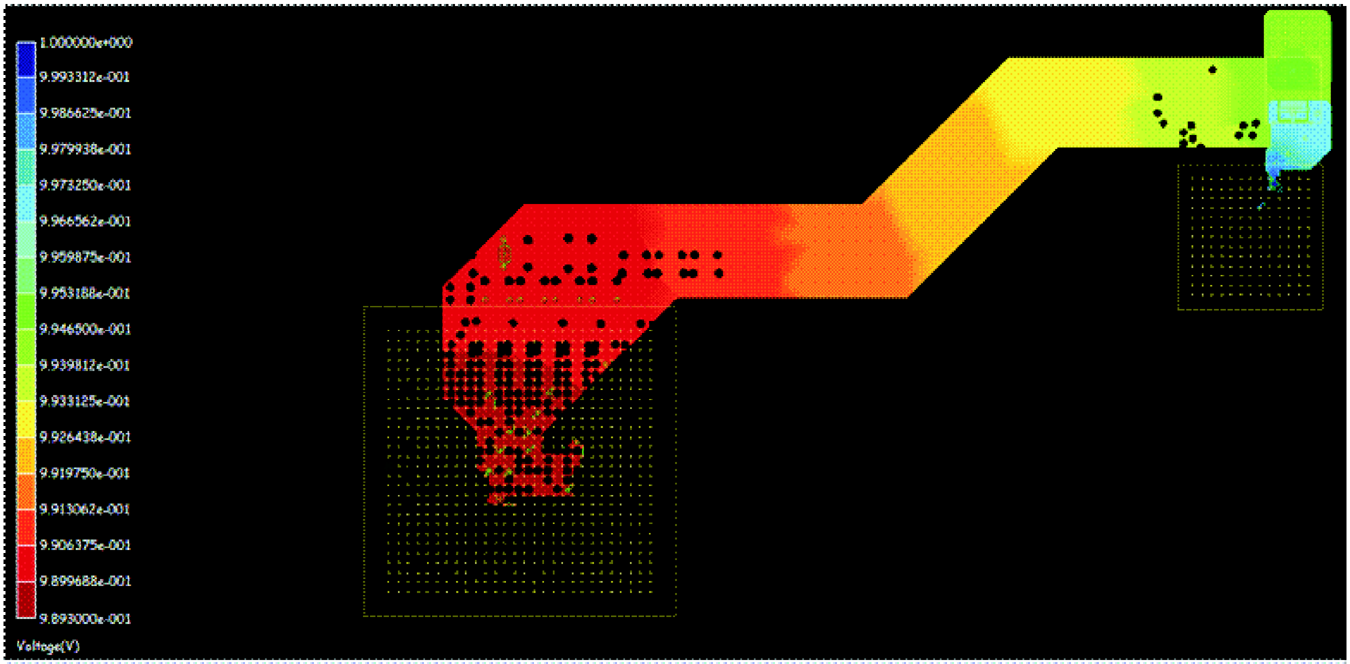


Figure 8-16. vdd Voltage/IR Drop [All Layers]

Dynamic analysis of this PCB design for the CORE power domain determined the vdd decoupling capacitor loop inductance and impedance vs frequency analysis shown below. As you can see, the loop inductance values ranged from 0.97 –1.75nH and were less than maximum 2.0nH recommended.

NOTE

Comparing loop inductances for capacitors at different distances from the SoC's input power balls shows an 18% reduction for caps placed closer. This was derived by averaging the inductances for the 3 caps with distances over 800mils (Avg LL = 1.33nH) vs the 3 caps with distances less than 600mils (Avg LL = 1.096nH).

Table 8-8. Rail - vdd

Cap Ref Des	Model Port #	Loop Inductacne [nH]	Footprint Types	PCB Side	Distance to Ball-Field [mils]	Value [µF]	Size
C487	10	0.97	4vWSE	Top	521	4.7	0805
C393	6	1.11	4vWSE	Bottom	358	1.0	0603
C394	7	1.12	4vWSE	Bottom	357	0.47	0603
C456	9	1.13	4vWSE	Bottom	403	2.2	0603
C386	3	1.16	2vWSE	Bottom	40	0.1	0402
C395	8	1.18	4vWSE	Bottom	460	0.22	0603
C363	1	1.46	2vWSE	Bottom	40	0.1	0402
C390	5	1.48	2vWSE	Bottom	40	0.1	0402
C364	2	1.74	2vWSE	Bottom	40	0.1	0402
C498	11	1.74	2vWSE	Bottom	40	0.1	0402
C388	4	1.75	2vWSE	Bottom	40	0.1	0402

Loop Inductance range: 0.97 –1.75nH

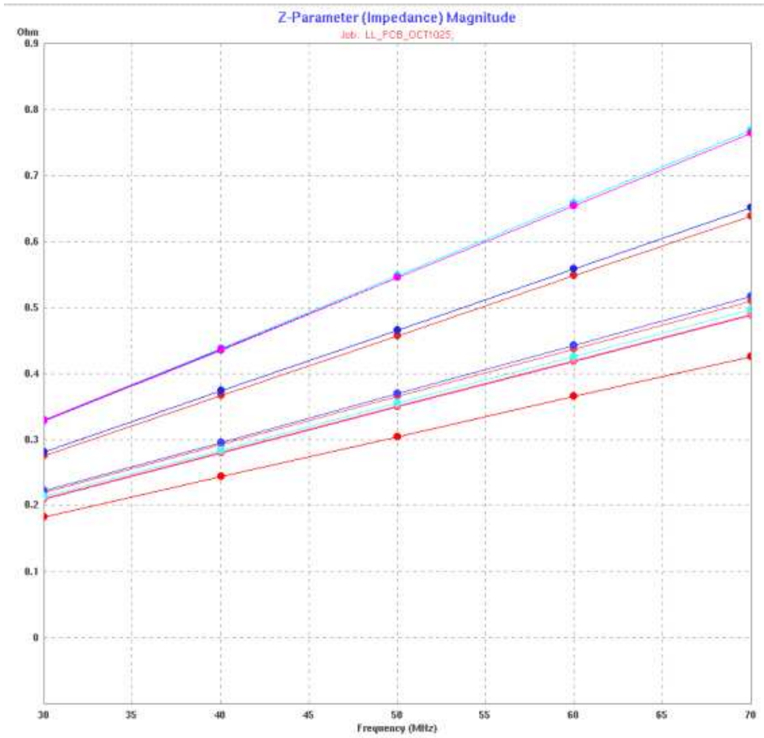


Figure 8-17. vdd Decoupling Cap Loop Inductances

Figure 8-18 shows vdd Impedance vs Frequency characteristics.

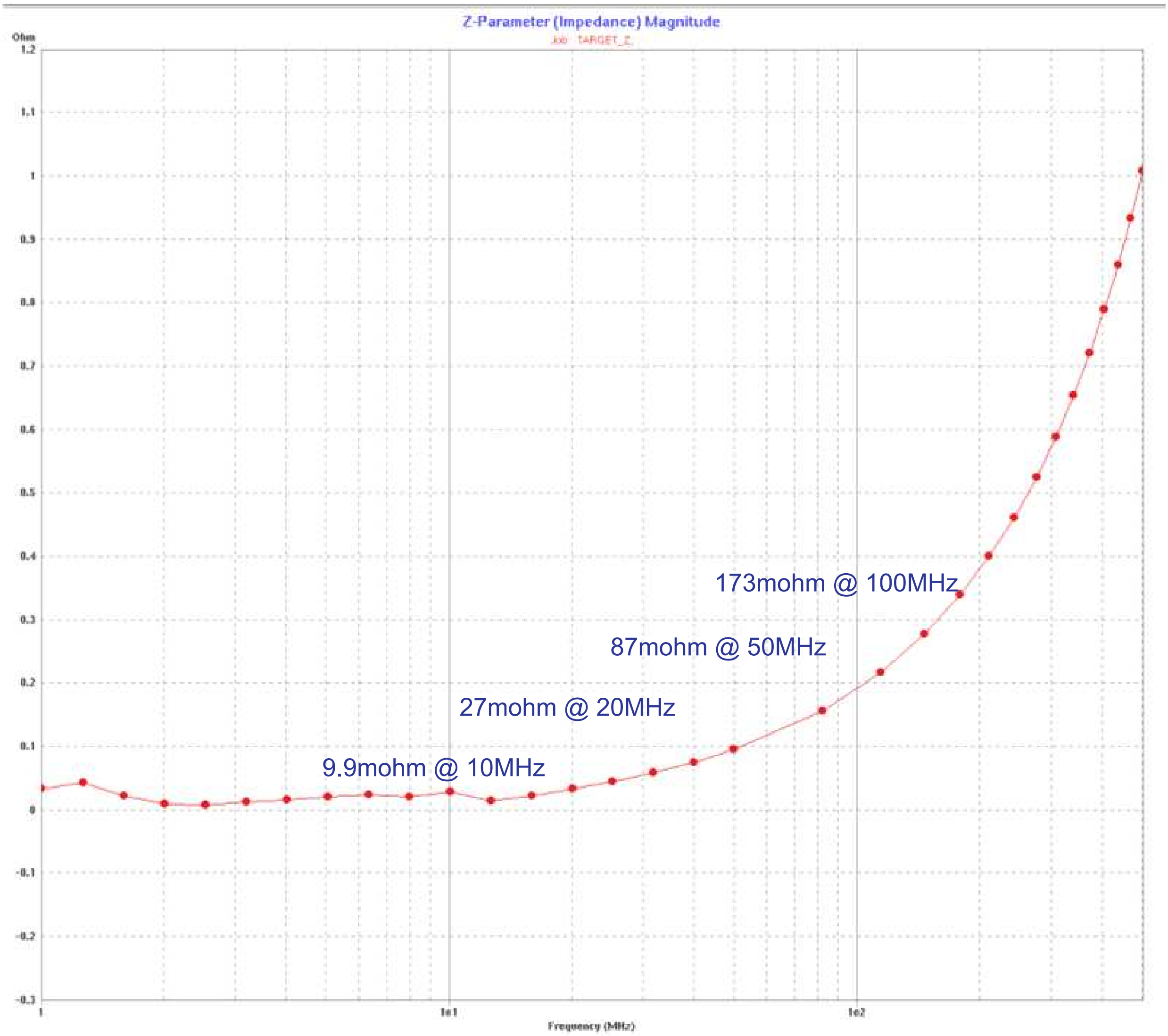


Figure 8-18. vdd Impedance vs Frequency

8.4 Single-Ended Interfaces

8.4.1 General Routing Guidelines

The following paragraphs detail the routing guidelines that must be observed when routing the various functional LVCMOS interfaces.

- Line spacing:
  – For a line width equal to W, the spacing between two lines must be 2W, at least. This minimizes the crosstalk between switching signals between the different lines. On the PCB, this is not achievable everywhere (for example, when breaking signals out from the device package), but it is recommended to follow this rule as much as possible. When violating this guideline, minimize the length of the traces running parallel to each other (see Figure 8-19).

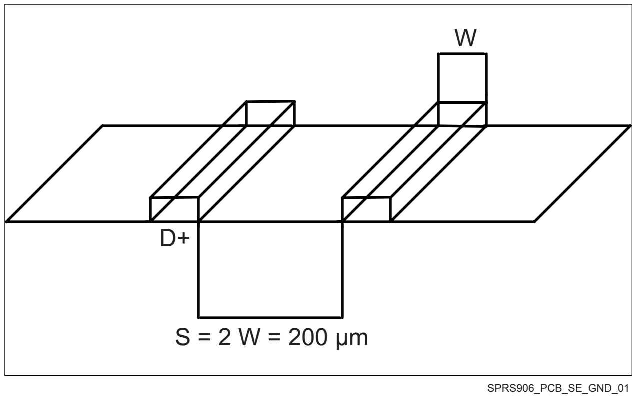


Figure 8-19. Ground Guard Illustration

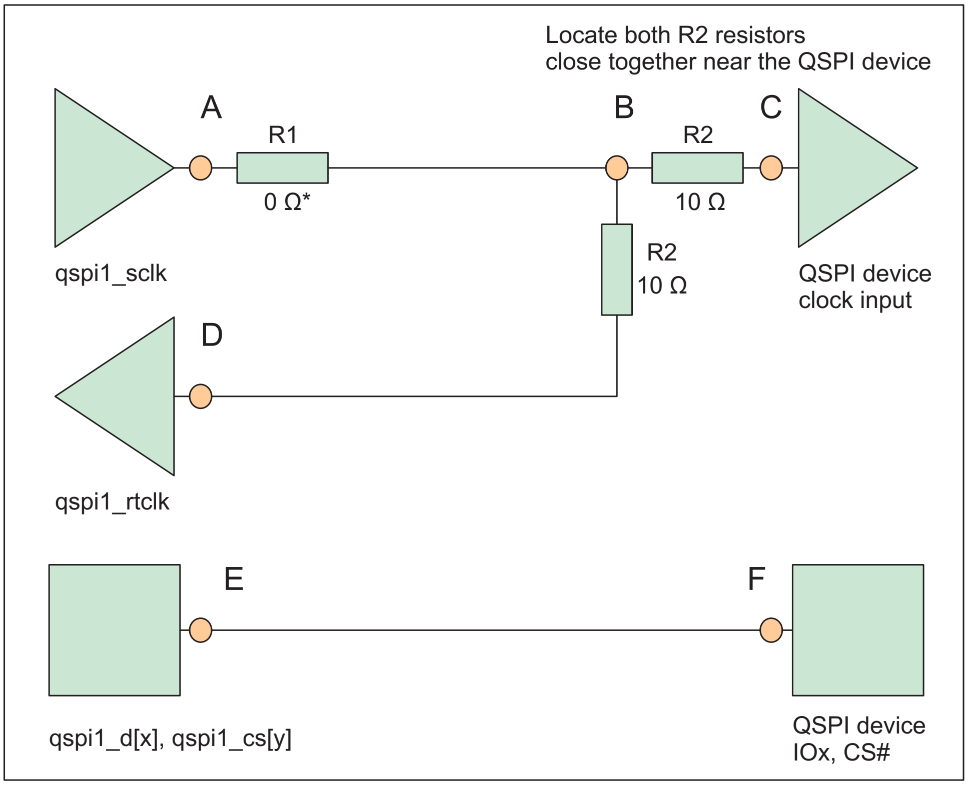
- Length matching (unless otherwise specified):
  – For bus or traces at frequencies less than 10 MHz, the trace length matching (maximum length difference between the longest and the shortest lines) must be less than 25 mm.
  – For bus or traces at frequencies greater than 10 MHz, the trace length matching (maximum length difference between the longest and the shortest lines) must be less than 2.5 mm.
- Characteristic impedance
  – Unless otherwise specified, the characteristic impedance for single-ended interfaces is recommended to be between 35-Ω and 65-Ω.
- Multiple peripheral support
  – For interfaces where multiple peripherals have to be supported in the star topology, the length of each branch has to be balanced. Before closing the PCB design, it is highly recommended to verify signal integrity based on simulations including actual PCB extraction.

8.4.2 QSPI Board Design and Layout Guidelines

The following section details the routing guidelines that must be observed when routing the QSPI interfaces.

- The qspi1_sclk output signal must be looped back into the qspi1_rtclk input.
- The signal propagation delay from the qspi1_sclk ball to the QSPI device CLK input pin (A to C) must be approximately equal to the signal propagation delay from the QSPI device CLK pin to the qspi1_rtclk ball (C to D).
- The signal propagation delay from the QSPI device CLK pin to the qspi1_rtclk ball (C to D) must be approximately equal to the signal propagation delay of the control and data signals between the QSPI device and the SoC device (E to F, or F to E).
- The signal propagation delay from the qspi1_sclk signal to the series terminators (R2 = 10 Ω) near the QSPI device must be < 450pS (~7cm as stripline or ~8cm as microstrip)
- 50 Ω PCB routing is recommended along with series terminations, as shown in Figure 8-20.

- Propagation delays and matching:
  - A to C = C to D = E to F.
  - Matching skew: < 60pS
  - A to B < 450pS
  - B to C = as small as possible (<60pS)



*0 Ω resistor (R1), located as close as possible to the qspi1_sclk pin, is placeholder for fine-tuning if needed.

Figure 8-20. QSPI Interface High Level Schematic

8.5 Differential Interfaces

8.5.1 General Routing Guidelines

To maximize signal integrity, proper routing techniques for differential signals are important for high speed designs. The following general routing guidelines describe the routing guidelines for differential lanes and differential signals.

- As much as possible, no other high-frequency signals must be routed in close proximity to the differential pair.
- Must be routed as differential traces on the same layer. The trace width and spacing must be chosen to yield the differential impedance value recommended.
- Minimize external components on differential lanes (like external ESD, probe points).
- Through-hole pins are not recommended.
- Differential lanes mustn't cross image planes (ground planes).
- No sharp bend on differential lanes.
- Number of vias on the differential pairs must be minimized, and identical on each line of the differential pair. In case of multiple differential lanes in the same interface, all lines should have the same number of vias.

- Shielded routing is to be promoted as much as possible (for instance, signals must be routed on internal layers that are inside power and/or ground planes).

8.5.2 USB 2.0 Board Design and Layout Guidelines

This section discusses schematic guidelines when designing a universal serial bus (USB) system.

8.5.2.1 Background

Clock frequencies generate the main source of energy in a USB design. The USB differential DP/DM pairs operate in high speed mode at 480 Mbps. System clocks can operate at 12 MHz, 48 MHz, and 60 MHz. The USB cable can behave as a monopole antenna; take care to prevent RF currents from coupling onto the cable.

When designing a USB board, the signals of most interest are:

- Device interface signals: Clocks and other signal/data lines that run between devices on the PCB.
- Power going into and out of the cable: The USB connector socket pin 1 (VBUS) may be heavily filtered and need only pass low frequency signals of less than ~100 KHz. The USB socket pin 4 (analog ground) must be able to return the current during data transmission, and must be filtered sparingly.
- Differential twisted pair signals going out on cable, DP and DM: Depending upon the data transfer rate, these device terminals can have signals with fundamental frequencies of 240 MHz (high speed), 6 MHz (full speed), and 750 kHz (low speed).
- External crystal circuit (device terminals XI and X0): 12 MHz, 19.2 MHz, 24 MHz, and 48 MHz fundamental. When using an external crystal as a reference clock, a 24 MHz and higher crystal is highly recommended.

8.5.2.2 USB PHY Layout Guide

The following sections describe in detail the specific guidelines for USB PHY Layout.

8.5.2.2.1 General Routing and Placement

Use the following routing and placement guidelines when laying out a new design for the USB physical layer (PHY). These guidelines help minimize signal quality and electromagnetic interference (EMI) problems on a four-or-more layer evaluation module (EVM).

- Place the USB PHY and major components on the un-routed board first. For more details, see Section 8.5.2.2.2.3.
- Route the high speed clock and high speed USB differential signals with minimum trace lengths.
- Route the high speed USB signals on the plane closest to the ground plane, whenever possible.
- Route the high speed USB signals using a minimum of vias and corners. This reduces signal reflections and impedance changes.
- When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal traces by minimizing impedance discontinuities.
- Do not route USB traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices or IC's that use or duplicate clock signals.
- Avoid stubs on the high speed USB signals because they cause signal reflections. If a stub is unavoidable, then the stub should be less than 200 mils.
- Route all high speed USB signal traces over continuous planes (V_{CC} or GND), with no interruptions. Avoid crossing over anti-etch, commonly found with plane splits.

8.5.2.2.2 Specific Guidelines for USB PHY Layout

The following sections describe in detail the specific guidelines for USB PHY Layout.

8.5.2.2.2.1 Analog, PLL, and Digital Power Supply Filtering

To minimize EMI emissions, add decoupling capacitors with a ferrite bead at power supply terminals for the analog, phase-locked loop (PLL), and digital portions of the chip. Place this array as close to the chip as possible to minimize the inductance of the line and noise contributions to the system. An analog and digital supply example is shown in Figure 8-21. In case of multiple power supply pins with the same function, tie them up to a single low-impedance point in the board and then add the decoupling capacitors, in addition to the ferrite bead. This array of caps and ferrite bead improve EMI and jitter performance. Take both EMI and jitter into account before altering the configuration.

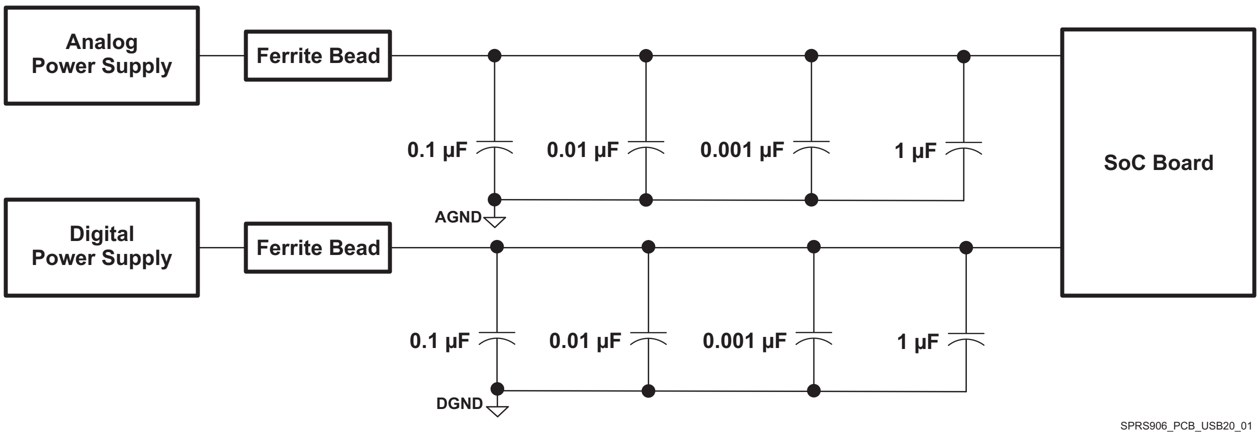


Figure 8-21. Suggested Array Capacitors and a Ferrite Bead to Minimize EMI

Consider the recommendations listed below to achieve proper ESD/EMI performance:

- Use a 0.01 µF cap on each cable power VBUS line to chassis GND close to the USB connector pin.
- Use a 0.01 µF cap on each cable ground line to chassis GND next to the USB connector pin.
- If voltage regulators are used, place a 0.01 µF cap on both input and output. This is to increase the immunity to ESD and reduce EMI. For other requirements, see the device-specific datasheet.

8.5.2.2.2.2 Analog, Digital, and PLL Partitioning

If separate power planes are used, they must be tied together at one point through a low-impedance bridge or preferably through a ferrite bead. Care must be taken to capacitively decouple each power rail close to the device. The analog ground, digital ground, and PLL ground must be tied together to the low-impedance circuit board ground plane.

8.5.2.2.2.3 Board Stackup

Because of the high frequencies associated with the USB, a printed circuit board with at least four layers is recommended; two signal layers separated by a ground and power layer as shown in Figure 8-22.

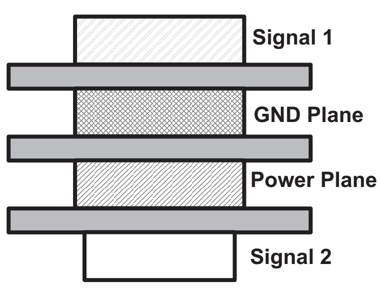


Figure 8-22. Four-Layer Board Stack-Up

The majority of signal traces should run on a single layer, preferably SIGNAL1. Immediately next to this layer should be the GND plane, which is solid with no cuts. Avoid running signal traces across a split in the ground or power plane. When running across split planes is unavoidable, sufficient decoupling must be used. Minimizing the number of signal vias reduces EMI by reducing inductance at high frequencies.

8.5.2.2.2.4 Cable Connector Socket

Short the cable connector sockets directly to a small chassis ground plane (GND *strap*) that exists immediately underneath the connector sockets. This shorts EMI (and ESD) directly to the chassis ground before it gets onto the USB cable. This etch plane should be as large as possible, but all the conductors coming off connector pins 1 through 6 must have the board signal GND plane run under. If needed, scoop out the chassis GND strap etch to allow for the signal ground to extend under the connector pins. Note that the etches coming from pins 1 and 4 (VBUS power and GND) should be wide and via-ed to their respective planes as soon as possible, respecting the filtering that may be in place between the connector pin and the plane. See Figure 8-23 for a schematic example.

Place a ferrite in series with the cable shield pins near the USB connector socket to keep EMI from getting onto the cable shield. The ferrite bead between the cable shield and ground may be valued between 10 Ω and 50 Ω at 100 MHz; it should be resistive to approximately 1 GHz. To keep EMI from getting onto the cable bus power wire (a very large antenna) a ferrite may be placed in series with cable bus power, VBUS, near the USB connector pin 1. The ferrite bead between connector pin 1 and bus power may be valued between 47 Ω and approximately 1000 Ω at 100 MHz. It should continue being resistive out to approximately 1 GHz, as shown in Figure 8-23.

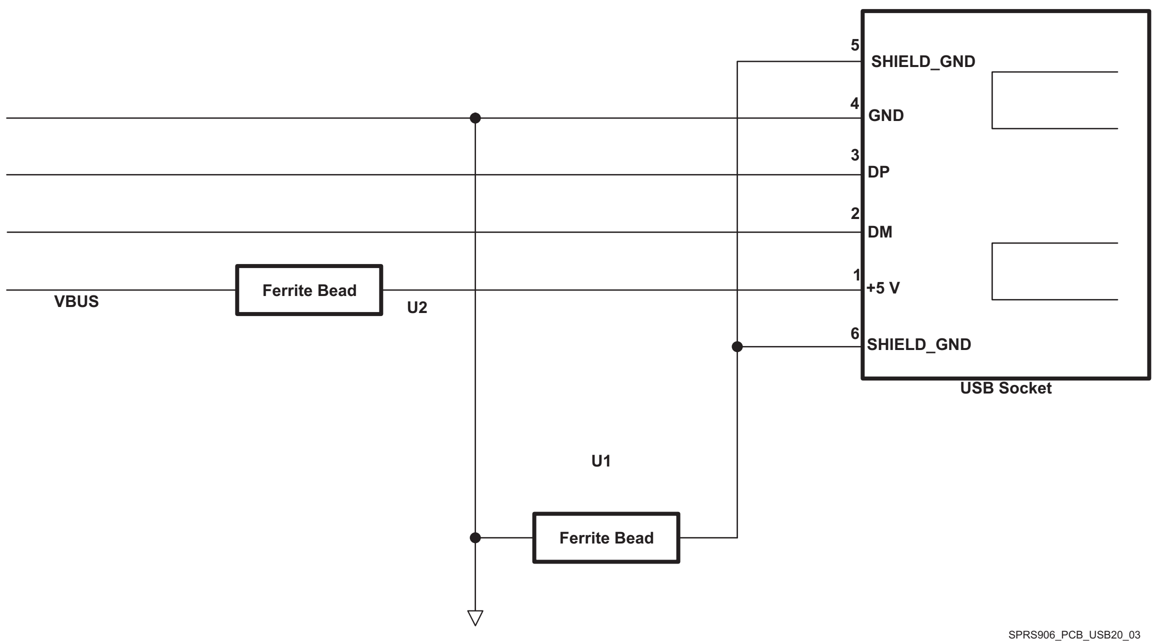


Figure 8-23. USB Connector

8.5.2.2.2.5 Clock Routings

To address the system clock emissions between devices, place a ~10 to 130 Ω resistor in series with the clock signal. Use a trial and error method of looking at the shape of the clock waveform on a high speed oscilloscope and of tuning the value of the resistance to minimize waveform distortion. The value on this resistor should be as small as possible to get the desired effect. Place the resistor close to the device generating the clock signal. If an external crystal is used, follow the guidelines detailed in the Selection and Specification of Crystals for Texas Instruments USB 2.0 Devices.

When routing the clock traces from one device to another, try to use the 3W spacing rule. The distance from the center of the clock trace to the center of any adjacent signal trace should be at least three times the width of the clock trace. Many clocks, including slow frequency clocks, can have fast rise and fall times. Using the 3W rule cuts down on crosstalk between traces. In general, leave space between each of the traces running parallel between the devices. Avoid using right angles when routing traces to minimize the routing distance and impedance discontinuities. For further protection from crosstalk, run guard traces beside the clock signals (GND pin to GND pin), if possible. This lessens clock signal coupling, as shown in Figure 8-24.

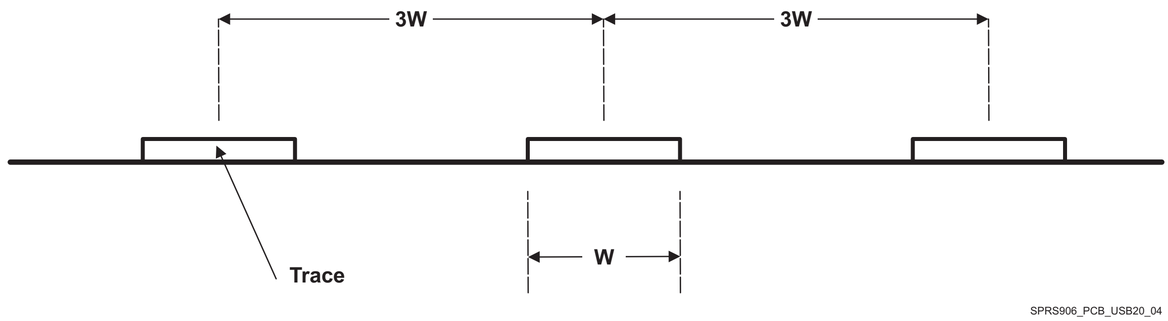


Figure 8-24. 3W Spacing Rule

8.5.2.2.2.6 Crystals/Oscillator

Keep the crystal and its load capacitors close to the USB PHY pins, XI and XO (see Figure 8-25). Note that frequencies from power sources or large capacitors can cause modulations within the clock and should not be placed near the crystal. In these instances, errors such as dropped packets occur. A placeholder for a resistor, in parallel with the crystal, can be incorporated in the design to assist oscillator startup.

Power is proportional to the current squared. The current is $I = C*dv/dt$, because dv/dt is a function of the PHY, current is proportional to the capacitive load. Cutting the load to 1/2 decreases the current by 1/2 and the power to 1/4 of the original value. For more details on crystal selection, see the Selection and Specification of Crystals for Texas Instruments USB 2.0 Devices.

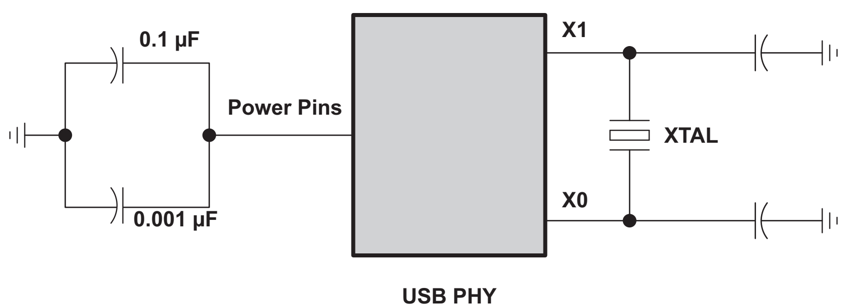


Figure 8-25. Power Supply and Clock Connection to the USB PHY

8.5.2.2.2.7 DP/DM Trace

Place the USB PHY as close as possible to the USB 2.0 connector. The signal swing during high speed operation on the DP/DM lines is relatively small (400 mV ± 10%), so any differential noise picked up on the twisted pair can affect the received signal. When the DP/DM traces do not have any shielding, the traces tend to behave like an antenna and picks up noise generated by the surrounding components in the environment. To minimize the effect of this behavior:

- DP/DM traces should always be matched lengths and must be no more than 4 inches in length; otherwise, the eye opening may be degraded (see Figure 8-26).

- Route DP/DM traces close together for noise rejection on differential signals, parallel to each other and within two mils in length of each other. The measurement for trace length must be started from device's balls.
- A high speed USB connection is made through a shielded, twisted pair cable with a differential characteristic impedance of 90 Ω ±15%. In layout, the impedance of DP and DM should each be 45 Ω ± 10%.
- DP/DM traces should not have any extra components to maintain signal integrity. For example, traces cannot be routed to two USB connectors.

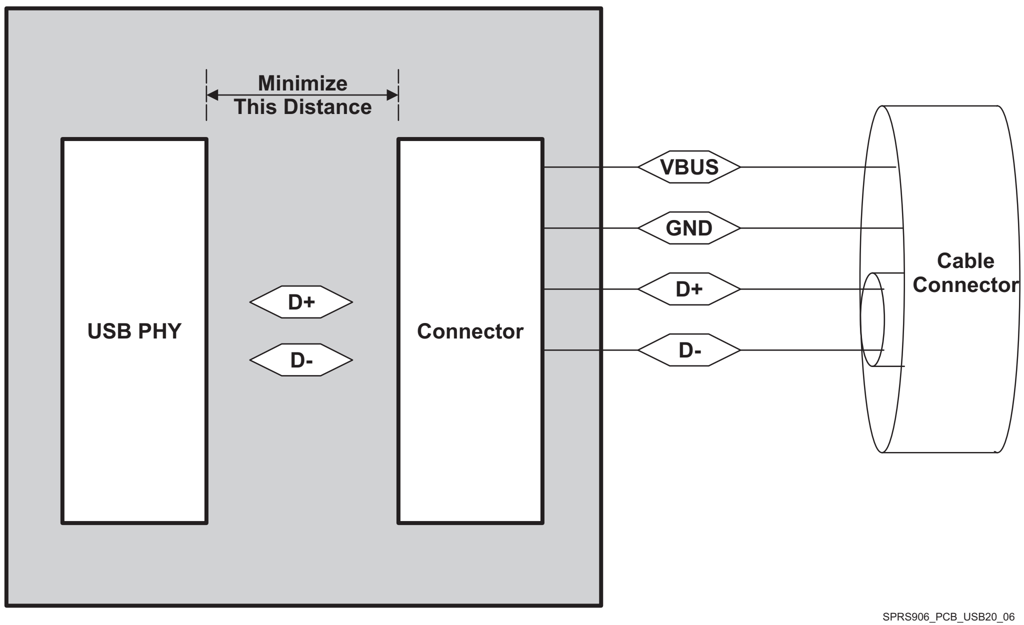


Figure 8-26. USB PHY Connector and Cable Connector

8.5.2.2.2.8 DP/DM Vias

When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points on twisted pair lines; through-hole pins are not recommended.

8.5.2.2.2.9 Image Planes

An image plane is a layer of copper (voltage plane or ground plane), physically adjacent to a signal routing plane. Use of image planes provides a low impedance, shortest possible return path for RF currents. For a USB board, the best image plane is the ground plane because it can be used for both analog and digital circuits.

- Do not route traces so they cross from one plane to the other. This can cause a broken RF return path resulting in an EMI radiating loop as shown in Figure 8-27. This is important for higher frequency or repetitive signals. Therefore, on a multi-layer board, it is best to run all clock signals on the signal plane above a solid ground plane.
- Avoid crossing the image power or ground plane boundaries with high speed clock signal traces immediately above or below the separated planes. This also holds true for the twisted pair signals (DP, DM). Any unused area of the top and bottom signal layers of the PCB can be filled with copper that is connected to the ground plane through vias.

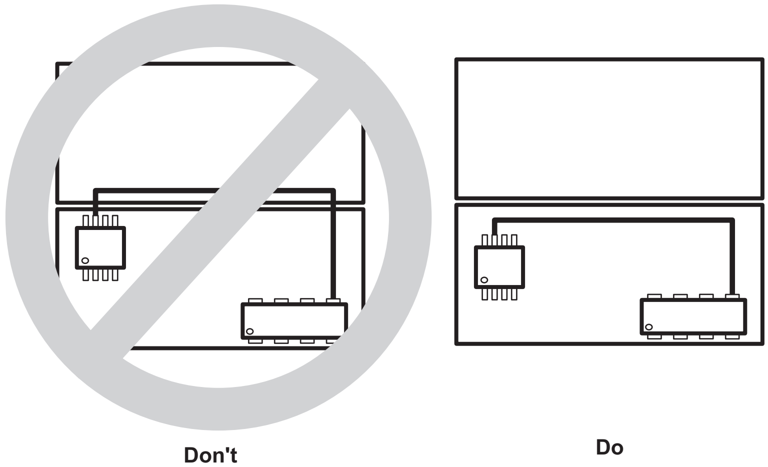


Figure 8-27. Do Not Cross Plane Boundaries

- Do not overlap planes that do not reference each other. For example, do not overlap a digital power plane with an analog power plane as this produces a capacitance between the overlapping areas that could pass RF emissions from one plane to the other, as shown in Figure 8-28.

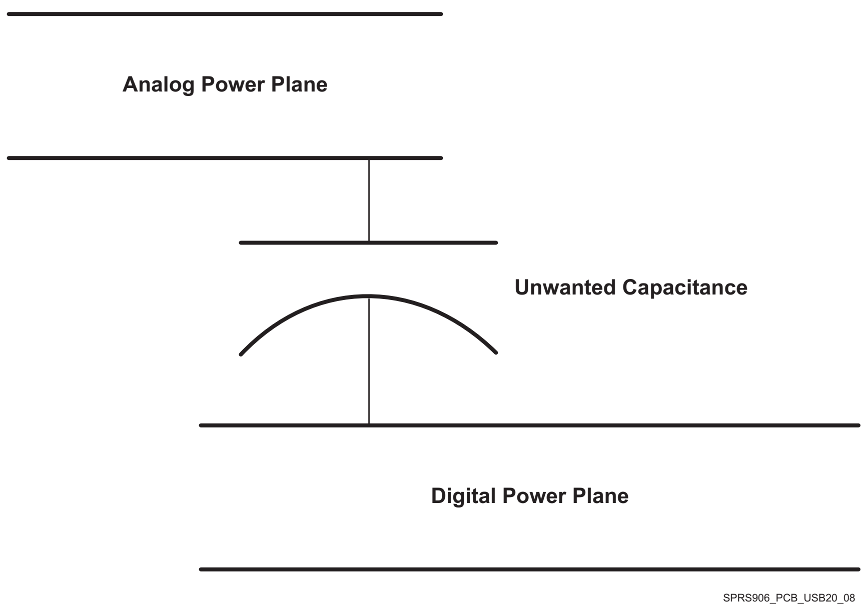


Figure 8-28. Do Not Overlap Planes

- Avoid image plane violations. Traces that route over a slot in an image plane results in a possible RF return loop, as shown in Figure 8-29.

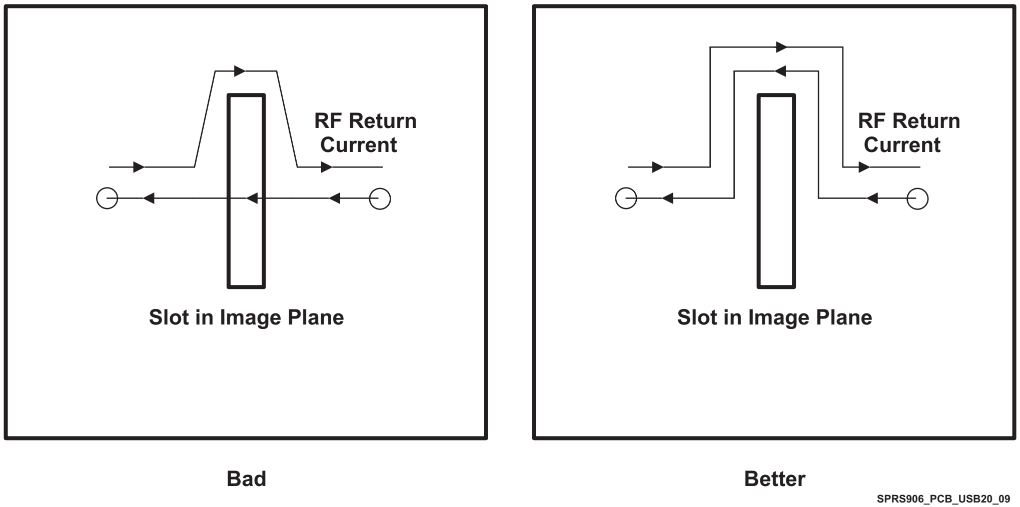


Figure 8-29. Do Not Violate Image Planes

8.5.2.2.2.10 Power Regulators

Switching power regulators are a source of noise and can cause noise coupling if placed close to sensitive areas on a circuit board. Therefore, the switching power regulator should be kept away from the DP/DM signals, the external clock crystal (or clock oscillator), and the USB PHY.

8.5.2.3 References

- USB 2.0 Specification, Intel, 2000
- High Speed USB Platform Design Guidelines, Intel, 2000
- Selection and Specification of Crystals for Texas Instruments USB 2.0 Devices

8.5.3 USB 3.0 Board Design and Layout Guidelines

This section provides the timing specification for the USB3.0 (USB1 in the device) interface as a PCB design and manufacturing specification. The design rules constrain PCB trace length, PCB trace skew, signal integrity, cross-talk, and signal timing. TI has performed the simulation and system design work to ensure the USB3.0 interface requirements are met. The design rules stated within this document are targeted at DEVICE mode electrical compliance. HOST mode and/or systems that do not include the 3m USB cable and far-end 11-inch PCB trace required by DEVICE mode compliance testing may not need the complete list of optimizations shown in this document; however, applying these optimizations to HOST mode systems will lead to optimal DEVICE mode performance.

8.5.3.1 USB 3.0 interface introduction

The USB 3.0 has two unidirectional differential pairs: TXp/TXn pair and RXp/RXn pair. AC coupling caps are needed on the board for TX traces.

Figure 8-30 present high level schematic diagram for USB 3.0 interface.

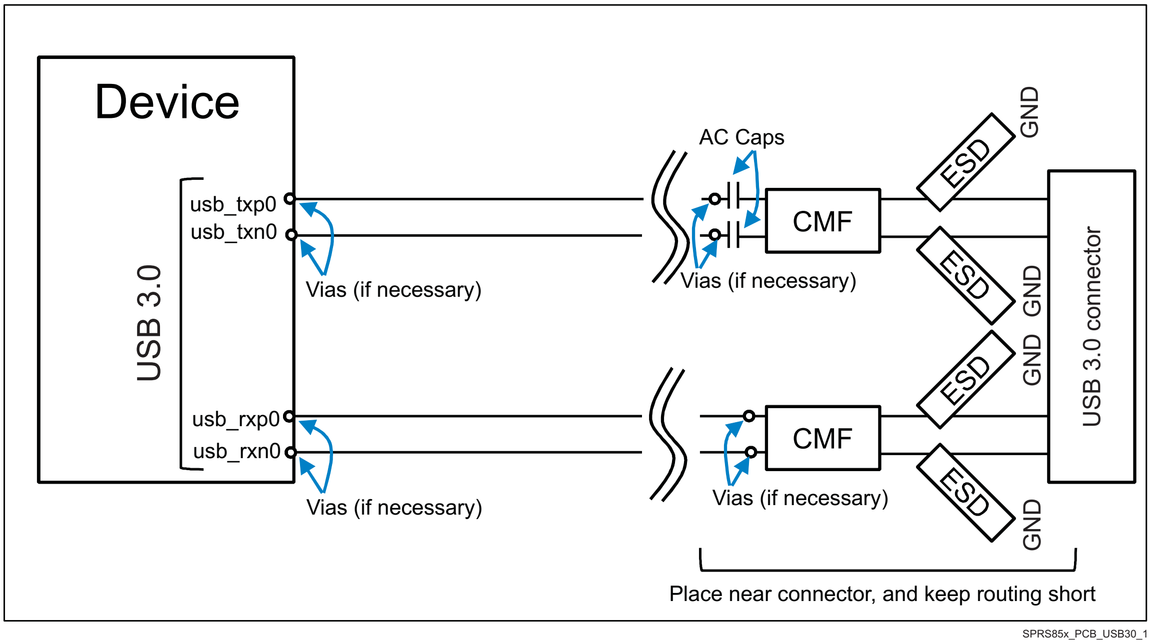


Figure 8-30. USB 3.0 Interface High Level Schematic

NOTE

ESD components should be on a PCB layer next to a system GND plane layer so the inductance of the via to GND will be minimal.

If vias are used, place the vias near the AC Caps or CMFs and under the SoC BGA, if necessary.

Figure 8-31 present placement diagram for USB 3.0 interface.

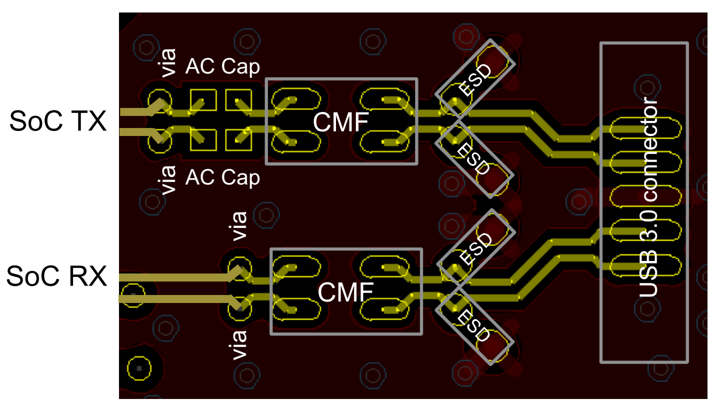


Figure 8-31. USB 3.0 placement diagram

Table 8-9. USB1 Component Reference

INTERFACE	COMPONENT	SUPPLIER	PART NUMBER
USB3 PHY	ESD	TI	TPD1E05U06
	CMF	Murata	DLW21SN900HQ2
	C	-	100nF (typical size: 0201)

8.5.3.2 USB 3.0 General routing rules

Some general routing guidelines regarding USB 3.0:

- Avoid crossing splits reference plane(s).
- Shorter trace length is preferred.
- Minimize the via usage and layer transition
- Keep large spacing between TX and RX pairs.
- Intra-lane delay mismatch between DP and DM less than 1ps. Same for RXp and RXn.
- Distance between common mode filter (CMF) and ESD protection device should be as short as possible
- Distance between ESD protection device and USB connector should be as short as possible.
- Distance between AC capacitors (TX only) and CMF should be as short as possible.
- USB 3.0 signals should always be routed over an adjacent ground plane.

Table 8-10 and Table 8-11 present routing specification and recommendations for USB1 in the device.

Table 8-10. USB1 Routing Specifications

PARAMETER	MIN	TYP	MAX	UNIT
Device balls to USB 3.0 connector trace length			3500	Mils
Skew within a differential pair		3	6	Mils
Number of stubs allowed on TX/RX traces			0	Stubs
TX/RX pair differential impedance	83.7	90	96.3	Ω
Number of vias on each TX/RX trace			2	Vias
Differential pair to any other trace spacing	2xDS	3xDS		
Number of ground plane cuts allowed within USB3 routing region (except for specific ground carving as explained in this document)			0	Cuts
Number of layers between USB3.0 routing region and reference ground plane			0	Layers
PCB trace width		6		Mils
PCB BGA escape via pad size		18		Mils
PCB BGA escape via hole size		10		Mils

1. Vias must be used in pairs and spaced equally along a signal path.
2. DS = differential spacing of the traces.
3. Exceptions may be necessary in the SoC package BGA area.
4. GND guard-bands on the same layer may be closer, but should not be allowed to affect the impedance of the differential pair routing. GND guard-bands to isolate USB3.0 differential pairs from all other signals are recommended.

Table 8-11. USB1 Routing Recommendations

Item	Description	Reason
ESD location	Place ESD component on same layer as connector (no via or stub to ESD component)	Eliminate reflection loss from via & stub to ESD
ESD part number	TPD1E05U06	Minimize capacitance (0.42pF)
CMF part number	DLW21SN900HQ2	Manufacturer's recommended device
Connector	Use USB3.0 connector with supporting s-parameter model	Enable full signal chain simulation
Carve Ground	Carve GND underneath AC Caps, ESD, CMF, and connector	Minimize capacitance under ESD and CMF

Table 8-11. USB1 Routing Recommendations (continued)

Item	Description	Reason
Round pads	Minimize pad size and round the corners of the pads for the ESD and CMF components	Minimize capacitance
Vias	Max 2 vias per signal trace. If vias are required, place vias close to the AC Caps and CMFs. Vias under the SoC grid array may be used if necessary to route signals away from BGA pattern.	Vias significantly degrade signal integrity at 2.5GHz

Figure 8-32 presents an example layout, demonstrating the “carve GND” concept.

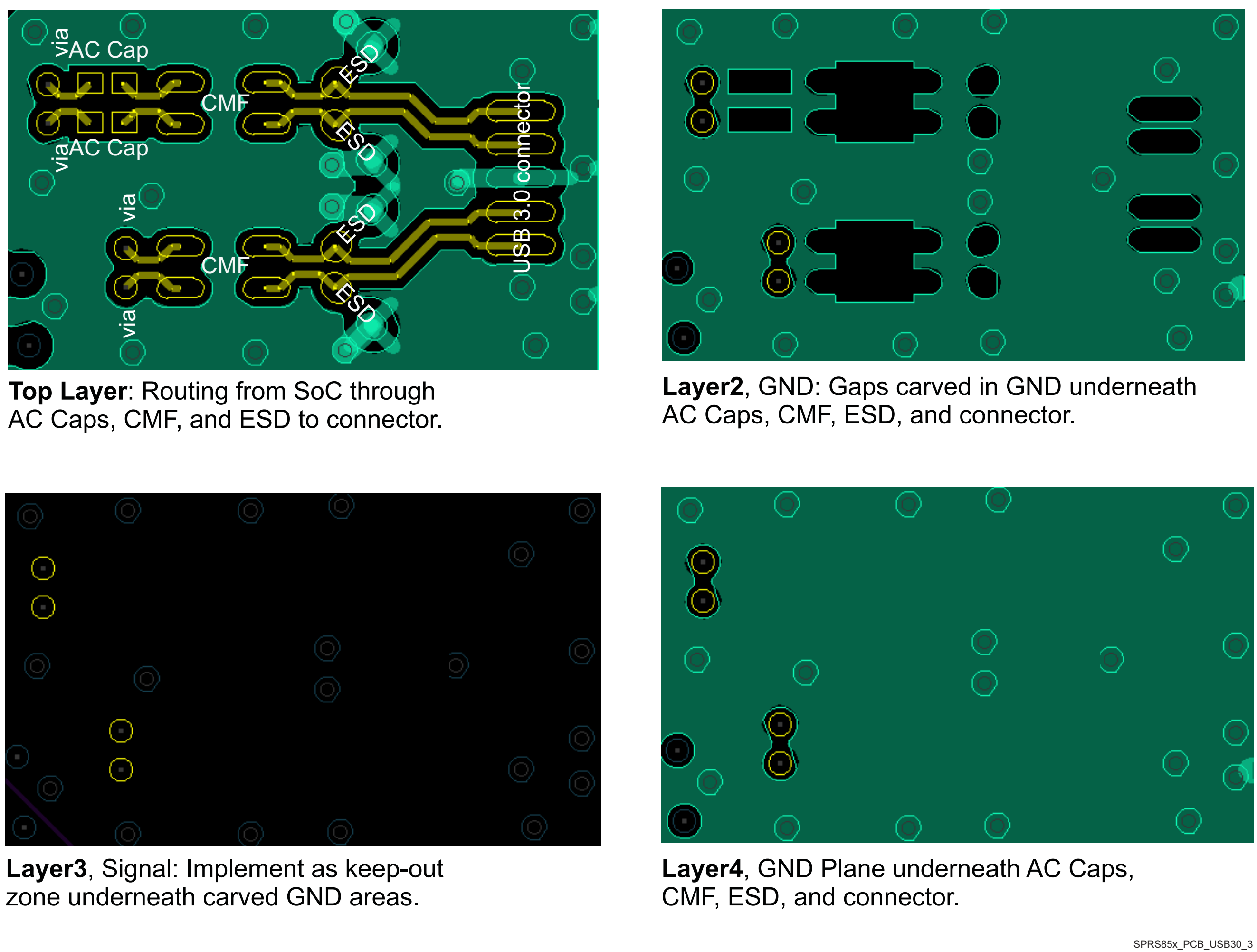


Figure 8-32. USB 3.0 Example “carve GND” layout

8.5.4 HDMI Board Design and Layout Guidelines

This section provides the timing specification for the HDMI interface as a PCB design and manufacturing specification. The design rules constrain PCB trace length, PCB trace skew, signal integrity, cross-talk, and signal timing. TI has performed the simulation and system design work to ensure the HDMI interface requirements are met. The design rules stated within this document are targeted at resolutions less than or equal to 1080p60 with 8-bit color; deep color (10-bit) requires further signal integrity optimization.

8.5.4.1 HDMI Interface Schematic

The HDMI bus is separated into three main sections (HDMI Ethernet and the optional Audio Return Channel are not specifically supported by this Device):

1. Transition Minimized Differential Signaling (TMDS) high speed digital video interface
2. Display Data Channel (I2C bus for configuration and status exchange between two devices)
3. Consumer Electronics Control (optional) for remote control of connected devices.

The DDC and CEC are low speed interfaces, so nothing special is required for PCB layout of these signals.

The TMDS channels are high speed differential pairs and therefore require the most care in layout. Specifications for TMDS layout are below.

Figure 8-33 shows the HDMI interface schematic.

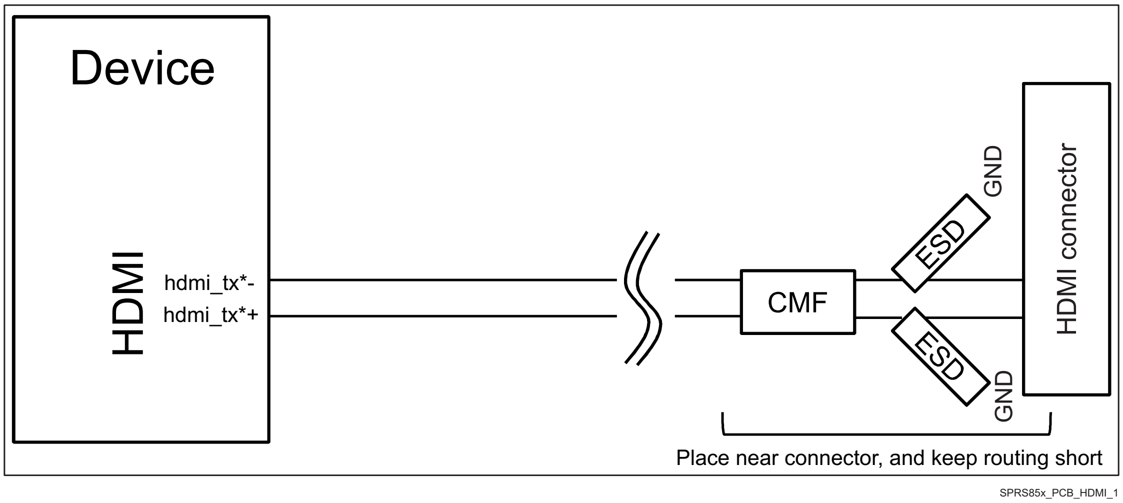


Figure 8-33. HDMI Interface High Level Schematic

Figure 8-34 presents placement diagram for HDMI interface.

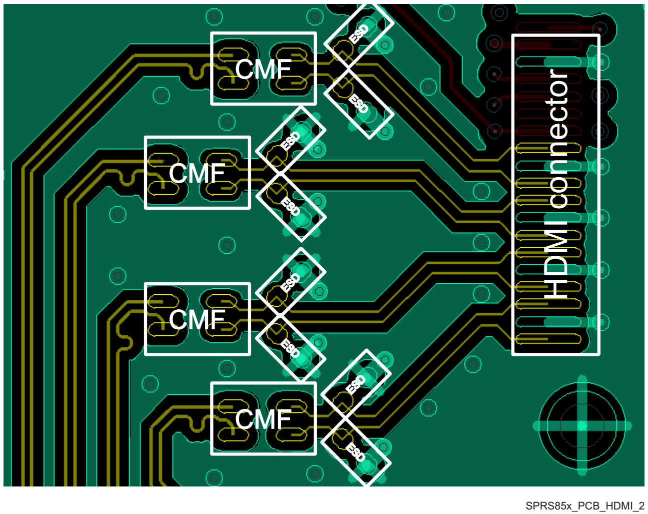


Figure 8-34. HDMI Placement Diagram

Table 8-12. HDMI Component Reference

INTERFACE	DEVICE	SUPPLIER	PART NUMBER
HDMI	ESD	TI	TPD1E05U06
	CMF	Murata	DLW21SN900HQ2

8.5.4.2 TMDS General Routing Guidelines

The TMDS signals are high speed differential pairs. Care must be taken in the PCB layout of these signals to ensure good signal integrity.

The TMDS differential signal traces must be routed to achieve 100 Ohms (+/- 10%) differential impedance and 60 ohms (+/-10%) single ended impedance. Single ended impedance control is required because differential signals can't be closely coupled on PCBs and therefore single ended impedance becomes important.

These impedances are impacted by trace width, trace spacing, distance to reference planes, and dielectric material. Verify with a PCB design tool that the trace geometry for both data signal pairs results in as close to 60 ohms impedance traces as possible. For best accuracy, work with your PCB fabricator to ensure this impedance is met.

In general, closely coupled differential signal traces are not an advantage on PCBs. When differential signals are closely coupled, tight spacing and width control is necessary. Very small width and spacing variations affect impedance dramatically, so tight impedance control can be more problematic to maintain in production.

Loosely coupled PCB differential signals make impedance control much easier. Wider traces and spacing make obstacle avoidance easier, and trace width variations don't affect impedance as much, therefore it's easier to maintain accurate impedance over the length of the signal. The wider traces also show reduced skin effect and therefore often result in better signal integrity.

Some general routing guidelines regarding TMDS:

- Avoid crossing splits reference plane(s).
- Shorter trace length is preferred.
- Distance between common mode filter (CMF) and ESD protection device should be as short as possible
- Distance between ESD protection device and HDMI connector should be as short as possible.

Table 8-13 shows the routing specifications for the TMDS signals.

Table 8-13. TMDS Routing Specifications

PARAMETER	MIN	TYP	MAX	UNIT
Device balls to HDMI header trace length			4000	Mils
Skew within a differential pair		3	5	Mils
Number of stubs allowed on TMDS traces			0	stubs
TMDS pair differential impedance	90	100	110	Ω
TMDS single-ended impedance	54	60	66	Ω
Number of vias on each TMDS trace			0	Vias
TMDS differential pair to any other trace spacing(1) (2) (3)	2×DS	3xDS		Mils
Number of ground plane cuts allowed within HDMI routing region (except for specific ground carving as explained in this document)			0	Cuts
Number of layers between HDMI routing region and reference ground plane			0	Layers
PCB trace width		4.4		Mils

(1) DS = differential spacing of the traces.

(2) Exceptions may be necessary in the SoC package BGA area.

(3) GND guard-bands may be closer, but should not be allowed to affect the impedance of the differential pair routing. GND guard-bands to isolate HDMI differential pairs from all other signals is recommended.

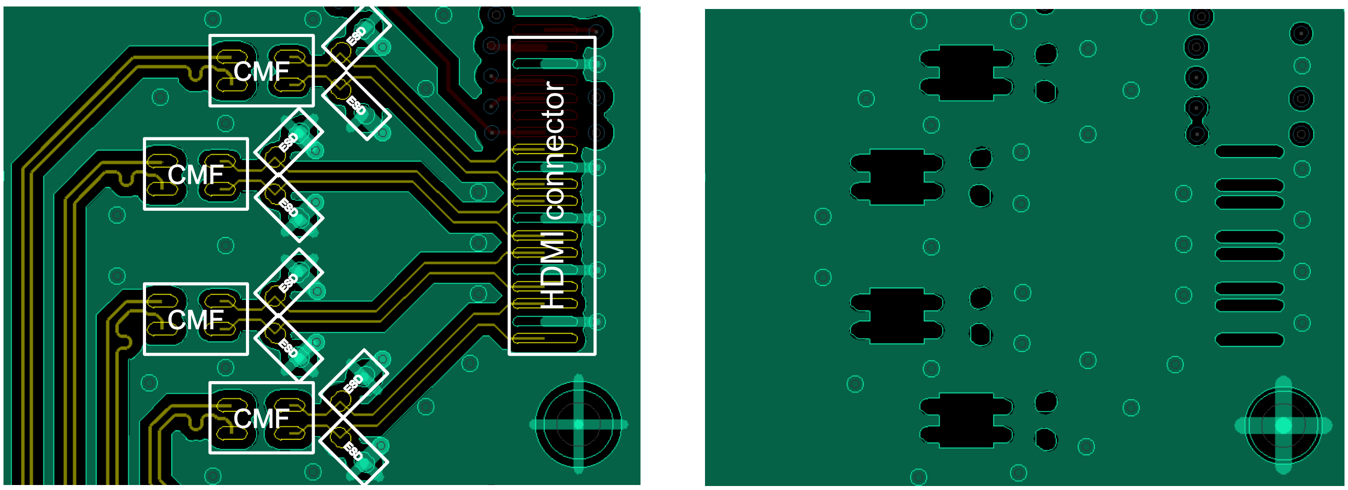
Table 8-14. TDMS Routing Recommendations

Item	Description	Reason
ESD part number	TPD1E05U06	Minimize capacitance (0.42pF)

Table 8-14. TDMS Routing Recommendations (continued)

Item	Description	Reason
Carve Ground	Carve GND underneath ESD and CMF	Minimize capacitance under ESD and CMF
Round pads	Reduce pad size and round the corners of the pads for the ESD and CMF components	Minimize capacitance
Routing layer	Route all signals only on the same layer as SoC	Minimize reflection loss

Figure 8-35presents an example layout, demonstrating the "carve GND" concept.



Top Layer: Routing from SoC through CMF, and ESD to connector.

Layer2, GND: Gaps carved in GND underneath, CMF, ESD, and connector.

SPRS85x_PCB_HDMI_3

Figure 8-35. HDMI Example "carve GND" layout

8.5.4.3 TPD5S115

The TPD5S115 is an integrated HDMI companion chip solution. The device provides a regulated 5 V output (5VOUT) for sourcing the HDMI power line. The TPD5S115 exceeds the IEC61000-4-2 (Level 4) ESD protection level.

8.5.4.4 HDMI ESD Protection Device (Required)

Interfaces that connect to a cable such as HDMI generally require more ESD protection than can be built into the processor's outputs. Therefore this HDMI interface requires the use of an ESD protection chip to provide adequate ESD.

When selecting an ESD protection chip, choose the lowest capacitance ESD protection available to minimize signal degradation. In no case should be ESD protection circuit capacitance be more than 5pF.

TI manufactures these devices that provide ESD protection for HDMI signals such as the TPDxE05U06. For more information see the ti.com website.

8.5.4.5 PCB Stackup Specifications

Table 8-15 shows the stackup and feature sizes required for HDMI.

Table 8-15. HDMI PCB Stackup Specifications

PARAMETER	MIN	TYP	MAX	UNIT
PCB Routing/Plane Layers	4	6	-	Layers

Table 8-15. HDMI PCB Stackup Specifications (continued)

PARAMETER	MIN	TYP	MAX	UNIT
Signal Routing Layers	2	3	-	Layers
Number of ground plane cuts allowed within HDMI routing region	-	-	0	Cuts
Number of layers between HDMI routing region and reference ground plane	-	-	0	Layers
PCB Trace width		4		Mils

8.5.4.6 Grounding

Each TMDS channel has its own shield pin and they should be grounded to provide a return current path for the TMDS signal.

8.5.5 SATA Board Design and Layout Guidelines

The device provides one SATA port. This section provides the timing specification for the SATA interface as a PCB design and manufacturing specification. The design rules constrain PCB trace length, PCB trace skew, signal integrity, cross-talk, and signal timing. TI has performed the simulation and system design work to ensure the SATA interface requirements are met.

8.5.5.1 SATA Interface Schematic

Figure 8-36 shows the data portion of the SATA interface schematic.

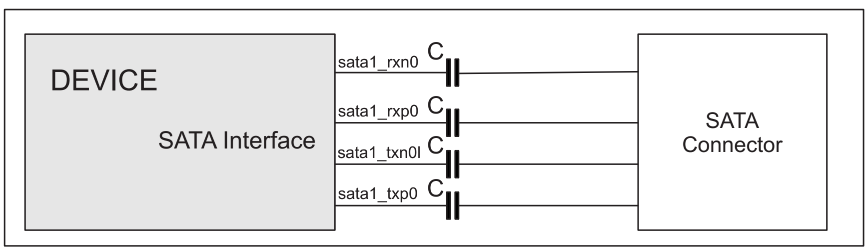


Figure 8-36. SATA Interface High Level Schematic

NOTE

AC coupling capacitors (C) are required on the receive and transmit data pairs. Table 8-16 shows the requirements for these capacitors.

Table 8-16. SATA AC Coupling Capacitors Requirements

PARAMETER	MIN	TYP	MAX	UNIT
SATA AC coupling capacitor value	0.3	10	12	nF
SATA AC coupling capacitor package size		0402	0603	EIA(1)(2)

(1) EIA L×W units, that is, a 0402 is a 40×20 mils surface mount capacitor.

(2) The physical size of the capacitor should be as small as practical. Use the same size on both lines in each pair placed side by side.

8.5.5.2 Compatible SATA Components and Modes

Table 8-17 shows the compatible SATA components and supported modes. Note that the only supported configuration is an internal cable from the processor host to the SATA device.

Table 8-17. Compatible SATA Components and Modes

PARAMETER	MIN	MAX	UNIT	SUPPORTED
Transfer Rates	1.5	3	Gbps	

Table 8-17. Compatible SATA Components and Modes (continued)

PARAMETER	MIN	MAX	UNIT	SUPPORTED
Internal Cable	-	-	-	YES

8.5.5.3 PCB Stackup Specifications

Table 8-18 shows the stackup and feature sizes required for these types of SATA connections.

Table 8-18. SATA PCB Stackup Specifications

PARAMETER	MIN	TYP	MAX	UNIT
Number of ground plane cuts allowed within SATA routing region	-	-	0	Cuts
Number of layers between SATA routing area and reference plane	-	-	0	Layers
PCB Routing clearance		4		Mils
PCB Trace width		4		Mils

8.5.5.4 Routing Specifications

The SATA data signal traces must be routed to achieve 100 Ohms (+/-10%) differential impedance and 60 ohms (+/-10%) single ended impedance. The signal ended impedance is required because differential signals can't be closely coupled on PCBs and therefore single ended impedance becomes important. 60 ohms is chosen for the single ended impedance to minimize problems caused by too low an impedance.

These impedances are impacted by trace width, trace spacing, distance to reference planes, and dielectric material. Verify with a PCB design tool that the trace geometry for both data signal pairs results in as close to 100 ohms differential and 60 ohms single ended impedance traces as possible. For best accuracy, work with your PCB fabricator to ensure this impedance is met.

Table 8-19 shows the routing specifications for the SATA data signals.

Table 8-19. SATA Routing Specifications

PARAMETER	MIN	TYP	MAX	UNIT
SATA signal trace length (device balls to SATA connector)			3050[1]	Mils
Differential pair trace skew matching			5	Mils
Number of stubs allowed on SATA traces[2]			0	stubs
TX/RX pair differential impedance	90	100	110	Ω
TX/RX single-ended impedance	54	60	66	Ω
Number of vias on each SATA trace			0	Vias
SATA differential pair to any other trace spacing	2×DS[3]			

(1) Beyond this, signal integrity may suffer.

(2) Inline pads may be used for probing.

(3) DS = differential spacing of the SATA traces.

Table 8-20. SATA Routing Recommendations

Item	Description	Reason
ESD part number	None	ESD suppression generally not used on SATA

8.5.6 PCIe Board Design and Layout Guidelines

The PCIe interface on the device provides support for a 5.0 Gbps lane with polarity inversion.

8.5.6.1 PCIe Connections and Interface Compliance

The PCIe interface on the device is compliant with the PCIe revision 3.0 specification. Please refer to the PCIe specifications for all connections that are described in it. Those recommendations are more descriptive and exhaustive than what is possible here.

The use of PCIe compatible bridges and switches is allowed for interfacing with more than one other processor or PCIe device.

8.5.6.1.1 Coupling Capacitors

AC coupling capacitors are required on the transmit data pair. Table 8-21 shows the requirements for these capacitors.

Table 8-21. PCIe AC Coupling Capacitors Requirements

PARAMETER	MIN	TYP	MAX	UNIT
PCIe AC coupling capacitor value	90	100	110	nF
PCIe AC coupling capacitor package size		0402	0603	EIA(1)(2)

(1) EIA L×W units, that is, a 0402 is a 40×20 mils surface mount capacitor.

(2) The physical size of the capacitor should be as small as practical. Use the same size on both lines in each pair placed side by side.

8.5.6.1.2 Polarity Inversion

The PCIe specification requires polarity inversion support. This means for layout purposes, polarity is unimportant because each signal can change its polarity on die inside the chip. This means polarity within a lane is unimportant for layout.

8.5.6.2 Non-standard PCIe connections

The following sections contain suggestions for any PCIe connection that is NOT described in the official PCIe specification, such as an on-board Device to Device or Device to other PCIe compliant processor connection.

8.5.6.2.1 PCB Stackup Specifications

Table 8-22 shows the stackup and feature sizes required for these types of PCIe connections.

Table 8-22. PCIe PCB Stackup Specifications

PARAMETER	MIN	TYP	MAX	UNIT
Number of ground plane cuts allowed within PCIe routing region	-	-	0	Cuts
Number of layers between PCIe routing area and reference plane (1)	-	-	0	Layers
PCB Routing clearance		4		Mils
PCB Trace width		4		Mils

(1) A reference plane may be a ground plane or the power plane referencing the PCIe signals.

8.5.6.2.2 Routing Specifications

8.5.6.2.2.1 Impedance

The PCIe data signal traces must be routed to achieve 100-Ω (±10%) differential impedance and 60-Ω (±10%) single-ended impedance. The single-ended impedance is required because differential signals are extremely difficult to closely couple on PCBs and, therefore, single-ended impedance becomes important. These requirements are the same as those recommended in the PCIe Motherboard Checklist 1.0 document, available from PCI-SIG (www.pcisig.com).

These impedances are impacted by trace width, trace spacing, distance between signals and referencing planes, and dielectric material. Verify with a PCB design tool that the trace geometry for both data signal pairs result in as close to 100-Ω differential impedance and 60-Ω single-ended impedance as possible. For best accuracy, work with your PCB fabricator to ensure this impedance is met. See Table 8-23 below.

8.5.6.2.2.2 Differential Coupling

In general, closely coupled differential signal traces are not an advantage on PCBs. When differential signals are closely coupled, tight spacing and width control is necessary. Very small width and spacing variations affect impedance dramatically, so tight impedance control can be more problematic to maintain in production. For PCBs with very tight space limitations (which are usually small) this can work, but for most PCBs, the loosely coupled option is probably best.

Loosely coupled PCB differential signals make impedance control much easier. Wider traces and spacing make obstacle avoidance easier (because each trace is not so fixed in position relative to the other), and trace width variations don’t affect impedance as much, therefore it’s easier to maintain an accurate impedance over the length of the signal. For longer routes, the wider traces also show reduced skin effect and therefore often result in better signal integrity with a larger eye diagram opening.

Table 8-23 shows the routing specifications for the PCIe data signals.

Table 8-23. PCI-E Routing Specifications

PARAMETER	MIN	TYP	MAX	UNIT
PCIe signal trace length (device balls to PCIe connector)			4700[1]	Mils
Differential pair trace matching			5[2]	Mils
Number of stubs allowed on PCIe traces[3]			0	stubs
TX/RX pair differential impedance	90	100	110	Ω
TX/RX single-ended impedance	54	60	66	Ω
Pad size of vias on PCIe trace			25[4]	Mils
Hole size of vias on PCIe trace			14	Mils
Number of vias on each PCIe trace			0	Vias
PCIe differential pair to any other trace spacing	2×DS[5]			

(1) Beyond this, signal integrity may suffer.
(2) For example, RXP0 within 5 Mils of RXN0.
(3) Inline pads may be used for probing.
(4) 35-Mil antipad maximum recommended.
(5) DS = differential spacing of the PCIe traces.

Table 8-24. PCI-E Routing Recommendations

Item	Description	Reason
ESD part number	None	ESD suppression generally not used on PCIe

8.5.6.2.2.3 *Pair Length Matching*

Each signal in the differential pair should be matched to within 5 mils of its matching differential signal. Length matching should be done as close to the mismatch as possible.

8.5.6.3 LJCB_REFN/P Connections

A Common Refclk Rx Architecture is required to be used for the device PCIe interface. Specifically, two modes of Common Refclk Rx Architecture are supported:

- **External REFCLK Mode**: An common external 100MHz clock source is distributed to both the Device and the link partner
- **Output REFCLK Mode**: A 100MHz HCSL clock source is output by the device and used by the link partner

In **External REFCLK Mode**, a high-quality, low-jitter, differential HCSL 100MHz clock source compliant to the PCIe REFCLK AC Specifications should be provided on the Device's ljcb_clkn / ljcb_clkp inputs. Alternatively, an LVDS clock source can be used with the following additional requirements:

- External AC coupling capacitors described in Table 8-25 should be populated at the ljcb_clkn / ljcb_clkp inputs.
- All termination requirements (ex. parallel 100Ω termination) from the clock source manufacturer should be followed.

In **Output REFCLK Mode**, the 100MHz clock from the Device's DPLL_PCIE_REF should be output on the Device's ljcb_clkn / ljcb_clkp pins and used as the HCSL REFCLK by the link partner. External near-side termination to ground described in Table 8-26 is required on both of the ljcb_clkn / ljcb_clkp outputs in this mode.

Table 8-25. LJCB_REFN/P Requirements in External LVDS REFCLK Mode

PARAMETER	MIN	TYP	MAX	UNIT
ljcb_clkn / ljcb_clkp AC coupling capacitor value		100		nF
ljcb_clkn / ljcb_clkp AC coupling capacitor package size		0402	0603	EIA(1)(2)

(1) EIA L×W units, that is, a 0402 is a 40×20 mils surface mount capacitor.

(2) The physical size of the capacitor should be as small as practical. Use the same size on both lines in each pair placed side by side.

Table 8-26. LJCB_REFN/P Requirements in Output REFCLK Mode

PARAMETER	MIN	TYP	MAX	UNIT
ljcb_clkn / ljcb_clkp near-side termination to ground value	47.5	50	52.5	Ω

8.5.7 *CSI2 Board Design and Routing Guidelines*

The MIPI D-PHY signals include the CSI2_0 and CSI2_1 camera serial interfaces to or from the Device.

For more information regarding the MIPI-PHY signals and corresponding balls, see Table 4-7, *CSI2 Signal Descriptions*.

For more information, you can also see the MIPI D-PHY specification v1-01-00_r0-03 (specifically the Interconnect and Lane Configuration and Annex B Interconnect Design Guidelines chapters).

In the next section, the PCB guidelines of the following differential interfaces are presented:

- CSI2_0 and CSI2_1 MIPI CSI-2 at 1.5 Gbps

Table 8-27 lists the MIPI D-PHY interface signals in the Device.

Table 8-27. MIPI D-PHY Interface Signals in the Device

SIGNAL NAME	BOTTOM BALL	SIGNAL NAME	BOTTOM BALL
csi2_0_dx0	AE1	csi2_0_dy0	AD2

Table 8-27. MIPI D-PHY Interface Signals in the Device (continued)

SIGNAL NAME	BOTTOM BALL	SIGNAL NAME	BOTTOM BALL
csi2_0_dx1	AF1	csi2_0_dy1	AE2
csi2_0_dx2	AF2	csi2_0_dy2	AF3
csi2_0_dx3	AH4	csi2_0_dy3	AG4
csi2_0_dx4	AH3	csi2_0_dy4	AG3
csi2_1_dx0	AG5	csi2_1_dy0	AH5
csi2_1_dx1	AG6	csi2_1_dy1	AH6
csi2_1_dx2	AH7	csi2_1_dy2	AG7

8.5.7.1 CSI2_0 and CSI2_1 MIPI CSI-2 (1.5 Gbps)

8.5.7.1.1 General Guidelines

The general guidelines for the PCB differential lines are:

- Differential trace impedance Z_0 = 100 Ω (minimum = 85 Ω, maximum = 115 Ω)
- Total conductor length from the Device package pins to the peripheral device package pins is 25 to 30 cm with common FR4 PCB and flex materials.

NOTE

Longer interconnect length can be supported at the expense of detailed simulations of the complete link including driver and receiver models.

The general rule of thumb for the space S = 2 × W is not designated (see Figure 8-19, *Guard Illustration*). It is because although the S = 2 × W rule is a good rule of thumb, it is not always the best solution. The electrical performance will be checked with the frequency-domain specification. Even though the designer does not follow the S = 2 × W rule, the differential lines are ok if the lines satisfy the frequency-domain specification.

Because the MIPI signals are used for low-power, single-ended signaling in addition to their high speed differential implementation, the pairs must be loosely coupled.

8.5.7.1.2 Length Mismatch Guidelines

8.5.7.1.2.1 CSI2_0 and CSI2_1 MIPI CSI-2 (1.5 Gbps)

The guidelines of the length mismatch for CSI-2 are presented in Table 8-28.

Table 8-28. Length Mismatch Guidelines for CSI-2 (1.5 Gbps)

PARAMETER	TYPICAL VALUE	UNIT
Operating speed	1500	Mbps
UI (bit time)	667	ps
Intralane skew	Have to satisfy mode-conversion S parameters(1)	
Interlane skew (UI / 50)	13.34	ps
PCB lane-to-lane skew (0.1 UI)	66.7	ps

(1) sdc12, scd21, scd12, sdc21, scd11, sdc11, scd22, and sdc22

8.5.7.1.3 Frequency-domain Specification Guidelines

After the PCB design is finished, the S-parameters of the PCB differential lines will be extracted with a 3D Maxwell Equation Solver such as the high-frequency structure simulator (HFSS) or equivalent, and compared to the frequency-domain specification as defined in the section 7 of the MIPI Alliance Specification for D-PHY Version v1-01-00_r0-03.

If the PCB lines satisfy the frequency-domain specification, the design is finished. Otherwise, the design needs to be improved.

8.6 Clock Routing Guidelines

8.6.1 32-kHz Oscillator Routing

When designing the printed-circuit board:

- Keep the crystal as close as possible to the crystal pins X1 and X2.
- Keep the trace lengths short and small to reduce capacitor loading and prevent unwanted noise pickup.
- Place a guard ring around the crystal and tie the ring to ground to help isolate the crystal from unwanted noise pickup.
- Keep all signals out from beneath the crystal and the X1 and X2 pins to prevent noise coupling.
- Finally, an additional local ground plane on an adjacent PCB layer can be added under the crystal to shield it from unwanted pickup from traces on other layers of the board. This plane must be isolated from the regular PCB ground plane and tied to the GND pin of the RTC. The plane must not be any larger than the perimeter of the guard ring. Make sure that this ground plane does not contribute to significant capacitance (a few pF) between the signal line and ground on the connections that run from X1 and X2 to the crystal.

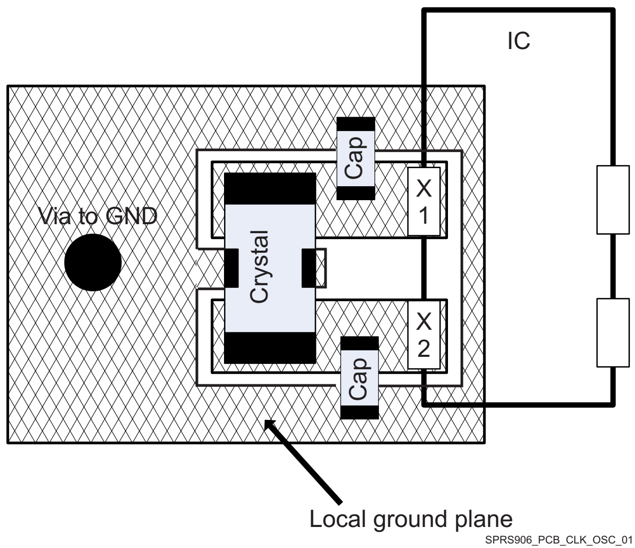


Figure 8-37. Slow Clock PCB Requirements

8.6.2 Oscillator Ground Connection

Although the impedance of a ground plane is low it is, of course, not zero. Therefore, any noise current in the ground plane causes a voltage drop in the ground. Figure 8-38 shows the grounding scheme for slow (low frequency) clock generated from the internal oscillator.

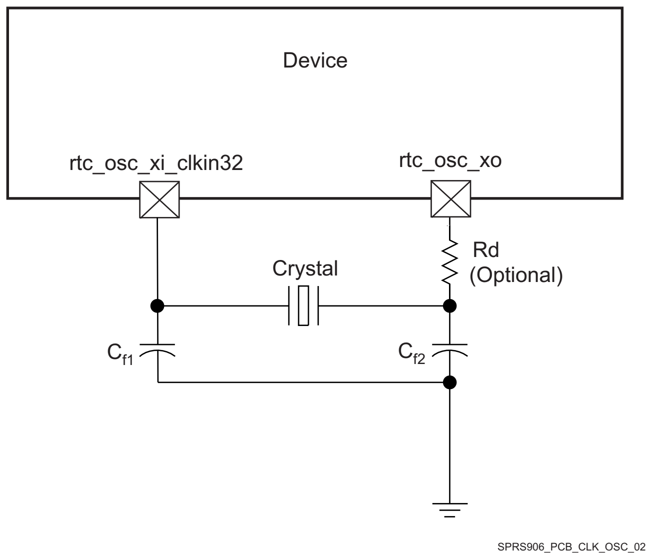
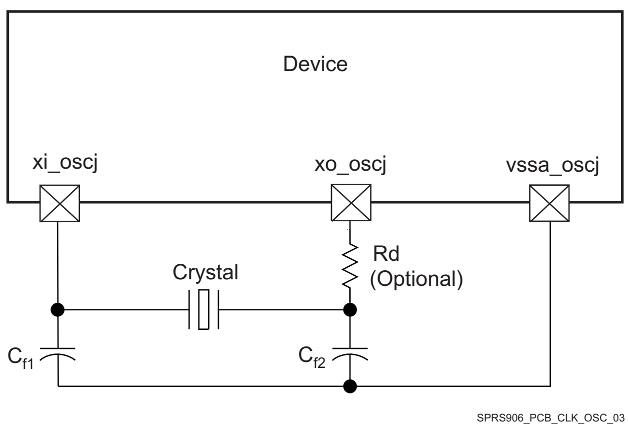


Figure 8-38. Grounding Scheme for Low-Frequency Clock

Figure 8-39 shows the grounding scheme for high-frequency clock.



(1) j in *_osc = 0 or 1

Figure 8-39. Grounding Scheme for High-Frequency Clock

8.7 DDR3 Board Design and Layout Guidelines

8.7.1 DDR3 General Board Layout Guidelines

To help ensure good signaling performance, consider the following board design guidelines:

- Avoid crossing splits in the power plane.
- Minimize Vref noise.
- Use the widest trace that is practical between decoupling capacitors and memory module.
- Maintain a single reference.
- Minimize ISI by keeping impedances matched.
- Minimize crosstalk by isolating sensitive bits, such as strobes, and avoiding return path discontinuities.
- Use proper low-pass filtering on the Vref pins.
- Keep the stub length as short as possible.
- Add additional spacing for on-clock and strobe nets to eliminate crosstalk.
- Maintain a common ground reference for all bypass and decoupling capacitors.

- Take into account the differences in propagation delays between microstrip and stripline nets when evaluating timing constraints.

8.7.2 DDR3 Board Design and Layout Guidelines

8.7.2.1 Board Designs

TI only supports board designs using DDR3 memory that follow the guidelines in this document. The switching characteristics and timing diagram for the DDR3 memory controller are shown in Table 8-29 and Figure 8-40.

Table 8-29. Switching Characteristics Over Recommended Operating Conditions for DDR3 Memory Controller

NO.	PARAMETER		MIN	MAX	UNIT
1	$t_{c(DDR\_CLK)}$	Cycle time, DDR_CLK	1.5	2.5(1)	ns

(1) This is the absolute maximum the clock period can be. Actual maximum clock period may be limited by DDR3 speed grade and operating frequency (see the DDR3 memory device data sheet).

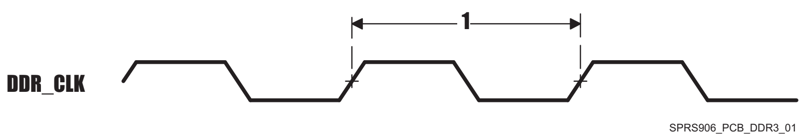


Figure 8-40. DDR3 Memory Controller Clock Timing

8.7.2.2 DDR3 EMIF

The processor contains one DDR3 EMIF.

8.7.2.3 DDR3 Device Combinations

Because there are several possible combinations of device counts and single- or dual-side mounting, Table 8-30 summarizes the supported device configurations.

Table 8-30. Supported DDR3 Device Combinations

NUMBER OF DDR3 DEVICES	DDR3 DATA DEVICE WIDTH (BITS)	MIRRORED?	DDR3 EMIF WIDTH (BITS)
1	16	N	16
2	8	Y(1)	16
2	16	N	32
2	16	Y(1)	32
3	16	N(3)(4)	32
4	8	N	32
4	8	Y(2)	32
5	8	N(3)(4)	32

(1) Two DDR3 devices are mirrored when one device is placed on the top of the board and the second device is placed on the bottom of the board.

(2) This is two mirrored pairs of DDR3 devices.

(3) Three or five DDR3 device combination is not available on this device, but combination types are retained for consistency with the TDA2xx family of devices.

(4) The DDR memory connected to the DDR ECC bus does NOT need to be the same part number as the DDR memories connected to the DDR data bus. However, some constraints do apply. When selecting a memory for the DDR ECC bus, the following restrictions must be adhered to as compared to the DDR memories on the data bus:

- Match the same DDR3 speed grade
- Have an equal number of internal banks
- Have an equal number of columns
- Have a greater or equal number of rows

8.7.2.4 DDR3 Interface Schematic

8.7.2.4.1 32-Bit DDR3 Interface

The DDR3 interface schematic varies, depending upon the width of the DDR3 devices used and the width of the bus used (16 or 32 bits). General connectivity is straightforward and very similar. 16-bit DDR devices look like two 8-bit devices. Figure 8-41 and Figure 8-42 show the schematic connections for 32-bit interfaces using x16 devices.

8.7.2.4.2 16-Bit DDR3 Interface

Note that the 16-bit wide interface schematic is practically identical to the 32-bit interface (see Figure 8-41 and Figure 8-42); only the high-word DDR memories are removed and the unused DQS inputs are tied off.

When not using all or part of a DDR interface, the proper method of handling the unused pins is to tie off the ddr1_dqs*i* pins to ground via a 1k-Ω resistor and to tie off the ddr1_dqsn*i* pins to the corresponding vdds_ddr*x* supply via a 1k-Ω resistor. This needs to be done for each byte not used. Although these signals have internal pullups and pulldowns, external pullups and pulldowns provide additional protection against external electrical noise causing activity on the signals.

The vdds_ddr*x* and ddr1_vref0 power supply pins need to be connected to their respective power supplies even if ddrx is not being used. All other DDR interface pins can be left unconnected. Note that the supported modes for use of the DDR EMIF are 32-bits wide, 16-bits wide, or not used.

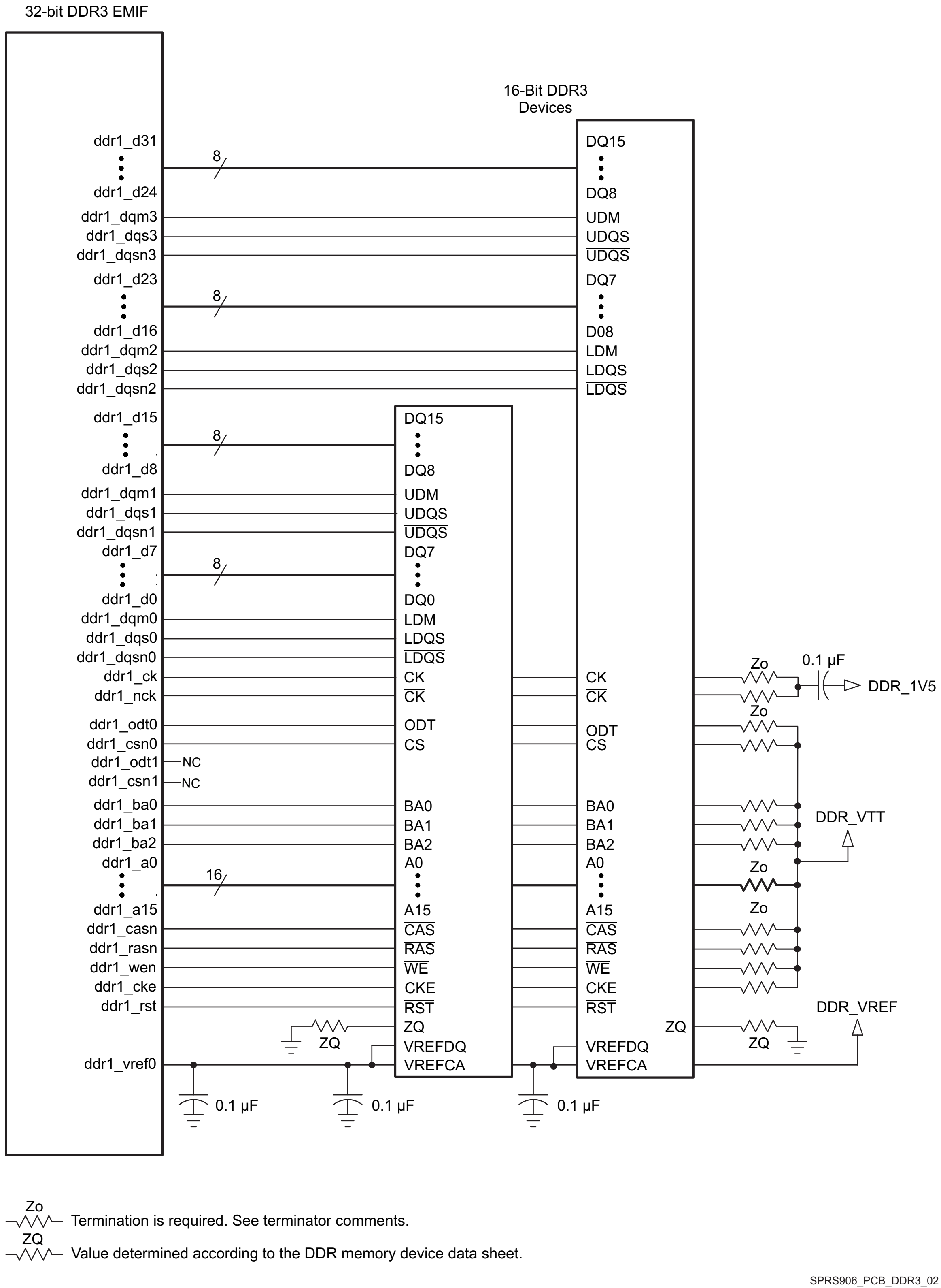


Figure 8-41. 32-Bit, One-Bank DDR3 Interface Schematic Using Two 16-Bit DDR3 Devices

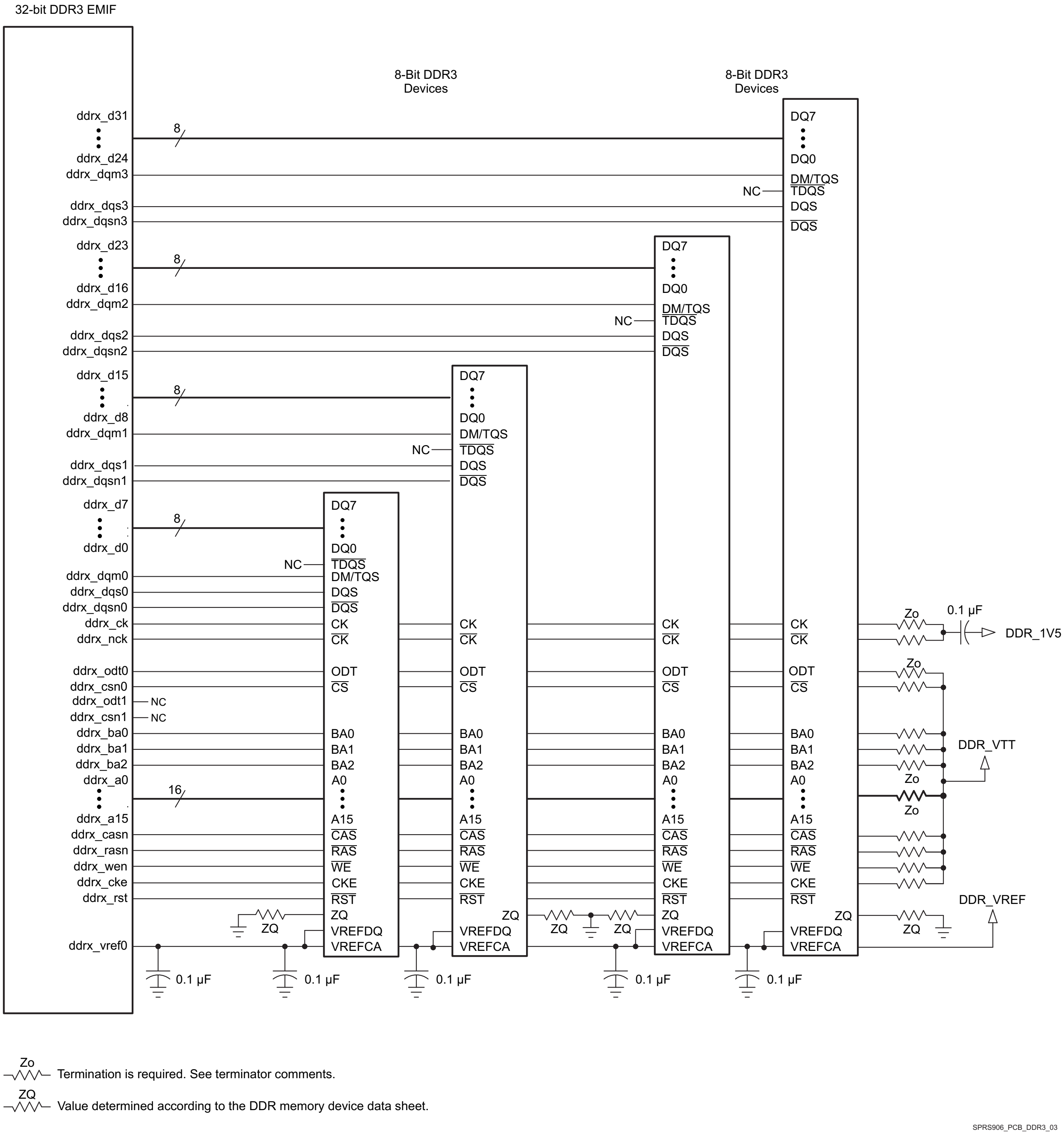


Figure 8-42. 32-Bit, One-Bank DDR3 Interface Schematic Using Four 8-Bit DDR3 Devices

8.7.2.5 Compatible JEDEC DDR3 Devices

Table 8-31 shows the parameters of the JEDEC DDR3 devices that are compatible with this interface. Generally, the DDR3 interface is compatible with DDR3-1333 devices in the x8 or x16 widths.

Table 8-31. Compatible JEDEC DDR3 Devices (Per Interface)

NO.	PARAMETER	CONDITION	MIN	MAX	UNIT
1	JEDEC DDR3 device speed grade(1)	DDR clock rate = 400MHz	DDR3-800	DDR3-1600	
		400MHz< DDR clock rate ≤ 533MHz	DDR3-1066	DDR3-1600	
		533MHz< DDR clock rate ≤ 667MHz	DDR3-1333	DDR3-1600	
2	JEDEC DDR3 device bit width		x8	x16	Bits
3	JEDEC DDR3 device count(2)		2	4	Devices

(1) Refer to Table 8-29 Switching Characteristics Over Recommended Operating Conditions for DDR3 Memory Controller for the range of supported DDR clock rates.

(2) For valid DDR3 device configurations and device counts, see Section 8.7.2.4, Figure 8-41, and Figure 8-42.

8.7.2.6 PCB Stackup

The minimum stackup for routing the DDR3 interface is a six-layer stack up as shown in Table 8-32. Additional layers may be added to the PCB stackup to accommodate other circuitry, enhance SI/EMI performance, or to reduce the size of the PCB footprint. Complete stackup specifications are provided in Table 8-33.

Table 8-32. Six-Layer PCB Stackup Suggestion

LAYER	TYPE	DESCRIPTION
1	Signal	Top routing mostly vertical
2	Plane	Ground
3	Plane	Split power plane
4	Plane	Split power plane or Internal routing
5	Plane	Ground
6	Signal	Bottom routing mostly horizontal

Table 8-33. PCB Stackup Specifications

NO.	PARAMETER	MIN	TYP	MAX	UNIT
PS1	PCB routing/plane layers	6			
PS2	Signal routing layers	3			
PS3	Full ground reference layers under DDR3 routing region(1)	1			
PS4	Full 1.5-V power reference layers under the DDR3 routing region(1)	1			
PS5	Number of reference plane cuts allowed within DDR routing region(2)			0	
PS6	Number of layers between DDR3 routing layer and reference plane(3)			0	
PS7	PCB routing feature size		4		Mils
PS8	PCB trace width, w		4		Mils
PS9	Single-ended impedance, Zo	50		75	Ω
PS10	Impedance control(5)	Z-5	Z	Z+5	Ω

(1) Ground reference layers are preferred over power reference layers. Be sure to include bypass caps to accommodate reference layer return current as the trace routes switch routing layers.
(2) No traces should cross reference plane cuts within the DDR routing region. High speed signal traces crossing reference plane cuts create large return current paths which can lead to excessive crosstalk and EMI radiation.
(3) Reference planes are to be directly adjacent to the signal plane to minimize the size of the return current loop.
(4) An 18-mil pad assumes Via Channel is the most economical BGA escape. A 20-mil pad may be used if additional layers are available for power routing. An 18-mil pad is required for minimum layer count escape.
(5) Z is the nominal singled-ended impedance selected for the PCB specified by PS9.

8.7.2.7 Placement

Figure 8-43 shows the required placement for the processor as well as the DDR3 devices. The dimensions for this figure are defined in Table 8-34. The placement does not restrict the side of the PCB on which the devices are mounted. The ultimate purpose of the placement is to limit the maximum trace lengths and allow for proper routing space. For a 16-bit DDR memory system, the high-word DDR3 devices are omitted from the placement.

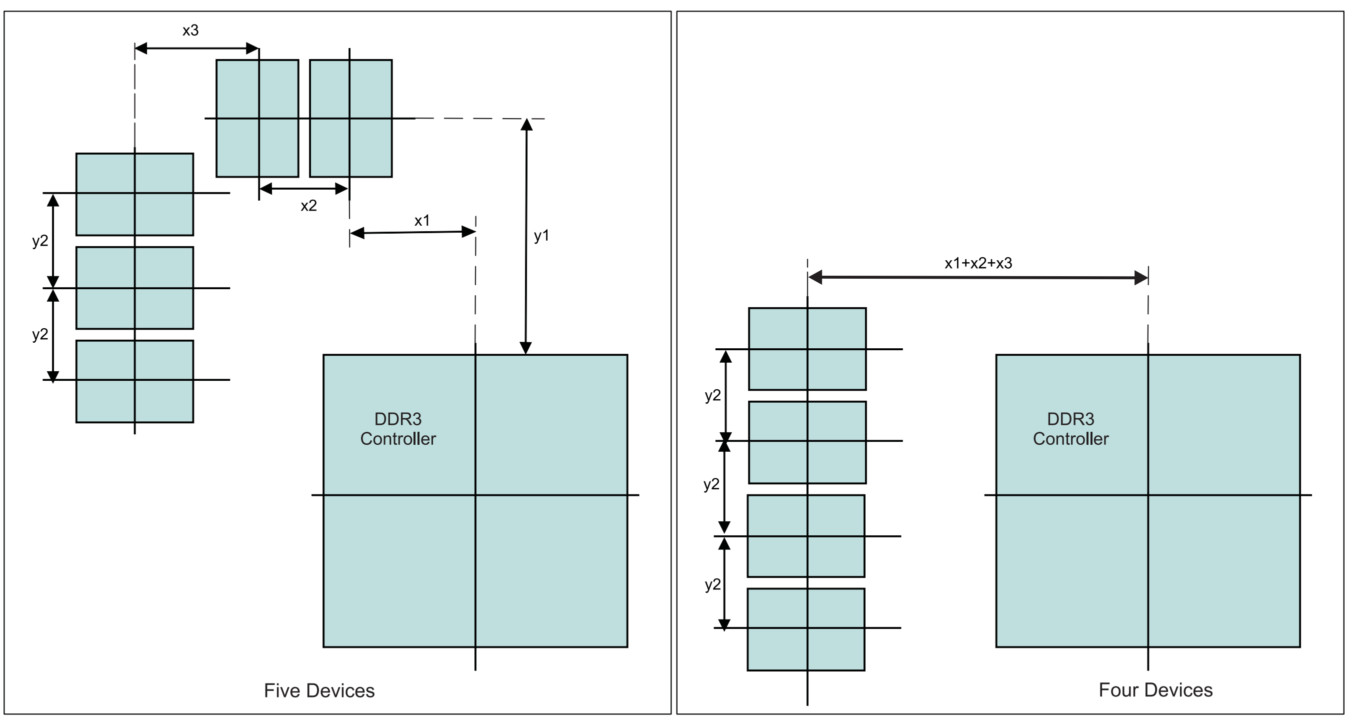


Figure 8-43. Placement Specifications

Table 8-34. Placement Specifications DDR3

NO.	PARAMETER	MIN	MAX	UNIT
KOD31	X1		500	Mils
KOD32	X2		600	Mils
KOD33	X3		600	Mils
KOD34	Y1		1800	Mils
KOD35	Y2		600	Mils
KOD36	DDR3 keepout region (1)			
KOD37	Clearance from non-DDR3 signal to DDR3 keepout region (2) (3)	4		W

(1) DDR3 keepout region to encompass entire DDR3 routing area.

(2) Non-DDR3 signals allowed within DDR3 keepout region provided they are separated from DDR3 routing layers by a ground plane.

(3) If a device has more than one DDR controller, the signals from the other controller(s) are considered non-DDR3 and should be separated by this specification.

8.7.2.8 DDR3 Keepout Region

The region of the PCB used for DDR3 circuitry must be isolated from other signals. The DDR3 keepout region is defined for this purpose and is shown in Figure 8-44. The size of this region varies with the placement and DDR routing. Additional clearances required for the keepout region are shown in Table 8-34. Non-DDR3 signals should not be routed on the DDR signal layers within the DDR3 keepout region. Non-DDR3 signals may be routed in the region, provided they are routed on layers separated from the DDR signal layers by a ground layer. No breaks should be allowed in the reference ground layers in this region. In addition, the 1.5-V DDR3 power plane should cover the entire keepout region. Also note that the two signals from the DDR3 controller should be separated from each other by the specification in Table 8-34 (see KOD37).

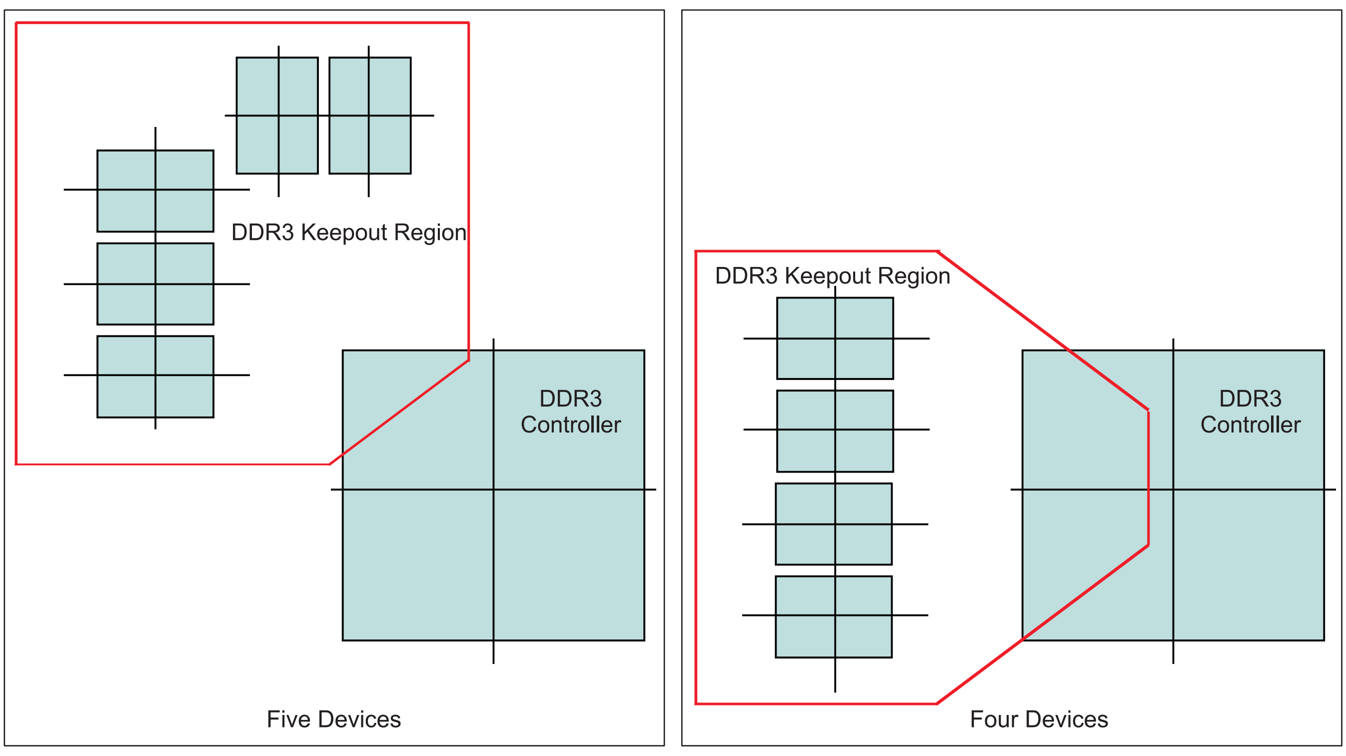


Figure 8-44. DDR3 Keepout Region

8.7.2.9 Bulk Bypass Capacitors

Bulk bypass capacitors are required for moderate speed bypassing of the DDR3 and other circuitry. Table 8-35 contains the minimum numbers and capacitance required for the bulk bypass capacitors. Note that this table only covers the bypass needs of the DDR3 controllers and DDR3 devices. Additional bulk bypass capacitance may be needed for other circuitry.

Table 8-35. Bulk Bypass Capacitors

NO.	PARAMETER	MIN	MAX	UNIT
1	vdds_ddr*x* bulk bypass capacitor count(1)	1		Devices
2	vdds_ddr*x* bulk bypass total capacitance	22		μF

(1) These devices should be placed near the devices they are bypassing, but preference should be given to the placement of the High Speed (HS) bypass capacitors and DDR3 signal routing.

8.7.2.10 High Speed Bypass Capacitors

High Speed (HS) bypass capacitors are critcal for proper DDR3 interface operation. It is particularly important to minimize the parasitic series inductance of the HS bypass capacitors, processor/DDR power, and processor/DDR ground connections. Table 8-36 contains the specification for the HS bypass capacitors as well as for the power connections on the PCB. Generally speaking, it is good to:

1. Fit as many HS bypass capacitors as possible.
2. Minimize the distance from the bypass cap to the pins/balls being bypassed.
3. Use the smallest physical sized capacitors possible with the highest capacitance readily available.
4. Connect the bypass capacitor pads to their vias using the widest traces possible and using the largest hole size via possible.
5. Minimize via sharing. Note the limites on via sharing shown in Table 8-36.

Table 8-36. High Speed Bypass Capacitors

NO.	PARAMETER	MIN	TYP	MAX	UNIT
1	HS bypass capacitor package size(1)		0201	0402	10 Mils
2	Distance, HS bypass capacitor to processor being bypassed(2)(3)(4)			400	Mils
3	Processor HS bypass capacitor count per vdds_ddrx rail(12)	See Table 8-3 and (11)			Devices
4	Processor HS bypass capacitor total capacitance per vdds_ddrx rail(12)	See Table 8-3 and (11)			μF
5	Number of connection vias for each device power/ground ball(5)				Vias
6	Trace length from device power/ground ball to connection via(2)		35	70	Mils
7	Distance, HS bypass capacitor to DDR device being bypassed(6)			150	Mils
8	DDR3 device HS bypass capacitor count(7)	12			Devices
9	DDR3 device HS bypass capacitor total capacitance(7)	0.85			μF
10	Number of connection vias for each HS capacitor(8)(9)	2			Vias
11	Trace length from bypass capacitor connect to connection via(2)(9)		35	100	Mils
12	Number of connection vias for each DDR3 device power/ground ball(10)	1			Vias
13	Trace length from DDR3 device power/ground ball to connection via(2)(8)		35	60	Mils

(1) L×W, 10-mil units, that is, a 0402 is a 40×20-mil surface-mount capacitor.

(2) Closer/shorter is better.

(3) Measured from the nearest processor power/ground ball to the center of the capacitor package.

(4) Three of these capacitors should be located underneath the processor, between the cluster of DDR_1V5 balls and ground balls, between the DDR interfaces on the package.

(5) See the Via Channel™ escape for the processor package.

(6) Measured from the DDR3 device power/ground ball to the center of the capacitor package.

(7) Per DDR3 device.

(8) An additional HS bypass capacitor can share the connection vias only if it is mounted on the opposite side of the board. No sharing of vias is permitted on the same side of the board.

(9) An HS bypass capacitor may share a via with a DDR device mounted on the same side of the PCB. A wide trace should be used for the connection and the length from the capacitor pad to the DDR device pad should be less than 150 mils.

(10) Up to a total of two pairs of DDR power/ground balls may share a via.

(11) The capacitor recommendations in this data manual reflect only the needs of this processor. Please see the memory vendor's guidelines for determining the appropriate decoupling capacitor arrangement for the memory device itself.

(12) For more information, see Section 8.3, *Core Power Domains*.

8.7.2.10.1 Return Current Bypass Capacitors

Use additional bypass capacitors if the return current reference plane changes due to DDR3 signals hopping from one signal layer to another. The bypass capacitor here provides a path for the return current to hop planes along with the signal. As many of these return current bypass capacitors should be used as possible. Because these are returns for signal current, the signal via size may be used for these capacitors.

8.7.2.11 Net Classes

Table 8-37 lists the clock net classes for the DDR3 interface. Table 8-38 lists the signal net classes, and associated clock net classes, for signals in the DDR3 interface. These net classes are used for the termination and routing rules that follow.

Table 8-37. Clock Net Class Definitions

CLOCK NET CLASS	processor PIN NAMES
CK	ddr1_ck/ddr1_nck
DQS0	ddr1_dqs0 / ddr1_dqsn0
DQS1	ddr1_dqs1 / ddr1_dqsn1
DQS2 (1)	ddr1_dqs2 / ddr1_dqsn2
DQS3 (1)	ddr1_dqs3 / ddr1_dqsn3

(1) Only used on 32-bit wide DDR3 memory systems.

Table 8-38. Signal Net Class Definitions

SIGNAL NET CLASS	ASSOCIATED CLOCK NET CLASS	processor PIN NAMES
ADDR_CTRL	CK	ddr1_ba[2:0], ddr1_a[14:0], ddr1_csn*j*, ddr1_casn, ddr1_rasn, ddr1_wen, ddr1_cke, ddr1_odt*i*
DQ0	DQS0	ddr1_d[7:0], ddr1_dqm0
DQ1	DQS1	ddr1_d[15:8], ddr1_dqm1
DQ2 (1)	DQS2	ddr1_d[23:16], ddr1_dqm2
DQ3 (1)	DQS3	ddr1_d[31:24], ddr1_dqm3

(1) Only used on 32-bit wide DDR3 memory systems.

8.7.2.12 DDR3 Signal Termination

Signal terminators are required for the CK and ADDR_CTRL net classes. The data lines are terminated by ODT and, thus, the PCB traces should be unterminated. Detailed termination specifications are covered in the routing rules in the following sections.

8.7.2.13 VREF_DDR Routing

ddr1_vref0 (VREF) is used as a reference by the input buffers of the DDR3 memories as well as the processor. VREF is intended to be half the DDR3 power supply voltage and is typically generated with the DDR3 VDDS and VTT power supply. It should be routed as a nominal 20-mil wide trace with 0.1 µF bypass capacitors near each device connection. Narrowing of VREF is allowed to accommodate routing congestion.

8.7.2.14 VTT

Like VREF, the nominal value of the VTT supply is half the DDR3 supply voltage. Unlike VREF, VTT is expected to source and sink current, specifically the termination current for the ADDR_CTRL net class Thevinen terminators. VTT is needed at the end of the address bus and it should be routed as a power sub-plane. VTT should be bypassed near the terminator resistors.

8.7.2.15 CK and ADDR_CTRL Topologies and Routing Definition

The CK and ADDR_CTRL net classes are routed in a fly-by topology. They are routed in a similar manner and are length matched to minimize skew between them. CK is a bit more complicated because it runs at a higher transition rate and is differential. The following subsections show the topology and routing for various DDR3 configurations for CK and ADDR_CTRL. The figures in the following subsections define the terms for the routing specification detailed in Table 8-39. Balanced-T routing is not recommended.

8.7.2.15.1 Four DDR3 Devices

Four DDR3 devices are supported on the DDR EMIF consisting of four x8 DDR3 devices arranged as one bank (CS). These four devices may be mounted on a single side of the PCB, or may be mirrored in two pairs to save board space at a cost of increased routing complexity and parts on the backside of the PCB.

8.7.2.15.1.1 CK and ADDR_CTRL Topologies, Four DDR3 Devices

Figure 8-45 shows the topology of the CK net classes and Figure 8-46 shows the topology for the corresponding ADDR_CTRL net classes.

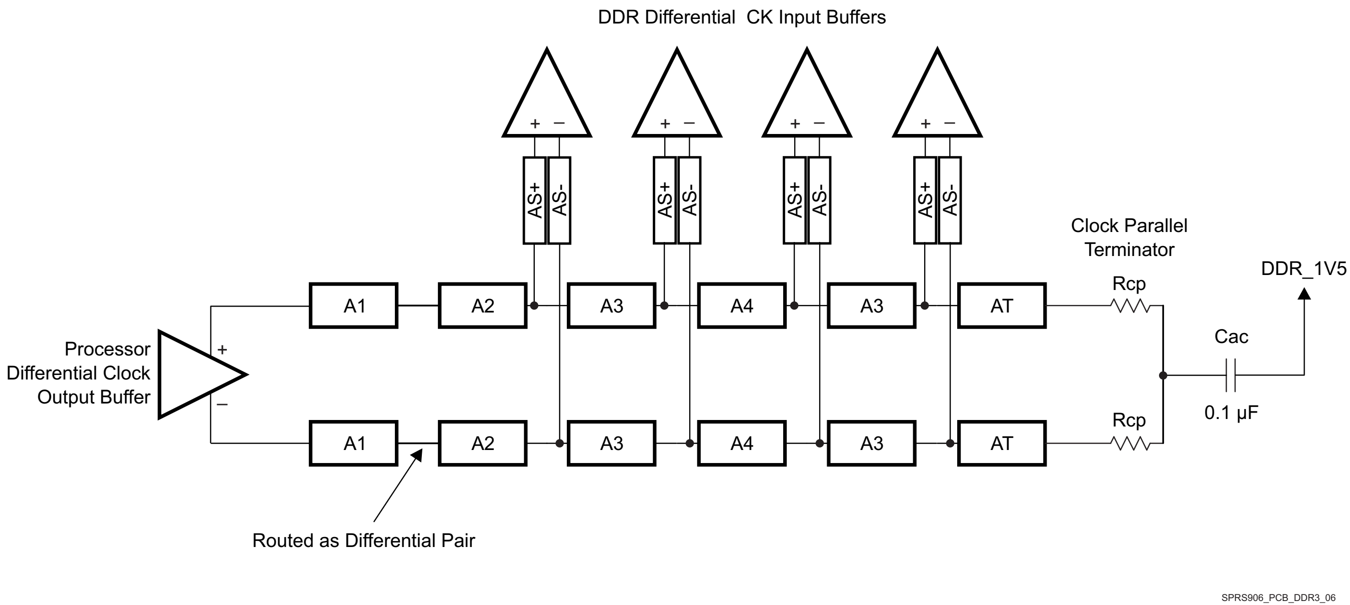


Figure 8-45. CK Topology for Four x8 DDR3 Devices

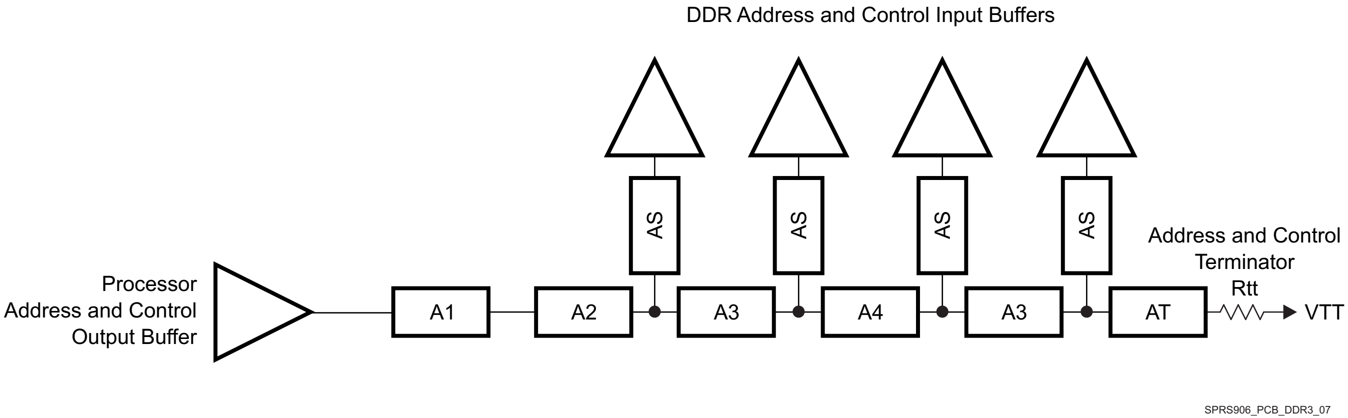


Figure 8-46. ADDR_CTRL Topology for Four x8 DDR3 Devices

8.7.2.15.1.2 CK and ADDR_CTRL Routing, Four DDR3 Devices

Figure 8-47 shows the CK routing for four DDR3 devices placed on the same side of the PCB. Figure 8-48 shows the corresponding ADDR_CTRL routing.

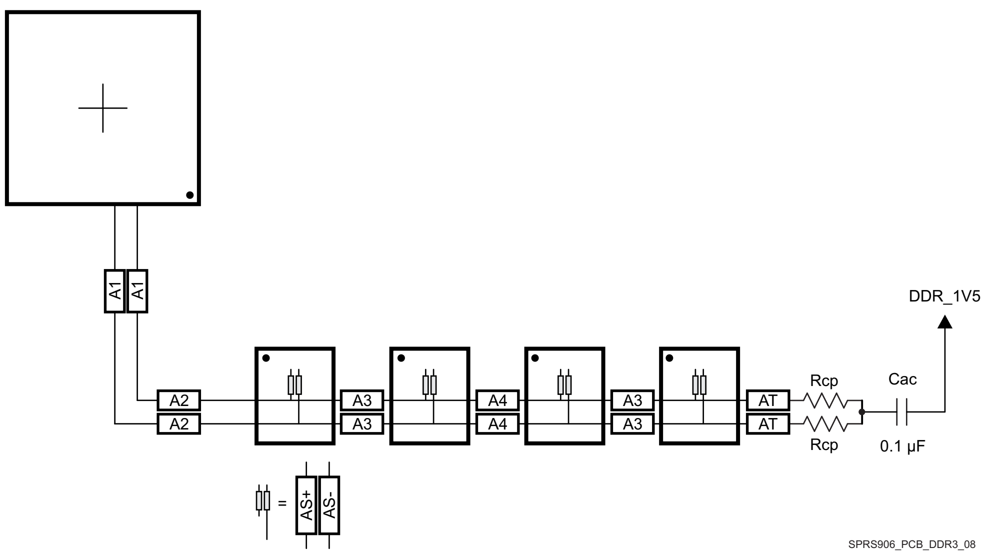


Figure 8-47. CK Routing for Four Single-Side DDR3 Devices

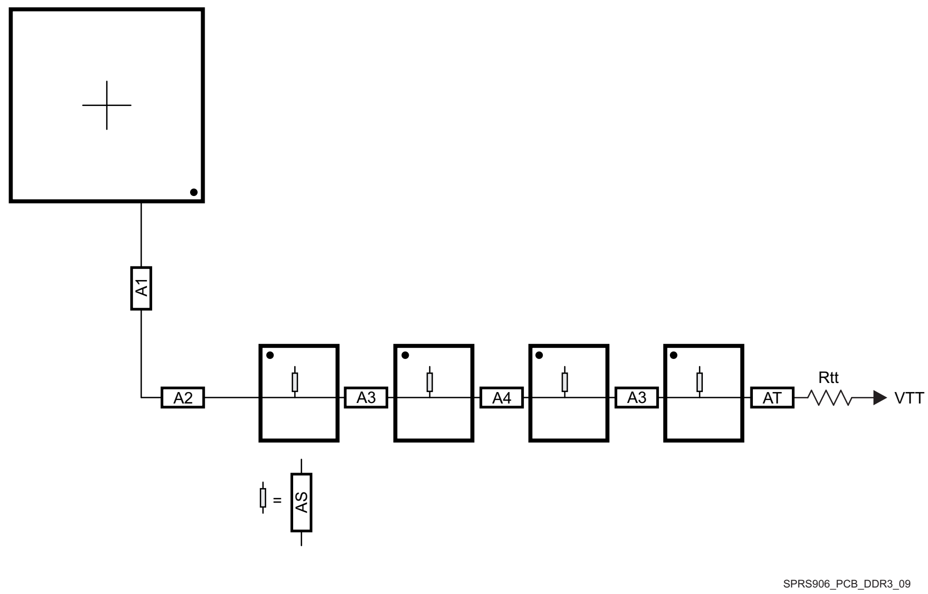


Figure 8-48. ADDR_CTRL Routing for Four Single-Side DDR3 Devices

To save PCB space, the four DDR3 memories may be mounted as two mirrored pairs at a cost of increased routing and assembly complexity. Figure 8-49 and Figure 8-50 show the routing for CK and ADDR_CTRL, respectively, for four DDR3 devices mirrored in a two-pair configuration.

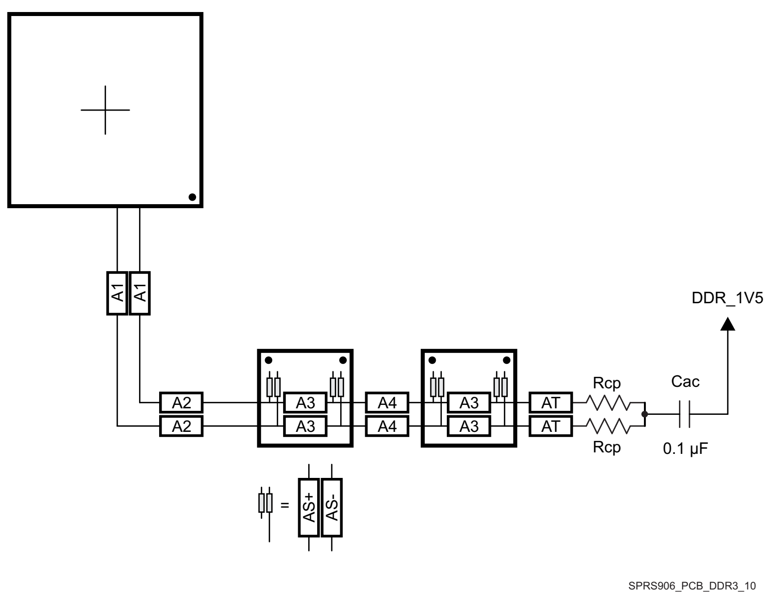


Figure 8-49. CK Routing for Four Mirrored DDR3 Devices

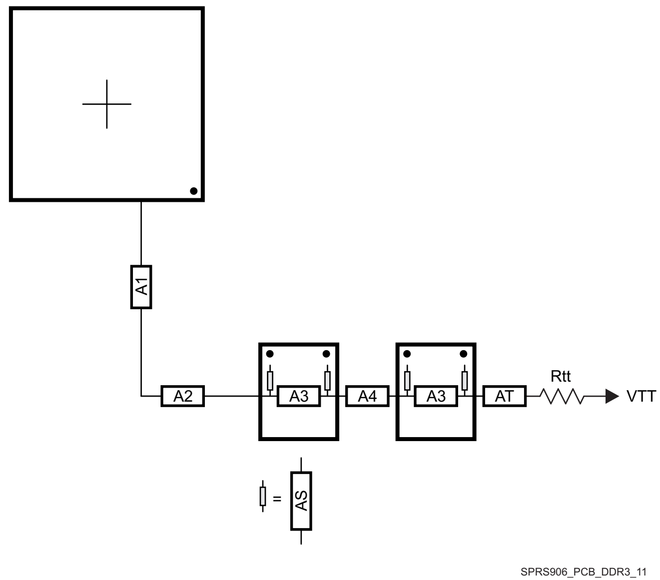


Figure 8-50. ADDR_CTRL Routing for Four Mirrored DDR3 Devices

8.7.2.15.2 Two DDR3 Devices

Two DDR3 devices are supported on the DDR EMIF consisting of two x8 DDR3 devices arranged as one bank (CS), 16 bits wide, or two x16 DDR3 devices arranged as one bank (CS), 32 bits wide. These two devices may be mounted on a single side of the PCB, or may be mirrored in a pair to save board space at a cost of increased routing complexity and parts on the backside of the PCB.

8.7.2.15.2.1 CK and ADDR_CTRL Topologies, Two DDR3 Devices

Figure 8-51 shows the topology of the CK net classes and Figure 8-52 shows the topology for the corresponding ADDR_CTRL net classes.

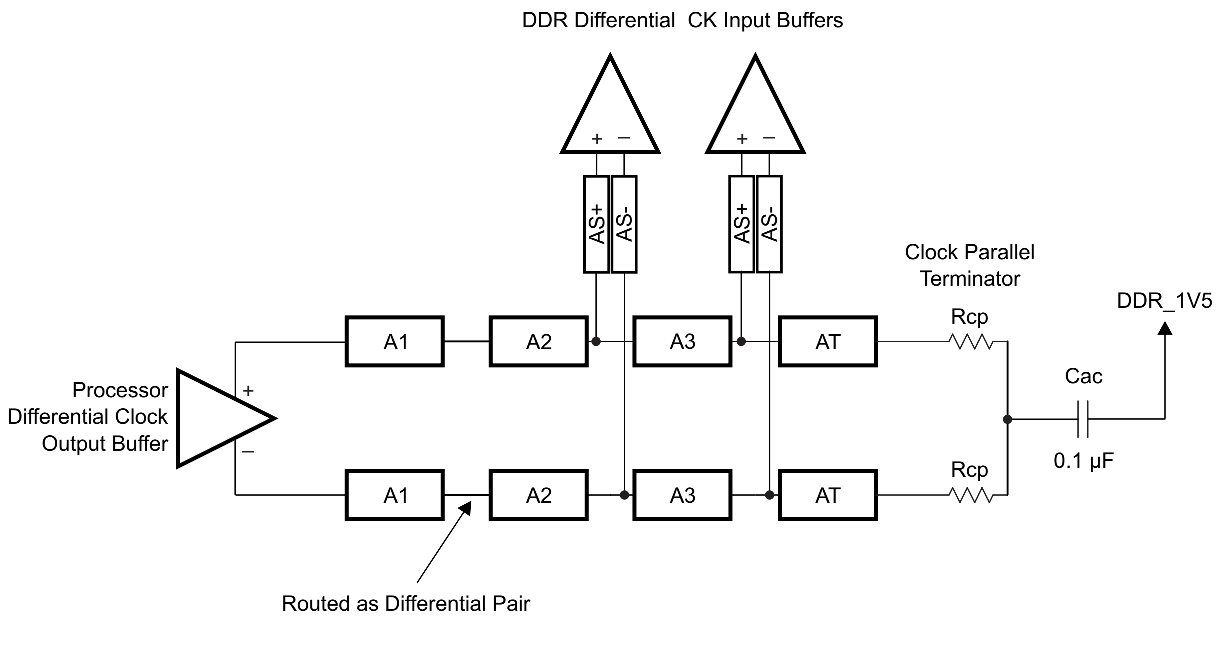


Figure 8-51. CK Topology for Two DDR3 Devices

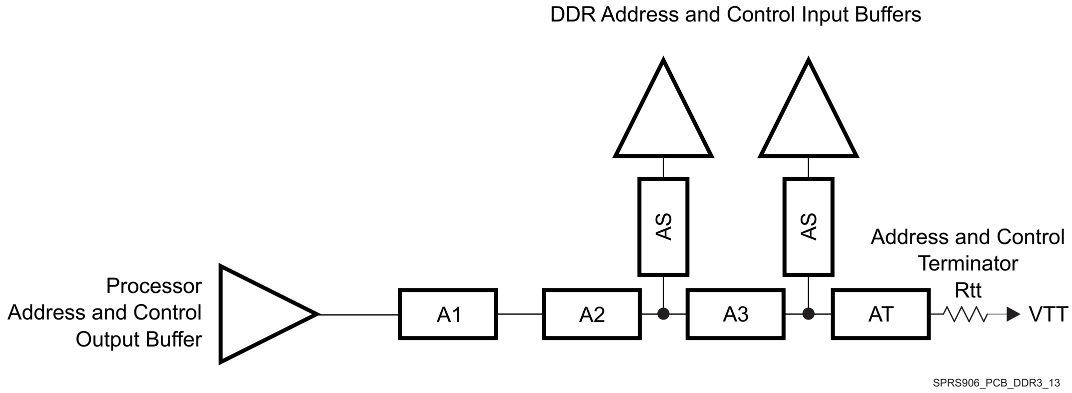


Figure 8-52. ADDR_CTRL Topology for Two DDR3 Devices

8.7.2.15.2.2 CK and ADDR_CTRL Routing, Two DDR3 Devices

Figure 8-53 shows the CK routing for two DDR3 devices placed on the same side of the PCB. Figure 8-54 shows the corresponding ADDR_CTRL routing.

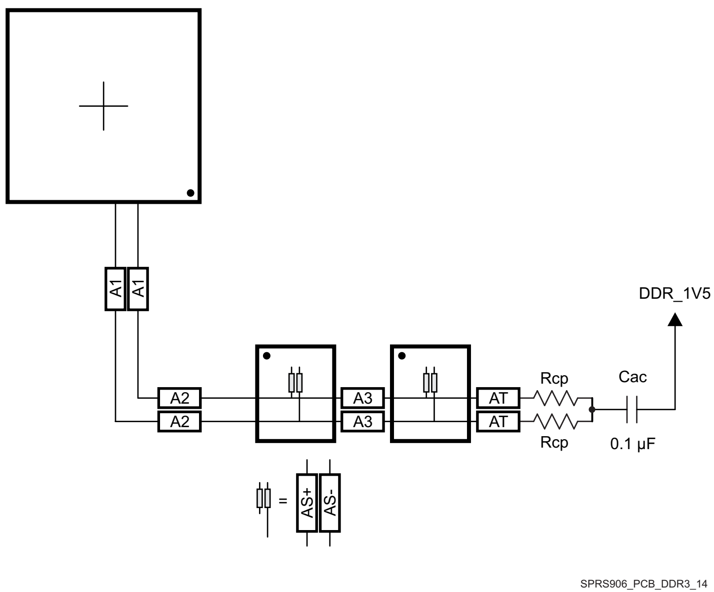


Figure 8-53. CK Routing for Two Single-Side DDR3 Devices

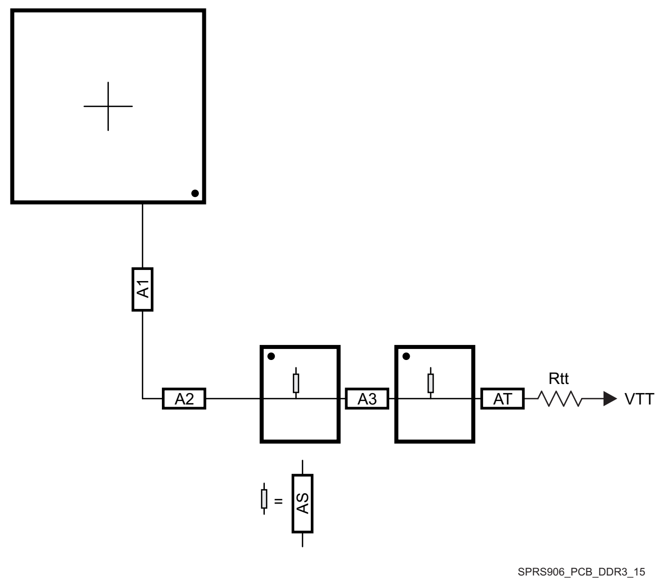


Figure 8-54. ADDR_CTRL Routing for Two Single-Side DDR3 Devices

To save PCB space, the two DDR3 memories may be mounted as a mirrored pair at a cost of increased routing and assembly complexity. Figure 8-55 and Figure 8-56 show the routing for CK and ADDR_CTRL, respectively, for two DDR3 devices mirrored in a single-pair configuration.

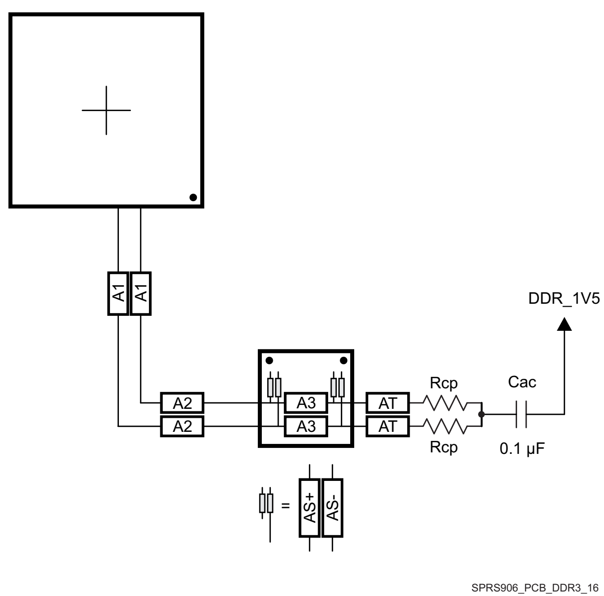


Figure 8-55. CK Routing for Two Mirrored DDR3 Devices

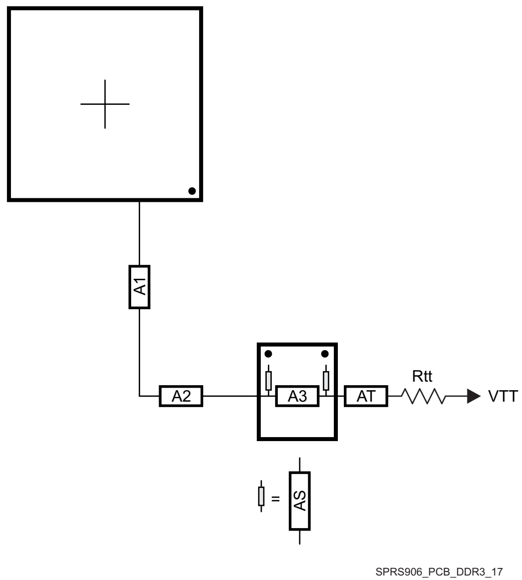


Figure 8-56. ADDR_CTRL Routing for Two Mirrored DDR3 Devices

8.7.2.15.3 One DDR3 Device

A single DDR3 device is supported on the DDR EMIF consisting of one x16 DDR3 device arranged as one bank (CS), 16 bits wide.

8.7.2.15.3.1 CK and ADDR_CTRL Topologies, One DDR3 Device

Figure 8-57 shows the topology of the CK net classes and Figure 8-58 shows the topology for the corresponding ADDR_CTRL net classes.

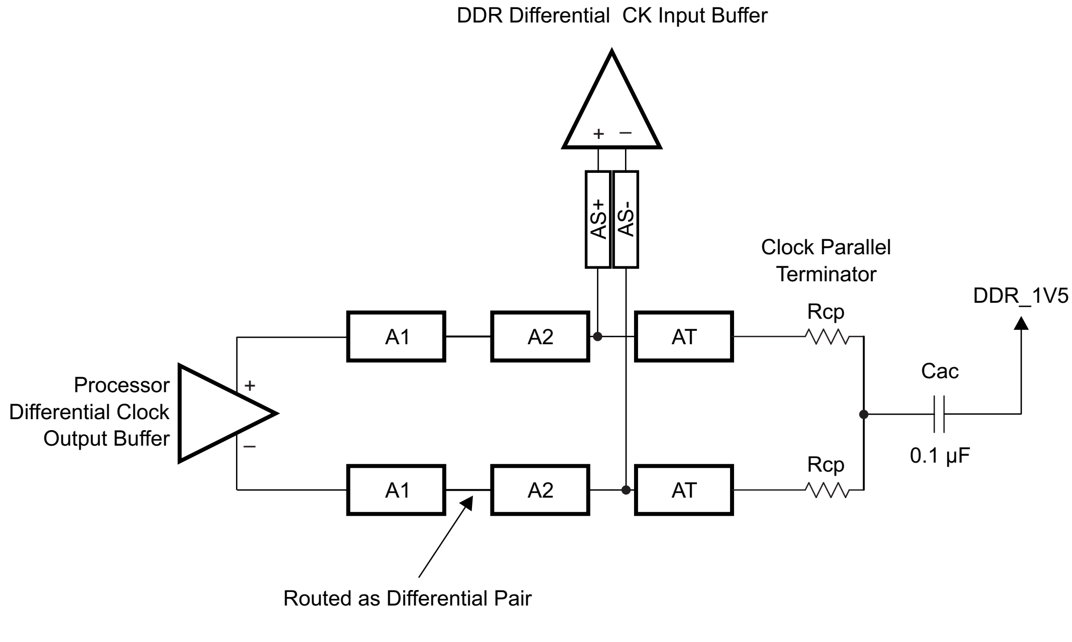


Figure 8-57. CK Topology for One DDR3 Device

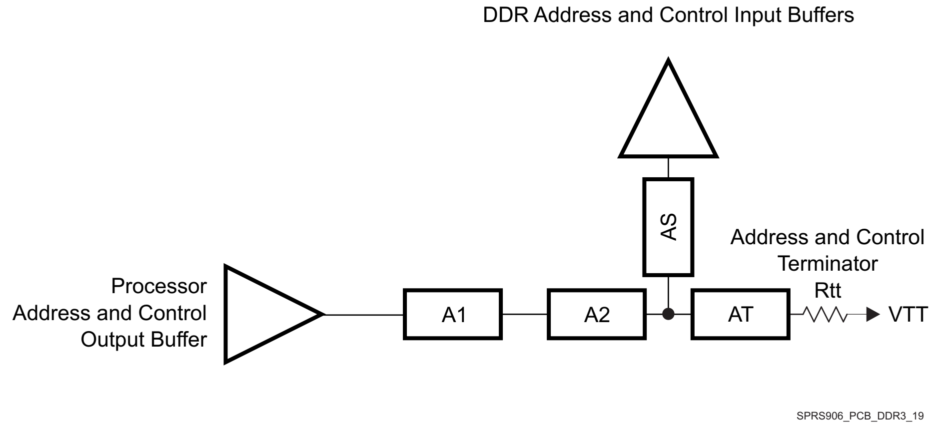


Figure 8-58. ADDR_CTRL Topology for One DDR3 Device

8.7.2.15.3.2 CK and ADDR/CTRL Routing, One DDR3 Device

Figure 8-59 shows the CK routing for one DDR3 device placed on the same side of the PCB. Figure 8-60 shows the corresponding ADDR_CTRL routing.

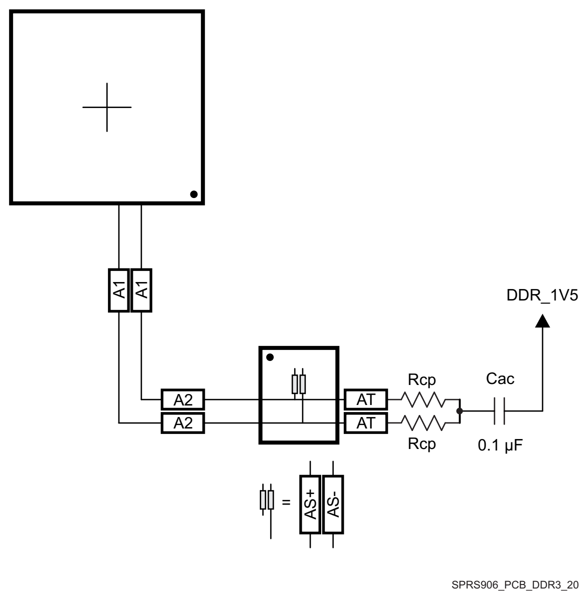


Figure 8-59. CK Routing for One DDR3 Device

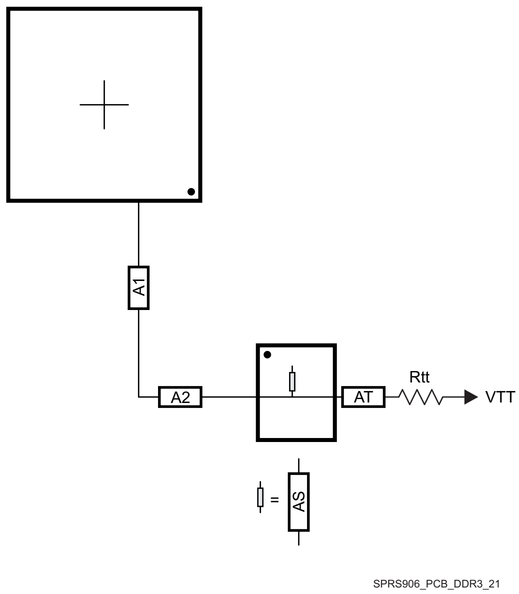


Figure 8-60. ADDR_CTRL Routing for One DDR3 Device

8.7.2.16 Data Topologies and Routing Definition

No matter the number of DDR3 devices used, the data line topology is always point to point, so its definition is simple.

Care should be taken to minimize layer transitions during routing. If a layer transition is necessary, it is better to transition to a layer using the same reference plane. If this cannot be accommodated, ensure there are nearby ground vias to allow the return currents to transition between reference planes if both reference planes are ground or vdds_ddr. Ensure there are nearby bypass capacitors to allow the return currents to transition between reference planes if one of the reference planes is ground. The goal is to minimize the size of the return current loops.

8.7.2.16.1 DQS and DQ/DM Topologies, Any Number of Allowed DDR3 Devices

DQS lines are point-to-point differential, and DQ/DM lines are point-to-point singled ended. Figure 8-61 and Figure 8-62 show these topologies.

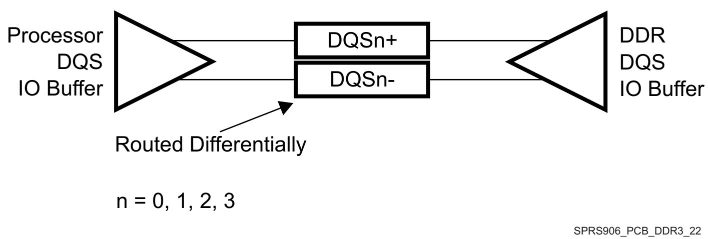


Figure 8-61. DQS Topology

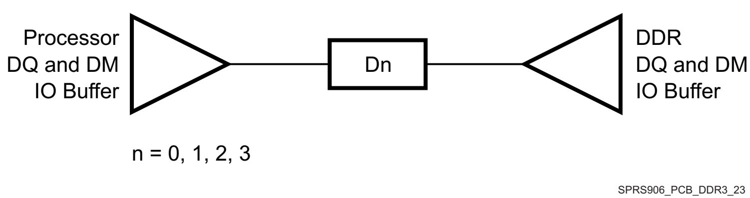


Figure 8-62. DQ/DM Topology

8.7.2.16.2 DQS and DQ/DM Routing, Any Number of Allowed DDR3 Devices

Figure 8-63 and Figure 8-64 show the DQS and DQ/DM routing.

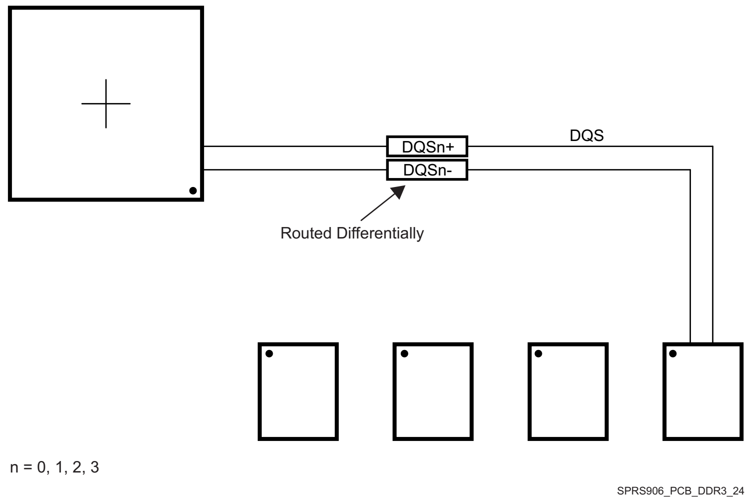


Figure 8-63. DQS Routing With Any Number of Allowed DDR3 Devices

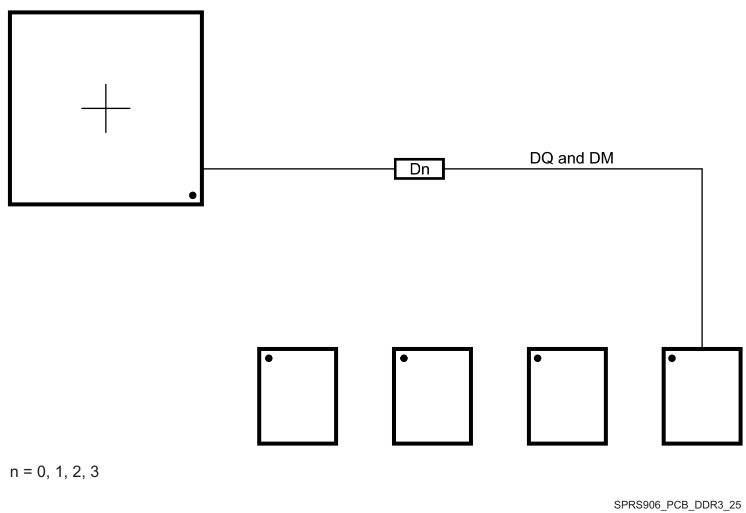


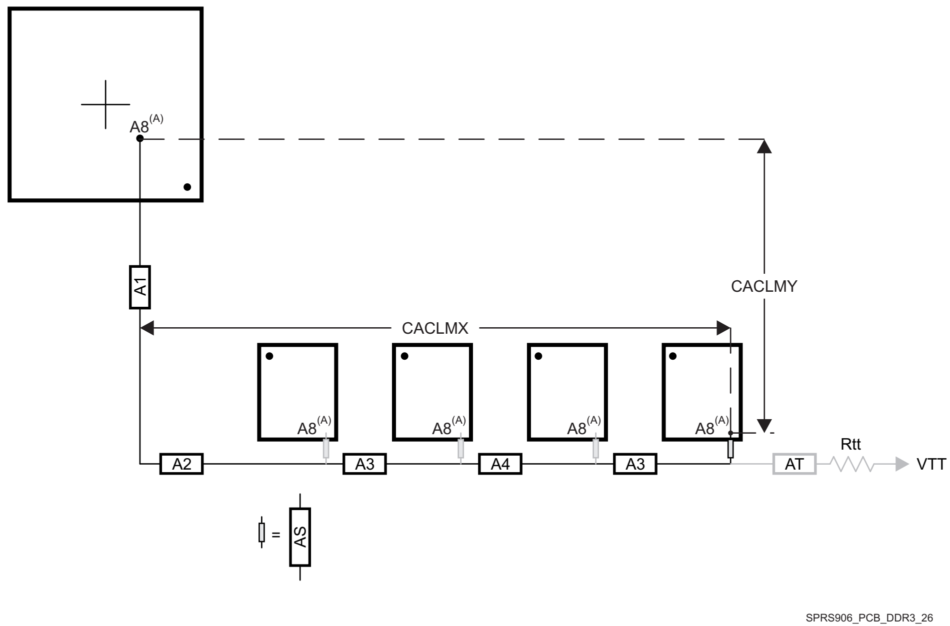
Figure 8-64. DQ/DM Routing With Any Number of Allowed DDR3 Devices

8.7.2.17 Routing Specification

8.7.2.17.1 CK and ADDR_CTRL Routing Specification

Skew within the CK and ADDR_CTRL net classes directly reduces setup and hold margin and, thus, this skew must be controlled. The only way to practically match lengths on a PCB is to lengthen the shorter traces up to the length of the longest net in the net class and its associated clock. A metric to establish this maximum length is Manhattan distance. The Manhattan distance between two points on a PCB is the length between the points when connecting them only with horizontal or vertical segments. A reasonable trace route length is to within a percentage of its Manhattan distance. CACLM is defined as Clock Address Control Longest Manhattan distance.

Given the clock and address pin locations on the processor and the DDR3 memories, the maximum possible Manhattan distance can be determined given the placement. Figure 8-65 and Figure 8-66 show this distance for four loads and two loads, respectively. It is from this distance that the specifications on the lengths of the transmission lines for the address bus are determined. CACLM is determined similarly for other address bus configurations; that is, it is based on the longest net of the CK/ADDR_CTRL net class. For CK and ADDR_CTRL routing, these specifications are contained in Table 8-39.

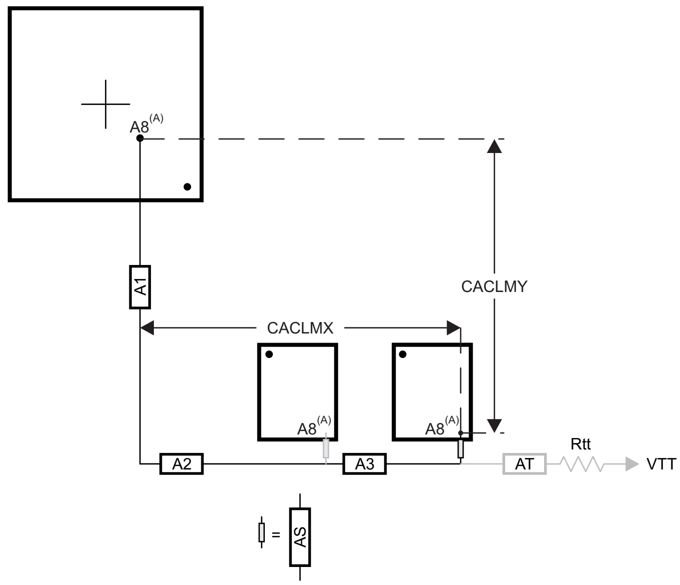


A. It is very likely that the longest CK/ADDR_CTRL Manhattan distance will be for Address Input 8 (A8) on the DDR3 memories. CACLM is based on the longest Manhattan distance due to the device placement. Verify the net class that satisfies this criteria and use as the baseline for CK/ADDR_CTRL skew matching and length control.

The length of shorter CK/ADDR_CTRL stubs as well as the length of the terminator stub are not included in this length calculation. Non-included lengths are grayed out in the figure.

Assuming A8 is the longest, CALM = CACLMY + CACLMX + 300 mils.
The extra 300 mils allows for routing down lower than the DDR3 memories and returning up to reach A8.

Figure 8-65. CACLM for Four Address Loads on One Side of PCB



A. It is very likely that the longest CK/ADDR_CTRL Manhattan distance will be for Address Input 8 (A8) on the DDR3 memories. CACLM is based on the longest Manhattan distance due to the device placement. Verify the net class that satisfies this criteria and use as the baseline for CK/ADDR_CTRL skew matching and length control.

The length of shorter CK/ADDR_CTRL stubs as well as the length of the terminator stub are not included in this length calculation. Non-included lengths are grayed out in the figure.

Assuming A8 is the longest, CALM = CACLMY + CACLMX + 300 mils.
The extra 300 mils allows for routing down lower than the DDR3 memories and returning up to reach A8.

Figure 8-66. CACLM for Two Address Loads on One Side of PCB

Table 8-39. CK and ADDR_CTRL Routing Specification(2)(3)

NO.	PARAMETER	MIN	TYP	MAX	UNIT
CARS31	A1+A2 length			500(1)	ps
CARS32	A1+A2 skew			29	ps
CARS33	A3 length			125	ps
CARS34	A3 skew(4)			6	ps
CARS35	A3 skew(5)			6	ps
CARS36	A4 length			125	ps
CARS37	A4 skew			6	ps
CARS38	AS length		5	17(1)	ps
CARS39	AS skew		1.3	14(1)	ps
CARS310	AS+/AS- length		5	12	ps
CARS311	AS+/AS- skew			1	ps
CARS312	AT length(6)		75		ps
CARS313	AT skew(7)		14		ps
CARS314	AT skew(8)			1	ps
CARS315	CK/ADDR_CTRL trace length			1020	ps
CARS316	Vias per trace			3(1)	vias
CARS317	Via count difference			1(15)	vias
CARS318	Center-to-center CK to other DDR3 trace spacing(9)	4w			
CARS319	Center-to-center ADDR_CTRL to other DDR3 trace spacing(9)(10)	4w			
CARS320	Center-to-center ADDR_CTRL to other ADDR_CTRL trace spacing(9)	3w			

Table 8-39. CK and ADDR_CTRL Routing Specification[2][3] (continued)

NO.	PARAMETER	MIN	TYP	MAX	UNIT
CARS321	CK center-to-center spacing[11][12]				
CARS322	CK spacing to other net[9]	4w			
CARS323	Rcp[13]	Zo-1	Zo	Zo+1	Ω
CARS324	Rtt[13][14]	Zo-5	Zo	Zo+5	Ω

(1) Max value is based upon conservative signal integrity approach. This value could be extended only if detailed signal integrity analysis of rise time and fall time confirms desired operation.

(2) The use of vias should be minimized.

(3) Additional bypass capacitors are required when using the DDR_1V5 plane as the reference plane to allow the return current to jump between the DDR_1V5 plane and the ground plane when the net class switches layers at a via.

(4) Non-mirrored configuration (all DDR3 memories on same side of PCB).

(5) Mirrored configuration (one DDR3 device on top of the board and one DDR3 device on the bottom).

(6) While this length can be increased for convenience, its length should be minimized.

(7) ADDR_CTRL net class only (not CK net class). Minimizing this skew is recommended, but not required.

(8) CK net class only.

(9) Center-to-center spacing is allowed to fall to minimum 2w for up to 1250 mils of routed length.

(10) The ADDR_CTRL net class of the other DDR EMIF is considered *other DDR3 trace spacing*.

(11) CK spacing set to ensure proper differential impedance.

(12) The most important thing to do is control the impedance so inadvertent impedance mismatches are not created. Generally speaking, center-to-center spacing should be either 2w or slightly larger than 2w to achieve a differential impedance equal to twice the singleended impedance, Zo.

(13) Source termination (series resistor at driver) is specifically not allowed.

(14) Termination values should be uniform across the net class.

(15) Via count difference may increase by 1 only if accurate 3-D modeling of the signal flight times – including accurately modeled signal propagation through vias – has been applied to ensure all segment skew maximums are not exceeded.

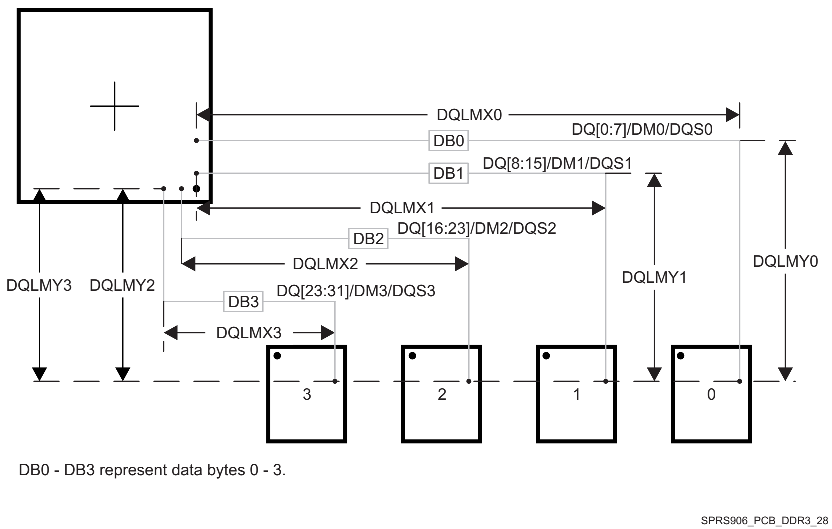
8.7.2.17.2 DQS and DQ Routing Specification

Skew within the DQS and DQ/DM net classes directly reduces setup and hold margin and thus this skew must be controlled. The only way to practically match lengths on a PCB is to lengthen the shorter traces up to the length of the longest net in the net class and its associated clock. As with CK and ADDR_CTRL, a reasonable trace route length is to within a percentage of its Manhattan distance. DQLMn is defined as DQ Longest Manhattan distance n, where n is the byte number. For a 32-bit interface, there are four DQLMs, DQLM0-DQLM3. Likewise, for a 16-bit interface, there are two DQLMs, DQLM0-DQLM1.

NOTE

It is not required, nor is it recommended, to match the lengths across all bytes. Length matching is only required within each byte.

Given the DQS and DQ/DM pin locations on the processor and the DDR3 memories, the maximum possible Manhattan distance can be determined given the placement. Figure 8-67 shows this distance for four loads. It is from this distance that the specifications on the lengths of the transmission lines for the data bus are determined. For DQS and DQ/DM routing, these specifications are contained in Table 8-40.



There are four DQLMs, one for each byte (32-bit interface). Each DQLM is the longest Manhattan distance of the byte; therefore:

DQLM0 = DQLMX0 + DQLMY0
DQLM1 = DQLMX1 + DQLMY1
DQLM2 = DQLMX2 + DQLMY2
DQLM3 = DQLMX3 + DQLMY3

Figure 8-67. DQLM for Any Number of Allowed DDR3 Devices

Table 8-40. Data Routing Specification(2)

NO.	PARAMETER	MIN	TYP	MAX	UNIT
DRS31	DB0 length			340	ps
DRS32	DB1 length			340	ps
DRS33	DB2 length			340	ps
DRS34	DB3 length			340	ps
DRS35	DBn skew(3)			5	ps
DRS36	DQSn+ to DQSn- skew			1	ps
DRS37	DQSn to DBn skew(3)(4)			5(10)	ps
DRS38	Vias per trace			2(1)	vias
DRS39	Via count difference			0(10)	vias
DRS310	Center-to-center DBn to other DDR3 trace spacing(6)	4			w(5)
DRS311	Center-to-center DBn to other DBn trace spacing(7)	3			w(5)
DRS312	DQSn center-to-center spacing(8)(9)				
DRS313	DQSn center-to-center spacing to other net	4			w(5)

(1) Max value is based upon conservative signal integrity approach. This value could be extended only if detailed signal integrity analysis of rise time and fall time confirms desired operation.
(2) External termination disallowed. Data termination should use built-in ODT functionality.
(3) Length matching is only done within a byte. Length matching across bytes is neither required nor recommended.
(4) Each DQS pair is length matched to its associated byte.
(5) Center-to-center spacing is allowed to fall to minimum 2w for up to 1250 mils of routed length.
(6) Other DDR3 trace spacing means other DDR3 net classes not within the byte.
(7) This applies to spacing within the net classes of a byte.
(8) DQS pair spacing is set to ensure proper differential impedance.
(9) The most important thing to do is control the impedance so inadvertent impedance mismatches are not created. Generally speaking, center-to-center spacing should be either 2w or slightly larger than 2w to achieve a differential impedance equal to twice the singleended impedance, Zo.
(10) Via count difference may increase by 1 only if accurate 3-D modeling of the signal flight times – including accurately modeled signal propagation through vias – has been applied to ensure DBn skew and DQSn to DBn skew maximums are not exceeded.

9 Device and Documentation Support

TI offers an extensive line of development tools, including methods to evaluate the performance of the processors, generate code, develop algorithm implementations, and fully integrate and debug software and hardware modules as listed below.

9.1 Device Nomenclature and Orderable Information

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all microprocessors (MPUs) and support tools. Each device has one of three prefixes: X, P, or null (no prefix) (for example, TDA2Ex). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMDX) through fully qualified production devices and tools (TMDS).

Device development evolutionary flow:

X Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.

P Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.

null Production version of the silicon die that is fully qualified.

Support tool development evolutionary flow:

TMDX Development-support product that has not yet completed Texas Instruments internal qualification testing.

TMDS Fully-qualified development-support product.

X and P devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

Production devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

For orderable part numbers of TDA2Ex devices in the ABC package type, see the Package Option Addendum of this document, the TI website (ti.com), or contact your TI sales representative.

9.1.1 Standard Package Symbolization

NOTE

Some devices may have a cosmetic circular marking visible on the top of the device package which results from the production test process. In addition, some devices may also show a color variation in the package substrate which results from the substrate manufacturer. These differences are cosmetic only with no reliability impact.

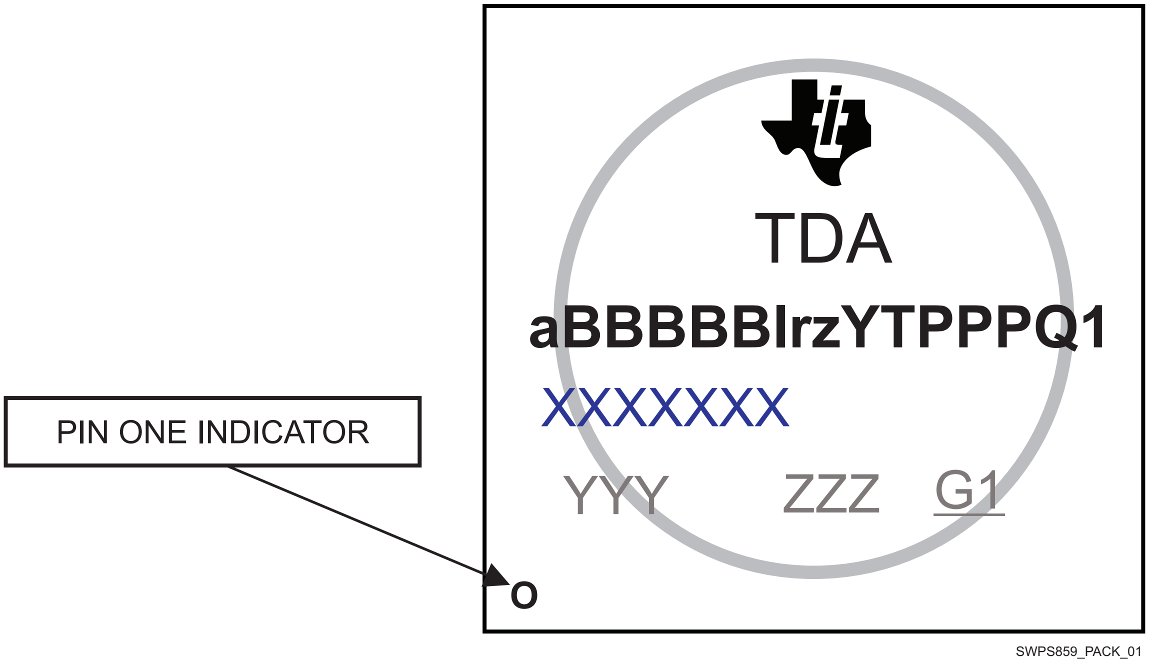


Figure 9-1. Printed Device Reference

9.1.2 Device Naming Convention

Table 9-1. Nomenclature Description

FIELD PARAMETER	FIELD DESCRIPTION	VALUES		DESCRIPTION
		SYMBOLIZATION	ORDERABLE	
a	Device evolution stage[1]	X	*Contact TI*	Prototype
		P		Preproduction (production test flow, no reliability data)
		BLANK		Production
BBBBB[3]	Base production part number	TDA2E		ADAS 2nd Generation Eco Tier
I	Device Identity	V		Scene Viewing
		G		GFX enabled
r	Device revision	BLANK		SR 1.0
		A		SR 2.0
		B		SR 2.1
z	Device Speed	D		Indicates the speed grade for each of the cores in the device. For more information see Table 3-1, *Device Comparison*.
		H		
Y	Device type	BLANK		General purpose (Prototype and Production)
		E		Emulation (E) devices
		S		High-Security device, Secure Boot Supported
		D		High security prototype devices with TI Development keys (D)
T	Temperature [2]	Q		Full temp range: -40°C to 125°C
PPP	Package designator	ABC		S-PBGA-N760 (23 mm × 23 mm) Package
c	Carrier designator	N/A	BLANK	Tray
		N/A	R	Tape & Reel

Table 9-1. Nomenclature Description (continued)

FIELD PARAMETER	FIELD DESCRIPTION	VALUES		DESCRIPTION
		SYMBOLIZATION	ORDERABLE	
Q1	Automotive Designator	BLANK		Not meeting automotive qualification
		Q1		Meeting Q100 equal requirements, with exceptions as specified in DM.
XXXXXXX	Lot Trace Code	*As marked*	N/A	
YYY	Production Code, For TI use only	*As marked*	N/A	
ZZZ	Production Code, For TI use only	*As marked*	N/A	
O	Pin one designator	*As marked*	N/A	
G1	ECAT—Green package designator	*As marked*	N/A	

(1) To designate the stages in the product development cycle, TI assigns prefixes to the part numbers. These prefixes represent evolutionary stages of product development from engineering prototypes through fully qualified production devices.
Prototype devices are shipped against the following disclaimer:
"This product is still under development and is intended for internal evaluation purposes."
Notwithstanding any provision to the contrary, TI makes no warranty expressed, implied, or statutory, including any implied warranty of merchantability of fitness for a specific purpose, of this device.

(2) Applies to device max junction temperature.

(3) XDRA726 base part number with X speed grade indicator is the part number for the superset device. Software should constrain the features and speed used to match the intended production device.

NOTE

BLANK in the symbol or part number is collapsed so there are no gaps between characters.

9.2 Tools and Software

The following products support development for TDA2Ex platforms:

Design Kits and Evaluation Modules

TDA2Ex Evaluation Module TDA2Ex EVM is an evaluation platform designed to speed up development efforts and reduce time to market for ADAS applications. It is based on a TDA2Eco SoC which incorporates a heterogeneous, scalable architecture that includes a mix of TI's fixed and floating-point TMS320C66x Digital Signal Processor (DSP) core, Arm Cortex-A15 MP core, 3D GPU core, H.264 encode/decode acceleration and dual Cortex-M4 processor cores. It also integrates a host of peripherals including multi-camera interfaces (both parallel and serial) for LVDS-based surround view systems, displays, CAN and GigB Ethernet AVB. The main board integrates key peripherals such as Ethernet, FPD-Link and HDMI, while the Vision application board provides interfaces for popular imagers.

Development Tools

Clock Tree Tool for Sitara, Automotive, Vision Analytics, & Digital Signal Processors The Clock Tree Tool (CTT) for Sitara™ Arm®, Automotive, and Digital Signal Processors is an interactive clock tree configuration software that provides information about the clocks and modules in these TI devices. It allows the user to:

- Visualize the device clock tree
- Interact with clock tree elements and view the effect on PRCM registers
- Interact with the PRCM registers and view the effect on the device clock tree
- View a trace of all the device registers affected by the user interaction with clock tree

XDS110 JTAG Debug Probe The Texas Instruments XDS110 is a new class of debug probe (emulator) for TI embedded processors. The XDS110 replaces the XDS100 family while supporting a wider variety of standards (IEEE1149.1, IEEE1149.7, SWD) in a single pod. Also, all XDS debug probes support Core and System Trace in all Arm and DSP processors that feature an Embedded Trace Buffer (ETB). The Texas Instruments XDS110 connects to the target board via a TI 20-pin connector (with multiple adapters for TI 14-pin and, Arm 10-pin and Arm 20-pin) and to the host PC via USB2.0 High Speed (480Mbps). It also features two additional connections: the Auxiliary 14-pin port connector that enables EnergyTrace™, a full duplex UART port and four General-Purpose I/Os, and the Expansion 30-pin connector to connect the XDS110 EnergyTrace HDR add-on.

Models

TDA2Ex BSDL Model BSDL Model

TDA2Ex IBIS Model IBIS Model

TDA2Ex Thermal Model Thermal Model

For a complete listing of development-support tools for the processor platform, visit the Texas Instruments website at ti.com. For information on pricing and availability, contact the nearest TI field sales office or authorized distributor.

9.3 Documentation Support

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

The following documents describe the TDA2Ex devices.

Technical Reference Manual

TDA2Ex SoC for Advanced Driver Assistance Systems (ADAS) 23mm (ABC) Package (SR2.0, SR1.0) 17mm (CBD) Package (SR2.1, SR2.0) Technical Reference Manual Details the integration, the environment, the functional description, and the programming models for each peripheral and subsystem in the TDA2Ex family of devices.

Errata

TDA2Ex SoC for Advanced Driver Assistance Systems (ADAS) 23mm (ABC) Package (SR2.0, SR1.0) 17mm (CBD) Package (SR2.1, SR2.0) Silicon Errata Describes the known exceptions to the functional specifications for the device.

9.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

10 Mechanical, Packaging, and Orderable Information

10.1 Packaging Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TDA2EGADQABCQ1	Active	Production	FCBGA (ABC) | 760	60 | EIAJ TRAY (5+1)	-	Call TI	Level-3-250C-168 HR	-40 to 125	TDA2EGADQABCQ1 JACINTO 784 784 ABC
TDA2EGAHQABCQ1	Active	Production	FCBGA (ABC) | 760	60 | JEDEC TRAY (5+1)	-	Call TI	Level-3-250C-168 HR	-40 to 125	TDA2EGAHQABCQ1 784 784 ABC
TDA2EGAHQABCRQ1	Active	Production	FCBGA (ABC) | 760	250 | LARGE T&R	-	Call TI	Level-3-250C-168 HR	-40 to 125	TDA2EGAHQABCQ1 784 784 ABC

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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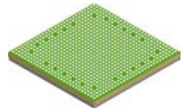
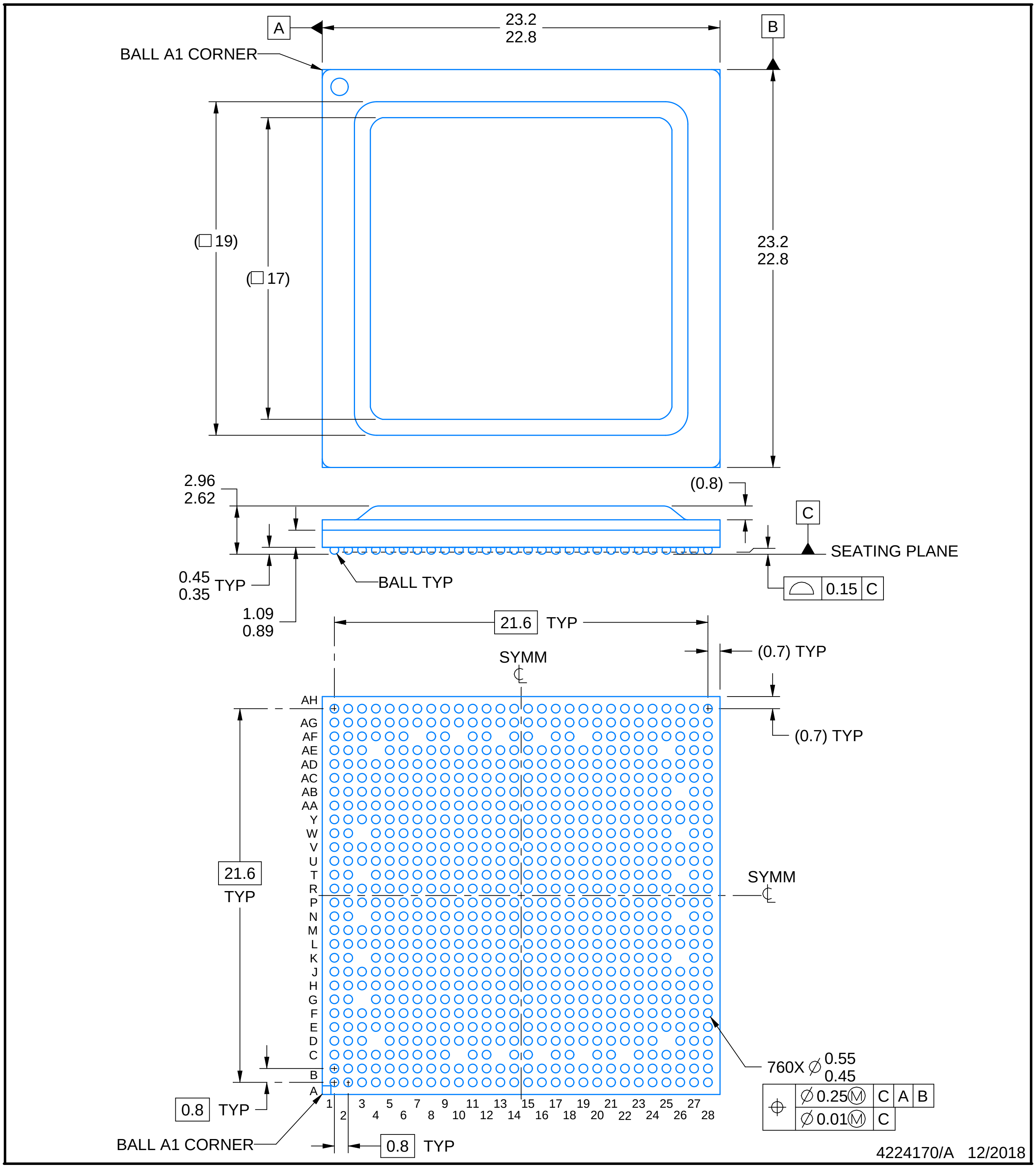


PACKAGE OUTLINE

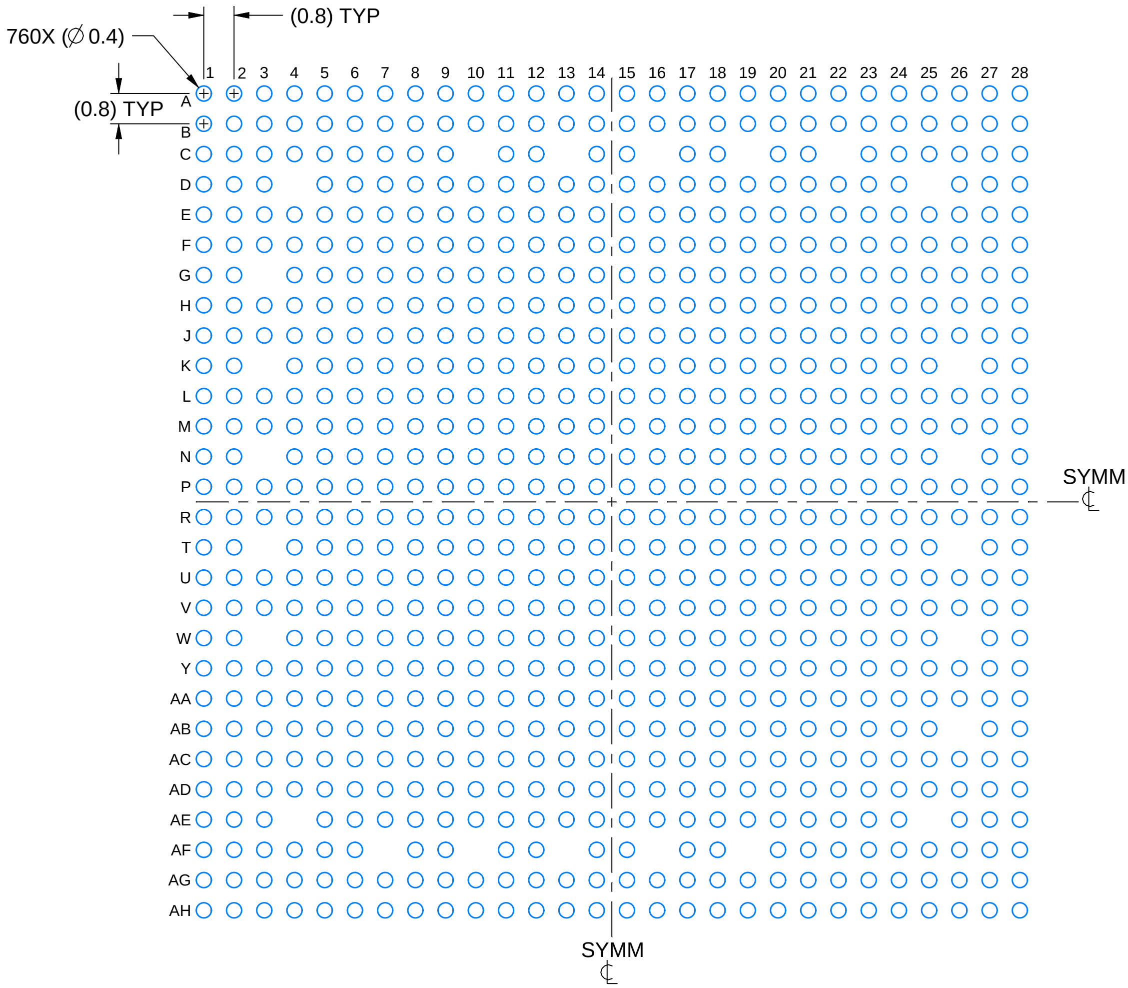
FCBGA - 2.96 mm max height

PLASTIC BALL GRID ARRAY

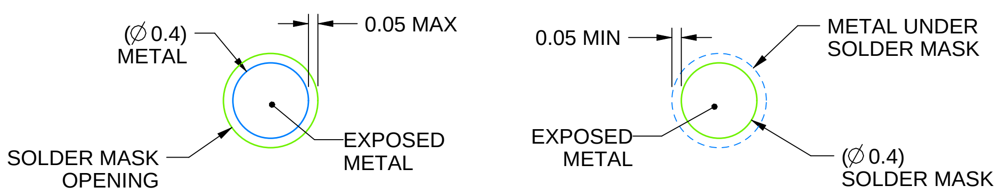


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:5X



NON-SOLDER MASK DEFINED (PREFERRED)

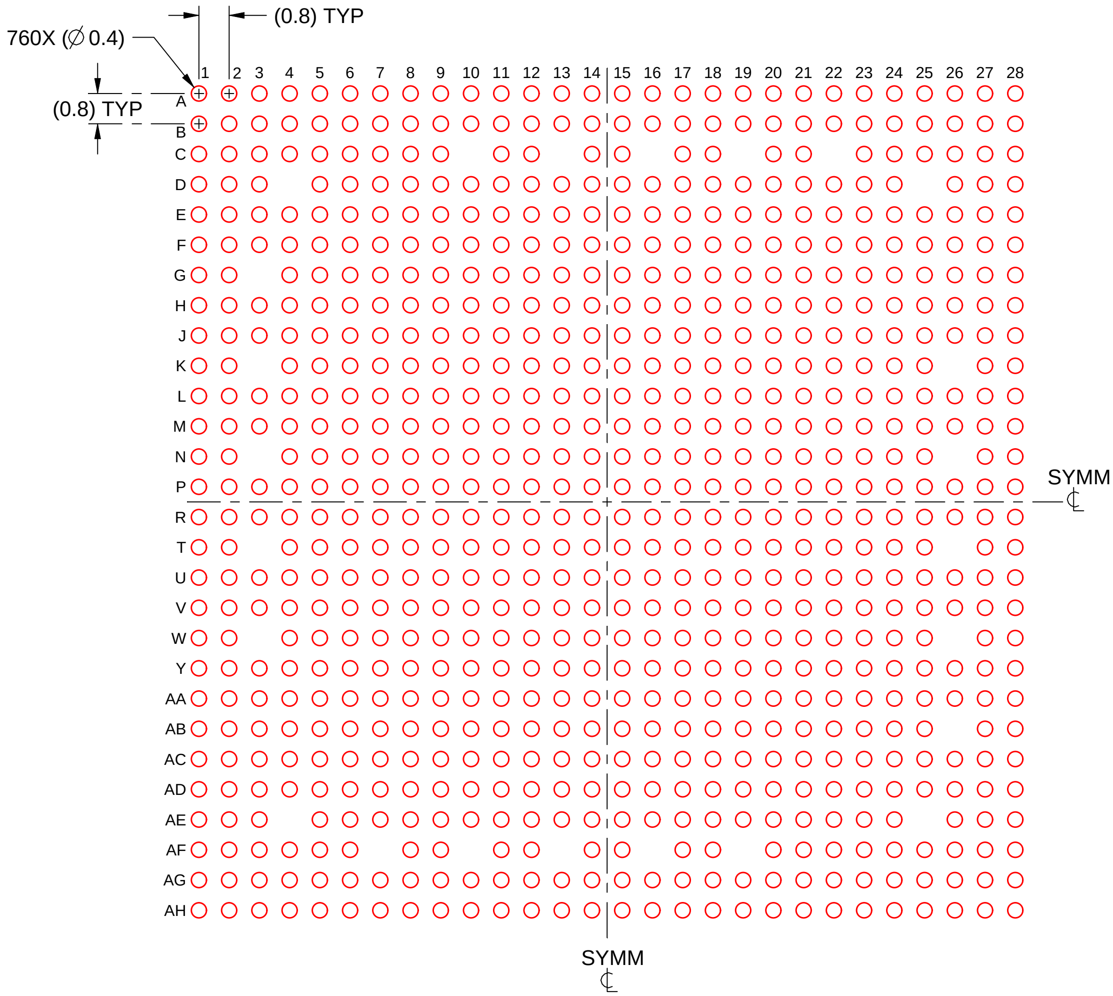
SOLDER MASK DEFINED

SOLDER MASK DETAILS
NOT TO SCALE

4224170/A 12/2018

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For information, see Texas Instruments literature number SPRU811 (www.ti.com/lit/spru811).



SOLDER PASTE EXAMPLE
BASED ON 0.15 mm THICK STENCIL
SCALE:5X

4224170/A 12/2018

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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