OPA818 2.7GHz, High-Voltage, FET-Input, Low-Noise, Operational Amplifier

1 Features

- High speed:
  - Gain-bandwidth product (GBWP): 2.7GHz
  - Bandwidth (G = 7V/V): 765MHz
  - Large-signal bandwidth ($2V_{PP}$): 400MHz
  - Slew rate: 1400V/µs
- Decompensated gain: 7V/V stable
- Low noise:
  - Input voltage noise: 2.2nV/√Hz
  - Input current noise: 3fA/√Hz (f = 10kHz)
- Input bias current: 4pA (typical)
- Low input capacitance:
  - Common-mode: 1.9pF
  - Differential mode: 0.5pF
- Low distortion (G = 7V/V, R_L = 1kΩ, V_O = $2V_{PP}$):
  - HD2, HD3 at 1MHz: –104dBc, –108dBc
  - HD2, HD3 at 50MHz: –57dBc, –72dBc
- Wide supply range: 6V to 13V
- Output swing: $8V_{PP}$ (V_S = 10V)
- Supply current: 27.7mA
- Shutdown supply current: 27µA
- Performance upgrade to OPA657

2 Applications

- Wideband transimpedance amplifier (TIA)
- Wafer scanning equipment
- Optical communication module
- High-speed data acquisition (DAQ)
- Active probe
- Optical time-domain reflectometry (OTDR)
- Test and measurement front-end
- Medical and chemical analyzer

3 Description

The OPA818 is a decompensated, voltage-feedback operational amplifier for high-speed and wide-dynamic-range applications. The OPA818 has a low-noise JFET input stage that combines high gain-bandwidth with a wide supply range from 6V to 13V. The fast slew rate (1400V/µs) provides high, large-signal bandwidth and low distortion. This amplifier is manufactured using TI's proprietary, high-speed, silicon-germanium (SiGe) process to achieve significant performance improvements over other high-speed, FET-input amplifiers.

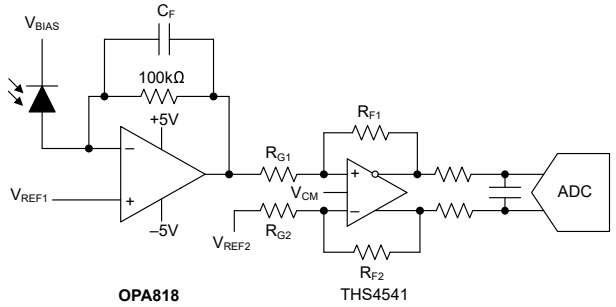
The OPA818 is an extremely versatile, wideband TIA photodiode amp for use in optical test and communication equipment, and many medical, scientific, and industrial instruments. The OPA818 showcases a 2.7GHz GBWP, low 2.4pF total input capacitance, and 2.2nV/√Hz input noise. The OPA818 achieves over 85MHz signal bandwidth in a TIA configuration with 20kΩ TIA gain (R_F) and 0.5pF photodiode capacitance (C_D) with wide output swings. The low-noise architecture with picoampere of input bias current is also an excellent choice for test and measurement applications. Though typically stable in gains ≥ 7V/V, the OPA818 is designed for use in applications with lower gains by applying noise-gain shaping techniques.

The OPA818 is available in an 5-pin SOT-23 package and an 8-lead WSON package with an exposed thermal pad for heat dissipation. This device is specified for operation over the industrial temperature range of –40°C to +85°C.

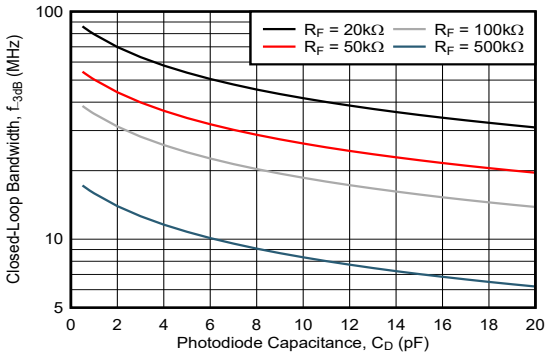
Package Information

PART NUMBER(1)	PACKAGE(2)	PACKAGE SIZE(3)
OPA818	DRG (WSON, 8)	3mm × 3mm
	DBV (SOT-23, 5)	2.9mm × 2.8mm

(1) See Section 4.
(2) For more information, see Section 11.
(3) The package size (length × width) is a nominal value and includes pins, where applicable.



High-Speed Optical Front-End



Photodiode Capacitance vs 3dB Bandwidth

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Device Comparison Table

DEVICE	V_S (V)	BW (MHz)	Input	SLEW RATE (V/µs)	VOLTAGE NOISE (nV/√ Hz)	MINIMUM STABLE GAIN (V/V)
OPA818	±6.5	2700	FET	1400	2.2	7
OPA657	±5	1600	FET	700	4.8	7
OPA656	±5	230	FET	290	7	1
OPA659	±6	350	FET	2550	8.9	1
LMH6629 (1)	±2.5	800 or 4000	BJT	530 or 1600	0.69	4 or 10
OPA858	±2.5	5500	CMOS	2000	2.5	7
THS4631	±15	210	FET	1000	7	1

(1) Pin selectable compensation.

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5 Pin Configuration and Functions

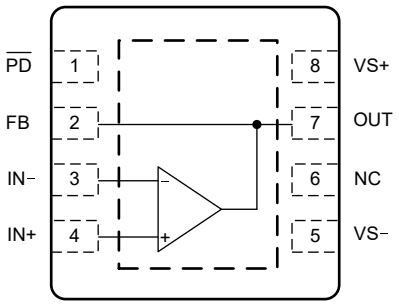

Figure 5-1. DRG Package, 8-Pin WSON With Thermal Pad (Top View)

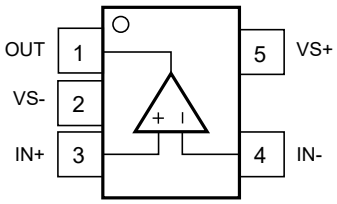

Figure 5-2. DBV Package, 5-Pin SOT-23 (Top View)

Table 5-1. Pin Functions

PIN			TYPE	DESCRIPTION
NAME	NO.			
	DRG (WSON)	DBV (SOT-23)		
FB	2	—	Output	Feedback resistor connection (optional)
IN–	3	4	Input	Inverting input
IN+	4	3	Input	Noninverting input
NC	6	—	—	No connect (no internal connection to die)
OUT	7	1	Output	Output of amplifier
$\overline{PD}$	1	—	Input	Power down (low = enable, high = disable). Internal 1MΩ pullup allows floating this pin.
VS–	5	2	Power	Negative power supply
VS+	8	5	Power	Positive power supply
Thermal pad	Thermal pad	—	—	Electrically isolated from the die substrate, but ESD diodes down-bonded to the thermal pad. Recommended connection to a heat-spreading plane, typically ground.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_S	Supply voltage, $(V_{S+}) – (V_{S–})$		13.5	V
$V_{IN,Diff}$	Differential input voltage		±5	V
V_{CM}	Common-mode input voltage	$V_{S–} – 0.5$	$V_{S–} + 10$	V
V_O	Output voltage	$V_{S–} – 0.5$	$V_{S+} + 0.5$	V
I_I	Continuous input current		±10	mA
I_O	Continuous output current(2)		25	mA
	Continuous current in feedback pin(2)		13	mA
T_J	Junction temperature		125	°C
T_A	Operating free-air temperature	–40	85	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* can cause permanent device damage. *Absolute maximum ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device cannot sustain damage, but cannot be fully functional. Operating the device in this manner affects device reliability, functionality, performance, and shorten the device lifetime.
(2) Long-term continuous current for electro-migration limits.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2500	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_S	Single-supply voltage	6	10	13	V
T_A	Ambient temperature	–40	25	85	°C

6.4 Thermal Information

THERMAL METRIC(1)		OPA818		UNIT
		DBV (SOT-23)	DRG (SON)	
		5 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	172	54.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	71.1	56.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	42.0	27.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	11.5	1.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	41.6	27.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	11.1	°C/W

(1) For information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.5 Electrical Characteristics

at T_A ≅ 25°C, V_{S+} = +5 V, $V_{S–}$ = –5 V, closed-loop gain (G) = 7 V/V, common-mode voltage (V_{CM}) = mid-supply, R_F = 301 Ω, and R_L = 100 Ω to mid-supply (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
AC PERFORMANCE							
SSBW	Small-signal bandwidth	V_O = 100 mV_{PP}			765		MHz
		G = 10, V_O = 100 mV_{PP}			430		
	Frequency response peaking				1.4		dB
LSBW	Large-signal bandwidth	V_O = 2 V_{PP}			400		MHz
GBWP	Gain-bandwidth product	G = 101 V/V, V_O = 100 mV_{PP}, R_F = 3.01 kΩ			2700		MHz
	Bandwidth for 0.1dB flatness	V_O = 100 mV_{PP}			100		MHz
SR	Slew rate (20%–80%)	V_O = 4 V step, rising and falling			1400		V/µs
		V_O = 4 V step, rising and falling, G = 10			1340		
t_r/t_f	Rise and fall time (10%–90%)	V_O = 100 mV step			0.52		ns
t_S	Settling time	V_O = 2 V step, to 0.1%			5.7		ns
	Overshoot and undershoot	V_O = 2 V step			7		%
	Overdrive recovery time	V_O = ($V_{S–}$ – 1 V) to (V_{S+} + 1 V)			25		ns
HD2	2nd harmonic distortion	V_O = 2 V_{PP}	f = 1 MHz		–84		dBc
			f = 10 MHz		–64		
			f = 50 MHz		–52		
			f = 10 MHz, R_L = 1 kΩ		–71		
HD3	3rd harmonic distortion	V_O = 2 V_{PP}	f = 1 MHz		–106		dBc
			f = 10 MHz, DRG package		–99		
			f = 10 MHz, DBV package		–95		
			f = 50 MHz		–74		
			f = 10 MHz, R_L = 1 kΩ		–82		
e_n	Input voltage noise	f ≥ 150 kHz			2.2		nV/√Hz
		1/f corner			15		kHz
i_n	Input current noise	f = 10 kHz			3		fA/√Hz
		f = 1 MHz			145		
Z_{CL}	Closed-loop output impedance	f = 10 MHz			0.2		Ω
DC PERFORMANCE							
A_{OL}	Open-loop voltage gain	f = dc, V_O = ±2 V		85	92		dB
V_{OS}	Input offset voltage				±0.35	±1.25	mV
		T_A = –40°C to +85°C				±1.8	
	Input offset voltage drift[1]	T_A = –40°C to +85°C			±3	±20	µV/°C
I_B	Input bias current[2]				±4	±25	pA
		T_A = –40°C to +85°C				700	
I_{OS}	Input offset current[2]				±1	±25	pA
CMRR	Common-mode rejection ratio	f = dc, V_{CM} = ±0.5 V		73	90		dB
		f = dc, V_{CM} = ±0.5 V, T_A = –40°C to +85°C		70			
	Internal feedback trace resistance	DRG package only, device turned off, OUT to FB pin resistance		0.8	1.2	1.7	Ω
INPUT							
	Common-mode input impedance				500 || 1.9		GΩ || pF
	Differential input impedance				500 || 0.5		GΩ || pF
	Most positive input voltage[3]			V_{S+} – 3.6	V_{S+} – 3.2		V

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6.5 Electrical Characteristics (continued)

at T_A ≅ 25°C, V_{S+} = +5 V, $V_{S–}$ = –5 V, closed-loop gain (G) = 7 V/V, common-mode voltage (V_{CM}) = mid-supply, R_F = 301 Ω, and R_L = 100 Ω to mid-supply (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Most negative input voltage(3)			$V_{S–}$	$V_{S–}$ + 0.25	V
	ΔV_{OS} at most positive input voltage(4)	V_{CM} = V_{S+} – 3.6 V		±0.03	±1	mV
		V_{CM} = V_{S+} – 3.6 V, T_A = -40°C to +85°C			±1.5	
	ΔV_{OS} at most negative input voltage(4)	V_{CM} = $V_{S–}$ + 0.25 V		±0.23	±1	mV
		V_{CM} = $V_{S–}$ + 0.25 V, T_A = -40°C to +85°C			±1.5	
OUTPUT						
V_{OH}	Output voltage swing high		V_{S+} – 1.2	V_{S+} – 1		V
		T_A = –40°C to +85°C	V_{S+} – 1.3			
		R_L = 1 kΩ	V_{S+} – 1	V_{S+} – 0.9		
		R_L = 1 kΩ, T_A = –40°C to +85°C	V_{S+} – 1.2			
V_{OL}	Output voltage swing low			$V_{S–}$ + 1.2	$V_{S–}$ + 1.33	V
		T_A = –40°C to +85°C			$V_{S–}$ + 1.4	
		R_L = 1 kΩ		$V_{S–}$ + 1.1	$V_{S–}$ + 1.2	
		R_L = 1 kΩ, T_A = –40°C to +85°C			$V_{S–}$ + 1.3	
I_{O_MAX}	Linear output drive	V_O = ±2.75 V, R_L to mid-supply = 50 Ω, [ΔV_{OS} from no-load V_{OS}] ≤ ±1 mV	±55			mA
		V_O = ±2.5 V, R_L to mid-supply = 50 Ω, [ΔV_{OS} from no-load V_{OS}] ≤ ±1 mV, T_A = –40°C to +85°C	±50			
I_{SC}	Output short-circuit current			±110		mA
POWER SUPPLY						
V_S	Single-supply operating range		6	10	13	V
I_Q	Quiescent current per channel	No load	26.5	27.7	29	mA
		No load, T_A = –40°C to +85°C	23		31.5	
	I_Q drift	No load, T_A = –40°C to +85°C		42		µA/°C
PSRR+	Positive power supply rejection ratio	ΔV_{S+} = ±0.25 V	75	95		dB
		ΔV_{S+} = ±0.25 V, T_A = –40°C to +85°C	70			
PSRR–	Negative power supply rejection ratio	$\Delta V_{S–}$ = ±0.25 V	80	94		dB
		$\Delta V_{S–}$ = ±0.25 V, T_A = –40°C to +85°C	74			
POWER DOWN						
V_{TH_EN}	Enable voltage threshold	Power on when $\overline{PD}$ > V_{TH_EN}, no load	V_{S+} – 1			V
V_{TH_DIS}	Disable voltage threshold	Power down when $\overline{PD}$ < V_{TH_DIS}, no load			V_{S+} – 3	V
	Power-down I_Q (VS+)	No load		27	40	µA
	$\overline{PD}$ pin bias current(2)	No load, $\overline{PD}$ = V_{S+}	–3	–2		µA
		No load, $\overline{PD}$ = $V_{S–}$		13	20	
	Turn-on time delay			125		ns
	Turn-off time delay			170		ns

(1) Input offset voltage drift and input bias current drift are average values calculated by taking data at the end-points, computing the difference, and dividing by the temperature range.
(2) Current is considered positive out of the pin. I_{OS} = I_{B+} – $I_{B–}$.
(3) Defined by ΔV_{OS} at most positive/negative input voltage specification
(4) ΔV_{OS} = |V_{OS} at specified V_{CM} – V_{OS} at 0 V V_{CM}|

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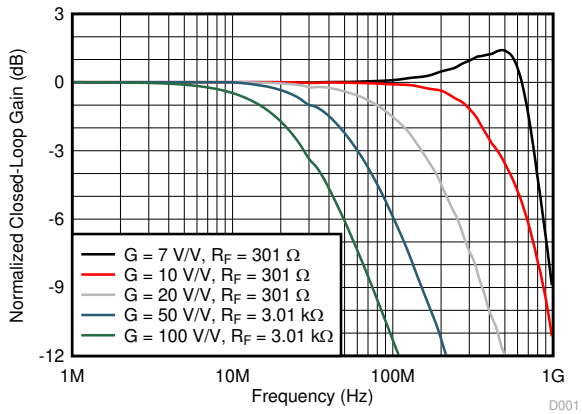
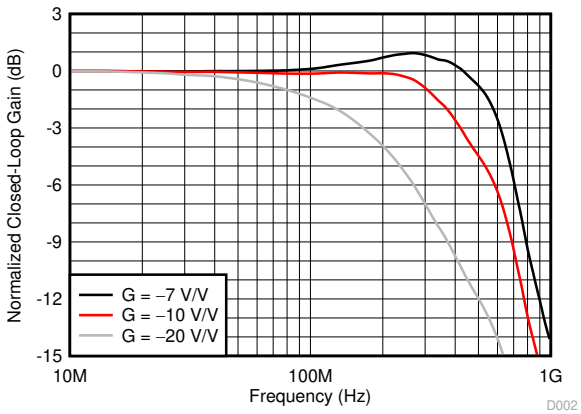
6.6 Typical Characteristics: V_S = ±5 V

at T_A ≅ 25°C, V_{S+} = +5 V, $V_{S–}$ = –5 V, closed-loop gain (G) = 7 V/V, V_{CM} = midsupply, R_F = 301 Ω, R_L = 100 Ω to midsupply, small-signal V_O = 100 mV_{PP}, and large-signal V_O = 2 V_{PP} (unless otherwise noted)



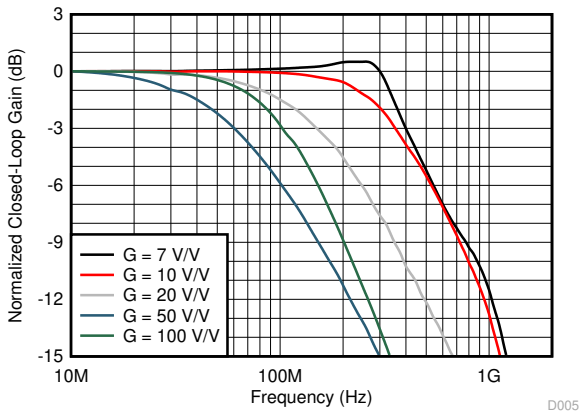
V_O = 100 mV_{PP}

Figure 6-1. Noninverting Small-Signal Frequency Response



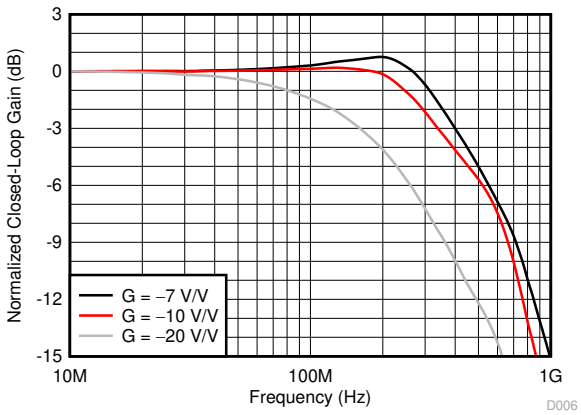
V_O = 100 mV_{PP}

Figure 6-2. Inverting Small-Signal Frequency Response



V_O = 2 V_{PP}

Figure 6-3. Noninverting Large-Signal Frequency Response



V_O = 2 V_{PP}

Figure 6-4. Inverting Large-Signal Frequency Response

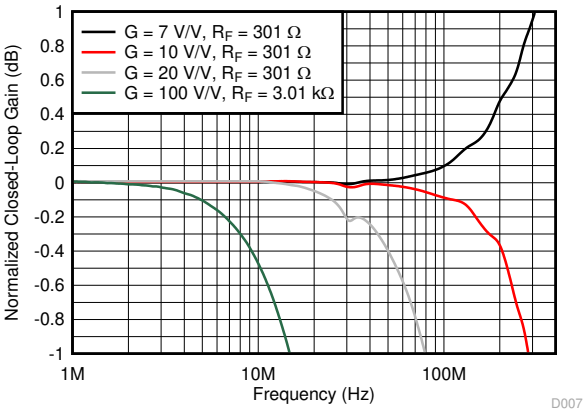


Figure 6-5. Gain Flatness vs Frequency

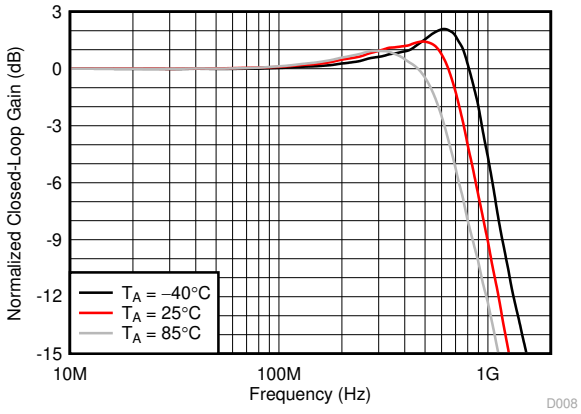


Figure 6-6. Noninverting Small-Signal Frequency Response Over Temperature

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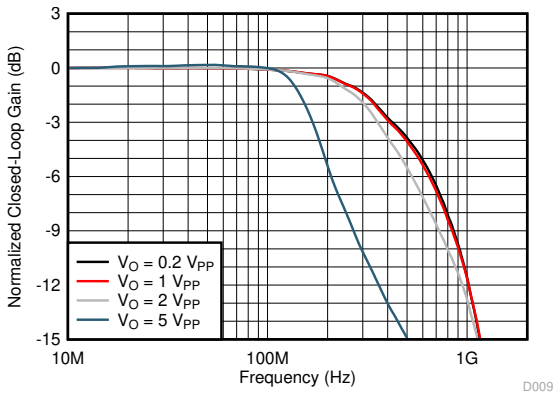
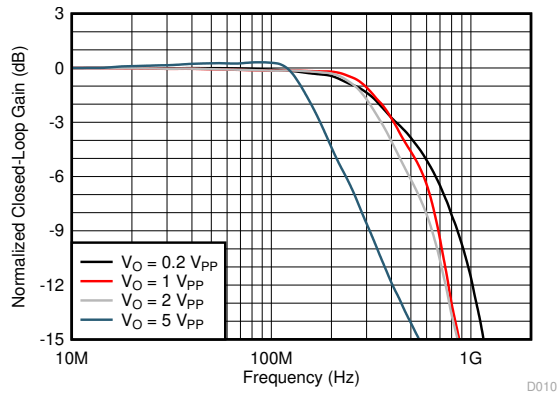
6.6 Typical Characteristics: V_S = ±5 V (continued)

at T_A ≅ 25°C, V_{S+} = +5 V, $V_{S–}$ = –5 V, closed-loop gain (G) = 7 V/V, V_{CM} = midsupply, R_F = 301 Ω, R_L = 100 Ω to midsupply, small-signal V_O = 100 mV_{PP}, and large-signal V_O = 2 V_{PP} (unless otherwise noted)



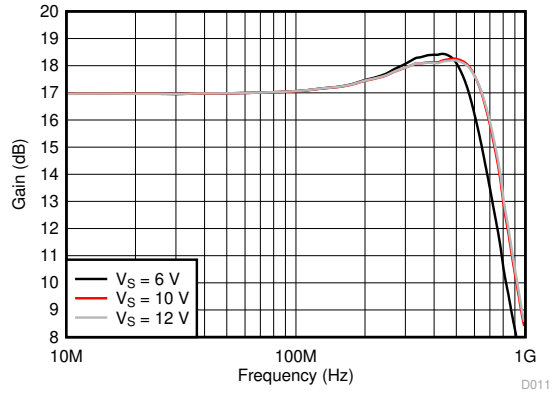
G = 10 V/V

Figure 6-7. Noninverting Frequency Response Over Output Swing



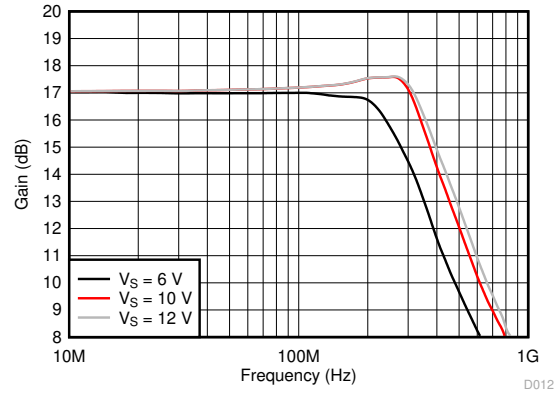
G = –10 V/V

Figure 6-8. Inverting Frequency Response Over Output Swing



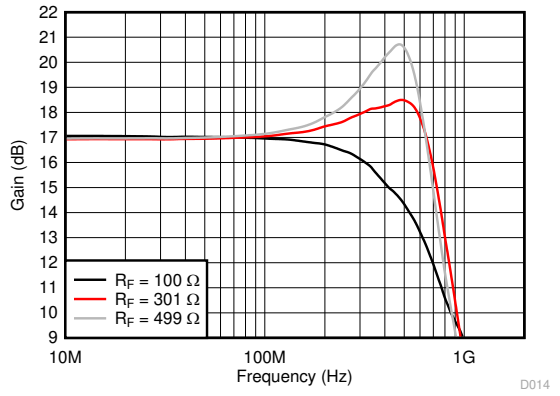
V_O = 100 mV_{PP}

Figure 6-9. Noninverting Small-Signal Frequency Response Over Voltage Supply



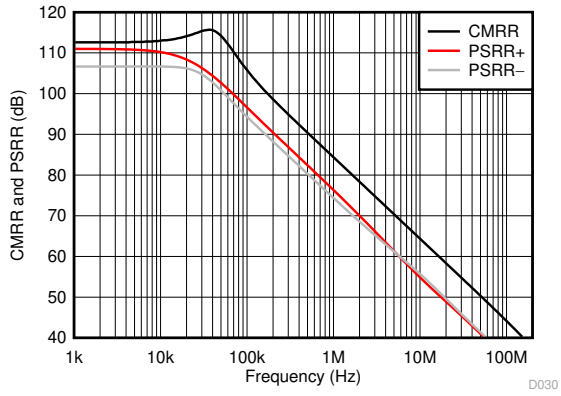
V_O = 2 V_{PP}

Figure 6-10. Noninverting Large-Signal Frequency Response Over Voltage Supply



V_O = 100 mV_{PP}

Figure 6-11. Noninverting Small-Signal Frequency Response Over R_F



Simulation

Figure 6-12. Common-Mode and Power-Supply Rejection Ratio vs Frequency

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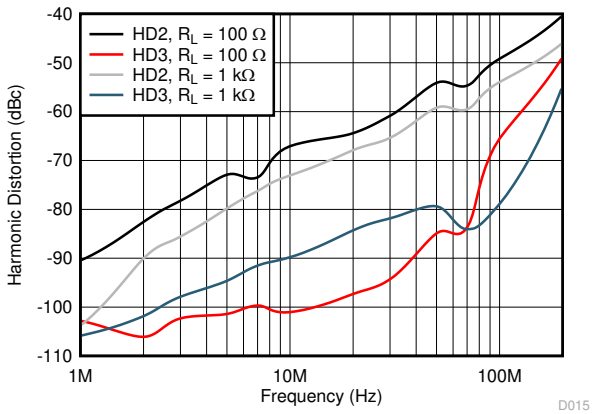
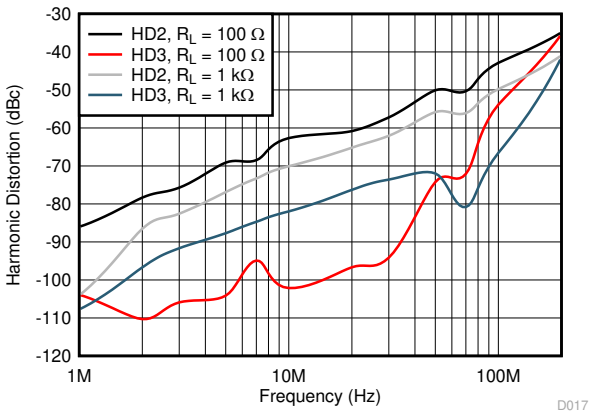
6.6 Typical Characteristics: V_S = ±5 V (continued)

at T_A ≅ 25°C, V_{S+} = +5 V, $V_{S–}$ = –5 V, closed-loop gain (G) = 7 V/V, V_{CM} = midsupply, R_F = 301 Ω, R_L = 100 Ω to midsupply, small-signal V_O = 100 mV_{PP}, and large-signal V_O = 2 V_{PP} (unless otherwise noted)



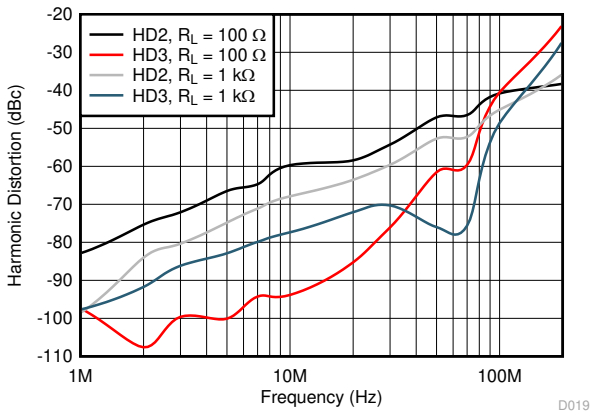
V_O = 1 V_{PP}

Figure 6-13. Harmonic Distortion vs Frequency Over R_L



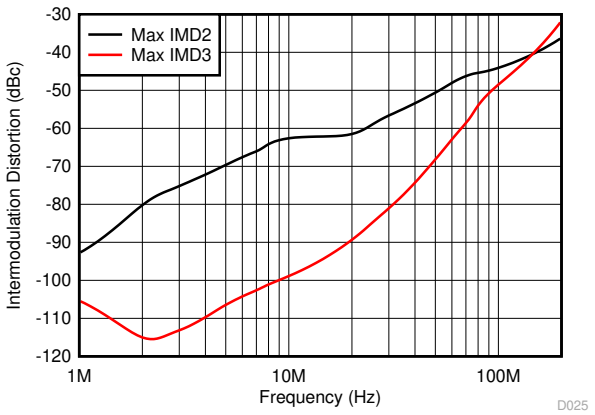
V_O = 2 V_{PP}

Figure 6-14. Harmonic Distortion vs Frequency Over R_L



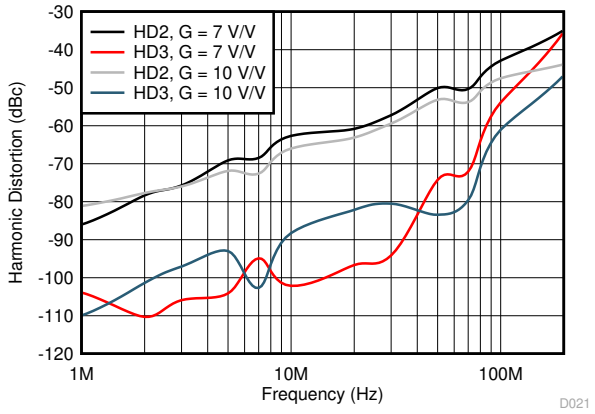
V_O = 4 V_{PP}

Figure 6-15. Harmonic Distortion vs Frequency Over R_L



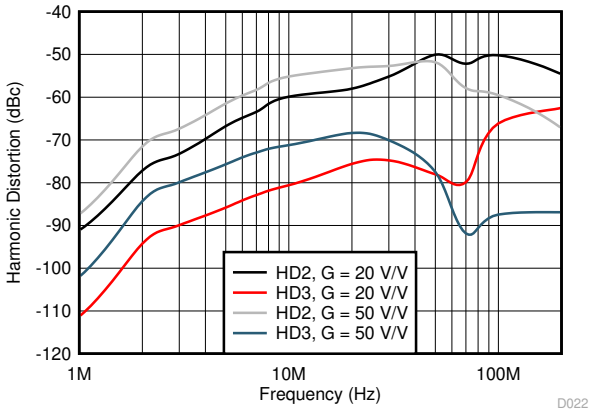
V_O = 2 V_{PP} per tone, ±100-kHz tone spacing

Figure 6-16. Inter Modulation Distortion vs Frequency



V_O = 2 V_{PP}, G = 7 V/V and 10 V/V

Figure 6-17. Harmonic Distortion vs Frequency Over Gain



V_O = 2 V_{PP}, G = 20 V/V and 50 V/V,
flattening HD at higher frequencies due to bandwidth roll-off

Figure 6-18. Harmonic Distortion vs Frequency Over Gain

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6.6 Typical Characteristics: V_S = ±5 V (continued)

at T_A ≅ 25°C, V_{S+} = +5 V, $V_{S–}$ = –5 V, closed-loop gain (G) = 7 V/V, V_{CM} = midsupply, R_F = 301 Ω, R_L = 100 Ω to midsupply, small-signal V_O = 100 mV_{PP}, and large-signal V_O = 2 V_{PP} (unless otherwise noted)

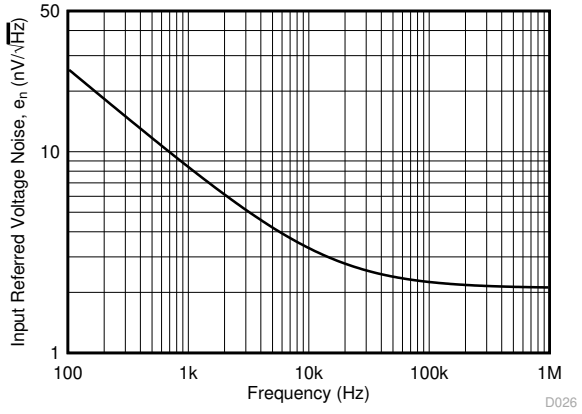

Figure 6-19. Voltage Noise Density vs Frequency

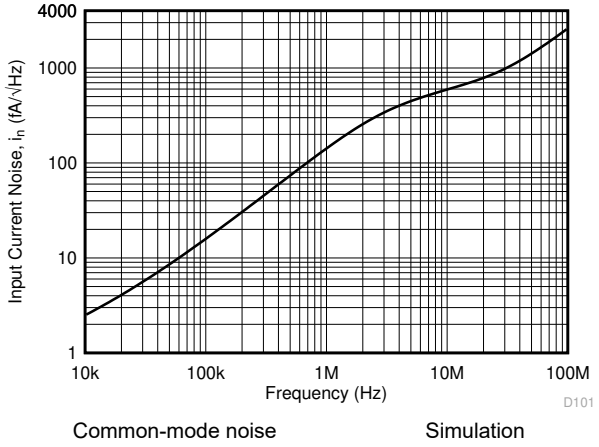

Figure 6-20. Current Noise Density vs Frequency

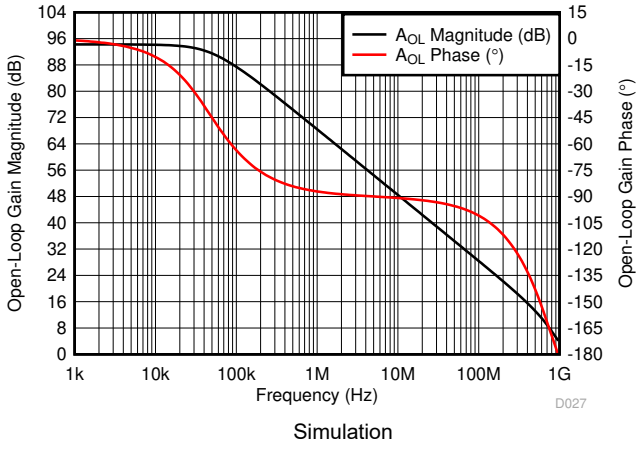

Figure 6-21. Open-Loop Gain Magnitude and Phase vs Frequency

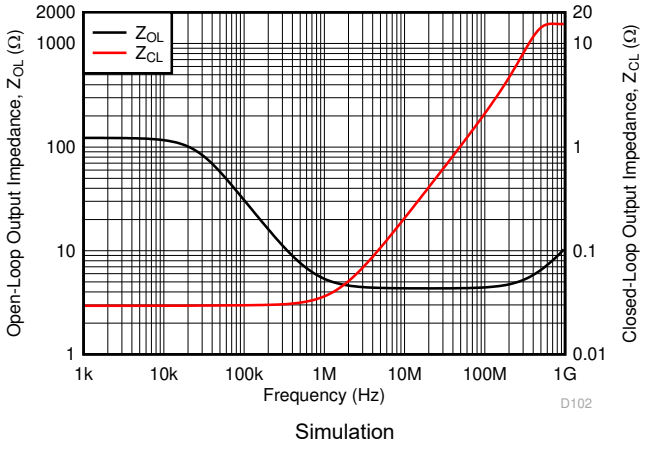

Figure 6-22. Open-Loop and Closed-Loop Output Impedance vs Frequency

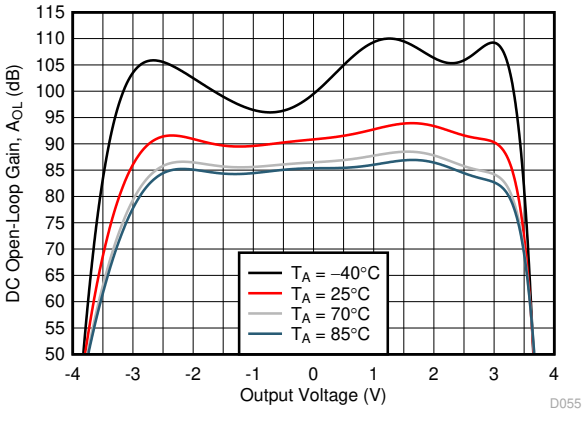

Figure 6-23. DC Open-Loop Gain vs Output Voltage

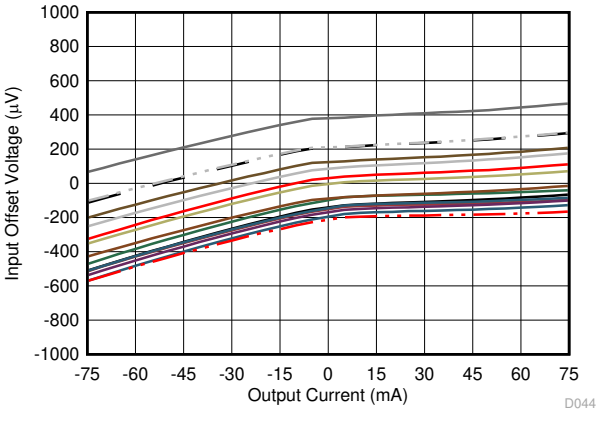

Figure 6-24. Input Offset Voltage vs Output Current

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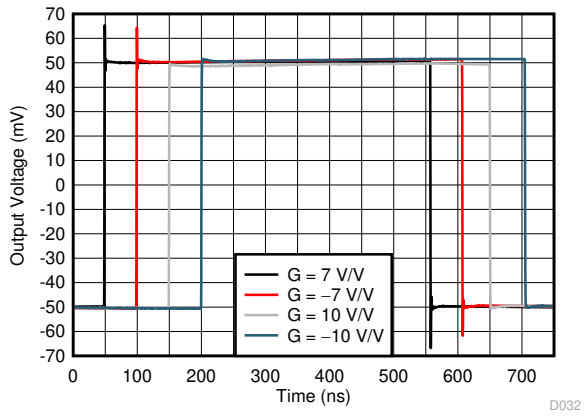
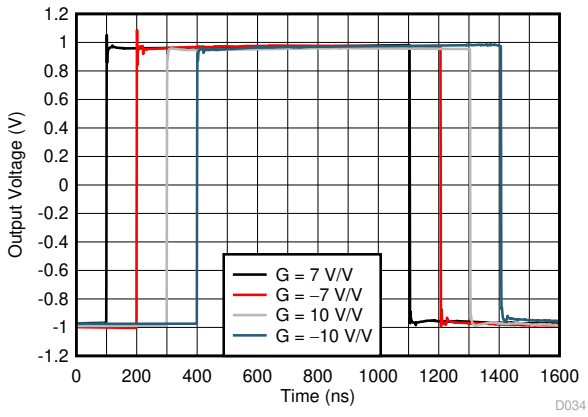
6.6 Typical Characteristics: V_S = ±5 V (continued)

at T_A ≅ 25°C, V_{S+} = +5 V, $V_{S–}$ = –5 V, closed-loop gain (G) = 7 V/V, V_{CM} = midsupply, R_F = 301 Ω, R_L = 100 Ω to midsupply, small-signal V_O = 100 mV_{PP}, and large-signal V_O = 2 V_{PP} (unless otherwise noted)



V_O = 100-mV step

Figure 6-25. Small-Signal Pulse Response



V_O = 2-V step

Figure 6-26. Large-Signal Pulse Response

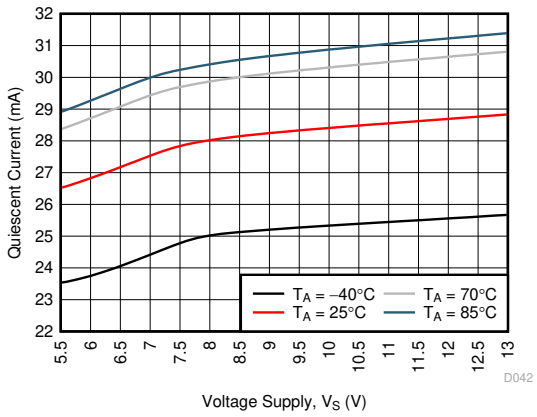


Figure 6-27. Quiescent Current vs Voltage Supply Over Temperature

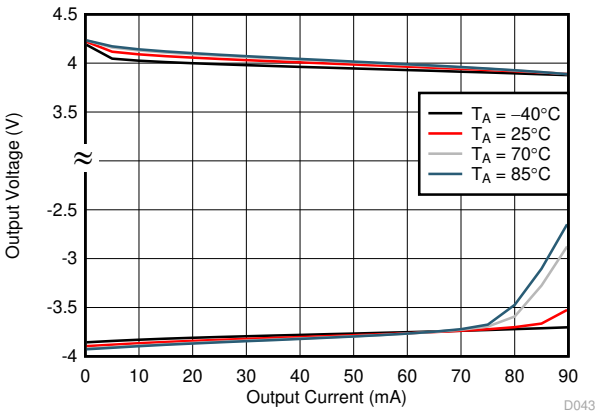


Figure 6-28. Output Voltage vs Output Current Over Temperature

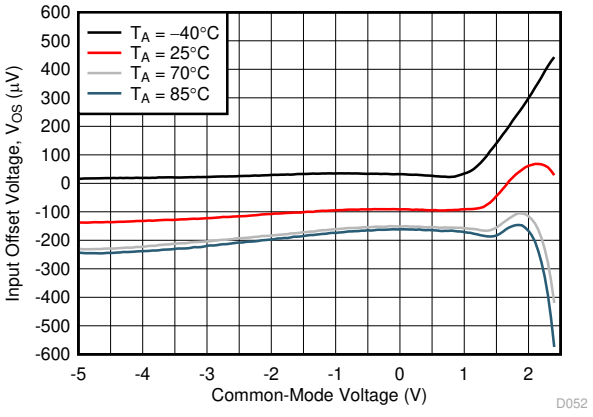


Figure 6-29. Input Offset Voltage vs Common-Mode Voltage Over Temperature

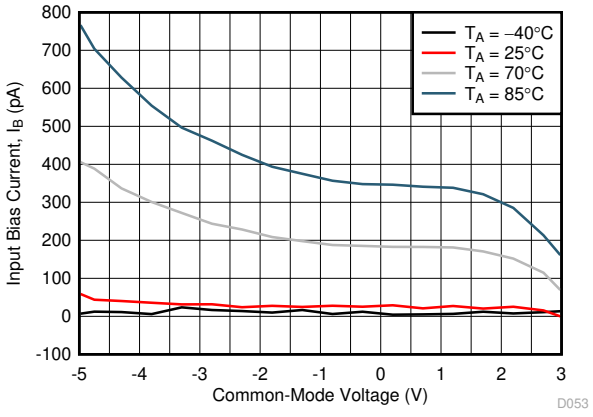


Figure 6-30. Input Bias Current vs Common-Mode Voltage Over Temperature

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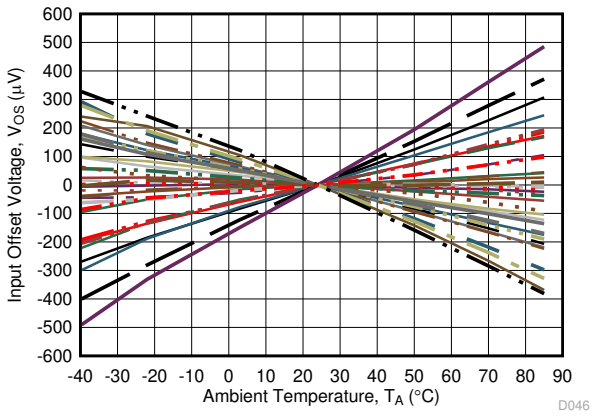
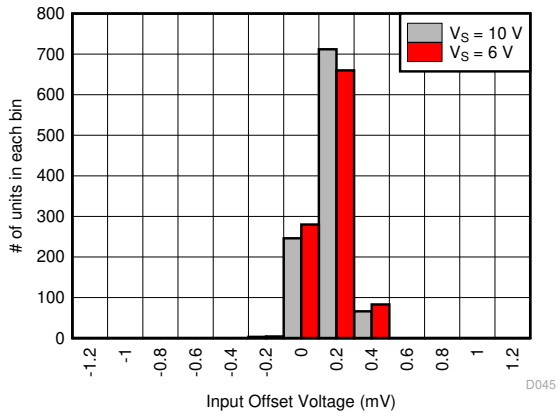
6.6 Typical Characteristics: V_S = ±5 V (continued)

at T_A ≅ 25°C, V_{S+} = +5 V, $V_{S–}$ = –5 V, closed-loop gain (G) = 7 V/V, V_{CM} = midsupply, R_F = 301 Ω, R_L = 100 Ω to midsupply, small-signal V_O = 100 mV_{PP}, and large-signal V_O = 2 V_{PP} (unless otherwise noted)



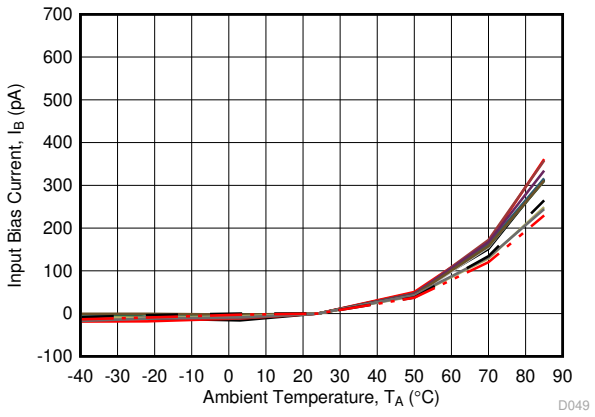
35 units, delta from 25°C V_{OS}

Figure 6-31. Input Offset Voltage vs Temperature



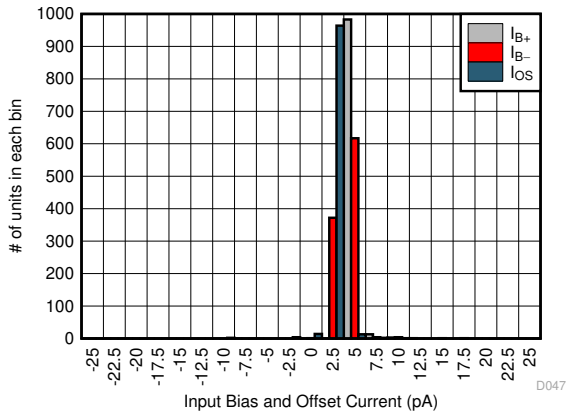
1000 units at each V_S

Figure 6-32. Input Offset Voltage Histogram



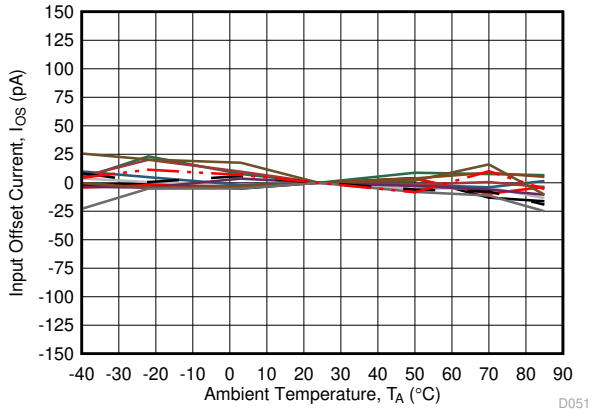
12 units, delta from 25°C I_B

Figure 6-33. Input Bias Current vs Temperature



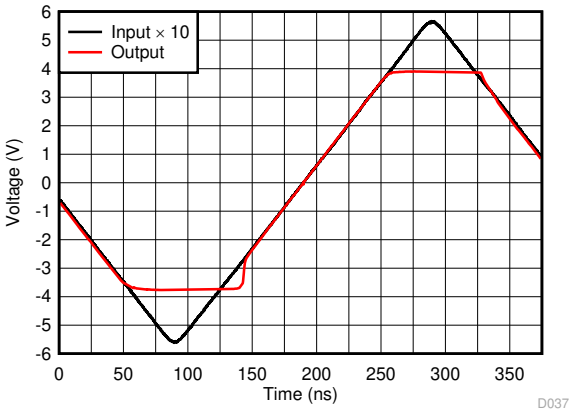
1000 units

Figure 6-34. Input Bias and Offset Current Histogram



12 units, delta from 25°C I_{OS}

Figure 6-35. Input Offset Current vs Temperature



G = 10 V/V

Figure 6-36. Output Overdrive Recovery

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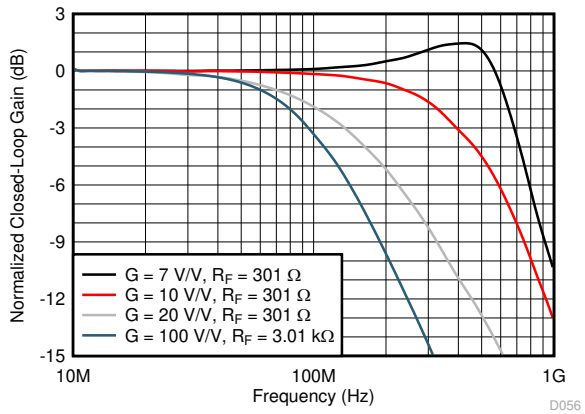
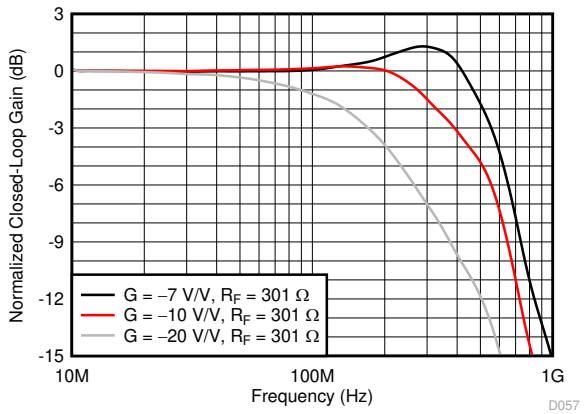
6.7 Typical Characteristics: V_S = 6 V

at T_A ≅ 25°C, V_{S+} = +4 V, $V_{S–}$ = –2 V, closed-loop gain (G) = 7 V/V, V_{CM} = midsupply, R_F = 301 Ω, R_L = 100 Ω to midsupply, small-signal V_O = 100 mV_{PP}, and large-signal V_O = 1 V_{PP} (unless otherwise noted)



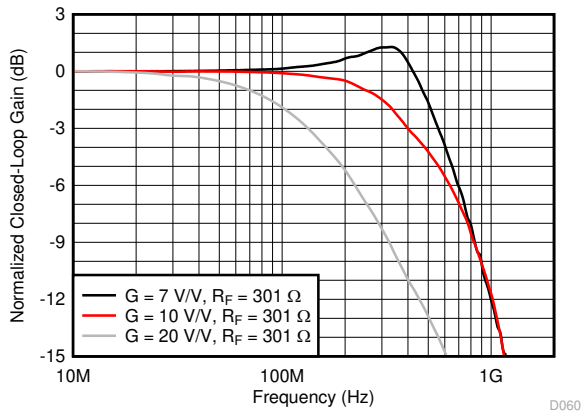
V_O = 100 mV_{PP}

Figure 6-37. Noninverting Small-Signal Frequency Response



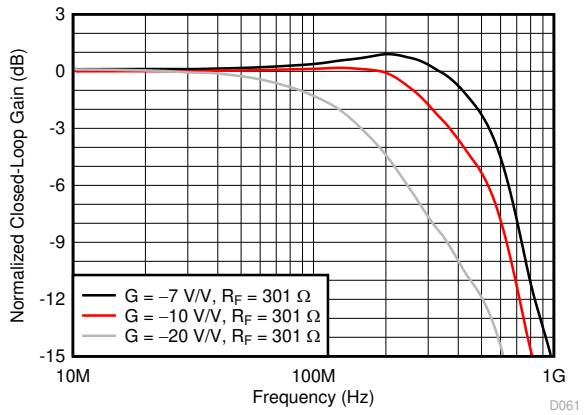
V_O = 100 mV_{PP}

Figure 6-38. Inverting Small-Signal Frequency Response



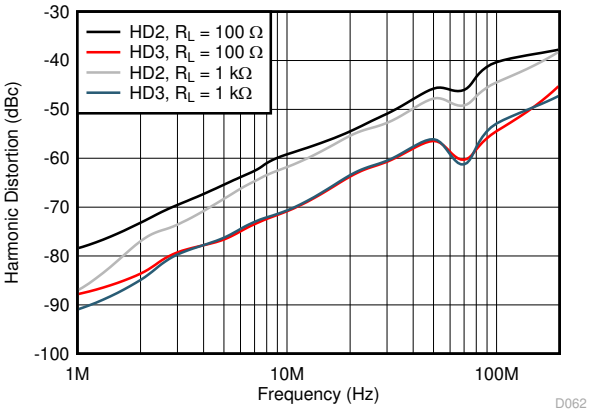
V_O = 1 V_{PP}

Figure 6-39. Noninverting Large-Signal Frequency Response



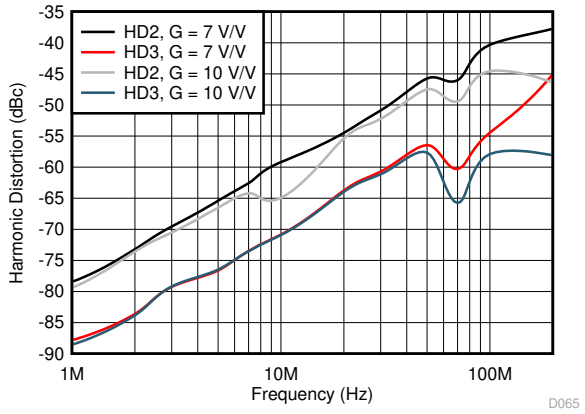
V_O = 1 V_{PP}

Figure 6-40. Inverting Large-Signal Frequency Response



V_O = 1 V_{PP}

Figure 6-41. Harmonic Distortion vs Frequency Over R_L



V_O = 1 V_{PP}

Figure 6-42. Harmonic Distortion vs Frequency Over Gain

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7 Detailed Description

7.1 Overview

The OPA818 is a 13-V supply, 2.7-GHz gain-bandwidth product (GBWP), voltage-feedback operational amplifier (op amp) featuring a 2.2-nV/√Hz, low-noise, JFET input stage. The OPA818 is decompensated to be typically stable in gains ≥ 7 V/V. The decompensated architecture allows for a favorable tradeoff of low quiescent current for a very high GBWP and low distortion performance in high-gain applications. The high voltage capability combined with a 1400-V/µs slew rate enables applications that require wide output swings (10 V_{PP} at V_S = 12 V) for high-frequency signals. Such applications include optical front ends, test and measurement, and medical systems. The low noise JFET input with pico amperes of bias current makes this device particularly attractive for high TIA gain applications and test and measurement front ends. The OPA818 also features a power-down mode that disables the core amplifier for power savings.

The OPA818 is built using TI's proprietary high-voltage, high-speed, complementary, bipolar SiGe process.

7.2 Functional Block Diagram

The OPA818 is a conventional voltage-feedback op amp with two high-impedance inputs and a low-impedance output. Standard amplifier configurations are supported. Figure 7-1 and Figure 7-2 show two basic configurations. The dc operating point for each configuration is level-shifted by the reference voltage (V_{REF}), which is typically set to midsupply in single-supply operation. V_{REF} is typically set to ground in split-supply applications.

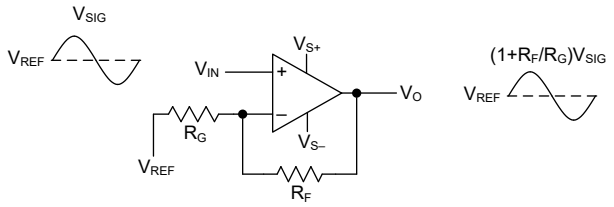

Figure 7-1. Noninverting Amplifier

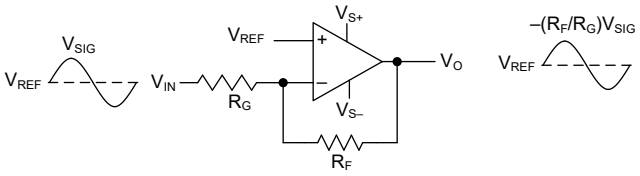

Figure 7-2. Inverting Amplifier

7.3 Feature Description

7.3.1 Input and ESD Protection

The OPA818 is built using a very high speed complementary bipolar process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in Section 6.1. Figure 7-3 shows how all the device pins are protected with internal ESD protection diodes.

These diodes also provide moderate protection to input overdrive voltages beyond the supplies. The protection diodes typically support 10mA continuous current. Where higher currents are possible (for example, in systems with ±12V supply parts driving into the OPA818), add current limiting series resistors in series with the two inputs to limit the current. Keep these resistor values as low as possible because high values degrade both noise performance and frequency response. There are no back-to-back ESD diodes between V_{IN+} and $V_{IN–}$. As a result, the differential input voltage between V_{IN+} and $V_{IN–}$ is entirely absorbed by the V_{GS} of the input JFET differential pair; do not exceed the voltage ratings in Section 6.1.

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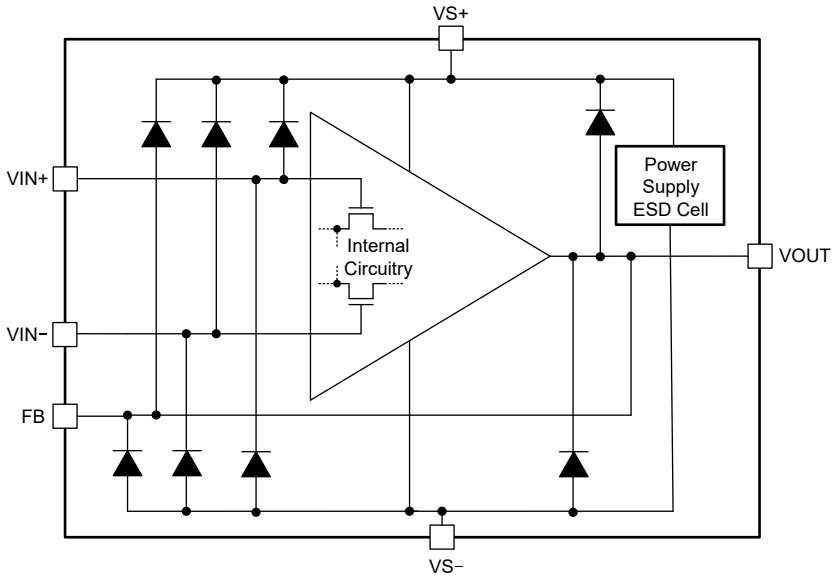

Figure 7-3. Internal ESD Protection

7.3.2 Feedback Pin

For high-speed analog design, minimizing parasitic capacitance and inductance is critical to get the best performance from a high-speed amplifier such as the OPA818. Parasitics are especially detrimental in the feedback path and at the inverting input. Parasitics result in undesired poles and zeroes in the feedback that potentially reduce phase margin or cause instability. Techniques used to correct for this phase margin reduction often result in reduced application bandwidth. To keep system engineers from making these tradeoff choices and to simplify the printed circuit board (PCB) layout, the OPA818 features a feedback pin (FB) pin on the same side as the inverting input pin (IN–). Figure 7-4 shows how this configuration allows for a very short feedback resistor (R_F) connection between the FB and the IN– pins, thus minimizing parasitics with minimal PCB design effort. Internally, the FB pin is connected to VOUT through metal routing on the silicon. As a result of the fixed metal sizing of this connection, the FB pin has limited current carrying capability; therefore, adhere to Section 6.1 for continuous operation.

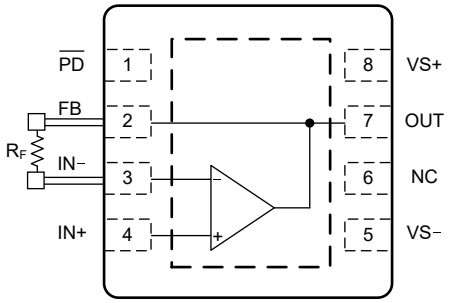

Figure 7-4. R_F Connection Between FB and IN– Pins

7.3.3 Decompensated Architecture With Wide Gain-Bandwidth Product

Figure 7-5 shows the open-loop gain and phase response of the OPA818. The GBWP of an op amp is measured in the 20-dB/decade constant slope region of the A_{OL} magnitude plot. The open-loop gain of 60 dB for the OPA818 is along this 20-dB/decade slope and the corresponding frequency intercept is at 2.7 MHz. Converting 60 dB to linear units (1000 V/V) and multiplying by the 2.7-MHz frequency intercept gives the GBWP of the OPA818 as 2.7 GHz. The A_{OL} Bode plot shows that the second pole in the A_{OL} response occurs before the A_{OL} magnitude drops to less than 0 dB (1 V/V). This result shows a phase change of more than 180° at 0 dB A_{OL}, indicating that the amplifier can not be stable in a gain of 1 V/V. Amplifiers, such as the OPA818, that are not

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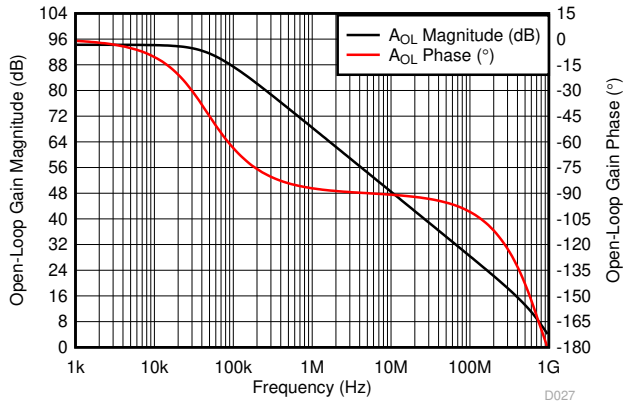
unity-gain stable are referred to as decompensated amplifiers. The decompensated architecture typically allows for higher GBWP, higher slew rate, and lower noise compared to a unity-gain stable amplifier with equivalent quiescent current. The additional advantage of the decompensated amplifier is better distortion performance at higher frequencies in high-gain applications for comparable quiescent current to a unity-gain stable amplifier.

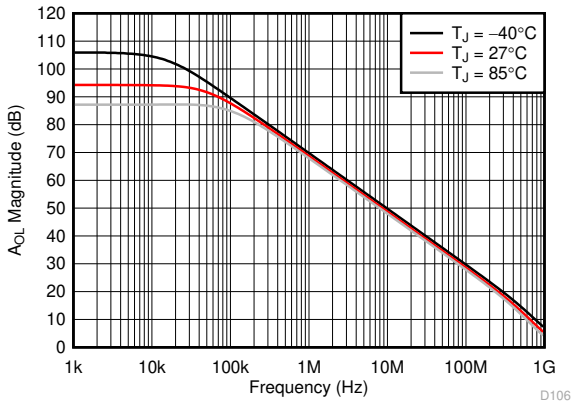
The OPA818 is stable in a noise gain of 7 V/V (16.9 dB) or greater in conventional gain circuits (see Figure 7-1 and Figure 7-2). In the noise gain of 7 V/V, the OPA818 has 790 MHz of SSBW with approximately 50° phase margin.

The high GBWP and low voltage and current noise make the OPA818 an excellent amplifier choice for wideband, moderate-to-high transimpedance-gain applications. Transimpedance gains of 50 kΩ or greater benefit from the low-current-noise JFET input. In a typical transimpedance-amplifier (TIA) circuit (see also Figure 8-2), a unity-gain stable amplifier is not required. At low frequencies, the noise gain of the TIA is 0 dB (1 V/V), and at high frequencies, the noise gain is set by the ratio of the total input capacitance (C_{TOT}) and the feedback capacitance (C_F). To maximize TIA closed-loop bandwidth, the feedback capacitance is typically less than the total input capacitance. This configuration results in a ratio of total input capacitance to feedback capacitance greater than 1, which is ultimately the noise gain of the TIA at higher frequencies. The blog series, *What you need to know about transimpedance amplifiers – part 1* and *What you need to know about transimpedance amplifiers – part 2* describe TIA compensation techniques in greater detail.



R_L = 100 Ω Simulation

Figure 7-5. Open-Loop Gain Magnitude and Phase vs Frequency



R_L = 100 Ω Simulation

Figure 7-6. Open-Loop Gain Magnitude vs Temperature

7.3.4 Low Input Capacitance

Often, the two primary considerations for TIA applications are maximizing the TIA closed-loop bandwidth and minimizing the total output noise to maximize the signal-to-noise ratio (SNR). The total input capacitance (C_{TOT}) of the TIA circuit causes a zero in the noise gain in combination with the transimpedance gain (feedback resistor, R_F) at frequency 1 / ($2\pi R_F C_{TOT}$). For a fixed R_F, this zero is at a lower frequency for a higher C_{TOT}, thus increasing the noise gain at the lower frequency. This configuration results in lower equivalent closed-loop bandwidth and higher total output noise compared to a lower C_{TOT}. The OPA818 features a low input capacitance (2.4 pF combined common-mode and differential). The OPA818 also provides high closed-loop bandwidth at low total output noise, or provides the flexibility to choose a photodiode with relatively higher capacitance for the TIA application. The C_{TOT} includes the input capacitance of the amplifier, the photodiode capacitance, and the PCB parasitic capacitance at the inverting input.

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7.4 Device Functional Modes

7.4.1 Split-Supply Operation (+4/–2 V to ±6.5 V)

In typical split-supply operation, the midpoint between the power rails is ground. The midpoint at ground in a split-supply configuration is a valid operating condition for the OPA818 when using symmetric supply voltages that are greater than or equal to ±4 V. This configuration facilitates interfacing the OPA818 with common lab equipment that have inputs and outputs referenced to ground, such as signal generators, network analyzers, oscilloscopes, and spectrum analyzers. However, when using split-supply voltages less than ±4 V, ensure that the input common-mode range is not violated. Be aware that the typical input common-mode range of the OPA818 includes $V_{S–}$ and extends up to 3.2 V from V_{S+}. For example, when using ±3 V supplies, ensure that the input common-mode voltage of the signal is typically 3.2 V from V_{S+} and 3.6 V from V_{S+}, per the maximum specified input common-mode range. Ground is not included in the input common-mode range with ±3 V supplies, and results in erroneous operation if the input signal has ground as the midpoint. To prevent this issue, use +4/–2 V supplies.

7.4.2 Single-Supply Operation (6 V to 13 V)

Many newer systems use single power supply to improve efficiency and reduce the cost of the extra power supply. The OPA818 is designed for use with split-supply configuration. However, the device is available for use with a single-supply with no change in performance, as long as the input and output are biased within the linear operation of the device. To change the circuit from split supply to single supply, level shift all the voltages to mid-supply using V_{REF}. Give additional consideration to the input common-mode range to not violate requirements when operating with supplies less than 8 V. One of the advantages of configuring an amplifier for single-supply operation is that the effects of –PSRR are minimized because the low supply rail is grounded.

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Wideband, Noninverting Operation

The OPA818 provides a unique combination of high GBWP, low-input voltage noise, and the dc precision of a trimmed JFET-input stage to provide an exceptionally high input impedance for a voltage-feedback amplifier. The high GBWP of 2.7 GHz is used to either deliver high-signal bandwidths at high gains, or to extend the achievable bandwidth or gain in photodiode-transimpedance applications. To achieve the full performance of the OPA818, pay careful attention to printed circuit board (PCB) layout and component selection; see also the following sections of this data sheet.

Figure 8-1 shows the noninverting gain of +7 V/V circuit used as the basis for most of the *Typical Characteristics: V_S = ±5 V*. Most of the curves are characterized using signal sources with 50-Ω driving impedance, and with measurement equipment presenting a 50-Ω load impedance. In Figure 8-1, the 49.9-Ω shunt resistor at the V_{IN} terminal matches the source impedance of the test generator, while the 49.9-Ω series resistor at the V_O terminal provides a matching resistor for the measurement equipment load. Generally, data-sheet voltage-swing specifications are at the output pin (V_O in Figure 8-1) while output power specifications are at the matched 50-Ω load. The total 100-Ω load at the output combined with the 350-Ω total feedback network load, presents the OPA818 with an effective output load of 78 Ω for the circuit of Figure 8-1.

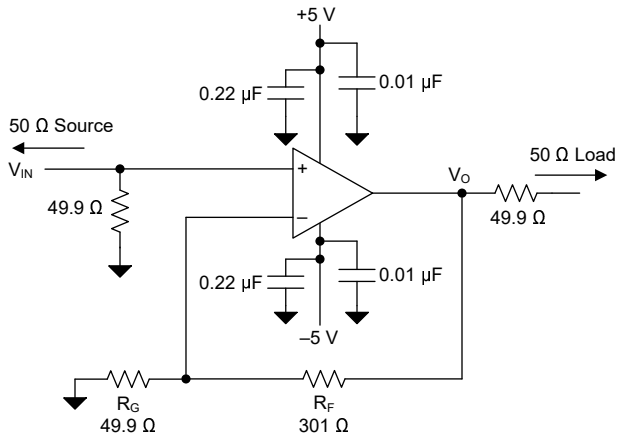

Figure 8-1. Noninverting G = +7 V/V Configuration and Test Circuit

Voltage-feedback operational amplifiers, unlike current feedback products, use a wide range of resistor values to set gain. To retain a controlled frequency response for the noninverting voltage amplifier of Figure 8-1, ensure that the parallel combination of R_F || R_G is less than 50 Ω. In the noninverting configuration, the parallel combination of R_F || R_G forms a pole with the parasitic input capacitance at the inverting node of the OPA818 (including layout parasitics). For best performance, set this pole to a frequency greater than the closed-loop bandwidth for the OPA818.

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8.1.2 Wideband, Transimpedance Design Using the OPA818

With high GBWP, low input voltage and current noise, and low input capacitance, the OPA818 design is optimized for wideband, low-noise transimpedance applications. The high-voltage capability allows greater flexibility of supply voltages along with wider output voltage swings. Figure 8-2 shows an example circuit of a typical photodiode amplifier circuit. Generally the photodiode is reverse biased in a TIA application so the photodiode current in the circuit of Figure 8-2 flows into the op amp feedback loop resulting in an output voltage that reduces from V_{REF} with increasing photodiode current. In this type of configuration and depending on the application needs, V_{REF} can be biased closer to V_{S+} to achieve the desired output swing. Do not violate the input common-mode range requirements when the V_{REF} bias is used.

The key design elements that determine the closed-loop bandwidth, f_{-3dB}, of the circuit are:

1. The op amp GBWP
2. The transimpedance gain, R_F
3. The total input capacitance, C_{TOT}, that includes photodiode capacitance, input capacitance of the amplifier (common-mode and differential capacitance), and PCB parasitic capacitance

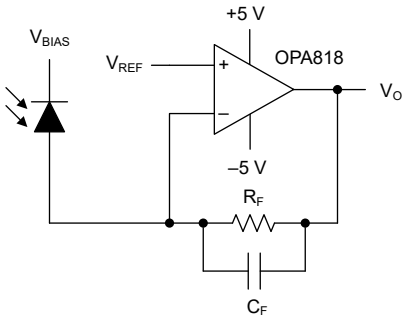

Figure 8-2. Wideband, Low-Noise, Transimpedance Amplifier

Equation 1 shows the relationship between the previously mentioned three elements for a Butterworth response.

$$f_{-3dB} = \sqrt{\frac{GBWP}{2\pi R_F C_{TOT}}} \quad (1)$$

The feedback resistance, R_F and the total input capacitance, C_{TOT} cause a zero in the noise gain that results in instability if left uncompensated. To counteract the effect of the zero, a pole is inserted in the noise gain by adding the feedback capacitor, C_F. The *Transimpedance Considerations for High-Speed Amplifiers* application report discusses theories and equations that show how to compensate a transimpedance amplifier for a particular gain and input capacitance. The bandwidth and compensation equations from the application report are available in an Excel™ calculator. *What You Need To Know About Transimpedance Amplifiers – Part 1* provides a link to the calculator. The details of maximizing the dynamic range of TIA front-ends (see *High-Speed Optical Front-End*) that uses voltages V_{REF1} and V_{REF2} are provided in the *Maximizing the dynamic range of analog TIA front-end application note*.

8.2 Typical Applications

8.2.1 High-Bandwidth, 100-kΩ Gain Transimpedance Design

The high GBWP and low input voltage and current noise make the OPA818 an excellent wideband transimpedance amplifier for moderate-to-high transimpedance gains.

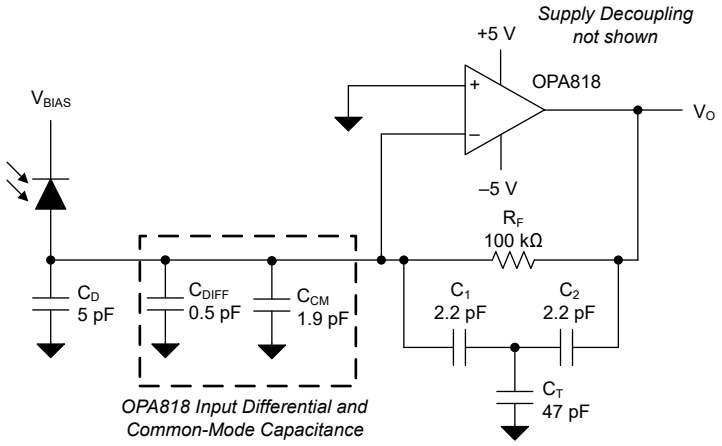

Figure 8-3. Wideband, High-Sensitivity, Transimpedance Amplifier

8.2.1.1 Design Requirements

Design a high-bandwidth, high-transimpedance-gain amplifier with the design requirements shown in Table 8-1.

Table 8-1. Design Requirements

TARGET BANDWIDTH (MHz)	TRANSIMPEDANCE GAIN (kΩ)	PHOTODIODE CAPACITANCE (pF)
24	100	5

8.2.1.2 Detailed Design Procedure

Designs that require high bandwidth from a large area detector with relatively high transimpedance gain benefit from the low input voltage noise of the OPA818. This input voltage noise is peaked up over frequency by the diode source capacitance, and in many cases, becomes the limiting factor to input sensitivity. Figure 8-3 shows the transimpedance circuit with the parameters defined in Section 8.2.1.1. To use the Excel calculator available in *What You Need To Know About Transimpedance Amplifiers – Part 1* to help with the component selection, determine the total input capacitance, C_{TOT}. In the calculator, C_{TOT} is referred to as C_{IN}. C_{TOT} is the sum of C_D, C_{DIFF}, and C_{CM}, which is 7.4 pF. Using this value of C_{TOT}, the targeted closed-loop bandwidth (f_{-3dB}) of 24 MHz, and the transimpedance gain of 100 kΩ results in the need for an amplifier with approximately 2.68 GHz GBWP and a feedback capacitance (C_F) of 0.092 pF. Table 8-2 shows the calculator results. These results are for a Butterworth response with a Q = 0.707 and a phase margin of approximately 65°, which corresponds to 4.3% overshoot.

Table 8-2. Results of Inputting Design Parameters in the TIA Calculator

Calculator II		
Closed-loop TIA bandwidth (f_{-3dB})	24.00	MHz
Feedback resistance (R_F)	100	kΩ
Input capacitance (C_{IN})	7.40	pF
Op-amp gain bandwidth product (GBWP)	2678.14	MHz
Feedback capacitance (C_F)	0.092	pF

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With a 2.7-GHz GBWP, the OPA818 is an excellent choice for the design requirements. A challenge with the calculated component results is practically realizing a 0.092-pF capacitor. Such a small capacitor is realized by using a capacitive tee network formed by C_1, C_2, and C_T (see Figure 8-3). The equivalent capacitance, C_{EQ}, of the tee network is given by Equation 2:

$$C_{EQ} = \frac{C_1 \times C_2}{C_1 + C_2 + C_T} \quad (2)$$

The tee network forms a capacitive attenuator from input to output with C_1 and C_T, and from output to input with C_2 and C_T. With the value of C_T being higher than C_1 or C_2, only a fraction of the output signal is seen by C_1. This network results in a much smaller shunting current provided to the input through C_1, and this reduced shunting current effect is equivalent to how a much smaller capacitor behaves. At a fixed frequency, a smaller capacitor has a higher impedance, and thus reduced current. Keep the same level of attenuation from input to output, and vice versa. To find the appropriate capacitor values for the tee network, chose an arbitrarily low but practically realizable and equal values for capacitors C_1 and C_2, set $C_{EQ} = C_{TOT}$, and use Equation 3 to get the value of the tunable capacitor, C_T. The values of capacitors C_1, C_2, and C_T in Figure 8-3 are determined using this process.

$$C_{EQ} = \frac{C_1 \times C_2 - (C_1 + C_2) \times C_{EQ}}{C_{EQ}} \quad (3)$$

Figure 8-4 shows the TINA-TI™ simulation software closed-loop bandwidth response of the circuit in Figure 8-3. The circuit is designed for f_{-3dB} = 24 MHz and the simulated closed-loop 3-dB frequency is 24.6 MHz with approximately 0.1-dB peaking. The OPA818 TINA-TI software model models the input common-mode and differential capacitors that are not added externally when simulating in the TINA-TI software. Figure 8-5 shows the noise simulation of the TIA circuit. The output-referred voltage noise shows on the Y-axis to the left. The input-referred current noise, which is essentially output-referred voltage noise divided by the transimpedance gain of 100k, shows on the secondary Y-axis to the right. The simulation results are fairly accurate because the OPA818 TINA-TI software model closely models the voltage and current noise performance of the amplifier. The flat-band output voltage noise is 41 nV/√Hz that is equivalent to 0.41 pA/√Hz of input-referred current noise. The noise in relatively low frequency region where the noise gain of the amplifier is 1 V/V is dominated by the thermal noise of the 100-kΩ resistor (40.7 nV/√Hz at 27°C). At mid-frequencies beyond the zero formed by R_F and C_{TOT}, the noise gain of the amplifier amplifies the voltage noise of the amplifier. The amplifier noise starts to become the dominant noise contributor from this frequency onward, before the output noise starts to roll off at frequencies beyond the 3-dB closed-loop bandwidth. When looking at the integrated root-mean-square (RMS) noise, mid-frequency noise is potentially a significant contributor. Therefore, use a 2.2-nV/√Hz low-noise amplifier, such as the OPA818, to minimize total RMS noise in the system.

8.2.1.3 Application Curves

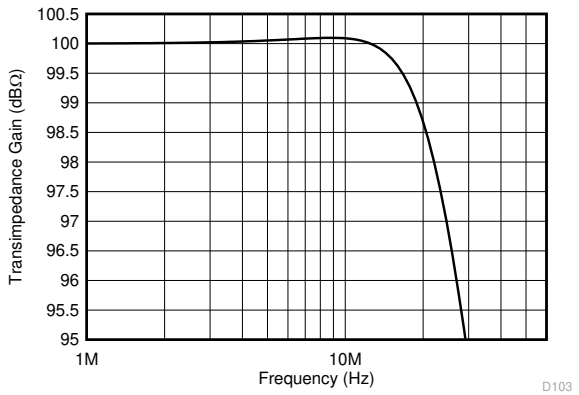

Figure 8-4. Simulated Closed-Loop Bandwidth of the TIA

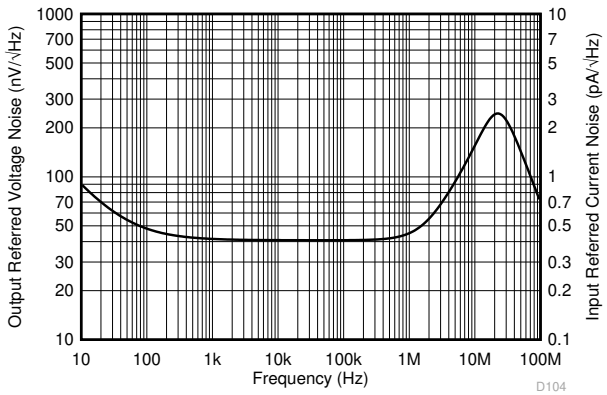

Figure 8-5. Simulated TIA Noise

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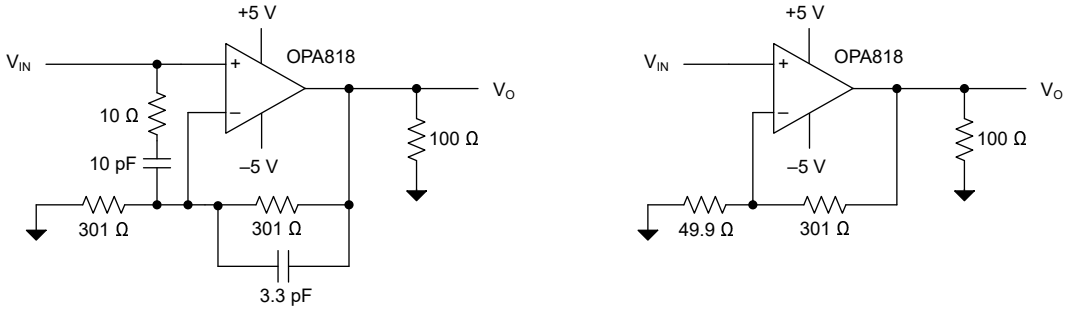
8.2.2 Noninverting Gain of 2 V/V

The OPA818 is typically stable in noise-gain configurations greater than 7 V/V when conventional feedback networks are used. The OPA818 is configurable in noise gains less than 7 V/V by using capacitors in the feedback path and between the inputs. This configuration maintains the desired gain at lower frequencies and increases the noise gain at higher frequencies such that the amplifier is stable. Configuration (a) in Figure 8-6 shows OPA818 configured in a gain of 2 V/V by using capacitors and resistors to shape the noise gain and achieve a phase margin of approximately 51° that is very close to the phase margin achieved for the conventional 7 V/V configuration (b) in Figure 8-6.

The key benefit of using a decompensated amplifier, such as the OPA818, at gains below the minimum stable gain is that designers can take advantage of the low noise and low distortion performance at power levels lower than those of comparable unity-gain stable architectures. The small-signal frequency response in Figure 8-6 shows flat ac performance beyond 100 MHz for a gain of 2 V/V configuration (a) in Figure 8-8, and by being in a lower gain configuration versus the minimum stable gain configuration of 7 V/V, the output-referred total noise is also lower (64 nV/√Hz at 100 MHz); see also Figure 8-8 compared to that at 166 nV/√Hz of configuration (b). Reducing the 10-pF input capacitor allows the system to achieve higher closed-loop bandwidth at the expense of increased peaking and reduced phase margin. Low-capacitance layout by minimizing trace lengths and removing planes under the traces and components connected to the inverting input is critical to minimize parasitic capacitance (see *Layout Guidelines*). Parasitic capacitance as small as 1 pF to 2 pF on the inverting input requires tweaking the noise-shaping component values to get flat frequency response and the desired phase margin. Configurations in Figure 8-6 do not take into account this parasitic capacitance but are considered for practical purposes. A 45° phase margin is generally acceptable, but anything less than 40° is not recommended to allow for component, PCB, and process tolerances. Details on the benefits of decompensated architectures are discussed in *Using a decompensated op amp for improved performance*.



(a) G = 2 V/V **(b) G = 7 V/V**

Figure 8-6. Noninverting Gain of 2 V/V and 7 V/V Configurations

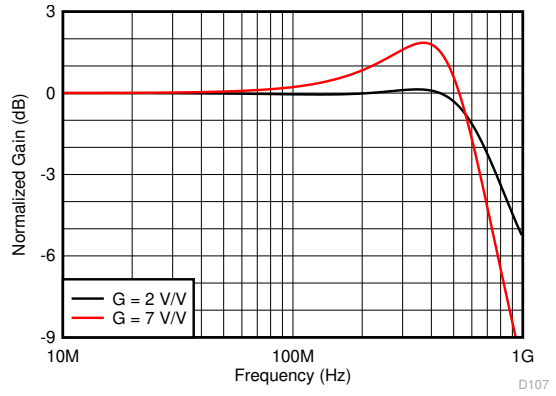


Figure 8-7. Small-Signal Frequency Response in Gains of 2 V/V and 7 V/V Configurations of Figure 8-6

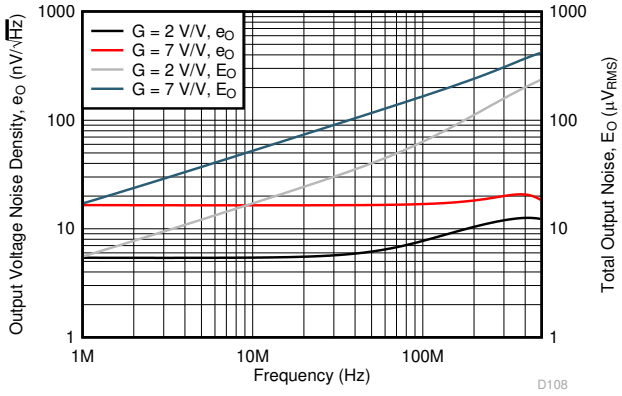


Figure 8-8. Output Noise in Gains of 2 V/V and 7 V/V Configurations of Figure 8-6

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8.3 Power Supply Recommendations

The OPA818 is intended for operation on supplies from 6 V (+4/–2 V) to 12 V (±6 V). The OPA818 supports single-supply, split, as well as balanced and unbalanced bipolar supplies. When operating at supplies less than 8 V, the midsupply is allowed to be outside the input common-mode range of the amplifier. Under these supply conditions, bias the common-mode voltage appropriately for linear operation. Thus, the limit to lower-supply-voltage operation is the useable input voltage range for the JFET-input stage. Operating from a single supply of 12 V has numerous advantages. With the negative supply at ground, the dc errors due to the –PSRR term are minimized. Typically, ac performance improves slightly at 12-V operation with minimal increase in supply current.

8.4 Layout

8.4.1 Layout Guidelines

Achieving optimized performance with a high-frequency amplifier such as the OPA818 requires careful attention to board layout parasitics and external component types. Recommendations that help optimize performance include:

1. **Minimize parasitic capacitance** to any ac ground for all of the signal I/O pins. Parasitic capacitance on the output and inverting input pins potentially causes instability. On the noninverting input, parasitic capacitance potentially reacts with the source impedance to cause unintentional band limiting. Ground and power metal planes act as one of the plates of a capacitor while the signal trace metal acts as the other separated by PCB dielectric. To reduce this unwanted capacitance, a plane cutout around and underneath the signal I/O pins on all ground and power planes is recommended. Otherwise, leave the ground and power planes unbroken elsewhere on the board. When configuring the amplifier as a TIA, if the required feedback capacitor is less than 0.15 pF, consider using two series resistors, each of half the value of a single resistor in the feedback loop to minimize the parasitic capacitance from the resistor.
2. **Minimize the distance** (less than 0.25-in) from the power-supply pins to high-frequency decoupling capacitors. Use high-quality, 100-pF to 0.1-µF, C0G and NPO-type decoupling capacitors with voltage ratings at least three times greater than the amplifiers maximum power supplies. This requirement provides a low-impedance path to the amplifier power-supply pins across the amplifier gain bandwidth specification. At the device pins, do not allow the ground and power plane layout to be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. Always decouple the power-supply connections with these capacitors. Use larger (2.2-µF to 6.8-µF) decoupling capacitors, effective at lower frequency, on the supply pins. Place these larger capacitors further from the device and share the capacitors among several devices in the same area of the PCB.
3. **Careful selection and placement of external components helps preserve the high frequency performance of the OPA818.** Use resistors with low reactance. Surface-mount resistors work best and allow a tighter overall layout. Metal film and carbon composition axially leaded resistors also provide good high frequency performance. Again, keep the leads and PCB trace length as short as possible. Never use wirewound type resistors in a high frequency application. Because the output pin and inverting input pin are the most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close as possible to the inverting input and the output pin, respectively. Place other network components, such as noninverting input termination resistors, close to the package. Even with a low parasitic capacitance shunting the external resistors, excessively high resistor values potentially create significant time constants that degrade performance. When the OPA818 is configured as a conventional voltage amplifier, keep the resistor values as low as possible and consistent with the load driving considerations. Lower resistor values minimize the effect of parasitic capacitance and reduce resistor noise terms. However, because the feedback network (R_F + R_G for noninverting and R_F for inverting configuration) acts as a load on the amplifier, lower resistor values increase the dynamic power consumption and the effective load on the output stage. Transimpedance applications (see Figure 8-2) use feedback resistors as required by the application, and as long as the feedback compensation capacitor is set considering all parasitic capacitance terms on the inverting node.
4. **Heat dissipation is important for a high voltage device such as the OPA818** . For good thermal relief, the thermal pad connected to a heat spreading plane that is preferably on the same layer as OPA818 or connected by as many vias as possible if the plane is on a different layer. Have at least one heat spreading plane on the same layer as the OPA818 that makes a direct connection to the thermal pad with wide metal

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for good thermal conduction when operating at high ambient temperatures. If more than one heat-spreading plane is available, connect them by a number of vias to further improve thermal conduction.

5. **Do not socket a high-speed device such as the OPA818.** The additional lead length and pin-to-pin capacitance introduced by the socket potentially creates an extremely troublesome parasitic network that potentially prevent a smooth, stable frequency response. Best results are obtained by soldering the OPA818 onto the board.

8.4.1.1 Thermal Considerations

The OPA818 does not require heat sinking or airflow in most applications. The maximum allowed junction temperature sets the maximum allowed internal power dissipation, and is described in the following paragraph. Do not exceed a maximum junction temperature of 105°C.

The operating junction temperature (T_J) is given by $T_A + P_D \times R_{\theta JA}$. The total internal power dissipation (P_D) is the sum of quiescent power (P_{DQ}) and additional power dissipated in the output stage (P_{DL}) to deliver load power. Quiescent power is simply the specified no-load supply current times the total supply voltage across the device. The P_{DL} depends on the output signal and load. For a grounded resistive load, the P_{DL} is at a maximum when the output is fixed at a voltage equal to 1/2 of either supply voltage (for balanced bipolar supplies). Under this condition, $P_{DL} = V_S{}^2 / (4 \times R_L)$, where R_L includes feedback network loading.

Be aware that the power in the output stage, and not into the load, determines internal power dissipation.

As a worst-case example, compute the maximum T_J using the OPA818 in the circuit of Figure 8-1 operating at a maximum specified ambient temperature of 85°C and driving a grounded 100-Ω load.

$P_D = 10\ V \times 27.7\ mA + 5^2 / (4 \times (100\ \Omega \parallel 350.9\ \Omega)) \cong 357\ mW$

Maximum $T_J = 85°C + (0.357\ W \times 54.6°C/W) = 104.5°C$.

In the circuit of Figure 8-1, all practical scenarios are able to operate at a lower internal power and junction temperature.

8.4.2 Layout Example

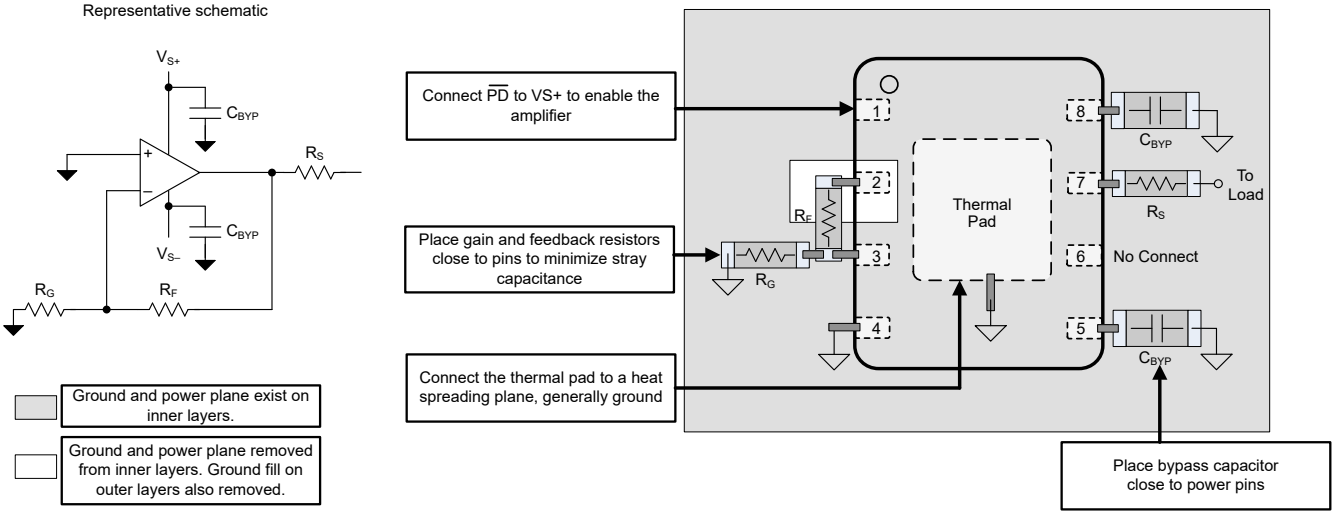

Figure 8-9. Layout Recommendation

When configuring the OPA818 as a transimpedance amplifier take extra care to minimize the inductance between the avalanche photodiode (APD) and the amplifier. Always place the photodiode on the same side of the PCB as the amplifier. Placing the amplifier and the APD on opposite sides of the PCB increases the parasitic effects due to via inductance. APD packaging can be quite large, which often requires the APD to be placed further away from the amplifier than ideal. The added distance between the two device results in increased inductance between the APD and op-amp feedback network (see also Equation 4). The added inductance is

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detrimental to a decompensated amplifier stability because this amplifier isolates the APD capacitance from the noise gain transfer function. Equation 4 calculates the noise gain. The added PCB trace inductance between the feedback network increases the denominator in Equation 4, thereby reducing the noise gain and the phase margin. In cases where a leaded APD in a TO can is used, further minimize inductance by cutting the leads of the TO can as short as possible. Also, consider edge mounting the photodiode on the PCB versus through the hole, if the application allows.

To improve the layout in Figure 8-10, follow some of the guidelines in Figure 8-11. The two key rules to follow are:

- Add an isolation resistor R_{ISO} as close as possible to the inverting input of the amplifier. Select the value of R_{ISO} to be between 10 Ω and 20 Ω. The resistor dampens the potential resonance caused by the trace inductance and the amplifiers internal capacitance.
- Close the loop between the feedback elements (R_F and C_F) and R_{ISO} as close to the APD pins as possible. This configuration provides a more balanced layout and reduces the inductive isolation between the APD and the feedback network.

$$\text{Noise Gain} = \left(1 + \frac{Z_F}{Z_{IN}}\right) \tag{4}$$

where,

- Z_F is the total impedance of the feedback network
- Z_{IN} is the total impedance of the input network

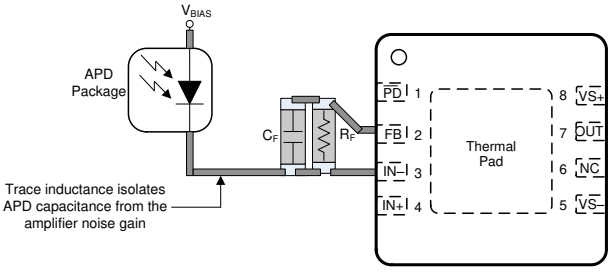

Figure 8-10. Non-Ideal TIA Layout

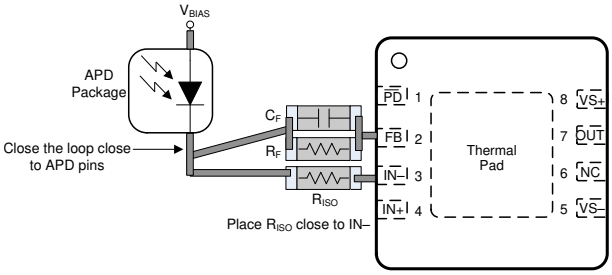

Figure 8-11. Improved TIA Layout

9 Device and Documentation Support

9.1 Device Support

9.1.1 Development Support

- Texas Instruments, *Wide Bandwidth Optical Front-end Reference Design*

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *OPA817EVM User's Guide*
- Texas Instruments, *Transimpedance Considerations for High-Speed Amplifiers application report*
- Texas Instruments, *Maximizing the Dynamic Range of Analog TIA Front-End technical brief*
- Texas Instruments, *What You Need To Know About Transimpedance Amplifiers – Part 1*
- Texas Instruments, *What You Need To Know About Transimpedance Amplifiers – Part 2*
- Texas Instruments, *Training Video: How to Design Transimpedance Amplifier Circuits*
- Texas Instruments, *Training Video: High-Speed Transimpedance Amplifier Design Flow*

9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (March 2020) to Revision B (December 2025)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Added DBV package (SOT-23, 5) and associated content as production data	1
• Added harmonic distortion for DBV package	5

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Changes from Revision * (May 2019) to Revision A (March 2020)	Page
• Changed document status From: *Advance Information* To: *Production Data*	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA818DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	-	SN	Level-1-260C-UNLIM	-40 to 125	O818
OPA818DBVT	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	-	SN	Level-1-260C-UNLIM	-40 to 125	O818
OPA818IDRGR	Active	Production	SON (DRG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA818
OPA818IDRGR.B	Active	Production	SON (DRG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA818
OPA818IDRGRG4	Active	Production	SON (DRG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA818
OPA818IDRGRG4.B	Active	Production	SON (DRG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA818
OPA818IDRGT	Active	Production	SON (DRG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA818
OPA818IDRGT.B	Active	Production	SON (DRG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA818

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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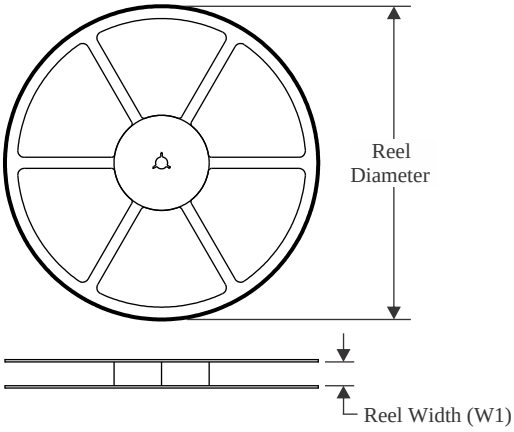
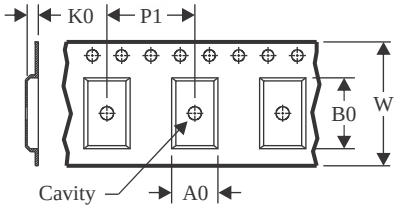
TAPE AND REEL INFORMATION

REEL DIMENSIONS

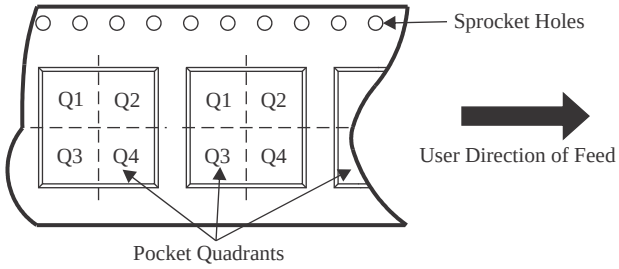


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

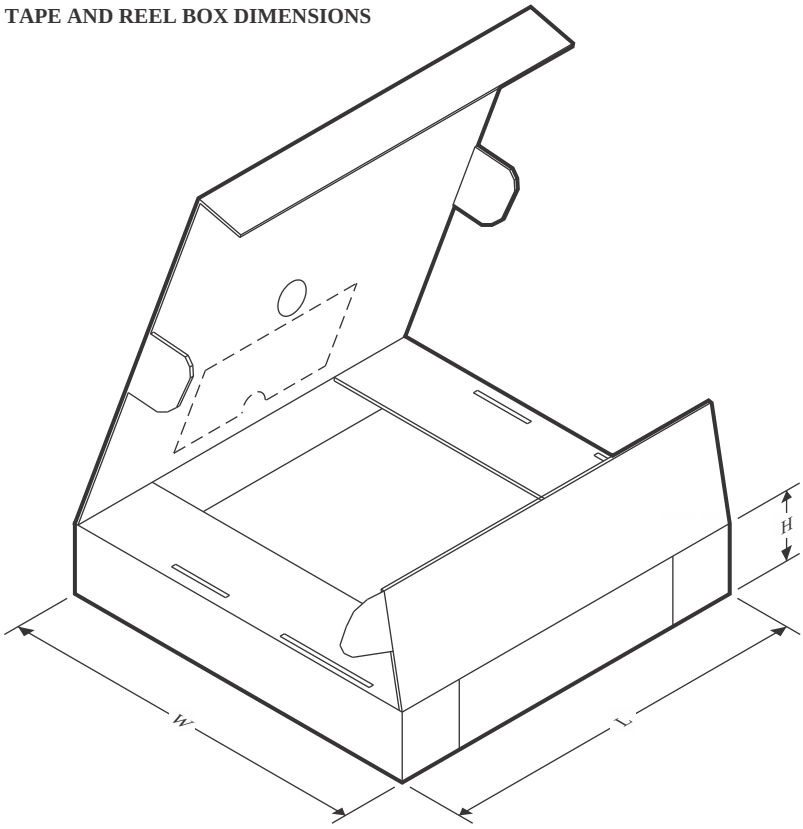
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA818DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA818DBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA818IDRGR	SON	DRG	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
OPA818IDRGRG4	SON	DRG	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
OPA818IDRGT	SON	DRG	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

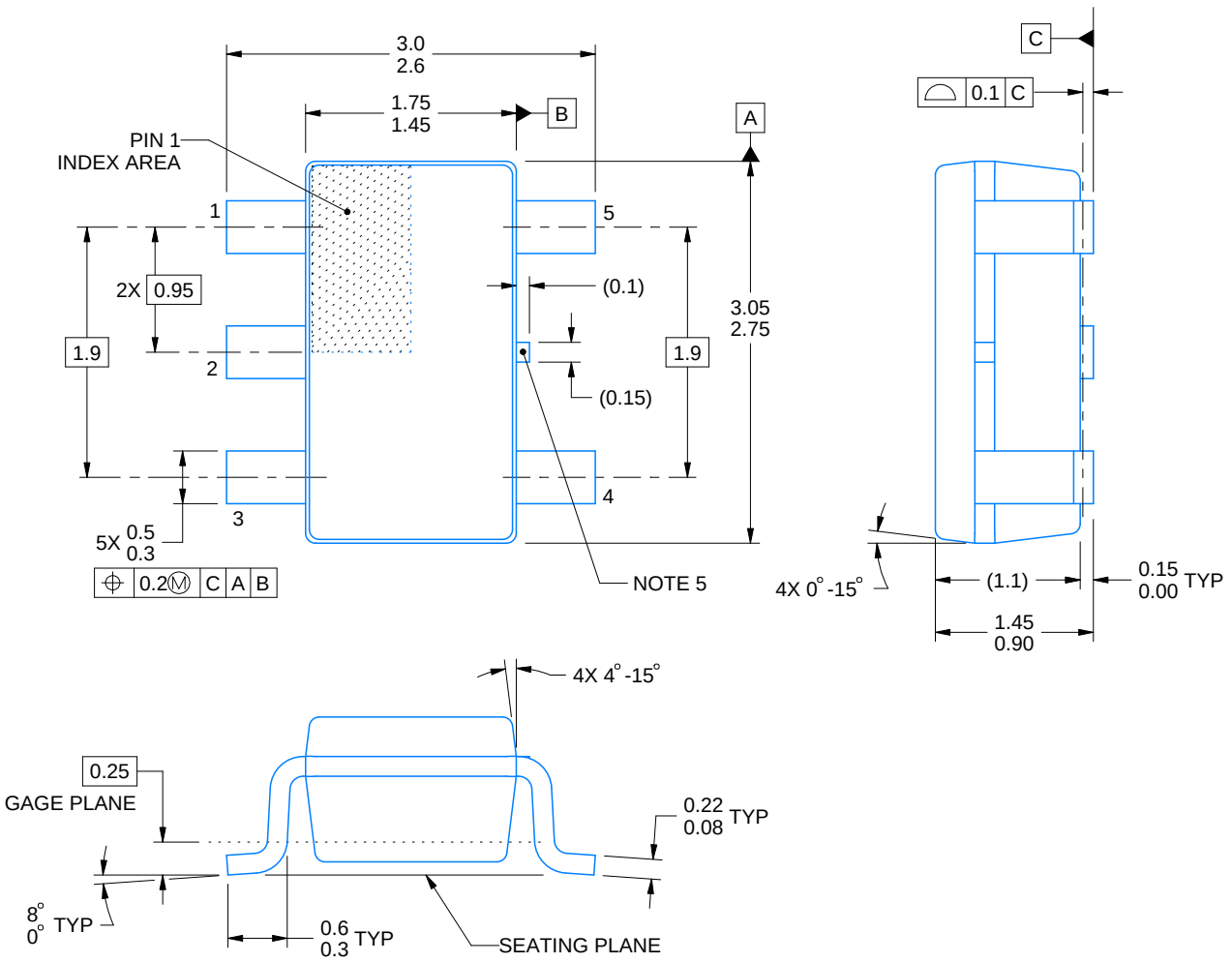
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA818DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
OPA818DBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
OPA818IDRGR	SON	DRG	8	3000	367.0	367.0	35.0
OPA818IDRGRG4	SON	DRG	8	3000	367.0	367.0	35.0
OPA818IDRGT	SON	DRG	8	250	210.0	185.0	35.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

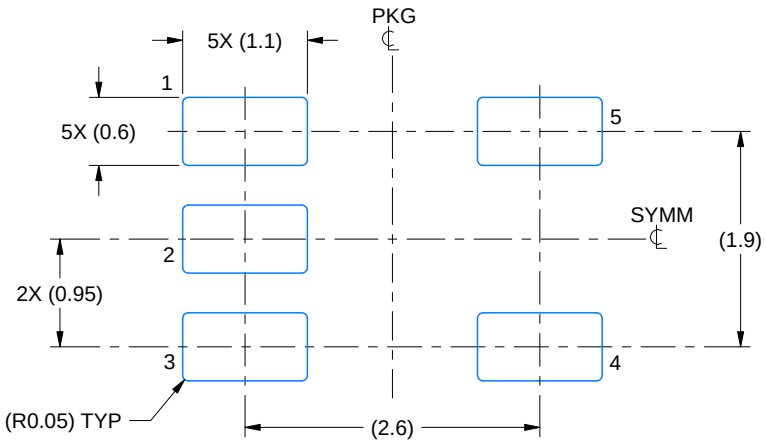
SMALL OUTLINE TRANSISTOR



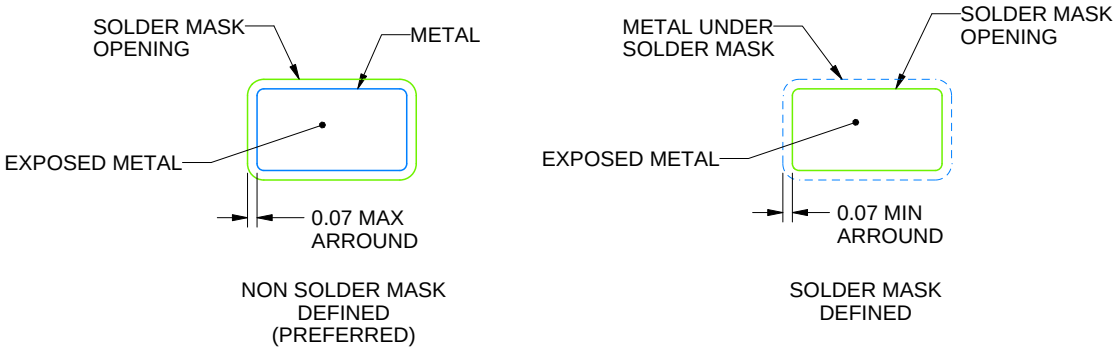
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

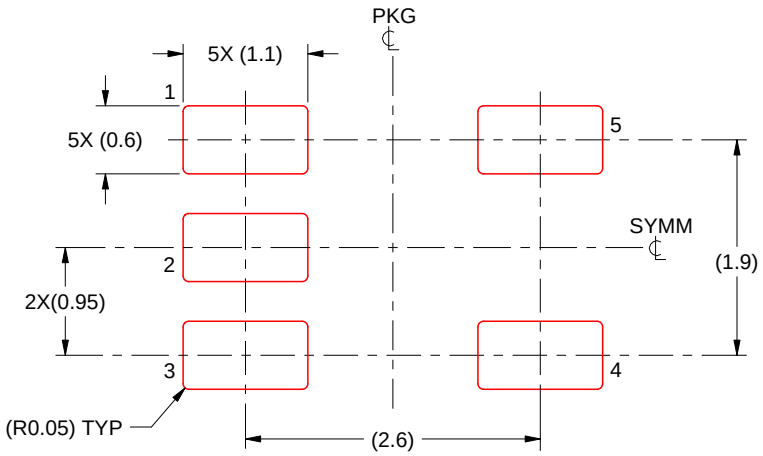


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

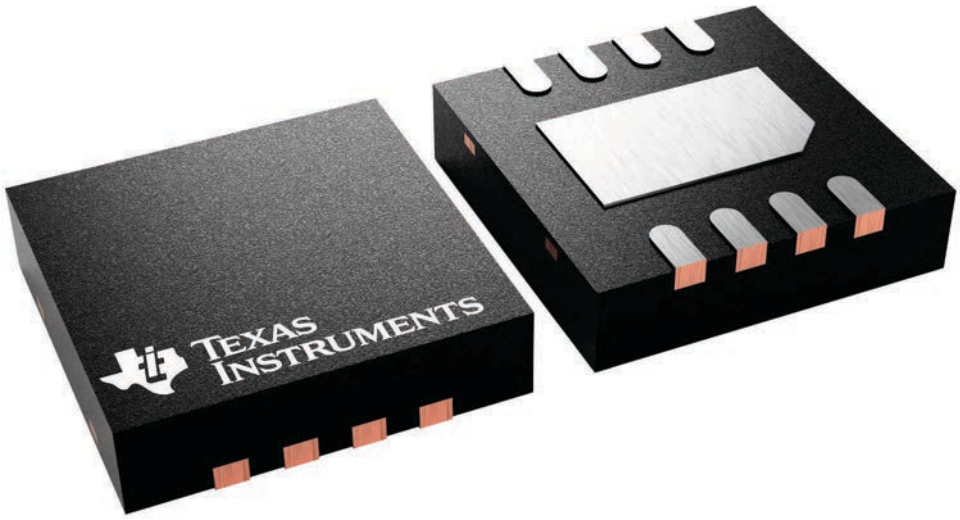
DRG 8

WSON - 0.8 mm max height

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



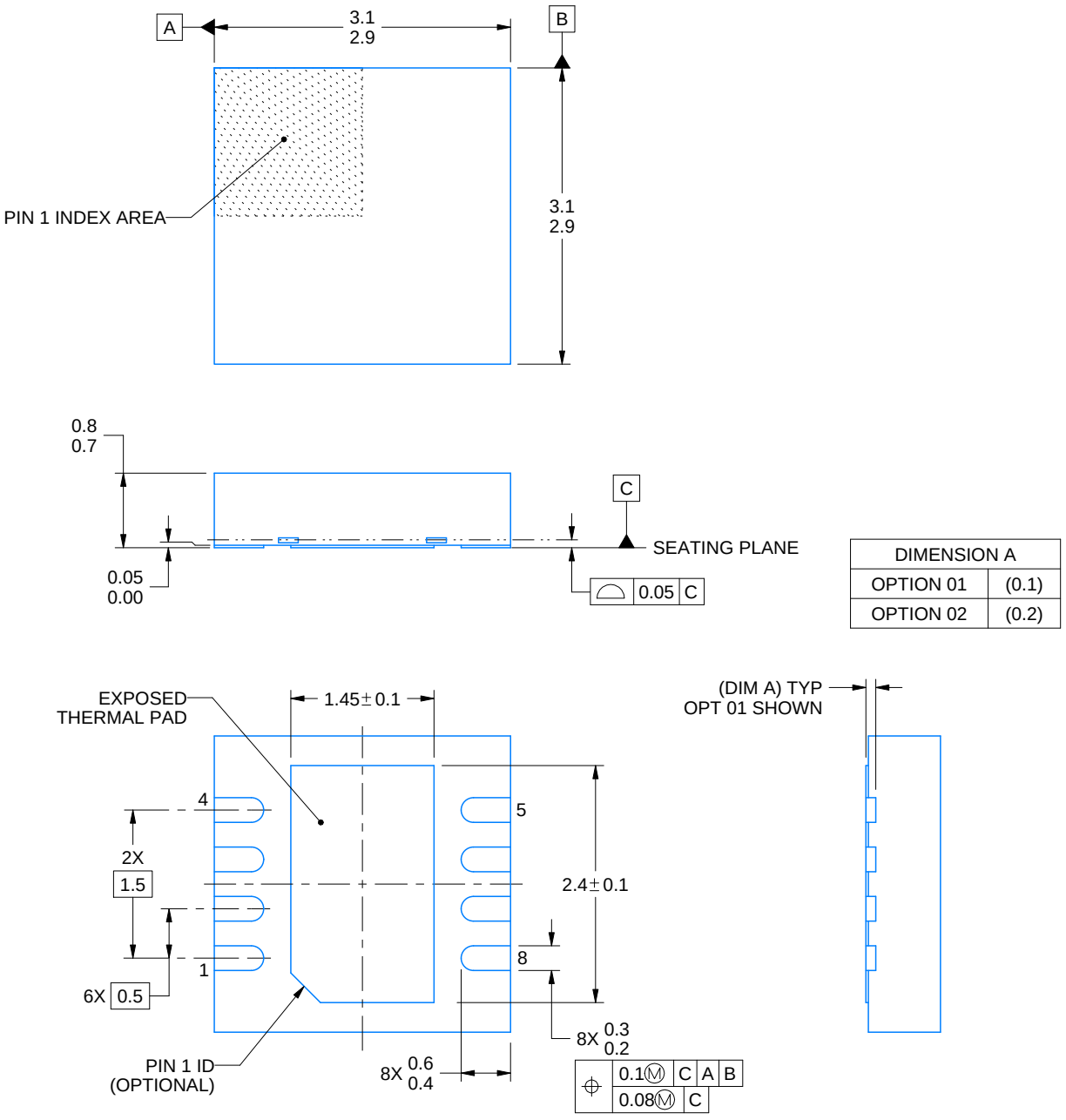
4225794/A

DRG0008B

PACKAGE OUTLINE

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

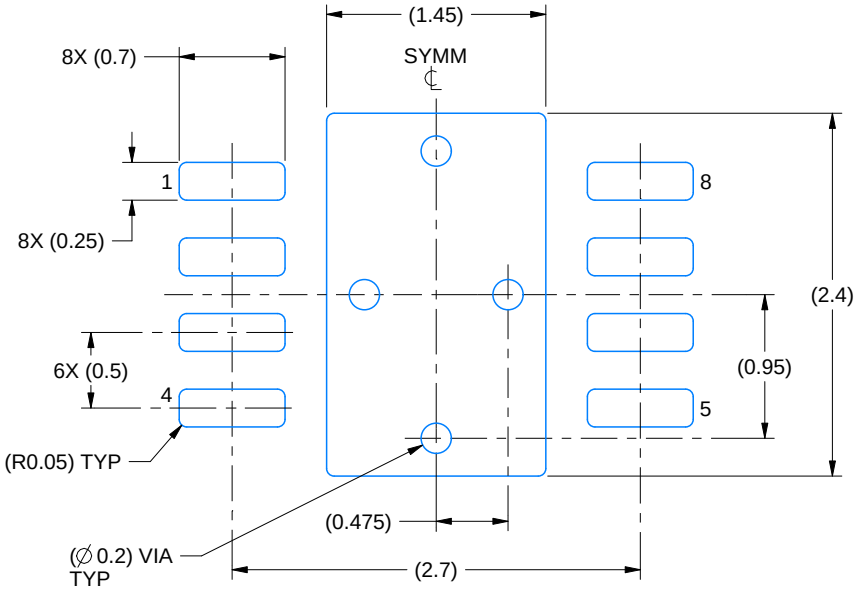


DIMENSION A	
OPTION 01	(0.1)
OPTION 02	(0.2)

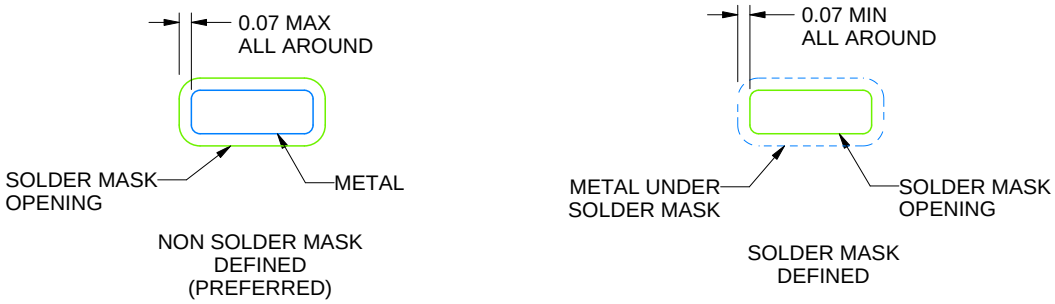
4218886/A 01/2020

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

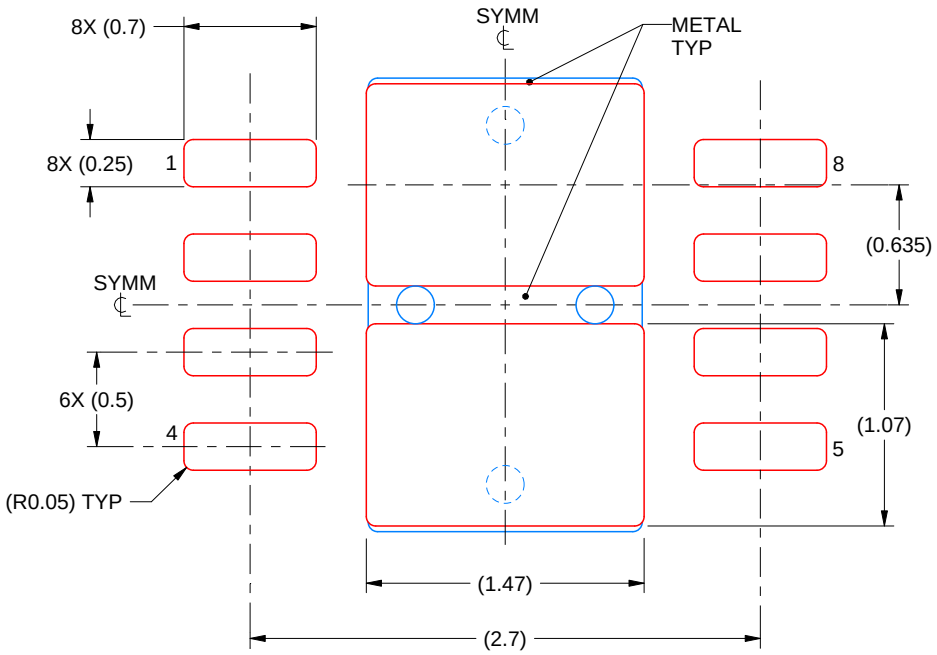


SOLDER MASK DETAILS

4218886/A 01/2020

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
82% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218886/A 01/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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