OPAx625 High-Bandwidth, High-Precision, Low THD+N, 16-Bit and 18-Bit Analog-to-Digital Converter (ADC) Drivers

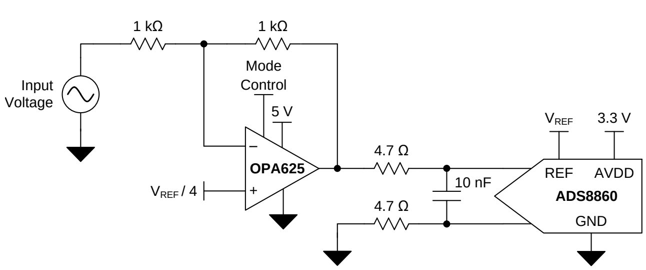
1 Features

- High-Drive Mode:
  - GBW (G = 100): 120 MHz
  - Slew Rate: 115 V/µs
  - 16-Bit Settling at 4-V Step: 280 ns
  - Low Voltage Noise: 2.5 nV/√Hz at 10 kHz
  - Low Output Impedance: 1 Ω at 1 MHz
  - Offset Voltage: ±100 µV (max)
  - Offset Voltage Drift: ±3 µV/ºC (max)
  - Low Quiescent Current: 2 mA (typ)
- Low-Power Mode:
  - GBW: 1 MHz
  - Low Quiescent Current: 270 µA (typ)
- Power-Scalable Features:
  - Ultrafast Transition from Low-Power to High-Drive Mode: 170 ns
- High AC and DC Precision:
  - Low Distortion: –122 dBc for HD2 and –140 dBc for HD3 at 100 kHz
  - Input Common-Mode Range Includes Negative Rail
  - Rail-to-Rail Output
  - Wide Temperature Range: Fully Specified from –40°C to +125°C

2 Applications

- Precision SAR ADC Drivers
- Precision Voltage Reference Buffers
- Programmable Logic Controllers
- Test and Measurement Equipment
- Power-Sensitive Data Acquisition Systems

SAR ADC Driver



3 Description

The OPAx625 family of operational amplifiers are excellent 16-bit and 18-bit, high-precision, SAR ADC drivers with low THD and noise that allow for a unique power-scalable solution. This family of devices is fully characterized and specified with a 16-bit settling time of 280 ns that enables a true 16-bit effective number of bits (ENOB). With a high dc precision of only 100 µV offset voltage, a wide gain-bandwidth product of 120 MHz, and a low wideband noise of 2.5 nV/√Hz, this family is optimized for driving high-throughput, high-resolution SAR ADCs, such as the ADS88xx family of SAR ADCs.

The OPAx625 features two operating modes: high-drive and low-power. In the innovative low-power mode, the OPAx625 tracks the input signal allowing the device to transition from low-power mode to high-drive mode at 16-bit ENOB within 170 ns.

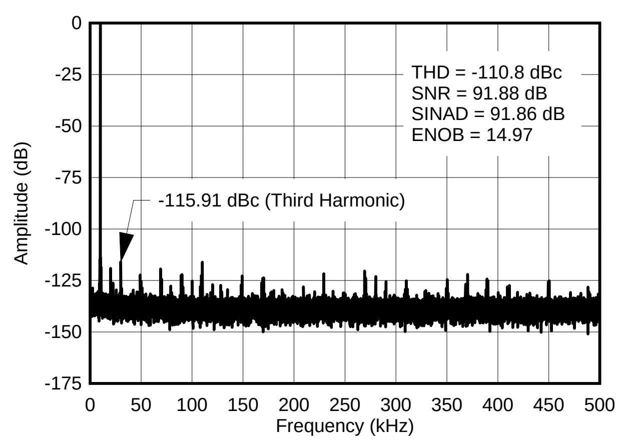
The OPAx625 family is available in 6-pin SOT and 10-pin VSSOP packages and is specified for operation from –40°C to +125°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA625	SOT (6)	2.90 mm × 1.60 mm
OPA2625	VSSOP (10)	3.00 mm × 3.00 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.

16-Bit SAR ADC, f_{IN} = 10-kHz, 1-MSPS FFT



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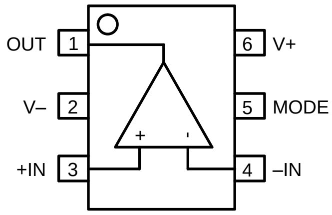
4 Revision History

Changes from Original (April 2015) to Revision A — **Page**

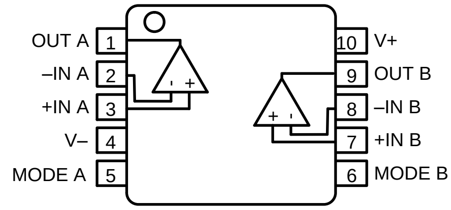
- Changed OPA2625 from product preview to production data; added OPA2625 specifications to data sheet ... 1
- Changed MODE B pin description options for V+ and V– ... 3
- Added crosstalk parameter to *Electrical Characteristics* table ... 5
- Added crosstalk parameter to *Electrical Characteristics* table ... 8
- Changed short-circuit current value from 150 mA to 80 mA in *Electrical Characteristics* table ... 9
- Changed short-circuit current value from 100 mA to 50 mA in *Electrical Characteristics* table ... 10
- Added OPA2625 data to Figure 12 ... 13
- Added Figure 24 ... 15
- Deleted "18" from several typical characteristic figure titles (typo) ... 19

5 Pin Configuration and Functions

OPA625: DBV Package
6-Pin SOT
Top View



OPA2625: DGS Package
10-Pin VSSOP
Top View



Pin Functions: OPA625

PIN		I/O	DESCRIPTION
NAME	NO		
+IN	3	I	Noninverting input
–IN	4	I	Inverting input
MODE	5	I	Controls OPA625 mode: V+ = low-power mode V– = high-drive mode NOTE: Do not float this pin.
OUT	1	O	Output terminal
V+	6	—	Positive supply voltage
V–	2	—	Negative supply voltage

Pin Functions: OPA2625

PIN		I/O	DESCRIPTION
NAME	NO.		
+IN A	3	I	Noninverting input for channel A
–IN A	2	I	Inverting input for channel A
+IN B	7	I	Noninverting input for channel B
–IN B	8	I	Inverting input for channel B
MODE A	5	I	Controls OPA2625 mode for channel A: V+ = low-power mode V– = high-drive mode NOTE: Do not float this pin.
MODE B	6	I	Controls OPA2625 mode for channel B: V+ = low-power mode V– = high-drive mode NOTE: Do not float this pin.
OUT A	1	O	Output terminal for channel A
OUT B	9	O	Output terminal for channel B
V+	10	—	Positive supply voltage
V–	4	—	Negative supply voltage

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage, V_S	(V+) – (V–)		6	V
Input voltage(2)	+IN	(V–) – 0.3	(V+) + 0.3	V
	–IN	(V–) – 0.3	(V+) + 0.3	
	MODE	(V–) – 0.3	(V+) + 0.3	
Output voltage	OUT	(V–)	(V+)	V
Sink current	+IN		10	mA
	–IN		10	
	MODE		10	
	OUT		150	
Source current	+IN		10	mA
	–IN		10	
	MODE		10	
	OUT(2)		150	
Temperature	Operating junction	–40	150	°C
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) For input voltages beyond the power-supply rails, voltage or current must be limited.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_S	Supply input voltage, (V+) – (V–)		2.7		5.5	V
V_I	Input voltage	+IN	(V–)		(V+) – 1.15	V
		–IN	(V–)		(V+) – 1.15	
		MODE	(V–)		(V+)	
V_O	Output voltage		(V–)		(V+)	V
I_O	Output current		–120		120	mA
T_A	Operating free-air temperature		–40		125	°C
T_J	Operating junction temperature		–40		125	°C

6.4 Thermal Information

THERMAL METRIC (1)		OPA625 DBV (SOT) 6 PINS	OPA2625 DGS (VSSOP) 10 PINS	UNIT
$R_{θJA}$	Junction-to-ambient thermal resistance	184.9	171.7	°C/W
$R_{θJC(top)}$	Junction-to-case (top) thermal resistance	123.6	68.4	°C/W
$R_{θJB}$	Junction-to-board thermal resistance	30.7	91.9	°C/W
$ψ_{JT}$	Junction-to-top characterization parameter	22.1	9.4	°C/W
$ψ_{JB}$	Junction-to-board characterization parameter	30.2	90.5	°C/W
$R_{θJC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics High-Drive Mode

at T_A = 25°C, V+ = 5 V, V– = 0 V, MODE pin connected to V– pin, V_{COM} = V_O = 2.5 V, gain (G) = 1, R_F = 1 kΩ, C_F = 2.7 pF, C_{LOAD} = 20 pF, and R_{LOAD} = 2 kΩ connected to 2.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
AC PERFORMANCE							
	Unity gain frequency	V_O = 10 mV_{PP}			80		MHz
$φ_m$	Phase margin				50		Degrees
GBW	Gain-bandwidth product	G = 100, V_O = 10 mV_{PP}			120		MHz
SR	Slew rate	V_O = 1-V step, G = 1			45		V/µs
		V_O = 4-V step, G = 2			115		
t_{settle}	Settling time	V_O = 4-V step, G = 2	Settling time to 0.1% (10-bit accuracy)		80		ns
			to 0.005% (14-bit accuracy)		110		
			to 0.00153% (16-bit accuracy)		280		
	Overshoot	V_O = 4-V step, G = 2			2.5%		
	Undershoot	V_O = 4-V step, G = 2			3%		
HD2	Second-order harmonic Distortion	V_O = 2 V_{PP}, G = 2	f = 10 kHz		144		dBc
			f = 100 kHz		122		
			f = 1 MHz		80		
HD3	Third-order harmonic Distortion	V_O = 2 V_{PP}, G = 2	f = 10 kHz		155		dBc
			f = 100 kHz		140		
			f = 1 MHz		80		
	Second-order intermodulation distortion	V_O = 2 V_{PP}, f = 1 MHz, 200-kHz tone spacing			90		dBc
	Third-order intermodulation distortion	V_O = 2 V_{PP}, f = 1 MHz, 200-kHz tone spacing			100		dBc
V_N	Input noise voltage	f = 0.1 Hz to 10 Hz, peak-to-peak			0.8		$µV_{PP}$
		f = 0.1 Hz to 10 Hz, rms			120		nV_{RMS}
V_n	Input voltage noise density	f = 1 kHz			3.2		nV/√Hz
		f = 10 kHz			2.5		
I_n	Input current noise density	f = 1 kHz			4.1		pA/√Hz
		f = 10 kHz			2.8		
t_{OR}	Overload recovery time	G = 5			50		ns
Z_o	Open-loop output impedance	f = 1 MHz			1		Ω
	Crosstalk	DC			150		dB
		f = 1 MHz			127		
DC PERFORMANCE							
V_{OS}	Input offset voltage				15	±100	µV
		T_A = –40°C to +125°C				±300	

Electrical Characteristics High-Drive Mode (continued)

at T_A = 25°C, V+ = 5 V, V– = 0 V, MODE pin connected to V– pin, V_{COM} = V_O = 2.5 V, gain (G) = 1, R_F = 1 kΩ, C_F = 2.7 pF, C_{LOAD} = 20 pF, and R_{LOAD} = 2 kΩ connected to 2.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to +125°C			0.5	±3	µV/°C
		OPA2625 only, T_A = –40°C to +125°C			0.6	±4	
PSRR	Power-supply rejection ratio	2.7 V ≤ (V+) ≤ 5 V		100			dB
			T_A = –40°C to +125°C	90	120		
I_B	Input bias current				2	4	µA
		T_A = –40°C to +125°C				5.7	
		OPA2625 only, T_A = –40°C to +125°C				6.5	
dI_B/dT	Input bias current drift	T_A = –40°C to +125°C			15		nA/°C
I_{OS}	Input offset current				20	120	nA
		T_A = –40°C to +125°C				150	
		OPA2625 only, T_A = –40°C to +125°C				200	
dI_{OS}/dT	Input offset current drift	T_A = –40°C to +125°C			0.6		nA/°C
OPEN LOOP GAIN							
A_{OL}	Open-loop gain	(V–) + 0.2 V < V_O < (V+) – 0.2 V, R_{LOAD} = 600 Ω		110			dB
		(V–) + 0.15 V < V_O < (V+) – 0.15 V, R_{LOAD} = 10 kΩ		114			
		T_A = –40°C to +125°C	(V–) + 0.2 V < V_O < (V+) – 0.2 V, R_{LOAD} = 600 Ω	106	128		
			(V–) + 0.15 V < V_O < (V+) – 0.15 V, R_{LOAD} = 10 kΩ	110	132		
INPUT VOLTAGE							
V_{CM}	Common-mode voltage range	T_A = –40°C to +125°C		(V–)		(V+) – 1.15	V
CMRR	Common-mode rejection ratio	(V–) < V_{COM} < (V+) – 1.15 V		100	117		dB
			T_A = –40°C to +125°C	90	115		
INPUT IMPEDANCE							
Z_{ID}	Differential input impedance				27 || 1.2		KΩ || pF
Z_{IC}	Common-mode input impedance				47 || 1.5		MΩ || pF
OUTPUT							
	Output voltage swing to the rail	R_{LOAD} = 600 Ω			60	80	mV
			T_A = –40°C to +125°C			100	
		R_{LOAD} = 10 kΩ			20	35	
			T_A = –40°C to +125°C			40	
I_{sc}	Short-circuit current				150		mA
C_{LOAD}	Capacitive load drive			See Typical Characteristics			
MODE							
V_{IL}	High-drive (HD) mode threshold	T_A = –40°C to +125°C		(V–)		(V–) + 0.5	V
V_{IH}	Low-power (LP) mode threshold	T_A = –40°C to +125°C		(V–) + 1.2		(V+)	V
I_{IL}	Low-level input current	T_A = –40°C to +125°C, V_{MODE} ≤ (V–) + 0.5 V			0.01	1	µA
I_{IH}	High-level input current	T_A = –40°C to +125°C, V_{MODE} ≥ (V–) + 1.2 V			20	30	µA
		OPA2625 only, T_A = –40°C to +125°C, V_{MODE} ≥ (V–) + 1.2 V				1	
POWER SUPPLY							
I_Q	Quiescent current per amplifier	I_O = 0 mA, MODE connected to ground			2	2.2	mA
			T_A = –40°C to +125°C			3.1	

6.6 Electrical Characteristics Low-Power Mode

at T_A = 25°C, V+ = 5 V, V– = 0 V, V_{MODE} = 5 V, V_{COM} = V_O = 2.5 V, gain (G) = 1, R_F = 1 kΩ, C_F = 2.7 pF, C_{LOAD} = 20 pF, and R_{LOAD} = 2 kΩ connected to 2.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
AC PERFORMANCE							
GBW	Gain-bandwidth product	G = 100, V_O = 10 mV_{PP}			1		MHz
$φ_m$	Phase margin				72		Degrees
SR	Slew rate	V_O = 1-V step			4.3		V/µs
		V_O = 4-V step, G = 2			4.1		
Z_o	Open-loop output impedance	f = 1 MHz			12		Ω
DC PERFORMANCE							
V_{OS}	Input offset voltage				0.6	3	mV
		T_A = –40°C to +125°C			0.7	3.7	
PSRR	Power-supply rejection ratio	2.7 V ≤ (V+) ≤ 5 V		74			dB
			T_A = –40°C to +125°C	70	100		
I_B	Input bias current					150	nA
		T_A = –40°C to +125°C			140	200	
		OPA2625 only, T_A = –40°C to +125°C				250	
I_{OS}	Input offset current					20	nA
		T_A = –40°C to +125°C				25	
OPEN LOOP GAIN							
A_{OL}	Open-loop gain	T_A = –40°C to +125°C	(V–) + 0.2 V < V_O < (V+) – 0.2 V, R_{LOAD} = 600 Ω	70	100		dB
			(V–) + 0.15 V < V_O < (V+) – 0.15 V, R_{LOAD} = 10 kΩ	90	100		
INPUT VOLTAGE							
V_{CM}	Common-mode voltage range	T_A = –40°C to +125°C		(V–)		(V+) – 1.15	V
CMRR	Common-mode rejection ratio	(V–) < V_{COM} < (V+) – 1.15 V		66	114		dB
			T_A = –40°C to +125°C	60	114		
OUTPUT							
	Output voltage swing to the rail	T_A = –40°C to +125°C	R_{LOAD} = 600 Ω			110	mV
			R_{LOAD} = 10 kΩ			40	
I_{sc}	Short-circuit current				100		mA
POWER SUPPLY							
I_Q	Quiescent current per amplifier	I_O = 0 mA, MODE connected to V+			270	320	µA
			T_A = –40°C to +125°C			450	

6.7 Electrical Characteristics High-Drive Mode

at T_A = +25°C, V+ = 2.7 V, V– = 0 V, V_{MODE} = 0 V, V_{COM} = V_O = 1.35 V, gain (G) = 1, R_F = 1 kΩ, C_F = 2.7 pF, C_{LOAD} = 20 pF, and R_{LOAD} = 1 kΩ connected to 1.35 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
AC PERFORMANCE							
	Unity gain frequency	V_O = 10 mV_{PP}			76		MHz
$φ_m$	Phase margin				45		Degrees
GBW	Gain-bandwidth product	G = 100, V_O = 10 mV_{PP}			120		MHz
SR	Slew rate	V_O = 1-V step, G = 2			45		V/µs
t_{settle}	Settling time	V_O = 1-V step, G = 2	to 0.1%		80		ns
			to 0.01%		170		
			to 0.000763% (17-bit accuracy)		250		
	Overshoot	V_O = 1-V step, G = 2			6%		
	Undershoot	V_O = 1-V step, G = 2			5%		
HD2	Second order harmonic Distortion	(V+) = 3.3 V, (V–) = 0 V, V_{COM} = 1.1 V, V_O = 2 V_{PP}	f = 10 kHz		136		dBc
			f = 100 kHz		118		
			f = 1 MHz		80		
HD3	Third order harmonic Distortion	(V+) = 3.3 V, (V–) = 0 V, V_{COM} = 1.1 V, V_O = 2 V_{PP}	f = 10 kHz		143		dBc
			OPA2625 only, f = 10 kHz		143		
			f = 100 kHz		130		
			OPA2625 only, f = 100 kHz		125		
			f = 1 MHz		85		
			OPA2625 only, f = 1 MHz		74		
	Second order inter-modulation distortion	(V+) = 3.3 V, (V–) = 0 V, V_{COM} = 1.1 V, V_O = 2 V_{PP}, f = 1 MHz, 200-kHz tone spacing			95		dBc
	Third order inter-modulation distortion	(V+) = 3.3 V, (V–) = 0 V, V_{COM} = 1.1V, V_O = 1 V_{PP}, f = 1 MHz, 200-kHz tone spacing			104		dBc
V_N	Input noise voltage	f = 0.1 Hz to 10 Hz peak to peak			0.8		$µV_{PP}$
		f = 0.1 Hz to 10 Hz rms			120		nV_{RMS}
V_n	Input voltage noise density	f = 10 kHz			2.5		nV/√Hz
I_n	Input current noise density	f = 10 kHz			2.8		pA/√Hz
t_{OR}	Overload recovery time	G = 5			35		ns
Z_o	Open-loop output impedance	f = 1 MHz			1.3		Ω
	Crosstalk	DC			150		dB
		f = 1 MHz			127		
DC PERFORMANCE							
V_{OS}	Input offset voltage				15	±100	µV
		T_A = –40°C to +125°C				±300	
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to +125°C			0.5	±3.1	µV/°C
		OPA2625 only, T_A = –40°C to +125°C			0.6	±4	
I_B	Input bias current				2	4	µA
		T_A = –40°C to +125°C				5.7	
		OPA2625 only, T_A = –40°C to +125°				6.5	
dI_B/dT	Input bias current drift	T_A = –40°C to +125°C			15		nA/°C
I_{OS}	Input offset current				20	120	nA
		T_A = –40°C to +125°C				150	
		OPA2625 only, T_A = –40°C to +125°				200	
dI_{OS}/dT	Input offset current drift	T_A = –40°C to +125°C			80		pA/°C
OPEN-LOOP GAIN							

Electrical Characteristics High-Drive Mode (continued)

at T_A = +25°C, V+ = 2.7 V, V– = 0 V, V_{MODE} = 0 V, V_{COM} = V_O = 1.35 V, gain (G) = 1, R_F = 1 kΩ, C_F = 2.7 pF, C_{LOAD} = 20 pF, and R_{LOAD} = 1 kΩ connected to 1.35 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
A_{OL}	Open-loop gain	(V–) + 0.2 V < V_O < (V+) – 0.2 V, R_{LOAD} = 600 Ω		110			dB
		(V–) + 0.15 V < V_O < (V+) – 0.15 V, R_{LOAD} = 10 kΩ		114			
		T_A = –40°C to +125°C	(V–) + 0.2 V < V_O < (V+) – 0.2 V, R_{LOAD} = 600 Ω	106	128		
			(V–) + 0.15 V < V_O < (V+) – 0.15 V, R_{LOAD} = 10 kΩ	110	132		
INPUT VOLTAGE							
V_{CM}	Common-mode voltage range	T_A = –40°C to +125°C		(V–)		(V+) – 1.15	V
CMRR	Common-mode rejection ratio	(V–) < V_{COM} < (V+) – 1.15 V		100	117		dB
			T_A = –40°C to +125°C	90	115		
INPUT IMPEDANCE							
Z_{ID}	Differential input impedance				27 || 0.8		KΩ || pF
Z_{IC}	Common-mode input impedance				47 || 1.2		MΩ || pF
OUTPUT							
	Output voltage swing to the rail	R_{LOAD} = 600 Ω			60	80	mV
			T_A = –40°C to +125°C			100	
		R_{LOAD} = 10 kΩ			20	35	
			T_A = –40°C to +125°C			40	
I_{SC}	Short-circuit current				80		mA
C_{LOAD}	Capacitive load drive				See Typical Characteristics		
MODE							
V_{IL}	High-drive (HD) mode threshold	T_A = –40°C to +125°C		(V–)		(V–) + 0.5	V
V_{IH}	Low-power (LP) mode threshold	T_A = –40°C to +125°C		(V–) + 1.2		(V+)	V
POWER SUPPLY							
I_Q	Quiescent current per amplifier	I_O = 0 mA MODE connected to ground			2	2.1	mA
			T_A = –40°C to +125°C			2.8	

6.8 Electrical Characteristics Low-Power Mode

at T_A = +25°C, V+ = 2.7 V, V– = 0 V, V_{MODE} = 2.7 V, V_{COM} = V_O = 1.35V, gain (G) = 1, R_F = 1 kΩ, C_F = 2.7 pF, C_{LOAD} = 20 pF, and R_{LOAD} = 1 kΩ connected to 1.35 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
AC PERFORMANCE							
GBW	Gain-bandwidth product	G = 100, V_{IN} = 10 mV_{PP}			0.8		MHz
$φ_m$	Phase margin				72		Degrees
SR	Slew rate	V_O = 1 V-step, G = 2			3.7		V/µs
Z_o	Open-loop output impedance	f = 1 MHz			13		Ω
DC PERFORMANCE							
V_{OS}	Input offset voltage				0.6	3	mV
		T_A = –40°C to +125°C			0.7	±3.6	
I_B	Input bias current					150	nA
		T_A = –40°C to +125°C			140	220	
		OPA2625 only, T_A = –40°C to +125°				250	
I_{OS}	Input offset current					20	nA
		T_A = –40°C to +125°C				25	
OPEN LOOP GAIN							
A_{OL}	Open-loop gain	T_A = –40°C to +125°C	(V–) + 0.2 V < V_O < (V+) – 0.2 V, R_{LOAD} = 600 Ω	74	100		dB
			(V–) + 0.15 V < V_O < (V+) – 0.15 V, R_{LOAD} = 10 kΩ	84	100		
INPUT VOLTAGE							
V_{CM}	Common-mode voltage range	T_A = –40°C to +125°C		(V–)		(V+) – 1.15	V
CMRR	Common-mode rejection ratio	(V–) < V_{COM} < (V+) – 1.15 V		66	114		dB
			T_A = –40°C to +125°C	60	114		
OUTPUT							
	Output voltage swing to rail	T_A = –40°C to +125°C	R_{LOAD} = 600 Ω			110	mV
			R_{LOAD} = 10 kΩ			40	
I_{sc}	Short-circuit current				50		mA
POWER SUPPLY							
I_Q	Quiescent current per amplifier	I_O = 0 mA, MODE connected to V+			250	270	µA
			T_A = –40°C to +125°C			400	

6.9 Switching Characteristics

at T_A = 25°C, V+ = 5 V, V– = 0 V, MODE pin connected to V– pin, gain (G) = 1 , V_{COM} = V_O = 2.5 V, C_{LOAD} = 20 pF, and R_{LOAD} = 1 kΩ connected to 2.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{LP\text{-}HD}$	Delay time, MODE pin falling (low-power mode to high-drive mode)	Settling time to within 50 µV of final value, MODE pin = high to low (LP to HD), V_O = 3.8 V		180		ns
		$t_{LP\text{-}HD}$ is defined as the time taken for the quiescent current to increase from 110% of its value in LP mode to 90% of its value in HD mode.		170		ns
$t_{HD\text{-}LP}$	Delay time, MODE pin rising (high-drive mode to low-power mode)	$t_{HD\text{-}LP}$ is defined as the time taken for the quiescent current to decrease from 90% of its value in HD mode to 110% of its value in LP mode.		300		ns

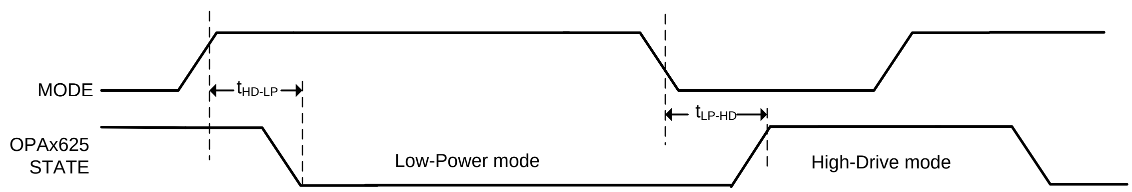
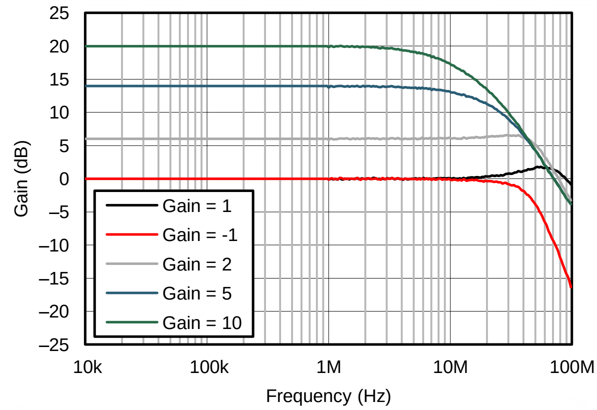


Figure 1. Switching Characteristics Timing Diagram

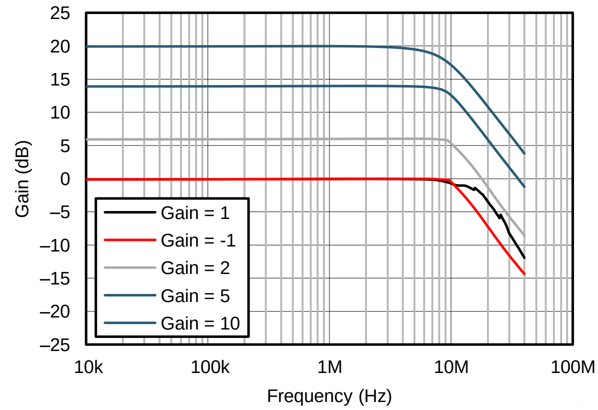
6.10 Typical Characteristics

At T_A = 25°C, V+ = 5 V, V– = 0 V, MODE = V–, V_{COM} = V_O = 2.5 V, gain (G) = 2, R_F = 1 kΩ, C_F= 2.7 pF, C_{LOAD}= 20 pF, and R_{LOAD} = 2 kΩ connected to 2.5 V (unless otherwise noted)



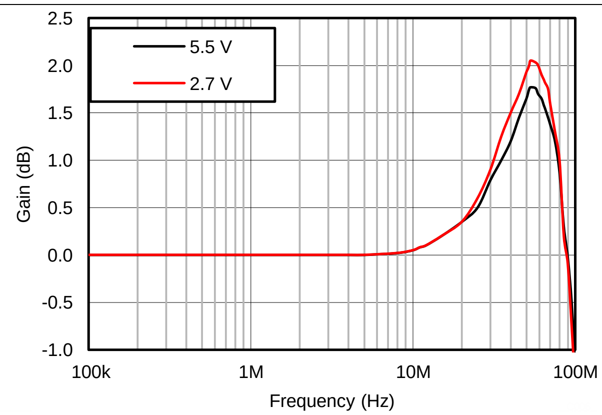
V_O = 10 mV_{PP}

Figure 2. Small-Signal Frequency Response for Various Gains



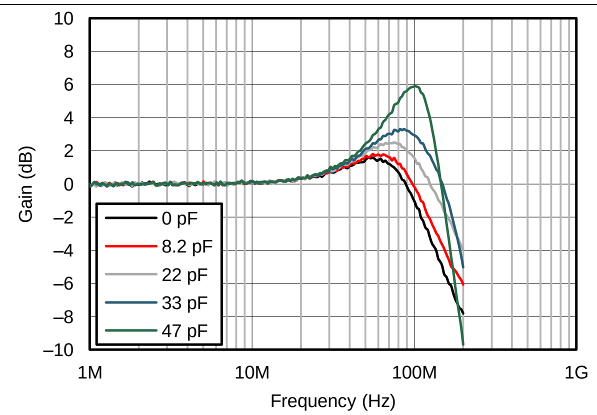
V_O = 2 V_{PP}

Figure 3. Large-Signal Frequency Response for Various Gains



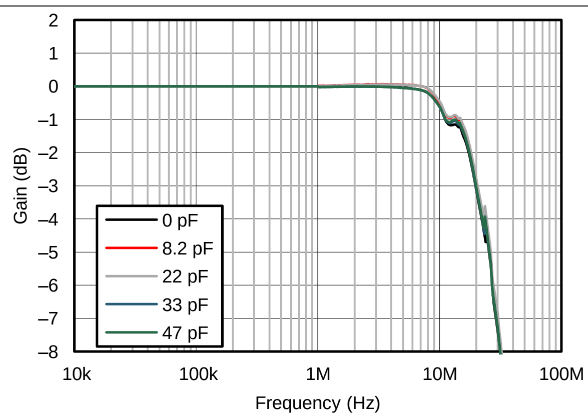
V_O = 10 mV_{PP}, G = 1

Figure 4. Small-Signal Frequency Response for Various Power Supply Voltages



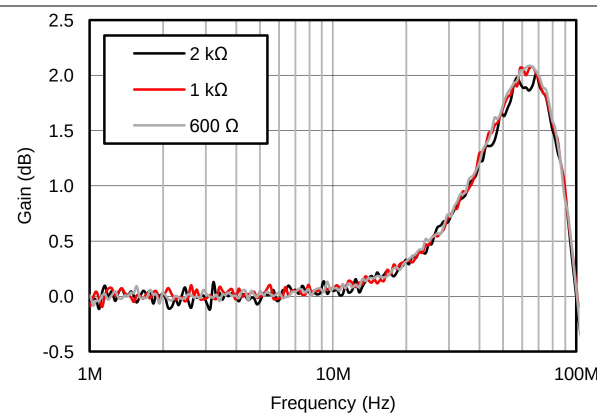
V_O = 10 mV_{PP} , G = 1

Figure 5. Small-Signal Frequency Response for Various Capacitive Loads



V_O = 2 V_{PP}, G = 1

Figure 6. Large-Signal Frequency Response for Various Capacitive Loads



V_O = 10 mV_{PP} , G = 1

Figure 7. Small-Signal Frequency Response for Various Resistive Loads

Typical Characteristics (continued)

At T_A = 25°C, V+ = 5 V, V– = 0 V, MODE = V–, V_{COM} = V_O = 2.5 V, gain (G) = 2, R_F = 1 kΩ, C_F= 2.7 pF, C_{LOAD}= 20 pF, and R_{LOAD} = 2 kΩ connected to 2.5 V (unless otherwise noted)

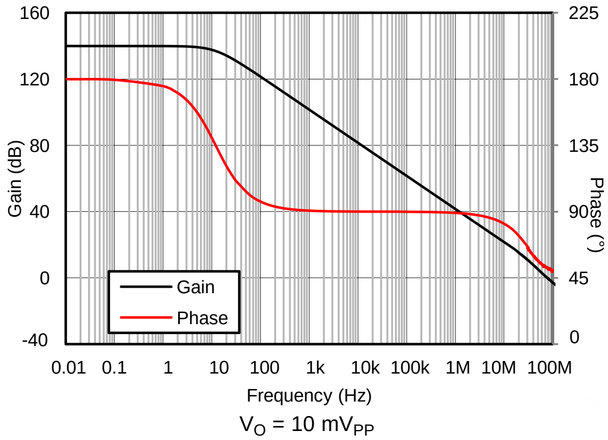


Figure 8. High-Drive Mode Open-Loop Gain and Phase vs Frequency

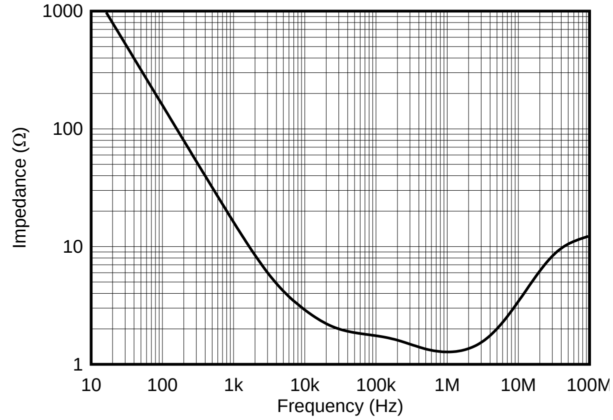


Figure 9. High-Drive Mode Open-Loop Output Impedance vs Frequency

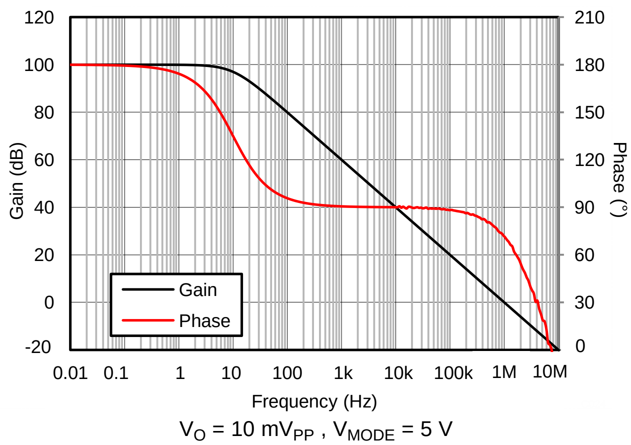


Figure 10. Low-Power Mode Open-Loop Gain and Phase vs Frequency

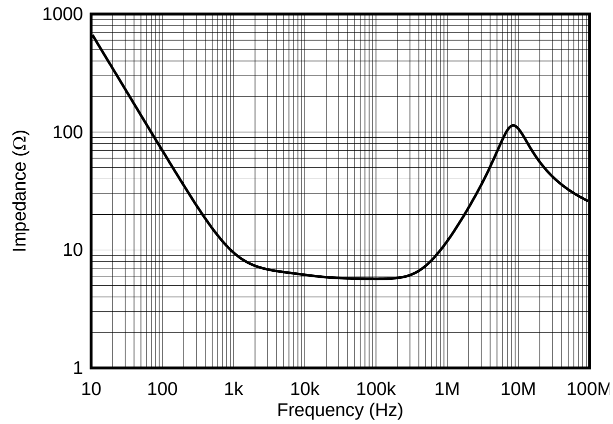


Figure 11. Low-Power Mode Open-Loop Output Impedance vs Frequency

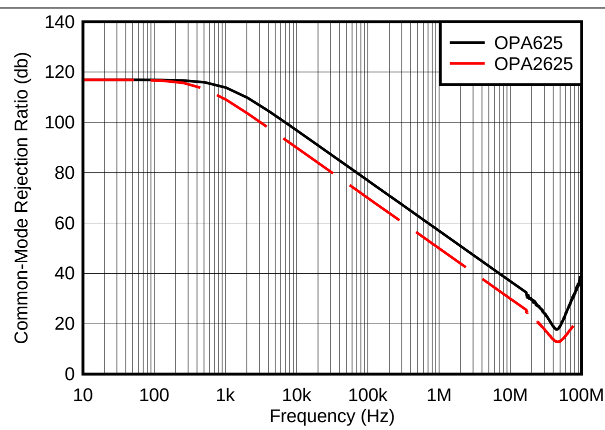


Figure 12. Common-Mode Rejection Ratio vs Frequency

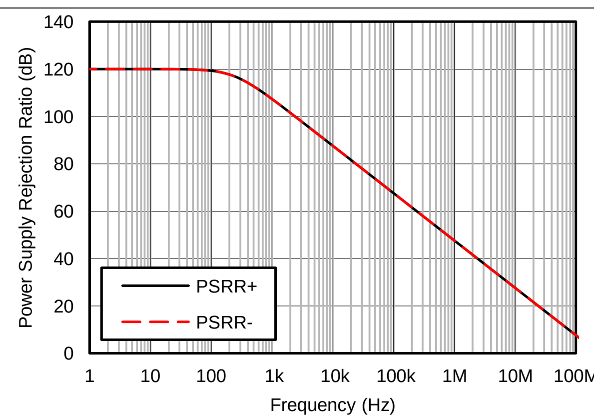
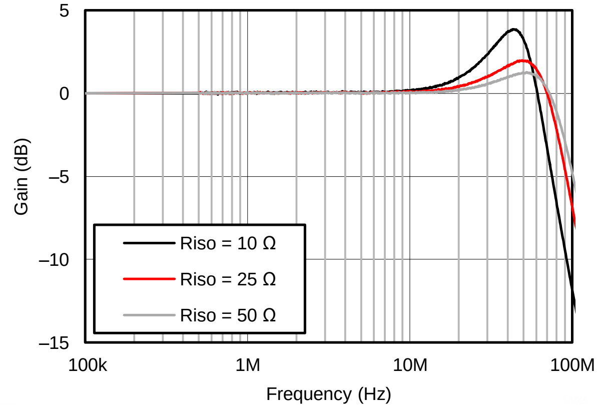


Figure 13. Power-Supply Rejection Ratio vs Frequency

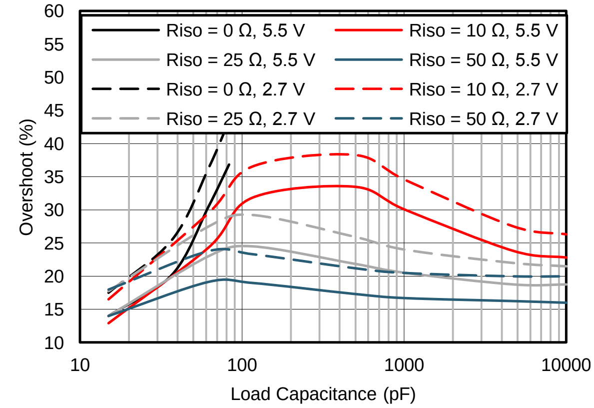
Typical Characteristics (continued)

At T_A = 25°C, V+ = 5 V, V– = 0 V, MODE = V–, V_{COM} = V_O = 2.5 V, gain (G) = 2, R_F = 1 kΩ, C_F= 2.7 pF, C_{LOAD}= 20 pF, and R_{LOAD} = 2 kΩ connected to 2.5 V (unless otherwise noted)



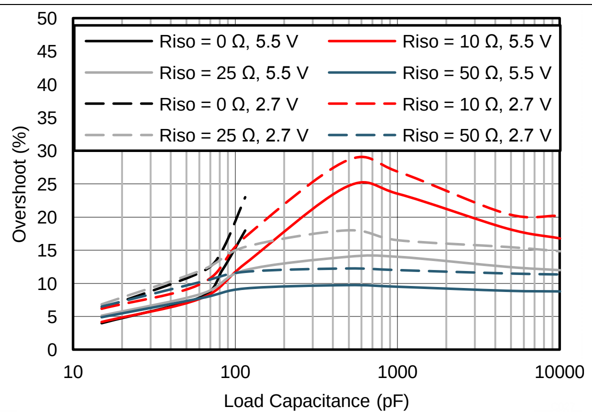
G = 1, C_{LOAD} = 1.2 nF

Figure 14. Series Resistance for Capacitive Load Stability



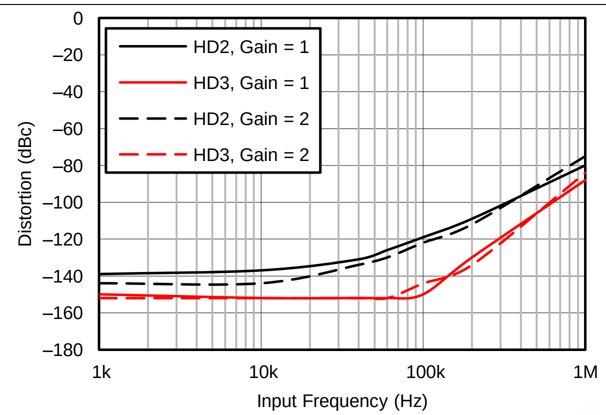
G = 1, V_O = 10 mV_{PP}

Figure 15. Overshoot vs Capacitive Load, G = 1



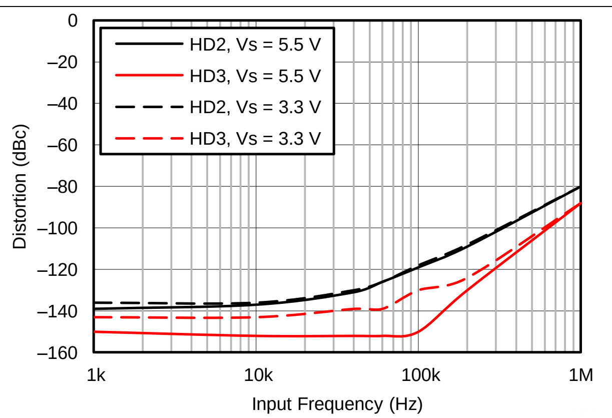
G = –1, V_O = 10 mV_{PP}

Figure 16. Overshoot vs Capacitive Load, G = –1



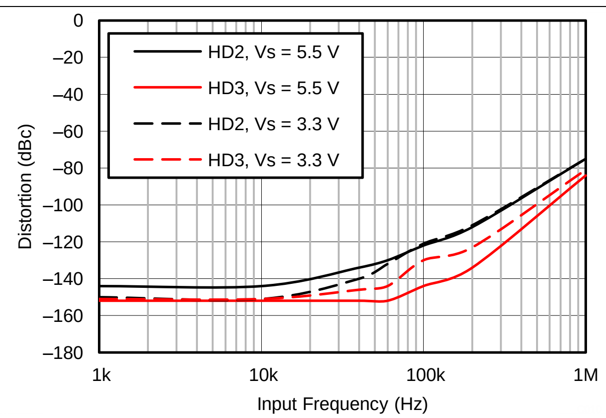
V_S = 5.5 V, V_O = 2 V_{PP}, R_{LOAD} = 600 Ω

Figure 17. Distortion vs Frequency for Various Gains



G = 1, V_O = 2 V_{PP}, R_{LOAD} = 600 Ω

Figure 18. Distortion vs Frequency for Various Power Supplies



G = 2, V_O = 2 V_{PP}, R_{LOAD} = 600 Ω

Figure 19. Distortion vs Frequency for Various Power Supplies

Typical Characteristics (continued)

At T_A = 25°C, V+ = 5 V, V– = 0 V, MODE = V–, V_{COM} = V_O = 2.5 V, gain (G) = 2, R_F = 1 kΩ, C_F= 2.7 pF, C_{LOAD}= 20 pF, and R_{LOAD} = 2 kΩ connected to 2.5 V (unless otherwise noted)

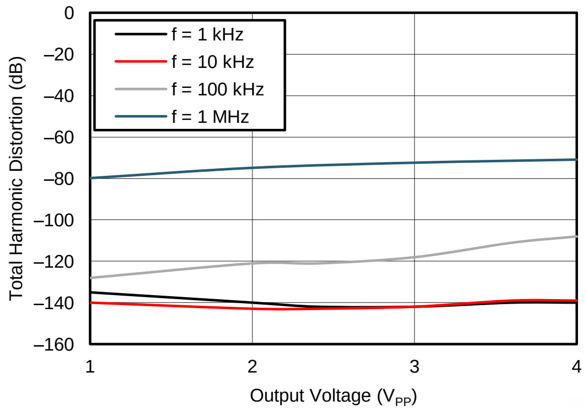


Figure 20. Total Harmonic Distortion vs Output Voltage for Various Frequencies

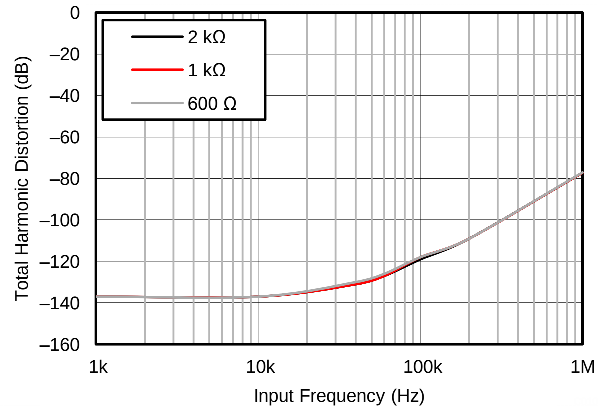


Figure 21. Total Harmonic Distortion vs Frequency for Various Loads

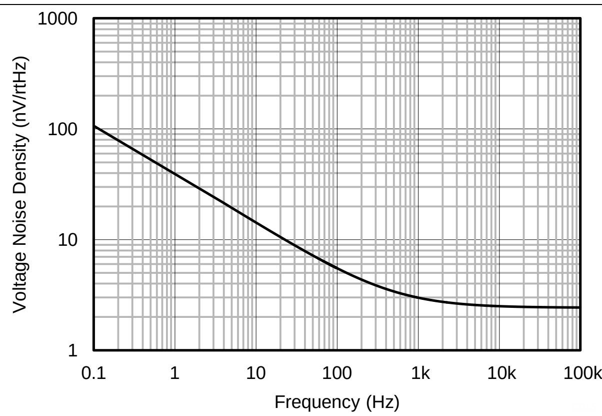


Figure 22. Voltage Noise Density vs Frequency

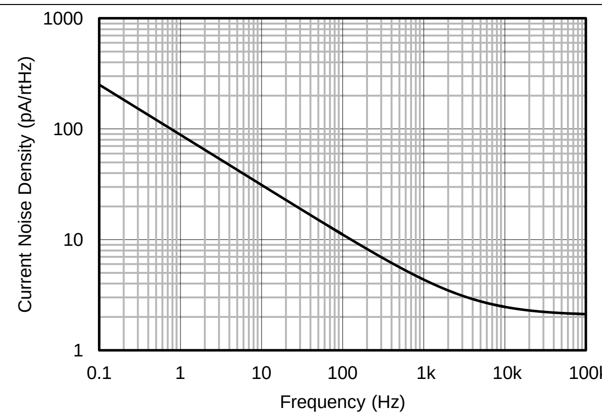


Figure 23. Current Noise Density vs Frequency

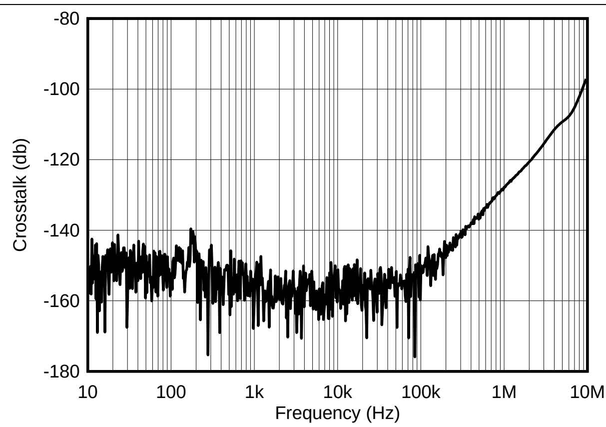


Figure 24. Crosstalk vs Frequency

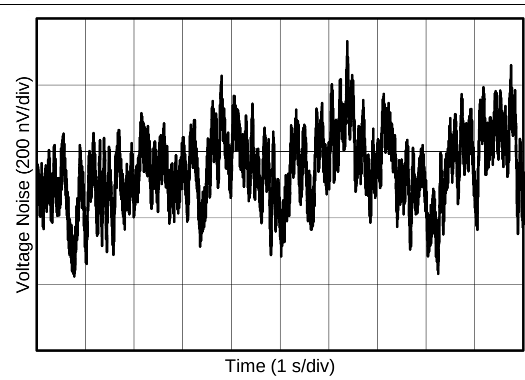


Figure 25. 0.1-Hz to 10-Hz Voltage Noise

Typical Characteristics (continued)

At T_A = 25°C, V+ = 5 V, V– = 0 V, MODE = V–, V_{COM} = V_O = 2.5 V, gain (G) = 2, R_F = 1 kΩ, C_F= 2.7 pF, C_{LOAD}= 20 pF, and R_{LOAD} = 2 kΩ connected to 2.5 V (unless otherwise noted)

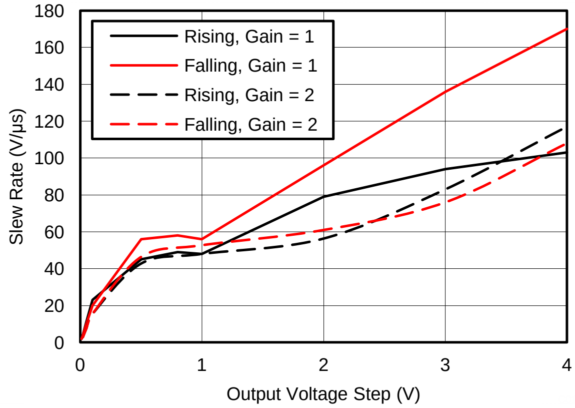


Figure 26. Slew Rate vs Output Step Size

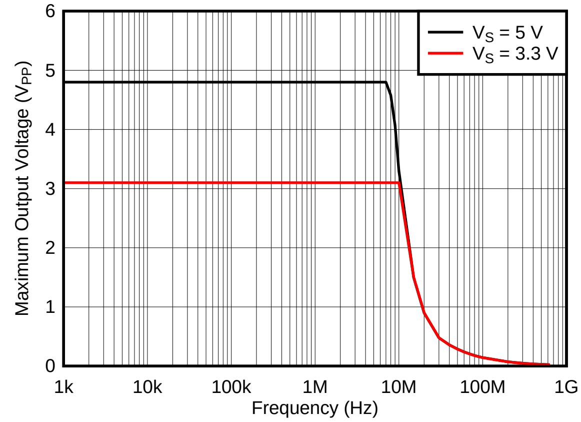
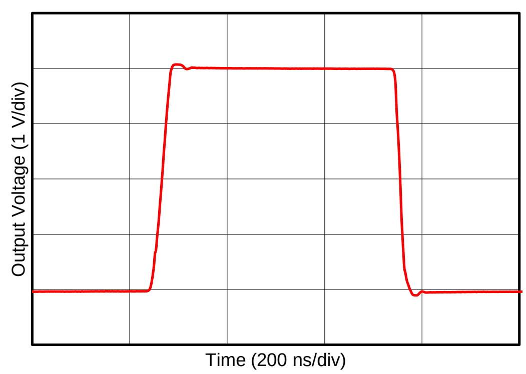
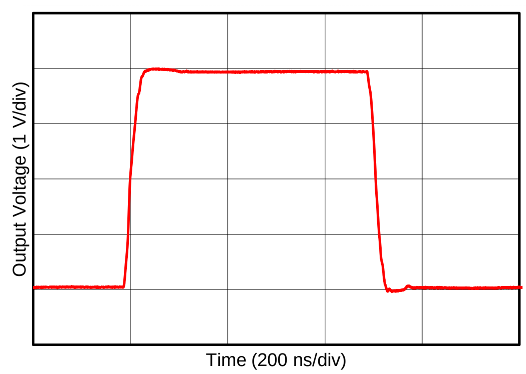


Figure 27. Maximum Output Voltage vs Frequency



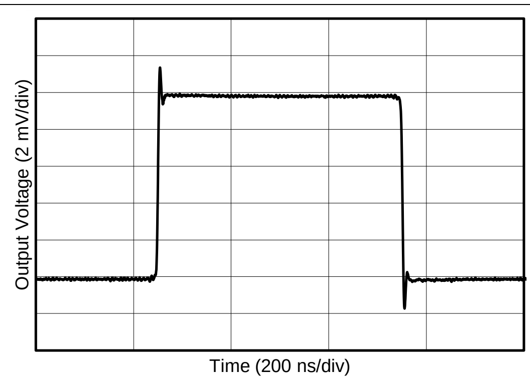
G = 1, V_O = 4-V step

Figure 28. Large-Signal Pulse Response



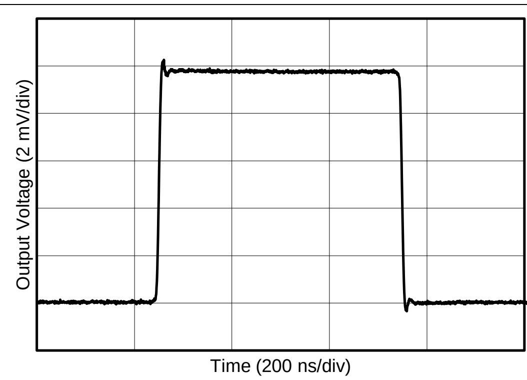
G = –1, V_O = 4-V step

Figure 29. Large-Signal Pulse Response



G = 1, V_O = 10-mV step

Figure 30. Small-Signal Pulse Response

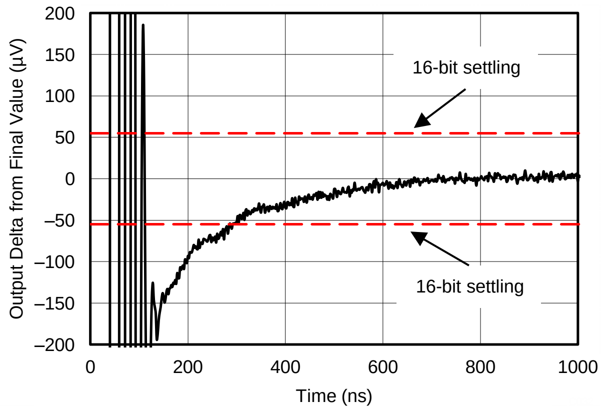


G = –1, V_O = 10-mV step

Figure 31. Small-Signal Pulse Response

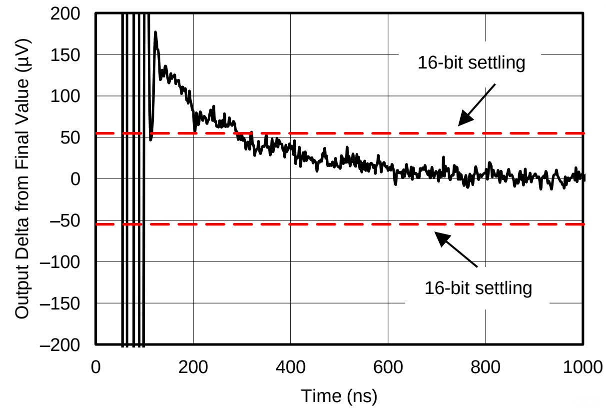
Typical Characteristics (continued)

At T_A = 25°C, V+ = 5 V, V– = 0 V, MODE = V–, V_{COM} = V_O = 2.5 V, gain (G) = 2, R_F = 1 kΩ, C_F= 2.7 pF, C_{LOAD}= 20 pF, and R_{LOAD} = 2 kΩ connected to 2.5 V (unless otherwise noted)



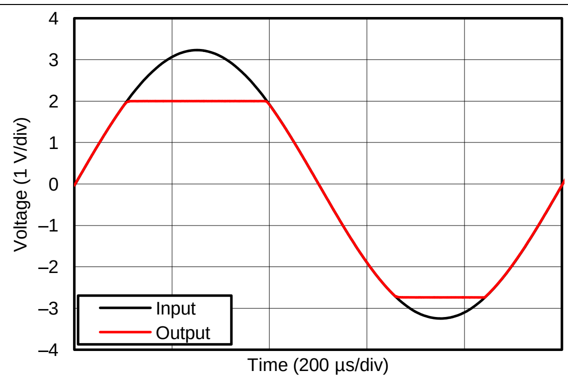
V_O = 3.6-V step at t = 0 s

Figure 32. 16-Bit Negative Settling Time



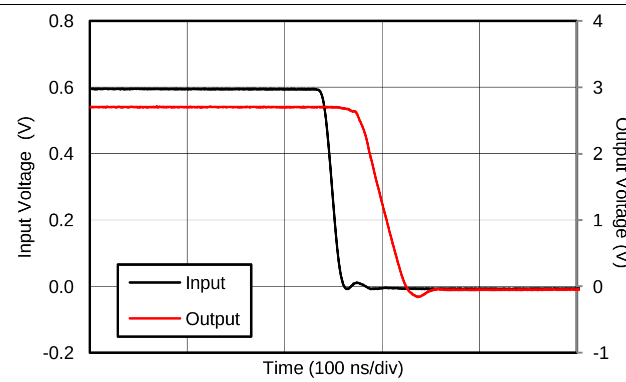
V_O = 3.6-V step at t = 0 s

Figure 33. 16-Bit Positive Settling Time



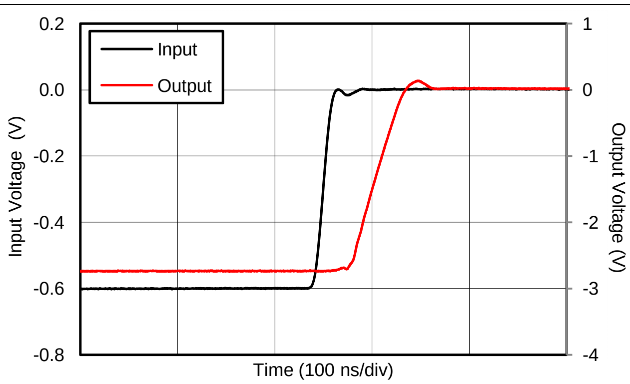
V_S = ±2.75 V, G = 1

Figure 34. No Phase Reversal



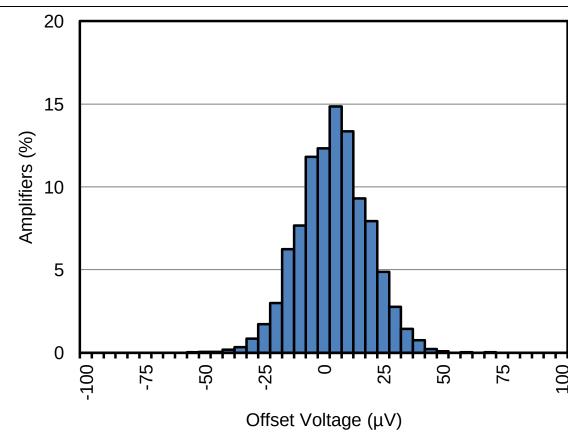
V_S = ±2.75 V, G = 5

Figure 35. Positive Overload Recovery



V_S = ±2.75 V, G = 5

Figure 36. Negative Overload Recovery

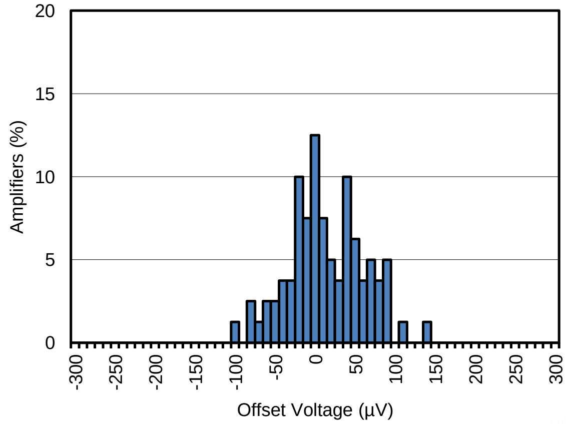


Distribution taken from 3139 amplifiers

Figure 37. Input Offset Voltage Distribution

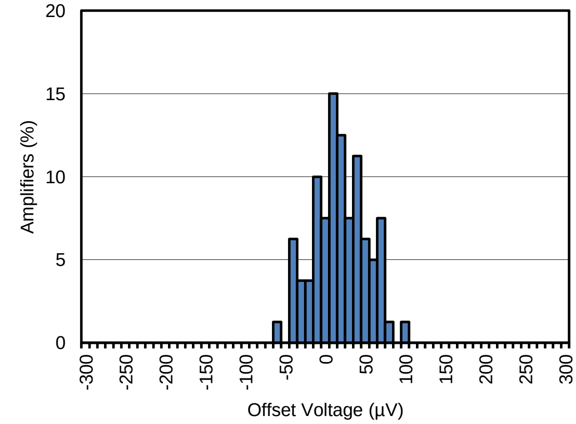
Typical Characteristics (continued)

At T_A = 25°C, V+ = 5 V, V– = 0 V, MODE = V–, V_{COM} = V_O = 2.5 V, gain (G) = 2, R_F = 1 kΩ, C_F= 2.7 pF, C_{LOAD}= 20 pF, and R_{LOAD} = 2 kΩ connected to 2.5 V (unless otherwise noted)



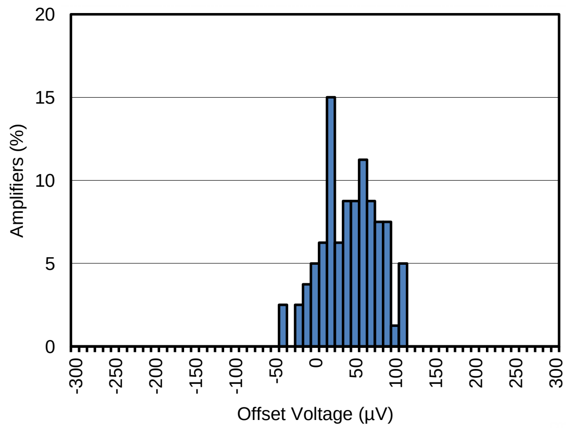
Distribution taken from 80 amplifiers, T_A = 125°C

Figure 38. Input Offset Voltage Distribution



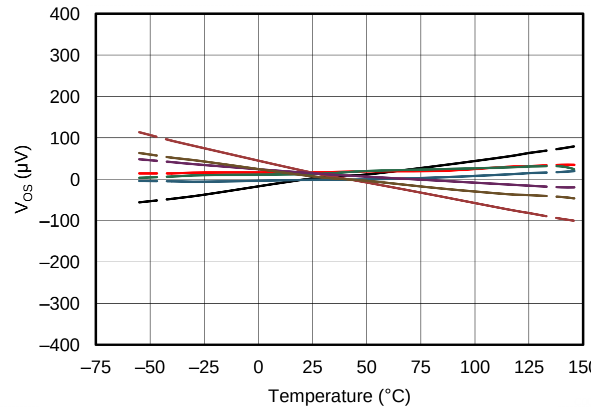
Distribution taken from 80 amplifiers, T_A = 85°C

Figure 39. Input Offset Voltage Distribution



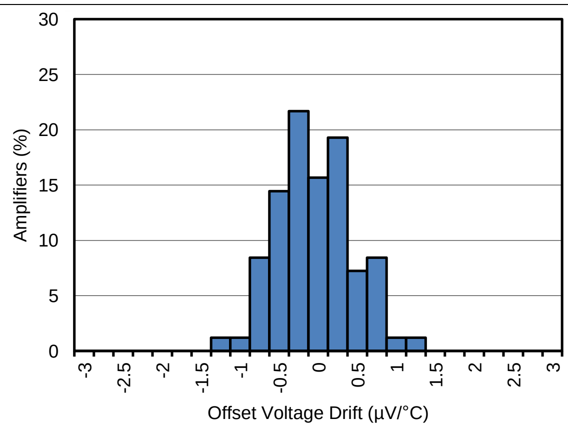
Distribution taken from 80 amplifiers, T_A = –40°C

Figure 40. Input Offset Voltage Distribution



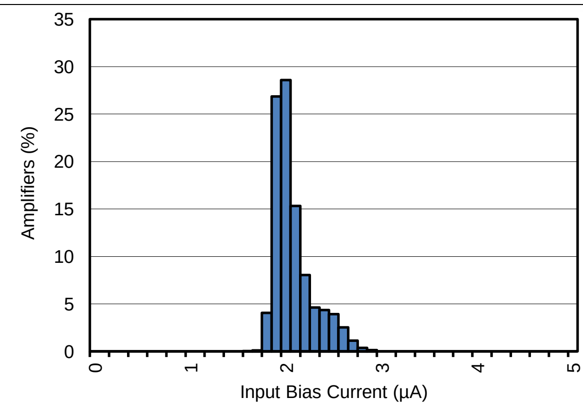
7 typical units shown

Figure 41. Input Offset Voltage vs Temperature



Distribution taken from 83 amplifiers, T_A = –40°C to +125°C

Figure 42. Input Offset Voltage Drift Distribution



Distribution taken from 3139 amplifiers

Figure 43. Input Bias Current Distribution

Typical Characteristics (continued)

At T_A = 25°C, V+ = 5 V, V– = 0 V, MODE = V–, V_{COM} = V_O = 2.5 V, gain (G) = 2, R_F = 1 kΩ, C_F= 2.7 pF, C_{LOAD}= 20 pF, and R_{LOAD} = 2 kΩ connected to 2.5 V (unless otherwise noted)

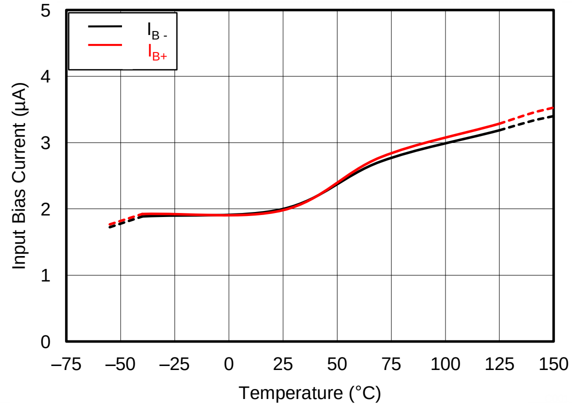
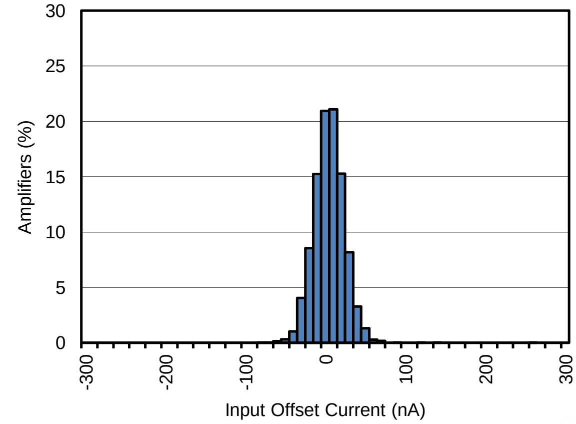


Figure 44. Input Bias Current vs Temperature



Distribution taken from 3139 amplifiers

Figure 45. Input Offset Current Distribution

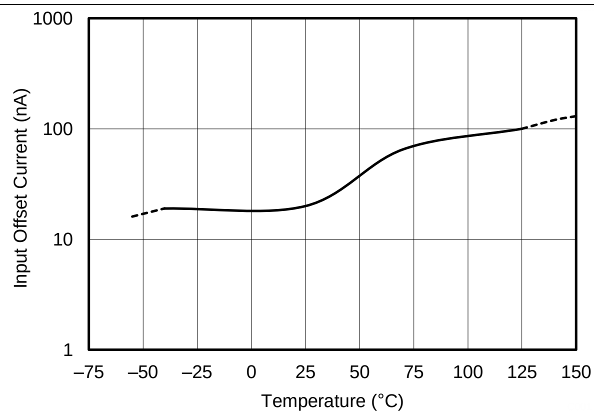


Figure 46. Input Offset Current vs Temperature

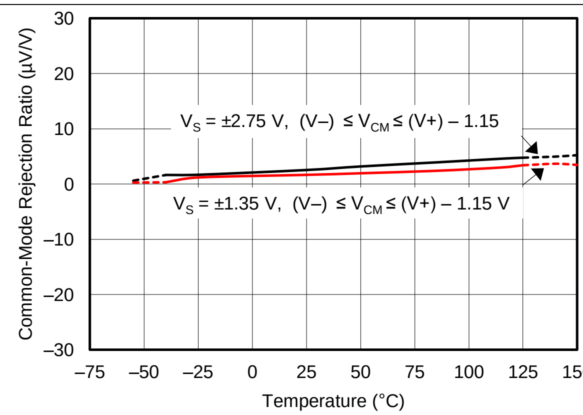
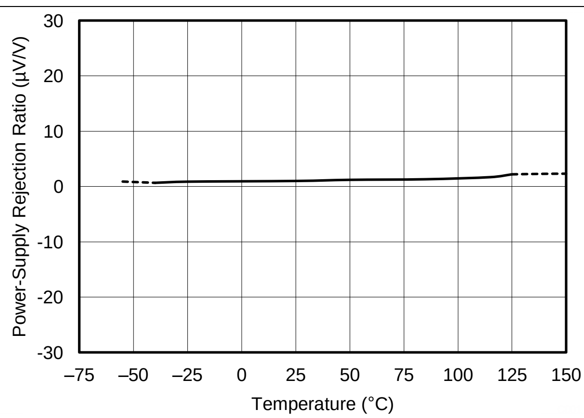
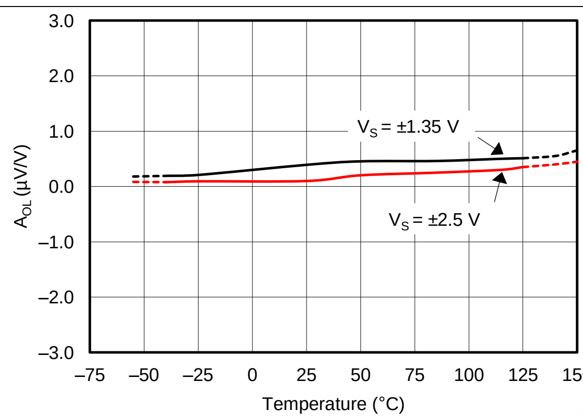


Figure 47. Common-Mode Rejection Ratio vs Temperature



2.7 V ≤ V_S ≤ 5.5 V

Figure 48. Power-Supply Rejection Ratio vs Temperature

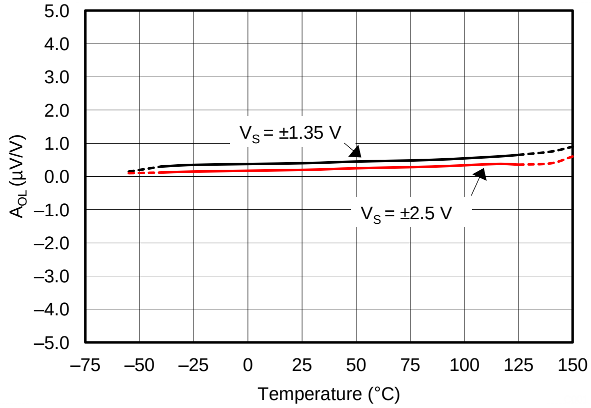


R_{LOAD} = 10 kΩ

Figure 49. Open-Loop Gain vs Temperature with 10-kΩ Load

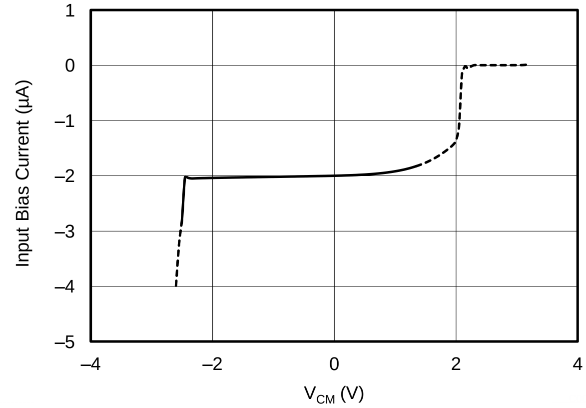
Typical Characteristics (continued)

At T_A = 25°C, V+ = 5 V, V– = 0 V, MODE = V–, V_{COM} = V_O = 2.5 V, gain (G) = 2, R_F = 1 kΩ, C_F= 2.7 pF, C_{LOAD}= 20 pF, and R_{LOAD} = 2 kΩ connected to 2.5 V (unless otherwise noted)



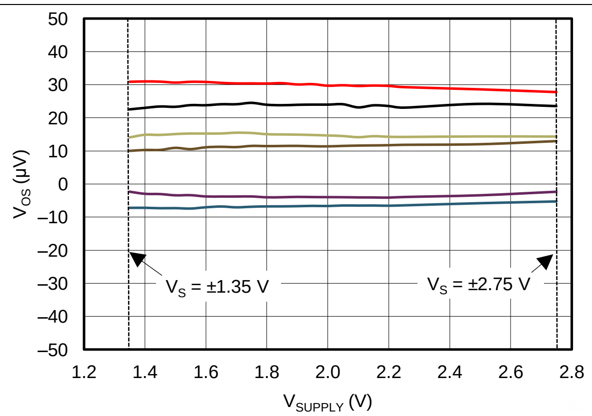
R_{LOAD} = 600 Ω

Figure 50. Open-Loop Gain vs Temperature with 600-Ω Load



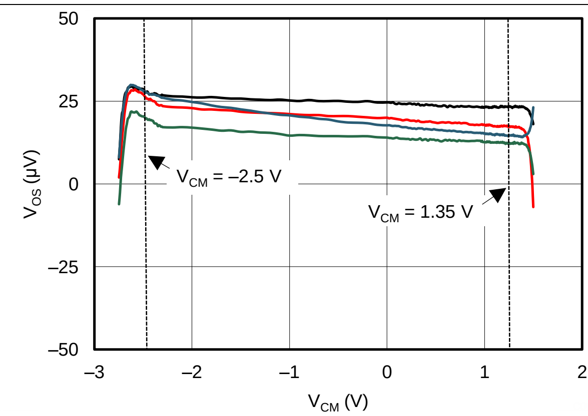
High-drive mode, V_S = ±2.5 V

Figure 51. Input Bias Current vs Input Common-Mode Voltage



6 typical units shown, V_S = ±1.35 V to ±2.75 V

Figure 52. Input Offset Voltage vs Power-Supply Voltage



6 typical units shown, V_S = ±2.5 V

Figure 53. Input Offset Voltage vs Common-Mode Voltage

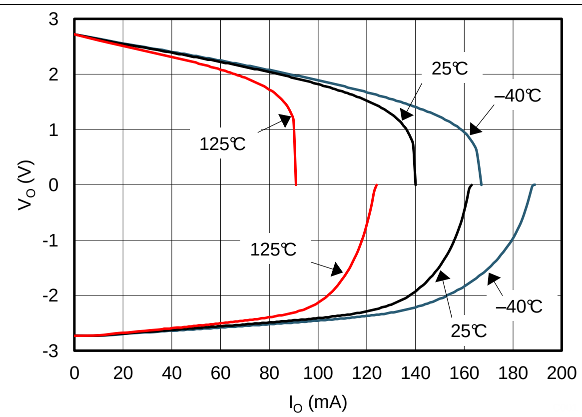


Figure 54. Output Voltage vs Output Current

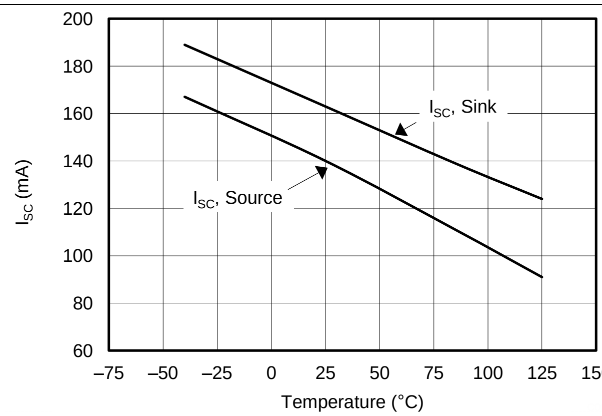
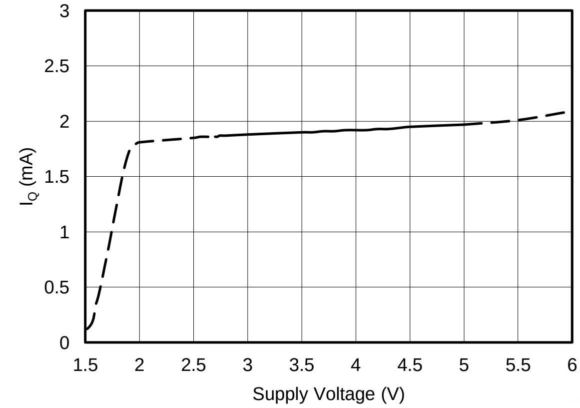


Figure 55. Short-Circuit Current vs Temperature

Typical Characteristics (continued)

At T_A = 25°C, V+ = 5 V, V– = 0 V, MODE = V–, V_{COM} = V_O = 2.5 V, gain (G) = 2, R_F = 1 kΩ, C_F= 2.7 pF, C_{LOAD}= 20 pF, and R_{LOAD} = 2 kΩ connected to 2.5 V (unless otherwise noted)



High-drive mode

Figure 56. High-Drive Mode Quiescent Current vs Power-Supply Voltage

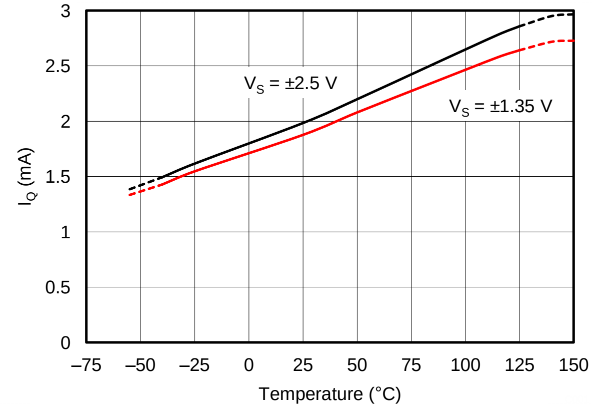
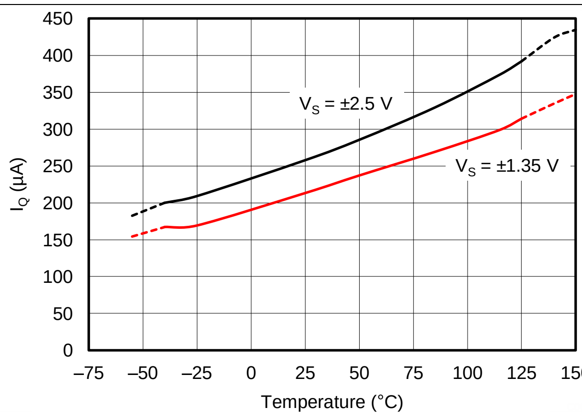
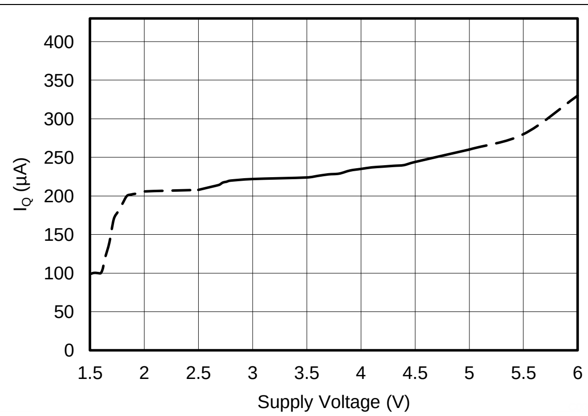


Figure 57. High-Drive Mode Quiescent Current vs Temperature



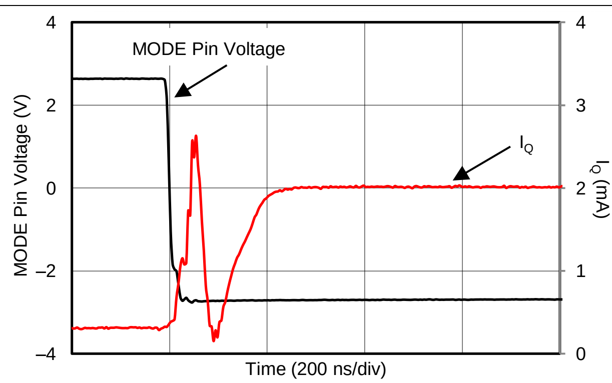
MODE pin connected to V+

Figure 58. Low-Power Mode Quiescent Current vs Temperature



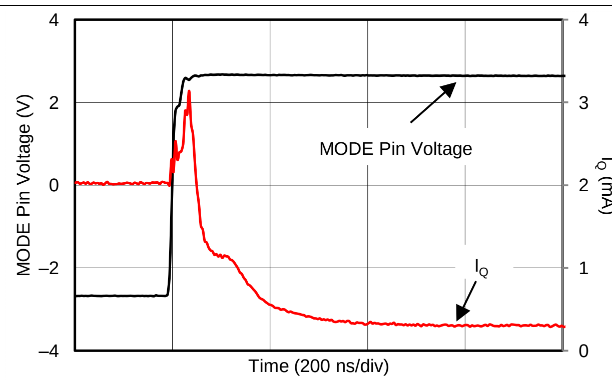
Low-drive mode, MODE pin connected to V+

Figure 59. Low-Power Mode Quiescent Current vs Power-Supply Voltage



V_S = ±2.75 V

Figure 60. Quiescent Current When MODE transitions From High To Low

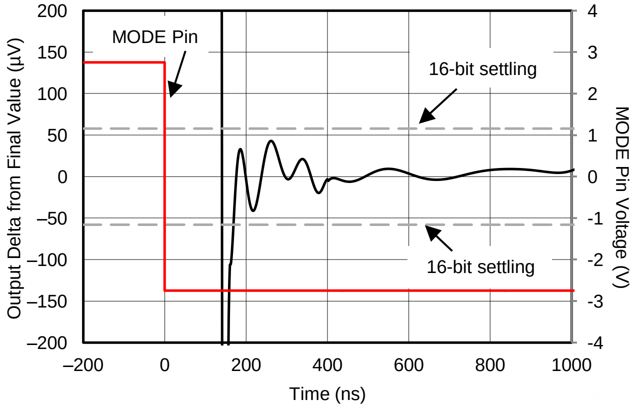


V_S = ±2.75 V

Figure 61. Quiescent Current When MODE Transitions From Low To High

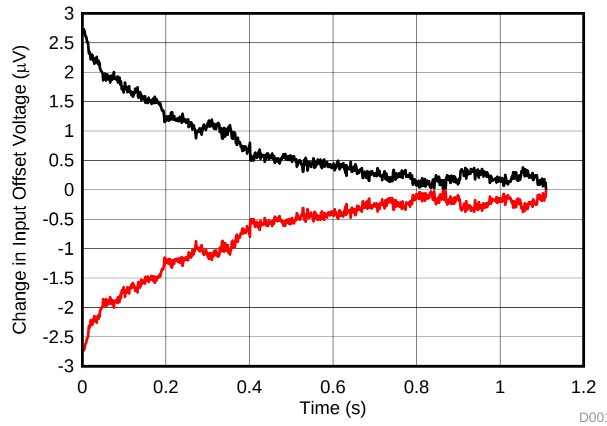
Typical Characteristics (continued)

At T_A = 25°C, V+ = 5 V, V– = 0 V, MODE = V–, V_{COM} = V_O = 2.5 V, gain (G) = 2, R_F = 1 kΩ, C_F= 2.7 pF, C_{LOAD}= 20 pF, and R_{LOAD} = 2 kΩ connected to 2.5 V (unless otherwise noted)



V_O = 3.8 VDC

Figure 62. Output Voltage When MODE Transitions From High To Low



OPA625 powered on in high-drive mode at t = 0 s, PCB dimensions: 4 in^2, 2 layer, FR4

Figure 63. Warm-Up Time

7 Parameter Measurement Information

7.1 DC Parameter Measurements

The circuit shown in Figure 64 is used to measure the dc input offset related parameters of the OPAx625. Input offset voltage, power supply rejection ratio, common mode rejection ratio and open loop gain can be measured with this circuit. The basic test procedure requires setting the inputs (the power-supply voltage, V_S, and the common-mode voltage, V_{CM}), to the desired values. V_O is set to the desired value by adjusting the loop-drive voltage while measuring V_O. After all inputs are configured, measure the input offset at the V_X measurement point. Calculate the input offset voltage by dividing the measured result by 101. Changing the voltages on the various inputs changes the input offset voltage. The input parameters can be measured according to the relationships illustrated in Equation 1 through Equation 5.

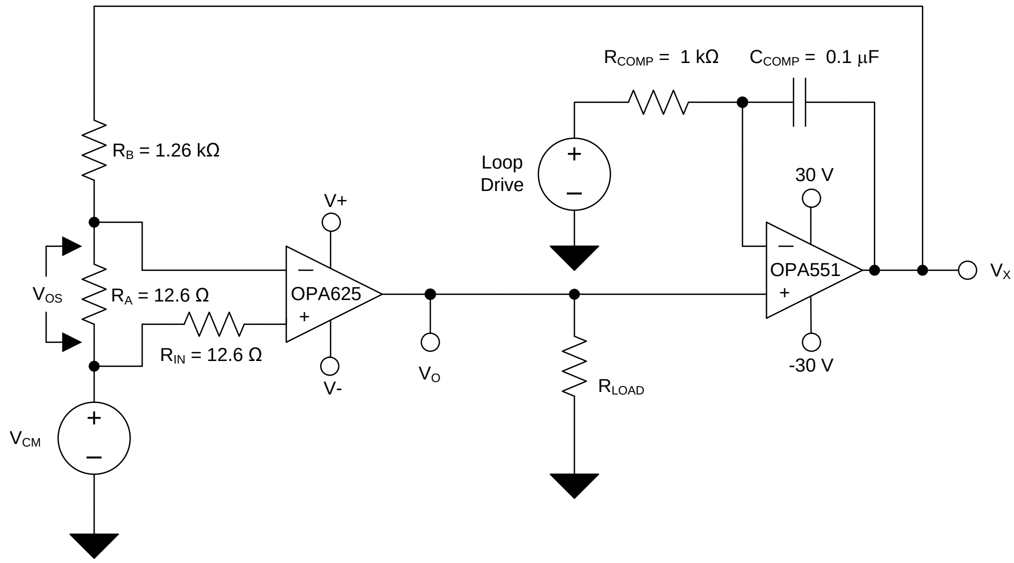


Figure 64. DC-Parameters Measurement Circuit

$$V_{OS} = \frac{V_X}{101} \tag{1}$$

$$V_{OSDrift} = \frac{\Delta V_{OS}}{\Delta Temperature} \tag{2}$$

$$PSRR = \frac{\Delta V_{OS}}{\Delta V_{SUPPLY}} \tag{3}$$

$$CMRR = \frac{\Delta V_{OS}}{\Delta V_{CM}} \tag{4}$$

$$AOL = \frac{\Delta V_O}{\Delta V_{OS}} \tag{5}$$

7.2 Transient Parameter Measurements

The circuit shown in Figure 65 is used to measure the transient response of the OPAx625. Configure V+, V–, R_{ISO}, R_{LOAD}, and C_{LOAD} as desired. Monitor the input and output voltages on an oscilloscope or other signal analyzer. Use this circuit to measure large-signal and small-signal transient response, slew rate, overshoot, and capacitive-load stability.

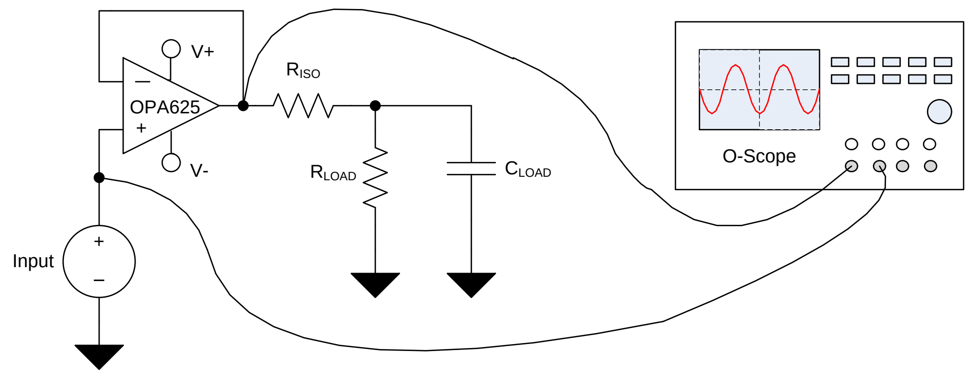


Figure 65. Pulse-Response Measurement Circuit

7.3 AC Parameter Measurements

The circuit shown in Figure 66 is used to measure the ac parameters of the OPAx625. Configure V+, V–, and C_{LOAD} as desired. The THS4271 are used to buffer the input and output of the OPAx625 to prevent loading by the gain phase analyzer. Monitor the input and output voltages on a gain phase analyzer. Use this circuit to measure the gain bandwidth product, and open-loop gain versus frequency versus capacitive load.

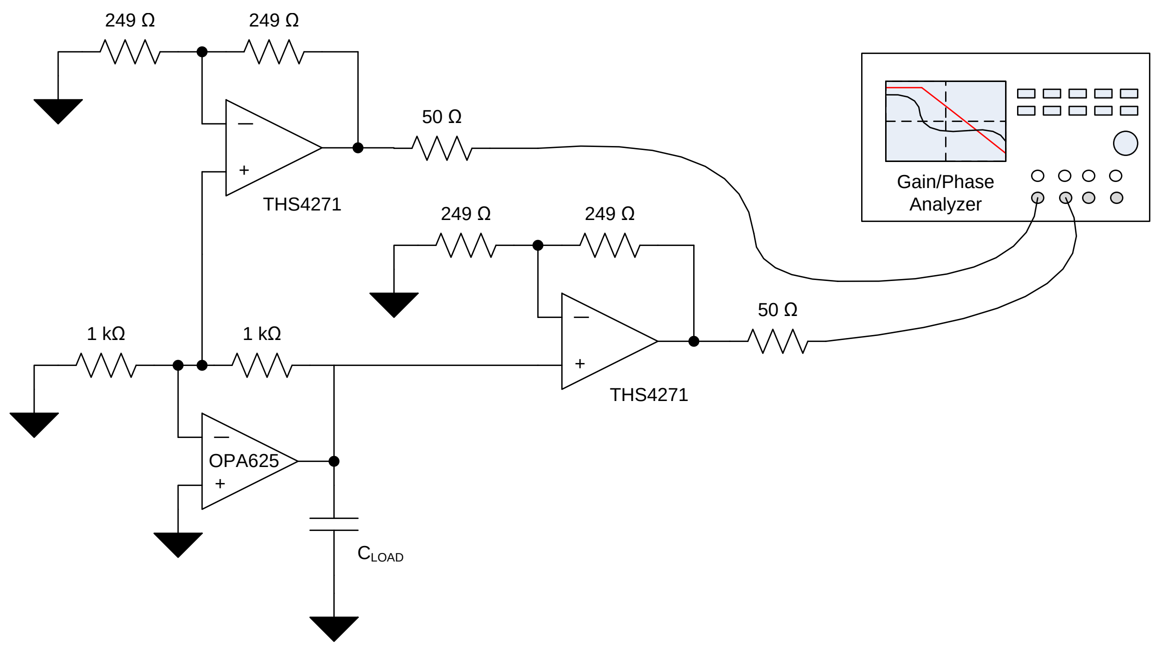


Figure 66. AC-Parameters Measurement Circuit

7.4 Noise Parameter Measurements

The circuit shown in Figure 67 is used to measure the voltage noise of the OPAx625. Configure V+, V–, and C_{LOAD} as desired.

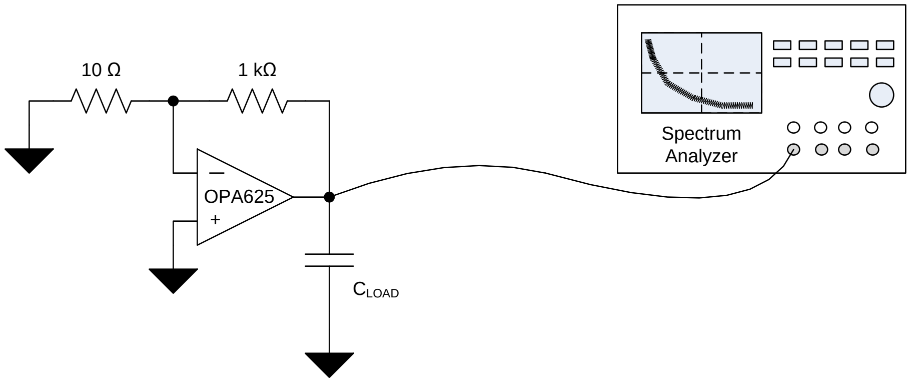


Figure 67. Voltage Noise Measurement Circuit

The circuit shown in Figure 68 is used to measure the current noise of the OPAx625. Configure V+, V– and C_{LOAD} as desired.

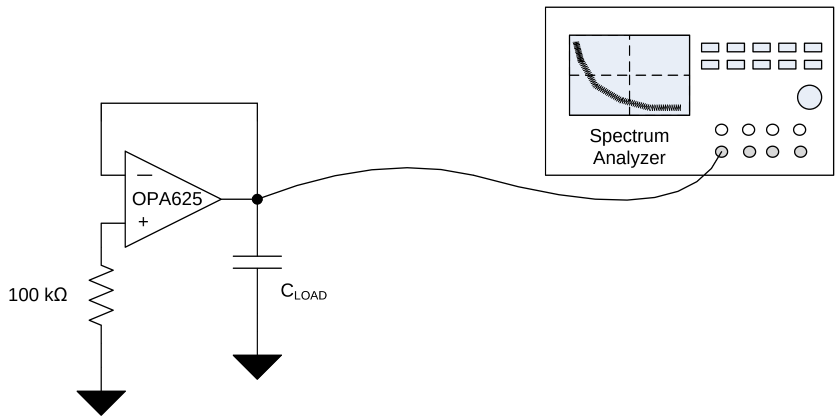


Figure 68. Current Noise Measurement Circuit

The circuit shown in Figure 69 is used to measure the OPAx625 0.1-Hz to 10-Hz voltage noise. Configure V+, V–, and C_{LOAD} as desired.

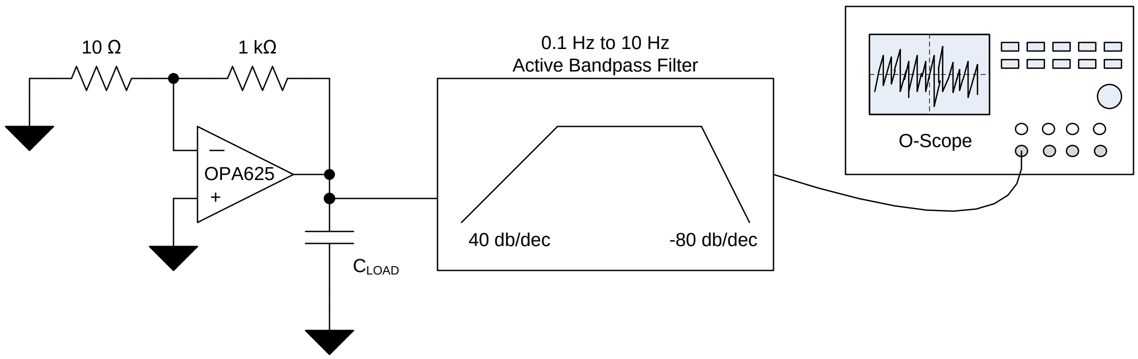


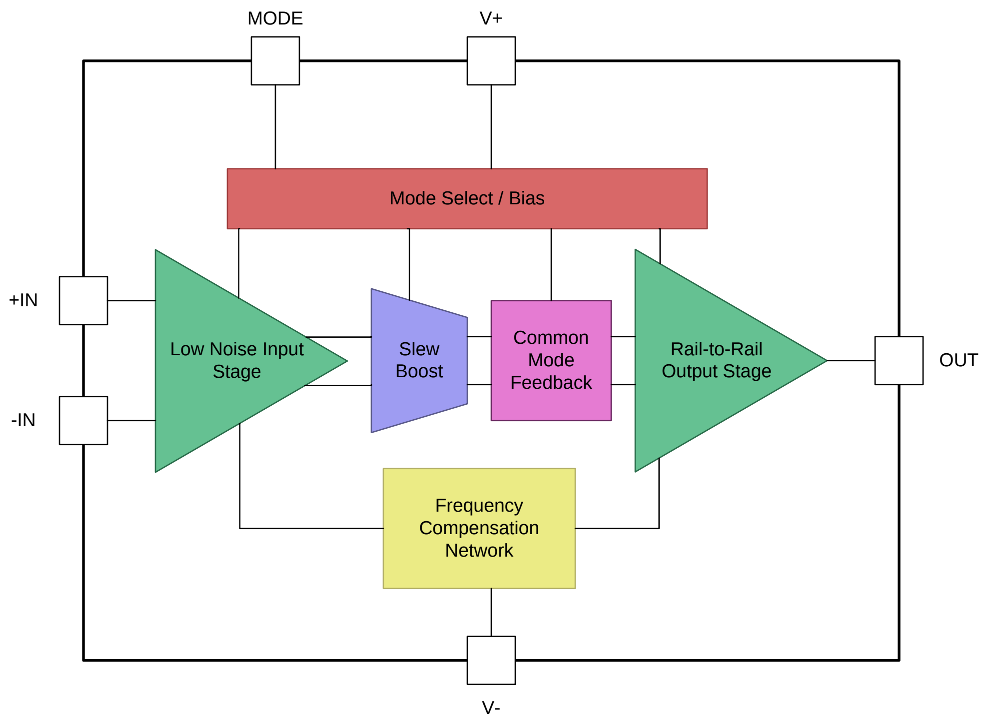
Figure 69. 0.1-Hz to 10-Hz Voltage-Noise Measurement Circuit

8 Detailed Description

8.1 Overview

The OPAx625 is a fast-settling, high slew rate, high-bandwidth, voltage-feedback operational amplifier. Low offset and low offset drift combine with the superior dynamic performance and very low output impedance, resulting in an amplifier suited for driving 16-bit SAR ADCs, and buffering precision voltage references in industrial applications. The OPAx625 is comprised of a low-noise input stage, a slew boost stage, and a rail-to-rail output stage. A mode bias select feature allows the OPAx625 to be configured in a high-drive mode and a low-power mode. High-drive mode is used when driving SAR ADCs during the ADC signal acquisition period. The OPAx625 is also configurable in low-power mode while the SAR ADC is converting the acquired signal, thus saving overall system power. To facilitate a fast transition from low-power mode to high-drive mode, the OPAx625 does not completely shut down while in low-power mode; rather, the device remains as an active amplifier with a lower bandwidth (1 MHz) and relaxed dc specifications.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 SAR ADC Driver

The OPAx625 is designed to drive precision (16-bit and 18-bit) SAR ADCs at sample rates up to 1 MSPS. The combination of low output impedance, low THD, low noise, and fast settling time make the OPAx625 the ideal choice for driving both the SAR ADC inputs, as well as the reference input to the ADC. Internal slew boost circuitry increases the slew rate as a function of the input signal magnitude, resulting in settling from a 4-V step input to 16-bit levels within 280 ns. Low output impedance (1 Ω at 1 MHz) ensures capacitive load stability with minimal overshoot.

8.3.2 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress (EOS). These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly. Having a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event is helpful. See Figure 70 for an illustration of the ESD circuits contained in the OPAx625. The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device or the power-supply ESD cell, internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

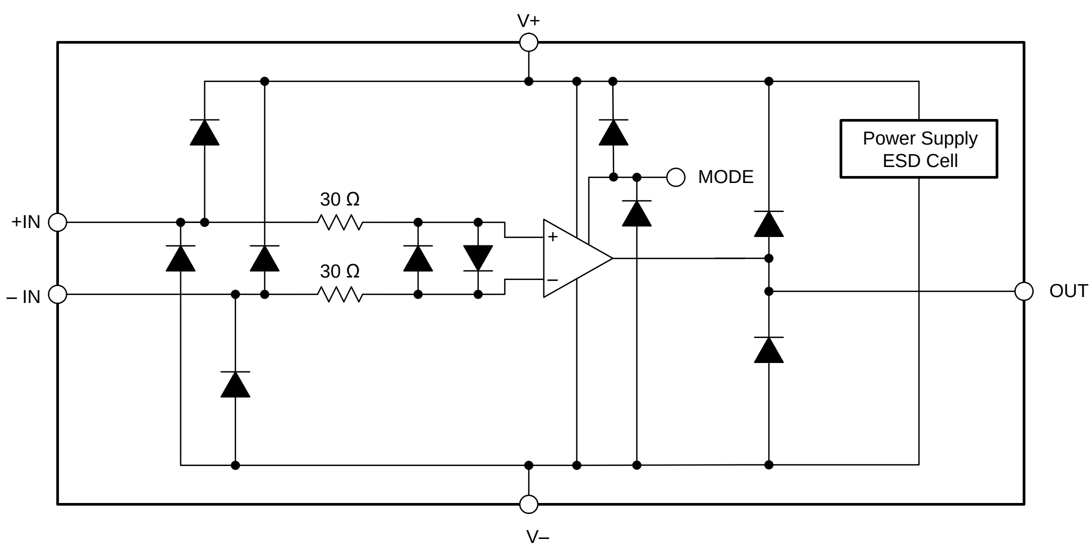


Figure 70. Simplified ESD Circuit

8.4 Device Functional Modes

The OPAx625 has two functional modes: high-drive and low-power. In low-power mode, the quiescent current of the OPAx625 is reduced to 270 µA (typ), and results in significantly lower bandwidth, higher noise, and lower output current drive. The OPAx625 transitions from low-power mode to high-drive mode in 170 ns.

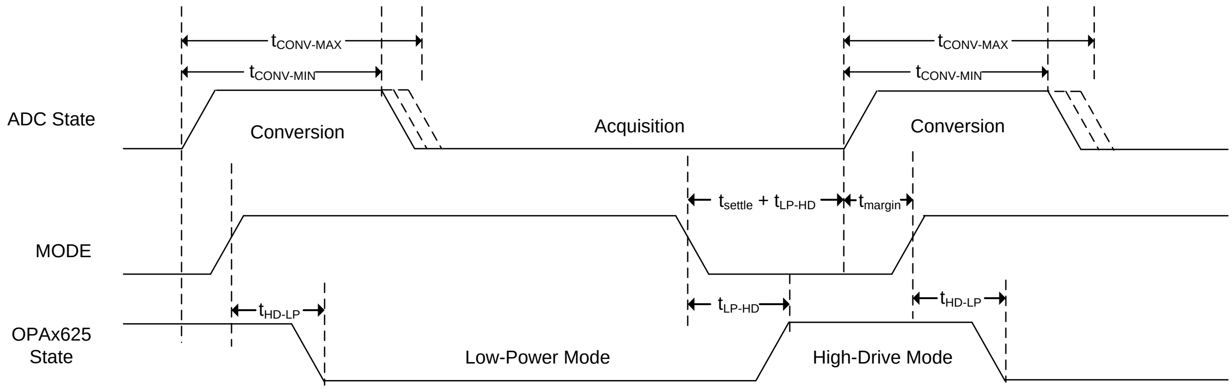


Figure 71. Simplified Timing Diagram: Power-Scaling Precision Signal Chain

8.4.1 High-Drive Mode

Place the OPAx625 into high-drive mode by applying a logic level low to the MODE pin. The MODE pin can be driven by a general-purpose input/output (GPIO) from the system controller, from discrete logic gates, or can be connected directly to the V– pin. Do not leave the MODE pin floating. When driving the MODE pin from a microcontroller GPIO, make sure that the GPIO is not placed into a high-impedance state. Placing the GPIO into a high impedance state results in the MODE pin essentially floating, and is not recommended. Do not drive the MODE pin voltage below the voltage at the V– pin; see the Absolute Maximum Ratings for the allowable voltage to drive the MODE pin. Use the MODE pin to force the OPAx625 in either the high-drive mode or the low-power mode. The OPAx625 has 120-MHz gain bandwidth, 2.5-nV/√Hz input-referred noise, and consumes just 2 mA of quiescent current in high-drive mode. In addition, the OPAx625 also has an offset voltage of 100 µV (max) and offset voltage drift of 1 µV/°C (typ). This combination of high precision, high speed, and low noise makes this device suitable for use as an input driver for high-precision, high-throughput SAR ADCs such as ADS88xx family of SAR ADC, as shown in Figure 73.

In high-drive mode, the OPAx625 is fully specified as a wideband, low-noise, low-distortion precision amplifier. High-drive mode is the primary mode of operation of the OPAx625 when driving the inputs of a SAR ADC during the signal acquisition period just before the start of the conversion period. Placing the OPAx625 into the high-drive mode before the acquisition period is complete, and before the start of the conversion period, allows the OPAx625 to settle to the final value just prior to the conversion. When the ADC is converting the input signal, and therefore no longer acquiring the signal, place the OPAx625 into the low-power mode to reduce system power. Using low-power mode allows the OPAx625 power consumption to scale directly with the sample rate.

The OPAx625 is unique in that the switching between the modes occurs in 170 ns (typ). This fast switching is achieved by the architecture of the OPAx625 during low-power mode; see the *Low-Power Mode* section for more information.

Device Functional Modes (continued)

8.4.2 Low-Power Mode

Place the OPAx625 low-power mode by applying a logic level high to the MODE pin. The MODE pin can be driven by a GPIO from the system controller, from discrete logic gates, or can be connected to directly to the V+ pin. Do not leave the MODE pin floating. When driving the MODE pin from a microcontroller GPIO, make sure that the GPIO is not placed into a high-impedance state. Placing the GPIO into a high-impedance state results in the MODE pin essentially floating, and is not recommended. Do not allow the MODE pin voltage to exceed the voltage at the V+ pin; see the Absolute Maximum Ratings for the allowable voltage to drive the MODE pin.

In low-power mode, the OPAx625 is fully specified as a general-purpose operational amplifier. The MODE signal can be controlled so that the OPAx625 is placed in high-drive mode just before the ADC enters the acquisition phase. This configuration makes sure that the voltage on the antialiasing filter capacitor settles to the required precision before the acquisition period is complete. The power consumed by the OPAx625 scales with the throughput of the system when operated in this manner. This feature is extremely useful in power-critical applications and variable-throughput data acquisition systems.

The OPAx625 is unique in that the switching between the modes occurs in 170 ns (typ). This fast switching is achieved by the architecture of the OPAx625 during low-power mode. Most amplifiers in power-down or shut-down mode consume very minimal power, but are also not operating in a linear fashion. For example, the output of a typical amplifier, when disabled, can be placed into a high-impedance state, and thus unable to drive any load whatsoever. Switching from a shut-down state to a linear state requires charging internal capacitances and bias points to a level within the linear operating range. Typically, this switch can take several microseconds or longer. This problem is solved with the OPAx625. The OPAx625 operates as a linear operational amplifier in low-power mode, and the output tracks the input signal, but with a lower bandwidth and slightly higher offset and noise. Switching from low-power mode to high-drive mode and settling to 16-bit levels occurs in 170 ns (typ) as a result of maintaining operation in a linear fashion throughout the duration of each mode. This configuration allows for dynamic power scaling, while still maintaining high throughput rates.

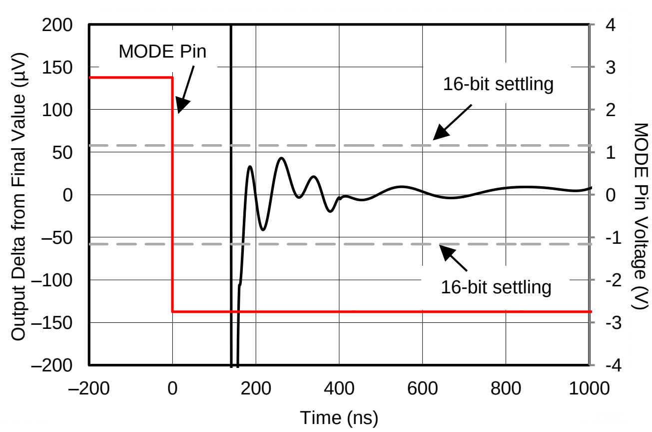


Figure 72. Output Voltage when Mode Pin Changes High to Low

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The OPAx625 is a precision, high-speed, voltage-feedback operational amplifier. Fast settling to 16-bit levels, low THD, and low noise make the OPAx625 suitable for driving SAR ADC inputs and buffering precision voltage references. With a wide power-supply voltage range from 2.7 V to 5.5 V, and operating from –40°C to +125°C, the OPAx625 is suitable for a variety of high-speed, industrial applications. The following sections show application information for the OPAx625. For simplicity, power-supply decoupling capacitors are not shown in these diagrams.

9.2 Typical Applications

9.2.1 Single-Supply, 16-Bit, 1-MSPS SAR ADC Driver

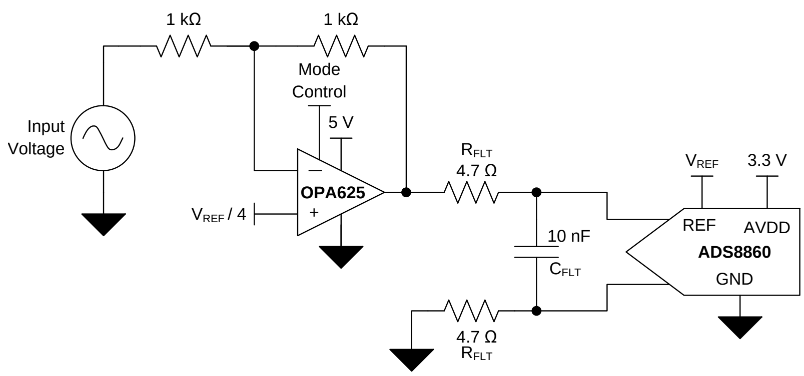


Figure 73. Single-Supply, 16-Bit, 1-MSPS SAR ADC Driver

9.2.1.1 Design Requirements

SAR ADCs, such as the ADS8860, use sampling capacitors on the data converter input. During the signal acquisition phase, these sampling capacitors are connected to the ADC analog input terminals, AINP and AINN, through a set of switches. After the acquisition period has elapsed, the internal sampling capacitors are disconnected from the input terminals and connected to the input of the ADC through a second set of switches, during this period the ADC is performing the analog-to-digital conversion. Figure 74 illustrates this architecture.

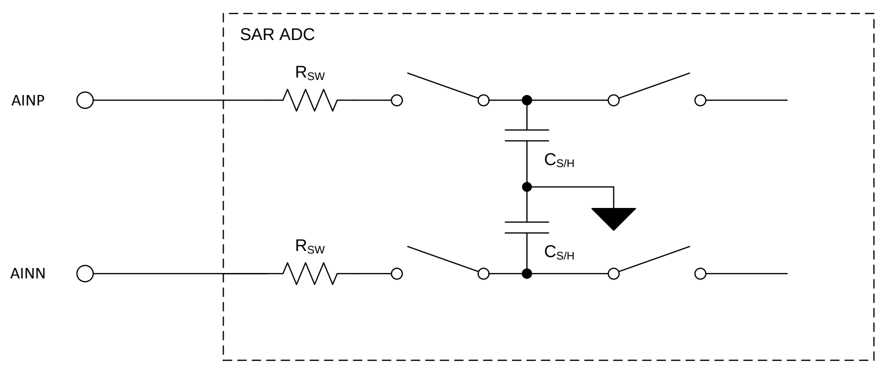


Figure 74. Simplified SAR ADC Input

Typical Applications (continued)

The SAR ADC inputs and sampling capacitors must be driven by the OPA625 to 16-bit levels within the acquisition time of the ADC. For the example illustrated in Figure 73, the OPA625 is used to drive the ADS8860 at a sample rate of 1 MSPS.

9.2.1.2 Detailed Design Procedure

The circuit illustrated in Figure 73 consists of the SAR ADC driver, a low-pass filter and the SAR ADC. The SAR ADC driver circuit consists of an OPA625 configured in an inverting gain of 1. The filter consists of R_{FLT} and C_{FLT}, connected between the output of the OPA625 and input of the ADS8860. Selecting the proper values for each of these passive components is critical to obtain the best performance from the ADC. Capacitor C_{FLT} serves as a charge reservoir, providing the necessary charge to the ADC sampling capacitors. The dynamic load presented by the ADC creates a glitch on the filter capacitor, C_{FLT}. To minimize the magnitude of this glitch, choose a value for C_{FLT} large enough to maintain a glitch amplitude of less than 100 mV. Maintaining such a low glitch amplitude at the amplifier output makes sure that the amplifier remains in the linear operating region, and results in a minimum settling time. Using Equation 6, a 10-nF capacitor is selected for C_{FLT}.

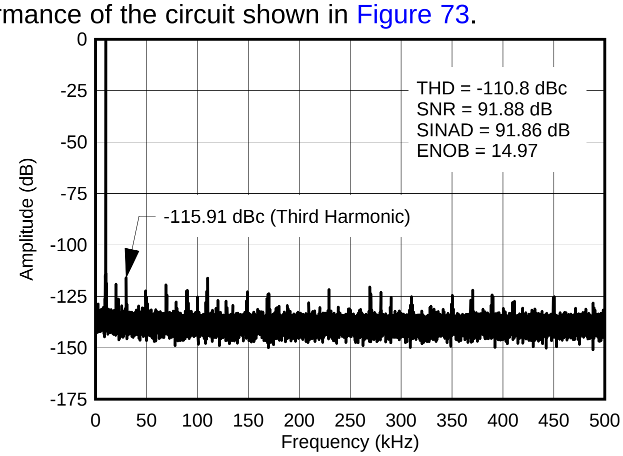
$$C_{FLT} \geq 15 \times C_{SH} \quad (6)$$

Connecting a 10-nF capacitor directly to the output of the OPA625 degrades the OPA625 phase margin and results in stability and settling-time problems. To properly drive the 10-nF capacitor, use a series resistor (R_{FLT}) to isolate the capacitor, C_{FLT}, from the OPA625. R_{FLT} must be sized based upon several constraints. To determination a suitable value for R_{FLT}, consider the impact upon the THD due to the voltage divider effect from R_{FLT} reacting with the switch resistance (R_{SW}) of the ADC input circuit, as well as the impact of the output impedance upon amplifier stability. In this example, 4.7-Ω resistors are selected. In this design example, Figure 16 can be used to estimate a suitable value for R_{ISO}. R_{ISO} represents the total resistance in series with C_{FLT}, and in this example is equivalent to 2 × R_{FLT}.

TI Precision Designs	For step-by-step design procedure, circuit schematics, bill of materials, printed circuit board (PCB) files, simulation results, and test results, refer to TI Precision Design, TIDU014, "Power-optimized 16-bit 1MSPS Data Acquisition Block for Lowest Distortion and Noise Reference Design".

9.2.1.3 Application Curves

Figure 75 illustrates the performance of the circuit shown in Figure 73.



4096-point FFT at 1 MSPS, f_{IN} = 10 kHz , V_{IN} = 1.5 V_{RMS}

Figure 75. ADC Output FFT for Figure 73

9.2.2 Single-Supply, 16-Bit, 1-MSPS, Multiplexed, SAR ADC Driver

In order to operate a high-resolution, 16-bit ADC at its maximum throughput, the full-scale voltage step must settle to better than 16-bit accuracy at the ADC inputs within the minimum specified acquisition time (t_{ACQ}). This settling imposes very stringent requirements on the driver amplifier in terms of large-signal bandwidth, slew rate, and settling time. Figure 76 illustrates a typical multiplexed ADC driver application using the OPA625.

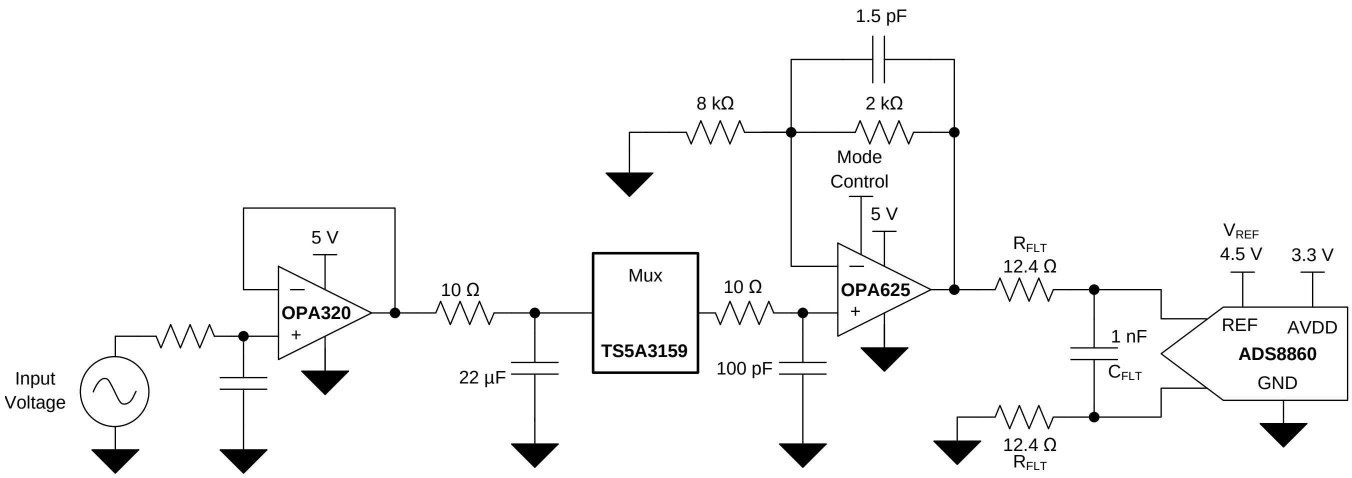


Figure 76. Single-Supply, 16-Bit, 1-MSPS, Multiplexed, SAR ADC Driver

9.2.2.1 Design Requirements

To optimize this circuit for performance, this design does not allow any large signal input transients at the inputs of the driver circuit for a small quiet-time period (t_{QT}) towards the end of the previous conversion. The input step voltage can appear anytime from the beginning of conversion (CONVST rising edge) until the elapse of a half cycle time (0.5 × t_{CYC}). This timing constraint on the input step allows a minimum settling time of (t_{QT} + t_{ACQ}) for the ADC input to settle within the required accuracy, in the worst-case scenario. This provides more time for the amplifier's output to slew and settle within the required accuracy before the next conversion starts. Figure 77 illustrates this timing sequence.

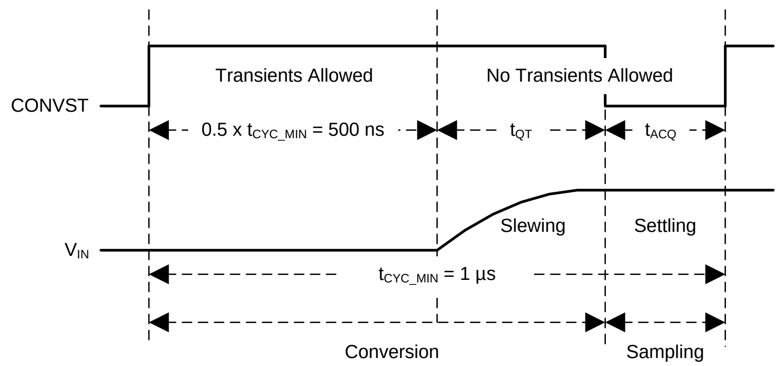


Figure 77. Timing Diagram for Input Signals

9.2.2.2 Detailed Design Procedure

An ADC input driver circuit mainly consists of two parts: a driving amplifier and a fly-wheel RC filter. The amplifier is used for signal conditioning of the input voltage and its low output impedance provides a buffer between the signal source and the ADC input. The RC filter helps attenuate the sampling charge-injection from the switched-capacitor input stage of the ADC as well as acts as an anti-aliasing filter to band-limit the wideband noise contributed by the front-end circuit. The design of the ADC input driver involves optimizing the bandwidth of the circuit, driven primarily by the following requirements:

- The $R_{FLT}C_{FLT}$ filter bandwidth should be low to band-limit the noise fed into the input of the ADC thereby increasing the signal-to-noise ratio (SNR) of the system.
- The overall system bandwidth should be large enough to accommodate optimal settling of the input signal at the ADC input before the start of conversion.

C_{FLT} is chosen based upon Equation 7 . C_{FLT} is chosen to be 1 nF.

$$C_{FLT} \geq 15 \times C_{SH} \quad (7)$$

Connecting a 1-nF capacitor directly to the output of the OPA625 would degrade the OPA625 phase margin and result in stability and settling time problems. To properly drive the 1-nF capacitor, a series resistor, R_{FLT}, is used to isolate the capacitor, C_{FLT}, from the OPA625. R_{FLT} must be sized based upon several constraints. To determination a suitable value for R_{FLT}, the system designer must consider the impact upon the THD due to the voltage divider effect from R_{FLT} reacting with the switch resistance, R_{SW}, of the ADC input circuit as well as the impact of the output impedance upon amplifier stability. In this example 12.4-Ω resistors are selected. In this design example, Figure 15 can be used to estimate a suitable value for R_{ISO}. R_{ISO} represents the total resistance in series with C_{FLT}, which in this example is equivalent to 2 × R_{FLT}.

TI Precision Designs

For step-by-step design procedure, circuit schematics, bill of materials, printed circuit board (PCB) files, simulation results, and test results, refer to TI Precision Design, TIDU012, "Power-optimized 16-bit 1MSPS Data Acquisition Block for Lowest Distortion and Noise Reference Design".

9.2.2.3 Application Curves

Figure 78 illustrates the performance of the circuit shown in Figure 76.

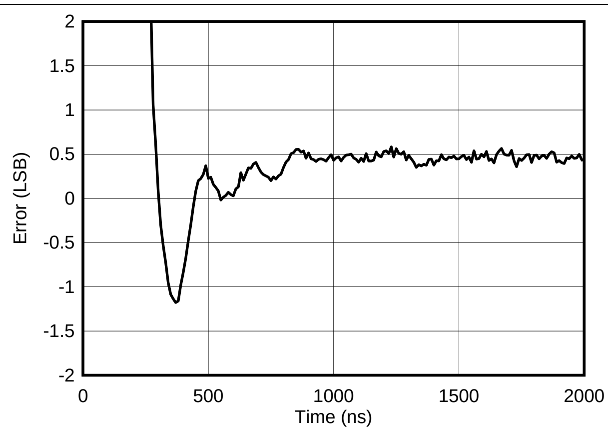


Figure 78. Positive Transient Response for Figure 76

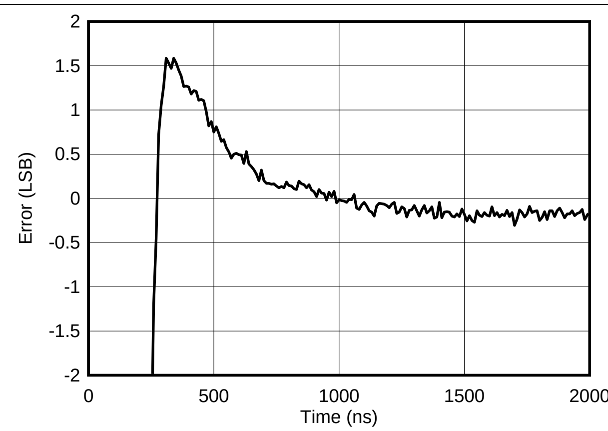


Figure 79. Negative Transient Response for Figure 76

10 Power Supply Recommendations

The OPAx625 is specified for operation from 2.7 V to 5.5 V (±1.35 V to ±2.75 V); many specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the Typical Characteristics. Place bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see the *Layout* section.

CAUTION

Supply voltages larger than 6 V can cause permanent damage to the device. See to the *Absolute Maximum Ratings* section.

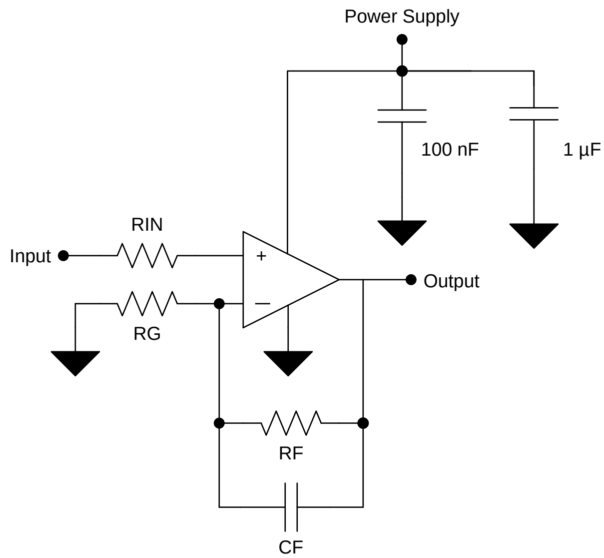
11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Use bypass capacitors to reduce the noise coupled from the power supply. Connect low ESR, ceramic, bypass capacitors between the power supply pins (V+ and V–) and the ground plane. Place the bypass capacitors as close to the device as possible with the 100-nF capacitor closest to the device, as indicated in Figure 80. For single-supply applications, bypass capacitors on the V– pin are not required.
- Separate grounding for analog and digital portions of the circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current. For more detailed information refer to SLOA089, *Circuit Board Layout Techniques*.
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Minimize parasitic coupling between +IN and OUT for best ac performance.
- Place the external components as close to the device as possible. As shown in Figure 80, keeping RF, CF, and RG close to the inverting input will minimize parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, bake the PCB assembly to remove moisture introduced into the device packaging during the cleaning process. A low-temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

11.2 Layout Example



(Schematic Representation)

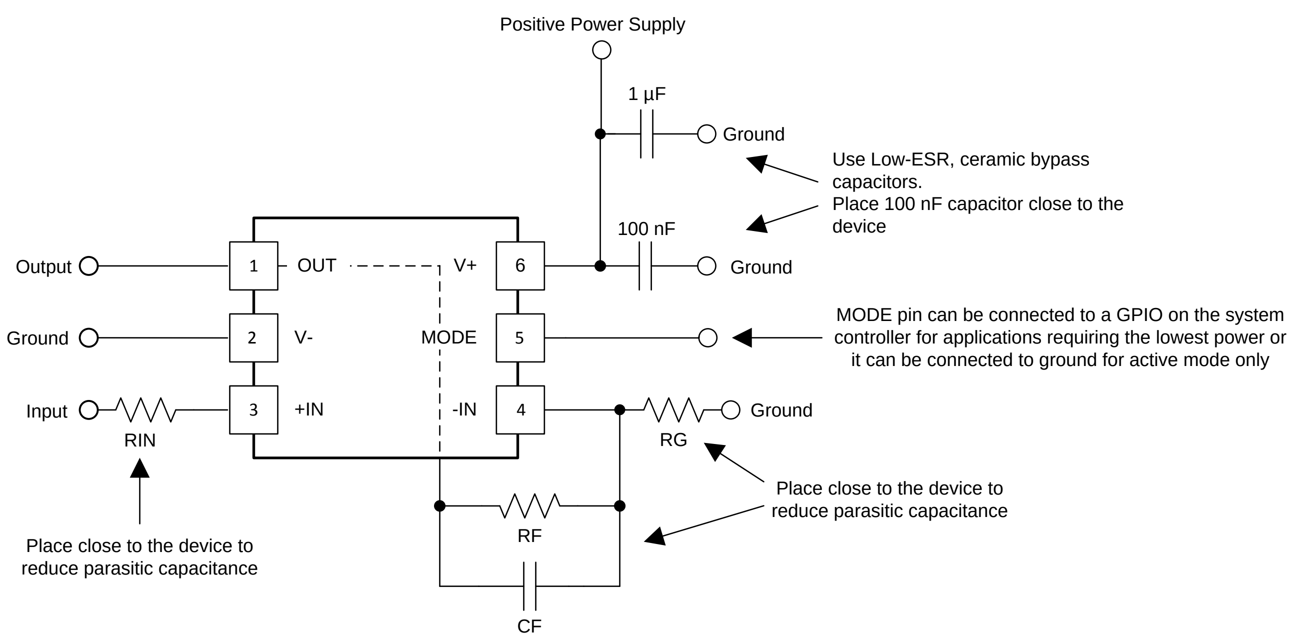


Figure 80. PCB Layout Example

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

12.1.1.1 TINA-TI™ (Free Software Download)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

12.1.1.2 TI Precision Designs

TI Precision Designs are available online at http://www.ti.com/ww/en/analog/precision-designs/. TI Precision Designs are analog solutions created by TI's precision analog applications experts and offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits.

12.2 Documentation Support

12.2.1 Related Documentation

16-Bit, 1MSPS Multiplexed Data Acquisition Reference Design Guide, TIDUAD9

12.3 Related Links

Table 1 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
OPA625	Click here	Click here	Click here	Click here	Click here
OPA2625	Click here	Click here	Click here	Click here	Click here

12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided *AS IS* by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 Trademarks

E2E is a trademark of Texas Instruments.
TINA-TI is a trademark of Texas Instruments, Inc and DesignSoft, Inc.
TINA is a trademark of DesignSoft, Inc.
All other trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA2625IDGSR	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2625
OPA2625IDGSR.B	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2625
OPA2625IDGST	Active	Production	VSSOP (DGS) | 10	250 | SMALL T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2625
OPA2625IDGST.B	Active	Production	VSSOP (DGS) | 10	250 | SMALL T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2625
OPA625IDBVR	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O625
OPA625IDBVR.B	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O625
OPA625IDBVRG4	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O625
OPA625IDBVRG4.B	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O625
OPA625IDBVT	Active	Production	SOT-23 (DBV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O625
OPA625IDBVT.B	Active	Production	SOT-23 (DBV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O625

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

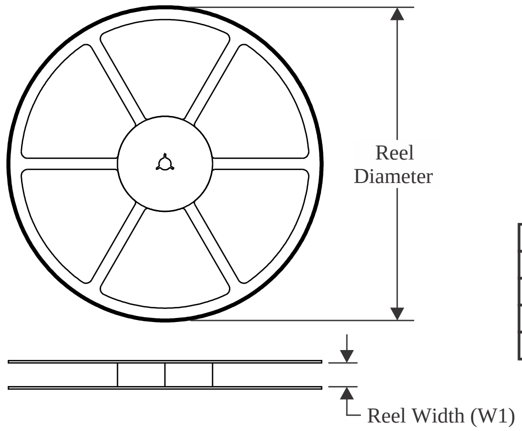
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

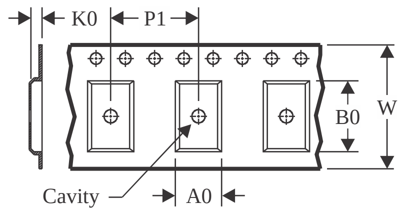
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

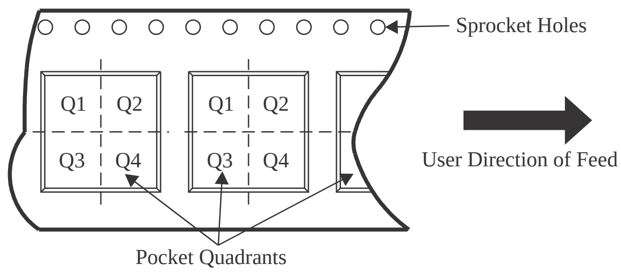


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

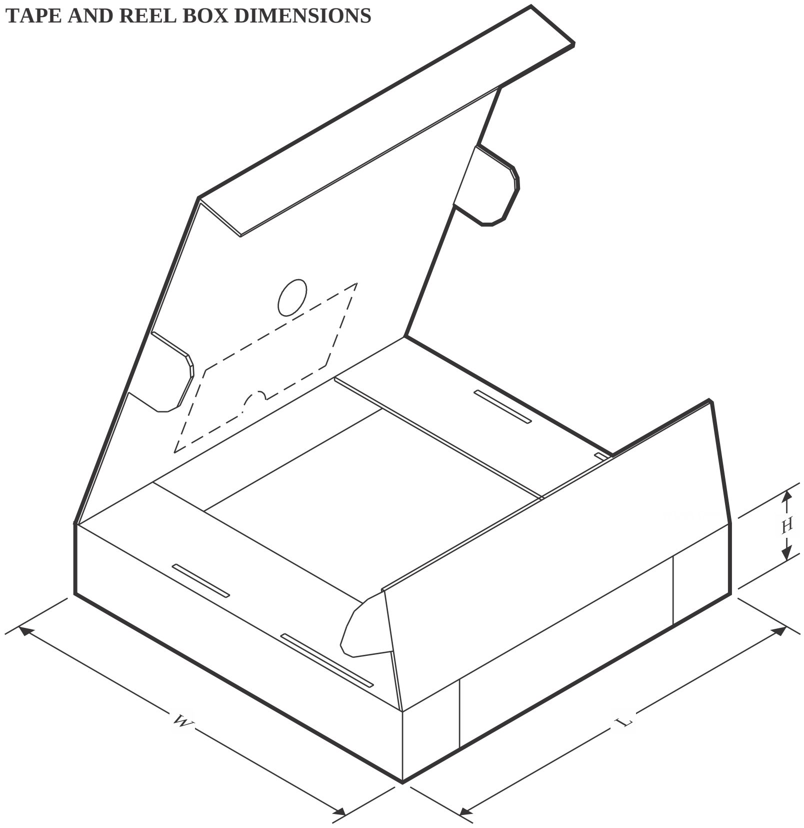
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

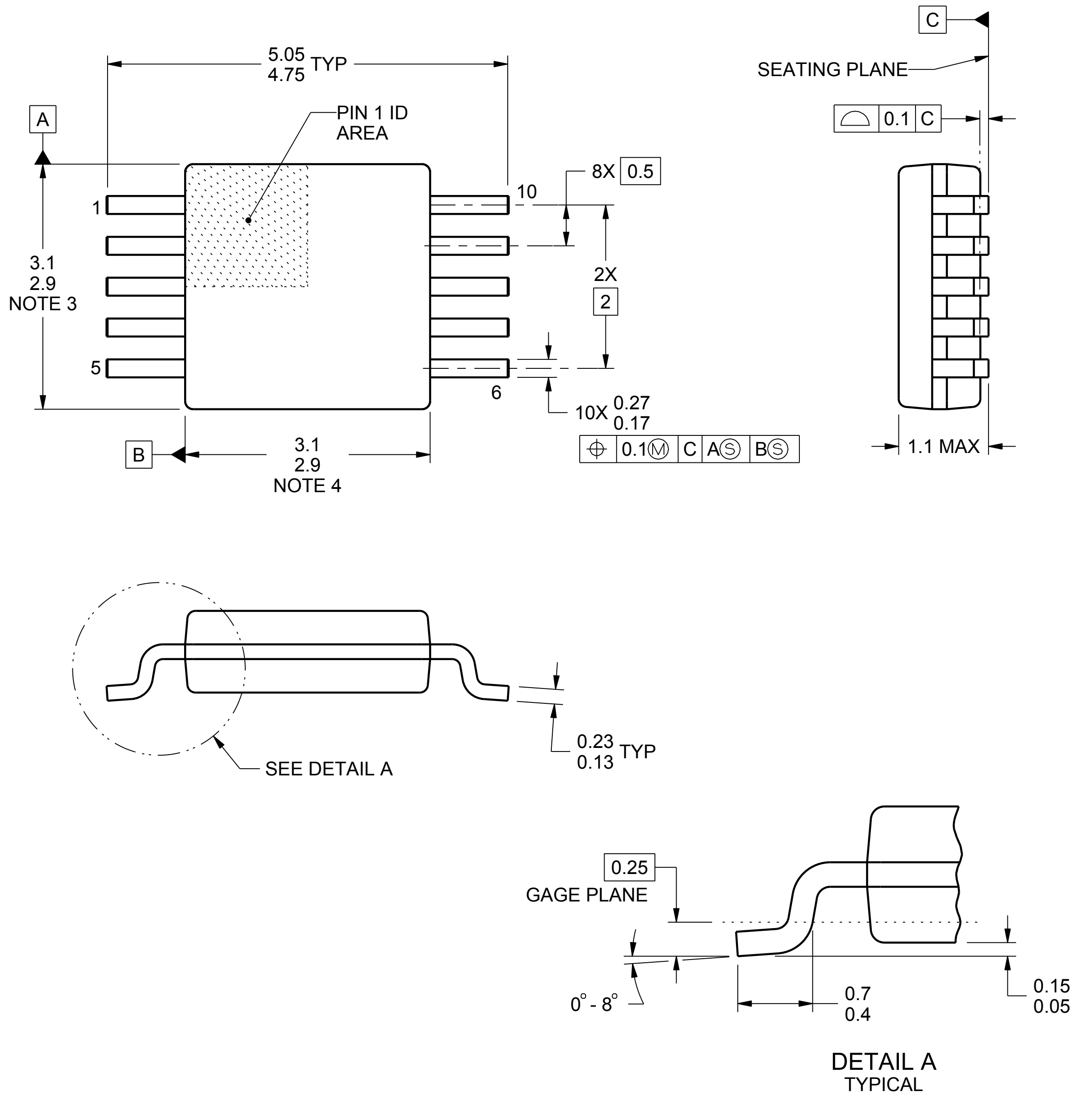
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2625IDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2625IDGST	VSSOP	DGS	10	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA625IDBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
OPA625IDBVRG4	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
OPA625IDBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

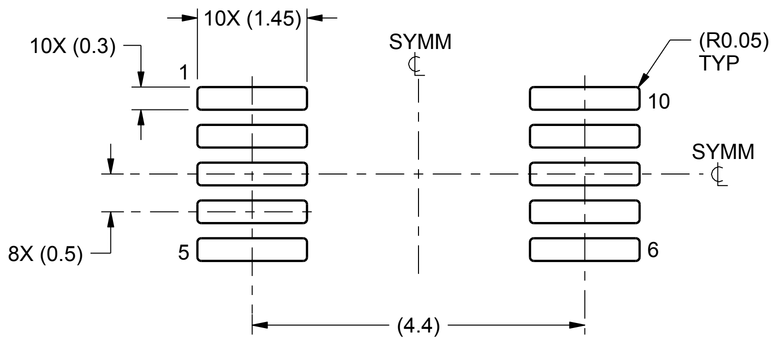
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2625IDGSR	VSSOP	DGS	10	2500	366.0	364.0	50.0
OPA2625IDGST	VSSOP	DGS	10	250	366.0	364.0	50.0
OPA625IDBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
OPA625IDBVRG4	SOT-23	DBV	6	3000	180.0	180.0	18.0
OPA625IDBVT	SOT-23	DBV	6	250	180.0	180.0	18.0



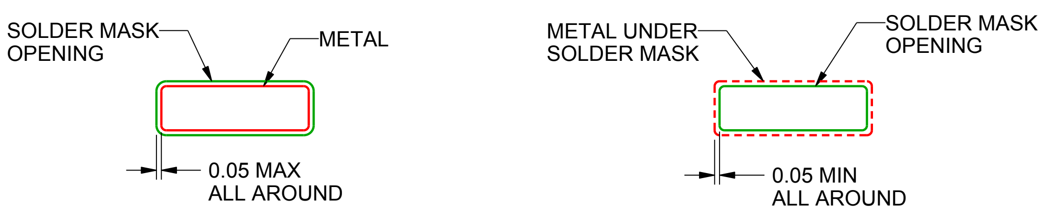
4221984/A 05/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X



NON SOLDER MASK
DEFINED

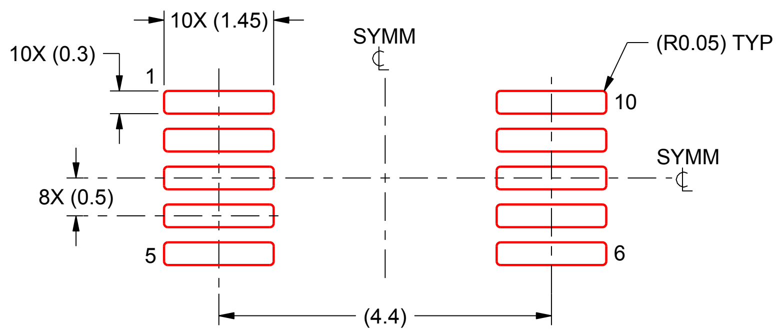
SOLDER MASK
DEFINED

SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

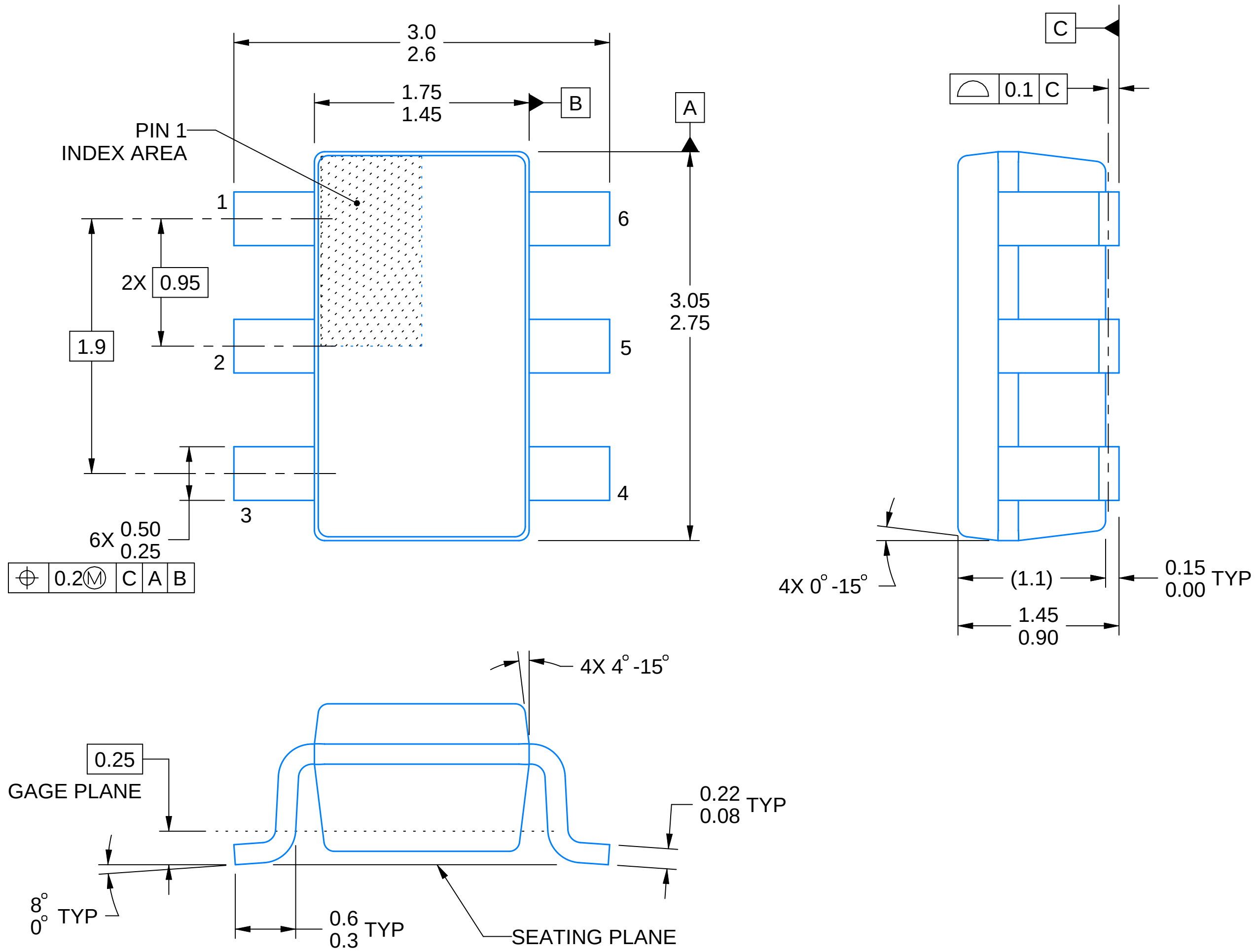
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

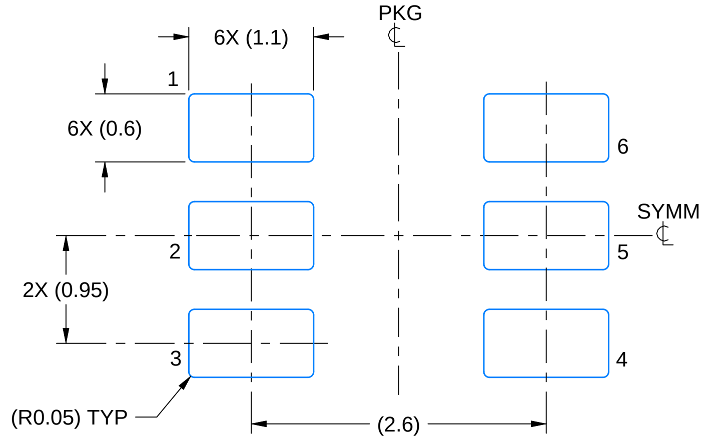
SMALL OUTLINE TRANSISTOR



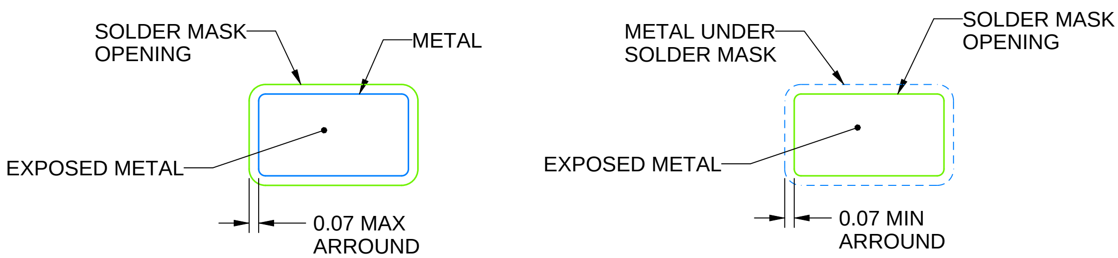
4214840/G 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



NON SOLDER MASK
DEFINED
(PREFERRED)

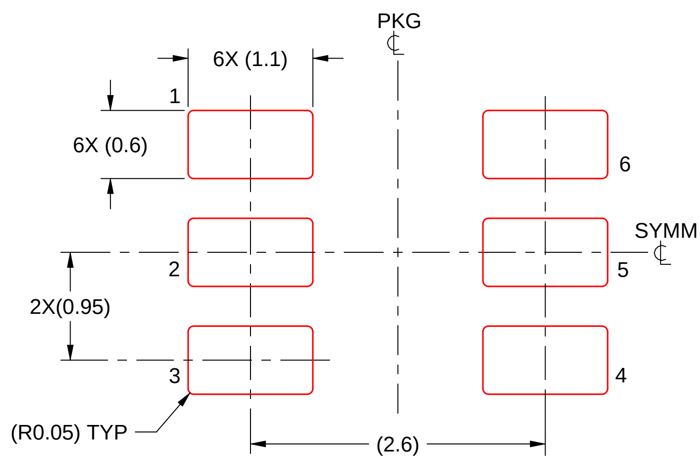
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214840/G 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/G 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.