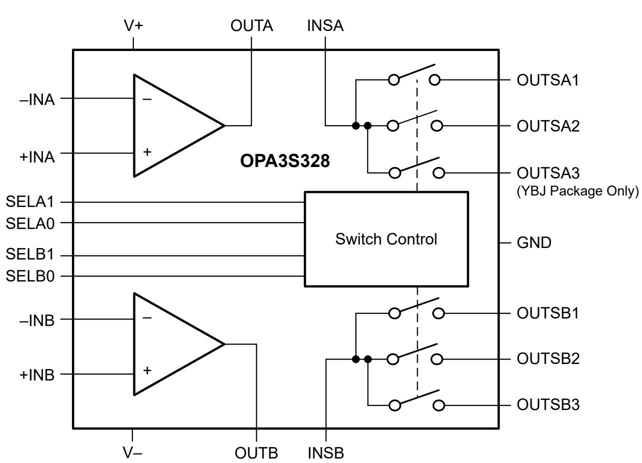
OPA3S328 40-MHz, Dual, Precision, Low-Noise, Low-Input-Bias-Current CMOS Operational Amplifier With Integrated Switches

1 Features

- Precision operational amplifier with integrated switches for transimpedance applications
- Wide bandwidth: 40 MHz
- Low offset voltage: 60 µV (max)
- Very low offset drift: 1 µV/°C (max)
- Low input bias current: 0.2 pA
- Rail-to-rail input and output
- Zero-crossover input stage
- Low voltage noise: 6.1 nV/√Hz at 10 kHz
- Low current noise: 0.125 pA/√Hz at 10 kHz
- Low leakage switches: 10 pA
- Slew rate: 30 V/µs
- Quiescent current: 3.8 mA per channel
- Current in shutdown mode: 30 µA
- Output impedance in shutdown mode: 100 GΩ
- Single-supply voltage range: 2.2 V to 5.5 V
- Unity-gain stable
- Small packages:
  – 20-lead, 3.5-mm x 3.5-mm VQFN
  – 2.0-mm x 2.0-mm DSBGA

2 Applications

- Optical transport inter-dc interconnect
- Optical module
- Optical network terminal unit (ONT)
- Small cell base station
- Digital multimeter (DMM)
- Data acquisition (DAQ)



Functional Block Diagram

3 Description

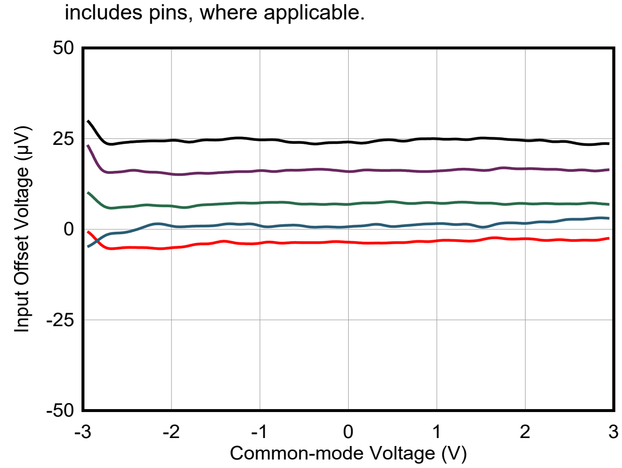
The OPA3S328 is a precision, low-voltage, CMOS operational amplifier (op amp) with integrated switches that are optimized for flexible transimpedance applications. Low input bias current and low input capacitance allows for high-frequency transimpedance gains at low photocurrent operation (< 1 nA). The integrated switches, low offset, and rail-to-rail output performance of the OPA3S328 enable high accuracy across multiple decades of current values. Small packages, along with integrated switches, allow for selectable transimpedance gains and help reduce size for space-constrained applications.

The OPA3S328 features zero-crossover input technology, giving the flexibility for the input common-mode range to span the full supply range without offset deviations. The device provides enable-disable capability to allow for portable, handheld applications in test and measurement. When disabled, the OPA3S328 output impedance is typically 100 GΩ, allowing for wired-OR applications using multiple transimpedance channels.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
OPA3S328	RGR (VQFN, 20)	3.5 mm × 3.5 mm
	YBJ (DSBGA, 24)	2 mm × 2 mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Input Offset Voltage vs Input Common-Mode Voltage

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4 Pin Configuration and Functions

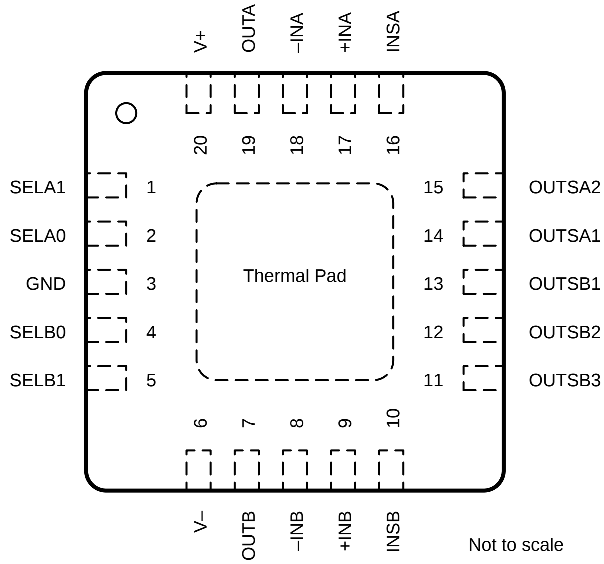


Figure 4-1. RGR Package, 20-Pin VQFN (Top View)

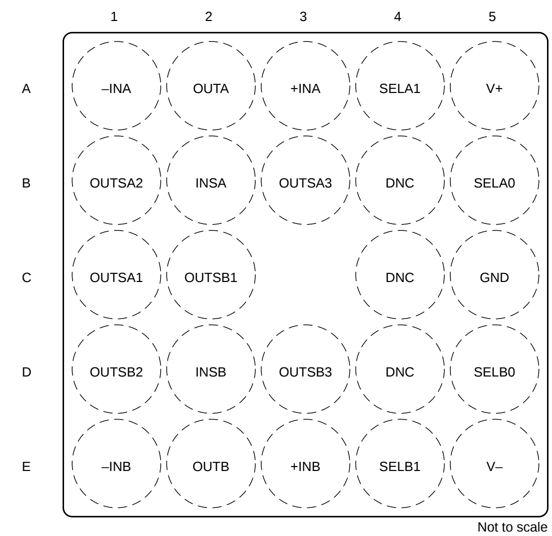


Figure 4-2. YBJ Package, 24-Pin DSBGA (Top View)

Table 4-1. Pin Functions

PIN			TYPE	DESCRIPTION
NAME	NO.			
	RGR (VQFN)	YBJ (DSBGA)		
DNC	—	B4, C4, D4	—	Do not connect
GND	3	C5	Ground	Digital ground pin
–INA	18	A1	Input	Negative (inverting) input for amplifier A
–INB	8	E1	Input	Negative (inverting) input for amplifier B
+INA	17	A3	Input	Positive (noninverting) input for amplifier A
+INB	9	E3	Input	Positive (noninverting) input for amplifier B
INSA	16	B2	Input/Output	Switch A1, A2, A3 input
INSB	10	D2	Input/Output	Switch B1, B2, B3 input
OUTA	19	A2	Output	Output of amplifier A
OUTB	7	E2	Output	Output of amplifier B
OUTSA1	14	C1	Input/Output	Switch A1 output
OUTSA2	15	B1	Input/Output	Switch A2 output
OUTSA3	—	B3	Input/Output	Switch A3 output
OUTSB1	13	C2	Input/Output	Switch B1 output
OUTSB2	12	D1	Input/Output	Switch B2 output
OUTSB3	11	D3	Input/Output	Switch B3 output
SELA0	2	B5	Input	Input select for switch matrix A
SELA1	1	A4	Input	Input select for switch matrix A
SELB0	4	D5	Input	Input select for switch matrix B
SELB1	5	E4	Input	Input select for switch matrix B
V–	6	E5	Power	Negative (lowest) power supply
V+	20	A5	Power	Positive (highest) power supply
Thermal Pad	Thermal Pad	—	—	Exposed thermal pad. Connect to V–

Table 4-2. Select Pin Decoder

SELA1	SELA0	SELB1	SELB0	SHUTDOWN STATUS	SWITCH CONFIGURATION					
					SWITCH A1 STATUS	SWITCH A2 STATUS	SWITCH A3[(1)] STATUS	SWITCH B1 STATUS	SWITCH B2 STATUS	SWITCH B3 STATUS
LOW	LOW	—	—	Amplifier A enabled	CLOSED	OPEN	OPEN	—	—	—
LOW	HIGH	—	—	Amplifier A enabled	OPEN	CLOSED	OPEN	—	—	—
HIGH	LOW	—	—	Amplifier A enabled	OPEN	OPEN	CLOSED	—	—	—
HIGH	HIGH	—	—	In special mode, the SELB0 and SELB1 decoding scheme shown here is ignored, and instead, Table 4-3 applies.				—	—	—
—	—	LOW	LOW	Amplifier B enabled	—	—	—	CLOSED	OPEN	OPEN
—	—	LOW	HIGH	Amplifier B enabled	—	—	—	OPEN	CLOSED	OPEN
—	—	HIGH	LOW	Amplifier B enabled	—	—	—	OPEN	OPEN	CLOSED
—	—	HIGH	HIGH	Amplifier B enabled	—	—	—	OPEN	OPEN	OPEN

(1) Switch A3 is available in the YBJ (DSBGA-24) package option only.

Table 4-3. Select Pin Decoder in Special Mode: SELA0 = SELA1 = HIGH

SELA1	SELA0	SELB1	SELB0	SHUTDOWN STATUS	SWITCH CONFIGURATION					
					SWITCH A1 STATUS	SWITCH A2 STATUS	SWITCH A3[(1)] STATUS	SWITCH B1 STATUS	SWITCH B2 STATUS	SWITCH B3 STATUS
HIGH	HIGH	LOW	LOW	Amplifier A in power down and amplifier B enabled	OPEN	OPEN	OPEN	OPEN	OPEN	OPEN
HIGH	HIGH	LOW	HIGH	Amplifier A enabled and amplifier B in power down	OPEN	OPEN	OPEN	OPEN	OPEN	OPEN
HIGH	HIGH	HIGH	LOW	Both Amplifier A and amplifier B enabled	OPEN	OPEN	OPEN	OPEN	OPEN	OPEN
HIGH	HIGH	HIGH	HIGH	Both Amplifier A and amplifier B in power down	OPEN	OPEN	OPEN	OPEN	OPEN	OPEN

(1) Switch A3 is available in the YBJ (DSBGA-24) package option only.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) [(1)]

		MIN	MAX	UNIT
V_S	Supply voltage, V_S = (V+) – (V–)	–0.3	6	V
	Input voltage, all pins	(V–) – 0.3	(V+) + 0.3	V
	Input current (INA+, INA–, INB+, INB–, INSA/B, OUTSA/B/1/2/3)	–10	+10	mA
	Output short-circuit[(2)]	Continuous	Continuous	
T_A	Operating temperature	–55	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Short-circuit to ground, one amplifier per package.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002[(2)]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_S	Supply voltage	Single-supply	2.2		5.5	V
		Dual-supply	±1.1		±2.75	V
V_D	Digital supply voltage, V_D = (V+) – (GND)		1.8		5.5	V
T_A	Specified temperature		–40		+125	°C

5.4 Thermal Information

THERMAL METRIC[(1)]		OPA3S328		UNIT
		RGR (VQFN)	YBJ (DSBGA)	
		20 PINS	24 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	43.7	66.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	41.7	0.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	19.5	15.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.8	0.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	19.5	15.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	5.3	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Electrical Characteristics

at T_A = 25°C, V_S = ±1.1 V to ±2.75 V (2.2 V to 5.5 V), R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, V_{OUT} = V_S / 2, and all voltages referred to V– (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage			10	±60	µV
		T_A = 0°C to 85°C			±90	
		T_A = –40°C to +125°C			±175	
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to +125°C		±0.15	±1	µV/°C
PSRR	Power supply rejection ratio	V_S = ±1.1 V to ±2.75 V		±1	±10	µV/V
		V_S = ±1.1 V to ±2.75 V, T_A = –40°C to +125°C		±15		
	Channel separation	f = dc		140		dB
		f = 100 kHz		75		
INPUT BIAS CURRENT						
I_B	Amplifier input bias current			±0.2	±10	pA
		T_A = 0°C to 85°C			±10	
		T_A = –40°C to +125°C			±100	
I_{OS}	Amplifier input offset current			±0.2	±20	pA
		T_A = 0°C to 85°C			±20	
		T_A = –40°C to +125°C			±200	
NOISE						
	Input voltage noise	f = 0.1 Hz to 10 Hz		3		$µV_{PP}$
e_N	Input voltage noise density	f = 100 Hz		25		nV/√Hz
		f = 1 kHz		9.8		
		f = 10 kHz		6.1		
i_N	Input current noise	f = 10 kHz		0.04		pA/√Hz
INPUT VOLTAGE						
V_{CM}	Common-mode voltage		(V–) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	(V–) – 0.1 V < V_{CM} < (V+) + 0.1 V	106	120		dB
		(V–) – 0.1 V < V_{CM} < (V+) + 0.1 V, T_A = –40°C to +125°C	96	110		
INPUT CAPACITANCE						
Z_{ID}	Differential			1 || 4		TΩ || pF
Z_{ICM}	Common-mode			1 || 2		TΩ || pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	(V–) + 100 mV < V_O < (V+) – 100 mV	108	132		dB
		(V–) + 100 mV < V_O < (V+) – 100 mV, T_A = –40°C to +125°C	96	130		
		(V–) + 100 mV < V_O < (V+) – 100 mV, R_L = 2 kΩ	106	123		
		(V–) + 100 mV < V_O < (V+) – 100 mV, R_L = 2 kΩ, T_A = –40°C to +125°C	90	120		

5.5 Electrical Characteristics (continued)

at T_A = 25°C, V_S = ±1.1 V to ±2.75 V (2.2 V to 5.5 V), R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, V_{OUT} = V_S / 2, and all voltages referred to V– (unless otherwise noted)

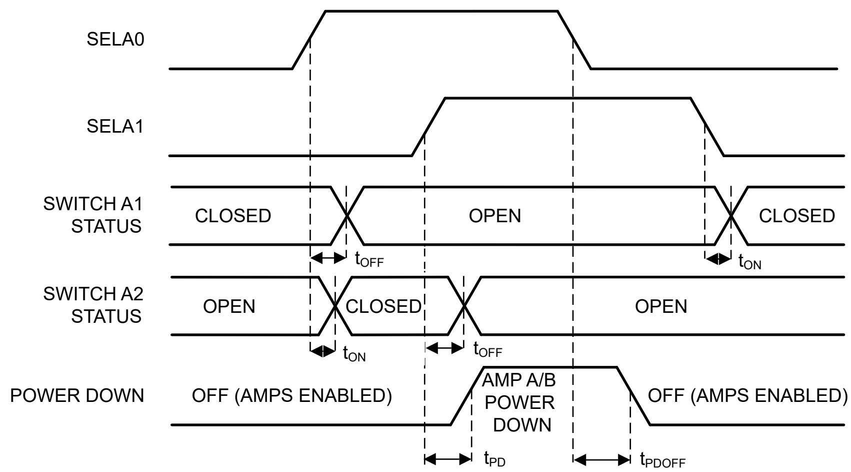
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product				40		MHz
SR	Slew rate	4-V step, G = +1			±30		V/µs
t_S	Settling time	To 0.1%, 4-V step , G = +1			0.3		µs
		To 0.01%, 4-V step , G = +1			0.42		
	Overload recovery time	V_{IN} × G > V_S			0.5		µs
THD+N	Total harmonic distortion + noise	V_O = 1 V_{RMS}, G = +1, f = 1 kHz			0.00017%		
f_{CP}	Charge pump frequency				27		MHz
OUTPUT							
	Voltage output swing from both rails	V_S = 2.2 V				5	mV
			R_L = 2 kΩ			15	
		V_S = 5.5 V				5	
			R_L = 2 kΩ			15	
I_{SC}	Short-circuit current	Sinking, V_S = 5.5 V			–68		mA
		Sourcing, V_S = 5.5 V			63		
Z_O	Open-loop output impedance	f = 10 kHz			55		Ω
OUTPUT DISABLE							
I_{QPD}	Quiescent current in power down	Total quiescent current, both amplifiers A and B disabled			30	50	µA
t_{PDOFF}	Output enable time				10		µs
t_{PD}	Output disable time				3		µs
Z_{PD}	Output impedance in power down				100 || 16		GΩ || pF
POWER SUPPLY							
I_Q	Quiescent current per amplifier	I_O = 0 mA			3.8	4.5	mA
			T_A = –40°C to +125°C			5.0	
SELECT INPUTS							
V_{IH}	High level input voltage	GND = 0 V		1.5		V+	V
V_{IL}	Low level input voltage	GND = 0 V		0		0.3	V
	GND voltage input range			(V–)		(V+) – 1.8	V
R_{PD}	Input pulldown resistance	SELA/B/0/1 pins			10		MΩ

5.5 Electrical Characteristics (continued)

at T_A = 25°C, V_S = ±1.1 V to ±2.75 V (2.2 V to 5.5 V), R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, V_{OUT} = V_S / 2, and all voltages referred to V– (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SWITCHES							
t_{ON}	Switching time off to on (open to close)	R_{L_SW} = 300 Ω, C_L = 35 pF, INSA/B = 5 V, OUTSA/B/1/2/3 = 0 V, V_S = 5 V			1.3		µs
t_{OFF}	Switching time on to off (close to open)	R_{L_SW} = 300 Ω, C_L = 35 pF, INSA/B = 5 V, OUTSA/B/1/2/3 = 0 V, V_S = 5 V			2		µs
I_{L_INS}	Switch input leakage current (INSA/B)	Switch open, INSA/B = 5 V, OUTSA/B/1/2/3 = 0 V			30		pA
		Switch open, INSA/B = 1.5 V, OUTSA/B/1/2/3 = 4.5 V			10	150	
			T_A = 0°C to 85°C		25	150	
			T_A = –40°C to +125°C		82	260	
I_{L_OUTS}	Switch output leakage current (OUTSA/B/1/2/3)	Switch open, INSA/B = 1.5 V, OUTSA/B/1/2/3 = 4.5 V			11	90	pA
			T_A = 0°C to 85°C		100	120	
			T_A = –40°C to +125°C		190	250	
I_{L_ON}	Channel on leakage	Switch closed, INSA/B = 5 V, OUTSA/B/1/2/3 = 5 V			5	20	pA
			T_A = 0°C to 85°C			140	
			T_A = –40°C to +125°C			155	
C_{IN}	Switch input capacitance	Switch open, INSA/B = 2.5 V			3		pF
C_{OUT}	Switch output capacitance	Switch open, OUTSA/B/1/2/3 = 2.5 V			0.7		pF
	Switch total capacitance	Switch closed, INSA/B = OUTSA/B/1/2/3 = 2.5 V			6		pF
R_{ON}	Switch on resistance	Switch closed, V+ = 5 V, INSA/B = 2.5 V			84	125	Ω
			T_A = 0°C to 85°C		88		
			T_A = –40°C to +125°C		102		
ΔR_{ON}	Switch on resistance match between channels	Switch closed, V+ = 5 V, INSA/B = 4 V			0.2	2	Ω
	Switch on resistance flatness (vs input signal range)	Switch closed, V+ = 5 V, INSA/B = 0 V to V+			27	40	Ω
			T_A = –40°C to +125°C			100	
	Switch charge injection	C_{L_SW} = 1 nF			6		pC
	Switch off isolation	R_{L_SW} = 50 Ω, C_{L_SW} = 5 pF, f = 1 MHz			84		dB
	Switch channel-to-channel crosstalk	R_{L_SW} = 50 Ω, C_{L_SW} = 5 pF, f = 1 MHz			76		dB
	Switch −3-dB bandwidth	R_{L_SW} = 50 Ω, C_{L_SW} = 5 pF			350		MHz

5.6 Timing Diagram



Note: SELA0 and SELA1 shown. Timing for SELB0 and SELB1 to SWITCH B1, B2 and B3 transitions matches SELA0 and SELA1.

Figure 5-1. Select Pin Timing Diagram

5.7 Typical Characteristics

at T_A = 25°C, V_S = 5.5 V, V_{CM} = V_{OUT} = mid-supply, C_L = 20 pF, and R_L = 10 kΩ (unless otherwise noted)

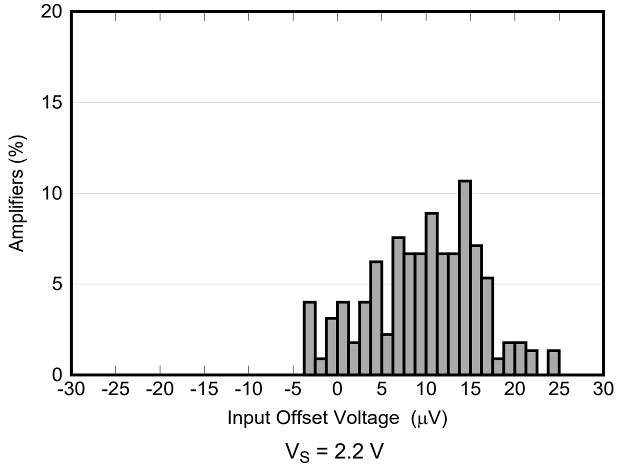


Figure 5-2. Offset Voltage Production Distribution

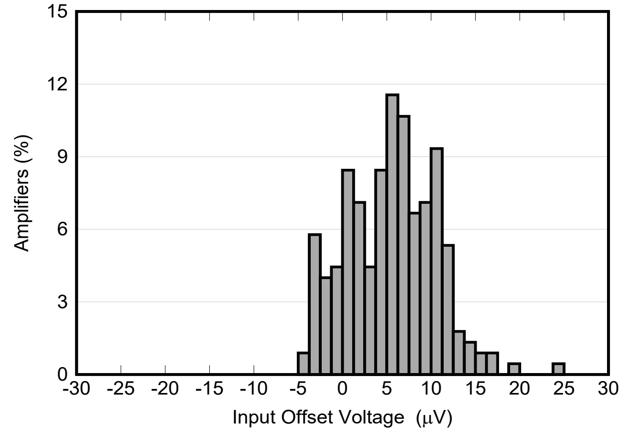


Figure 5-3. Offset Voltage Production Distribution

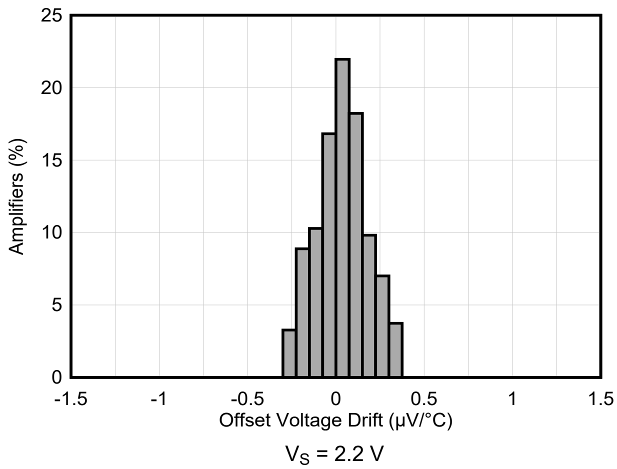


Figure 5-4. Offset Voltage Drift Distribution

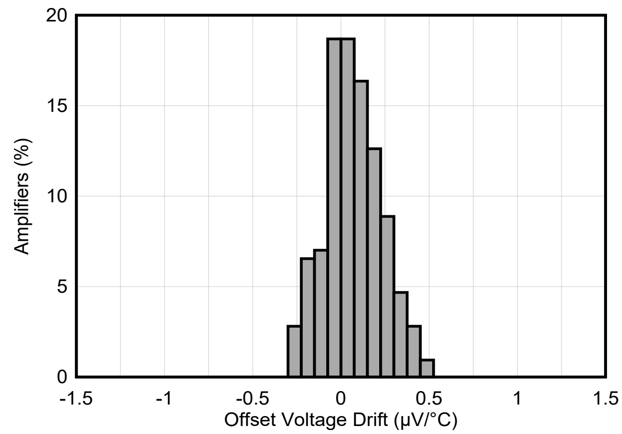


Figure 5-5. Offset Voltage Drift Distribution

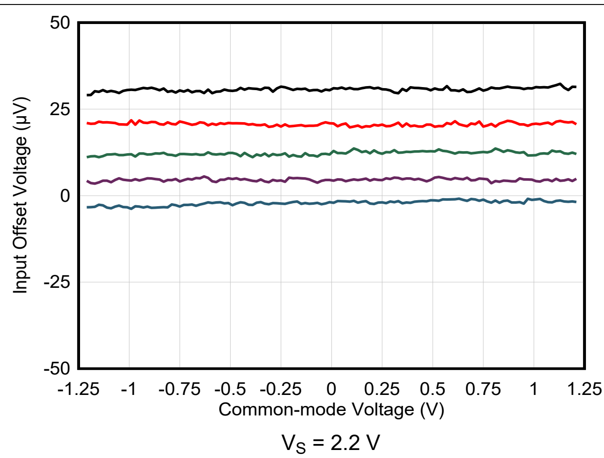


Figure 5-6. Offset Voltage vs Common-Mode Voltage

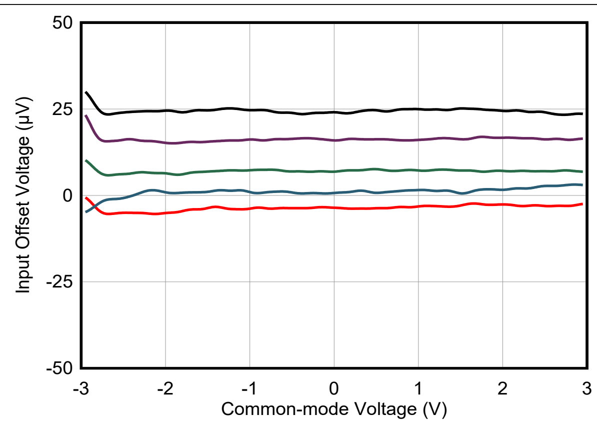


Figure 5-7. Offset Voltage vs Common-Mode Voltage

5.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5 V, V_{CM} = V_{OUT} = mid-supply, C_L = 20 pF, and R_L = 10 kΩ (unless otherwise noted)

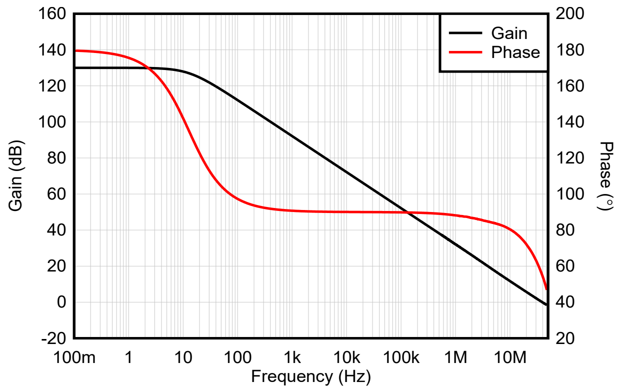


Figure 5-8. Open-Loop Gain/Phase vs Frequency

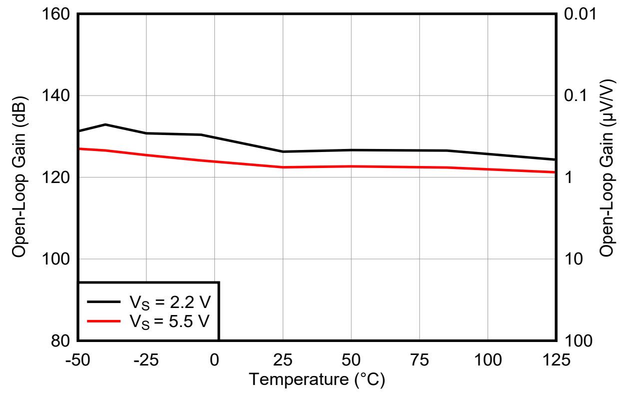


Figure 5-9. Open-Loop Gain vs Temperature

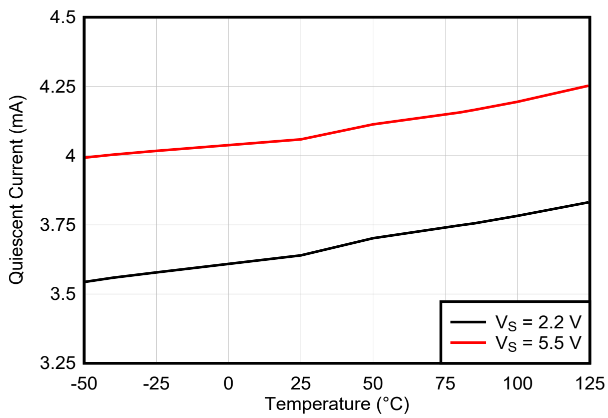


Figure 5-10. Quiescent Current vs Supply Voltage

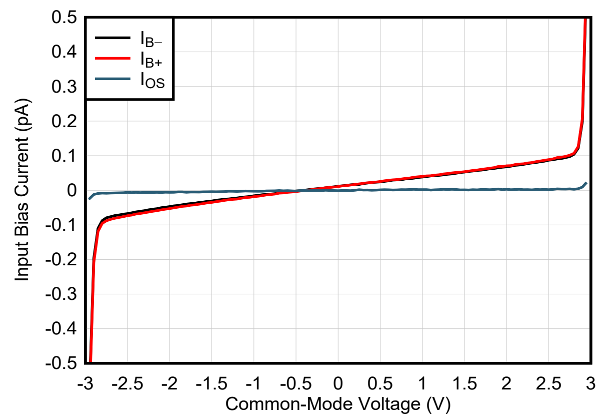


Figure 5-11. Input Bias Current vs Common-Mode Voltage

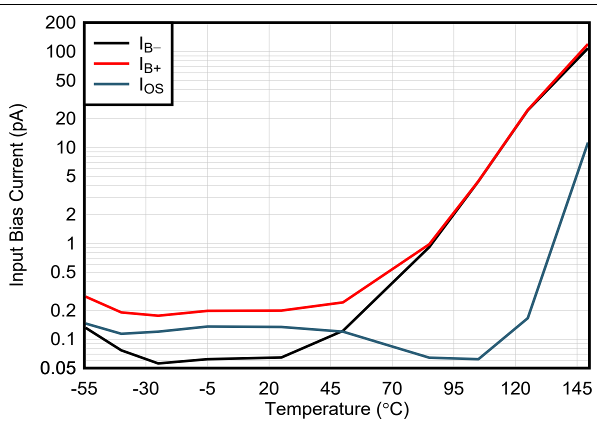


Figure 5-12. Input Bias Current vs Temperature

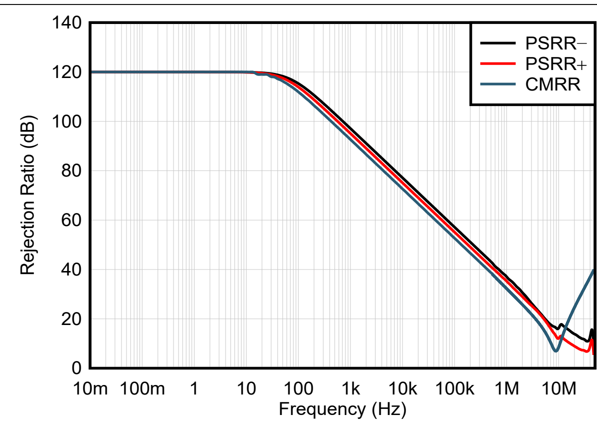


Figure 5-13. CMRR and PSRR vs Frequency

5.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5 V, V_{CM} = V_{OUT} = mid-supply, C_L = 20 pF, and R_L = 10 kΩ (unless otherwise noted)

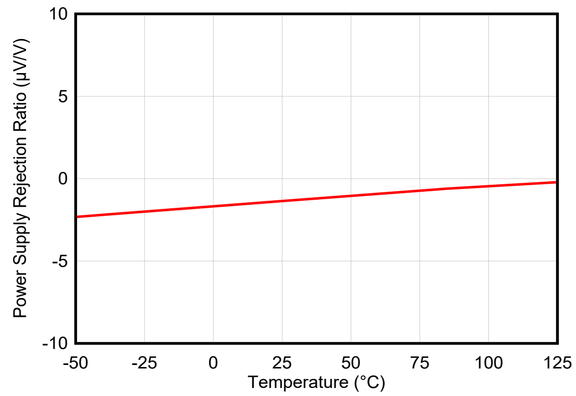


Figure 5-14. PSRR vs Temperature

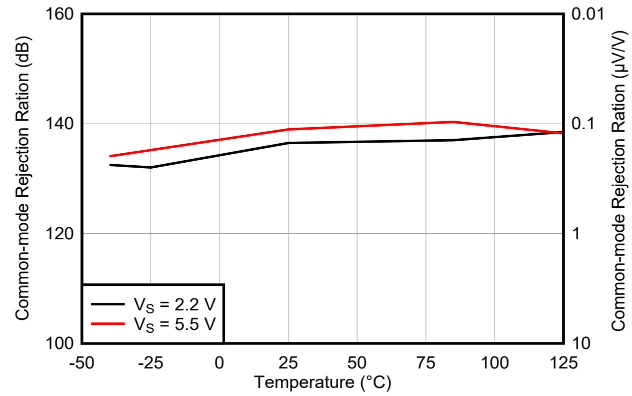


Figure 5-15. CMRR vs Temperature

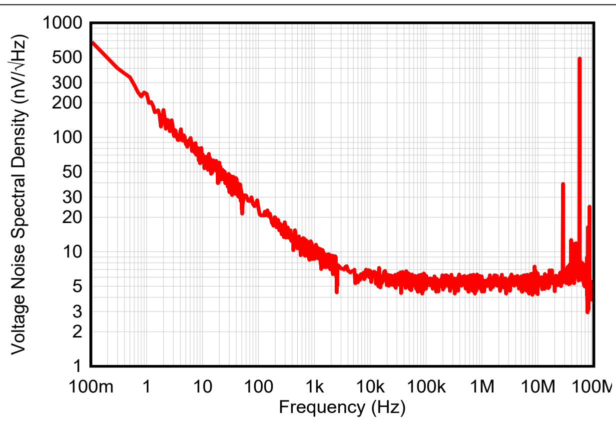


Figure 5-16. Input Voltage Noise Spectral Density vs Frequency

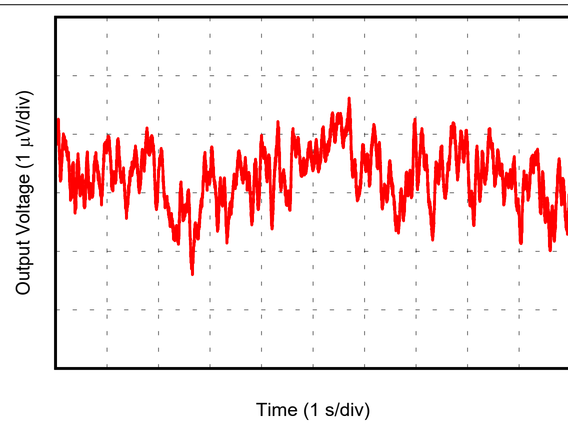


Figure 5-17. 0.1-Hz to 10-Hz Input Voltage Noise

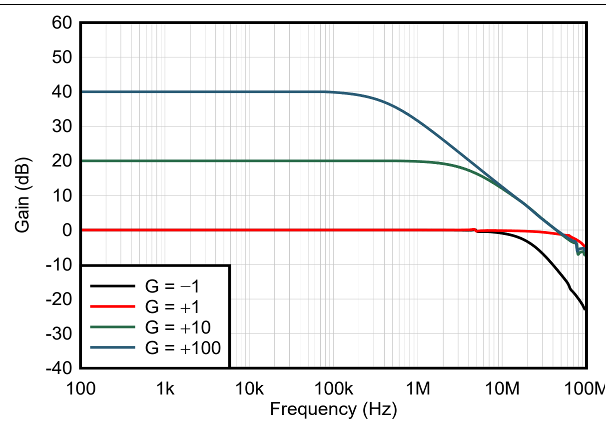


Figure 5-18. Closed-Loop Gain vs Frequency

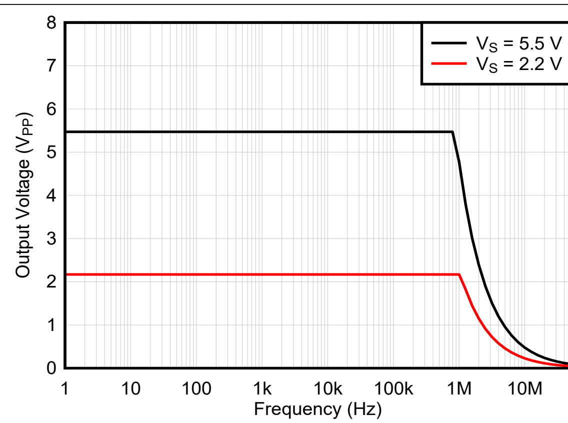
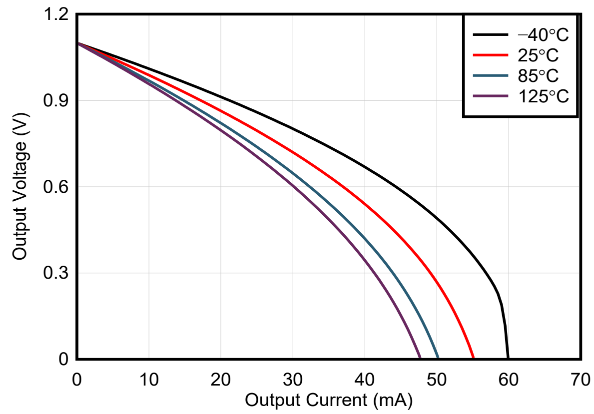


Figure 5-19. Maximum Output Voltage vs Frequency

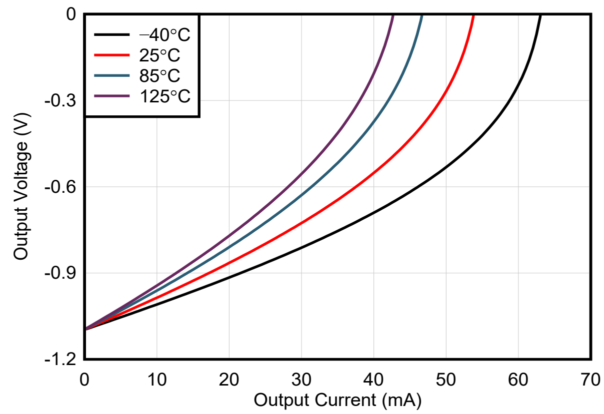
5.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5 V, V_{CM} = V_{OUT} = mid-supply, C_L = 20 pF, and R_L = 10 kΩ (unless otherwise noted)



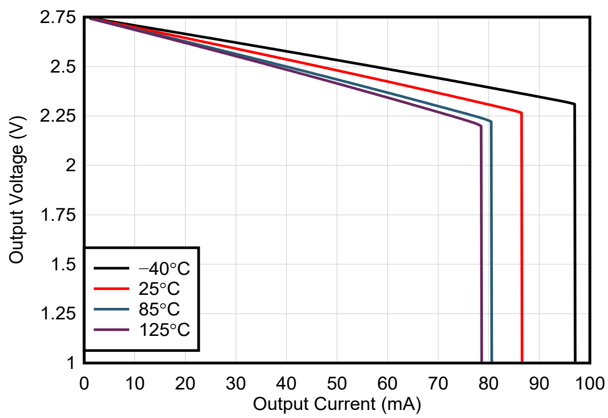
V_{V+} = 1.1 V, $V_{V–}$ = –1.1 V, current source load

Figure 5-20. Output Voltage Swing vs Output Current



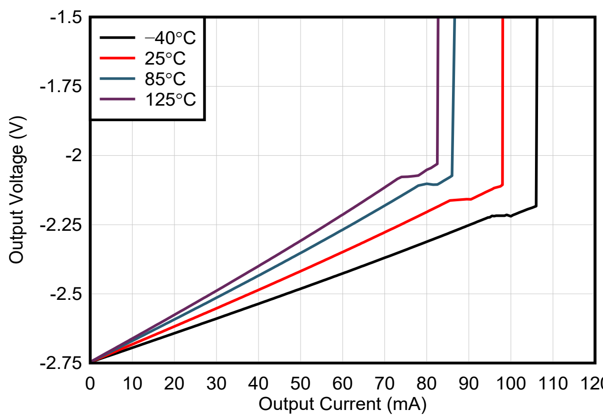
V_{V+} = 1.1 V, $V_{V–}$ = –1.1 V, current source load

Figure 5-21. Output Voltage Swing vs Output Current



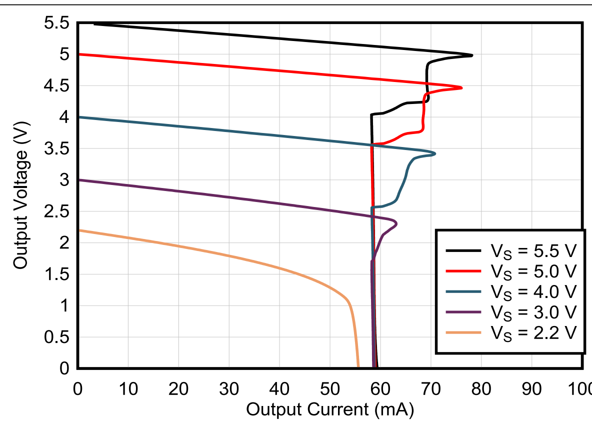
V_{V+} = 2.75 V, $V_{V–}$ = –2.75 V, current source load

Figure 5-22. Output Voltage Swing vs Output Current



V_{V+} = 2.75 V, $V_{V–}$ = –2.75 V, current source load

Figure 5-23. Output Voltage Swing vs Output Current



V_{V+} = 5.5 V, $V_{V–}$ = 0 V, voltage source load

Figure 5-24. Output Voltage Swing vs Output Current

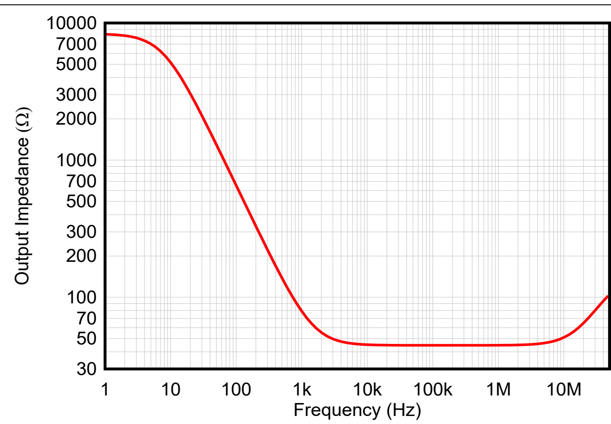


Figure 5-25. Open-Loop Output Impedance vs Frequency

5.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5 V, V_{CM} = V_{OUT} = mid-supply, C_L = 20 pF, and R_L = 10 kΩ (unless otherwise noted)

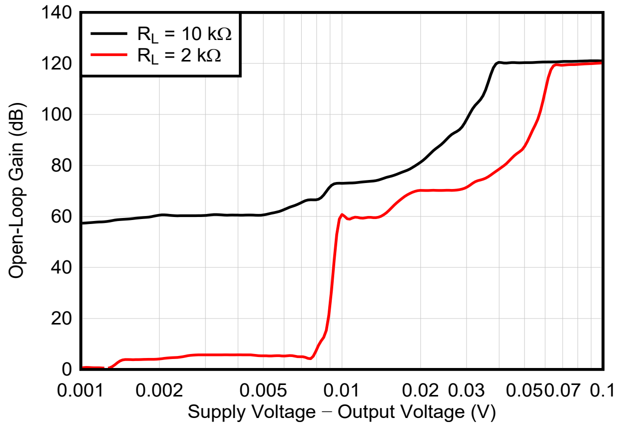
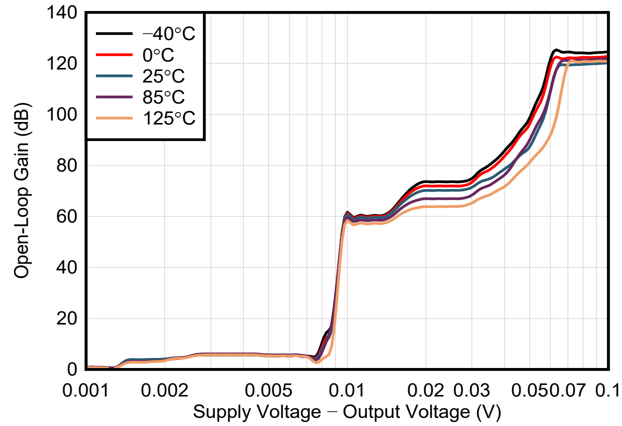
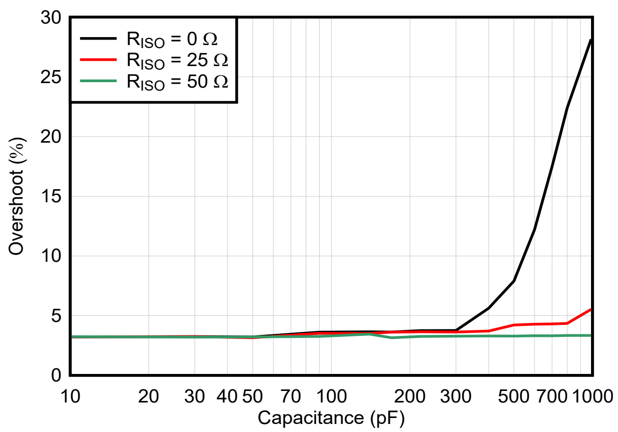


Figure 5-26. Open-Loop Gain vs Output to Supply Voltage Delta



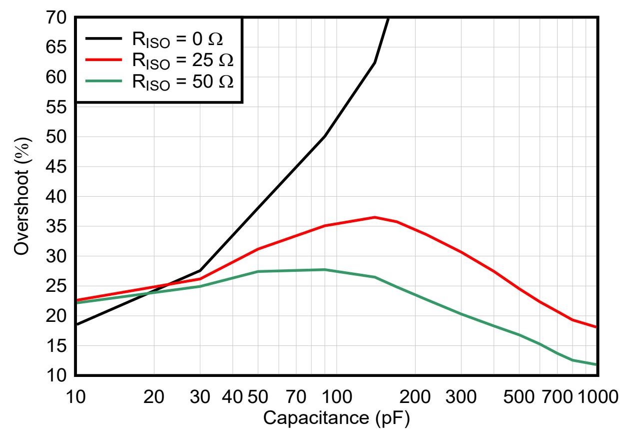
R_L = 2 kΩ

Figure 5-27. Open-Loop Gain vs Output to Supply Voltage Delta



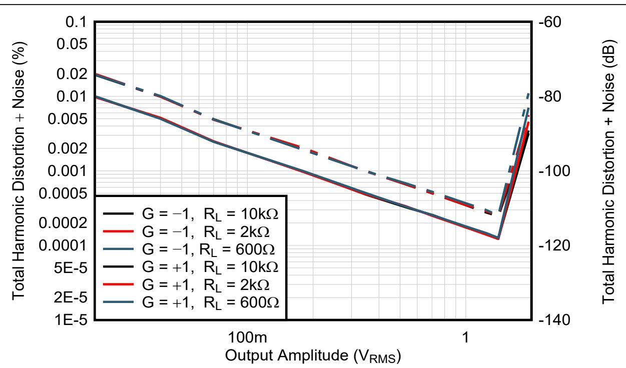
G = −1

Figure 5-28. Small-Signal Overshoot vs Load Capacitance



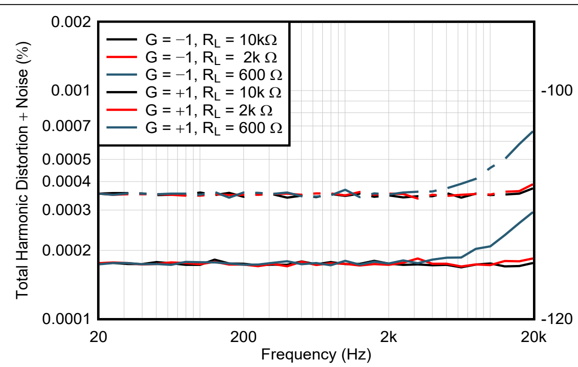
G = +1

Figure 5-29. Small-Signal Overshoot vs Load Capacitance



f = 1 kHz

Figure 5-30. THD+N vs Amplitude



V_{OUT} = 1 V_{RMS}

Figure 5-31. THD+N vs Frequency

5.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5 V, V_{CM} = V_{OUT} = mid-supply, C_L = 20 pF, and R_L = 10 kΩ (unless otherwise noted)

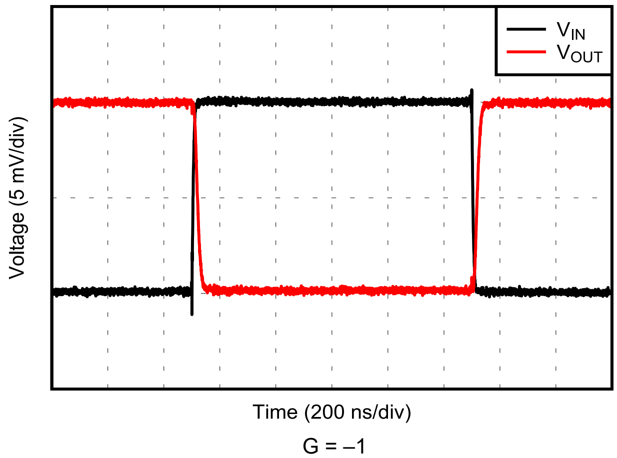


Figure 5-32. Small-Signal Step Response

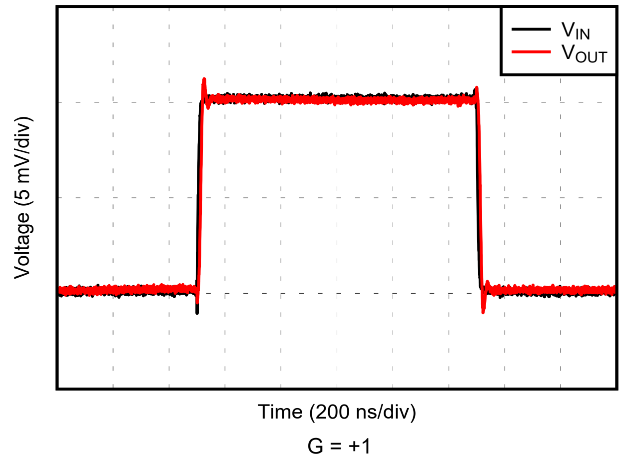


Figure 5-33. Small-Signal Step Response

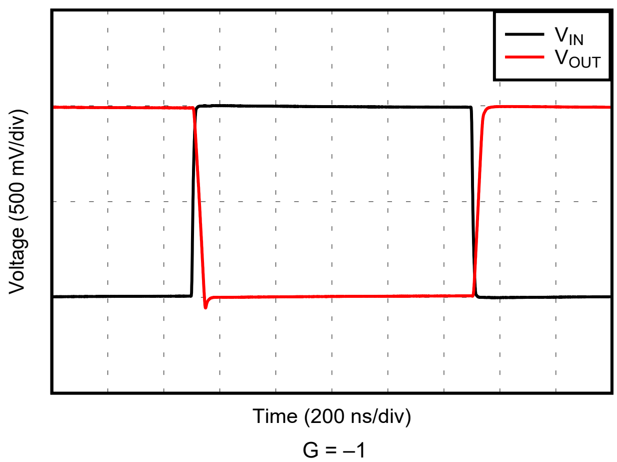


Figure 5-34. Large-Signal Step Response

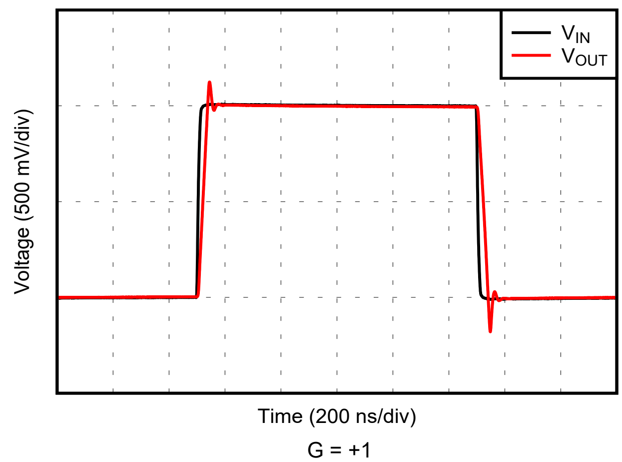


Figure 5-35. Large-Signal Step Response

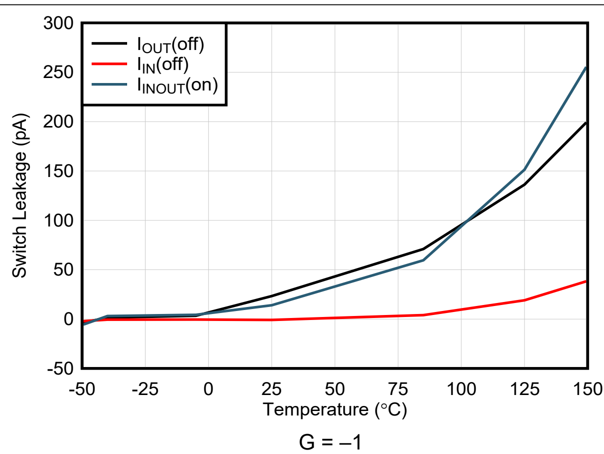


Figure 5-36. Switch Leakage Current vs Temperature

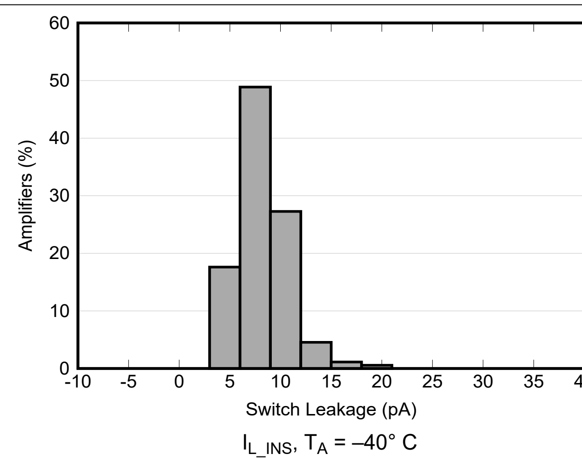


Figure 5-37. Switch Input Leakage Current Histogram

5.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5 V, V_{CM} = V_{OUT} = mid-supply, C_L = 20 pF, and R_L = 10 kΩ (unless otherwise noted)

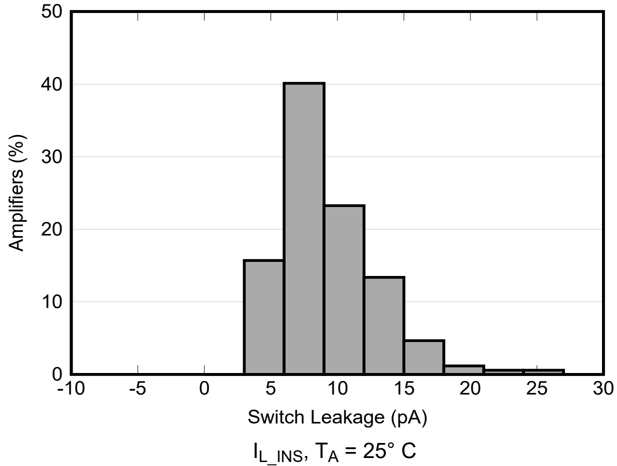


Figure 5-38. Switch Input Leakage Current Histogram

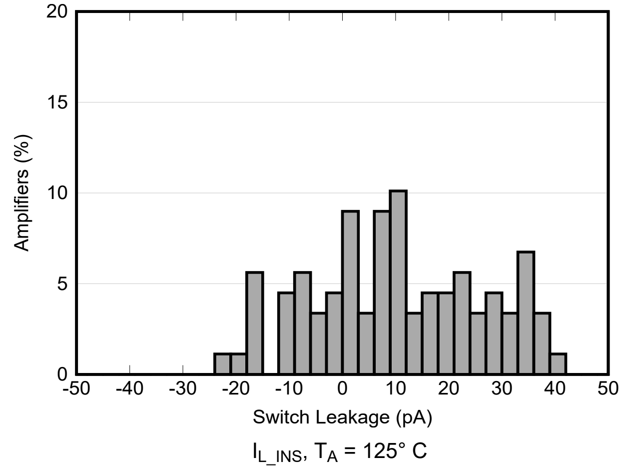


Figure 5-39. Switch Input Leakage Current Histogram

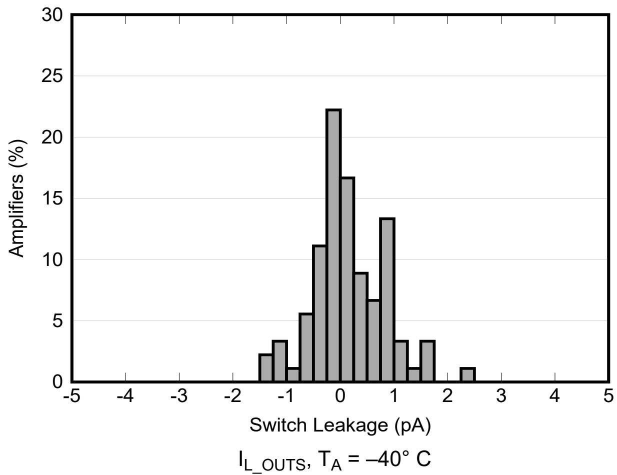


Figure 5-40. Switch Output Leakage Current Histogram

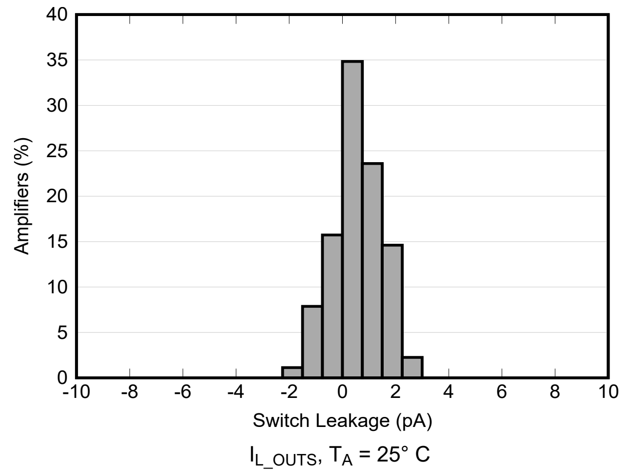


Figure 5-41. Switch Output Leakage Current Histogram

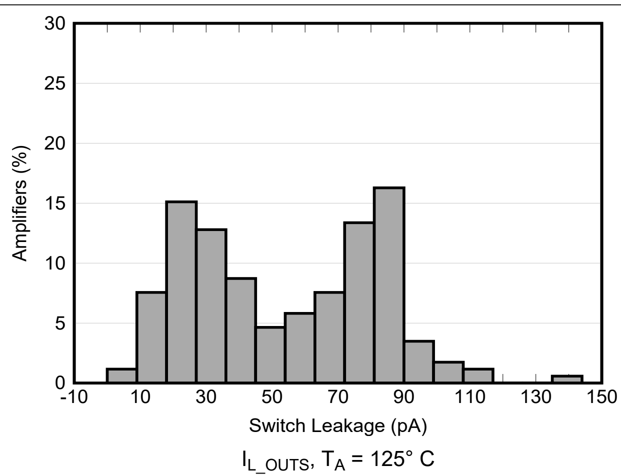


Figure 5-42. Switch Output Leakage Current Histogram

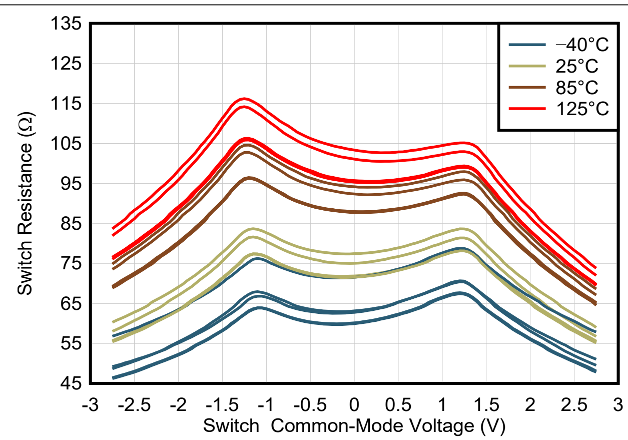


Figure 5-43. Switch On-Resistance vs Common-Mode Voltage

5.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5 V, V_{CM} = V_{OUT} = mid-supply, C_L = 20 pF, and R_L = 10 kΩ (unless otherwise noted)

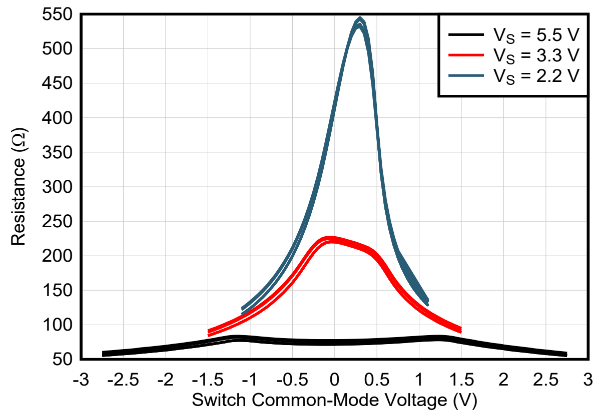


Figure 5-44. Switch On-Resistance vs Common-Mode Voltage

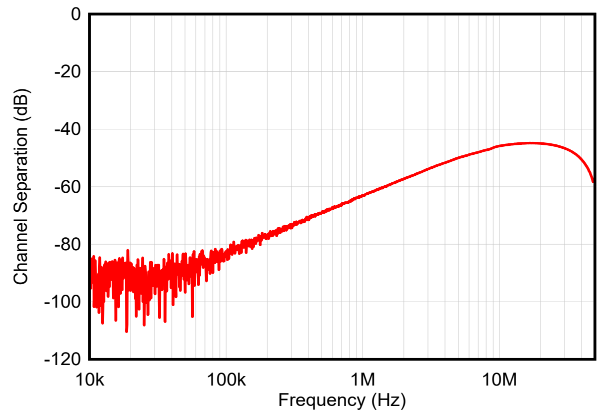


Figure 5-45. Switch Crosstalk vs Frequency

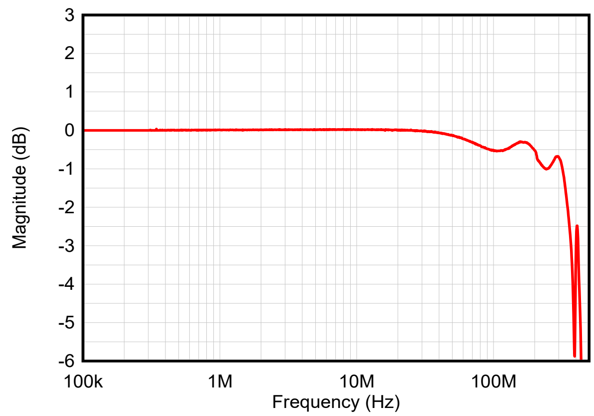


Figure 5-46. Switch Attenuation vs Frequency

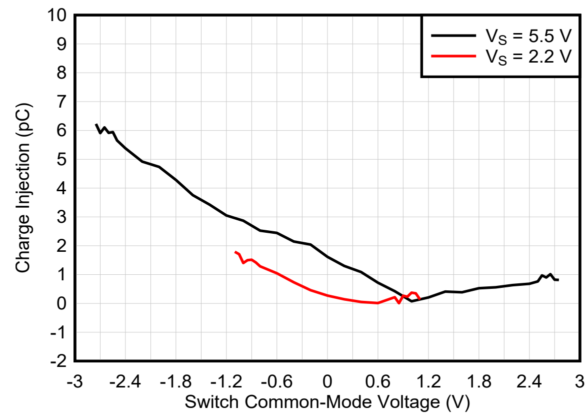


Figure 5-47. Switch Charge Injection vs Common-Mode Voltage

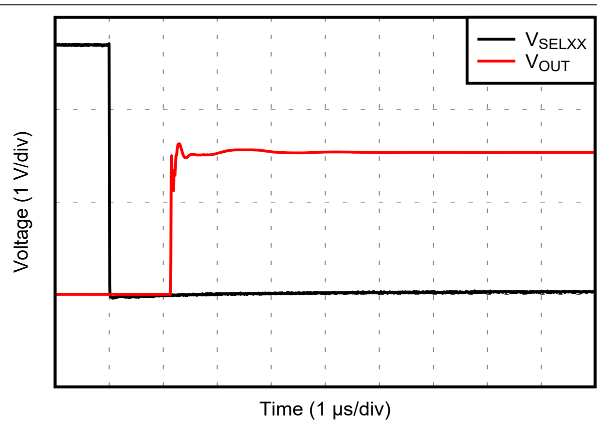


Figure 5-48. Switch Turn-on

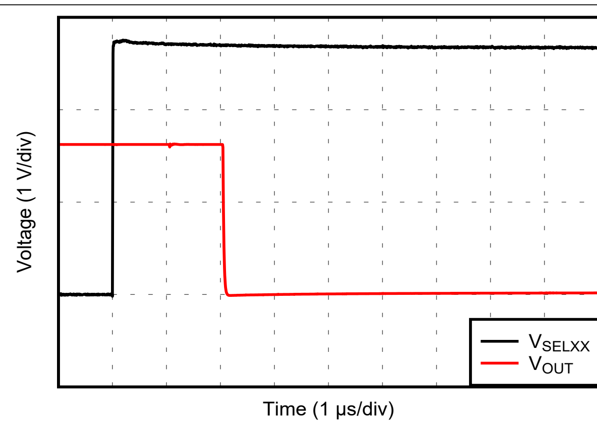


Figure 5-49. Switch Turn-off

6 Parameter Measurement Information

6.1 Switch Characterization Configurations

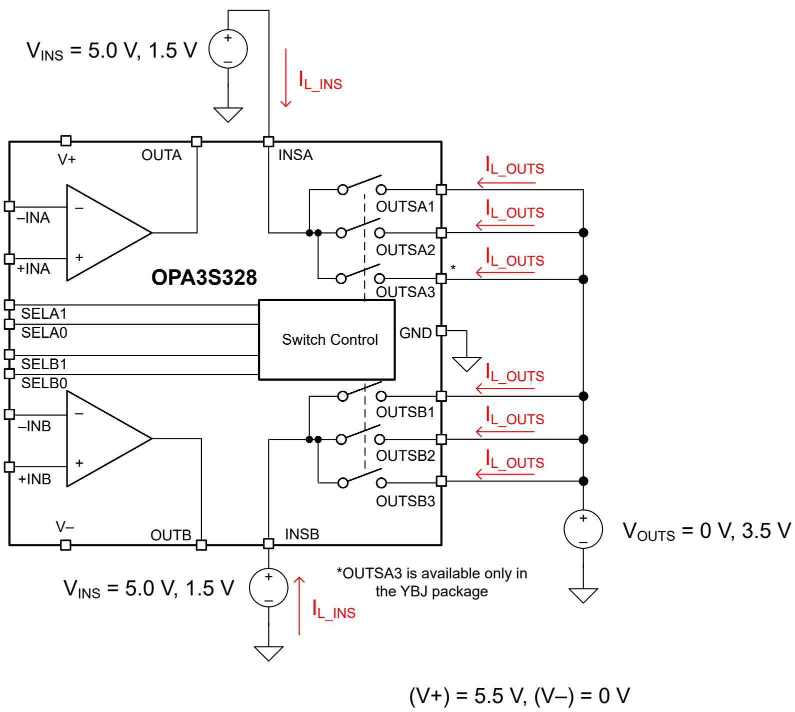


Figure 6-1. Switch Leakage Current, Open

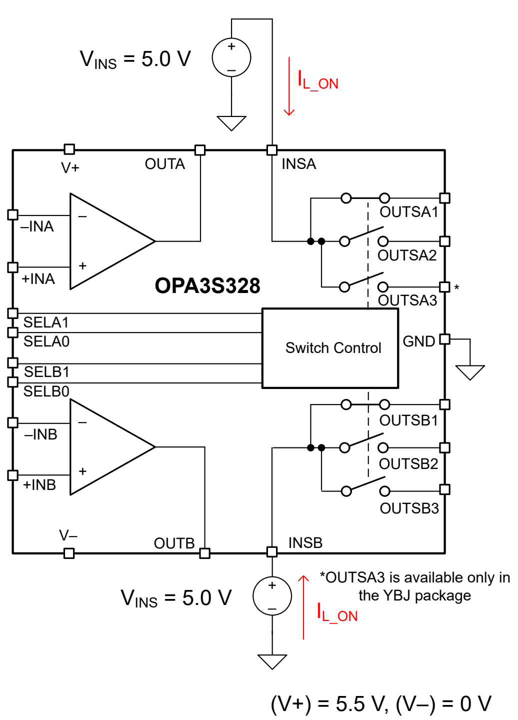


Figure 6-2. Switch Leakage Current, Closed

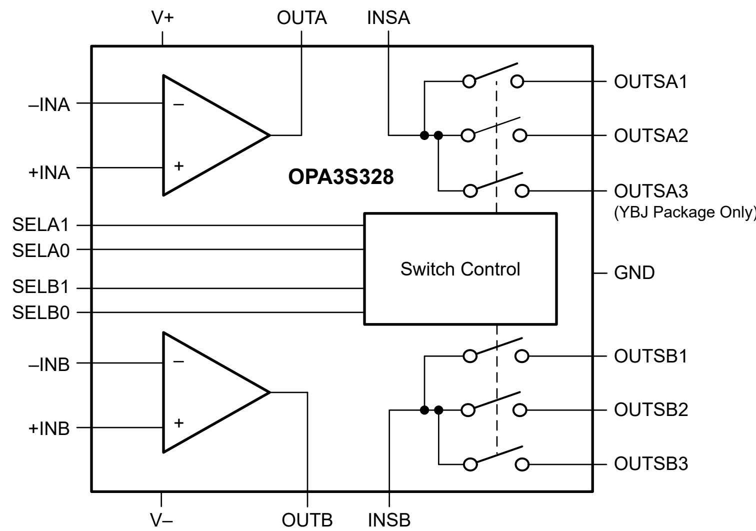
7 Detailed Description

7.1 Overview

The OPA3S328 features two high-speed, precision amplifiers combined with programmable switches that are designed to offer a compact sensor or optical interface for high resolution analog-to-digital converters (ADCs). Low output impedance with flat frequency characteristics and zero-crossover distortion circuitry enable high linearity over the full input common-mode range, achieving true rail-to-rail input from a 2.2-V to 5.5-V single supply. Integrated switches allow for multiple gain settings on a single amplifier stage without the need for an additional multiplexer device.

In addition to transimpedance applications, the OPA3S328 is flexible with many different application uses for a variety of equipment, such as optical modules, battery testers, medical instrumentation. This device can be used to replace larger transimpedance amplifiers, log amplifiers, programmable gain amplifiers, or programmable active filters.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Low Operating Voltage

The OPA3S328 amplifiers and switches operate on a single-supply voltage (2.2 V to 5.5 V), or a dual-supply voltage (±1.1 V to ±2.75 V), making these devices highly versatile, and easy to use with low supply rails. Use local bypass ceramic capacitors (typically, 0.001 µF to 0.1 µF) to ground on the power-supply pins, as well as a bypass capacitor connected between the positive and negative supply pins for dual-supply operation.

The digital input pins for switch and shutdown control (SELA0, SELA1, SELB0, SELB1) are referenced to the V+ supply for the positive rail, and to the digital ground (GND pin) for the negative rail. The GND pin can be forced to any voltage greater than V– and less than V+. However, the voltage between GND and V+ must be greater than the minimum requirement for the digital circuit block operation; see Section 7.4. For single-supply use cases, connect GND to V–.

The OPA3S328 amplifiers are fully specified from 2.2 V to 5.5 V and over the temperature range of –40°C to +125°C.

7.3.2 Input and ESD Protection

The OPA3S328 incorporates internal electrostatic discharge (ESD) protection circuits on all pins. In the case of input and output pins, this protection primarily consists of current-steering diodes connected between the input and power-supply pins. These ESD protection diodes also provide in-circuit input overdrive protection, provided that the current is limited to 10 mA. Many input signals are inherently current-limited to less than 10 mA; therefore, a limiting resistor is not required. Figure 7-1 shows how a series input resistor (R_S) can be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input; therefore, keep this value to a minimum in noise-sensitive applications.

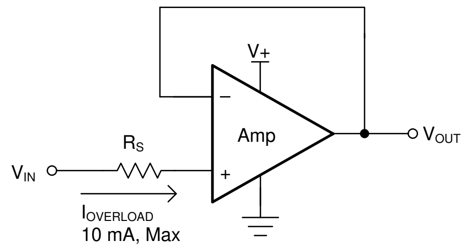


Figure 7-1. Input Current Protection

7.3.3 Programmable Switches

The OPA3S328 features integrated switches that can be used in many different configurations. Two sets of switches each have a single input (INSA and INSB) that multiplexes to two or three different outputs (OUTSA1, 2, and 3 and OUTSB1, 2, and 3). The QFN package has both a 1-to-2 switch matrix and a 1-to-3 switch matrix. The DSBGA package has two 1-to-3 switch matrices. The switches feature *make-before-break* switching, meaning that when programmed to a different switch connection, the previous switch does not change to high-impedance state until the new switch is closed, with a typical 2-µs delay when both switches are closed. This feature keeps the amplifier from operating in an open-loop state when the switches are used in a switched-gain transimpedance configuration.

7.3.4 Rail-to-Rail Input

The OPA3S328 features true rail-to-rail input operation, with supply voltages as low as ±1.1 V (2.2 V). The design of the OPA3S328 amplifiers include an internal charge-pump that powers the amplifier input stage with an internal supply rail at approximately 1.6 V greater than the external supply (V_{S+}). This internal supply rail allows the single differential input pair to operate and remain very linear over a very-wide input common-mode range. A unique zero-crossover input topology eliminates the input offset transition region typical of many rail-to-rail, complementary-input-stage, operational amplifiers. This topology allows the OPA3S328 to provide excellent common-mode performance (CMRR > 120 dB, typical) over the entire common-mode input range, which extends 100 mV beyond both power-supply rails. When driving analog-to-digital converters (ADCs), the highly linear V_{CM} range of the OPA3S328 provides maximum linearity and lowest distortion.

7.3.5 Phase Reversal

The OPA3S328 op amps are designed to be immune to phase reversal when the input pins exceed the supply voltages, and thus provide further in-system stability and predictability. Figure 7-2 shows the input voltage exceeding the supply voltage without any phase reversal.

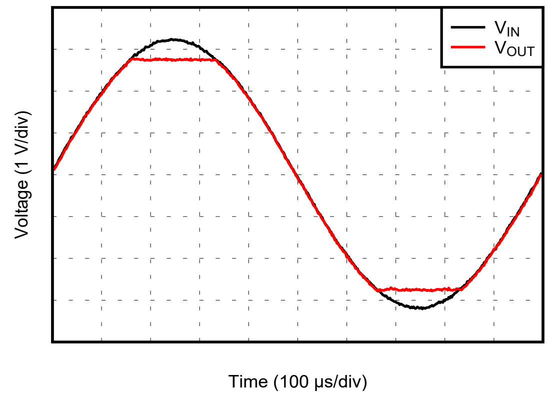


Figure 7-2. No Phase Reversal

7.4 Device Functional Modes

The OPA3S328 is specified to operate when power-supply voltages are between 2.2 V to 5.5 V (single-ended). Each amplifier can also be placed in power-down mode, as described in the in the following subsection.

7.4.1 Power-Down Mode

The OPA3S328 amplifiers can be placed into a power-down state independently. When in this power-down state, the output of the amplifier is high-impedance (> 1 GΩ) and the amplifier consumes 30 µA of quiescent current.

Power down is controlled through digital logic pins SELA0, SELA1, SELB0 and SELB1, which require a minimum 1.8 V between V+ and GND to provide functionality. For guidance on programming the device for power down, see the logic table in Table 4-3.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The OPA3S328 offers a unique combination of two outstanding dc and ac performance amplifiers, along with integrated low-leakage switches. This combination of devices can be configured in a variety of ways in many different circuit blocks, such as switched-gain transimpedance amplifiers, switched-gain voltage amplifiers, programmable frequency active filters, and flexible analog-to-digital converter front ends.

8.1.1 Capacitive Load and Stability

The OPA3S328 is designed to be used in high-speed applications for TIA and ADC input-driving amplifiers. As with all op amps, there can be specific instances where the OPA3S328 becomes unstable. The particular op-amp circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether an amplifier is stable in operation. An op amp in the unity-gain (1-V/V) buffer configuration and driving a capacitive load exhibits a greater tendency to become unstable than an amplifier operated at a higher noise gain, as seen in Figure 5-29. The capacitive load, in conjunction with the op amp output resistance, creates a pole within the feedback loop that degrades the phase margin. The degradation of the phase margin increases as the capacitive loading increases. When operating in the unity-gain configuration, the OPA3S328 remains stable with a pure capacitive load up to 100 pF.

One technique to increase the capacitive load drive capability of an amplifier operating in a unity-gain configuration is to insert a small resistor (R_S), typically 10 Ω to 50 Ω, in series with the output. Figure 8-1 shows this technique. This resistor significantly reduces the overshoot and ringing associated with large capacitive loads.

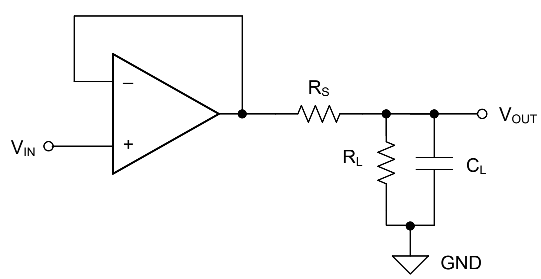


Figure 8-1. Improving Capacitive Load Drive

8.1.2 EMI Susceptibility and Input Filtering

Operational amplifiers vary in susceptibility to electromagnetic interference (EMI). If conducted EMI enters the operational amplifier, the dc offset observed at the amplifier output can shift from the nominal value while EMI is present. This shift is a result of signal rectification associated with the internal semiconductor junctions. While all operational amplifier pin functions can be affected by EMI, the input pins are most likely susceptible. The OPA3S328 operational amplifiers incorporate an internal input low-pass filter that reduces the amplifiers response to EMI. Both common-mode and differential-mode filtering are provided by the input filter. Figure 8-2 shows the amplifier EMIRR response.

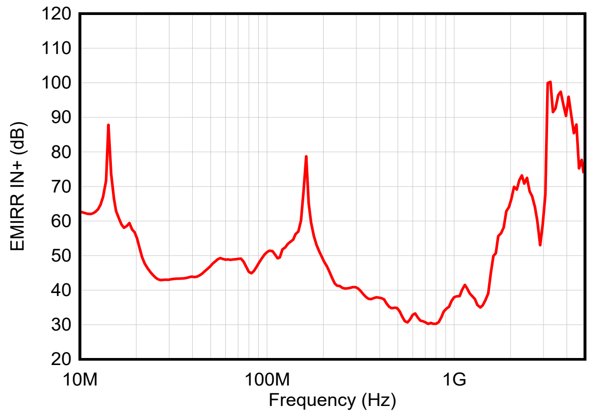


Figure 8-2. OPA3S328 EMIRR Response

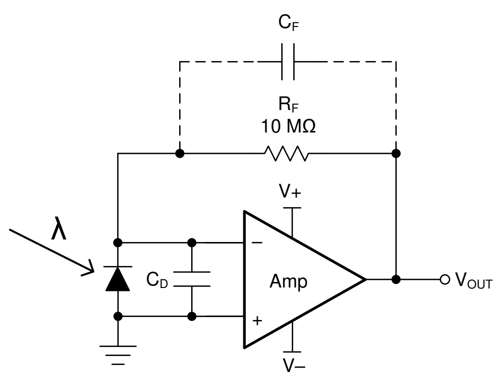
8.1.3 Transimpedance Amplifier

Wide gain bandwidth, low-input bias current, low input voltage, and current noise make the OPA3S328 an excellent wideband photodiode transimpedance amplifier. Low-voltage noise is important because photodiode capacitance causes the effective noise gain of the circuit to increase at high frequency.

Figure 8-3 shows the key elements to a transimpedance design, which are:

- expected diode capacitance (C_D); include the parasitic input common-mode voltage and differential-mode input capacitance
- desired transimpedance gain (R_F)
- gain-bandwidth (GBW) for the OPA3S328 (40 MHz)

With these three variables set, the feedback capacitor value (C_F) can be set to control the frequency response. C_F includes the stray capacitance of R_F, which is 0.2 pF for a typical surface-mount resistor.



NOTE: C_F is optional to prevent gain peaking, and includes the stray capacitance of R_F.

Figure 8-3. Dual-Supply Transimpedance Amplifier

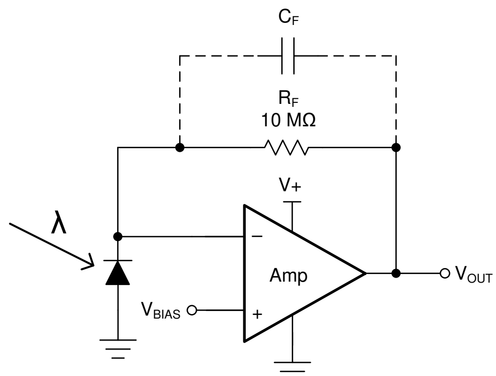
For optimized frequency response, set the feedback pole as follows:

$$\frac{1}{2\pi R_F C_F} = \sqrt{\frac{GBW}{4\pi R_F C_D}} \quad (1)$$

Equation 2 calculates the bandwidth.

$$f_{-3dB} = \sqrt{\frac{GBW}{2\pi R_F C_D}} \quad (Hz) \quad (2)$$

For single-supply applications, the +IN input can be biased with a positive dc voltage to allow the output to reach true zero when the photodiode is not exposed to any light, and respond without the added delay that results from coming out of the negative rail. Figure 8-4 shows this configuration. This bias voltage also appears across the photodiode, providing a reverse bias for faster operation.



NOTE: C_F is optional to prevent gain peaking, and includes the stray capacitance of R_F.

Figure 8-4. Single-Supply Transimpedance Amplifier

For more information, see the *Compensate Transimpedance Amplifiers Intuitively* and *Build a Programmable Gain Transimpedance Amplifier Using the OPA3S328* application reports.

8.1.3.1 Optimizing the Transimpedance Circuit

To achieve the best performance, select components according to the following guidelines:

1. For the lowest noise, select R_F to create the total required gain. A lower value for R_F and adding gain after the transimpedance amplifier generally produces poorer noise performance. The noise produced by R_F increases with the square-root of R_F; whereas, the signal increases linearly. Therefore, signal-to-noise ratio improves when all the required gain is placed in the transimpedance stage.
2. Minimize photodiode capacitance and stray capacitance at the summing junction (inverting input). This capacitance causes the op-amp voltage noise to be amplified (increased amplification at high frequency). Use a low-noise voltage source to reverse-bias a photodiode to significantly reduce capacitance. Smaller photodiodes have lower capacitance. Use optics to concentrate light on a small photodiode.
3. Noise increases with increased bandwidth. Limit the circuit bandwidth to only that required. Use a capacitor across the R_F to limit bandwidth, even if not required for stability.
4. Circuit board leakage can degrade the performance of an otherwise well-designed amplifier. Clean the circuit board carefully. A circuit-board guard trace that encircles the summing junction and is driven at the same voltage helps to control leakage.

For more information, see the *Noise Analysis of FET Transimpedance Amplifiers* and the *Noise Analysis for High-Speed Op Amps* application reports.

8.2 Typical Application

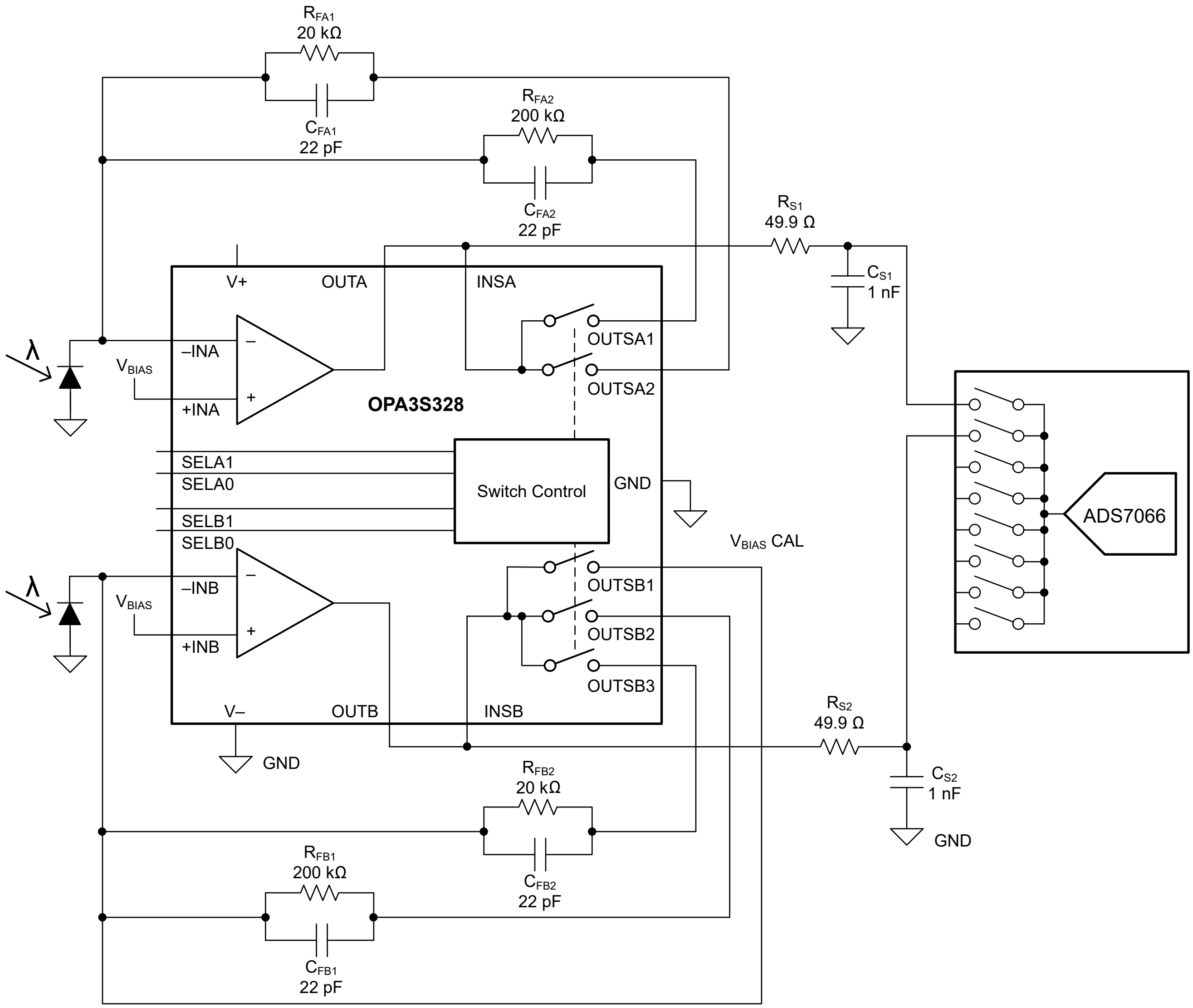


Figure 8-5. Dual Transimpedance Front End With Gain Switching

8.2.1 Design Requirements

- Gain = 0.02 V/µA and 0.2 V/µA
- Low-pass cutoff frequency = 36 kHz
- 1% accuracy from 10 nA to 100 µA

8.2.2 Detailed Design Procedure

- Select transimpedance gains to align the measurement current range within the range of the ADC. For the ADS7066, the input range is programmed to 5 V. Using this configuration, the peak current range is calculated by dividing the input range by the feedback resistor, R_{FB}, which yields 25 μA for a 200-kΩ resistor and 250 μA for a 20-kΩ feedback resistor.
- The current measurement LSB size is 5 V / (R_F × 65536). The result yields 381 pA resolution for a 200-kΩ feedback resistor, and 3.81 nA resolution for a 20-kΩ resistor.
- A dc voltage is used on the noninverting pin of the amplifier for two important reasons. The first reason is to reverse-bias the photodiode, which helps reduce photodiode capacitance and makes sure the photodiode does not operate in a forward-bias state. The second reason is to keep the output voltage of the amplifier from coming too close to the negative supply (V–) voltage when the input current is zero. If the output voltage comes within approximately 40 mV (assuming a 10-kΩ load), the amplifier enters a saturation state, which results in loss of open-loop gain and slow transient response to exit the state (overload recovery). Typically 100 mV is enough to make sure that the amplifier does not saturate.
- A feedback capacitor can be used to help the stability of the circuit. Typically, if the feedback capacitor has a higher capacitance than the total input capacitance, advanced compensation schemes are not necessary to maintain stability of the amplifier along with the capacitance of the photodiode. This configuration can limit the usable bandwidth of the circuit; see Section 8.1.3.1 for further details.

8.2.3 Application Curve

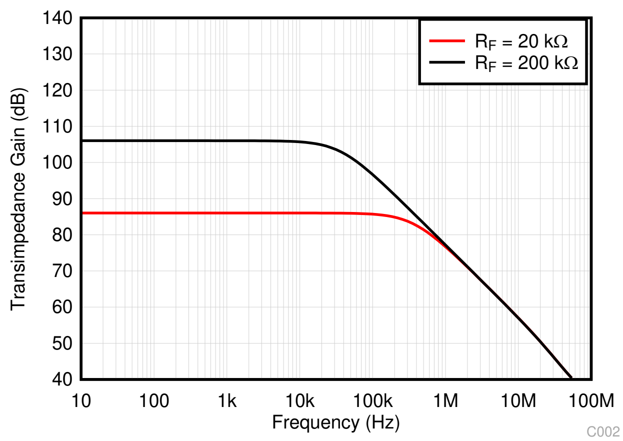


Figure 8-6. OPA3S328 Transimpedance Gain

8.3 Power Supply Recommendations

The OPA3S328 is specified for operation from 2.2 V to 5.5 V (±1.1 V to ±2.75 V), and many specifications apply from –40°C to +125°C.

CAUTION

Supply voltages larger than 6 V can permanently damage the device; see Section 5.1.

Place 0.1-μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see Section 8.4.

8.4 Layout

8.4.1 Layout Guidelines

The OPA3S328 contains two wideband amplifiers and an integrated charge pump. To realize the full operational performance of the device and remove the noise from the charge pump circuit, good high-frequency PCB layout practices must be employed. The bypass capacitors must be connected between each supply pin and ground as close to the device as possible. Additionally, in dual-supply systems, there must be a ceramic bypass capacitor between the supply pins. Use bypass capacitor traces designed for minimum inductance.

8.4.2 Layout Example

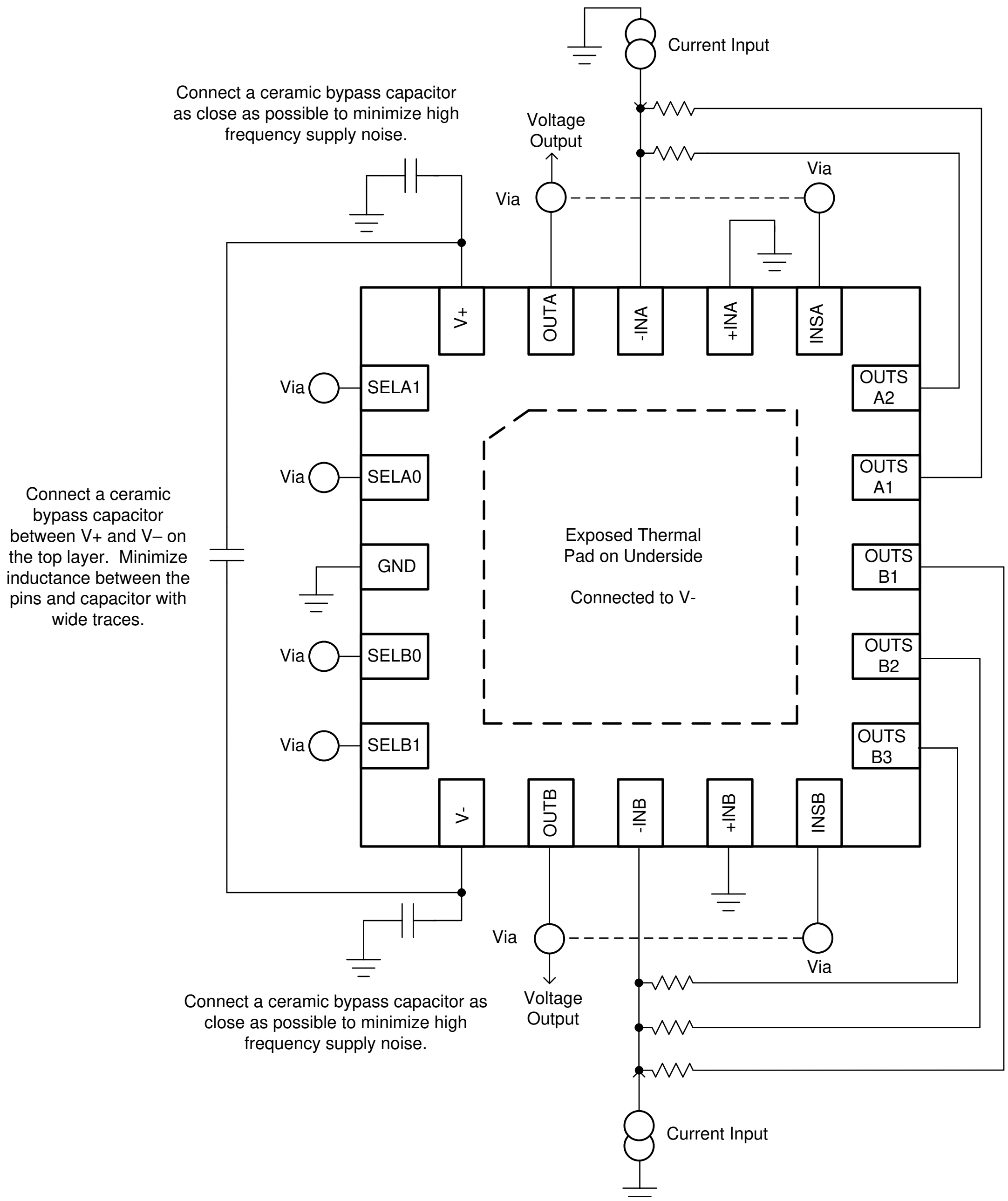


Figure 8-7. Layout Example

9 Device and Documentation Support

9.1 Device Support

9.1.1 Development Support

9.1.1.1 PSpice® for TI

PSpice® for TI is a design and simulation environment that helps evaluate performance of analog circuits. Create subsystem designs and prototype solutions before committing to layout and fabrication, reducing development cost and time to market.

9.1.1.2 TINA-TI™ Simulation Software (Free Download)

TINA-TI™ simulation software is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI simulation software is a free, fully-functional version of the TINA™ software, preloaded with a library of macromodels, in addition to a range of both passive and active models. TINA-TI simulation software provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Design tools and simulation web page, TINA-TI simulation software offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

Note

These files require that either the TINA software or TINA-TI software be installed. Download the free TINA-TI simulation software from the TINA-TI™ software folder.

9.1.1.3 TI Reference Designs

TI reference designs are analog solutions created by TI's precision analog applications experts. TI reference designs offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits. TI reference designs are available online at https://www.ti.com/reference-designs.

9.1.1.4 Filter Design Tool

The filter design tool is a simple, powerful, and easy-to-use active filter design program. The filter design tool allows the user to create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners.

Available as a web-based tool from the Design tools and simulation web page, the filter design tool allows the user to design, optimize, and simulate complete multistage active filter solutions within minutes.

9.2 Documentation Support

9.2.1 Related Documentation

The following documents are relevant to using the OPA3S328, and recommended for reference. All are available for download at www.ti.com (unless otherwise noted):

- Texas Instruments, *PM2.5/PM10 Particle Sensor Analog Front-End for Air Quality Monitoring Design*
- Texas Instruments, *QFN/SON PCB Attachment*
- Texas Instruments, *Quad Flatpack No-Lead Logic Packages*
- Texas Instruments, *Compensate Transimpedance Amplifiers Intuitively*
- Texas Instruments, *Noise Analysis of FET Transimpedance Amplifiers*
- Texas Instruments, *Noise Analysis for High-Speed Op Amps*
- Texas Instruments, *Build a Programmable Gain Transimpedance Amplifier Using the OPA3S328*

9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.5 Trademarks

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TINA™ is a trademark of DesignSoft, Inc.
PSpice® is a registered trademark of Cadence Design Systems, Inc.
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9.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.7 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (August 2023) to Revision D (December 2023) — **Page**

- Changed OPA3S328 YBJ (DSBGA, 24) package status from advanced information (preview with samples) to production data (active)........ 1

Changes from Revision B (November 2021) to Revision C (August 2023) — **Page**

- Changed OPA3S328 YBJ (DSBGA, 24) package status from preview (no samples) to advanced information (preview with samples)........ 1
- Changed the ESD rating to the bidirectional value........ 5
- Changed open-loop output impedance symbol from Ro to Zo........ 6

Changes from Revision A (September 2021) to Revision B (November 2021)	Page
• Changed YBJ preview Figure 5-2 to correct pin configuration	3

Changes from Revision * (October 2020) to Revision A (September 2021)	Page
• Changed OPA3S328 RGR (VQFN-20) package status from advanced information (preview) to production data (active)	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA3S328RGRR	Active	Production	VQFN (RGR) | 20	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	O3S328
OPA3S328RGRR.A	Active	Production	VQFN (RGR) | 20	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	O3S328
OPA3S328RGRT	Active	Production	VQFN (RGR) | 20	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	O3S328
OPA3S328RGRT.A	Active	Production	VQFN (RGR) | 20	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	O3S328
OPA3S328YBJR	Active	Production	DSBGA (YBJ) | 24	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	OPA3S328
OPA3S328YBJR.A	Active	Production	DSBGA (YBJ) | 24	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	OPA3S328

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

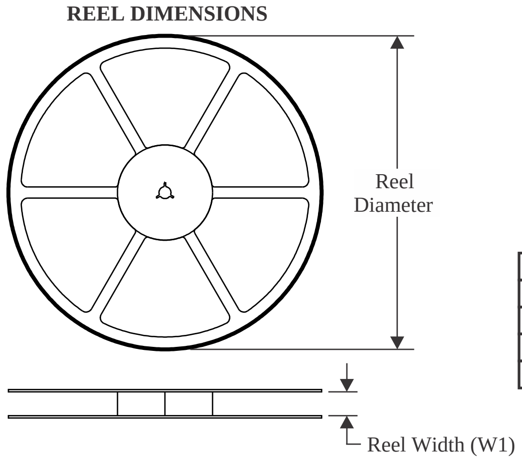
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

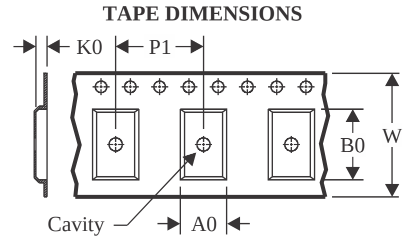
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

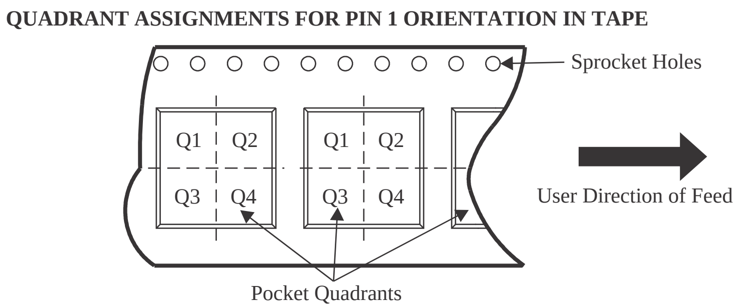
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION





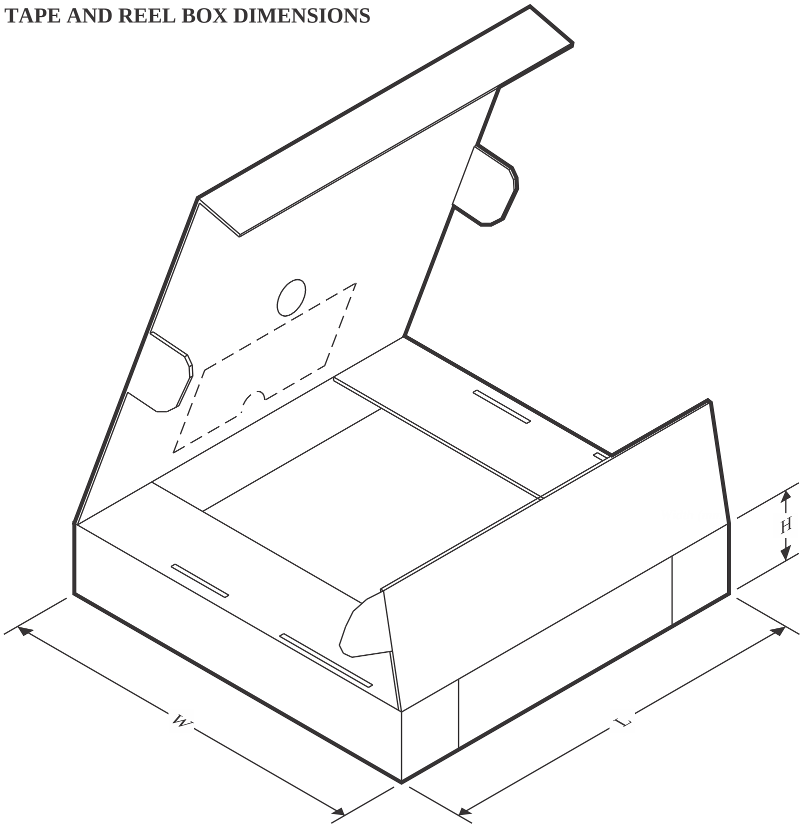
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

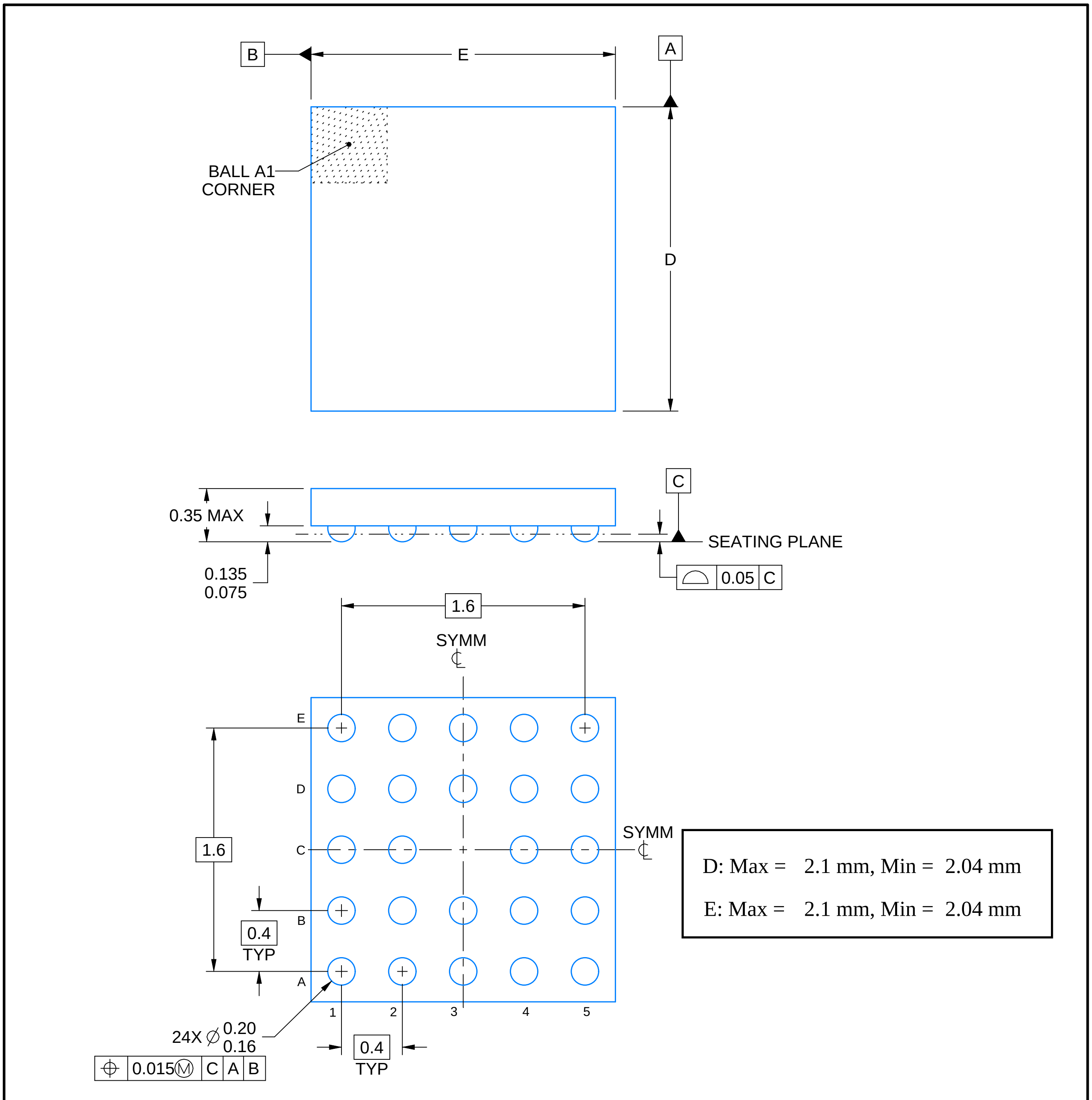
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA3S328RGRR	VQFN	RGR	20	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q2
OPA3S328RGRT	VQFN	RGR	20	250	180.0	12.4	3.75	3.75	1.15	8.0	12.0	Q2
OPA3S328YBJR	DSBGA	YBJ	24	3000	180.0	8.4	2.24	2.24	0.45	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

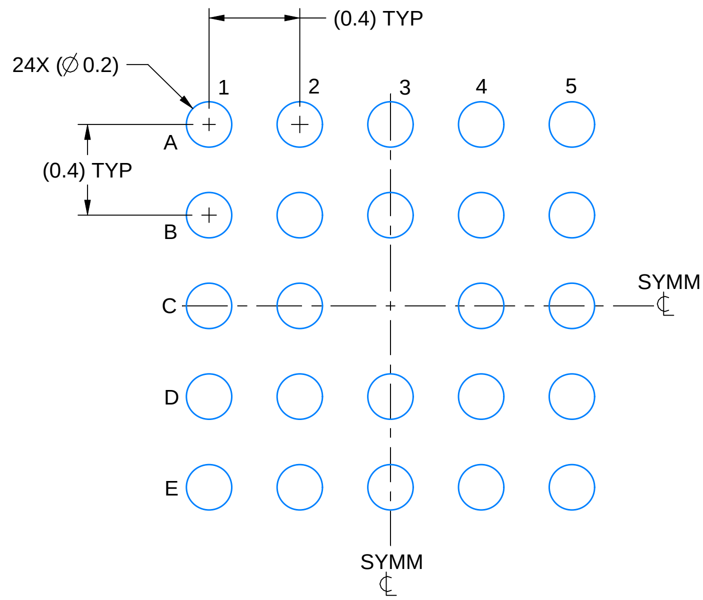
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA3S328RGRR	VQFN	RGR	20	3000	367.0	367.0	35.0
OPA3S328RGRT	VQFN	RGR	20	250	210.0	185.0	35.0
OPA3S328YBJR	DSBGA	YBJ	24	3000	182.0	182.0	20.0



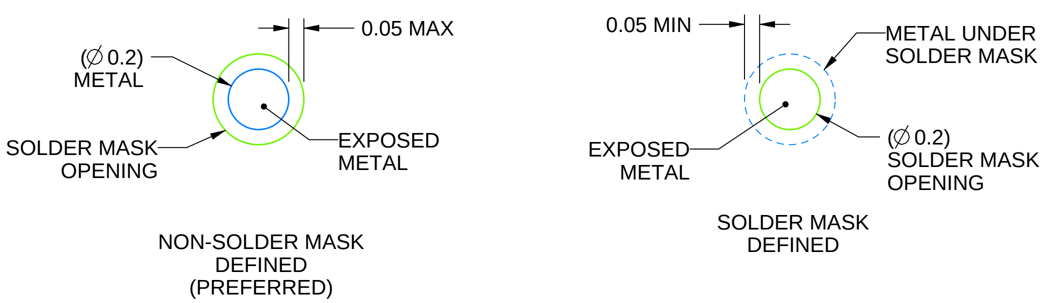
4226700/A 03/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 30X

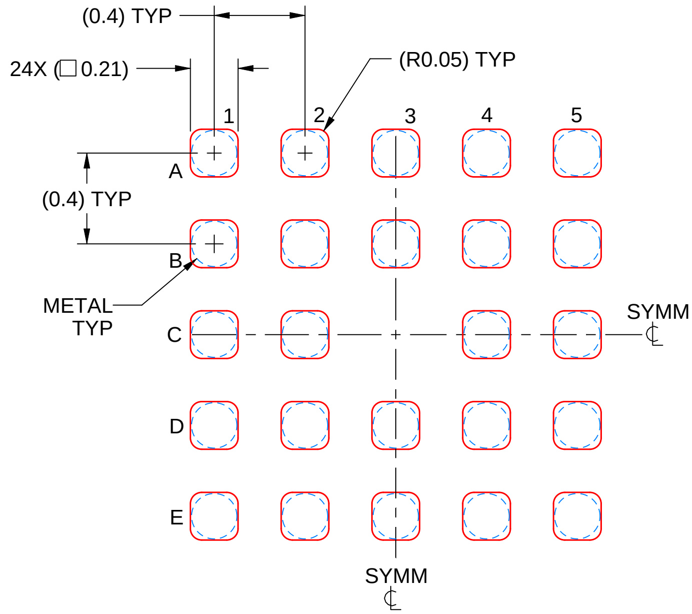


SOLDER MASK DETAILS
NOT TO SCALE

4226700/A 03/2021

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 30X

4226700/A 03/2021

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

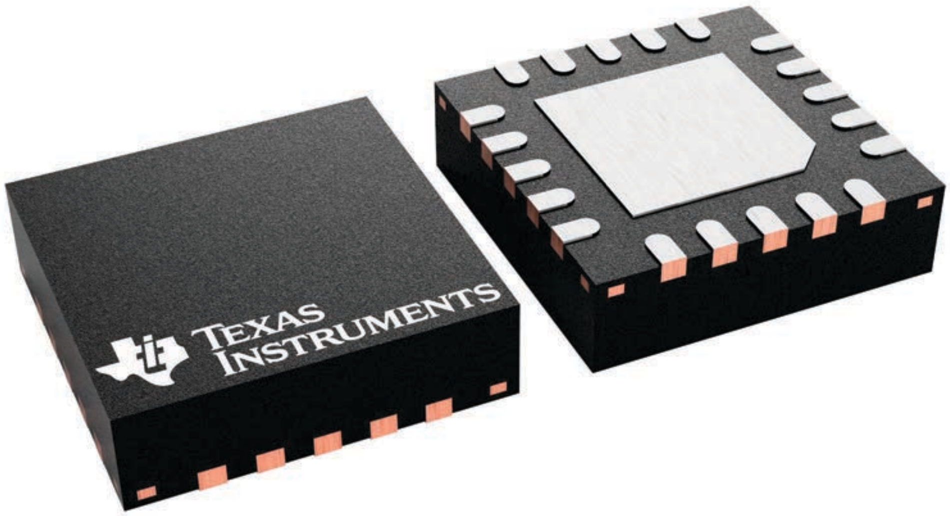
RGR 20

VQFN - 1 mm max height

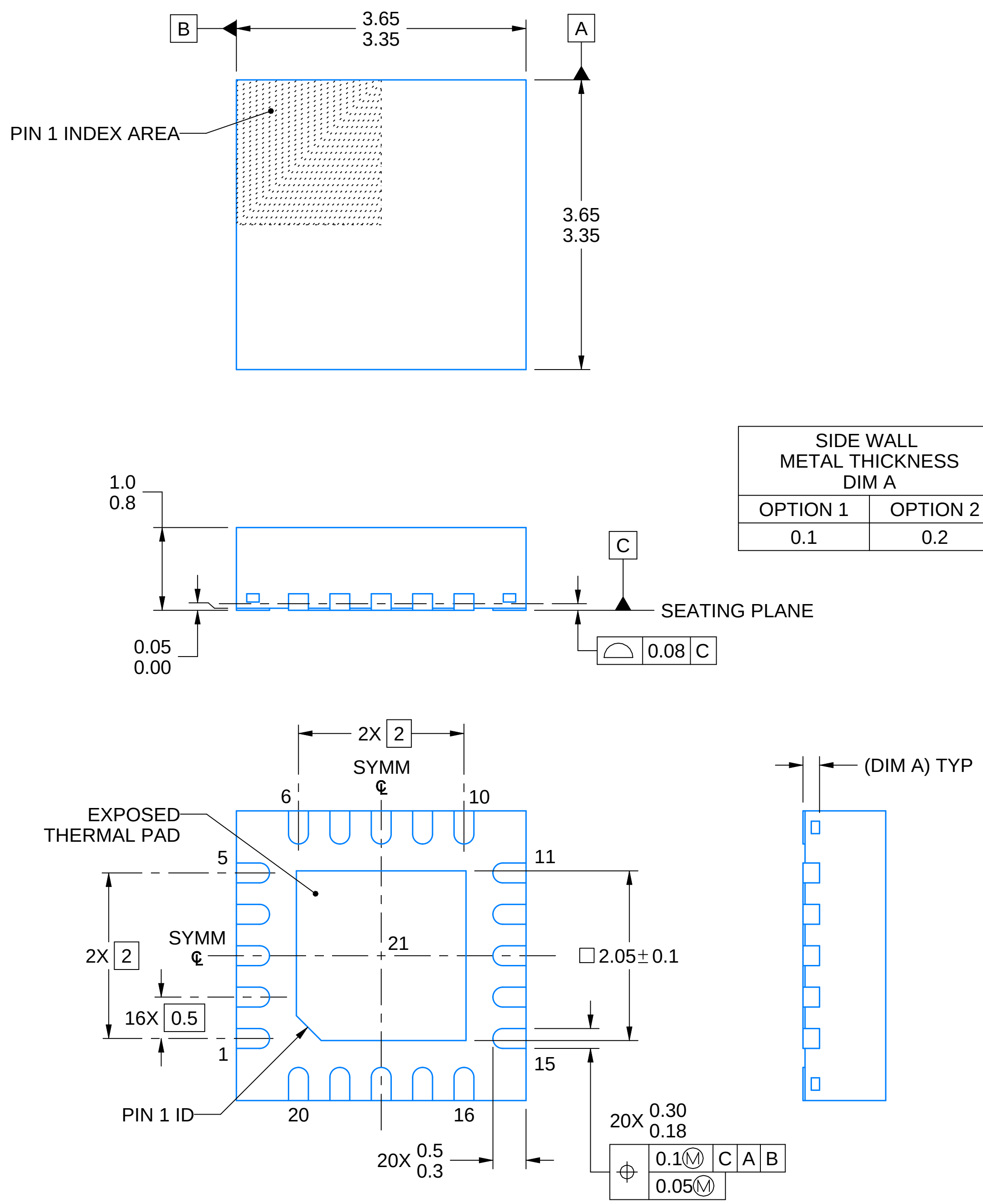
3.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4228482/A

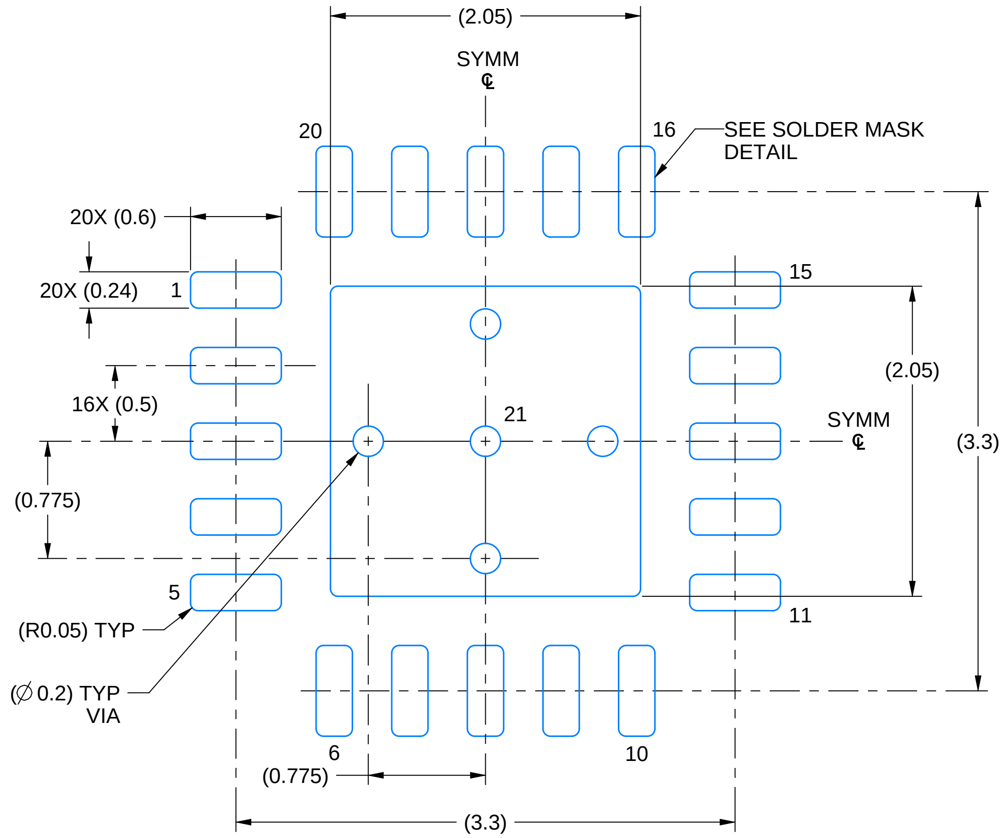


SIDE WALL METAL THICKNESS DIM A	
OPTION 1	OPTION 2
0.1	0.2

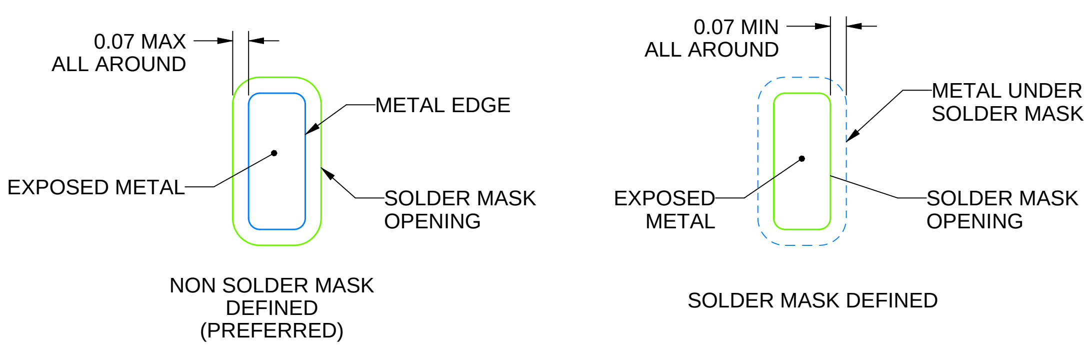
4219031/B 04/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

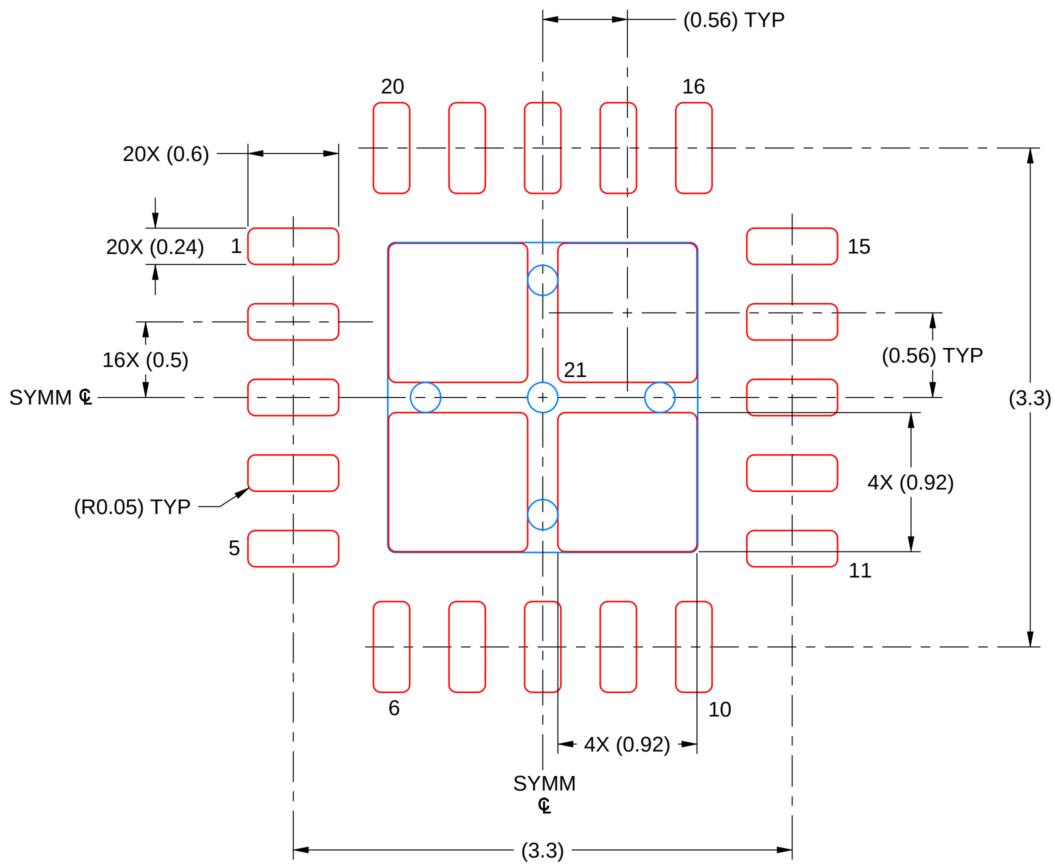


SOLDER MASK DETAILS

4219031/B 04/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 21
81% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4219031/B 04/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.