

# OPAx388 Precision, Zero-Drift, Zero-Crossover, True Rail-to-Rail, Input/Output Operational Amplifiers

## 1 Features

- Ultra-low offset voltage:  $\pm 0.25 \mu\text{V}$
- Zero drift:  $\pm 0.005 \mu\text{V}/^\circ\text{C}$
- Zero crossover: 140-dB CMRR true RRIO
- Low noise:  $7.0 \text{ nV}\sqrt{\text{Hz}}$  at 1 kHz
- No 1/f noise:  $140 \text{ nV}_{\text{PP}}$  (0.1 Hz to 10 Hz)
- Fast settling:  $2 \mu\text{s}$  (1 V to 0.01%)
- Gain bandwidth: 10 MHz
- Single supply: 2.5 V to 5.5 V
- Dual supply:  $\pm 1.25 \text{ V}$  to  $\pm 2.75 \text{ V}$
- True rail-to-rail input and output
- EMI/RFI filtered inputs
- Industry-standard packages:
  - Single in SOIC-8, SOT-23-5, and VSSOP-8
  - Dual in SOIC-8 and VSSOP-8
  - Quad in SOIC-14 and TSSOP-14

## 2 Applications

- [Merchant network and server PSU](#)
- [Notebook PC power adapter design](#)
- [Weigh scale](#)
- [Lab and field instrumentation](#)
- [Battery test](#)
- [Electronic thermometer](#)
- [Temperature transmitter](#)

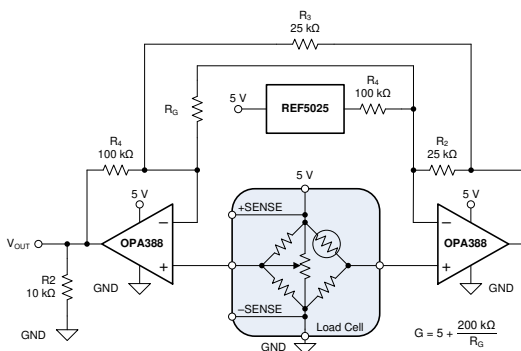
## 3 Description

The OPAx388 (OPA388, OPA2388, and OPA4388) series of precision operational amplifiers are ultra-low noise, fast-settling, zero-drift, zero-crossover devices that provide rail-to-rail input and output operation. These features and excellent ac performance, combined with only  $0.25 \mu\text{V}$  of offset and  $0.005 \mu\text{V}/^\circ\text{C}$  of drift over temperature, makes the OPAx388 a great choice for driving high-precision, analog-to-digital converters (ADCs) or buffering the output of high-resolution, digital-to-analog converters (DACs). This design results in excellent performance when driving analog-to-digital converters (ADCs) without degradation of linearity. The OPA388 (single version) is available in the VSSOP-8, SOT23-5, and SOIC-8 packages. The OPA2388 (dual version) is offered in the VSSOP-8 and SO-8 packages. The OPA4388 (quad version) is offered in the TSSOP-14 and SO-14 packages. All versions are specified over the industrial temperature range of  $-40^\circ\text{C}$  to  $+125^\circ\text{C}$ .

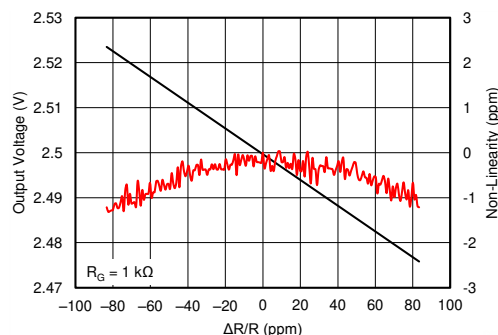
### Device Information

| PART NUMBER | PACKAGE <sup>(1)</sup> | BODY SIZE (NOM)   |
|-------------|------------------------|-------------------|
| OPA388      | SOIC (8)               | 4.90 mm × 3.90 mm |
|             | SOT-23 (5)             | 2.90 mm × 1.60 mm |
|             | VSSOP (8)              | 3.00 mm × 3.00 mm |
| OPA2388     | SOIC (8)               | 4.90 mm × 3.90 mm |
|             | VSSOP (8)              | 3.00 mm × 3.00 mm |
| OPA4388     | SOIC (14)              | 8.65 mm × 3.90 mm |
|             | TSSOP (14)             | 5.00 mm × 4.40 mm |

- (1) For all available packages, see the package option addendum at the end of the data sheet.



**The OPA388 in a High-CMRR, Instrumentation Amplifier Application**



**The OPA388 Allows Precision, Low-Error Measurements**



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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

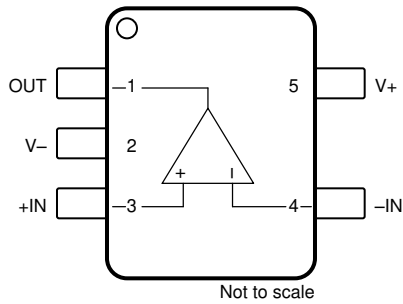
| <b>Changes from Revision C (May 2019) to Revision D (July 2020)</b>                                       | <b>Page</b> |
|---|-------------|
| • Changed OPA2388 SOIC-8 (D) package from advanced information (preview) to production data (active) .... | 1           |
| • Changed typical application schematic to show correct locations for reference designators.....          | 1           |
| • Changed Figure 8-5 to show correct locations for reference designators .....                            | 25          |

| <b>Changes from Revision B (January 2019) to Revision C (May 2019)</b>                 | <b>Page</b> |
|--|-------------|
| • Changed OPA4388 from advanced information (preview) to production data (active)..... | 1           |
| • Added VOS specifications for OPA4388.....  | 7           |
| • Added dVOS/dT specifications for OPA4388.....  | 7           |
| • Added PSRR specifications for OPA4388.....   | 7           |
| • Added IB specifications for OPA4388.....   | 7           |
| • Added IOS specifications for OPA4388.....  | 7           |
| • Added CMRR specifications for OPA4388.....   | 7           |
| • Added AOL specifications for OPA4388.....  | 7           |

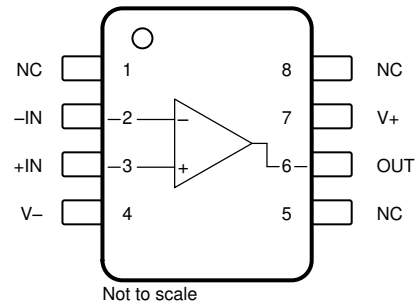
| <b>Changes from Revision A (July 2018) to Revision B (January 2019)</b>       | <b>Page</b> |
|---|-------------|
| • Changed OPA388 DBV (SOT-23) package from preview to production data .....   | 1           |
| • Deleted redundant temperature specification in EC table.....                | 7           |
| • Added Figure 6, <i>Offset Voltage vs Supply Voltage: OPA4388</i> .....      | 10          |
| • Added Figure 7, <i>Offset Voltage Long Term Drift</i> .....                 | 10          |
| • Changed Figure 50, <i>OPA388 Layout Example</i> ; updated for accuracy..... | 26          |

| <b>Changes from Revision * (December 2016) to Revision A (July 2018)</b>   | <b>Page</b> |
|--|-------------|
| • Changed device status from Production Data to Production Data/Mixed Status.....  | 1           |
| • Added top navigator link for TI reference design.....  | 1           |
| • Added preview notes to 5-pin SOT-23 (OPA388), 8-pin SOIC (OPA2388), 14-pin SOIC, and 14-pin TSSOP (OPA4388) packages in <i>Device Information</i> table..... | 1           |
| • Added package preview notes to <i>Pin Configuration and Functions</i> section.....   | 4           |
| • AOL test condition changed to 0.15 V from 0.1 V.....   | 7           |
| • AOL test condition changed to 0.15 V from 0.1 V.....   | 7           |
| • AOL test condition changed to 0.25 V from 0.2 V.....   | 7           |
| • AOL test condition changed to 0.3 V from 0.25 V.....   | 7           |

## 5 Pin Configuration and Functions



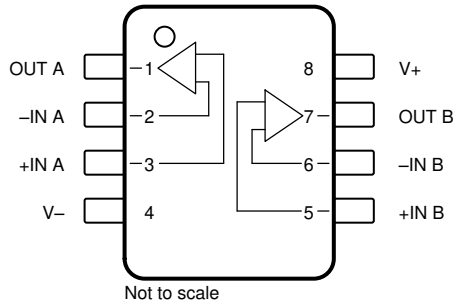
**Figure 5-1. OPA388 DBV Package, 5-Pin SOT-23, Top View**



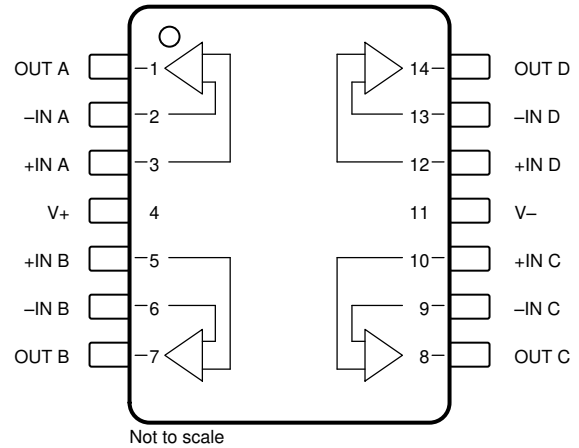
**Figure 5-2. OPA388 D and DGK Packages, 8-Pin SOIC and VSSOP, Top View**

### Pin Functions: OPA388

| NAME | PIN                      |              | I/O | DESCRIPTION                                   |
|------|--------------------------|--------------|-----|---|
|      | OPA388                   |              |     |   |
|      | D (SOIC),<br>DGK (VSSOP) | DBV (SOT-23) |     |   |
| -IN  | 2                        | 4            | I   | Inverting input                               |
| +IN  | 3                        | 3            | I   | Noninverting input                            |
| NC   | 1, 5, 8                  | —            | —   | No internal connection (can be left floating) |
| OUT  | 6                        | 1            | O   | Output  |
| V-   | 4                        | 2            | —   | Negative (lowest) power supply                |
| V+   | 7                        | 5            | —   | Positive (highest) power supply               |



**Figure 5-3. OPA2388 8-Pin SOIC (D) Package and 8-Pin VSSOP (DGK) Package, Top View**



**Figure 5-4. OPA4388 14-Pin SOIC (D) and TSSOP-14 (PW) Packages, Top View**

**Pin Functions: OPA2388 and OPA4388**

| NAME  | PIN                                 |                                    | I/O | DESCRIPTION                     |
|-------|-------------------------------------|------------------------------------|-----|---------------------------------|
|       | OPA2388<br>D (SOIC),<br>DGK (VSSOP) | OPA4388<br>D (SOIC),<br>PW (TSSOP) |     |                                 |
| -IN A | 2                                   | 2                                  | I   | Inverting input, channel A      |
| -IN B | 6                                   | 6                                  | I   | Inverting input, channel B      |
| -IN C | —                                   | 9                                  | I   | Inverting input, channel C      |
| -IN D | —                                   | 13                                 | I   | Inverting input, channel D      |
| +IN A | 3                                   | 3                                  | I   | Noninverting input, channel A   |
| +IN B | 5                                   | 5                                  | I   | Noninverting input, channel B   |
| +IN C | —                                   | 10                                 | I   | Noninverting input, channel C   |
| +IN D | —                                   | 12                                 | I   | Noninverting input, channel D   |
| OUT A | 1                                   | 1                                  | O   | Output, channel A               |
| OUT B | 7                                   | 7                                  | O   | Output, channel B               |
| OUT C | —                                   | 8                                  | O   | Output, channel C               |
| OUT D | —                                   | 14                                 | O   | Output, channel D               |
| V-    | 4                                   | 11                                 | —   | Negative (lowest) power supply  |
| V+    | 8                                   | 4                                  | —   | Positive (highest) power supply |

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                                     |                     |               | MIN               | MAX        | UNIT |
|-------------------------------------|---------------------|---------------|-------------------|------------|------|
| Supply voltage                      | $V_S = (V+) - (V-)$ | Single-supply |                   | 6          | V    |
|                                     |                     | Dual-supply   |                   | ±3         |      |
| Signal input pins                   | Voltage             | Common-mode   | (V-) – 0.5        | (V+) + 0.5 | V    |
|                                     |                     | Differential  | (V+) – (V-) + 0.2 |            |      |
|                                     | Current             |               |                   | ±10        | mA   |
| Output short circuit <sup>(2)</sup> |                     |               | Continuous        | Continuous |      |
| Temperature                         | Operating, $T_A$    |               | –55               | 150        | °C   |
|                                     | Junction, $T_J$     |               |                   | 150        |      |
|                                     | Storage, $T_{stg}$  |               | –65               | 150        |      |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Short-circuit to ground, one amplifier per package.

### 6.2 ESD Ratings

|             |                         |  | VALUE | UNIT |
|-------------|-------------------------|--|-------|------|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>              | ±4000 | V    |
|             |                         | Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup> | ±1000 |      |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|                                     |               | MIN   | NOM | MAX   | UNIT |
|-------------------------------------|---------------|-------|-----|-------|------|
| Supply voltage, $V_S = (V+) - (V-)$ | Single-supply | 2.5   |     | 5.5   | V    |
|                                     | Dual-supply   | ±1.25 |     | ±2.75 |      |
| Specified temperature               |               | –40   |     | 125   | °C   |

### 6.4 Thermal Information: OPA388

| THERMAL METRIC <sup>(1)</sup> |  | OPA388   |              |             | UNIT |
|-------------------------------|--|----------|--------------|-------------|------|
|                               |  | D (SOIC) | DBV (SOT-23) | DGK (VSSOP) |      |
|                               |  | 8 PINS   | 5 PINS       | 5 PINS      |      |
| $R_{\theta JA}$               | Junction-to-ambient thermal resistance       | 116      | 145.7        | 177         | °C/W |
| $R_{\theta JC(top)}$          | Junction-to-case (top) thermal resistance    | 60       | 94.8         | 69          | °C/W |
| $R_{\theta JB}$               | Junction-to-board thermal resistance         | 56       | 43.4         | 100         | °C/W |
| $\Psi_{JT}$                   | Junction-to-top characterization parameter   | 12.8     | 24.7         | 9.9         | °C/W |
| $\Psi_{JB}$                   | Junction-to-board characterization parameter | 55.9     | 43.1         | 98.3        | °C/W |
| $R_{\theta JC(bot)}$          | Junction-to-case (bottom) thermal resistance | N/A      | N/A          | n/a         | °C/W |

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics application report](#).

### 6.5 Thermal Information: OPA2388

| THERMAL METRIC <sup>(1)</sup> |  | OPA2388  |             | UNIT |
|-------------------------------|--|----------|-------------|------|
|                               |  | D (SOIC) | DGK (VSSOP) |      |
|                               |  | 8 PINS   | 8 PINS      |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 120.0    | 165         | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance    | 52.3     | 53          | °C/W |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 65.6     | 87          | °C/W |
| Ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 9.6      | 4.9         | °C/W |
| Ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 64.4     | 85          | °C/W |
| R <sub>θJC(bot)</sub>         | Junction-to-case (bottom) thermal resistance | N/A      | N/A         | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics application report](#).

### 6.6 Thermal Information: OPA4388

| THERMAL METRIC <sup>(1)</sup> |  | OPA4388  |            | UNIT |
|-------------------------------|--|----------|------------|------|
|                               |  | D (SOIC) | PW (TSSOP) |      |
|                               |  | 14 PINS  | 14 PINS    |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 86.4     | 109.6      | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance    | 46.3     | 27.4       | °C/W |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 41.0     | 56.1       | °C/W |
| Ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 11.3     | 1.5        | °C/W |
| Ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 40.7     | 54.9       | °C/W |
| R <sub>θJC(bot)</sub>         | Junction-to-case (bottom) thermal resistance | N/A      | N/A        | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics application report](#).

### 6.7 Electrical Characteristics: VS = ±1.25 V to ±2.75 V (VS = 2.5 to 5.5 V)

at T<sub>A</sub> = 25°C, V<sub>CM</sub> = V<sub>OUT</sub> = V<sub>S</sub> / 2, and R<sub>LOAD</sub> = 10 kΩ connected to V<sub>S</sub> / 2 (unless otherwise noted)

| PARAMETER             |                              | TEST CONDITIONS  | MIN             | TYP    | MAX   | UNIT  |       |
|-----------------------|------------------------------|--|-----------------|--------|-------|-------|-------|
| <b>OFFSET VOLTAGE</b> |                              |  |                 |        |       |       |       |
| V <sub>OS</sub>       | Input offset voltage         | OPA388, OPA2388  |                 | ±0.25  | ±5    | μV    |       |
|                       |                              | V <sub>S</sub> = 5.5 V                                   | OPA4388         |        | ±2.25 |       | ±8    |
|                       |                              | T <sub>A</sub> = -40°C to +125°C                         | OPA388, OPA2388 |        |       |       | ±7.5  |
|                       |                              | T <sub>A</sub> = -40°C to +125°C, V <sub>S</sub> = 5.5 V | OPA4388         |        |       |       | ±10.5 |
| dV <sub>OS</sub> /dT  | Input offset voltage drift   | T <sub>A</sub> = -40°C to +125°C                         | OPA388, OPA2388 | ±0.005 | ±0.05 | μV/°C |       |
|                       |                              | T <sub>A</sub> = -40°C to +125°C, V <sub>S</sub> = 5.5 V | OPA4388         | ±0.005 | ±0.05 |       |       |
| PSRR                  | Power-supply rejection ratio | T <sub>A</sub> = -40°C to +125°C                         | OPA388, OPA2388 | ±0.1   | ±1    | μV/V  |       |
|                       |                              |  | OPA4388         | ±1.25  | ±3.5  |       |       |

### 6.7 Electrical Characteristics: VS = ±1.25 V to ±2.75 V (VS = 2.5 to 5.5 V) (continued)

at TA = 25°C, VCM = VOUT = VS / 2, and RLOAD = 10 kΩ connected to VS / 2 (unless otherwise noted)

| PARAMETER   |                              | TEST CONDITIONS                                    |                                 | MIN        | TYP       | MAX        | UNIT     |
|---|------------------------------|--|---------------------------------|------------|-----------|------------|----------|
| <b>INPUT BIAS CURRENT</b>                                   |                              |  |                                 |            |           |            |          |
| IB  | Input bias current           | RIN = 100 kΩ, OPA388, OPA2388                      | TA = 0°C to +85°C               |            | ±30       | ±350       | pA       |
|   |                              |  | TA = -40°C to +125°C            |            |           | ±400       |          |
|   |                              |  | TA = -40°C to +125°C            |            |           | ±700       |          |
|   |                              | RIN = 100 kΩ, OPA4388                              | TA = 0°C to +85°C               |            | ±30       | ±500       |          |
|   |                              |  | TA = -40°C to +125°C            |            |           | ±600       |          |
|   |                              |  | TA = -40°C to +125°C            |            |           | ±800       |          |
| IOS   | Input offset current         | RIN = 100 kΩ, OPA388, OPA2388                      | TA = 0°C to +85°C               |            |           | ±700       |          |
|   |                              |  | TA = -40°C to +125°C            |            |           | ±800       |          |
|   |                              |  | TA = -40°C to +125°C            |            |           | ±800       |          |
|   |                              | RIN = 100 kΩ, OPA4388                              | TA = 0°C to +85°C               |            |           | ±1000      |          |
|   |                              |  | TA = -40°C to +125°C            |            |           | ±1100      |          |
|   |                              |  | TA = -40°C to +125°C            |            |           | ±1100      |          |
| <b>NOISE</b>  |                              |  |                                 |            |           |            |          |
| EN  | Input voltage noise          | f = 0.1 Hz to 10 Hz                                |                                 |            | 0.14      |            | μVPP     |
| eN  | Input voltage noise density  | f = 10 Hz  |                                 |            | 7         |            | nV/√Hz   |
|   |                              | f = 100 Hz   |                                 |            | 7         |            |          |
|   |                              | f = 1 kHz  |                                 |            | 7         |            |          |
|   |                              | f = 10 kHz   |                                 |            | 7         |            |          |
| IN  | Input current noise density  | f = 1 kHz  |                                 |            | 100       |            | fA/√Hz   |
| <b>INPUT VOLTAGE</b>  |                              |  |                                 |            |           |            |          |
| VCM   | Common-mode voltage range    |  |                                 | (V-) - 0.1 |           | (V+) + 0.1 | V        |
| CMRR  | Common-mode rejection ratio  | (V-) - 0.1 V < VCM < (V+) + 0.1 V                  | VS = ±1.25 V<br>OPA388, OPA2388 | 124        | 138       |            | dB       |
|   |                              |  | VS = ±1.25 V<br>OPA4388         | 102        | 110       |            |          |
|   |                              |  | VS = ±2.75 V                    | 124        | 140       |            |          |
|   |                              | (V-) < VCM < (V+) + 0.1 V,<br>TA = -40°C to +125°C | VS = ±1.25 V<br>OPA388, OPA2388 | 114        | 134       |            |          |
|   |                              |  | VS = ±1.25 V<br>OPA4388         | 102        | 107       |            |          |
|   |                              |  | VS = ±2.75 V                    | 124        | 140       |            |          |
| (V-) - 0.05 V < VCM < (V+) + 0.1 V,<br>TA = -40°C to +125°C | VS = ±1.25 V                 |  |                                 |            |           |            |          |
|   | VS = ±2.75 V                 |  |                                 |            |           |            |          |
| <b>INPUT IMPEDANCE</b>                                      |                              |  |                                 |            |           |            |          |
| Zid   | Differential input impedance |  |                                 |            | 100    2  |            | MΩ    pF |
| Zic   | Common-mode input impedance  |  |                                 |            | 60    4.5 |            | TΩ    pF |

## 6.7 Electrical Characteristics: $V_S = \pm 1.25\text{ V}$ to $\pm 2.75\text{ V}$ ( $V_S = 2.5$ to $5.5\text{ V}$ ) (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_{CM} = V_{OUT} = V_S / 2$ , and  $R_{LOAD} = 10\text{ k}\Omega$  connected to  $V_S / 2$  (unless otherwise noted)

| PARAMETER  |                                   | TEST CONDITIONS   |  | MIN             | TYP      | MAX | UNIT             |  |
|--|-----------------------------------|---|--|-----------------|----------|-----|------------------|--|
| <b>OPEN-LOOP GAIN</b>  |                                   |   |  |                 |          |     |                  |  |
| $A_{OL}$   | Open-loop voltage gain            | $(V^-) + 0.15\text{ V} < V_O < (V^+) - 0.15\text{ V}$ , $R_{LOAD} = 10\text{ k}\Omega$  |  | 126             | 148      |     | dB               |  |
|  |                                   | $(V^-) + 0.15\text{ V} < V_O < (V^+) - 0.15\text{ V}$ , $R_{LOAD} = 10\text{ k}\Omega$ , $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$                        |  | OPA388, OPA2388 | 120      | 126 |                  |  |
|  |                                   | $(V^-) + 0.15\text{ V} < V_O < (V^+) - 0.15\text{ V}$ , $R_{LOAD} = 10\text{ k}\Omega$ , $V_S = 5.5\text{ V}$ , $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ |  | OPA4388         | 120      | 126 |                  |  |
|  |                                   | $(V^-) + 0.25\text{ V} < V_O < (V^+) - 0.25\text{ V}$ , $R_{LOAD} = 2\text{ k}\Omega$   |  |                 | 126      | 148 |                  |  |
|  |                                   | $(V^-) + 0.30\text{ V} < V_O < (V^+) - 0.30\text{ V}$ , $R_{LOAD} = 2\text{ k}\Omega$   |  | OPA388, OPA2388 | 120      | 148 |                  |  |
|  |                                   | $(V^-) + 0.30\text{ V} < V_O < (V^+) - 0.30\text{ V}$ , $R_{LOAD} = 2\text{ k}\Omega$ , $V_S = 5.5\text{ V}$ , $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$  |  | OPA4388         | 120      | 126 |                  |  |
| <b>FREQUENCY RESPONSE</b>  |                                   |   |  |                 |          |     |                  |  |
| GBW  | Unity-gain bandwidth              |   |  |                 | 10       |     | MHz              |  |
| SR   | Slew rate                         | $G = 1$ , 4-V step  |  |                 | 5        |     | V/ $\mu\text{s}$ |  |
| THD+N  | Total harmonic distortion + noise | $G = 1$ , $f = 1\text{ kHz}$ , $V_O = 1\text{ V}_{RMS}$   |  |                 | 0.0005%  |     |                  |  |
| $t_S$  | Settling time                     | To 0.1%   | $V_S = \pm 2.5\text{ V}$ , $G = 1$ , 1-V step                          |                 | 0.75     |     | $\mu\text{s}$    |  |
|  |                                   | To 0.01%  | $V_S = \pm 2.5\text{ V}$ , $G = 1$ , 1-V step                          |                 | 2        |     | $\mu\text{s}$    |  |
| $t_{OR}$   | Overload recovery time            | $V_{IN} \times G = V_S$   |  |                 | 10       |     | $\mu\text{s}$    |  |
| <b>OUTPUT</b>  |                                   |   |  |                 |          |     |                  |  |
| $V_O$  | Voltage output swing from rail    | Positive rail   | No load  |                 | 1        | 15  | mV               |  |
|  |                                   |   | $R_{LOAD} = 10\text{ k}\Omega$   |                 | 5        | 20  |                  |  |
|  |                                   |   | $R_{LOAD} = 2\text{ k}\Omega$  |                 | 20       | 50  |                  |  |
|  |                                   | Negative rail   | No load  |                 | 5        | 15  |                  |  |
|  |                                   |   | $R_{LOAD} = 10\text{ k}\Omega$   |                 | 10       | 20  |                  |  |
|  |                                   |   | $R_{LOAD} = 2\text{ k}\Omega$  |                 | 40       | 60  |                  |  |
| $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ , both rails, $R_{LOAD} = 10\text{ k}\Omega$ |                                   |   | 10   | 25              |          |     |                  |  |
| $I_{SC}$   | Short-circuit current             | $V_S = 5.5\text{ V}$  |  |                 | $\pm 60$ |     | mA               |  |
|  |                                   | $V_S = 2.5\text{ V}$  |  |                 | $\pm 30$ |     | mA               |  |
| $C_{LOAD}$   | Capacitive load drive             | See <a href="#">Figure 6-26</a>   |  |                 |          |     |                  |  |
| $Z_O$  | Open-loop output impedance        | $f = 1\text{ MHz}$ , $I_O = 0\text{ A}$ , see <a href="#">Figure 6-25</a>   |  |                 | 100      |     | $\Omega$         |  |
| <b>POWER SUPPLY</b>  |                                   |   |  |                 |          |     |                  |  |
| $I_Q$  | Quiescent current per amplifier   | $V_S = \pm 1.25\text{ V}$ ( $V_S = 2.5\text{ V}$ )  | $I_O = 0\text{ A}$   |                 | 1.7      | 2.4 | mA               |  |
|  |                                   |   | $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ , $I_O = 0\text{ A}$ |                 | 1.7      | 2.4 |                  |  |
|  |                                   | $V_S = \pm 2.75\text{ V}$ ( $V_S = 5.5\text{ V}$ )  | $I_O = 0\text{ A}$   |                 | 1.9      | 2.6 |                  |  |
|  |                                   |   | $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ , $I_O = 0\text{ A}$ |                 | 1.9      | 2.6 |                  |  |

## 6.8 Typical Characteristics

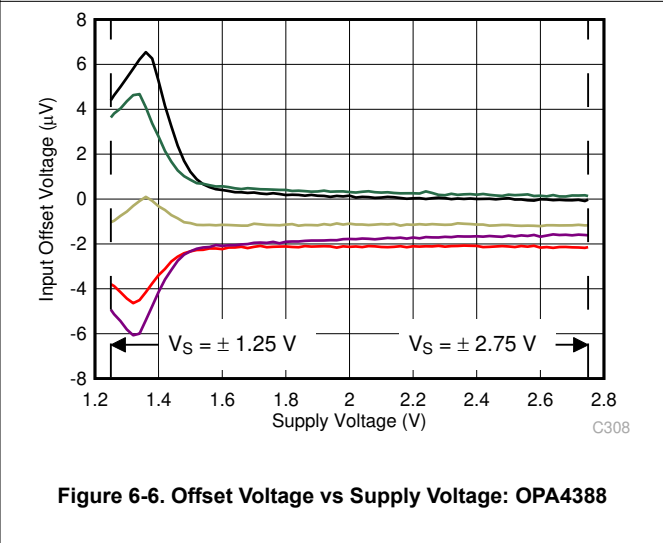
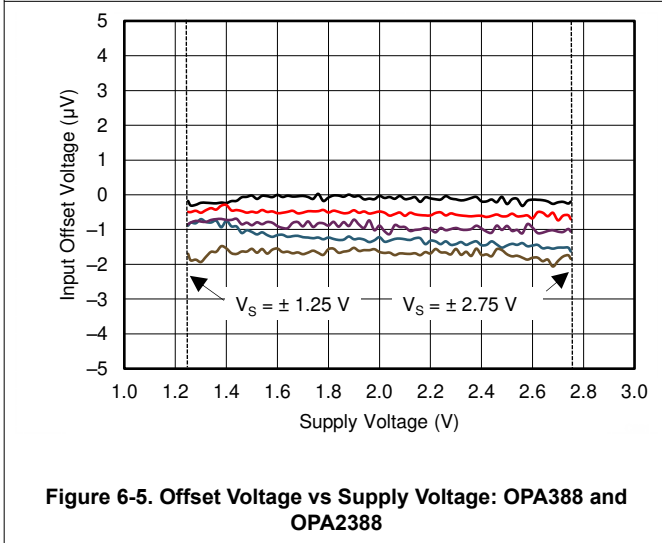
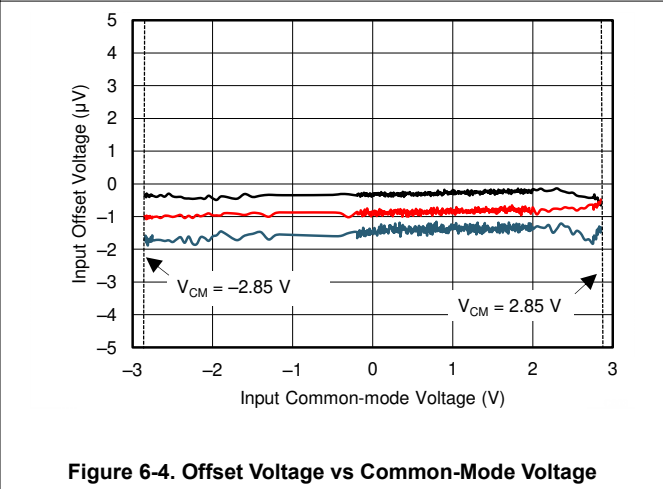
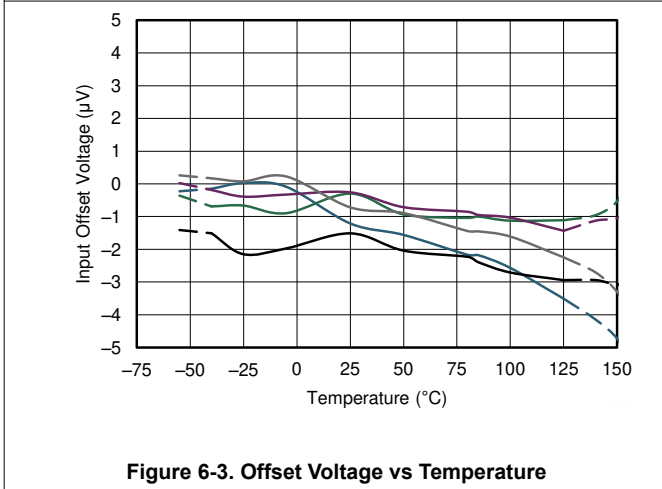
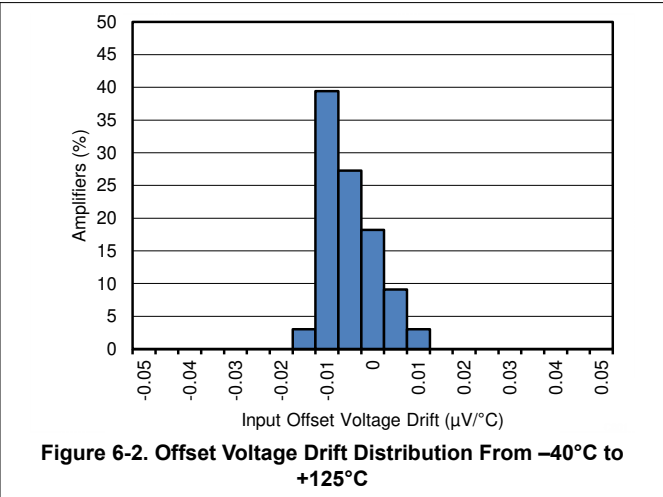
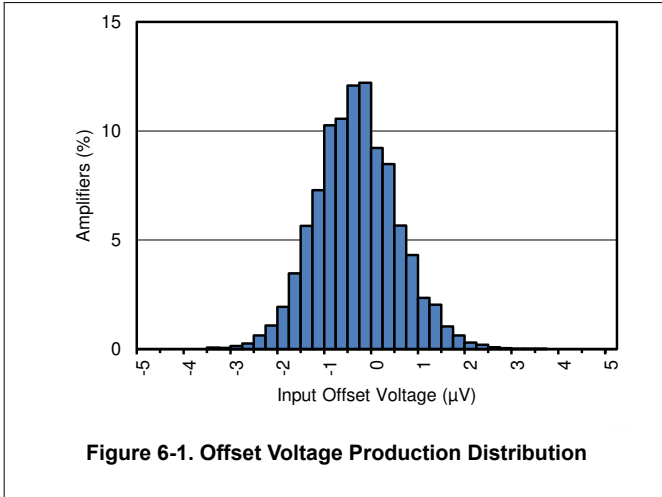
at  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 2.5\text{ V}$ ,  $V_{CM} = V_S / 2$ ,  $R_{LOAD} = 10\text{ k}\Omega$  connected to  $V_S / 2$ , and  $C_L = 100\text{ pF}$  (unless otherwise noted)

**Table 6-1. Table of Graphs**

| DESCRIPTION  | FIGURE  |
|--|---|
| Offset Voltage Production Distribution   | <a href="#">Figure 6-1</a>                                |
| Offset Voltage Drift Distribution From $-40^\circ\text{C}$ to $+125^\circ\text{C}$ | <a href="#">Figure 6-2</a>                                |
| Offset Voltage vs Temperature  | <a href="#">Figure 6-3</a>                                |
| Offset Voltage vs Common-Mode Voltage  | <a href="#">Figure 6-4</a>                                |
| Offset Voltage vs Power Supply: OPA388 and OPA2388                                 | <a href="#">Figure 6-5</a>                                |
| Offset Voltage vs Power Supply: OPA4388  | <a href="#">Figure 6-6</a>                                |
| Offset Voltage Long Term Drift   | <a href="#">Figure 6-7</a>                                |
| Open-Loop Gain and Phase vs Frequency  | <a href="#">Figure 6-8</a>                                |
| Closed-Loop Gain and Phase vs Frequency  | <a href="#">Figure 6-9</a>                                |
| Input Bias Current vs Common-Mode Voltage  | <a href="#">Figure 6-10</a>                               |
| Input Bias Current vs Temperature  | <a href="#">Figure 6-11</a>                               |
| Output Voltage Swing vs Output Current (Maximum Supply)                            | <a href="#">Figure 6-12</a>                               |
| CMRR and PSRR vs Frequency   | <a href="#">Figure 6-13</a>                               |
| CMRR vs Temperature  | <a href="#">Figure 6-14</a>                               |
| PSRR vs Temperature  | <a href="#">Figure 6-15</a>                               |
| 0.1-Hz to 10-Hz Noise  | <a href="#">Figure 6-16</a>                               |
| Input Voltage Noise Spectral Density vs Frequency                                  | <a href="#">Figure 6-17</a>                               |
| THD+N Ratio vs Frequency   | <a href="#">Figure 6-18</a>                               |
| THD+N vs Output Amplitude  | <a href="#">Figure 6-19</a>                               |
| Spectral Content   | <a href="#">Figure 6-20</a> , <a href="#">Figure 6-21</a> |
| Quiescent Current vs Supply Voltage  | <a href="#">Figure 6-22</a>                               |
| Quiescent Current vs Temperature   | <a href="#">Figure 6-23</a>                               |
| Open-Loop Gain vs Temperature  | <a href="#">Figure 6-24</a>                               |
| Open-Loop Output Impedance vs Frequency  | <a href="#">Figure 6-25</a>                               |
| Small-Signal Overshoot vs Capacitive Load (10-mV Step)                             | <a href="#">Figure 6-26</a>                               |
| No Phase Reversal  | <a href="#">Figure 6-27</a>                               |
| Positive Overload Recovery   | <a href="#">Figure 6-28</a>                               |
| Negative Overload Recovery   | <a href="#">Figure 6-29</a>                               |
| Small-Signal Step Response (10-mV Step)  | <a href="#">Figure 6-30</a> , <a href="#">Figure 6-31</a> |
| Large-Signal Step Response (4-V Step)  | <a href="#">Figure 6-32</a> , <a href="#">Figure 6-33</a> |
| Settling Time  | <a href="#">Figure 6-34</a> , <a href="#">Figure 6-35</a> |
| Short-Circuit Current vs Temperature   | <a href="#">Figure 6-36</a>                               |
| Maximum Output Voltage vs Frequency  | <a href="#">Figure 6-37</a>                               |
| EMIRR vs Frequency   | <a href="#">Figure 6-38</a>                               |

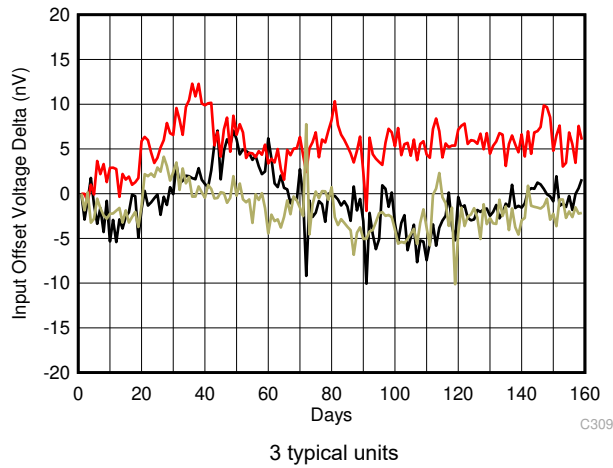
### 6.8 Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 2.5\text{ V}$ ,  $V_{CM} = V_S / 2$ ,  $R_{LOAD} = 10\text{ k}\Omega$  connected to  $V_S / 2$ , and  $C_L = 100\text{ pF}$  (unless otherwise noted)

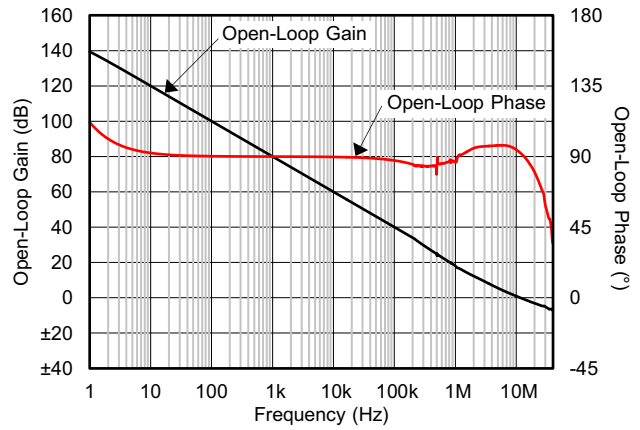


### 6.8 Typical Characteristics (continued)

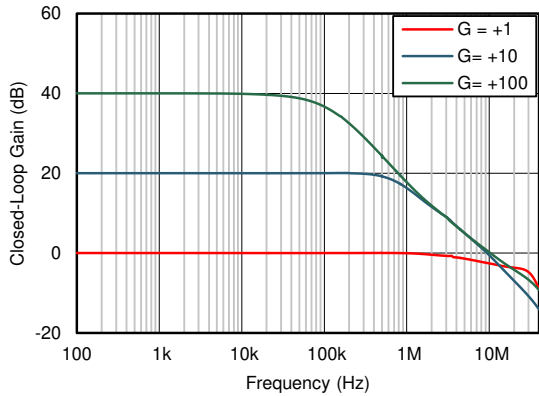
at  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 2.5\text{ V}$ ,  $V_{CM} = V_S / 2$ ,  $R_{LOAD} = 10\text{ k}\Omega$  connected to  $V_S / 2$ , and  $C_L = 100\text{ pF}$  (unless otherwise noted)



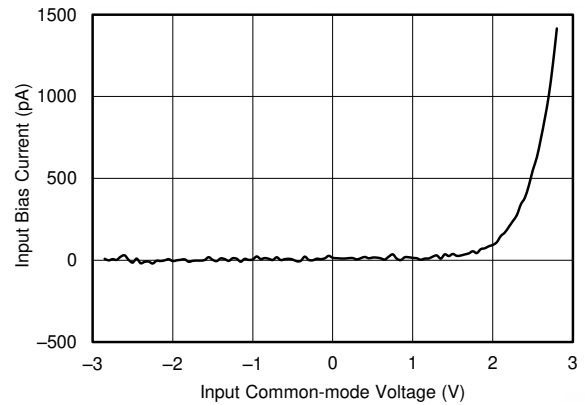
**Figure 6-7. Offset Voltage Long Term Drift**



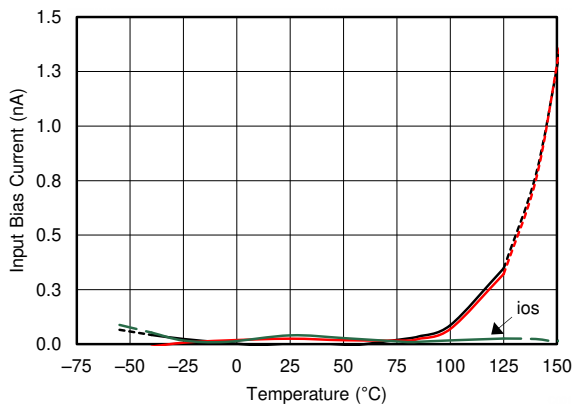
**Figure 6-8. Open-Loop Gain and Phase vs Frequency**



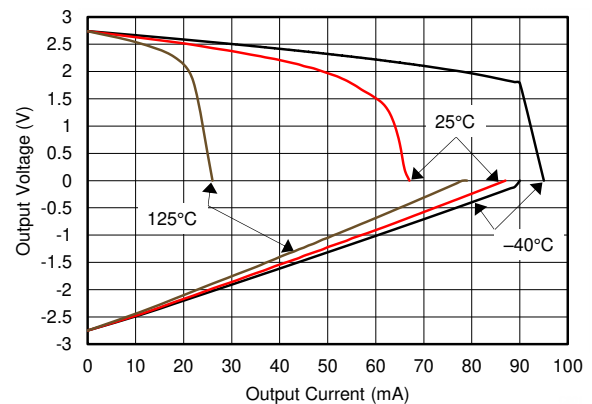
**Figure 6-9. Closed-Loop Gain and Phase vs Frequency**



**Figure 6-10. Input Bias Current vs Common-Mode Voltage**



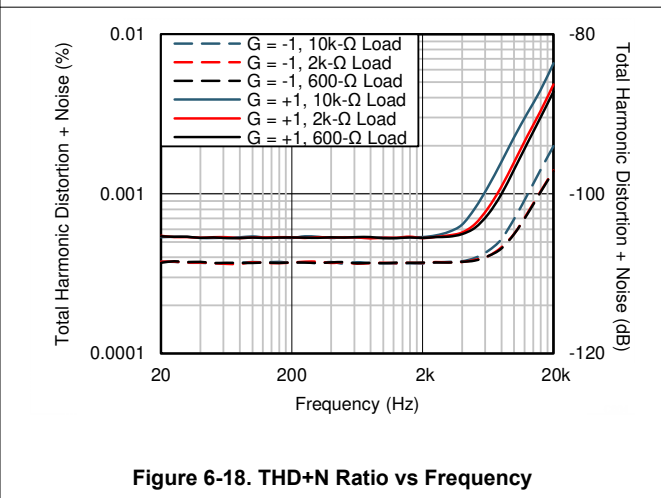
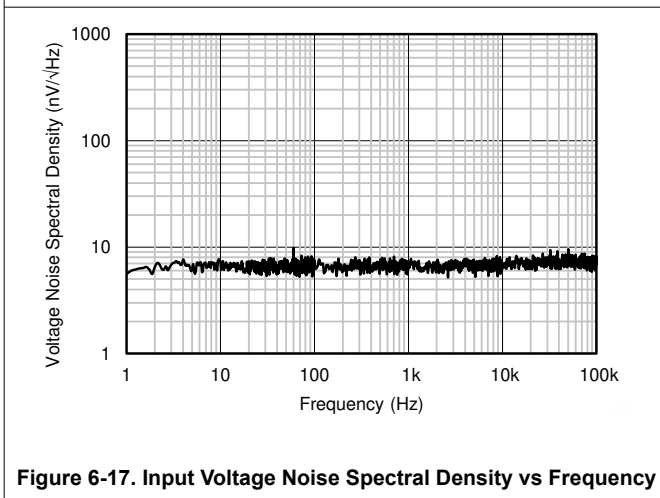
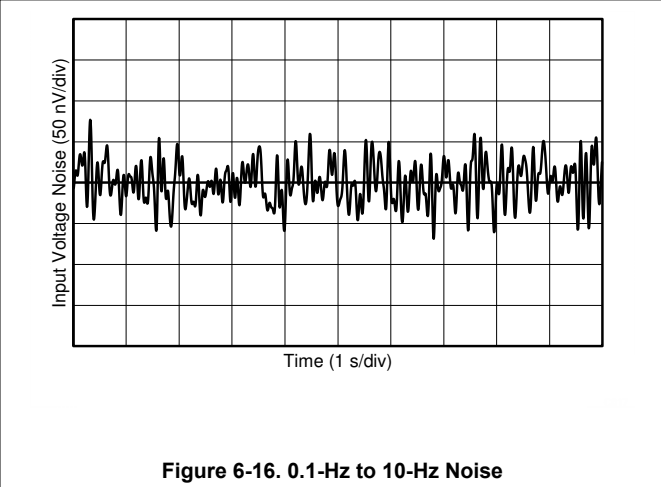
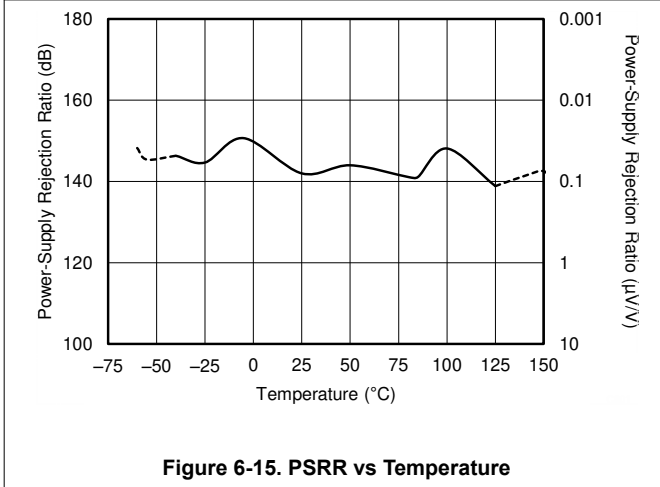
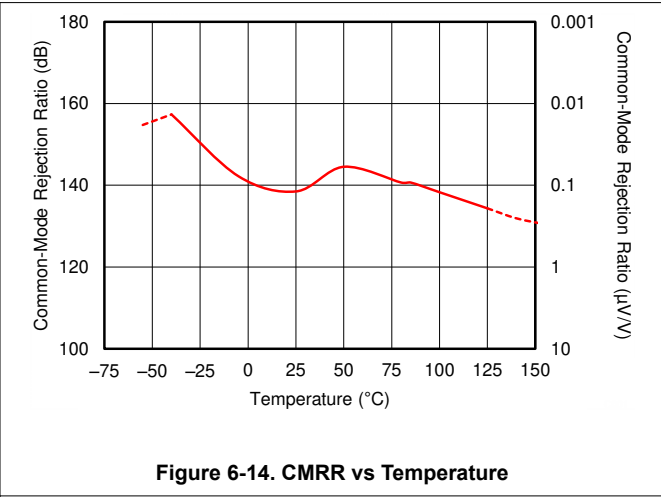
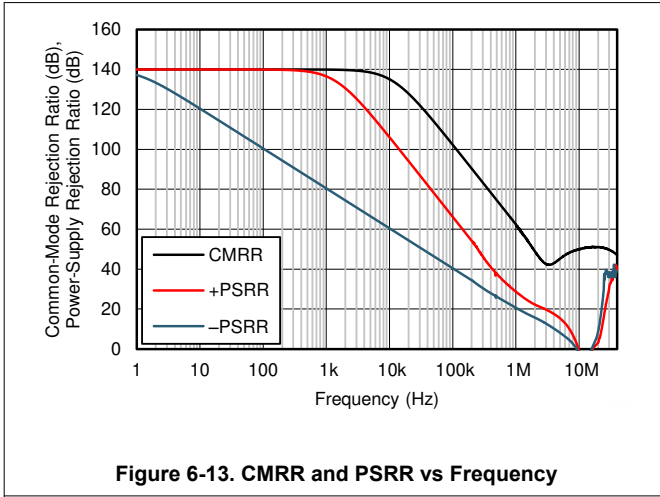
**Figure 6-11. Input Bias Current vs Temperature**



**Figure 6-12. Output Voltage Swing vs Output Current (Maximum Supply)**

### 6.8 Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 2.5\text{ V}$ ,  $V_{CM} = V_S / 2$ ,  $R_{LOAD} = 10\text{ k}\Omega$  connected to  $V_S / 2$ , and  $C_L = 100\text{ pF}$  (unless otherwise noted)



### 6.8 Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 2.5\text{ V}$ ,  $V_{CM} = V_S / 2$ ,  $R_{LOAD} = 10\text{ k}\Omega$  connected to  $V_S / 2$ , and  $C_L = 100\text{ pF}$  (unless otherwise noted)

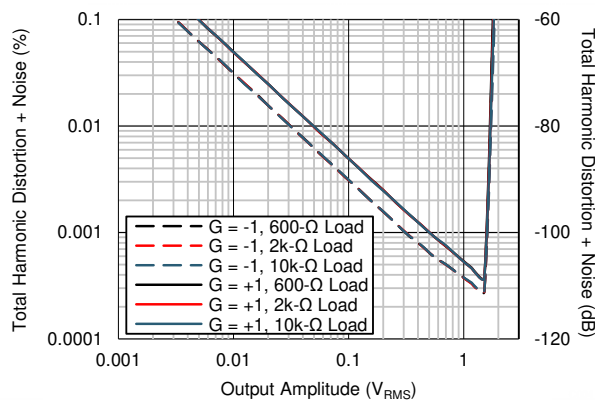
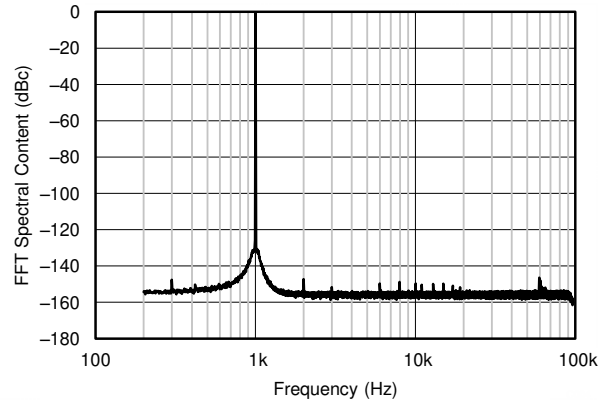
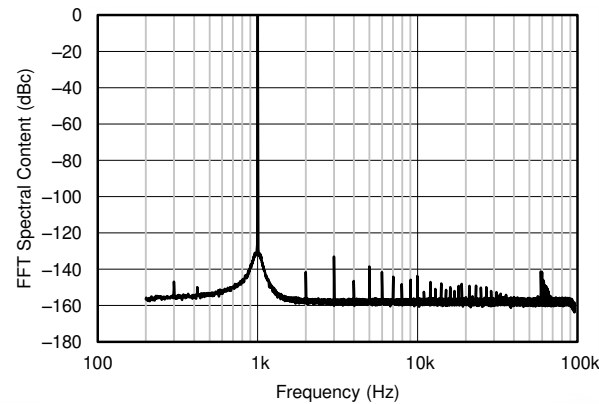


Figure 6-19. THD+N vs Output Amplitude



$G = +1$ ,  $f = 1\text{ kHz}$ ,  $V_O = 4.5\text{ V}_{PP}$ ,  $R_L = 10\text{ k}\Omega$ ,  $BW = 90\text{ kHz}$

Figure 6-20. Spectral Content (With 10-kΩ Load)



$G = +1$ ,  $f = 1\text{ kHz}$ ,  $V_O = 4.5\text{ V}_{PP}$ ,  $R_L = 2\text{ k}\Omega$ ,  $BW = 90\text{ kHz}$

Figure 6-21. Spectral Content (With 2-kΩ Load)

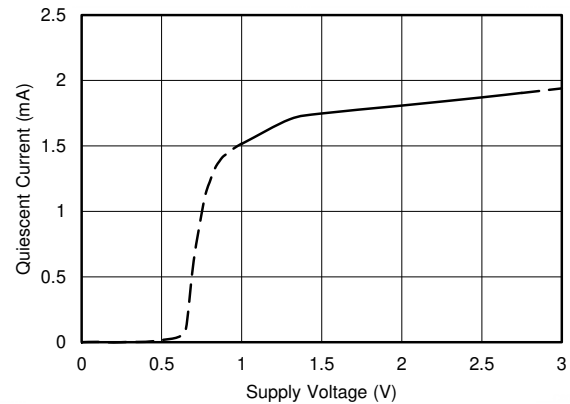


Figure 6-22. Quiescent Current vs Supply Voltage

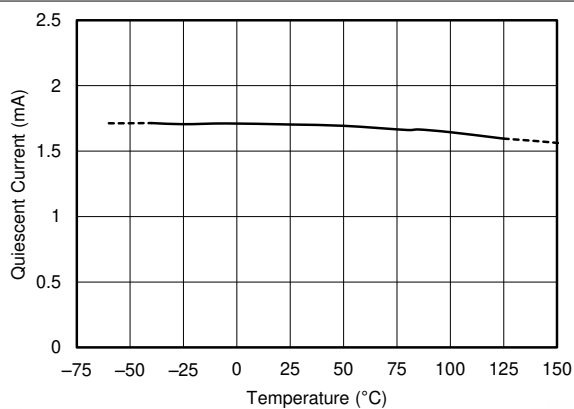


Figure 6-23. Quiescent Current vs Temperature

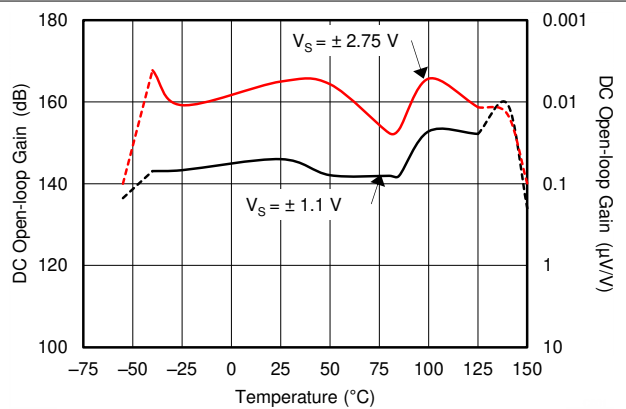


Figure 6-24. Open-Loop Gain vs Temperature

### 6.8 Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 2.5\text{ V}$ ,  $V_{CM} = V_S / 2$ ,  $R_{LOAD} = 10\text{ k}\Omega$  connected to  $V_S / 2$ , and  $C_L = 100\text{ pF}$  (unless otherwise noted)

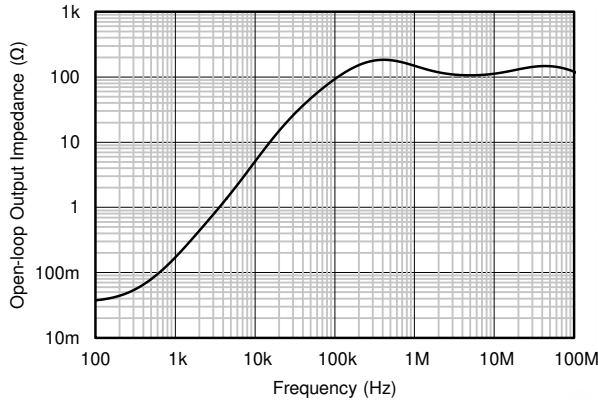


Figure 6-25. Open-Loop Output Impedance vs Frequency

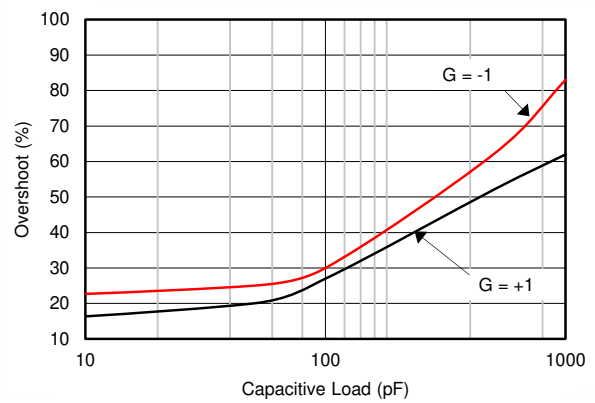


Figure 6-26. Small-Signal Overshoot vs Capacitive Load (10-mV Step)

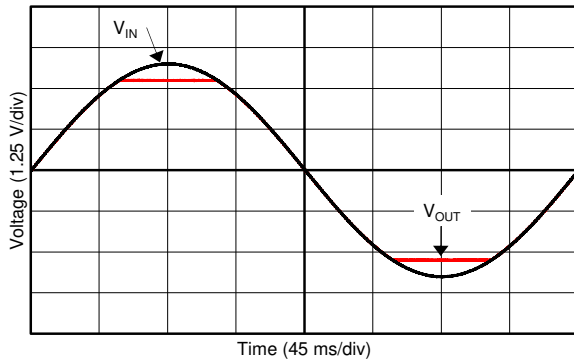


Figure 6-27. No Phase Reversal

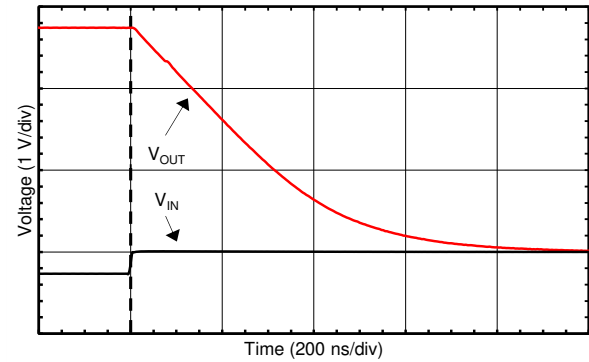


Figure 6-28. Positive Overload Recovery

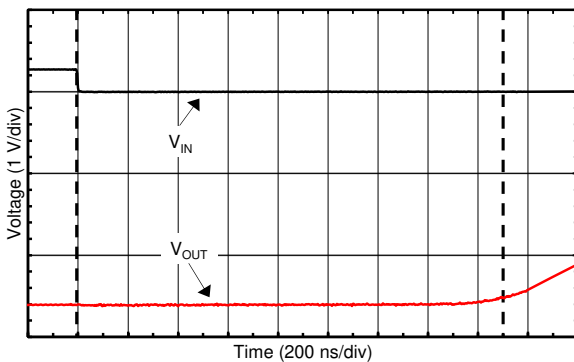
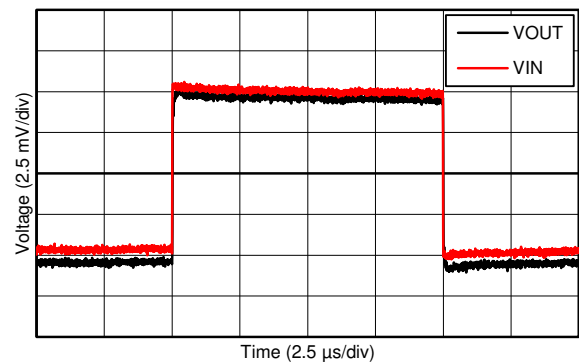


Figure 6-29. Negative Overload Recovery

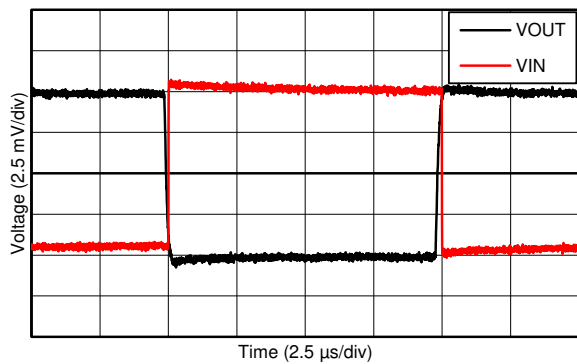


G = +1

Figure 6-30. Small-Signal Step Response (10-mV Step)

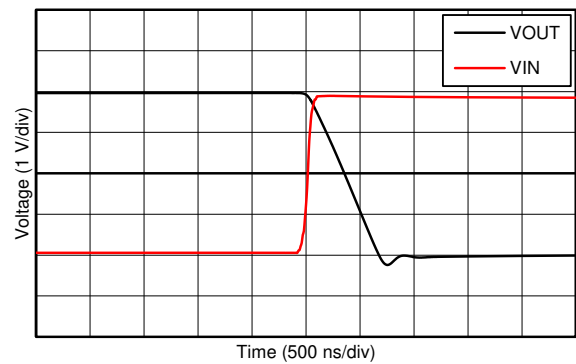
## 6.8 Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 2.5\text{ V}$ ,  $V_{CM} = V_S / 2$ ,  $R_{LOAD} = 10\text{ k}\Omega$  connected to  $V_S / 2$ , and  $C_L = 100\text{ pF}$  (unless otherwise noted)



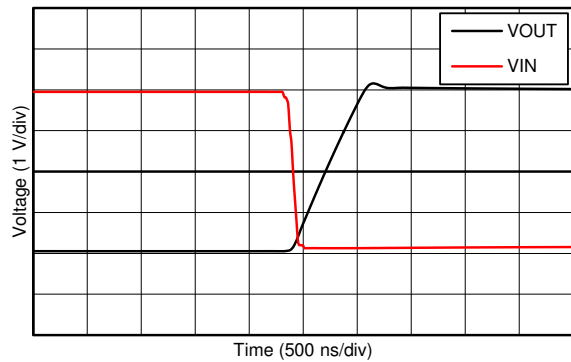
$G = -1$

Figure 6-31. Small-Signal Step Response (10-mV Step)



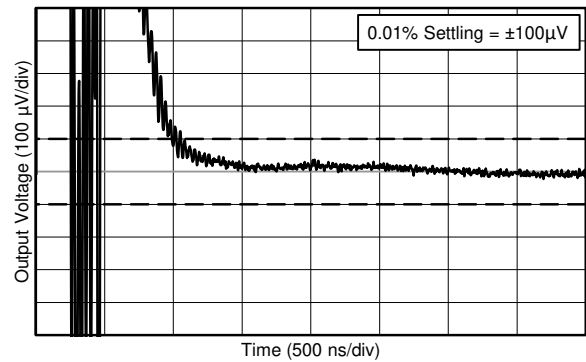
Falling output

Figure 6-32. Large-Signal Step Response (4-V Step)



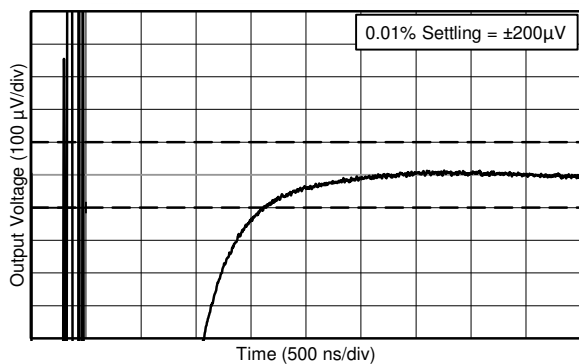
Rising output

Figure 6-33. Large-Signal Step Response (4-V Step)



0.01% settling =  $\pm 100\ \mu\text{V}$

Figure 6-34. Settling Time (1-V Positive Step)



0.01% settling =  $\pm 200\ \mu\text{V}$

Figure 6-35. Settling Time (1-V Negative Step)

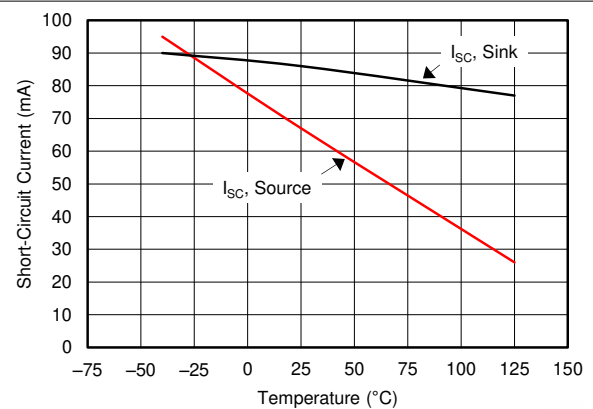
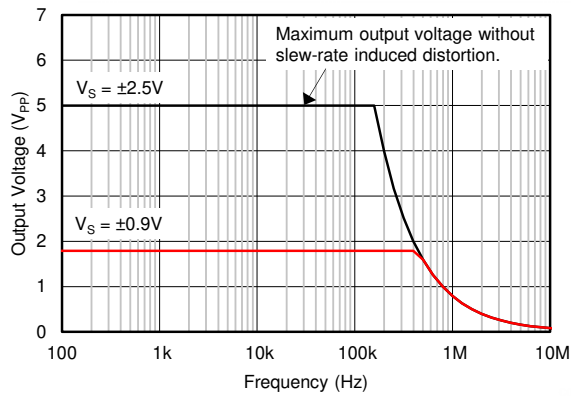


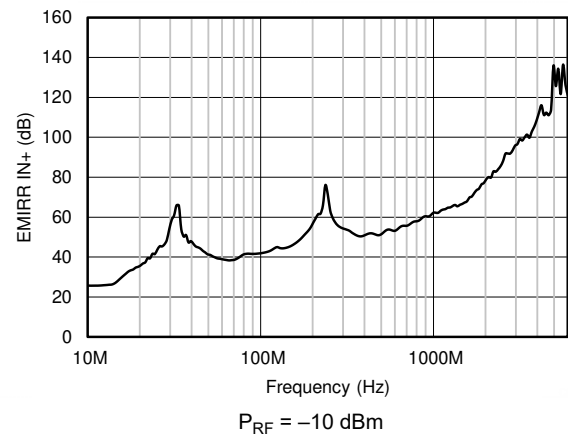
Figure 6-36. Short-Circuit Current vs Temperature

### 6.8 Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 2.5\text{ V}$ ,  $V_{CM} = V_S / 2$ ,  $R_{LOAD} = 10\text{ k}\Omega$  connected to  $V_S / 2$ , and  $C_L = 100\text{ pF}$  (unless otherwise noted)



**Figure 6-37. Maximum Output Voltage vs Frequency**



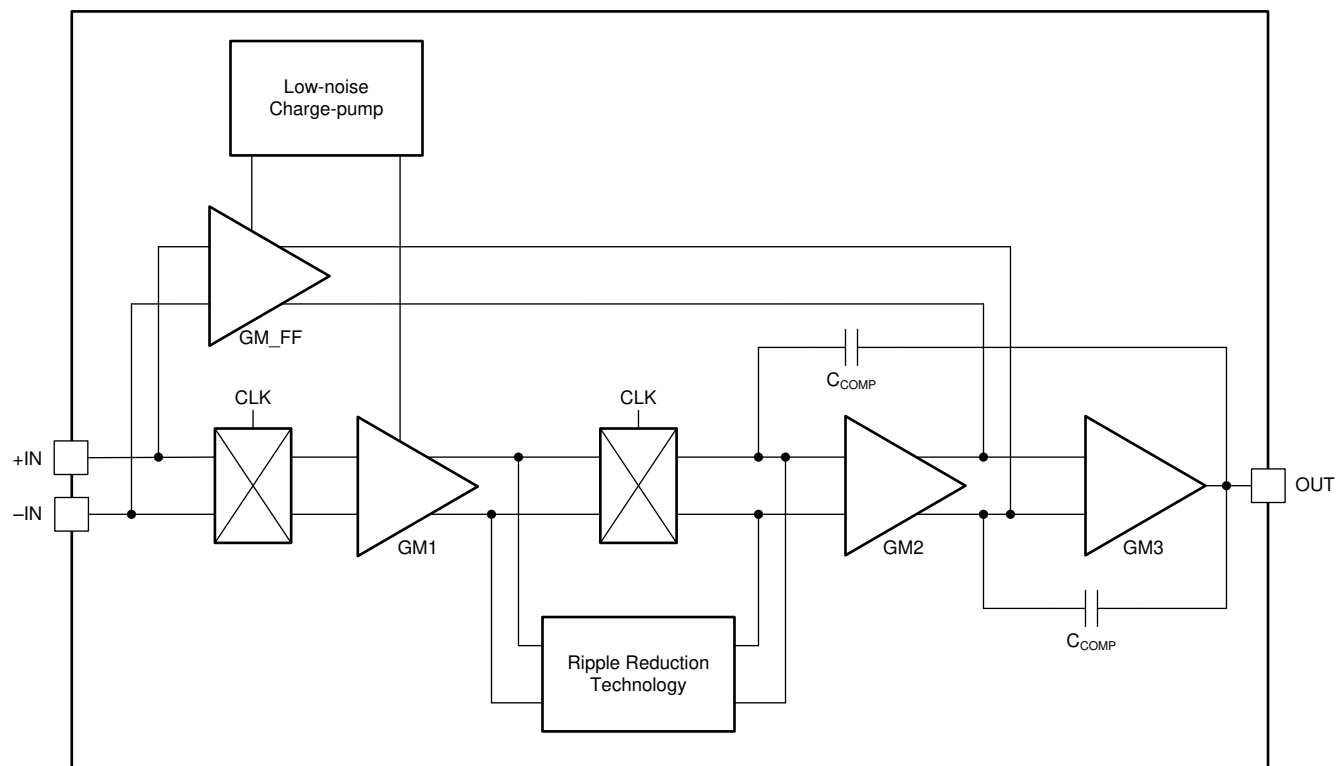
**Figure 6-38. EMIRR vs Frequency**

## 7 Detailed Description

### 7.1 Overview

The OPAx388 family of zero-drift amplifiers is engineered with the unique combination of a proprietary precision auto-calibration technique paired with a low-noise, low-ripple, input charge pump. These amplifiers offer ultra-low input offset voltage and drift and achieve excellent input and output dynamic linearity. The OPAx388 operate from 2.5 V to 5.5 V, is unity-gain stable, and are designed for a wide range of general-purpose and precision applications. The integrated, low-noise charge pump allows true rail-to-rail input common-mode operation without distortion associated with complementary rail-to-rail input topologies (input crossover distortion). The OPAx388 strengths also include 10-MHz bandwidth,  $7\text{-nV}/\sqrt{\text{Hz}}$  noise spectral density, and no  $1/f$  noise, making the OPAx388 optimal for interfacing with sensor modules and buffering high-fidelity, digital-to-analog converters (DACs).

### 7.2 Functional Block Diagram



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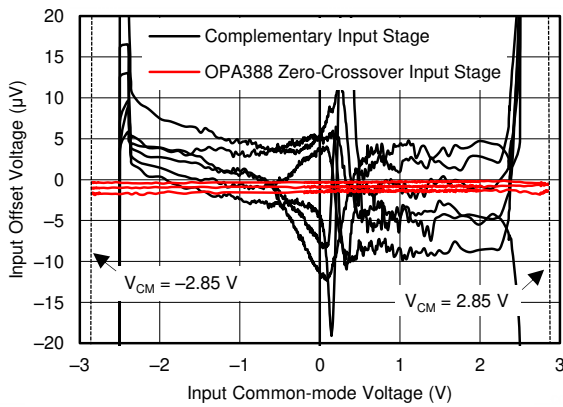
## 7.3 Feature Description

### 7.3.1 Operating Voltage

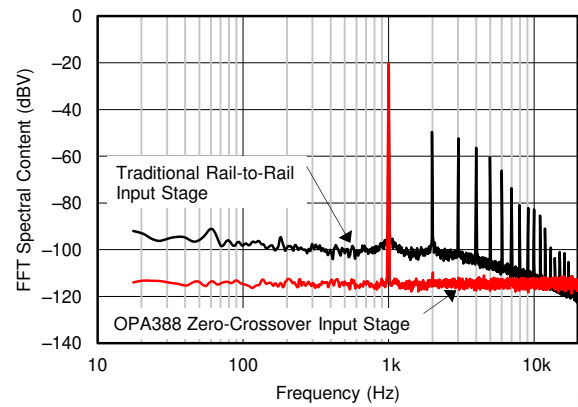
The OPAx388 family of operational amplifiers can be used with single or dual supplies from an operating range of  $V_S = 2.5\text{ V}$  ( $\pm 1.25\text{ V}$ ) up to  $5.5\text{ V}$  ( $\pm 2.75\text{ V}$ ). Supply voltages greater than  $7\text{ V}$  can permanently damage the device (see the *Absolute Maximum Ratings* table). Key parameters that vary over the supply voltage or temperature range are shown in the *Typical Characteristics* section.

### 7.3.2 Input Voltage and Zero-Crossover Functionality

The OPAx388 input common-mode voltage range extends  $0.1\text{ V}$  beyond the supply rails. This amplifier family is designed to cover the full range without the troublesome transition region found in some other rail-to-rail amplifiers. Operating a complementary rail-to-rail input amplifier with signals traversing the transition region results in unwanted non-linear behavior and polluted spectral content. [Figure 7-1](#) and [Figure 7-2](#) contrast the performance of a traditional complementary rail-to-rail input stage amplifier with the performance of the zero-crossover OPA388. Significant harmonic content and distortion is generated during the differential pair transition (such a transition does not exist in the OPA388). Crossover distortion is eliminated through the use of a single differential pair coupled with an internal low-noise charge pump. The OPAx388 maintains noise, bandwidth, and offset performance throughout the input common-mode range, thus reducing printed circuit board (PCB) and bill of materials (BOM) complexity through the reduction of power-supply rails.

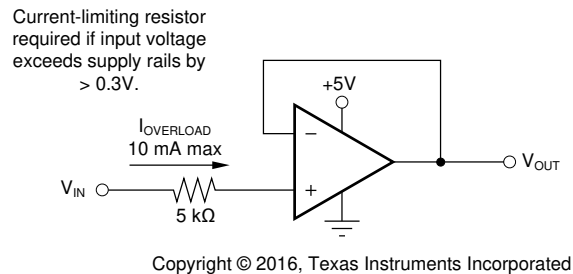


**Figure 7-1. Input Crossover Distortion Nonlinearity**



**Figure 7-2. Input Crossover Distortion Spectral Content**

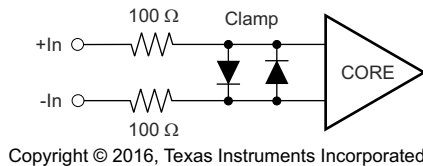
Typically, input bias current is approximately  $\pm 30$  pA. Input voltages exceeding the power supplies, however, can cause excessive current to flow into or out of the input pins. Momentary voltages greater than the power supply can be tolerated if the input current is limited to 10 mA. This limitation is easily accomplished with an input resistor, as shown in Figure 7-3.



**Figure 7-3. Input Current Protection**

### 7.3.3 Input Differential Voltage

The typical input bias current of the OPAx388 during normal operation is approximately 30 pA. In overdriven conditions, the bias current can increase significantly. The most common cause of an overdriven condition occurs when the operational amplifier is outside of the linear range of operation. When the output of the operational amplifier is driven to one of the supply rails, the feedback loop requirements cannot be satisfied and a differential input voltage develops across the input pins. This differential input voltage results in activation of parasitic diodes inside the front-end input chopping switches that combine with 10-k $\Omega$  electromagnetic interference (EMI) filter resistors to create the equivalent circuit shown in Figure 7-4. Notice that the input bias current remains within specification in the linear region.



**Figure 7-4. Equivalent Input Circuit**

### 7.3.4 Internal Offset Correction

The OPA388 family of operational amplifiers uses an auto-calibration technique with a time-continuous, 200-kHz operational amplifier in the signal path. This amplifier is zero-corrected every 5  $\mu$ s using a proprietary technique. At power-up, the amplifier requires approximately 1 ms to achieve the specified  $V_{OS}$  accuracy. This design has no aliasing or flicker noise.

### 7.3.5 EMI Susceptibility and Input Filtering

Operational amplifiers vary in susceptibility to EMI. If conducted EMI enters the operational amplifier, the dc offset at the amplifier output can shift from its nominal value when EMI is present. This shift is a result of signal rectification associated with the internal semiconductor junctions. Although all operational amplifier pin functions can be affected by EMI, the input pins are likely to be the most susceptible. The OPAx388 operational amplifier family incorporates an internal input low-pass filter that reduces the amplifier response to EMI. Both common-mode and differential-mode filtering are provided by the input filter. The filter is designed for a cutoff frequency of approximately 20 MHz ( $-3$  dB), with a rolloff of 20 dB per decade.

## 7.4 Device Functional Modes

The OPA388 has a single functional mode and is operational when the power-supply voltage is greater than 2.5 V ( $\pm 1.25$  V). The maximum specified power-supply voltage for the OPAx388 is 5.5 V ( $\pm 2.75$  V).

## 8 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

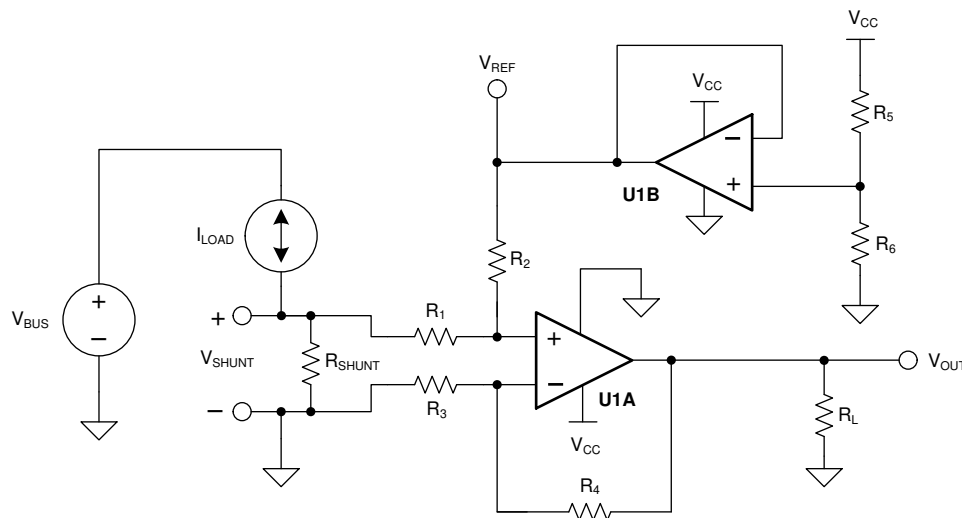
The OPAx388 is a unity-gain stable, precision operational amplifier family free from unexpected output and phase reversal. The use of proprietary zero-drift circuitry gives the benefit of low input offset voltage over time and temperature, as well as lowering the  $1/f$  noise component. As a result of the high PSRR, these devices work well in applications that run directly from battery power without regulation. The OPAx388 family is optimized for full rail-to-rail input, allowing for low-voltage, single-supply operation or split-supply use. These miniature, high-precision, low-noise amplifiers offer high-impedance inputs that have a common-mode range 100 mV beyond the supplies without input crossover distortion and a rail-to-rail output that swings within 5 mV of the supplies under normal test conditions. The OPAx388 series of precision amplifiers is designed for upstream analog signal chain applications in low or high gains, as well as downstream signal chain functions such as DAC buffering.

### 8.2 Typical Applications

#### 8.2.1 Bidirectional Current-Sensing

This single-supply, low-side, bidirectional current-sensing solution detects load currents from  $-1\text{ A}$  to  $+1\text{ A}$ . The single-ended output spans from 110 mV to 3.19 V. This design uses the OPAx388 because of its low offset voltage and rail-to-rail input and output. One of the amplifiers is configured as a difference amplifier and the other amplifier provides the reference voltage.

Figure 8-1 shows the solution.



**Figure 8-1. Bidirectional Current-Sensing Schematic**

### 8.2.1.1 Design Requirements

This solution has the following requirements:

- Supply voltage: 3.3 V
- Input: –1 A to 1 A
- Output: 1.65 V ±1.54 V (110 mV to 3.19 V)

### 8.2.1.2 Detailed Design Procedure

The load current,  $I_{LOAD}$ , flows through the shunt resistor ( $R_{SHUNT}$ ) to develop the shunt voltage,  $V_{SHUNT}$ . The shunt voltage is then amplified by the difference amplifier consisting of U1A and  $R_1$  through  $R_4$ . The gain of the difference amplifier is set by the ratio of  $R_4$  to  $R_3$ . To minimize errors, set  $R_2 = R_4$  and  $R_1 = R_3$ . The reference voltage,  $V_{REF}$ , is supplied by buffering a resistor divider using U1B. The transfer function is given by [Equation 1](#).

$$V_{OUT} = V_{SHUNT} \times \text{Gain}_{\text{Diff\_Amp}} + V_{REF} \quad (1)$$

where

- $V_{SHUNT} = I_{LOAD} \times R_{SHUNT}$
- $\text{Gain}_{\text{Diff\_Amp}} = \frac{R_4}{R_3}$
- $V_{REF} = V_{CC} \times \left[ \frac{R_6}{R_5 + R_6} \right]$

There are two types of errors in this design: offset and gain. Gain errors are introduced by the tolerance of the shunt resistor and the ratios of  $R_4$  to  $R_3$  and, similarly,  $R_2$  to  $R_1$ . Offset errors are introduced by the voltage divider ( $R_5$  and  $R_6$ ) and how closely the ratio of  $R_4 / R_3$  matches  $R_2 / R_1$ . The latter value affects the CMRR of the difference amplifier, ultimately translating to an offset error.

The value of  $V_{SHUNT}$  is the ground potential for the system load because  $V_{SHUNT}$  is a low-side measurement. Therefore, a maximum value must be placed on  $V_{SHUNT}$ . In this design, the maximum value for  $V_{SHUNT}$  is set to 100 mV. [Equation 2](#) calculates the maximum value of the shunt resistor given a maximum shunt voltage of 100 mV and maximum load current of 1 A.

$$R_{SHUNT(\text{Max})} = \frac{V_{SHUNT(\text{Max})}}{I_{LOAD(\text{Max})}} = \frac{100 \text{ mV}}{1 \text{ A}} = 100 \text{ m}\Omega \quad (2)$$

The tolerance of  $R_{SHUNT}$  is directly proportional to cost. For this design, a shunt resistor with a tolerance of 0.5% was selected. If greater accuracy is required, select a 0.1% resistor or better.

The load current is bidirectional; therefore, the shunt voltage range is –100 mV to 100 mV. This voltage is divided down by  $R_1$  and  $R_2$  before reaching the operational amplifier, U1A. Make sure that the voltage present at the noninverting node of U1A is within the common-mode range of the device. Therefore, use an operational amplifier, such as the OPA388, that has a common-mode range that extends below the negative supply voltage. Finally, to minimize offset error, note that the OPA388 has a typical offset voltage of merely ±0.25 μV (±5 μV maximum).

Given a symmetric load current of –1 A to 1 A, the voltage divider resistors ( $R_5$  and  $R_6$ ) must be equal. To be consistent with the shunt resistor, a tolerance of 0.5% was selected. To minimize power consumption, 10-kΩ resistors were used.

To set the gain of the difference amplifier, the common-mode range and output swing of the OPA388 must be considered. Equation 3 and Equation 4 depict the typical common-mode range and maximum output swing, respectively, of the OPA388 given a 3.3-V supply.

$$-100 \text{ mV} < V_{\text{CM}} < 3.4 \text{ V} \tag{3}$$

$$100 \text{ mV} < V_{\text{OUT}} < 3.2 \text{ V} \tag{4}$$

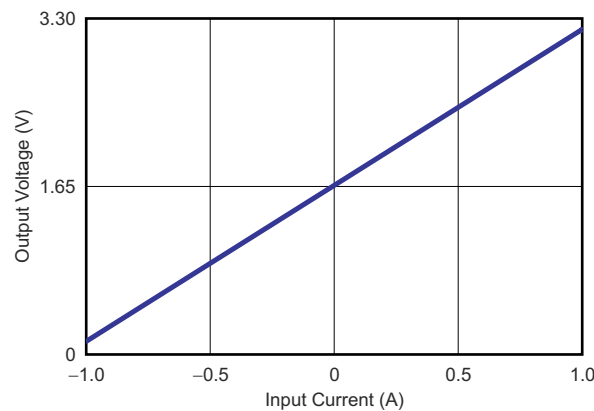
The gain of the difference amplifier can now be calculated as shown in Equation 5.

$$\text{Gain}_{\text{Diff\_Amp}} = \frac{V_{\text{OUT\_Max}} - V_{\text{OUT\_Min}}}{R_{\text{SHUNT}} \times (I_{\text{MAX}} - I_{\text{MIN}})} = \frac{3.2 \text{ V} - 100 \text{ mV}}{100 \text{ m}\Omega \times [1 \text{ A} - (-1 \text{ A})]} = 15.5 \frac{\text{V}}{\text{V}} \tag{5}$$

The resistor value selected for R<sub>1</sub> and R<sub>3</sub> was 1 kΩ. 15.4 kΩ was selected for R<sub>2</sub> and R<sub>4</sub> because this number is the nearest standard value. Therefore, the ideal gain of the difference amplifier is 15.4 V/V.

The gain error of the circuit primarily depends on R<sub>1</sub> through R<sub>4</sub>. As a result of this dependence, 0.1% resistors were selected. This configuration reduces the likelihood that the design requires a two-point calibration. A simple one-point calibration, if desired, removes the offset errors introduced by the 0.5% resistors.

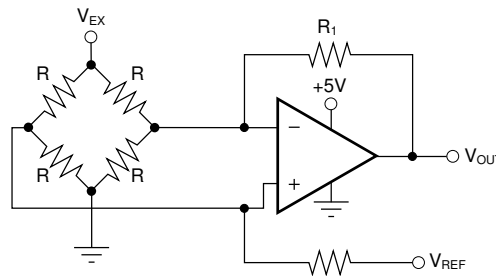
### 8.2.1.3 Application Curve



**Figure 8-2. Bidirectional Current-Sensing Circuit Performance: Output Voltage vs Input Current**

### 8.2.2 Single Operational Amplifier Bridge Amplifier

Figure 8-3 shows the basic configuration for a bridge amplifier.



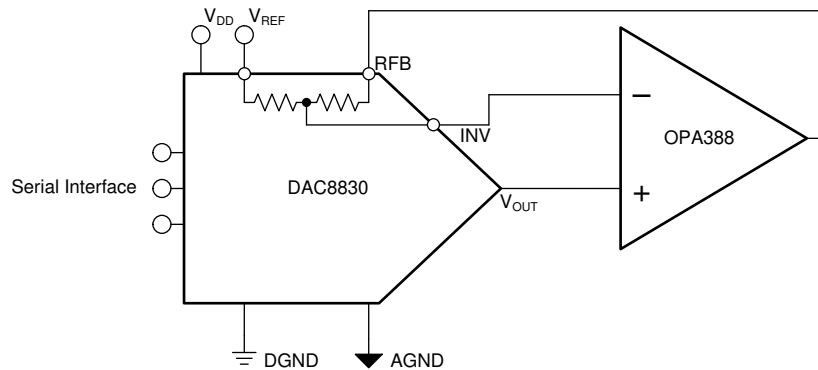
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**Figure 8-3. Single Operational Amplifier Bridge Amplifier Schematic**

### 8.2.3 Precision, Low-Noise, DAC Buffer

The OPA388 can be used for a precision DAC buffer, as shown in Figure 8-4, in conjunction with the DAC8830.

The OPA388 provides an ultra-low drift, precision output buffer for the DAC. A wide range of DAC codes can be used in the linear region because the OPA388 employs zero-crossover technology. A precise reference is essential for maximum accuracy because the DAC8830 is a 16-bit converter.



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**Figure 8-4. Precision DAC Buffer**

### 8.2.4 Load Cell Measurement

Figure 8-5 shows the OPA388 in a high-CMRR dual-op amp instrumentation amplifier with a trim resistor and 6-wire load cell for precision measurement. Figure 8-6 illustrates the output voltage as a function of load cell resistance change, along with the nonlinearity of the system.

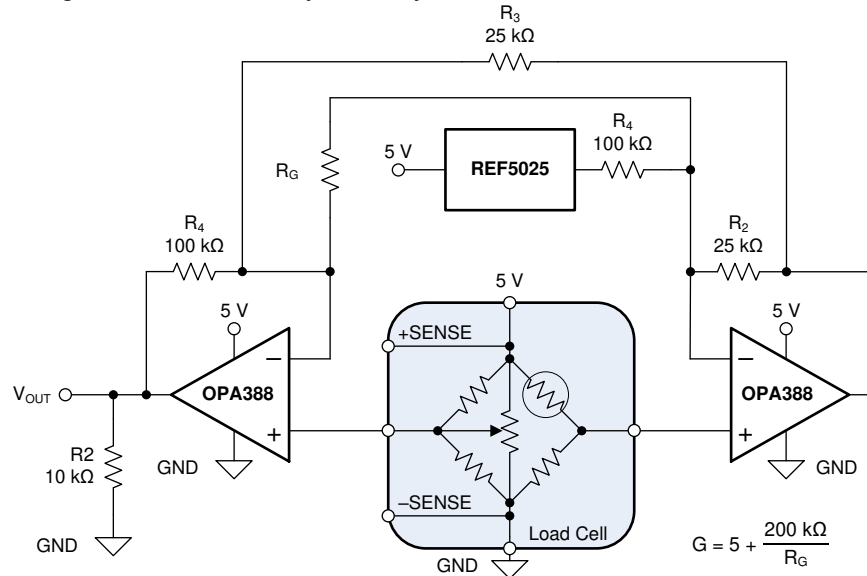


Figure 8-5. Load Cell Measurement Schematic

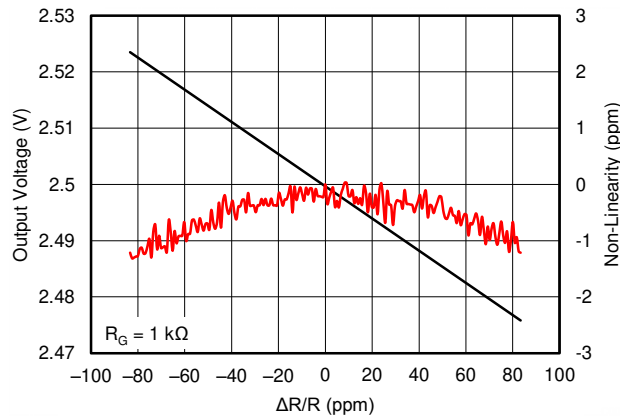


Figure 8-6. Load Cell Measurement Output

## 9 Power Supply Recommendations

The OPAx388 family of devices is specified for operation from 2.5 V to 5.5 V ( $\pm 1.25 \text{ V}$  to  $\pm 2.75 \text{ V}$ ). Parameters that can exhibit significant variance with regard to operating voltage are presented in the *Typical Characteristics* section.

## 10 Layout

### 10.1 Layout Guidelines

Paying attention to good layout practice is always recommended. Keep traces short and, when possible, use a printed-circuit board (PCB) ground plane with surface-mount components placed as close to the device pins as possible. Place a 0.1- $\mu\text{F}$  capacitor closely across the supply pins. These guidelines must be applied throughout the analog circuit to improve performance and provide benefits such as reducing the electromagnetic interference (EMI) susceptibility.

For lowest offset voltage and precision performance, circuit layout and mechanical conditions must be optimized. Avoid temperature gradients that create thermoelectric (Seebeck) effects in the thermocouple junctions formed from connecting dissimilar conductors. These thermally-generated potentials can be made to cancel by assuring they are equal on both input terminals. Other layout and design considerations include:

- Use low thermoelectric-coefficient conditions (avoid dissimilar metals).
- Thermally isolate components from power supplies or other heat sources.
- Shield operational amplifier and input circuitry from air currents, such as cooling fans.

Following these guidelines reduces the likelihood of junctions being at different temperatures, which can cause thermoelectric voltage drift of 0.1  $\mu\text{V}/^\circ\text{C}$  or higher, depending on materials used.

### 10.2 Layout Example

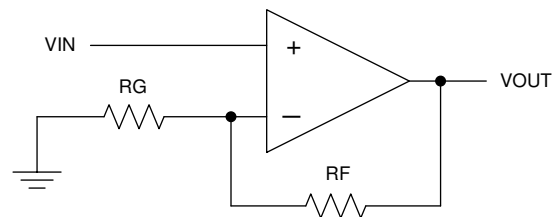


Figure 10-1. Schematic Representation

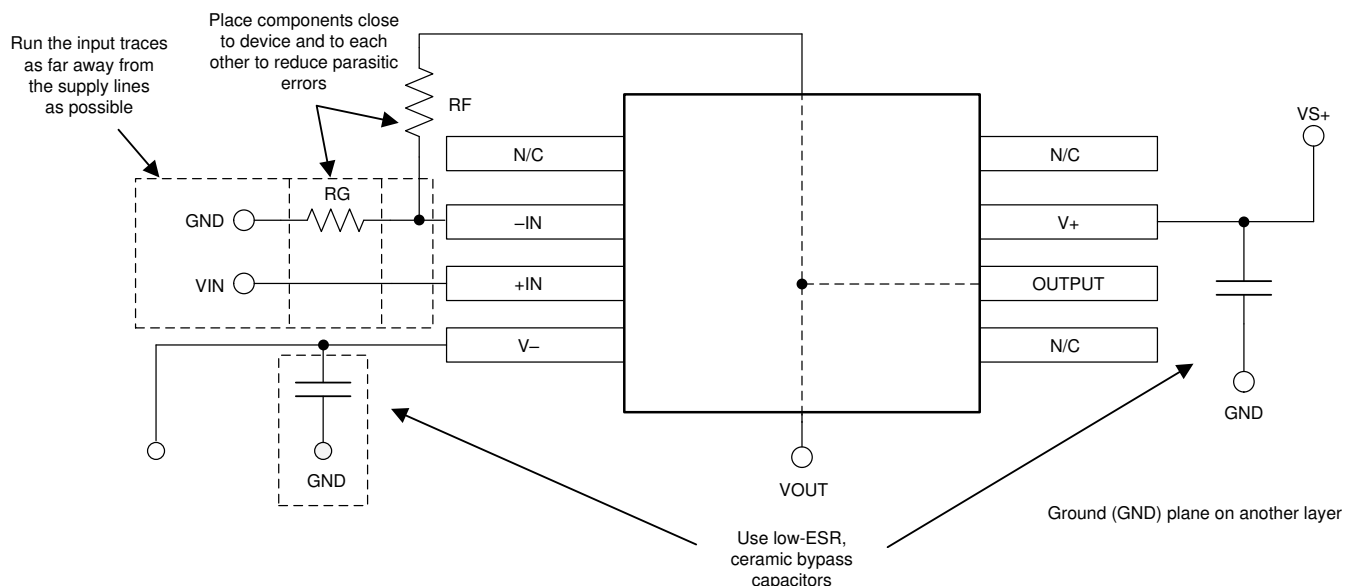


Figure 10-2. OPA388 Layout Example

## 11 Device and Documentation Support

### 11.1 Device Support

#### 11.1.1 Development Support

##### 11.1.1.1 TINA-TI™ Simulation Software (Free Download)

TINA-TI™ simulation software is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI simulation software is a free, fully-functional version of the TINA™ software, preloaded with a library of macromodels, in addition to a range of both passive and active models. TINA-TI simulation software provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a [free download](#) from the Analog eLab Design Center, TINA-TI simulation software offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

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#### Note

These files require that either the TINA software or TINA-TI software be installed. Download the free TINA-TI simulation software from the [TINA-TI™ software folder](#).

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##### 11.1.1.2 TI Precision Designs

The OPAx388 family is featured on TI Precision Designs, available online at [www.ti.com/ww/en/analog/precision-designs/](http://www.ti.com/ww/en/analog/precision-designs/). TI Precision Designs are analog solutions created by TI's precision analog applications experts and offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits.

### 11.2 Documentation Support

#### 11.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, [Circuit board layout techniques](#)
- Texas Instruments, [DAC883x 16-Bit, Ultra-Low Power, Voltage-Output Digital-to-Analog Converters data sheet](#)

#### 11.3 Related Links

[Table 11-1](#) lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 11-1. Related Links**

| PARTS   | PRODUCT FOLDER             | SAMPLE & BUY               | TECHNICAL DOCUMENTS        | TOOLS & SOFTWARE           | SUPPORT & COMMUNITY        |
|---------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| OPA388  | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| OPA2388 | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| OPA4388 | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |

#### 11.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

#### 11.5 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

## 11.6 Trademarks

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TINA™ is a trademark of DesignSoft, Inc.

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## 11.7 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 11.8 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

| Orderable part number        | Status<br>(1) | Material type<br>(2) | Package   Pins   | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|------------------------------|---------------|----------------------|------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">OPA2388ID</a>    | Active        | Production           | SOIC (D)   8     | 75   TUBE             | Yes         | SN                                   | Level-2-260C-1 YEAR               | -40 to 125   | OP2388              |
| OPA2388ID.B                  | Active        | Production           | SOIC (D)   8     | 75   TUBE             | Yes         | SN                                   | Level-2-260C-1 YEAR               | -40 to 125   | OP2388              |
| <a href="#">OPA2388IDGKR</a> | Active        | Production           | VSSOP (DGK)   8  | 2500   LARGE T&R      | Yes         | NIPDAU   SN                          | Level-2-260C-1 YEAR               | -40 to 125   | 1D36                |
| OPA2388IDGKR.B               | Active        | Production           | VSSOP (DGK)   8  | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | 1D36                |
| <a href="#">OPA2388IDGKT</a> | Active        | Production           | VSSOP (DGK)   8  | 250   SMALL T&R       | Yes         | NIPDAU   SN<br>  NIPDAUAG            | Level-2-260C-1 YEAR               | -40 to 125   | 1D36                |
| OPA2388IDGKT.B               | Active        | Production           | VSSOP (DGK)   8  | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | 1D36                |
| <a href="#">OPA2388IDR</a>   | Active        | Production           | SOIC (D)   8     | 2500   LARGE T&R      | Yes         | SN                                   | Level-2-260C-1 YEAR               | -40 to 125   | OP2388              |
| OPA2388IDR.B                 | Active        | Production           | SOIC (D)   8     | 2500   LARGE T&R      | Yes         | SN                                   | Level-2-260C-1 YEAR               | -40 to 125   | OP2388              |
| <a href="#">OPA388ID</a>     | Active        | Production           | SOIC (D)   8     | 75   TUBE             | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | OPA388              |
| OPA388ID.B                   | Active        | Production           | SOIC (D)   8     | 75   TUBE             | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | OPA388              |
| <a href="#">OPA388IDBVR</a>  | Active        | Production           | SOT-23 (DBV)   5 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | 14KV                |
| OPA388IDBVR.B                | Active        | Production           | SOT-23 (DBV)   5 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | 14KV                |
| <a href="#">OPA388IDBVT</a>  | Active        | Production           | SOT-23 (DBV)   5 | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | 14KV                |
| OPA388IDBVT.B                | Active        | Production           | SOT-23 (DBV)   5 | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | 14KV                |
| OPA388IDBVTG4                | Active        | Production           | SOT-23 (DBV)   5 | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | 14KV                |
| OPA388IDBVTG4.B              | Active        | Production           | SOT-23 (DBV)   5 | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | 14KV                |
| <a href="#">OPA388IDGKR</a>  | Active        | Production           | VSSOP (DGK)   8  | 2500   LARGE T&R      | Yes         | NIPDAUAG                             | Level-2-260C-1 YEAR               | -40 to 125   | 14LV                |
| OPA388IDGKR.B                | Active        | Production           | VSSOP (DGK)   8  | 2500   LARGE T&R      | Yes         | NIPDAUAG                             | Level-2-260C-1 YEAR               | -40 to 125   | 14LV                |
| <a href="#">OPA388IDGKT</a>  | Active        | Production           | VSSOP (DGK)   8  | 250   SMALL T&R       | Yes         | NIPDAUAG                             | Level-2-260C-1 YEAR               | -40 to 125   | 14LV                |
| OPA388IDGKT.B                | Active        | Production           | VSSOP (DGK)   8  | 250   SMALL T&R       | Yes         | NIPDAUAG                             | Level-2-260C-1 YEAR               | -40 to 125   | 14LV                |
| <a href="#">OPA388IDR</a>    | Active        | Production           | SOIC (D)   8     | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | OPA388              |
| OPA388IDR.B                  | Active        | Production           | SOIC (D)   8     | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | OPA388              |
| OPA388IDRG4                  | Active        | Production           | SOIC (D)   8     | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | OPA388              |
| OPA388IDRG4.B                | Active        | Production           | SOIC (D)   8     | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | OPA388              |
| <a href="#">OPA4388ID</a>    | Active        | Production           | SOIC (D)   14    | 50   TUBE             | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | OPA4388             |
| OPA4388ID.B                  | Active        | Production           | SOIC (D)   14    | 50   TUBE             | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | OPA4388             |
| <a href="#">OPA4388IDR</a>   | Active        | Production           | SOIC (D)   14    | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | OPA4388             |
| OPA4388IDR.B                 | Active        | Production           | SOIC (D)   14    | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | OPA4388             |

| Orderable part number       | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|-----------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">OPA4388IPW</a>  | Active        | Production           | TSSOP (PW)   14 | 90   TUBE             | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | OPA4388             |
| OPA4388IPW.B                | Active        | Production           | TSSOP (PW)   14 | 90   TUBE             | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | OPA4388             |
| <a href="#">OPA4388IPWR</a> | Active        | Production           | TSSOP (PW)   14 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | OPA4388             |
| OPA4388IPWR.B               | Active        | Production           | TSSOP (PW)   14 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | OPA4388             |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**OTHER QUALIFIED VERSIONS OF OPA2388, OPA388 :**

- Automotive : [OPA2388-Q1](#), [OPA388-Q1](#)

**NOTE: Qualified Version Definitions:**

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| OPA2388IDGKR  | VSSOP        | DGK             | 8    | 2500 | 330.0              | 12.4               | 5.25    | 3.35    | 1.25    | 8.0     | 12.0   | Q1            |
| OPA2388IDGKR  | VSSOP        | DGK             | 8    | 2500 | 330.0              | 12.4               | 5.3     | 3.4     | 1.4     | 8.0     | 12.0   | Q1            |
| OPA2388IDGKT  | VSSOP        | DGK             | 8    | 250  | 330.0              | 12.4               | 5.25    | 3.35    | 1.25    | 8.0     | 12.0   | Q1            |
| OPA2388IDGKT  | VSSOP        | DGK             | 8    | 250  | 330.0              | 12.4               | 5.3     | 3.4     | 1.4     | 8.0     | 12.0   | Q1            |
| OPA2388IDR    | SOIC         | D               | 8    | 2500 | 330.0              | 12.8               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| OPA388IDBVR   | SOT-23       | DBV             | 5    | 3000 | 180.0              | 8.4                | 3.23    | 3.17    | 1.37    | 4.0     | 8.0    | Q3            |
| OPA388IDBVT   | SOT-23       | DBV             | 5    | 250  | 180.0              | 8.4                | 3.23    | 3.17    | 1.37    | 4.0     | 8.0    | Q3            |
| OPA388IDBVTG4 | SOT-23       | DBV             | 5    | 250  | 180.0              | 8.4                | 3.23    | 3.17    | 1.37    | 4.0     | 8.0    | Q3            |
| OPA388IDGKR   | VSSOP        | DGK             | 8    | 2500 | 330.0              | 12.4               | 5.3     | 3.4     | 1.4     | 8.0     | 12.0   | Q1            |
| OPA388IDGKT   | VSSOP        | DGK             | 8    | 250  | 330.0              | 12.4               | 5.3     | 3.4     | 1.4     | 8.0     | 12.0   | Q1            |
| OPA388IDR     | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| OPA388IDRG4   | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| OPA4388IDR    | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| OPA4388IPWR   | TSSOP        | PW              | 14   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

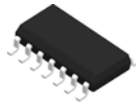
| Device        | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| OPA2388IDGKR  | VSSOP        | DGK             | 8    | 2500 | 366.0       | 364.0      | 50.0        |
| OPA2388IDGKR  | VSSOP        | DGK             | 8    | 2500 | 353.0       | 353.0      | 32.0        |
| OPA2388IDGKT  | VSSOP        | DGK             | 8    | 250  | 366.0       | 364.0      | 50.0        |
| OPA2388IDGKT  | VSSOP        | DGK             | 8    | 250  | 353.0       | 353.0      | 32.0        |
| OPA2388IDR    | SOIC         | D               | 8    | 2500 | 366.0       | 364.0      | 50.0        |
| OPA388IDBVR   | SOT-23       | DBV             | 5    | 3000 | 213.0       | 191.0      | 35.0        |
| OPA388IDBVT   | SOT-23       | DBV             | 5    | 250  | 213.0       | 191.0      | 35.0        |
| OPA388IDBVTG4 | SOT-23       | DBV             | 5    | 250  | 213.0       | 191.0      | 35.0        |
| OPA388IDGKR   | VSSOP        | DGK             | 8    | 2500 | 366.0       | 364.0      | 50.0        |
| OPA388IDGKT   | VSSOP        | DGK             | 8    | 250  | 366.0       | 364.0      | 50.0        |
| OPA388IDR     | SOIC         | D               | 8    | 2500 | 353.0       | 353.0      | 32.0        |
| OPA388IDRG4   | SOIC         | D               | 8    | 2500 | 353.0       | 353.0      | 32.0        |
| OPA4388IDR    | SOIC         | D               | 14   | 2500 | 353.0       | 353.0      | 32.0        |
| OPA4388IPWR   | TSSOP        | PW              | 14   | 2000 | 353.0       | 353.0      | 32.0        |

**TUBE**


\*All dimensions are nominal

| Device       | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|--------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| OPA2388ID    | D            | SOIC         | 8    | 75  | 517    | 7.87   | 635    | 4.25   |
| OPA2388ID.B  | D            | SOIC         | 8    | 75  | 517    | 7.87   | 635    | 4.25   |
| OPA388ID     | D            | SOIC         | 8    | 75  | 506.6  | 8      | 3940   | 4.32   |
| OPA388ID.B   | D            | SOIC         | 8    | 75  | 506.6  | 8      | 3940   | 4.32   |
| OPA4388ID    | D            | SOIC         | 14   | 50  | 506.6  | 8      | 3940   | 4.32   |
| OPA4388ID.B  | D            | SOIC         | 14   | 50  | 506.6  | 8      | 3940   | 4.32   |
| OPA4388IPW   | PW           | TSSOP        | 14   | 90  | 530    | 10.2   | 3600   | 3.5    |
| OPA4388IPW.B | PW           | TSSOP        | 14   | 90  | 530    | 10.2   | 3600   | 3.5    |

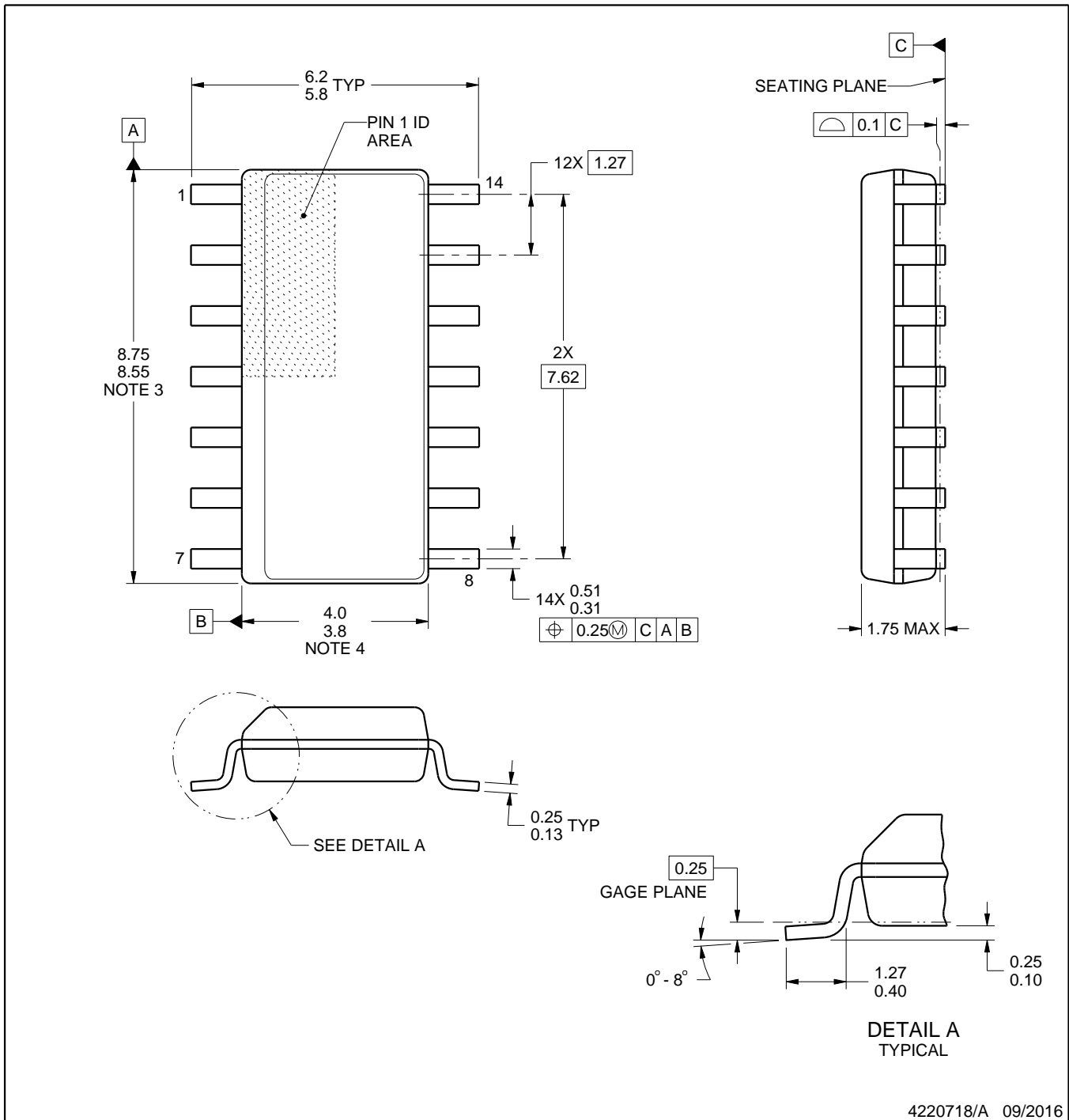
D0014A



# PACKAGE OUTLINE

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

# EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

### NOTES:

- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed  $.006$  [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



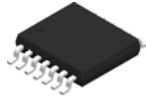
SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW0014A



# PACKAGE OUTLINE

## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220202/B 12/2023

NOTES:

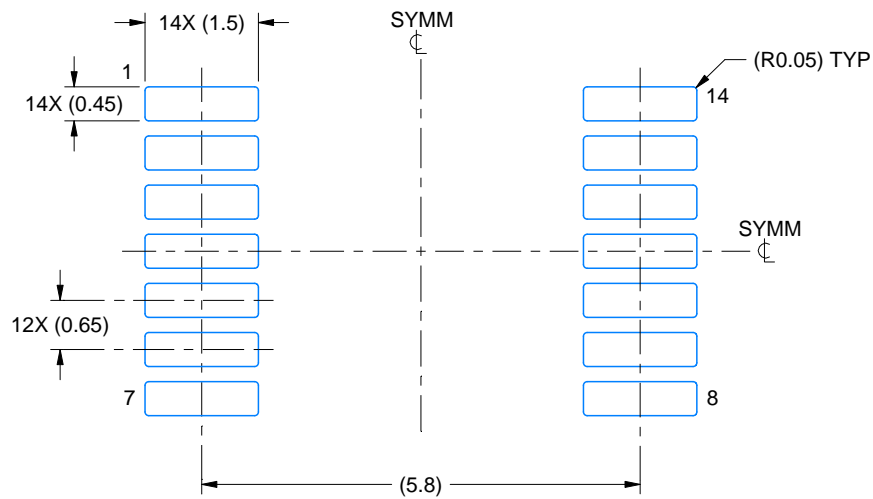
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220202/B 12/2023

NOTES: (continued)

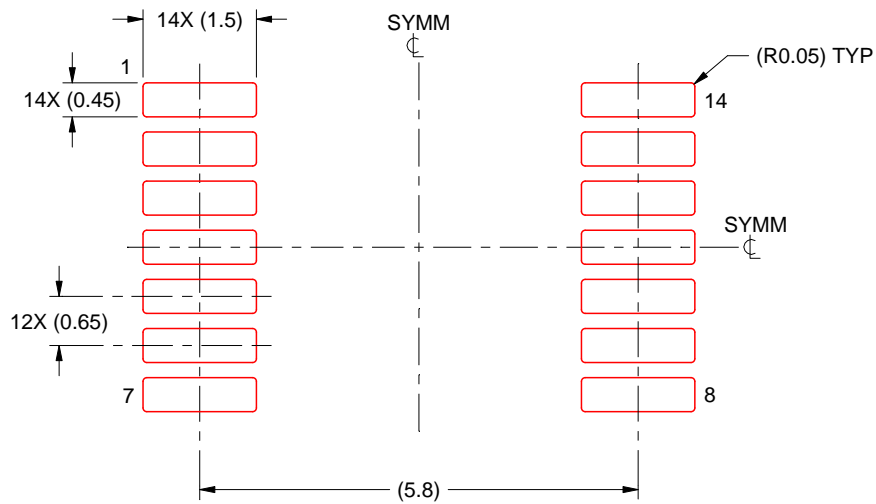
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



# EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

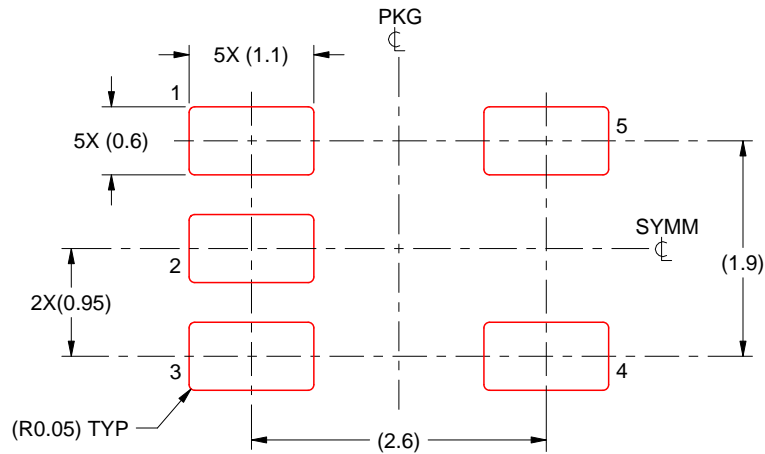
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

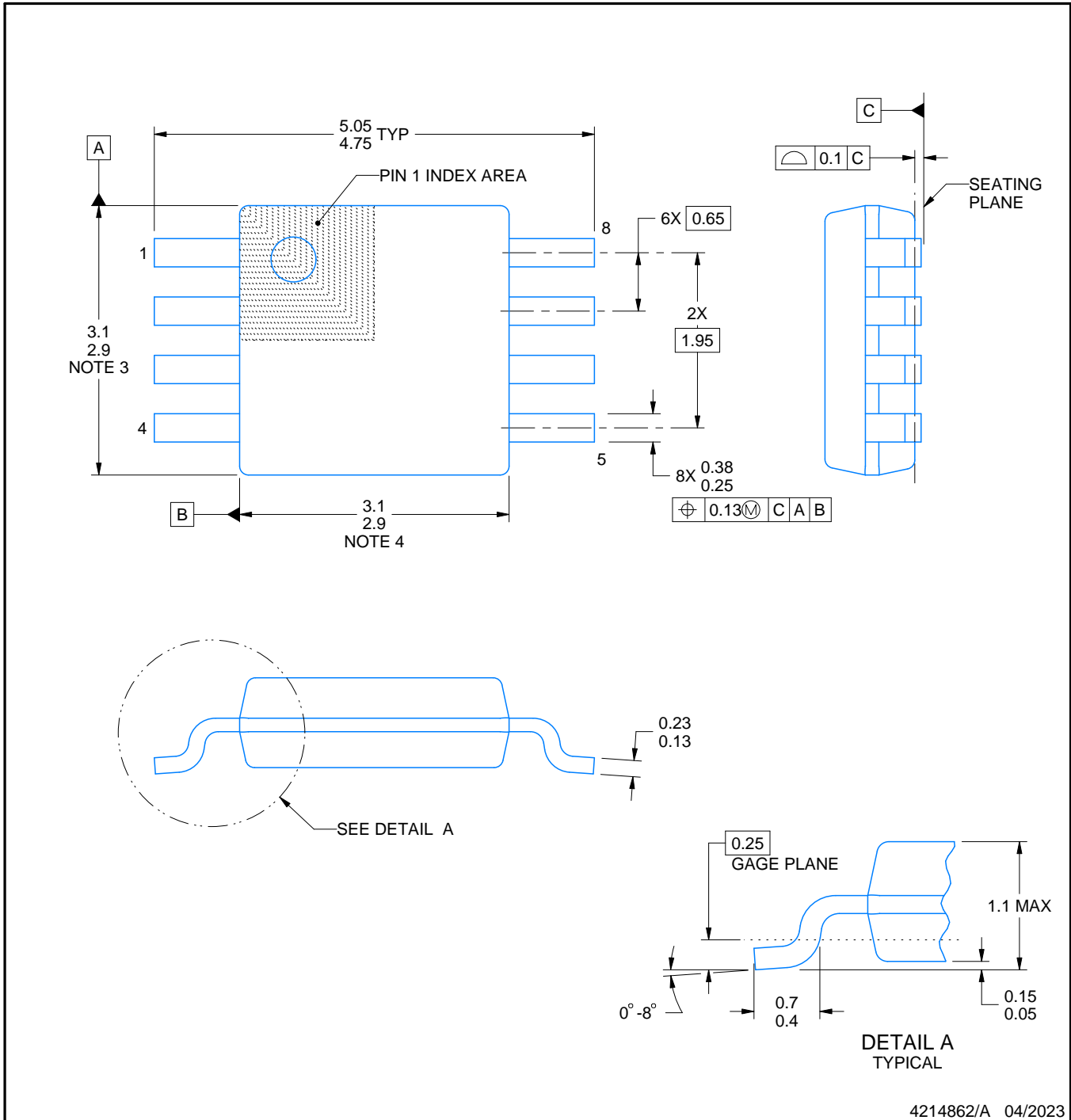
# DGK0008A



# PACKAGE OUTLINE

## VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4214862/A 04/2023

**NOTES:**

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

# EXAMPLE BOARD LAYOUT

DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 15X



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

# EXAMPLE STENCIL DESIGN

DGK0008A

<sup>TM</sup> VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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