0.05 μV/°C MAX, SINGLE-SUPPLY CMOS OPERATIONAL AMPLIFIER ZERO-DRIFT SERIES

FEATURES

- **Low Offset Voltage: 5 μV (max)**
- **Zero Drift: 0.02 μV/°C (typ)**
- **Quiescent Current: 570 μA**
- **Single-Supply Operation**
- **Ceramic DIP Package**

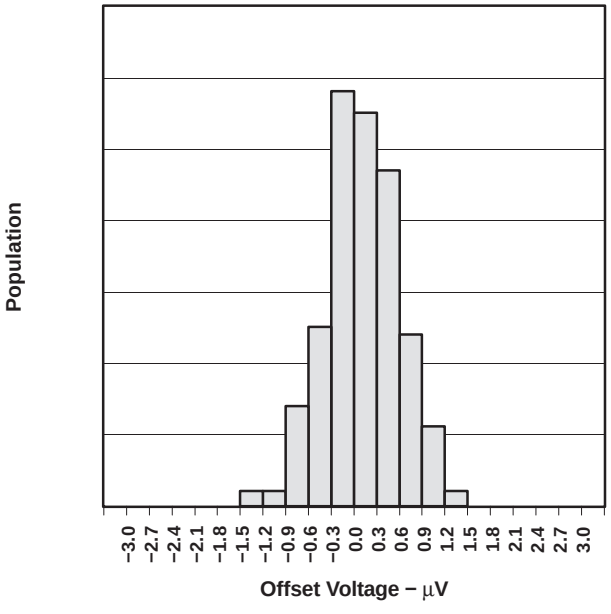
APPLICATIONS

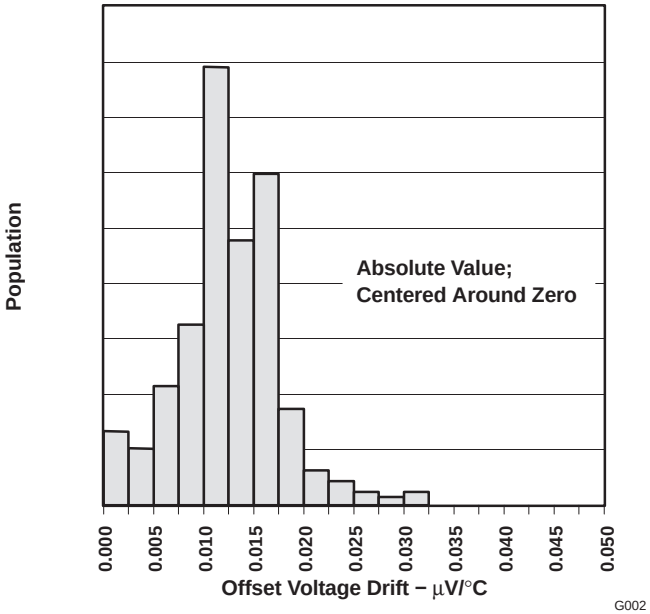
- **Transducer Applications**
- **Temperature Measurement**
- **Electronic Scales**
- **Medical Instrumentation**
- **Battery-Powered Instruments**
- **Handheld Test Equipment**

DESCRIPTION

The OPA2335 CMOS operational amplifier uses auto-zeroing techniques to simultaneously provide very low offset voltage (5 μV max), and near-zero drift over time and temperature. This high-precision, low quiescent current amplifier offers high input impedance and rail-to-rail output swing. Single or dual supplies as low as 2.7 V (±1.35 V) and up to 5.5 V (±2.75 V) may be used. This op amp is optimized for low-voltage, single-supply operation.

The OPA2335 is available in a CDIP-8 package and is specified for operation from –55°C to 125°C.





Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

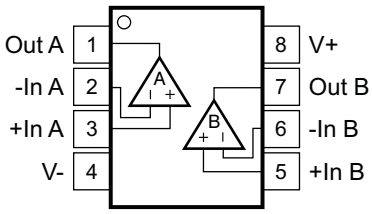
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER
OPA2335	CDIP-8	JG	–55°C to 125°C	OPA2335AMJG	OPA2335AMJG

PIN CONFIGURATIONS

OPA2335



CDIP

P0037-01

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
Supply voltage		7 V	
Signal input terminals	Voltage(2)	–0.5 to (V+) + 0.5	V
	Current(2)	±10	mA
Output short circuit(3)		Continuous	
Operating temperature T_A		–55 to 150	°C
Storage temperature T_A		–65 to 150	°C
Junction temperature		150	°C
Lead temperature (soldering, 10s)		300	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these, or any other conditions beyond those specified, is not implied.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails should be current-limited to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package

ELECTRICAL CHARACTERISTICS

At T_A = 25°C, V_S = +5 V, R_L = 10 kΩ connected to $V_S/2$, and V_{OUT} = $V_S/2$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
Input offset voltage	V_{OS}	V_{CM} = $V_S/2$	T_A = 25°C		1	5	µV
			T_A = Full range			10	
vs Temperature	dV_{OS}/dT				±0.02		µV/°C

ELECTRICAL CHARACTERISTICS (continued)

At T_A = 25°C, V_S = +5 V, R_L = 10 kΩ connected to V_S/2, and V_{OUT} = V_S/2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
vs Power supply	PSSR	V_S = 2.7 V to 5.5 V	T_A = Full range		±1	±2	µV/V
Long-term stability					See Note (1)		
Channel separation, dc					0.1		µV/V
INPUT BIAS CURRENT							
Input bias current	I_B	V_{CM} = V_S/2	T_A = 25°C		±70	±200	pA
			T_A = Full range		1		nA
Input offset current	I_{OS}				±120	±400	pA
NOISE							
Input voltage noise	e_n	f = 0.01 Hz to 10 Hz			1.4		µVpp
Input current noise density	i_n	f = 10 Hz			20		fA/√Hz
INPUT VOLTAGE RANGE							
Common-mode voltage range	V_{CM}			(V–) –0.1		(V+) –1.5	V
Common-mode rejection ratio	CMRR	(V–) – 0.1 V < V_{CM} < (V+) – 1.5V	T_A = 25°C	110	130		dB
		(V–) < V_{CM} < (V+) – 1.5V	T_A = Full range	110	130		dB
INPUT CAPACITANCE							
Differential					1		pF
Common-mode					5		pF
OPEN-LOOP GAIN							
Open-loop voltage gain	A_{OL}	50 mV < V_O < (V+) – 50 mV, R_L = 100 kΩ, V_{CM} = V_S/2	T_A = Full range	110	130		dB
		100 mV < V_O < (V+) – 100 mV, R_L = 10 kΩ, V_{CM} = V_S/2	T_A = Full range	110	130		dB
FREQUENCY RESPONSE							
Gain-Bandwidth Product	GBW				2		MHz
Slew Rate	SR	G = +1			1.6		V/µs
OUTPUT							
Voltage output swing from rail		R_L = 10 kΩ	T_A = Full range		15	100	mV
		R_L = 100 kΩ	T_A = Full range		1	50	mV
Short-circuit current	I_{SC}				±50		mA
Capacitive load drive	C_{LOAD}				See Typical Characteristics		
POWER SUPPLY							
Operating voltage range				2.7		5.5	V
Quiescent current	I_Q	I_O = 0, V_S = +5 V	T_A = 25°C		570	700	µA
(total-2 amplifiers)			T_A = Full range			900	µA
TEMPERATURE RANGE							
Operating range	T_A			–55		125	°C
Storage range				–65		150	°C
Thermal resistance	θ_{JA}				119		°C/W

(1) 500-hour life test at 150°C demonstrated randomly distributed variation approximately equal to measurement repeatability of 1 µV.

TYPICAL CHARACTERISTICS

At T_A = 25°C, V_S = +5 V, R_L = 10 kΩ connected to V_S/2 and V_{OUT} = V_S/2 (unless otherwise noted)

OFFSET VOLTAGE PRODUCTION DISTRIBUTION

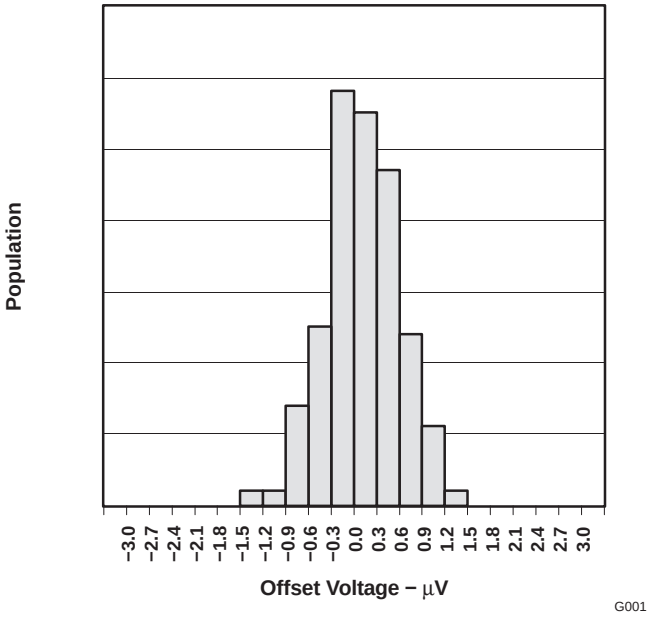


Figure 1.

OFFSET VOLTAGE DRIFT PRODUCTION DISTRIBUTION

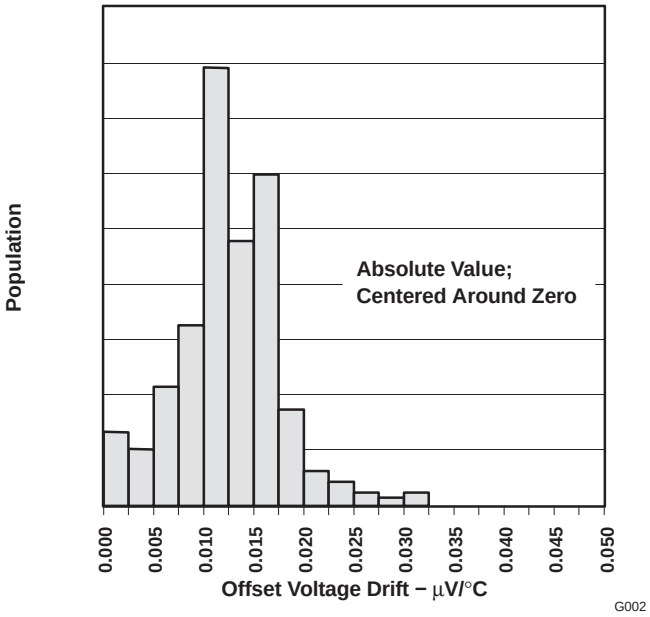


Figure 2.

OFFSET VOLTAGE SWING vs OUTPUT CURRENT

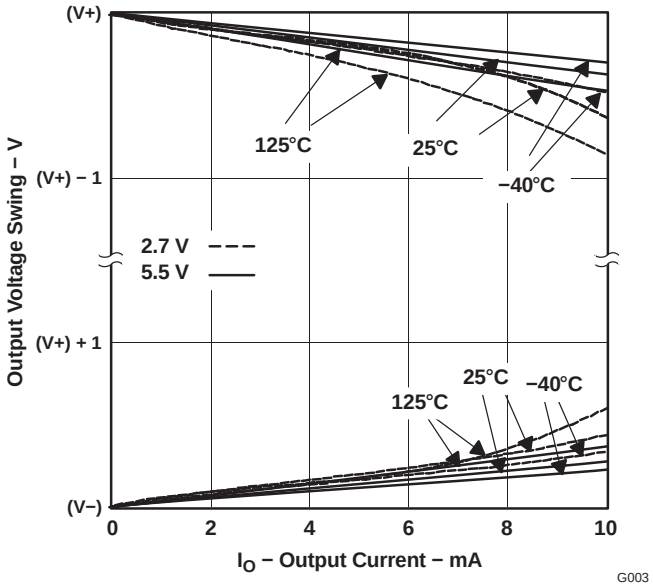


Figure 3.

INPUT BIAS CURRENT vs COMMON-MODE VOLTAGE

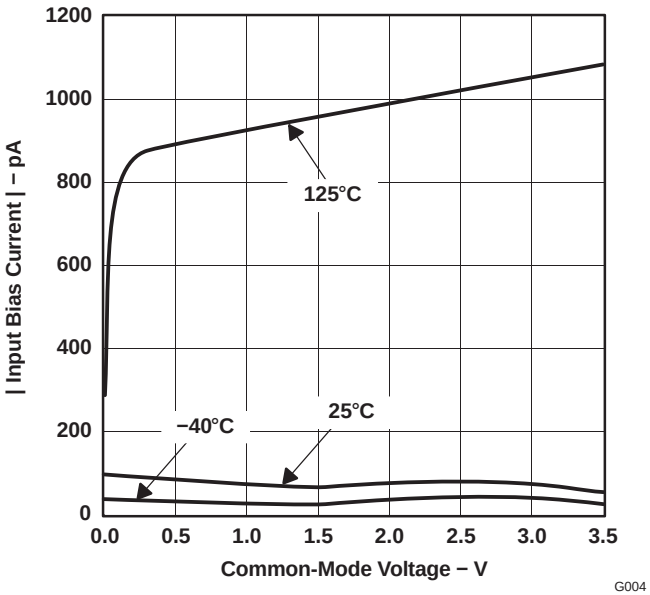


Figure 4.

TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C, V_S = +5 V, R_L = 10 kΩ connected to $V_S/2$ and V_{OUT} = $V_S/2$ (unless otherwise noted)

INPUT BIAS CURRENT vs TEMPERATURE

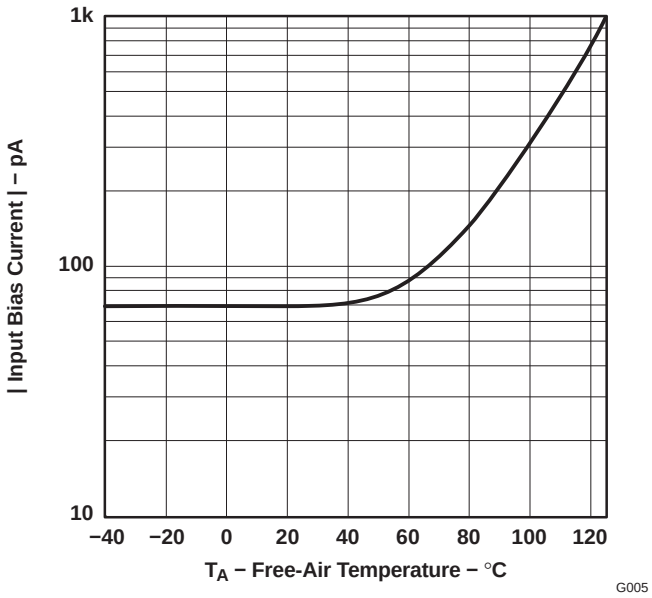


Figure 5.

QUIESCENT CURRENT (per channel) vs TEMPERATURE

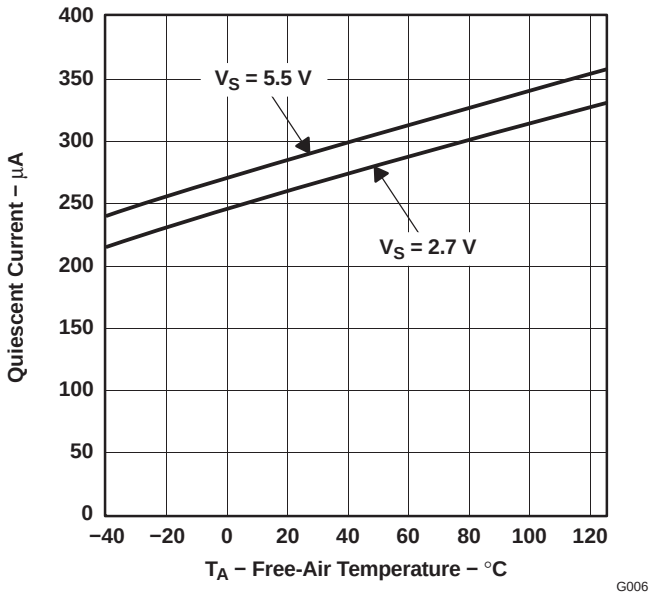


Figure 6.

OPEN-LOOP GAIN/PHASE vs FREQUENCY

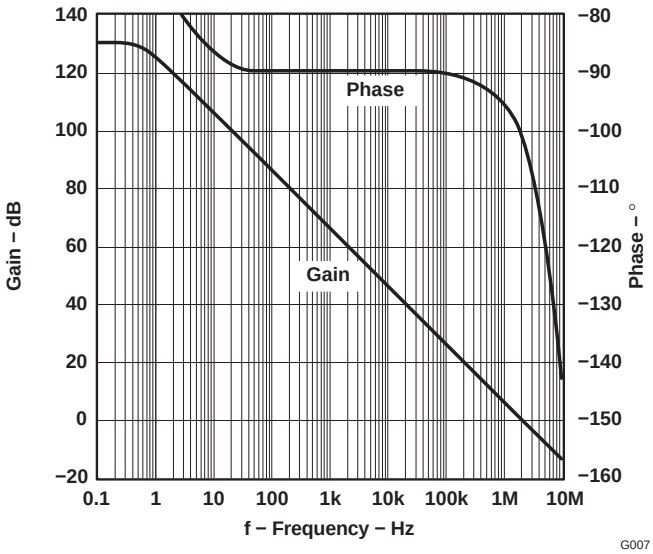


Figure 7.

LARGE-SIGNAL RESPONSE

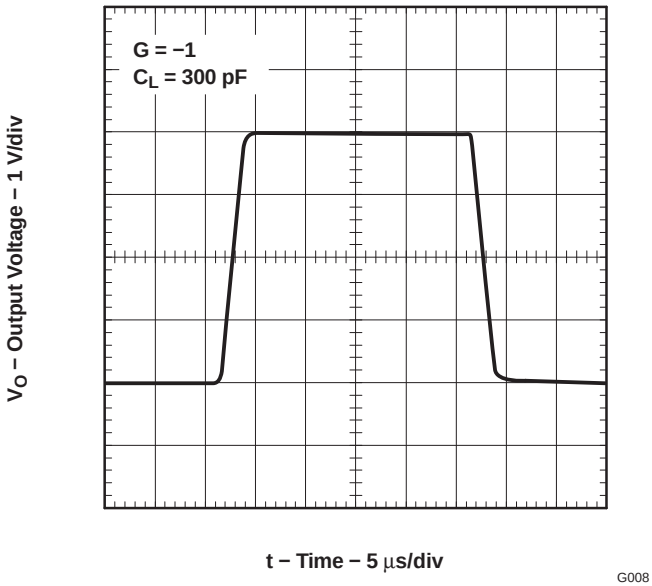


Figure 8.

TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C, V_S = +5 V, R_L = 10 kΩ connected to V_S/2 and V_{OUT} = V_S/2 (unless otherwise noted)

SMALL-SIGNAL RESPONSE

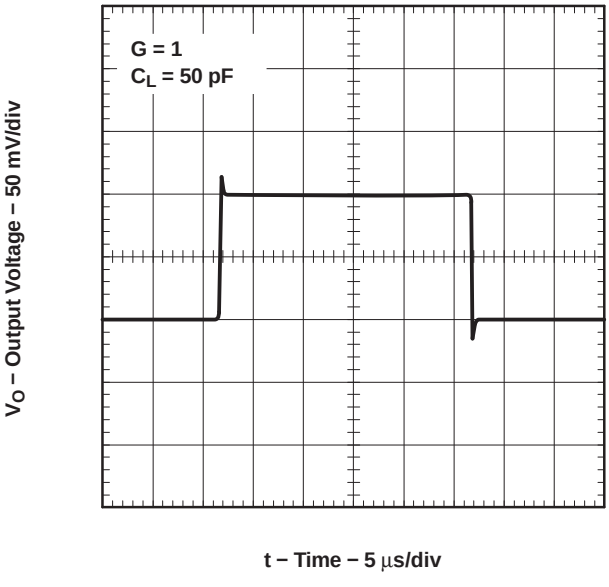


Figure 9.

POSITIVE OVER-VOLTAGE RECOVERY

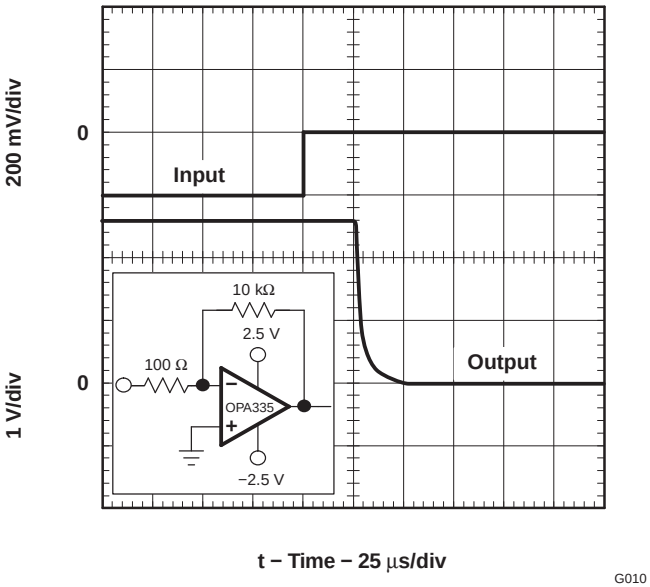


Figure 10.

NEGATIVE OVER-VOLTAGE RECOVERY

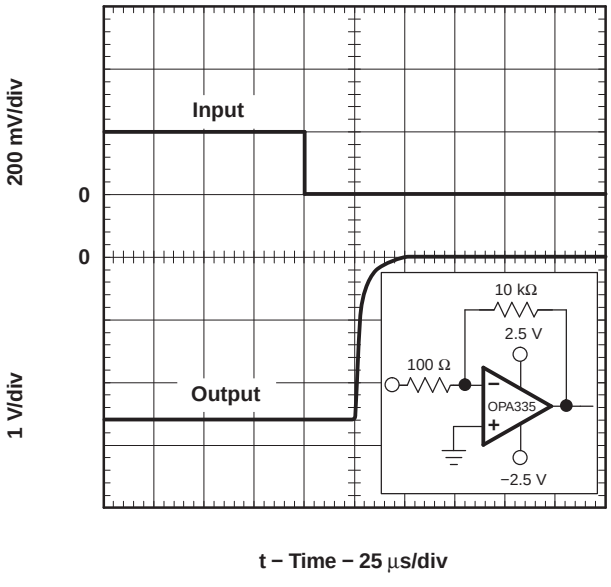


Figure 11.

COMMON-MODE REJECTION vs FREQUENCY

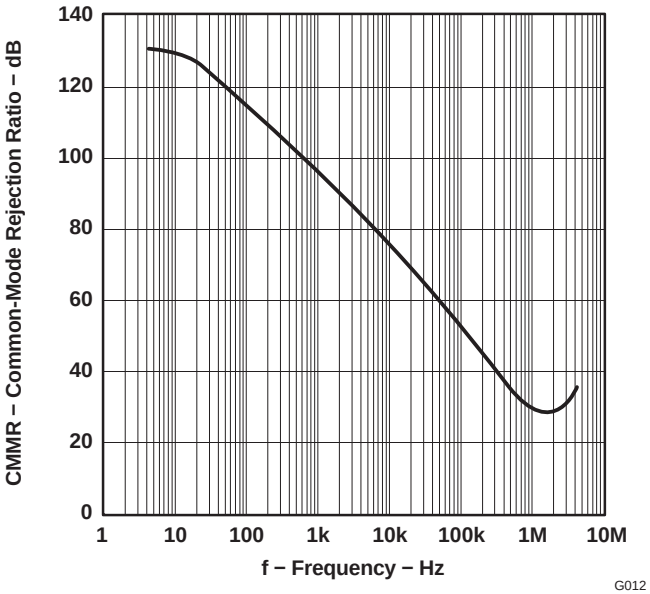


Figure 12.

TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C, V_S = +5 V, R_L = 10 kΩ connected to V_S/2 and V_{OUT} = V_S/2 (unless otherwise noted)

POWER-SUPPLY REJECTION RATIO vs FREQUENCY

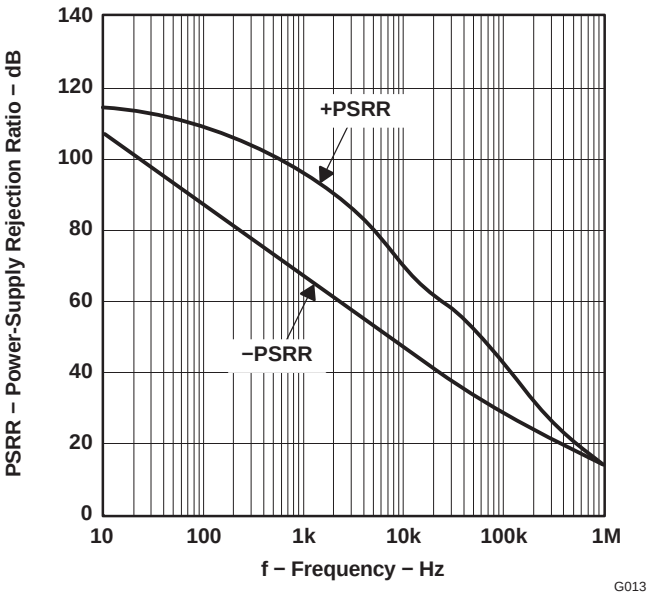


Figure 13.

SAMPLING FREQUENCY vs SUPPLY VOLTAGE

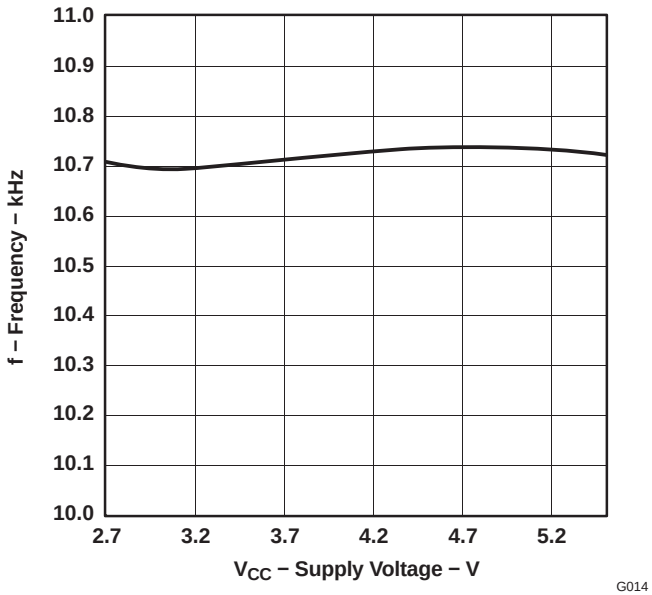


Figure 14.

NOISE vs FREQUENCY

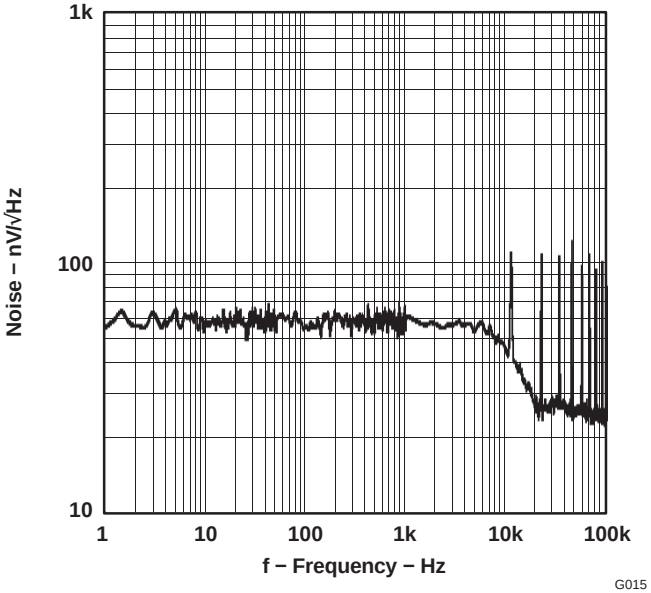


Figure 15.

0.01-Hz TO 10-Hz NOISE

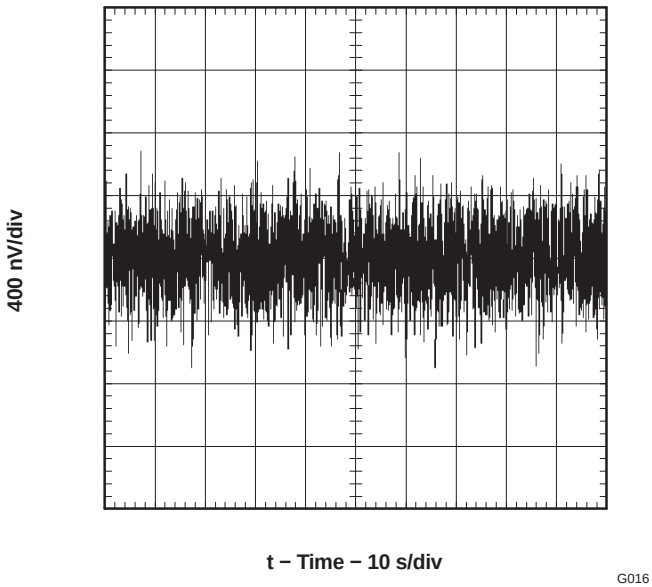


Figure 16.

TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C, V_S = +5 V, R_L = 10 kΩ connected to V_S/2 and V_{OUT} = V_S/2 (unless otherwise noted)

SAMPLING FREQUENCY vs TEMPERATURE

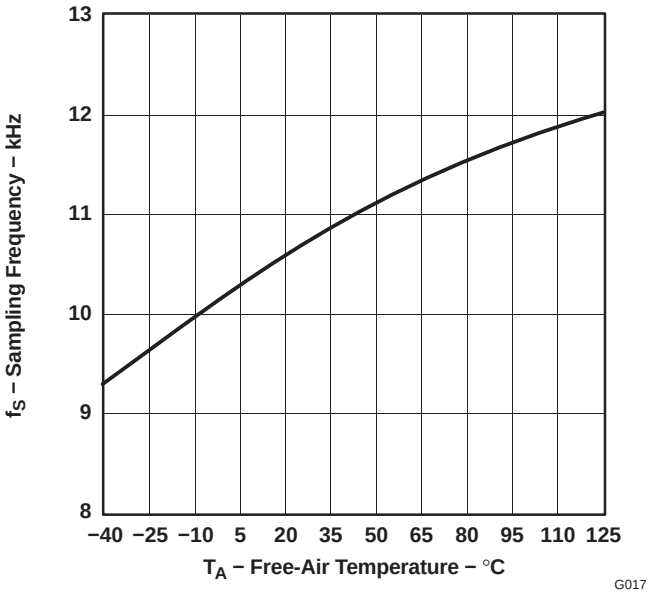


Figure 17.

SMALL-SIGNAL OVERSHOOT vs LOAD CAPACITANCE (V_S = 2.7 V TO 5 V)

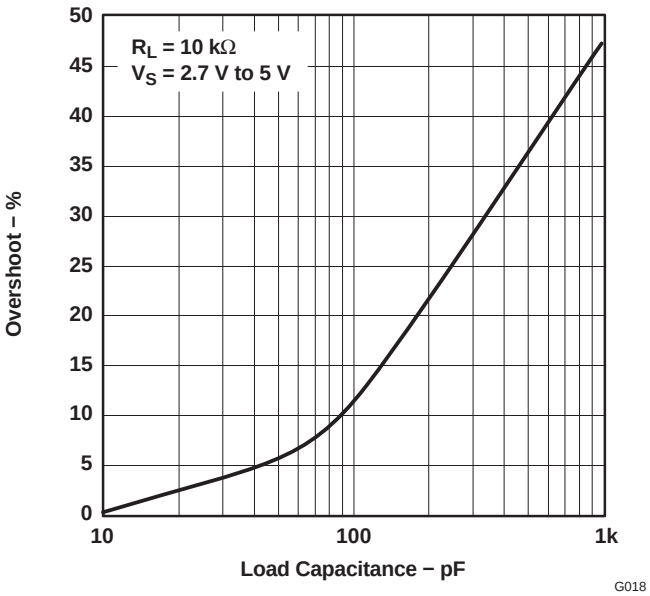


Figure 18.

SETTLING TIME vs CLOSED-LOOP GAIN

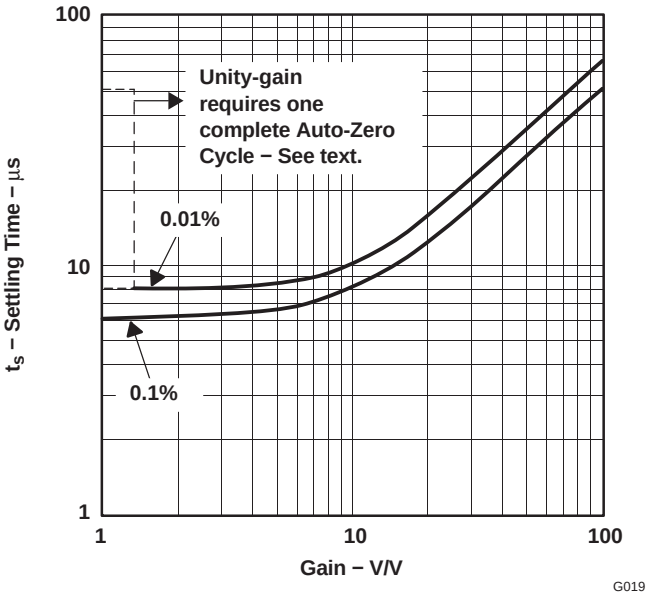


Figure 19.

COMMON-MODE RANGE vs SUPPLY VOLTAGE

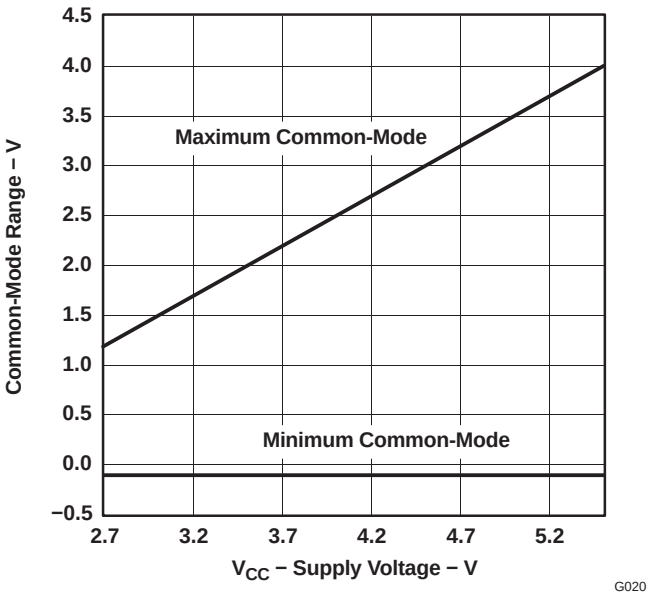


Figure 20.

APPLICATION INFORMATION

The OPA2335 op amp is unity-gain stable and free from unexpected output phase reversal. It uses auto-zeroing techniques to provide low offset voltage and very low drift over time and temperature.

Good layout practice mandates use of a 0.1-µF capacitor placed closely across the supply pins.

For lowest offset voltage and precision performance, circuit layout and mechanical conditions should be optimized. Avoid temperature gradients that create thermoelectric (Seebeck) effects in thermocouple junctions formed from connecting dissimilar conductors. These thermally-generated potentials can be made to cancel by assuring that they are equal on both input terminals.

- Use low thermoelectric-coefficient connections (avoid dissimilar metals).
- Thermally isolate components from power supplies or other heat-sources.
- Shield op amp and input circuitry from air currents, such as cooling fans.

Following these guidelines will reduce the likelihood of junctions being at different temperatures, which can cause thermoelectric voltages of 0.1 µV/°C or higher, depending on materials used.

OPERATING VOLTAGE

The OPA2335 op amp operates over a power-supply range of 2.7 V to 5.5 V (±1.35 V to ±2.75 V). Supply voltages higher than 7 V (absolute maximum) can permanently damage the amplifier. Parameters that vary over supply voltage or temperature are shown in the Typical Characteristics section of this data sheet.

INPUT VOLTAGE

The input common-mode range extends from (V–) – 0.1 V to (V+) – 1.5 V. For normal operation, the inputs must be limited to this range. The common-mode rejection ratio is only valid within the valid input common-mode range. A lower supply voltage results in lower input common-mode range; therefore, attention to these values must be given when selecting the input bias voltage. For example, when operating on a single 3-V power supply, common-mode range is from 0.1 V below ground to half the power-supply voltage.

Normally, input bias current is approximately 70 pA; however, input voltages exceeding the power supplies can cause excessive current to flow in or out of the input pins. Momentary voltages greater than the power supply can be tolerated if the input current is limited to 10 mA. This is easily accomplished with an input resistor, as shown in Figure 21.

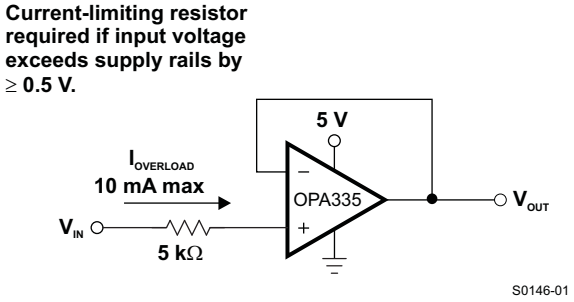


Figure 21. Input Current Protection

INTERNAL OFFSET CORRECTION

The OPA2335 op amp uses an auto-zero topology with a time-continuous 2-MHz op amp in the signal path. This amplifier is zero-corrected every 100 µs using a proprietary technique. Upon power-up, the amplifier requires one full auto-zero cycle of approximately 100 µs to achieve specified V_{OS} accuracy. Prior to this time, the amplifier functions properly, but with unspecified offset voltage.

This design has remarkably little aliasing and noise. Zero correction occurs at a 10-kHz rate, but there is virtually no fundamental noise energy present at that frequency. For all practical purposes, any glitches have energy at 20 MHz or higher and are easily filtered, if required. Most applications are not sensitive to such high-frequency noise, and no filtering is required.

APPLICATION INFORMATION (continued)

Unity-gain operation demands that the auto-zero circuitry correct for common-mode rejection errors of the main amplifier. Because these errors can be larger than 0.01% of a full-scale input step change, one calibration cycle (100 μs) can be required to achieve full accuracy. This behavior is shown in the typical characteristic section, see *Settling Time vs Closed-Loop Gain.*

ACHIEVING OUTPUT SWING TO THE OP AMP'S NEGATIVE RAIL

Some applications require output voltage swing from 0 V to a positive full-scale voltage (such as 2.5 V) with excellent accuracy. With most single-supply op amps, problems arise when the output signal approaches 0 V, near the lower output swing limit of a single-supply op amp. A good single-supply op amp may swing close to single-supply ground, but will not reach ground. The output of the OPA2335 can be made to swing to ground, or slightly below, on a single-supply power source. To do so requires use of another resistor and an additional, more negative, power supply than the op amp's negative supply. A pull-down resistor may be connected between the output and the additional negative supply to pull the output down below the value that the output would otherwise achieve, as shown in Figure 22.

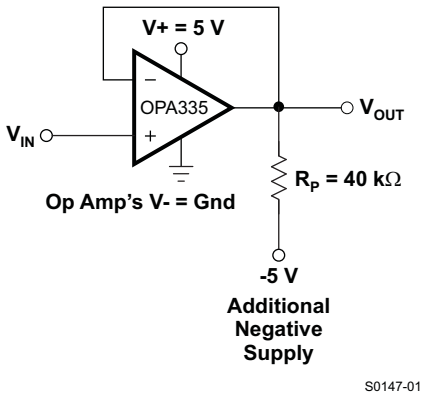


Figure 22. Op Amp With Pull-Down Resistor to Achieve V_{OUT} = Ground

The OPA2335 has an output stage that allows the output voltage to be pulled to its negative supply rail, or slightly below using the above technique. This technique only works with some types of output stages. The OPA2335 has been characterized to perform well with this technique. Accuracy is excellent down to 0 V and as low as –2 mV. Limiting and non-linearity occurs below –2 mV, but excellent accuracy returns as the output is again driven above –2 mV. Lowering the resistance of the pull-down resistor allows the op amp to swing even further below the negative rail. Resistances as low as 10 kΩ can be used to achieve excellent accuracy, down to –10 mV.

LAYOUT GUIDELINES

Attention to good layout practices is always recommended. Keep traces short. When possible, use a PCB ground plane with surface-mount components placed as close to the device pins as possible. Place a 0.1-μF capacitor closely across the supply pins. These guidelines should be applied throughout the analog circuit to improve performance and provide benefits, such as reducing the EMI (electromagnetic-interference) susceptibility.

APPLICATION INFORMATION (continued)

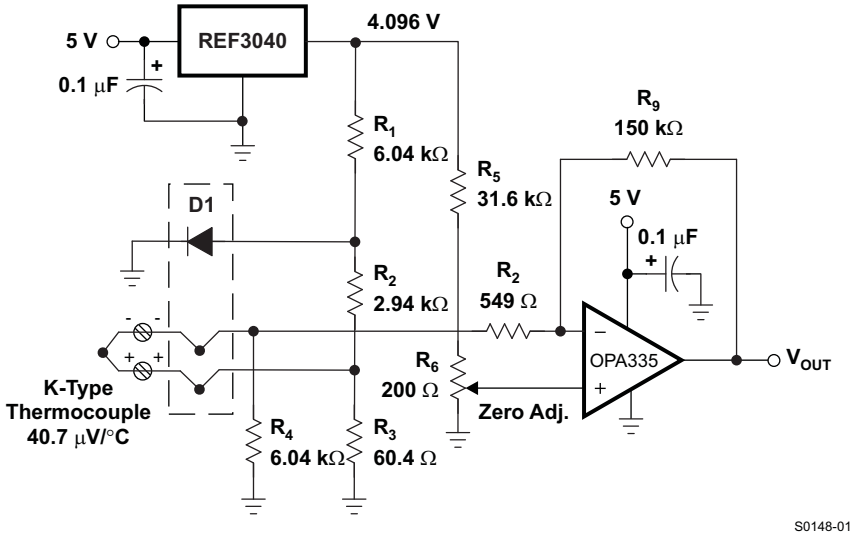


Figure 23. Temperature Measurement Circuit

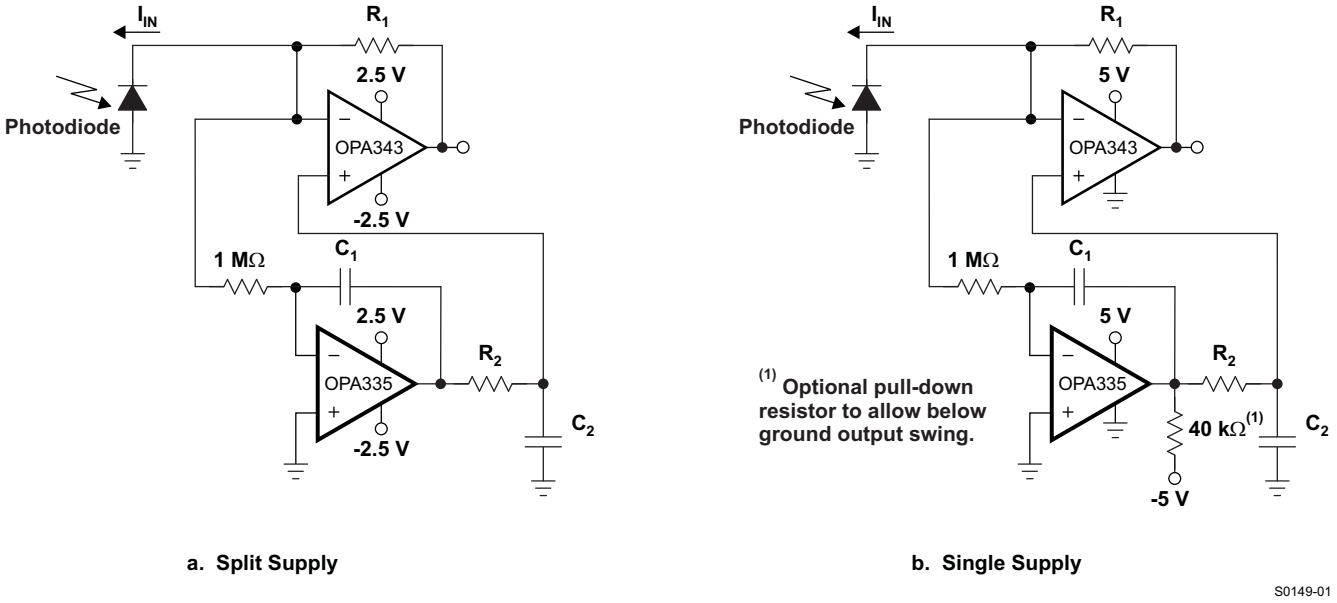
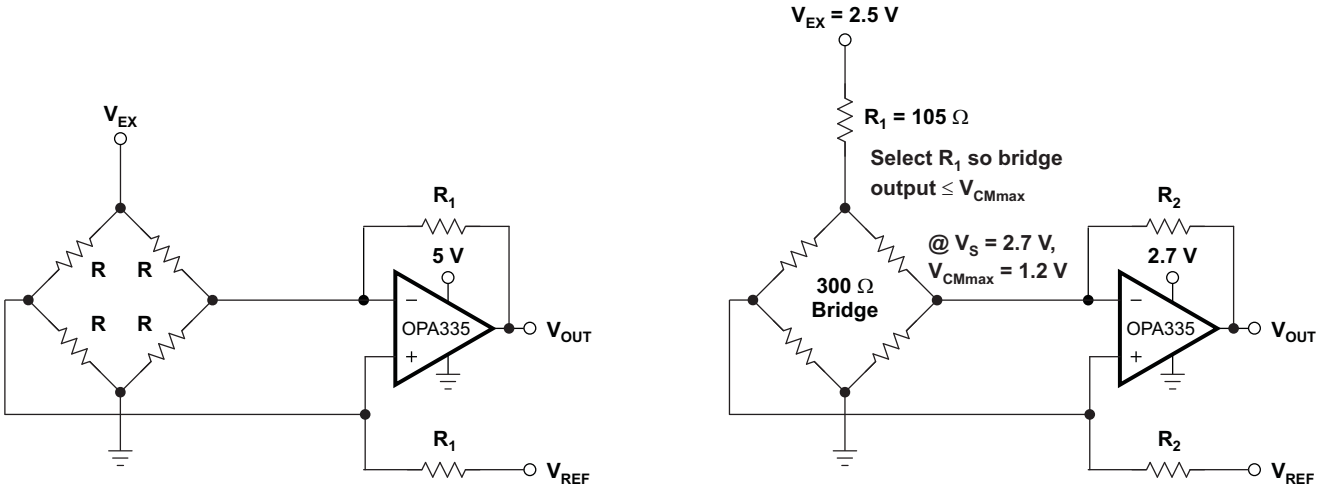


Figure 24. Auto-Zeroed Transimpedance Amplifier

APPLICATION INFORMATION (continued)

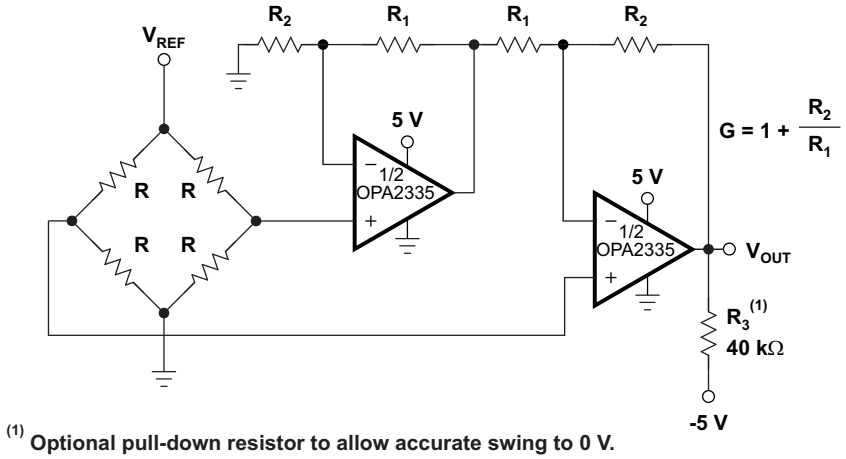


a. 5 V Supply Bridge Amplifier

b. 2.7 V Supply Bridge Amplifier

S0150-01

Figure 25. Single Op-Amp Bridge Amplifier Circuits



(1) Optional pull-down resistor to allow accurate swing to 0 V.

S0151-01

Figure 26. Dual Op-Amp IA Bridge Amplifier

APPLICATION INFORMATION (continued)

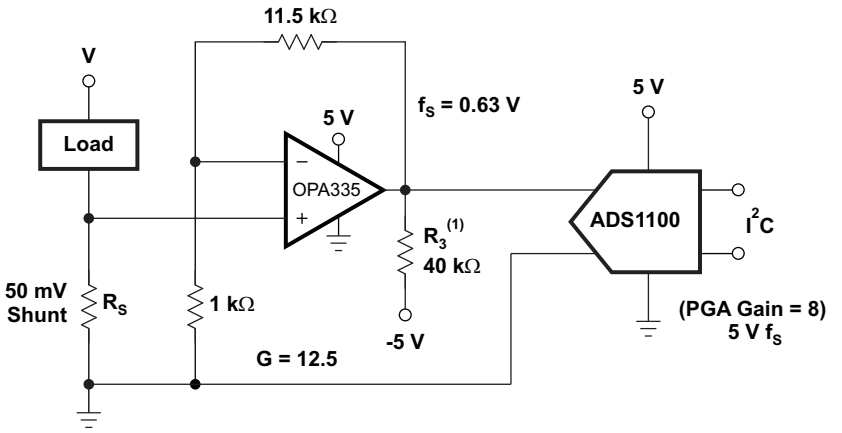


Figure 27. Low-Side Current Measurement

APPLICATION INFORMATION (continued)

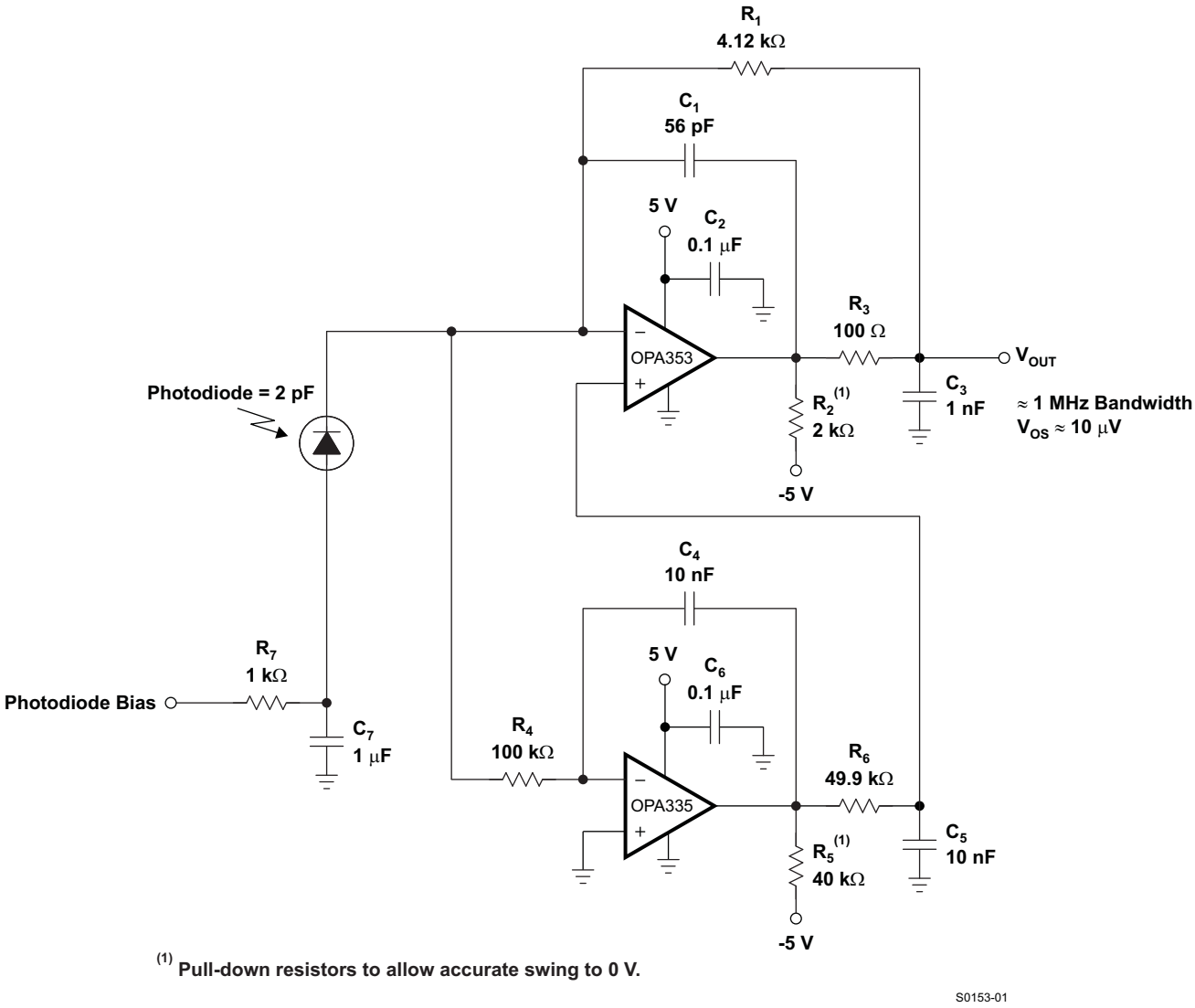
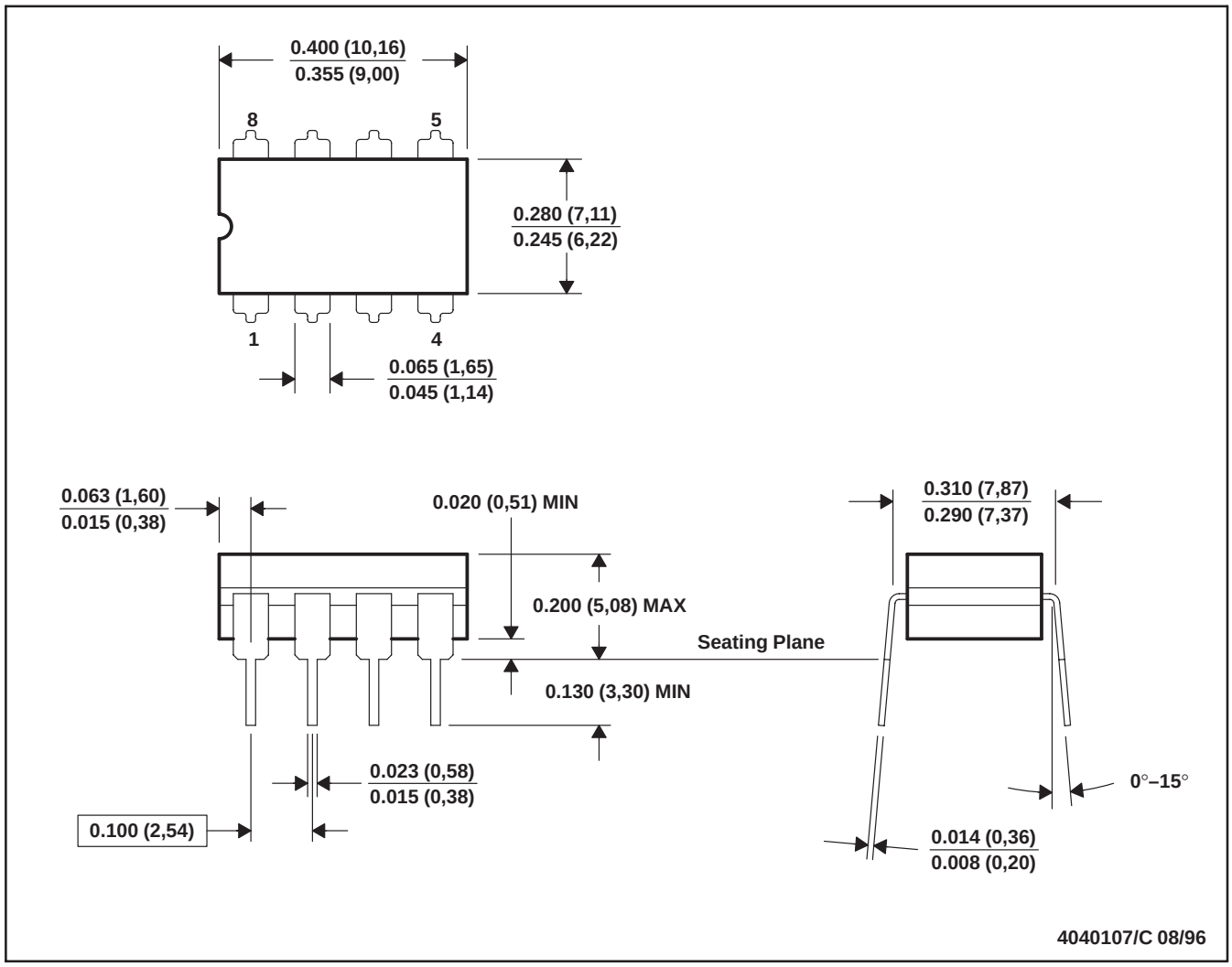


Figure 28. High Dynamic-Range Transimpedance Amplifier

MCER001A – JANUARY 1995 – REVISED JANUARY 1997

JG (R-GDIP-T8) **CERAMIC DUAL-IN-LINE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification.
E. Falls within MIL STD 1835 GDIP1-T8

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA2335AMJG	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	OPA2335AMJG

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF OPA2335M :

- Catalog : OPA2335

NOTE: Qualified Version Definitions:

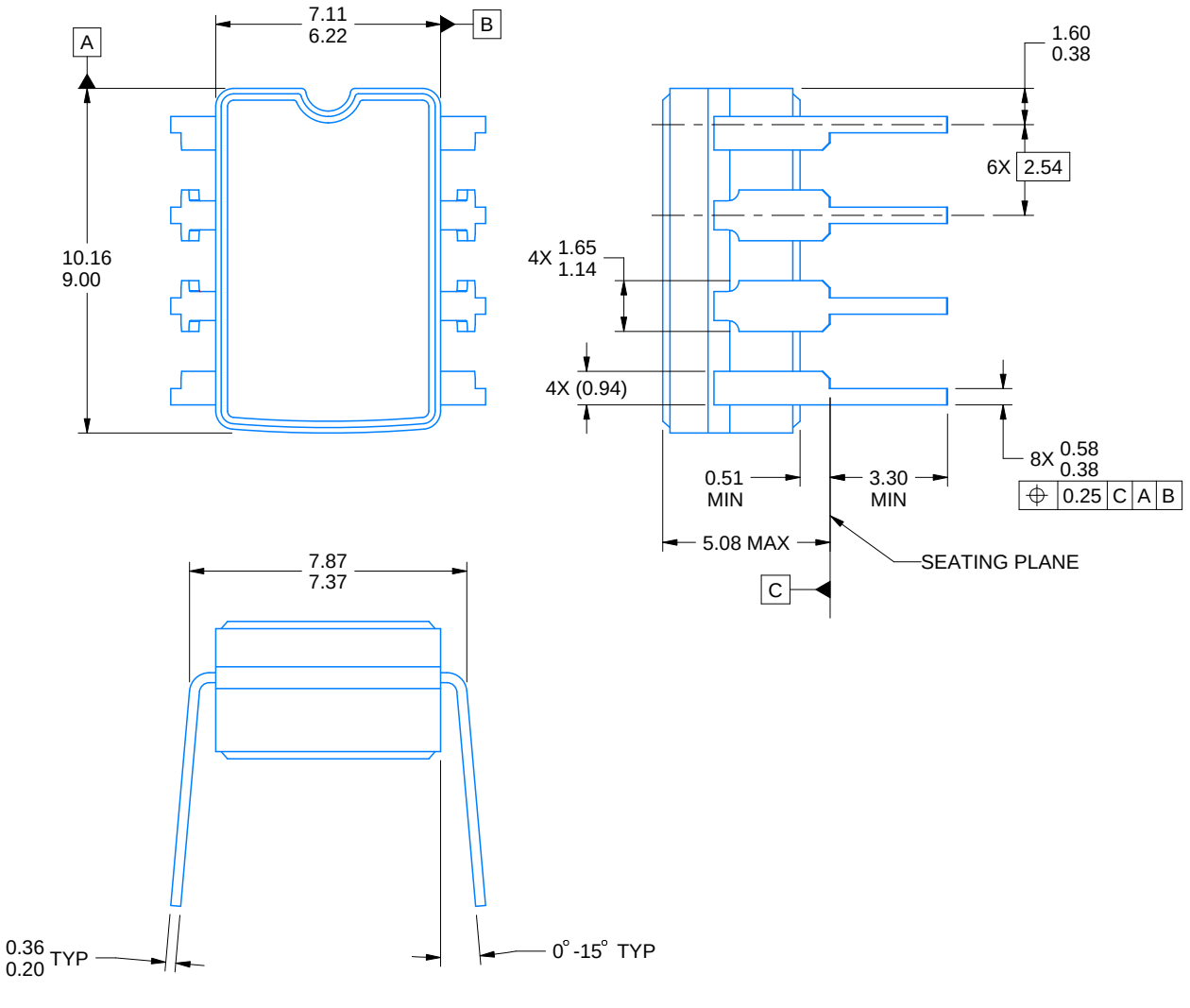
- Catalog - TI's standard catalog product

PACKAGE OUTLINE

JG0008A

CDIP - 5.08 mm max height

CERAMIC DUAL IN-LINE PACKAGE



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NOTES:

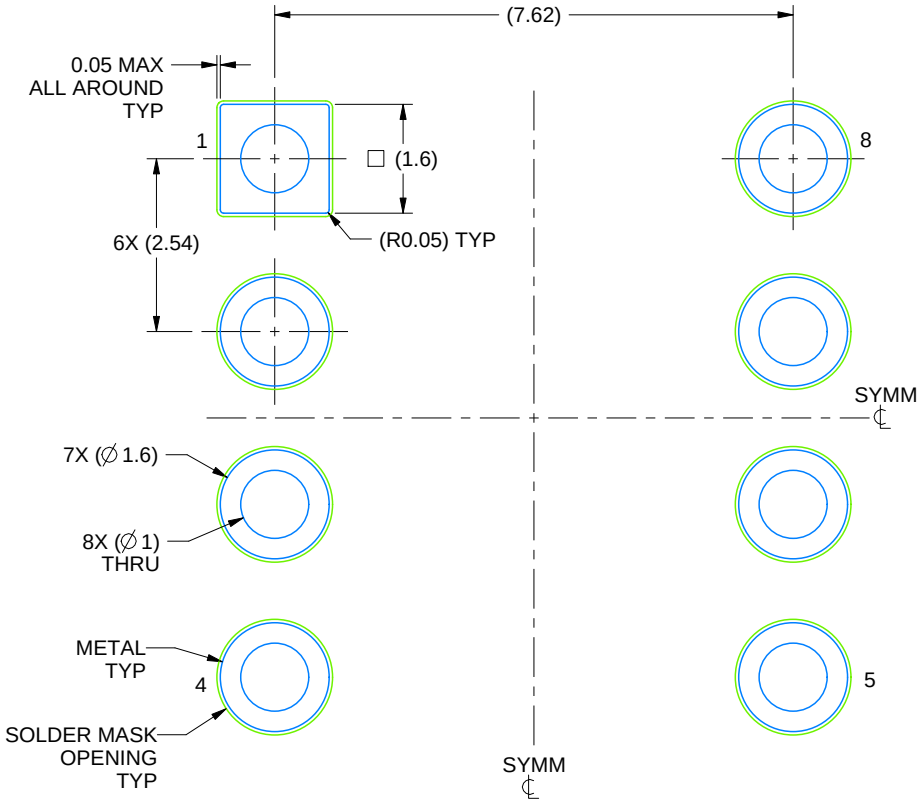
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package can be hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification.
5. Falls within MIL STD 1835 GDIP1-T8

EXAMPLE BOARD LAYOUT

JG0008A

CDIP - 5.08 mm max height

CERAMIC DUAL IN-LINE PACKAGE



LAND PATTERN EXAMPLE
NON SOLDER MASK DEFINED
SCALE: 9X

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Last updated 10/2025