OPAx316-Q1 10-MHz, Rail-to-Rail Input/Output, Low-Voltage, 1.8-V CMOS Operational Amplifier

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to +125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level 3A
  - Device CDM ESD Classification Level C5
- Unity-Gain Bandwidth: 10 MHz
- Low I_Q: 400 µA/ch
- Wide Supply Range: 1.8 V to 5.5 V
- Low Noise: 11 nV/$\sqrt{\text{Hz}}$ at 1 kHz
- Low Input Bias Current: ±5 pA
- Offset Voltage: ±0.5 mV
- Unity-Gain Stable
- Internal RFI-EMI Filter
- Extended Temperature Range: –40°C to +125°C

2 Applications

- Automotive Applications:
  - ADAS
  - Body Electronics and Lighting
  - Current Sensing
  - Battery Management Systems

3 Description

The OPAx316-Q1 family of single and dual operational amplifiers represents a new generation of general-purpose, low-power operational amplifiers. Featuring rail-to-rail input and output swings, low quiescent current (400 µA/ch typical) combined with a wide bandwidth of 10 MHz and very-low noise (11 nV/$\sqrt{\text{Hz}}$ at 1 kHz) makes this family suitable for circuits requiring a good speed and power ratio. The low input bias current supports those operational amplifiers for applications with megaohm source impedances. The low input bias current of the OPAx316-Q1 yields a very-low current noise to make the device attractive for high impedance sensor interfaces.

The robust design of the OPAx316-Q1 provides ease-of-use to the circuit designer: a unity-gain stable, integrated RFI and EMI rejection filter, no phase reversal in overdrive condition, and high electrostatic discharge (ESD) protection (4-kV HBM).

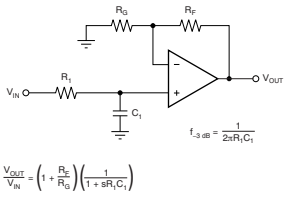
These devices are optimized for low-voltage operation as low as 1.8 V (±0.9 V) and up to 5.5 V (±2.75 V). This latest addition of low-voltage CMOS automotive grade operational amplifiers provide a family of wide bandwidth, low noise, and low power that meet the needs of a wide variety of applications.

Device Information(1)

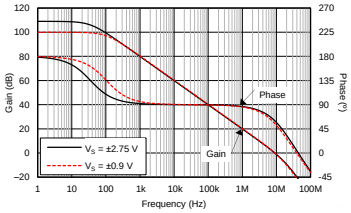
PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA316-Q1	SOT-23 (5)	1.60 mm × 2.90 mm
OPA2316-Q1	VSSOP (8)	3.00 mm × 3.00 mm
OPA4316-Q1	TSSOP (14)	4.40 mm × 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Single-Pole, Low-Pass Filter



Low-Supply Current (400 µA/ch) for 10-MHz Bandwidth



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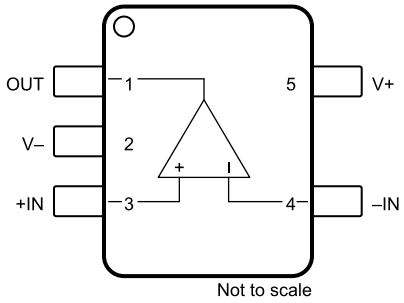
4 Revision History

Changes from Original (November 2016) to Revision A **Page**

- Changed CDM classification reduced from C6 ... 1
- Deleted OPA2316S-Q1 package and body size information from *Device Information* table ... 1
- Deleted SC70 (5) (OPA316-Q1), DFN (8), MSOP (8), SOIC (8) (OPA2316-Q1), and SOIC (14) packages (OPA4316-Q1) from the *Device Information* table, *Thermal Information* tables, and pinout diagrams ... 1
- Deleted OPA2316S-Q1 pin diagram and Pin Functions table in *Pin Configurations and Functions* section ... 3
- Deleted D (SOIC) package from OPA4316-Q1 pin diagram in Pin Configurations and Functions section ... 5
- Changed CDM rating from ±1500 V to ±750 V ... 6
- Deleted OPA2316S-Q1 device thermal information in the *Thermal Information* table ... 7
- Added thermal information for OPA4316-Q1 device ... 9
- Deleted the literature numbers in parentheses from the format of TI document references in the *Documentation Support* section ... 27

5 Pin Configuration and Functions

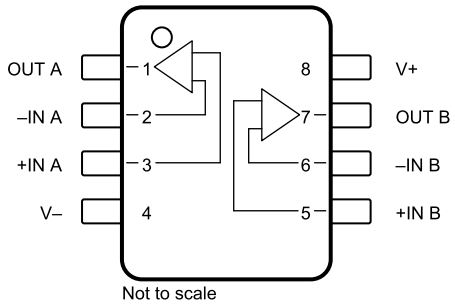
OPA316-Q1 DBV Package
5-Pin SOT-23
Top View



Pin Functions: OPA316-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
–IN	4	I	Inverting input
+IN	3	I	Noninverting input
V–	2	—	Negative supply or ground (for single-supply operation).
V+	5	—	Positive supply
OUT	1	O	Output

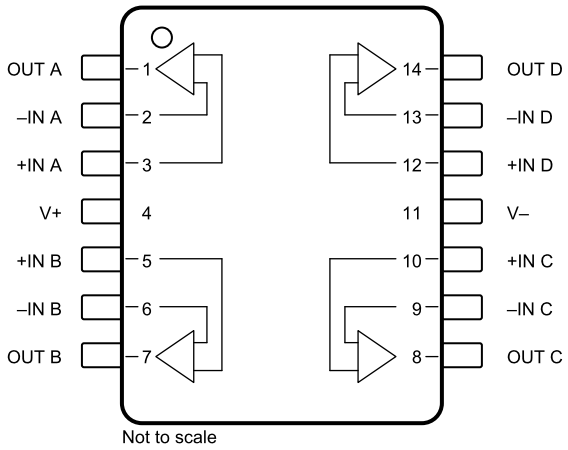
OPA2316-Q1 DGK Package
8-Pin VSSOP
Top View



Pin Functions: OPA2316-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
–IN A	2	I	Inverting input, channel A
+IN A	3	I	Noninverting input, channel A
–IN B	6	I	Inverting input, channel B
+IN B	5	I	Noninverting input, channel B
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
V–	4	—	Negative supply or ground (for single-supply operation).
V+	8	—	Positive supply

OPA4316-Q1 PW Package
14-Pin TSSOP
Top View



Not to scale

Pin Functions: OPA4316-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
–IN A	2	I	Inverting input, channel A
+IN A	3	I	Noninverting input, channel A
–IN B	6	I	Inverting input, channel B
+IN B	5	I	Noninverting input, channel B
–IN C	9	I	Inverting input, channel C
+IN C	10	I	Noninverting input, channel C
–IN D	13	I	Inverting input, channel D
+IN D	12	I	Noninverting input, channel D
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
OUT C	8	O	Output, channel C
OUT D	14	O	Output, channel D
V–	11	—	Negative supply or ground (for single-supply operation)
V+	4	—	Positive supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted)(1)

			MIN	MAX	UNIT
Supply voltage				7	V
Signal input pins	Voltage(2)	Common-mode	(V–) – 0.5	(V+) + 0.5	V
		Differential		(V+) – (V–) + 0.2	V
	Current(2)		–10	10	mA
Output short-circuit(3)			Continuous		
T_A	Operating temperature		–55	150	°C
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input pins are diode-clamped to the power-supply rails. Current limit input signals that can swing more than 0.5 V beyond the supply rails to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±4000	V
		Charged-device model (CDM), per AEC Q100-011	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_S	Supply voltage	1.8	5.5	V
	Specified temperature	–40	125	°C

6.4 Thermal Information: OPA316-Q1

THERMAL METRIC[1]		OPA316-Q1 DBV (SOT-23) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance[2]	221.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance[3]	144.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance[4]	49.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter[5]	26.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter[6]	49	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance[7]	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

6.5 Thermal Information: OPA2316-Q1

THERMAL METRIC[1]		OPA2316-Q1	UNIT
		DGK (VSSOP)	
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance[2]	186.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance[3]	78.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance[4]	107.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter[5]	15.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter[6]	106.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance[7]	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

6.6 Thermal Information: OPA4316-Q1

THERMAL METRIC[1]		OPA4316-Q1	UNIT
		PW (TSSOP)	
		14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance[2]	117.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance[3]	46.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance[4]	58.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter[5]	4.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter[6]	58.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance[7]	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

6.7 Electrical Characteristics

V_S (total supply voltage) = (V+) – (V–) = 1.8 V to 5.5 V.
at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	V_S = 5 V		±0.5	±2.5	mV
		V_S = 5 V, T_A = –40°C to 125°C			±3.5	mV
dV_{OS}/dT	Drift	V_S = 5 V, T_A = –40°C to 125°C		±2	±10	µV/°C
PSRR	vs power supply	V_S = 1.8 V – 5.5 V, V_{CM} = (V–)		±30	±150	µV/V
		V_S = 1.8 V – 5.5 V, V_{CM} = (V–), T_A = –40°C to 125°C			±250	µV/V
	Channel separation, dc	At dc		10		µV/V
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage	V_S = 1.8 V to 2.5 V	(V–) – 0.2		(V+)	V
		V_S = 2.5 V to 5.5 V	(V–) – 0.2		(V+) + 0.2	V
CMRR	Common-mode rejection ratio	V_S = 1.8 V, (V–) – 0.2 V < V_{CM} < (V+) – 1.4 V, T_A= –40°C to 125°C	70	86		dB
		V_S = 5.5 V, (V–) – 0.2 V < V_{CM} < (V+) – 1.4 V, T_A= –40°C to 125°C	76	90		dB
		V_S = 1.8 V, V_{CM} = –0.2 V to 1.8 V, T_A= –40°C to 125°C	57	72		dB
		V_S = 5.5 V, V_{CM} = –0.2 V to 5.7 V, T_A= –40°C to 125°C	65	80		dB
INPUT BIAS CURRENT						
I_B	Input bias current			±5	±15	pA
		T_A= –40°C to 125°C			±15	nA
I_{OS}	Input offset current			±2	±15	pA
		T_A= –40°C to 125°C			±8	nA
NOISE						
E_n	Input voltage noise (peak-to-peak)	V_S = 5 V, f = 0.1 Hz to 10 Hz		3		μV_{PP}
e_n	Input voltage noise density	V_S = 5 V, f = 1 kHz		11		nV/√Hz
i_n	Input current noise density	f = 1 kHz		1.3		fA/√Hz
INPUT IMPEDANCE						
Z_{ID}	Differential			2 || 2		$10^{16}\Omega$ || pF
Z_{IC}	Common-mode			2 || 4		$10^{11}\Omega$ || pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	V_S = 1.8 V, (V–) + 0.04 V < V_O < (V+) – 0.04 V, R_L = 10 kΩ	94	100		dB
		V_S = 5.5 V, (V–) + 0.05 V < V_O < (V+) – 0.05 V, R_L = 10 kΩ	104	110		dB
		V_S = 1.8 V, (V–) + 0.1 V < V_O < (V+) – 0.1 V, R_L = 2 kΩ	90	96		dB
		V_S = 5.5 V, (V–) + 0.15 V < V_O < (V+) – 0.15 V, R_L = 2 kΩ	100	106		dB
		V_S = 5.5 V, (V–) + 0.05 V < V_O < (V+) – 0.05 V, R_L = 10 kΩ, T_A= –40°C to 125°C	86			dB
		V_S = 5.5 V, (V–) + 0.15 V < V_O < (V+) – 0.15 V, R_L = 2 kΩ, T_A= –40°C to 125°C	84			dB
FREQUENCY RESPONSE						
GBP	Gain bandwidth product	V_S = 5 V, G = 1		10		MHz
φ_m	Phase margin	V_S = 5 V, G = 1		60		Degrees
SR	Slew rate	V_S = 5 V, G = 1		6		V/µs
t_S	Settling time	To 0.1%, V_S = 5 V, 2-V step , G = 1, C_L = 100 pF		1		µs
		To 0.01%, V_S = 5 V, 2-V step , G = 1, C_L = 100 pF		1.66		µs
t_{OR}	Overload recovery time	V_S = 5 V, V_{IN} × gain = V_S		0.3		µs
THD + N	Total harmonic distortion + noise(1)	V_S = 5 V, V_O = 0.5 V_{RMS}, G = 1 f = 1 kHz		0.0008%		

(1) Third-order filter; bandwidth = 80 kHz at –3 dB.

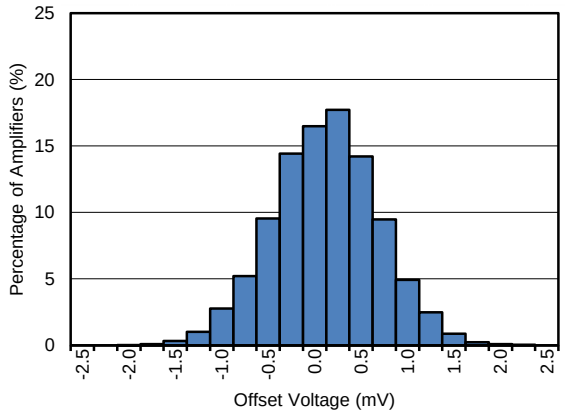
Electrical Characteristics (continued)

V_S (total supply voltage) = (V+) – (V–) = 1.8 V to 5.5 V.
at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
V_O	Voltage output swing from supply rails	V_S = 1.8 V, R_L = 10 kΩ, T_A= –40°C to 125°C			15	mV
		V_S = 5.5 V, R_L = 10 kΩ, T_A= –40°C to 125°C			30	mV
		V_S = 1.8 V, R_L = 2 kΩ, T_A= –40°C to 125°C			60	mV
		V_S = 5.5 V, R_L = 2 kΩ, T_A= –40°C to 125°C			120	mV
I_{SC}	Short-circuit current	V_S = 5 V		±50		mA
Z_O	Open-loop output impedance	V_S = 5 V, f = 10 MHz		250		Ω
POWER SUPPLY						
V_S	Specified voltage		1.8		5.5	V
I_Q	Quiescent current per amplifier	V_S = 5 V, I_O = 0 mA, T_A= –40°C to 125°C		400	500	µA
	Power-on time	V_S = 0 V to 5.5 V		200		µs

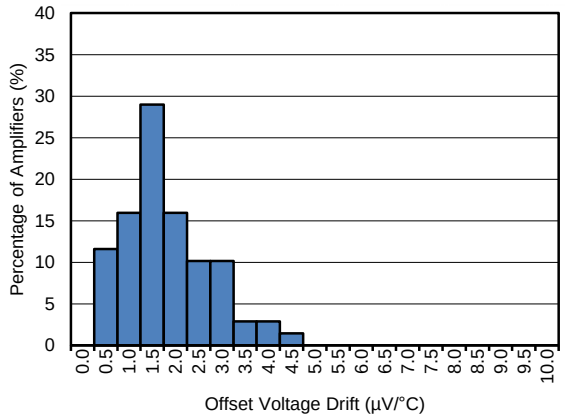
6.8 Typical Characteristics

at T_A = 25°C, V_S = 5.5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.



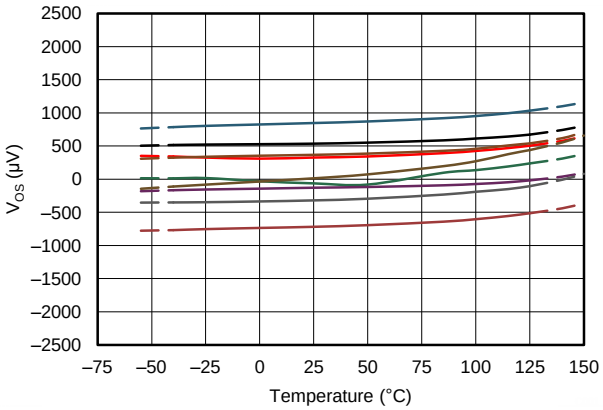
Distribution taken from 12551 amplifiers

Figure 1. Offset Voltage Production Distribution



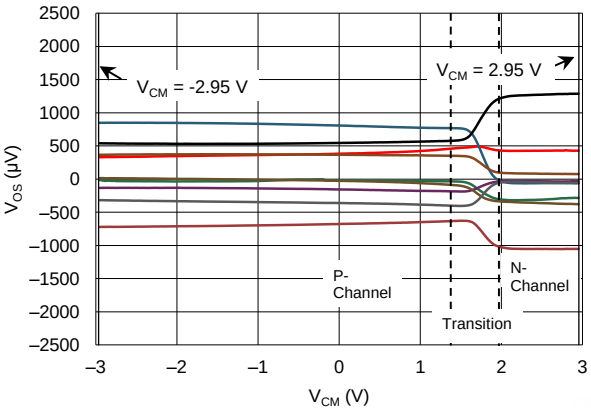
T_A = –40°C to +125°C, Distribution taken from 70 amplifiers

Figure 2. Offset Voltage Drift Distribution



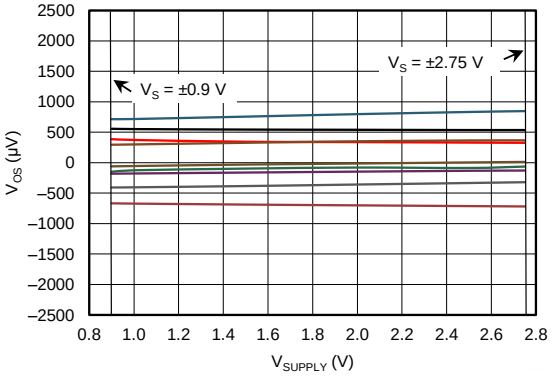
9 typical units shown

Figure 3. Offset Voltage vs Temperature



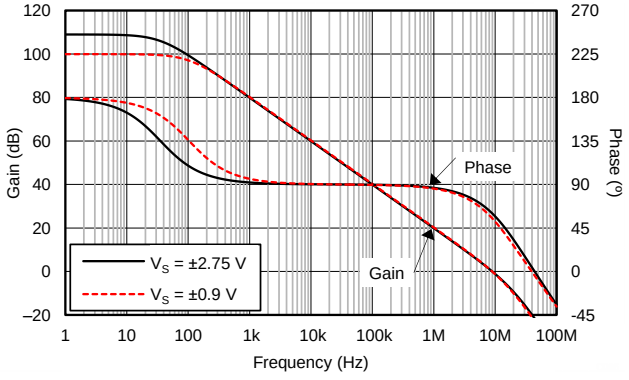
V+ = 2.75 V, V– = –2.75 V, 9 typical units shown

Figure 4. Offset Voltage vs Common-Mode Voltage



V+ = 0.9 V to 2.75 V, V– = –0.9 V to –2.75 V,
9 typical units shown

Figure 5. Offset Voltage vs Power Supply



V_{CM} < (V+) – 1.4 V

Figure 6. Open-Loop Gain and Phase vs Frequency

Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.

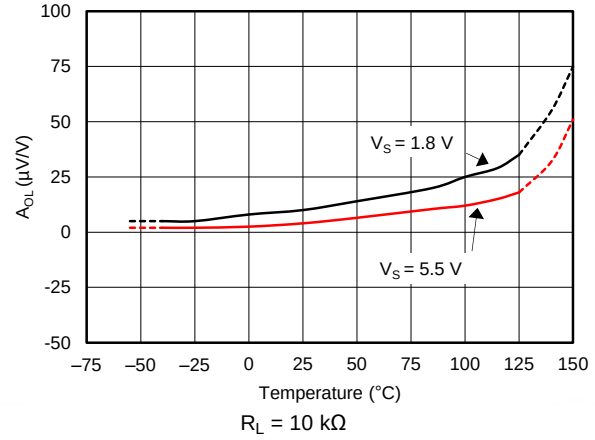


Figure 7. Open-Loop Gain vs Temperature

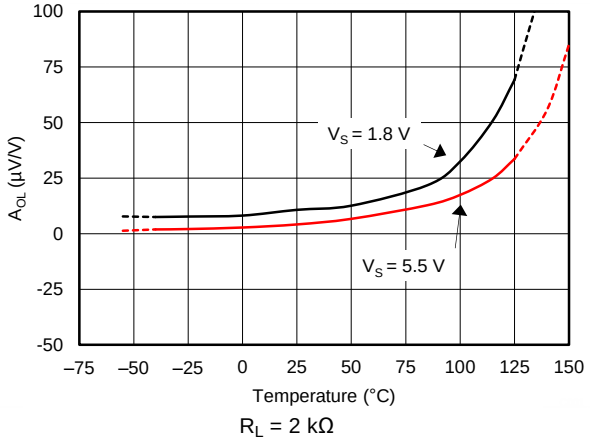


Figure 8. Open-Loop Gain vs Temperature

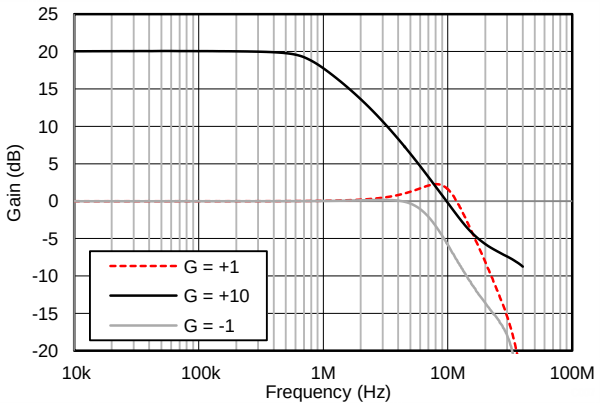


Figure 9. Closed-Loop Gain vs Frequency

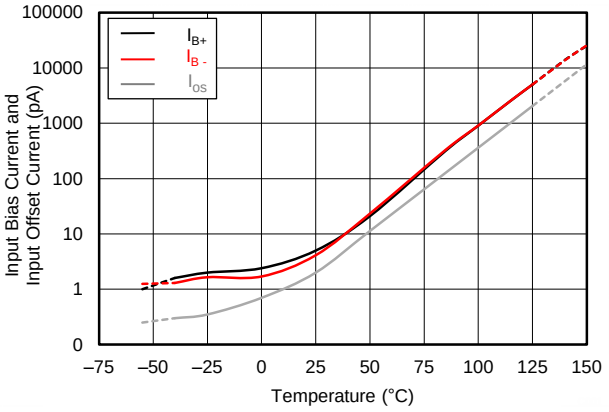


Figure 10. Input Bias and Offset Current vs Temperature

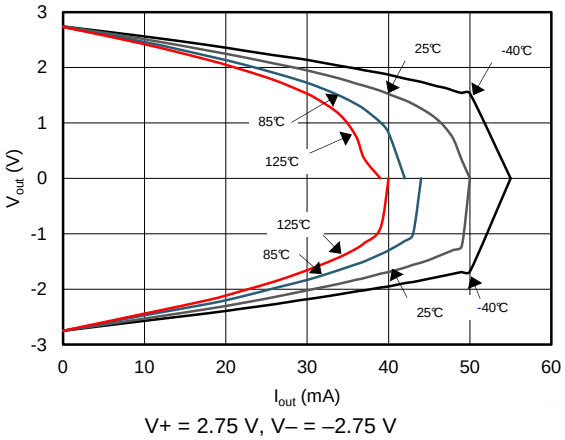


Figure 11. Output Voltage Swing vs Output Current

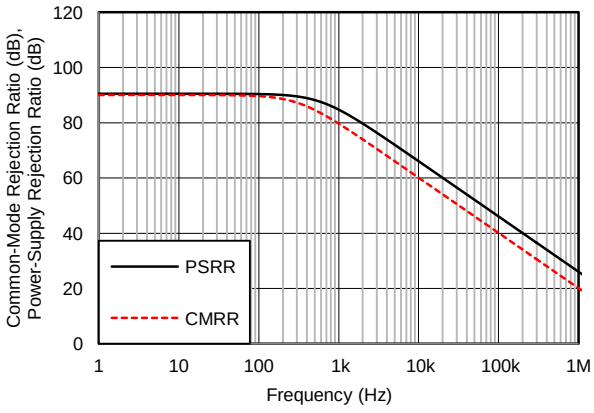


Figure 12. CMRR and PSRR vs Frequency (Referred to Input)

Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.

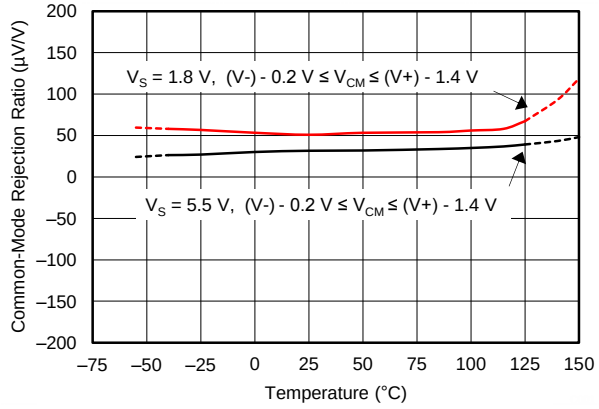


Figure 13. CMRR vs Temperature (Narrow Range)

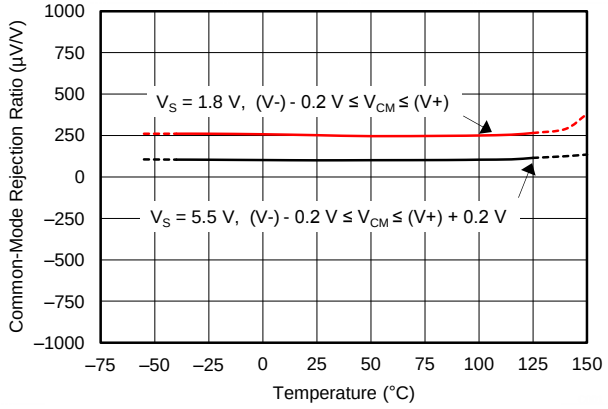


Figure 14. CMRR vs Temperature (Wide Range)

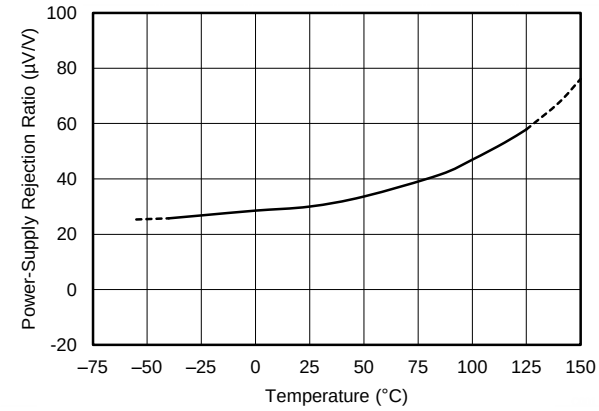


Figure 15. PSRR vs Temperature

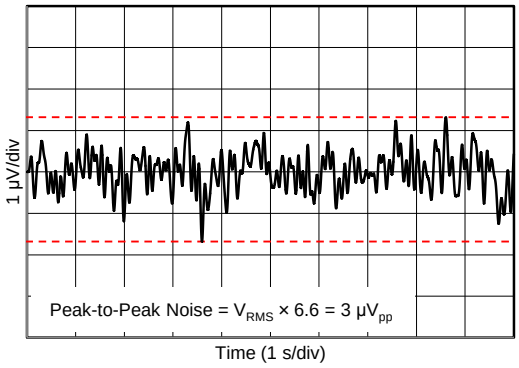


Figure 16. 0.1-Hz to 10-Hz Input Voltage Noise

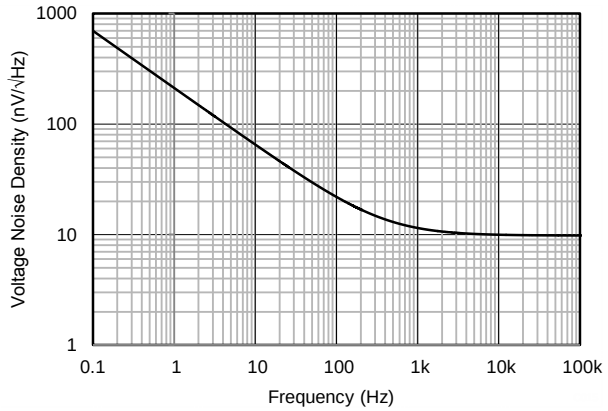


Figure 17. Input Voltage Noise Spectral Density vs Frequency

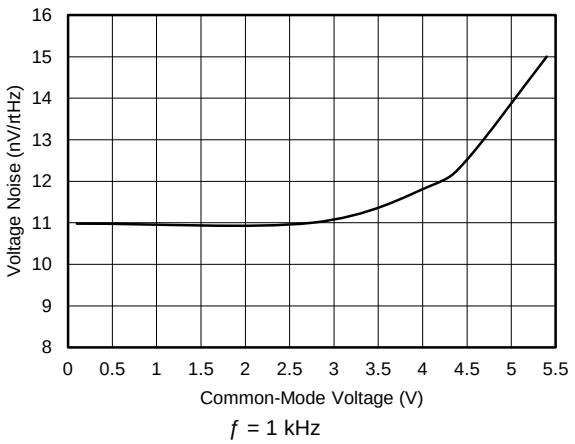
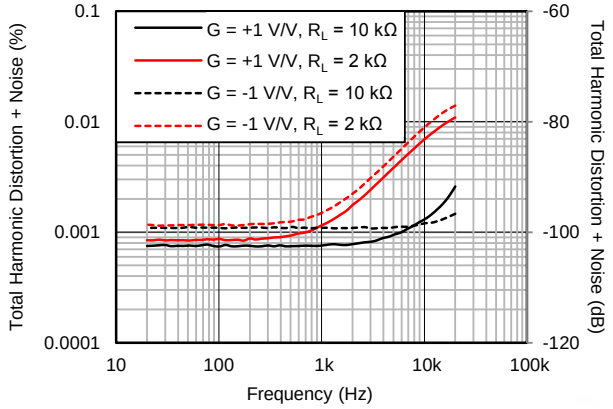


Figure 18. Input Voltage Noise vs Common-Mode Voltage

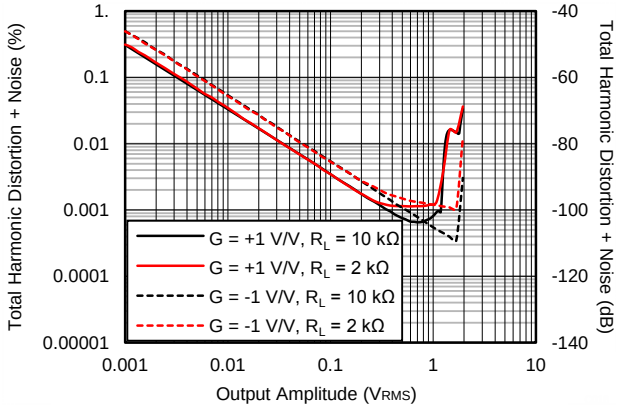
Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.



Bandwidth = 80 kHz, V_{OUT} = 0.5 V_{RMS}

Figure 19. THD + N vs Frequency



f = 1 kHz, Bandwidth = 80 kHz

Figure 20. THD + N vs Amplitude

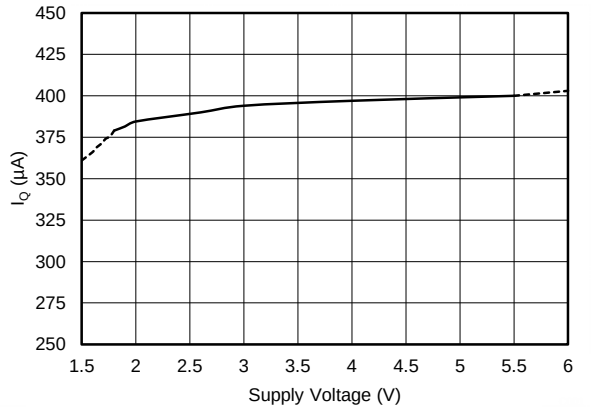


Figure 21. Quiescent Current vs Supply Voltage

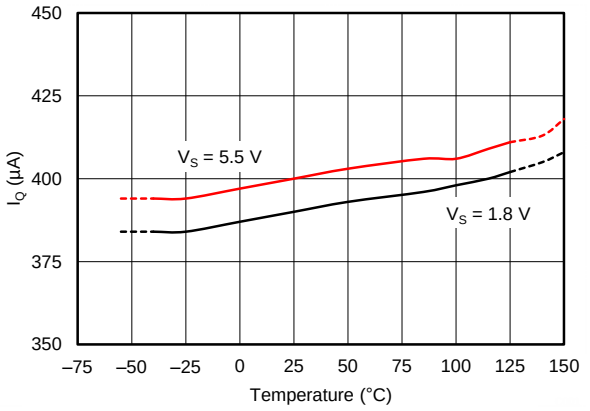


Figure 22. Quiescent Current vs Temperature

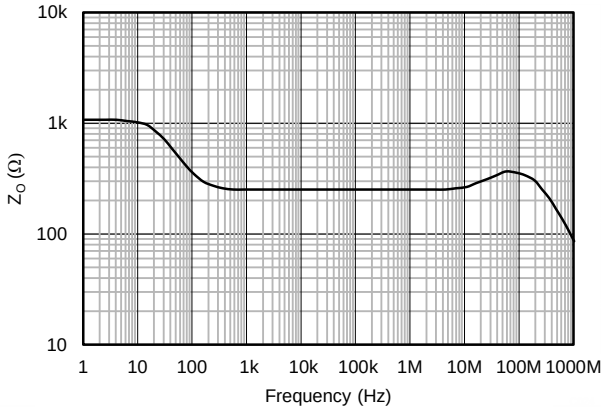
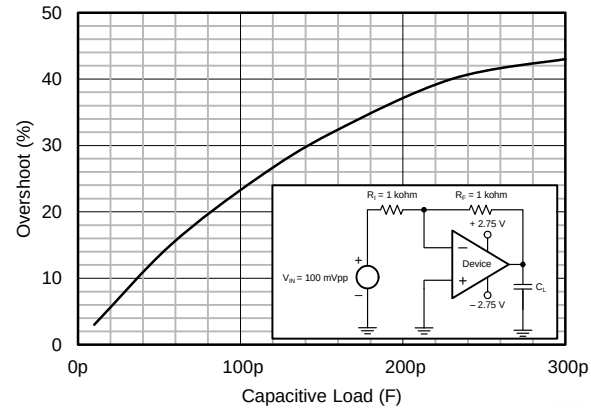


Figure 23. Open-Loop Output Impedance vs Frequency

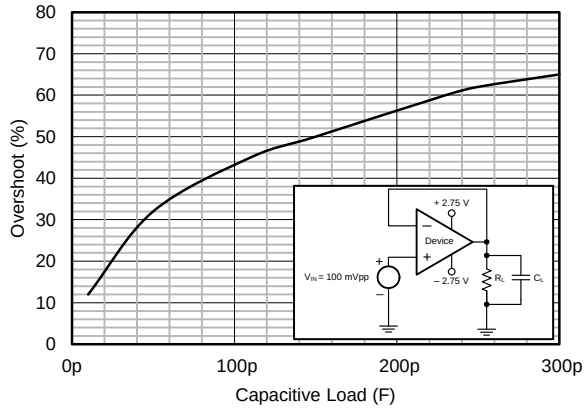


V+ = 2.75 V V– = –2.75 V G = –1 V/V

Figure 24. Small-Signal Overshoot vs Load Capacitance

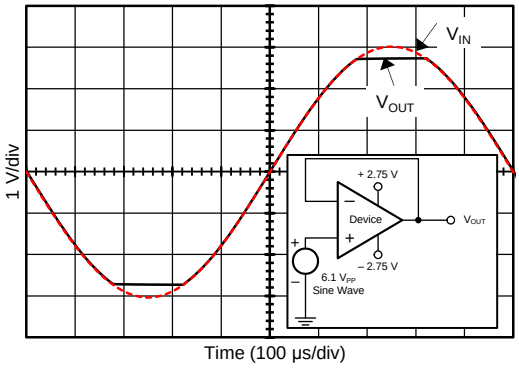
Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.



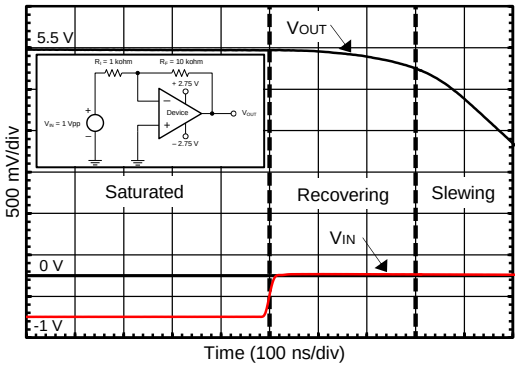
V+ = 2.75 V G = +1 V/V R_L = 1 kΩ
V– = –2.75 V

Figure 25. Small-Signal Overshoot vs Load Capacitance



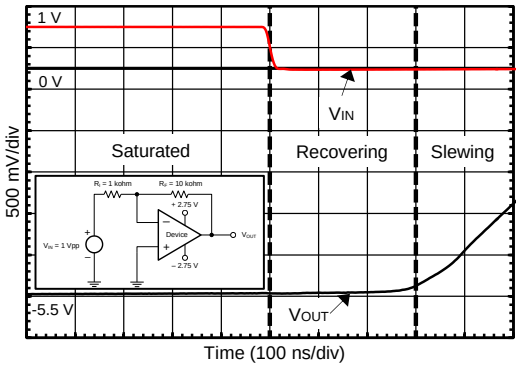
V+ = 2.75 V V– = –2.75 V

Figure 26. No Phase Reversal



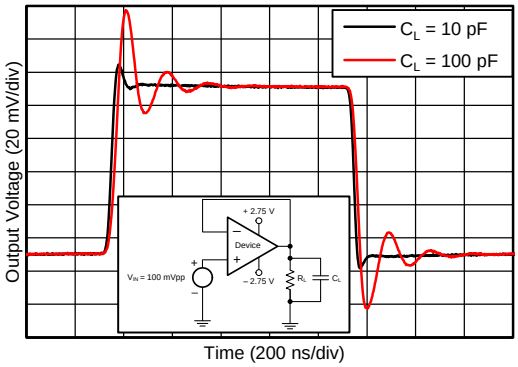
V+ = 2.75 V V– = –2.75 V G = –10 V/V

Figure 27. Positive Overload Recovery



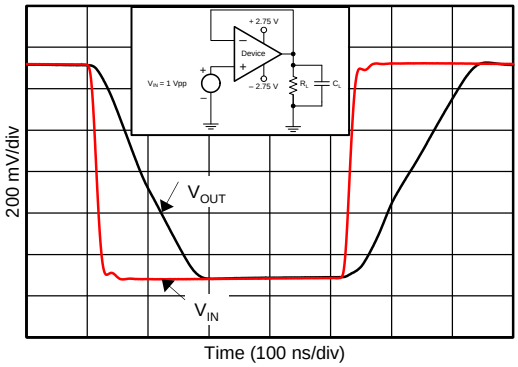
V+ = 2.75 V V– = –2.75 V G = –10 V/V

Figure 28. Negative Overload Recovery



V+ = 2.75 V V– = –2.75 V G = +1 V/V

Figure 29. Small-Signal Step Response

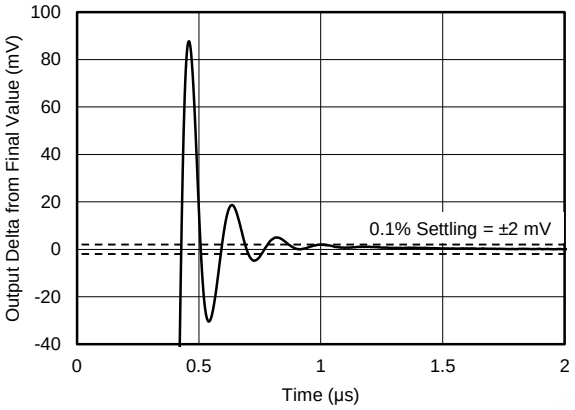


V+ = 2.75 V C_L = 100 pF G = +1 V/V
V– = –2.75 V

Figure 30. Large-Signal Step Response

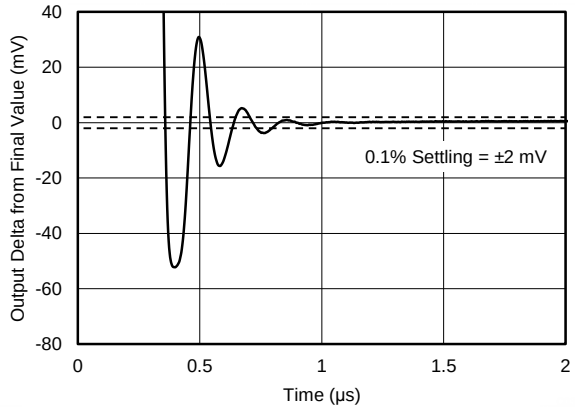
Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.



C_L = 100 pF G = +1 V/V

Figure 31. Positive Large-Signal Settling Time



C_L = 100 pF G = +1 V/V

Figure 32. Negative Large-Signal Settling Time

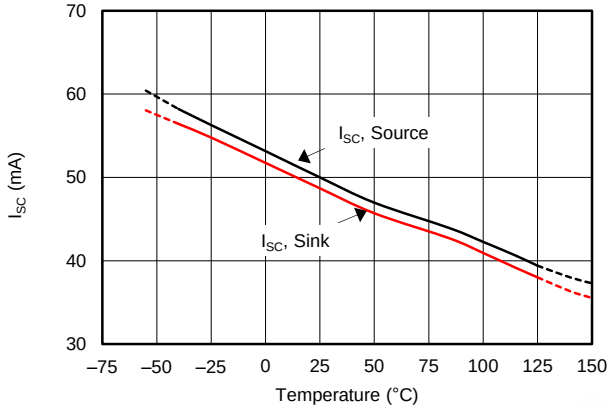


Figure 33. Short-Circuit Current vs Temperature

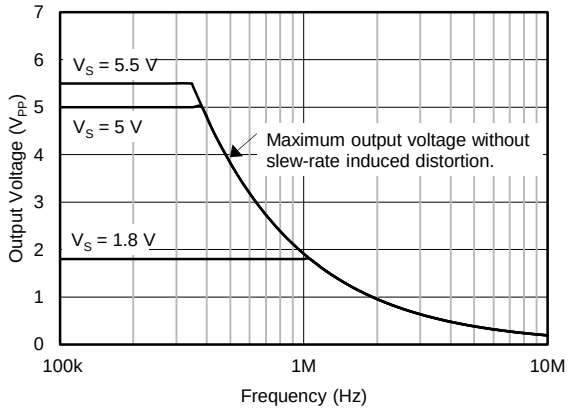
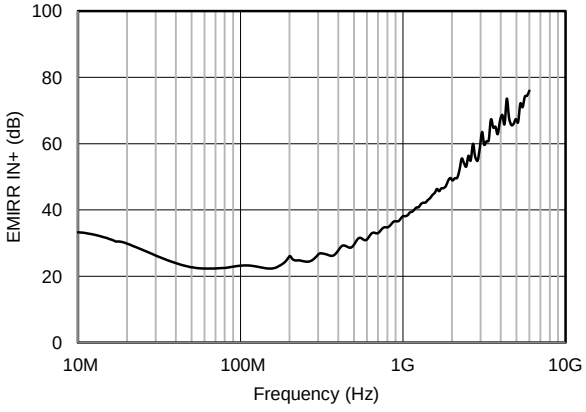
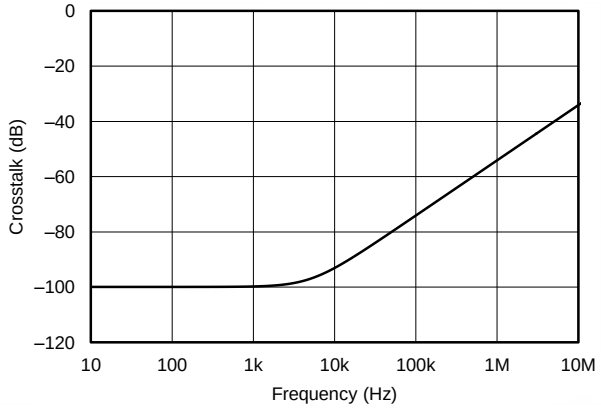


Figure 34. Maximum Output Voltage vs Frequency and Supply Voltage



P_{RF} = –10 dBm

Figure 35. Electromagnetic Interference Rejection Ratio Referred to Noninverting Input (EMIRR IN+) vs Frequency



V+ = 2.75 V, V– = –2.75 V

Figure 36. Channel Separation vs Frequency

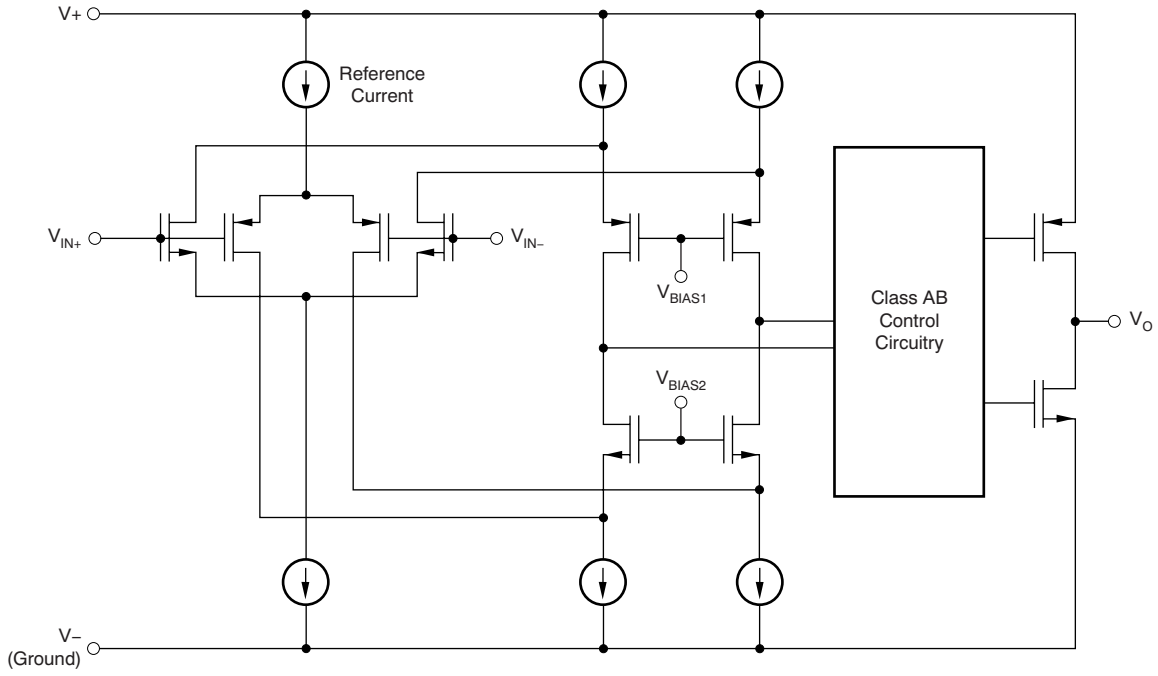
7 Detailed Description

7.1 Overview

The OPAx316-Q1 is a family of low-power, rail-to-rail input and output operational amplifiers. These devices operate from 1.8 V to 5.5 V, are unity-gain stable, and are suitable for a wide range of general-purpose applications. The class AB output stage is capable of driving less than or equal to 10-kΩ loads connected to any point between V+ and ground. The input common-mode voltage range includes both rails and allows the OPAx316-Q1 series to be used in virtually any single-supply application. Rail-to-rail input and output swing significantly increases dynamic range, especially in low-supply applications, and makes them suitable for driving sampling analog-to-digital converters (ADCs).

The OPAx316-Q1 family features 10-MHz bandwidth and 6-V/μs slew rate with only 400-μA supply current per channel, providing good ac performance at very-low-power consumption. DC applications are well served with a very-low input noise voltage of 11 nV/√Hz at 1 kHz, low input bias current (5 pA), and a typical input offset voltage of 0.5-mV.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Operating Voltage

The OPAx316-Q1 operational amplifiers are fully specified and ensured for operation from 1.8 V to 5.5 V. In addition, many specifications apply from –40°C to +125°C. Parameters that vary significantly with operating voltages or temperature are illustrated in the *Typical Characteristics* graphs.

Feature Description (continued)

7.3.2 Rail-to-Rail Input

The input common-mode voltage range of the OPAx316-Q1 series extends 200 mV beyond the supply rails for supply voltages greater than 2.5 V. This performance is achieved with a complementary input stage: an N-channel input differential pair in parallel with a P-channel differential pair, as shown in the *Functional Block Diagram*. The N-channel pair is active for input voltages close to the positive rail, typically (V+) – 1.4 V to 200 mV above the positive supply, whereas the P-channel pair is active for inputs from 200 mV below the negative supply to approximately (V+) – 1.4 V. There is a small transition region, typically (V+) – 1.2 V to (V+) – 1 V, in which both pairs are on. This 200-mV transition region can vary up to 200 mV with process variation. Thus, the transition region (both stages on) can range from (V+) – 1.4 V to (V+) – 1.2 V on the low end, up to (V+) – 1 V to (V+) – 0.8 V on the high end. Within this transition region, PSRR, CMRR, offset voltage, offset drift, and THD can degrade compared to device operation outside this region.

7.3.3 Input and ESD Protection

The OPAx316-Q1 incorporates internal ESD protection circuits on all pins. In the case of input and output pins, this protection primarily consists of current-steering diodes connected between the input and power-supply pins. These ESD protection diodes provide in-circuit, input overdrive protection, as long as the current is limited to 10 mA, as stated in *Absolute Maximum Ratings* table. Figure 37 shows how a series input resistor can be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and the value must be kept to a minimum in noise-sensitive applications.

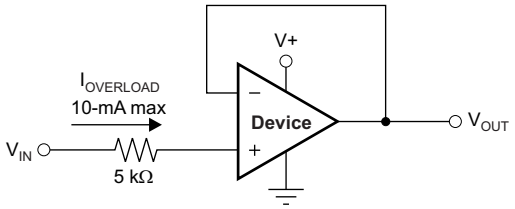


Figure 37. Input Current Protection

7.3.4 Common-Mode Rejection Ratio (CMRR)

CMRR for the OPAx316-Q1 is specified in several ways so the user can select the best match for a given application, as shown in the *Electrical Characteristics* table. First, the data sheet gives the CMRR of the device in the common-mode range below the transition region [V_{CM} < (V+) – 1.4 V]. This specification is the best indicator of device capability when the application requires use of one of the differential input pairs. Second, the CMRR over the entire common-mode range is specified at V_{CM} = –0.2 V to 5.7 V for V_S = 5.5 V. This last value includes the variations shown in Figure 4 through the transition region.

7.3.5 EMI Susceptibility and Input Filtering

Operational amplifiers vary with regard to the susceptibility of the device to electromagnetic interference (EMI). If conducted EMI enters the operational amplifier, the dc offset observed at the amplifier output can shift from the nominal value when EMI is present. This shift is a result of signal rectification associated with the internal semiconductor junctions. Although EMI can affect all operational amplifier pin functions, the signal input pins are likely to be the most susceptible. The OPA316-Q1 operational amplifier family incorporates an internal input low-pass filter that reduces the amplifier response to EMI. This filter provides both common-mode and differential-mode filtering. The filter is designed for a cutoff frequency of approximately 80 MHz (–3 dB), with a roll-off of 20 dB per decade.

TI developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. The EMI rejection ratio (EMIRR) metric allows operational amplifiers to be directly compared by the EMI immunity. Figure 35 illustrates the testing results on the OPAx316-Q1. For more information, see *EMI Rejection Ratio of Operational Amplifiers*.

Feature Description (continued)

7.3.6 Rail-to-Rail Output

Designed as a low-power, low-noise operational amplifier, the OPAx316-Q1 delivers a robust output drive capability. A class AB output stage with common-source transistors achieves full rail-to-rail output swing capability. For resistive loads of 10-kΩ, the output swings typically to within 30 mV of either supply rail regardless of the power-supply voltage applied. Different load conditions change the ability of the amplifier to swing close to the rails; see Figure 11.

7.3.7 Capacitive Load and Stability

The OPAx316-Q1 is designed for applications where driving a capacitive load is required. As with all operational amplifiers, there may be specific instances where the OPAx316-Q1 can become unstable. The particular operational amplifier circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether or not an amplifier is stable in operation. An operational amplifier in the unity-gain (1 V/V) buffer configuration that drives a capacitive load exhibits a greater tendency to be unstable than an amplifier operated at a higher noise gain. The capacitive load, in conjunction with the operational amplifier output resistance, creates a pole within the feedback loop that degrades the phase margin. The degradation of the phase margin increases as the capacitive loading increases. As a conservative best practice, designing for 25% overshoot (40° phase margin) provides improved stability over process variations. The equivalent series resistance (ESR) of some very-large capacitors (C_L with a value greater than 1 μF) is sufficient to alter the phase characteristics in the feedback loop such that the amplifier remains stable. Increasing the amplifier closed-loop gain allows the amplifier to drive increasingly larger capacitance. This increased capability is evident when observing the overshoot response of the amplifier at higher voltage gains. See Figure 24 (G = –1 V/V) and Figure 25 (G = 1 V/V).

Inserting a small resistor (typically 10-Ω to 20-Ω) can increase the capacitive load capability of the amplifier in a unity-gain configuration, as shown in Figure 38. This resistor significantly reduces the overshoot and ringing associated with large capacitive loads. One possible problem with this technique, however, is that a voltage divider is created with the added series resistor and any resistor connected in parallel with the capacitive load. The voltage divider introduces a gain error at the output that reduces the output swing.

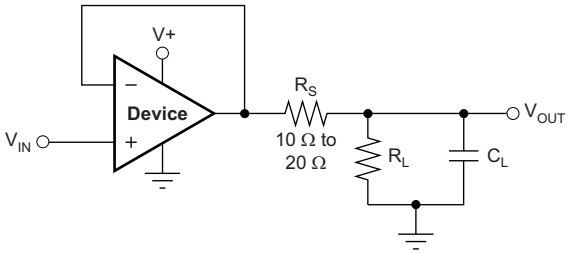


Figure 38. Improving Capacitive Load Drive

7.3.8 Overload Recovery

Overload recovery is defined as the time required for the operational amplifier output to recover from a saturated state to a linear state. The output devices of the operational amplifier enter a saturation region when the output voltage exceeds the rated operating voltage, either because of the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return back to the linear state. After the charge carriers return back to the linear state, the device begins to slew at the specified slew rate. Thus, the propagation delay in case of an overload condition is the sum of the overload recovery time and the slew time. The overload recovery time for the OPAx316-Q1 is approximately 300 ns.

7.4 Device Functional Modes

The OPAx316-Q1 devices are powered on when the supply is connected. The devices can operate as a single-supply operational amplifier or a dual-supply amplifier, depending on the application.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 General Configurations

When receiving low-level signals, the device often requires limiting the bandwidth of the incoming signals into the system. The simplest way to establish this limited bandwidth is to place an RC filter at the noninverting pin of the amplifier, as Figure 39 shows.

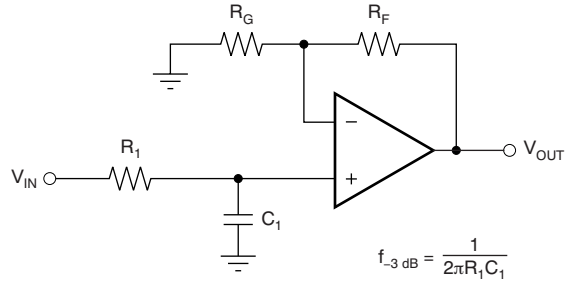


Figure 39. Single-Pole Low-Pass Filter

If even more attenuation is needed, the device requires a multiple-pole filter. The Sallen-Key filter can be used for this task, as Figure 40 shows. For best results, the amplifier must have a bandwidth that is eight to 10 times the filter frequency bandwidth. Failure to follow this guideline can result in phase shift of the amplifier.

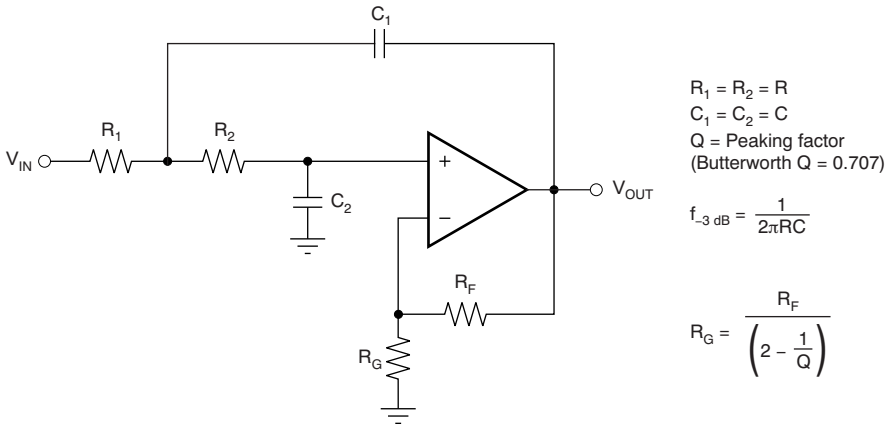


Figure 40. Two-Pole, Low-Pass, Sallen-Key Filter

8.2 Typical Application

Some applications require differential signals. Figure 41 shows a simple circuit to convert a single-ended input of 0.1 V to 2.4 V into a differential output of ±2.3 V on a single 2.7-V supply. The output range is intentionally limited to maximize linearity. The circuit is composed of two amplifiers. One amplifier functions as a buffer and creates a voltage (V_{OUT+}). The second amplifier inverts the input and adds a reference voltage to generate $V_{OUT–}$. V_{OUT+} and $V_{OUT–}$ range from 0.1 V to 2.4 V. The difference (V_{DIFF}) is the difference between V_{OUT+} and $V_{OUT–}$, resulting in a differential output voltage range of 2.3 V.

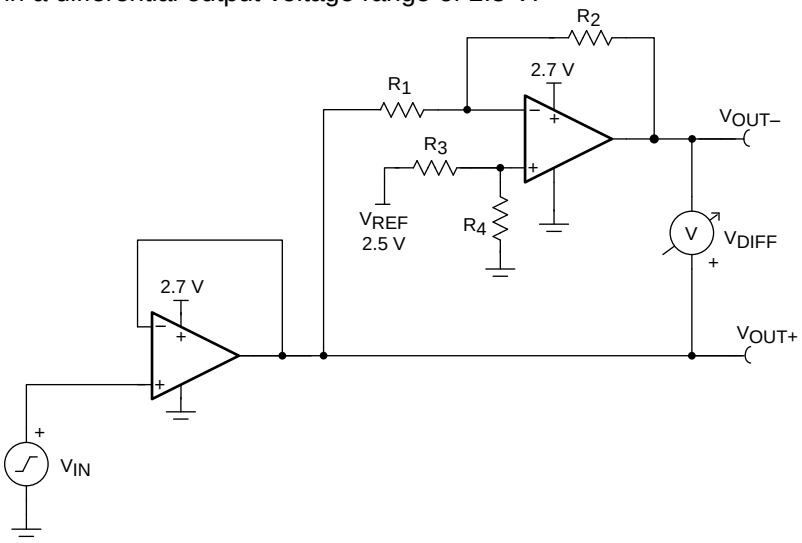


Figure 41. Schematic for a Single-Ended Input to Differential Output Conversion

8.2.1 Design Requirements

Table 1 lists the design requirements:

Table 1. Design Parameters

DESIGN PARAMETER	VALUE
Supply voltage	2.7 V
Reference voltage	2.5 V
Input voltage	0.1 V to 2.4 V
Output differential voltage	±2.3 V
Output common-mode voltage	1.25 V
Small-signal bandwidth	5 MHz

8.2.2 Detailed Design Procedure

The circuit in Figure 41 takes a single-ended input signal (V_{IN}) and generates two output signals (V_{OUT+} and $V_{OUT–}$) using two amplifiers and a reference voltage (V_{REF}). V_{OUT+} is the output of the first amplifier and is a buffered version of the input signal (V_{IN}) , as shown in Equation 1. $V_{OUT–}$ is the output of the second amplifier that uses V_{REF} to add an offset voltage to V_{IN} and feedback to add inverting gain. The transfer function for $V_{OUT–}$ is given in Equation 2.

$$V_{OUT+} = V_{IN} \tag{1}$$

$$V_{OUT–} = V_{REF} \times \left(\frac{R_4}{R_3 + R_4} \right) \times \left(1 + \frac{R_2}{R_1} \right) – V_{IN} \times \frac{R_2}{R_1} \tag{2}$$

The differential output signal (V_{DIFF}) is the difference between the two single-ended output signals (V_{OUT+} and $V_{OUT–}$). Equation 3 shows the transfer function for V_{DIFF}. Using conditions in Equation 4 and Equation 5 and applying the conditions that $R_1 = R_2$ and $R_3 = R_4$, the transfer function is simplified into Equation 6. Using this configuration, the maximum input signal is equal to the reference voltage, and the maximum output of each amplifier is equal to V_{REF}. The differential output range is 2 × V_{REF}. Furthermore, the common-mode voltage is one half of V_{REF}, as shown in Equation 7.

$$V_{DIFF} = V_{OUT+} - V_{OUT-} = VIN \times \left(1 + \frac{R_2}{R_1}\right) - V_{REF} \times \left(\frac{R_4}{R_3 + R_4}\right) \times \left(1 + \frac{R_2}{R_1}\right) \quad (3)$$

$$V_{OUT+} = V_{IN} \quad (4)$$

$$V_{OUT-} = V_{REF} - V_{IN} \quad (5)$$

$$V_{DIFF} = 2 \times V_{IN} - V_{REF} \quad (6)$$

$$V_{CM} = \left(\frac{V_{OUT+} + V_{OUT-}}{2}\right) = \frac{1}{2} V_{REF} \quad (7)$$

8.2.2.1 Amplifier Selection

Linearity over the input range is key for good dc accuracy. The common-mode input range and output swing limitations determine the linearity. In general, an amplifier with rail-to-rail input and output swing is required. Bandwidth is a key concern for this design, so the OPAx316-Q1 is selected because the bandwidth is greater than the target of 5 MHz. The bandwidth and power ratio makes this device power efficient and the low offset and drift ensure good accuracy for moderate precision applications.

8.2.2.2 Passive Component Selection

Because the transfer function of $V_{OUT–}$ is heavily reliant on resistors (R_1, R_2, R_3, and R_4), use resistors with low tolerances to maximize performance and minimize error. This design uses resistors with resistance values of 49.9-kΩ and tolerances of 0.1%. However, if the noise of the system is a key parameter, smaller resistance values (6-kΩ or lower) can be selected to keep the overall system noise low. This ensures that the noise from the resistors is lower than the amplifier noise.

8.2.3 Application Curves

The measured transfer functions in Figure 42, Figure 43, and Figure 44 are generated by sweeping the input voltage from 0.1 V to 2.4 V. The full input range is actually 0 V to 2.5 V, but is restricted to 0.1 V to maintain optimal linearity. For more details on this design and other alternative devices that can be used in place of the OPAx316-Q1, see *Single-Ended Input to Differential Output Conversion Circuit Reference Design*.

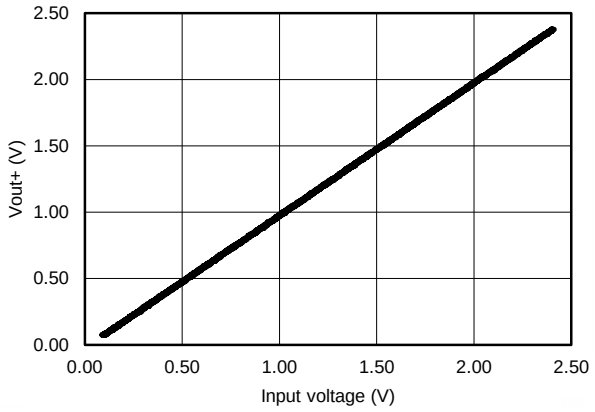


Figure 42. V_{OUT+} vs Input Voltage

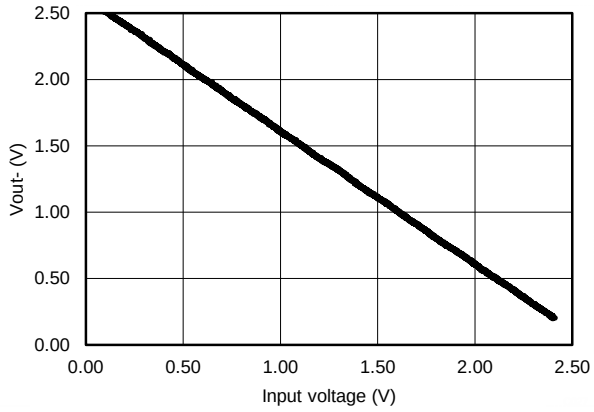


Figure 43. V_{OUT-} vs Input Voltage

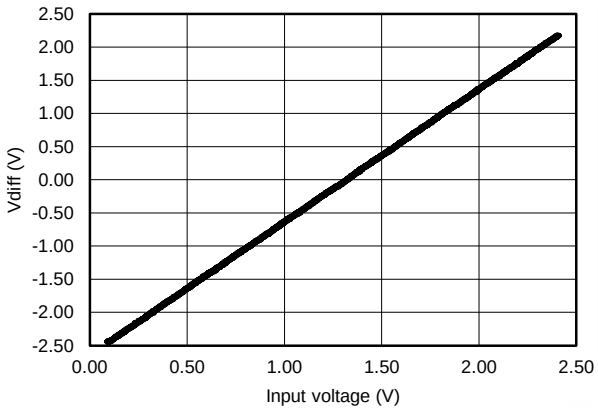


Figure 44. V_{DIFF} vs Input Voltage

9 Power Supply Recommendations

The OPAx316-Q1 family is specified for operation from 1.8 V to 5.5 V (±0.9 V to ±2.75 V); many specifications apply from –40°C to +125°C. The *Typical Characteristics* section presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

CAUTION

Supply voltages larger than 7 V can permanently damage the device; see the *Absolute Maximum Ratings* table.

Place 0.1-μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more information on bypass capacitor placement, see the *Layout Guidelines* section.

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and the operational amplifier. Bypass capacitors reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of the circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are typically devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Take care to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicularly is much better than crossing in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping R_F and R_G close to the inverting input minimizes parasitic capacitance, as shown in Figure 45 .
- Keep the length of input traces as short as possible. Remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

10.2 Layout Example

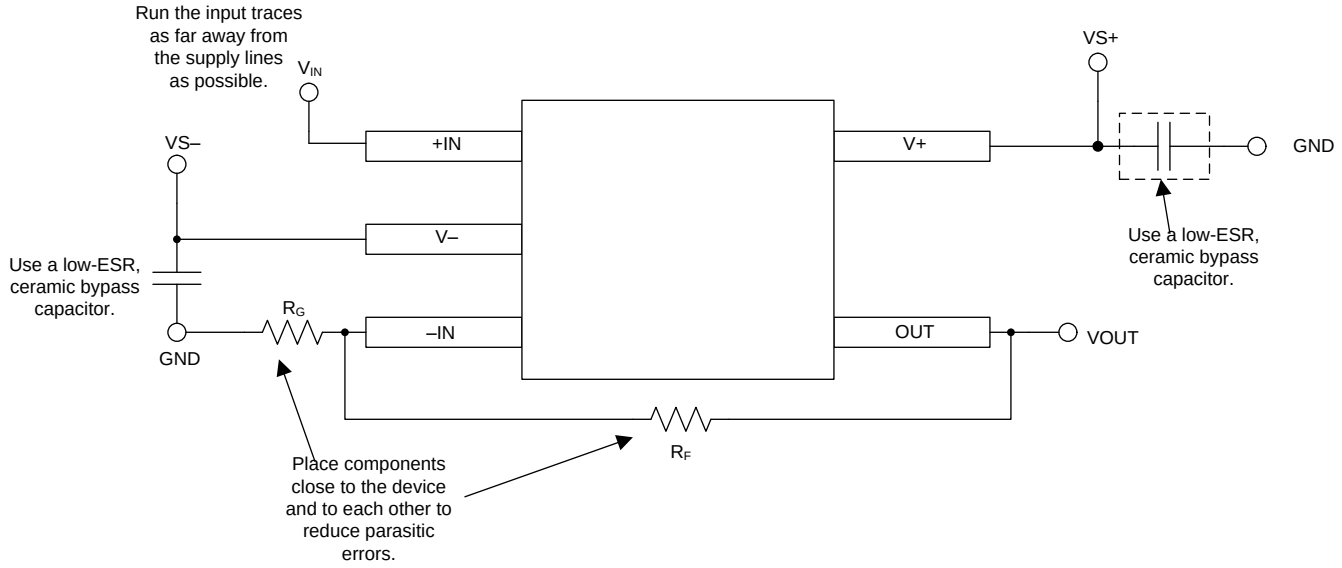


Figure 45. Operational Amplifier Board Layout for Noninverting Configuration

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- *EMI Rejection Ratio of Operational Amplifiers*
- *Single-Ended Input to Differential Output Conversion Circuit Reference Design*

11.2 Related Links

Table 2 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
OPA316-Q1	Click here	Click here	Click here	Click here	Click here
OPA2316-Q1	Click here	Click here	Click here	Click here	Click here
OPA4316-Q1	Click here	Click here	Click here	Click here	Click here

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

E2E is a trademark of Texas Instruments.

11.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA2316QDGKQ1	Active	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	15E6
OPA2316QDGKQ1.B	Active	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	15E6
OPA2316QDGKRQ1	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	15E6
OPA2316QDGKRQ1.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	15E6
OPA316QDBVRQ1	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	15AD
OPA316QDBVRQ1.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	15AD
OPA316QDBVTQ1	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	15AD
OPA316QDBVTQ1.B	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	15AD
OPA4316QPWRQ1	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	4316Q1
OPA4316QPWRQ1.B	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	4316Q1

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative

and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF OPA2316-Q1, OPA316-Q1, OPA4316-Q1 :

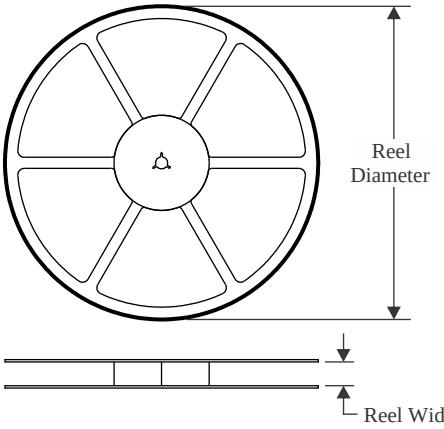
- Catalog : OPA2316, OPA316, OPA4316

NOTE: Qualified Version Definitions:

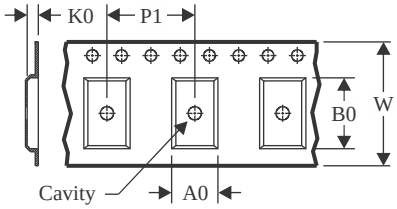
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

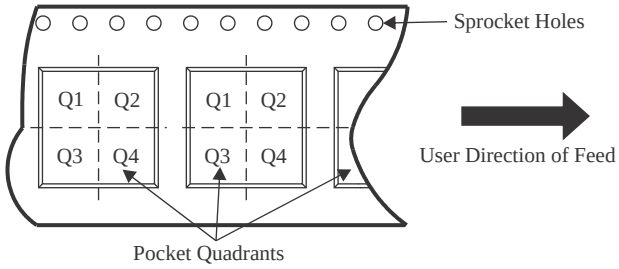


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

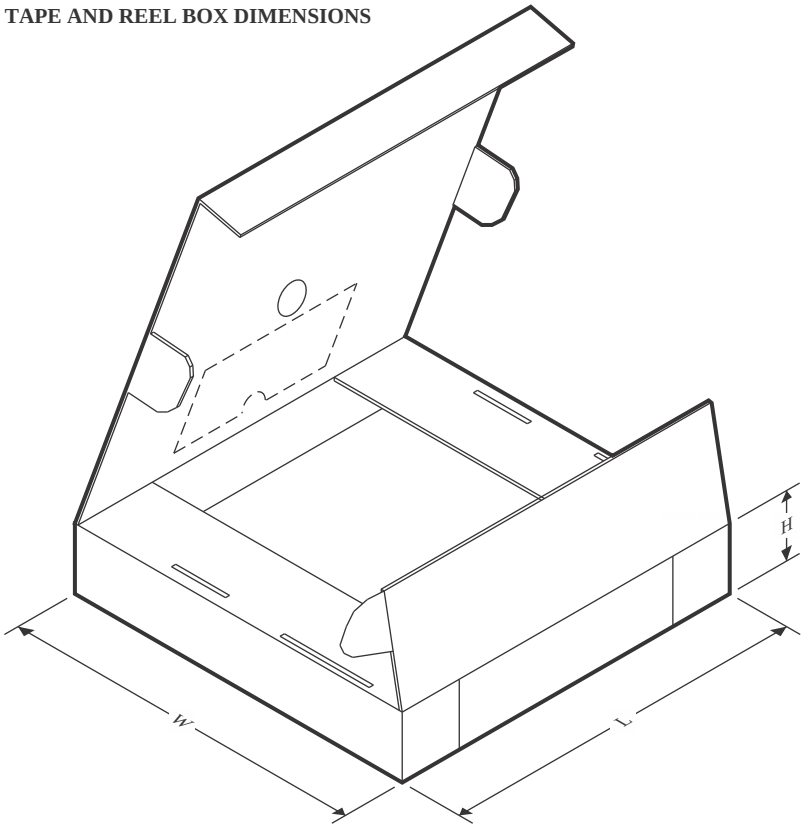
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2316QDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2316QDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA316QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA316QDBVTQ1	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA316QDBVTQ1	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
OPA4316QPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

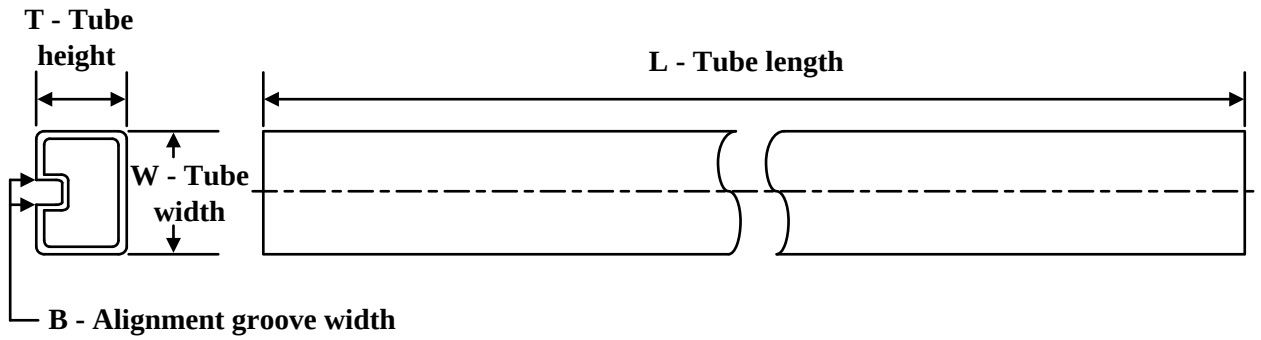
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2316QDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA2316QDGKRQ1	VSSOP	DGK	8	2500	353.0	353.0	32.0
OPA316QDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
OPA316QDBVTQ1	SOT-23	DBV	5	250	210.0	185.0	35.0
OPA316QDBVTQ1	SOT-23	DBV	5	250	180.0	180.0	18.0
OPA4316QPWRQ1	TSSOP	PW	14	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

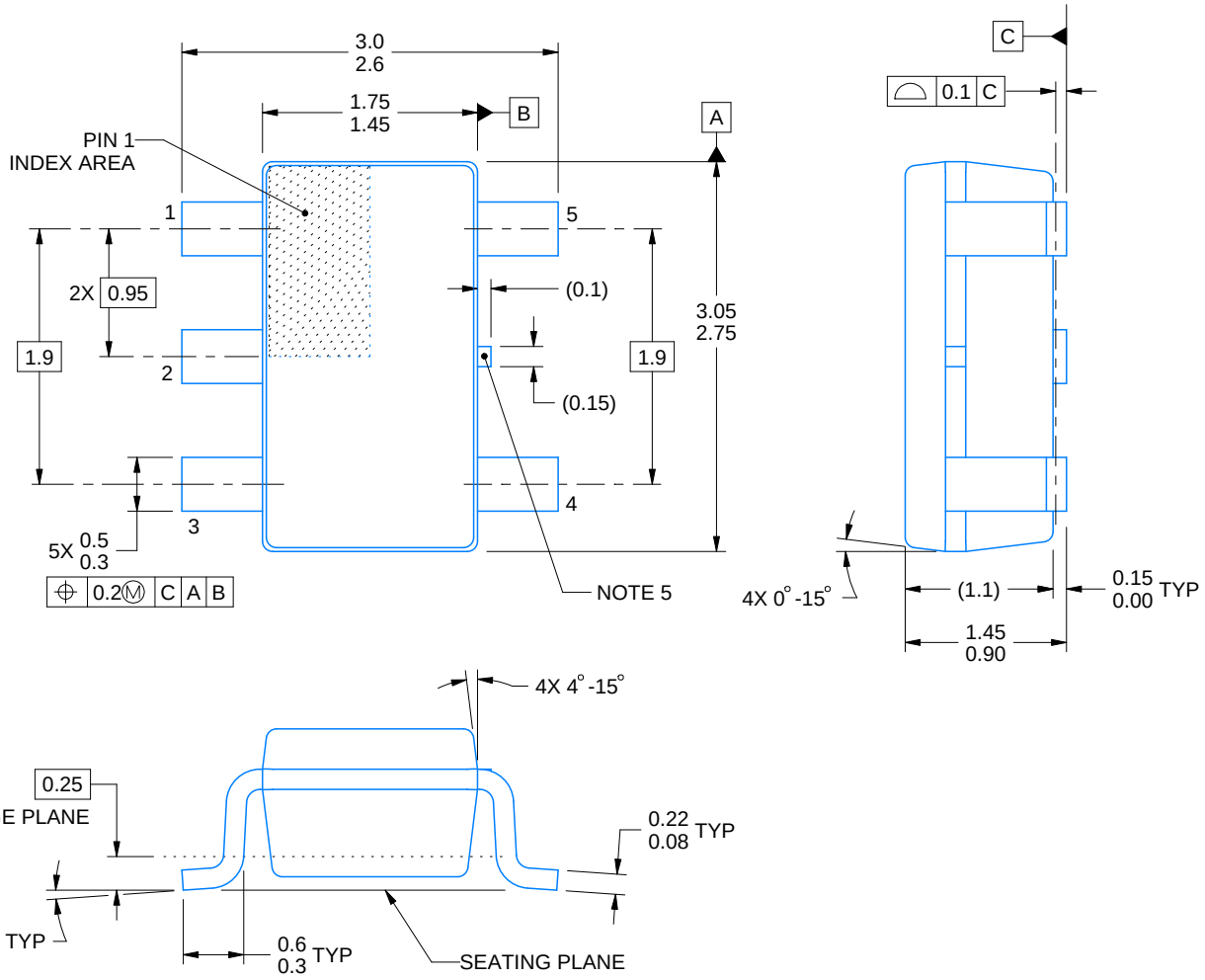
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA2316QDGKQ1	DGK	VSSOP	8	80	330	6.55	500	2.88
OPA2316QDGKQ1.B	DGK	VSSOP	8	80	330	6.55	500	2.88

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

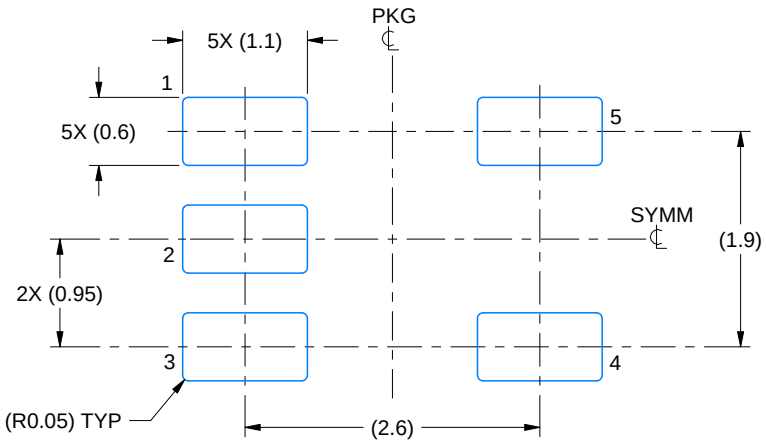
SMALL OUTLINE TRANSISTOR



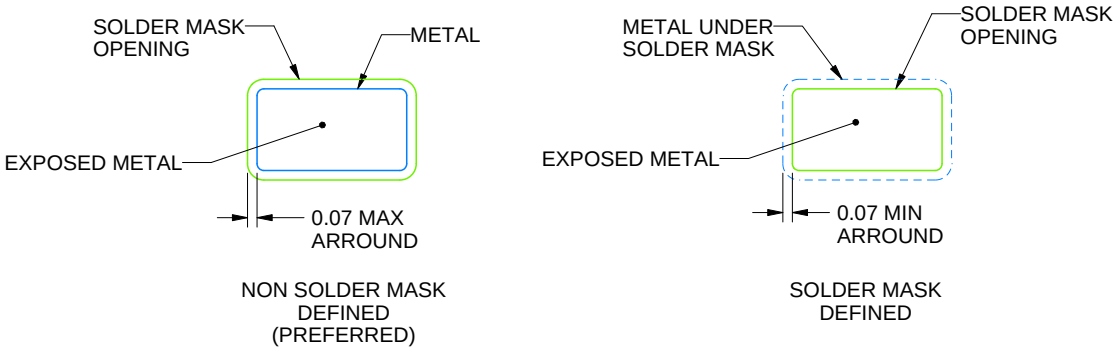
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

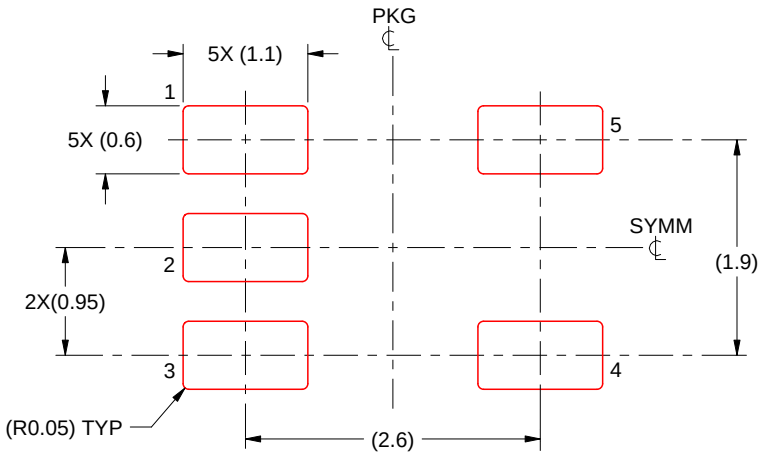


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

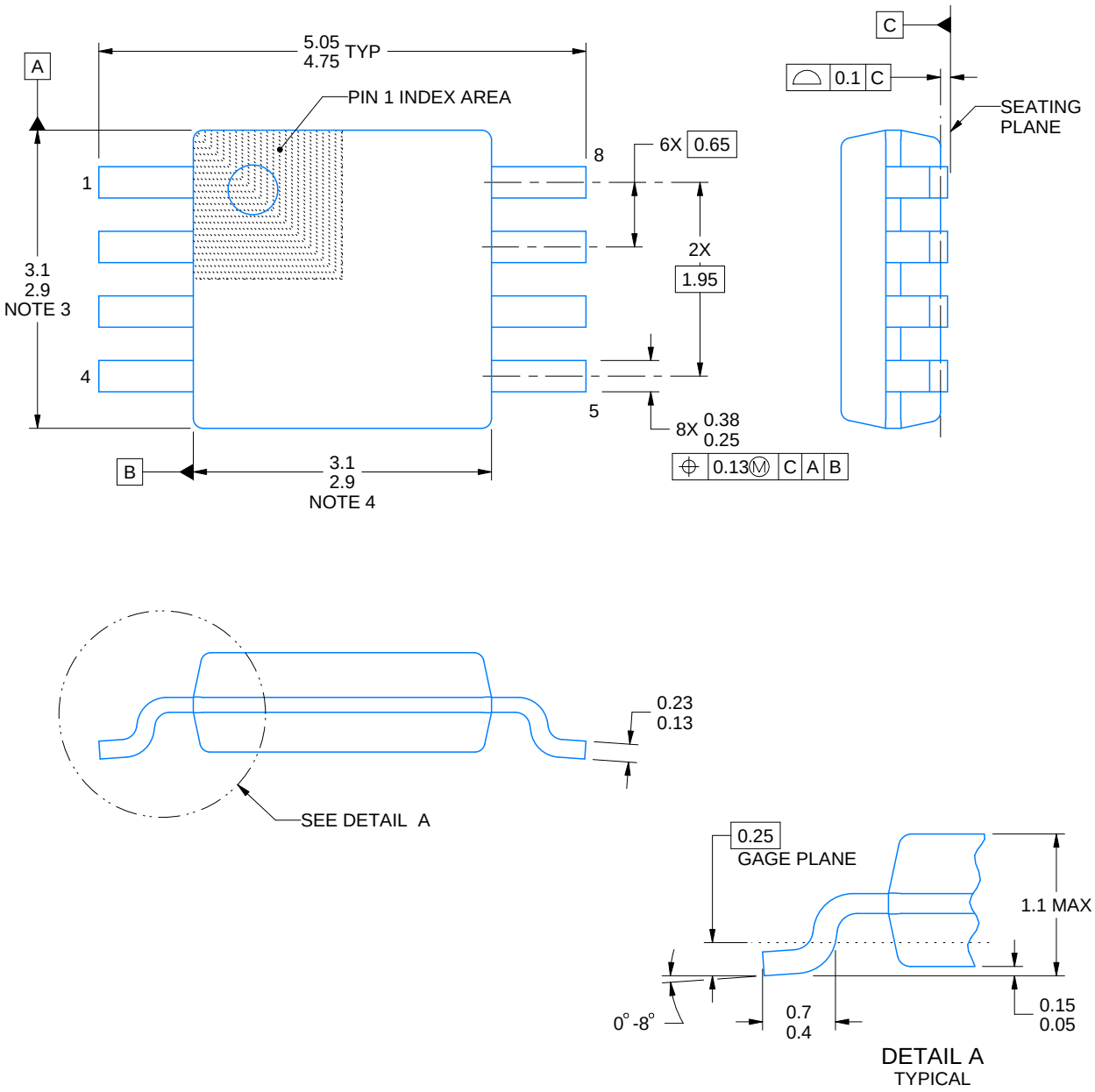
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

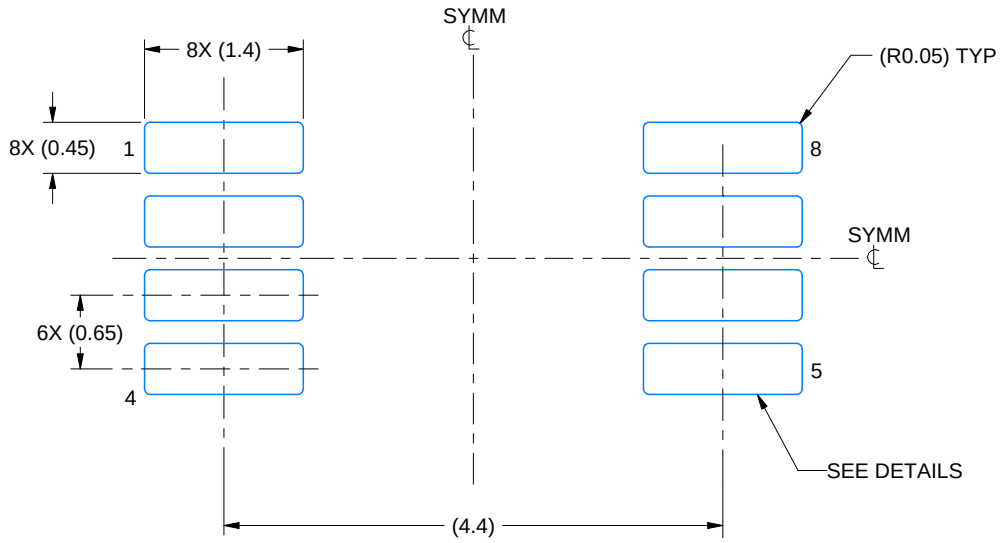
SMALL OUTLINE PACKAGE



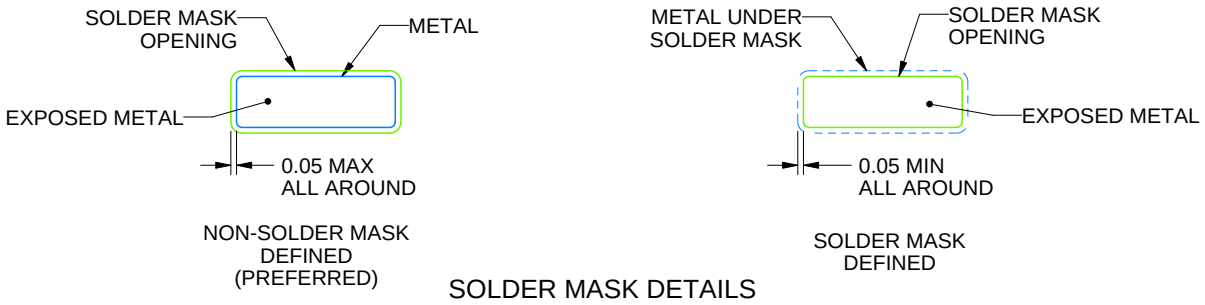
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

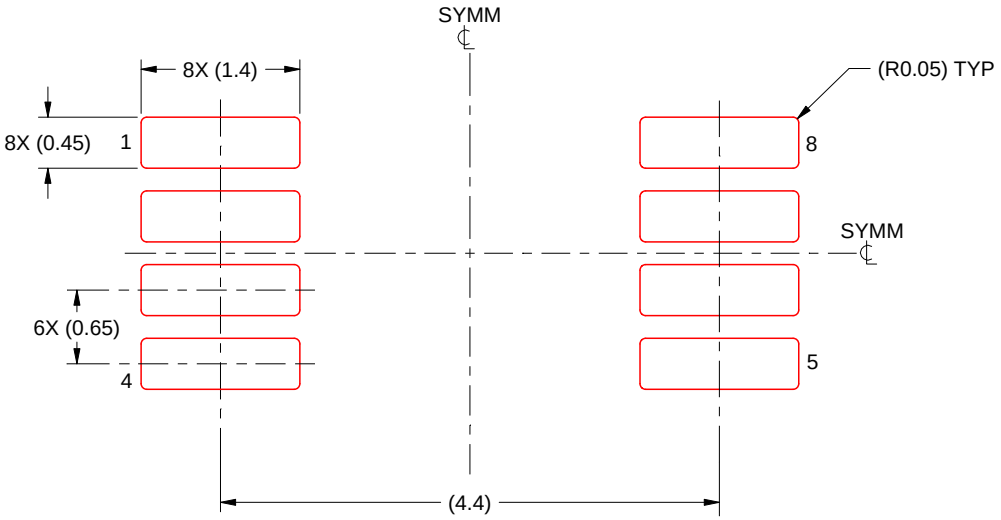


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

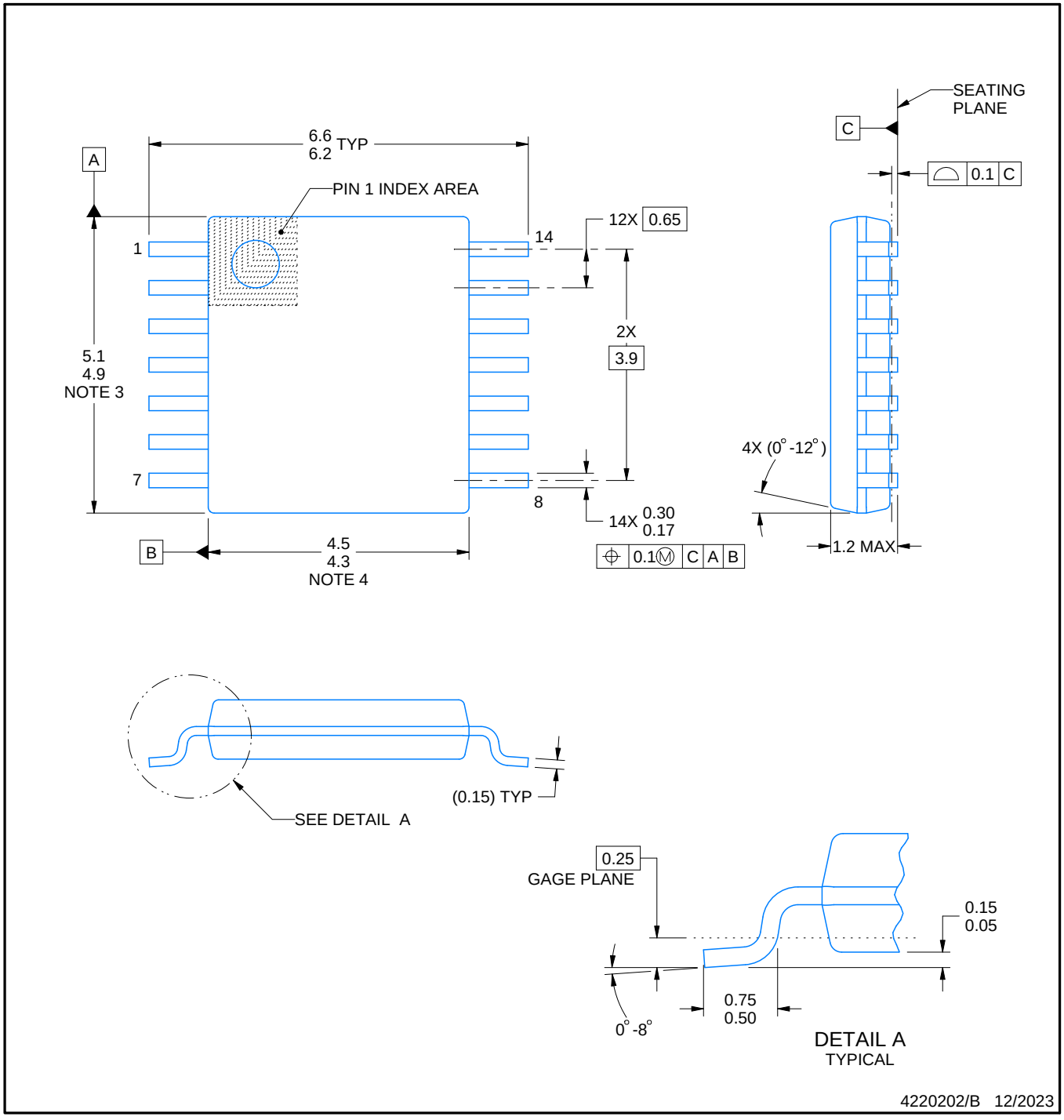
11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0014A

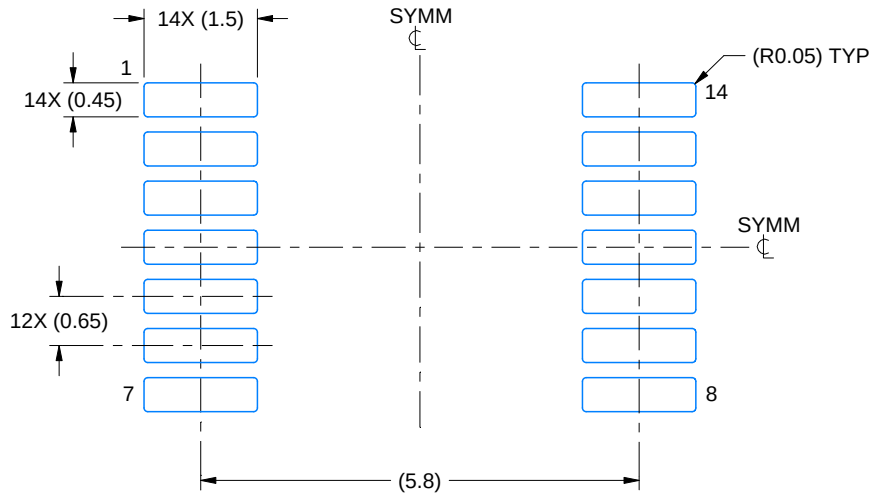
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

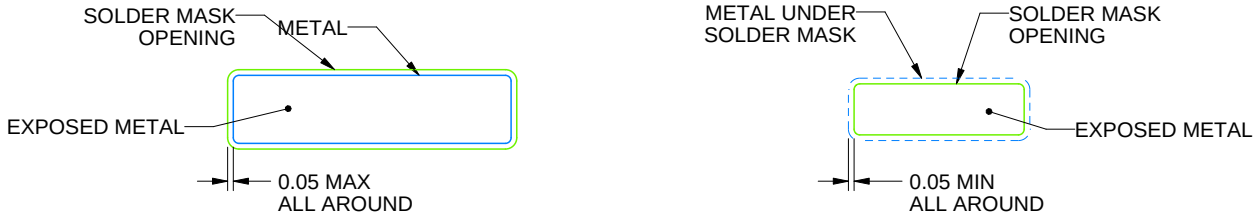


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

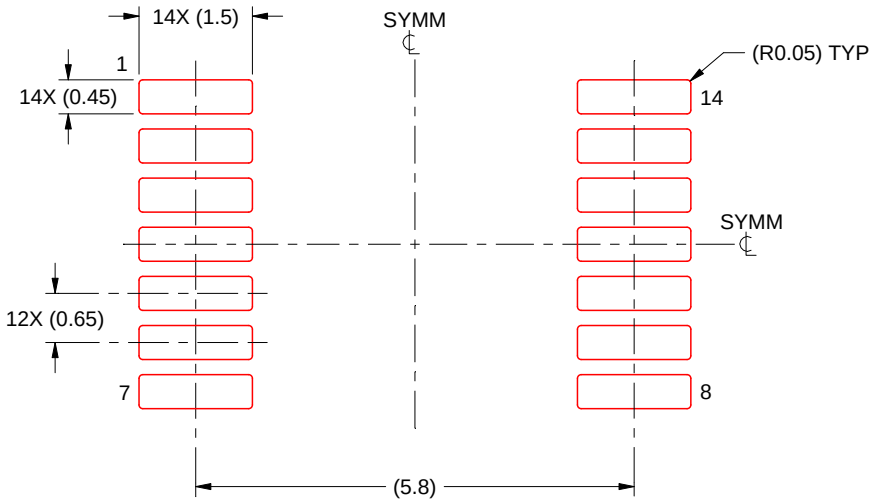


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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