

# MCF8329HS-Q1 Automotive Sensorless Field Oriented Control (FOC) Three-Phase BLDC Gate Driver

## 1 Features

- AEC-Q100 qualified for automotive applications
  - Temperature Grade-1 :  $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$
- Three-phase BLDC gate driver with integrated sensorless motor control algorithm
  - Code-free Field Oriented Control (FOC)
  - Supports up to 2.5kHz (electrical frequency)
  - Speed, current, power or voltage control modes
  - Forward and reverse windmilling support
  - Configurable power and speed limit
  - Analog, PWM, freq. or I<sup>2</sup>C based control input
  - Configurable dry run detection for pumps
  - External MCU watchdog monitoring with limp home mode and reset signal
  - Optional 1-Hall input support
  - 5-point configurable reference profile support
  - Anti-voltage surge and active braking to prevent DC bus overvoltage
  - Flux weakening for high speed operation
  - Maximum torque per ampere (MTPA) for higher efficiency
- 65V Three phase half-bridge gate driver
  - Drives 3 high-side and 3 low-side N-channel MOSFETs, 4.5 to 60V operating voltage
  - Supports 100% PWM duty cycle
  - Bootstrap based gate driver architecture
  - 1A/2A peak source/sink current
- Integrated current sense amplifier
  - Adjustable gain (5, 10, 20, 40V/V)
- Low power sleep mode
  - 5 $\mu\text{A}$  (maximum) at  $V_{\text{PVDD}} = 24\text{V}$ ,  $T_A = 25^{\circ}\text{C}$
- Speed loop accuracy: < 3% with internal clock
- Configurable EEPROM with R/W security
- Support up to 80kHz PWM switching frequency
- Configurable LDO: (3.3V or 5V)  $\pm 3\%$ , 50mA
- Independent driver shutdown path (DRVOFF)
- Spread spectrum and PWM dithering for EMI mitigation
- Suite of integrated protection features
  - Undervoltage protection on all supply rails
  - Loss of phase (no motor) detection including lost phase(s) information
  - Short-circuit protection (VDS) for all 6 FETs
  - Motor lock detection
  - Thermal shutdown (TSD)
  - Fault indication on nFAULT or FG pin
  - Optional fault diagnostics over I<sup>2</sup>C interface

## 2 Applications

- Coolant and water pumps
- Fuel and oil pumps
- HVAC blowers
- Engine and battery cooling fans
- Sunroof modules, Wiper modules
- Zonal modules

## 3 Description

The MCF8329HS-Q1 provides a single-chip, code-free sensorless FOC solution for driving 12V or 24V automotive brushless-DC motors (BLDC) or Permanent Magnet Synchronous motors (PMSM) up to 2.5kHz (electrical speed). The MCF8329HS-Q1 provide three half-bridge gate drivers, each capable of driving high-side and low-side N-channel power MOSFETs. A trickle charge pump is included to support 100% duty cycle. The MCF8329HS-Q1 can operate from a single power supply.

The algorithm configuration can be stored in non-volatile EEPROM, which allows the device to operate stand-alone once it has been configured. There are a large number of protection features integrated into the MCF8329HS-Q1, intended to protect the device, motor, and system against fault events.

MCF8329HS-Q1 is available in a 32-pin, 0.5mm pin pitch, 6x4mm, wettable flank WQFN package (RRY).

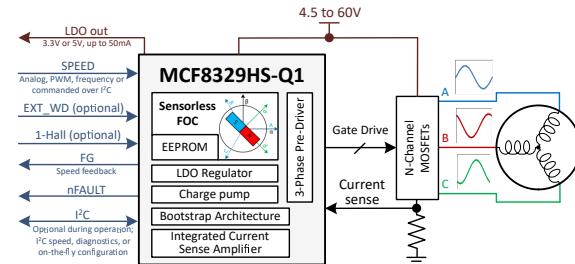
### Device Information <sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
MCF8329HSIQRRYRQ1	WQFN (32)	6.00mm x 4.00mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Documentation for reference:

- Refer [MCF8329HS-Q1 EVM](#)
- Refer [MCF8329HS-Q1 GUI \(MOTORSTUDIO\)](#)



**Simplified Schematic**



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (March 2025) to Revision A (March 2025)	Page
• Updated device status to Production Data.....	<b>1</b>

## 5 Pin Configuration and Functions

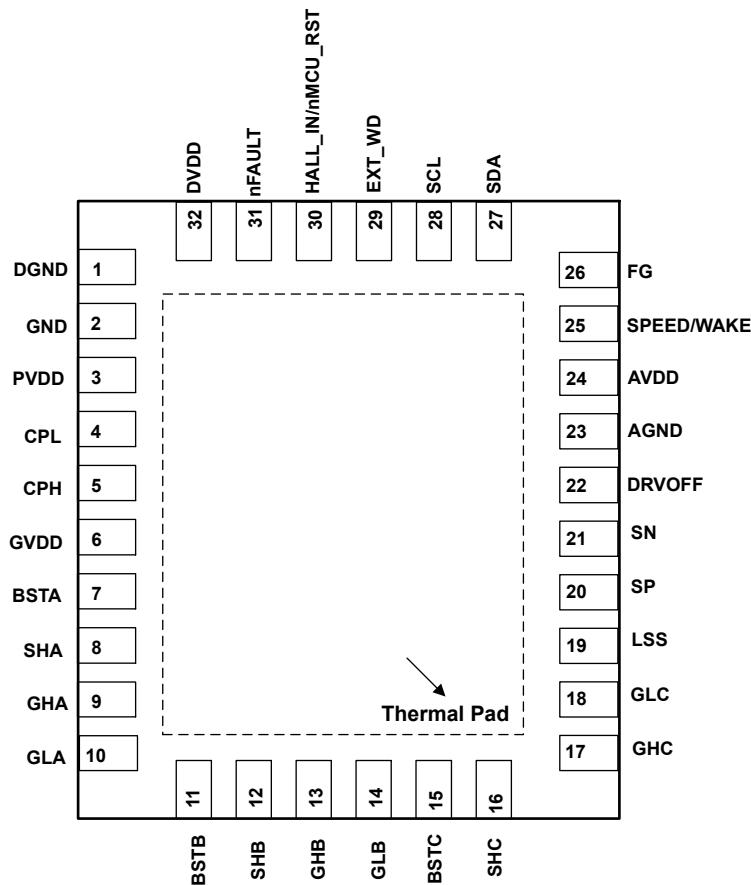


Figure 5-1. MCF8329HS-Q1 32-Pin WQFN With Exposed Thermal Pad Top View

Table 5-1. Pin Functions

PIN	32-pin package	TYPE <sup>(1)</sup>	DESCRIPTION
NAME	MCF8329HS-Q1		
AGND	23	GND	Device analog ground
AVDD	24	PWR	3.3 or 5V regulator output. Connect a X7R, 1µF or 2.2µF, 10V ceramic capacitor between the AVDD and AGND pins. This regulator can source up to 50mA for external circuits. AVDD capacitor should have an effective capacitance between 0.5µF and 2.8µF after operating voltage (AVDD) and temperature derating.
BSTA	7	O	Bootstrap output pin. Connect a X7R, 1µF, 25V ceramic capacitor between BSTA and SHA.
BSTB	11	O	Bootstrap output pin. Connect a X7R, 1µF, 25V ceramic capacitor between BSTB and SHB.
BSTC	15	O	Bootstrap output pin. Connect a X7R, 1µF, 25V ceramic capacitor between BSTC and SHC.
CPH	5	PWR	Charge pump switching node. Connect a X7R, PVDD-rated ceramic capacitor between the CPH and CPL pins. TI recommends a capacitor voltage rating at least twice the normal operating voltage of the pin.
CPL	4	PWR	
DGND	1	GND	Device digital ground
DRVOFF	22	I	Independent driver shutdown path. Pulling DRVOFF high turns off all external MOSFETs by putting the gate drivers into the pull-down state. This signal bypasses and overrides the digital and control core.

**Table 5-1. Pin Functions (continued)**

PIN	32-pin package	TYPE <sup>(1)</sup>	DESCRIPTION
NAME	MCF8329HS-Q1		
DVDD	32	PWR	1.5V internal regulator output. Connect a X7R, 1 $\mu$ F or 2.2 $\mu$ F, 10V ceramic capacitor between the DVDD and DGND pins. DVDD capacitor should have an effective capacitance between 0.5 $\mu$ F and 2.8 $\mu$ F after operating voltage (DVDD) and temperature derating.
EXT_WD	29	I	Watchdog input for external MCU monitoring
FG	26	O	Motor speed indicator: open-drain output that requires a pull-up resistor to 1.8 to 5V. An optional internal pull-up resistor to AVDD can be enabled by setting PULLUP_ENABLE to 1b; no external pull-up resistor should be used when internal pull-up resistor is enabled.
GHA	9	O	High-side gate driver output. Connect to the gate of the high-side power MOSFET
GHB	13	O	High-side gate driver output. Connect to the gate of the high-side power MOSFET
GHC	17	O	High-side gate driver output. Connect to the gate of the high-side power MOSFET
GLA	10	O	Low-side gate driver output. Connect to the gate of the low-side power MOSFET
GLB	14	O	Low-side gate driver output. Connect to the gate of the low-side power MOSFET
GLC	18	O	Low-side gate driver output. Connect to the gate of the low-side power MOSFET
GND	2	GND	Device power ground
GVDD	6	PWR	Gate driver power supply output. Connect a X7R, 30V rated ceramic $\geq$ 10 $\mu$ F local capacitance between the GVDD and GND pins. TI recommends a capacitor value of $>10x C_{B_{STX}}$ and voltage rating at least twice the normal operating voltage of the pin.
HALL_IN/ nMCU_RST	30	I/O	Multi-purpose pin. Single (3.3V or 5V) digital hall latch (optional) input for redundancy in motor lock detection or active-low (with internal pull-up to AVDD) reset signal to external MCU in case of watchdog timeout fault.
LSS	19	PWR	Low side source pin, connect all sources of the external low-side MOSFETs here. This pin is the sink path for the low-side gate driver, and serves as an input to monitor the low-side MOSFET VDS voltage and VSEN_OCP voltage.
nFAULT	31	O	Fault indicator. Pulled logic-low during fault condition; open-drain output that requires a pull-up resistor to 1.8V to 5V. An optional internal pull-up resistor to AVDD is enabled by setting PULLUP_ENABLE to 1b; no external pull-up resistor should be used when internal pull-up resistor is enabled
PVDD	3	PWR	Gate driver power supply input. Connect to the bridge power supply. Connect a X7R, 0.1 $\mu$ F, $>2x$ PVDD-rated ceramic and $>10\mu$ F local capacitance between the PVDD and GND pins. TI recommends a capacitor voltage rating at least twice the normal operating voltage of the pin.
SCL	28	I	I <sup>2</sup> C clock input
SDA	27	I/O	I <sup>2</sup> C data line
SHA	8	I/O	High-side source pin. Connect to the high-side power MOSFET source. This pin is an input for the VDS monitor and the output for the high-side gate driver sink.
SHB	12	I/O	High-side source pin. Connect to the high-side power MOSFET source. This pin is an input for the VDS monitor and the output for the high-side gate driver sink.
SHC	16	I/O	High-side source pin. Connect to the high-side power MOSFET source. This pin is an input for the VDS monitor and the output for the high-side gate driver sink.
SN	21	I	Current sense amplifier input. Connect to the low-side of the current shunt resistor.
SP	20	I	Low-side current shunt amplifier input. Connect to the low-side power MOSFET source and high-side of the current shunt resistor.
SPEED/ WAKE	25	I	Multifunction input. Device sleep/wake input. Device speed input; supports analog, PWM or frequency based reference (speed or current or power or voltage) input.
Thermal pad	-	PWR	Must be connected to ground

(1) I = input, O = output, GND = ground pin, PWR = power, NC = no connect

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Power supply pin voltage	PVDD	-0.3	65	V
Bootstrap pin voltage	BSTx	-0.3	80	V
Bootstrap pin voltage	BSTx with respect to SHx	-0.3	20	V
Bootstrap pin voltage	BSTx with respect to GHx	-0.3	20	V
Charge pump pin voltage	CPL, CPH	-0.3	$V_{GVDD}$	V
Voltage difference between ground pins	GND, DGND, AGND	-0.3	0.3	V
Gate driver regulator pin voltage	GVDD	-0.3	20	V
Digital regulator pin voltage	DVDD	-0.3	1.7	V
Analog regulator pin voltage	AVDD	-0.3	6	V
Logic pin voltage	DRVOFF, EXT_WD, HALL_IN, SCL, SDA, SPEED/WAKE	-0.3	6	V
Open drain pin output voltage	nFAULT, FG, nMCU_RST	-0.3	6	V
High-side gate drive pin voltage	GHx	-8	80	V
Transient 500-ns high-side gate drive pin voltage	GHx	-10	80	V
High-side gate drive pin voltage	GHx with respect to SHx	-0.3	20	V
High-side source pin voltage	SHx	-8	70	V
Transient 500-ns high-side source pin voltage	SHx	-10	72	V
Low-side gate drive pin voltage	GLx with respect to LSS	-0.3	20	V
Transient 500-ns low-side gate drive pin voltage <sup>(2)</sup>	GLx with respect to LSS	-1	20	V
Low-side gate drive pin voltage	GLx with respect to GVDD		0.3	V
Transient 500-ns low-side gate drive pin voltage	GLx with respect to GVDD		1	V
Low-side source sense pin voltage	LSS	-1	1	V
Transient 500-ns low-side source sense pin voltage	LSS	-10	8	V
Gate drive current	GHx, GLx	Internally Limited	Internally Limited	A
Shunt amplifier input pin voltage	SN, SP	-1	1	V
Transient 500-ns shunt amplifier input pin voltage	SN, SP	-10	8	V
Ambient temperature, $T_A$		-40	125	°C
Junction temperature, $T_J$		-40	150	°C
Storage temperature, $T_{stg}$		-65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime

(2) Supports up to 5A for 500 nS when GLx-LSS is negative

### 6.2 ESD Ratings Auto

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 <sup>(1)</sup> HBM ESD Classification Level 2	$\pm 2000$	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B	Corner pins $\pm 750$ Other pins $\pm 750$	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 6.3 Recommended Operating Conditions

over operating temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
$V_{PVDD}$	Power supply voltage	PVDD	4.5	60		V
$V_{PVDD\_RAMP}$	Power supply voltage ramp rate at power up	PVDD		30		V/ $\mu$ s
$V_{BST}$	Bootstrap pin voltage with respect to SHx	SPEED/WAKE = High, Outputs are switching	4	20		V
$I_{AVDD}$ <sup>(1)</sup>	Regulator external load current	AVDD		50		mA
$I_{TRICKLE}$	Trickle charge pump external load current	BSTx		2		$\mu$ A
$V_{IN}$	Logic input voltage	DRVOFF, EXT_WD, HALL_IN, SCL, SDA, SPEED/WAKE	0	5.5		V
$f_{PWM}$	PWM frequency		0	80		kHz
$V_{OD}$	Open drain pullup voltage	FG, nFAULT, nMCU_RST		5.5		V
$I_{OD}$	Open drain output current	nFAULT		-10		mA
$I_{GS}$ <sup>(1)</sup>	Total average gate-drive current (Low Side and High Side Combined)	$I_{GHx}$ , $I_{GLx}$		30		mA
$V_{SHSL}$	Slew Rate on SHx pins			4		V/ns
$C_{BOOT}$	Capacitor between BSTx and SHx			4.7 <sup>(2)</sup>		$\mu$ F
$C_{GVDD}$	Capacitor between GVDD and GND			130		$\mu$ F
$T_A$	Operating ambient temperature		-40	125		°C
$T_J$	Operating junction temperature		-40	150		°C

(1) Power dissipation and thermal limits must be observed

(2) Current flowing through boot diode (DBOOT) needs to be limited for  $C_{BSTx} > 4.7\mu$ F.

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		MCF8329HS -Q1	UNIT
		RRY (WQFN)	
		32 pins	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	31.3	°C/W
$R_{\theta JC(\text{top})}$	Junction-to-case (top) thermal resistance	19.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	10.7	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	0.6	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	10.7	°C/W
$R_{\theta JC(\text{bot})}$	Junction-to-case (bottom) thermal resistance	3.7	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics application report](#).

## 6.5 Electrical Characteristics

4.5 V ≤  $V_{PVDD}$  ≤ 60 V,  $-40^\circ C \leq T_J \leq 150^\circ C$  (unless otherwise noted). Typical limits apply for  $T_A = 25^\circ C$ ,  $V_{PVDD} = 12 V$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
<b>POWER SUPPLIES (PVDD, GVDD, AVDD, DVDD)</b>							
$I_{PVDDQ}$	PVDD sleep mode current	$V_{PVDD} = 12V$ , $V_{SPEED/WAKE} = 0$ , $T_A = 25^\circ C$		3	5	$\mu A$	
		$V_{SPEED/WAKE} = 0$ , $T_A = 125^\circ C$		3.5	6	$\mu A$	
$I_{PVDDS}$	PVDD standby mode current	$V_{PVDD} = 12 V$ , $V_{SPEED/WAKE} < V_{EN\_SB}$ , $DRVOFF = LOW$ , $T_A = 25^\circ C$ , $CLOCK\_FREQUENCY = 0x0$		28	30	mA	
		$V_{SPEED/WAKE} < V_{EN\_SB}$ , $DRVOFF = LOW$ , $CLOCK\_FREQUENCY = 0x0$		28	30	mA	
$I_{PVDDS}$	PVDD standby mode current	$V_{PVDD} = 12 V$ , $V_{SPEED/WAKE} < V_{EN\_SB}$ , $DRVOFF = LOW$ , $T_A = 25^\circ C$ , $CLOCK\_FREQUENCY = 0x1$		24	26	mA	
		$V_{SPEED/WAKE} < V_{EN\_SB}$ , $DRVOFF = LOW$ , $CLOCK\_FREQUENCY = 0x1$		24	26	mA	
$I_{PVDDS}$	PVDD standby mode current	$V_{PVDD} = 12 V$ , $V_{SPEED/WAKE} < V_{EN\_SB}$ , $DRVOFF = LOW$ , $T_A = 25^\circ C$ , $CLOCK\_FREQUENCY = 0x2$		20	22	mA	
		$V_{SPEED/WAKE} < V_{EN\_SB}$ , $DRVOFF = LOW$ , $CLOCK\_FREQUENCY = 0x2$		20	22	mA	
$I_{PVDD}$	PVDD active mode current	$V_{PVDD} = 12 V$ , $V_{SPEED/WAKE} > V_{EX\_SL}$ , $PWM\_FREQ\_OUT = 0011b$ (25 kHz), $T_J = 25^\circ C$ , No FETs and motor connected, $CLOCK\_FREQUENCY = 0x0$		28	30	mA	
		$V_{SPEED/WAKE} > V_{EX\_SL}$ , $PWM\_FREQ\_OUT = 0011b$ (25 kHz), No FETs and motor connected, $CLOCK\_FREQUENCY = 0x0$		28	30	mA	
$I_{PVDD}$	PVDD active mode current	$V_{PVDD} = 12 V$ , $V_{SPEED/WAKE} > V_{EX\_SL}$ , $PWM\_FREQ\_OUT = 0011b$ (25 kHz), $T_J = 25^\circ C$ , No FETs and motor connected, $CLOCK\_FREQUENCY = 0x1$		24	26	mA	
		$V_{SPEED/WAKE} > V_{EX\_SL}$ , $PWM\_FREQ\_OUT = 0011b$ (25 kHz), No FETs and motor connected, $CLOCK\_FREQUENCY = 0x1$		24	26	mA	
$I_{PVDD}$	PVDD active mode current	$V_{PVDD} = 12 V$ , $V_{SPEED/WAKE} > V_{EX\_SL}$ , $PWM\_FREQ\_OUT = 0011b$ (25 kHz), $T_J = 25^\circ C$ , No FETs and motor connected, $CLOCK\_FREQUENCY = 0x2$		20	22	mA	
		$V_{SPEED/WAKE} > V_{EX\_SL}$ , $PWM\_FREQ\_OUT = 0011b$ (25 kHz), No FETs and motor connected, $CLOCK\_FREQUENCY = 0x2$		20	22	mA	
$IL_{BSx}$	Bootstrap pin leakage current	$V_{BSTx} = V_{SHx} = 60V$ , $V_{GVDD} = 0V$ , $V_{SPEED/WAKE} = LOW$		5	10	$\mu A$	
$IL_{BS\_TRAN}$	Bootstrap pin active mode transient leakage current	$GLx = GHx = \text{Switching at 20kHz}$ , No FETs connected		60	115	300	$\mu A$

## 6.5 Electrical Characteristics (continued)

4.5 V  $\leq$   $V_{PVDD}$   $\leq$  60 V,  $-40^\circ C \leq T_J \leq 150^\circ C$  (unless otherwise noted). Typical limits apply for  $T_A = 25^\circ C$ ,  $V_{PVDD} = 12 V$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{GVDD\_RT}$	GVDD Gate driver regulator voltage (Room Temperature)	$V_{PVDD} \geq 40 V$ , $I_{GS} = 10 mA$ , $T_J = 25^\circ C$	11.8	13	15	V
		$22 V \leq V_{PVDD} \leq 40 V$ , $I_{GS} = 30 mA$ , $T_J = 25^\circ C$	11.8	13	15	V
		$8 V \leq V_{PVDD} \leq 22 V$ , $I_{GS} = 30 mA$ , $T_J = 25^\circ C$	11.8	13	15	V
		$6.75 V \leq V_{PVDD} \leq 8 V$ , $I_{GS} = 10 mA$ , $T_J = 25^\circ C$	11.8	13	14.5	V
		$4.5 V \leq V_{PVDD} \leq 6.75 V$ , $I_{GS} = 10 mA$ , $T_J = 25^\circ C$	$2^*V_{PVDD} - 1$		13.5	V
$V_{GVDD}$	GVDD Gate driver regulator voltage	$V_{PVDD} \geq 40 V$ , $I_{GS} = 10 mA$	11.5		15.5	V
		$22 V \leq V_{PVDD} \leq 40 V$ , $I_{GS} = 30 mA$	11.5		15.5	V
		$8 V \leq V_{PVDD} \leq 22 V$ , $I_{GS} = 30 mA$	11.5		15.5	V
		$6.75 V \leq V_{PVDD} \leq 8 V$ , $I_{GS} = 10 mA$	11.5		14.5	V
		$4.5 V \leq V_{PVDD} \leq 6.75 V$ , $I_{GS} = 10 mA$	$2^*V_{PVDD} - 1.4$		13.5	V
$V_{AVDD\_RT}$	AVDD Analog regulator voltage (Room Temperature), $AVDD\_VOL\_SEL = 0b$	$V_{PVDD} \geq 6 V$ , $0 mA \leq I_{AVDD} \leq 50 mA$ , $T_J = 25^\circ C$	3.2	3.3	3.34	V
		$4.5 \leq V_{PVDD} < 6 V$ , $0 mA \leq I_{AVDD} \leq 50 mA$ , $T_J = 25^\circ C$	3.13	3.3	3.46	V
$V_{AVDD\_RT}$	AVDD Analog regulator voltage (Room Temperature), $AVDD\_VOL\_SEL = 1b$	$V_{PVDD} \geq 6 V$ , $0 mA \leq I_{AVDD} \leq 50 mA$ , $T_J = 25^\circ C$	4.85	5	5.15	V
$V_{AVDD}$	AVDD Analog regulator voltage, $AVDD\_VOL\_SEL = 0b$	$V_{PVDD} \geq 6 V$ , $0 mA \leq I_{AVDD} \leq 50 mA$	3.2	3.3	3.4	V
		$4.5 \leq V_{PVDD} < 6 V$ , $0 mA \leq I_{AVDD} \leq 50 mA$	3.125	3.3	3.5	V
$V_{AVDD}$	AVDD Analog regulator voltage, $AVDD\_VOL\_SEL = 1b$	$V_{PVDD} \geq 6 V$ , $0 mA \leq I_{AVDD} \leq 50 mA$	4.85	5	5.15	V
$V_{DVDD}$	Digital regulator voltage		1.52	1.62	1.7	V
<b>GATE DRIVERS (GHx, GLx, SHx, SLx)</b>						
$V_{GSHx\_LO}$	High-side gate drive low level voltage	$I_{GHx} = -100 mA$ ; $V_{GVDD} = 12V$ ; No FETs connected	0.05	0.11	0.24	V
$V_{GSHx\_HI}$	High-side gate drive high level voltage ( $V_{BSTx} - V_{GHx}$ )	$I_{GHx} = 100 mA$ ; $V_{GVDD} = 12V$ ; No FETs connected	0.28	0.44	0.82	V
$V_{GSLx\_LO}$	Low-side gate drive low level voltage	$I_{GLx} = -100 mA$ ; $V_{GVDD} = 12V$ ; No FETs connected	0.05	0.11	0.27	V
$V_{GSLx\_HI}$	Low-side gate drive high level voltage ( $V_{GVDD} - V_{GLx}$ )	$I_{GLx} = 100 mA$ ; $V_{GVDD} = 12V$ ; No FETs connected	0.28	0.44	0.82	V
$R_{DS(ON)\_PU\_HS}$	High-side pullup switch resistance	$I_{GHx} = 100 mA$ ; $V_{GVDD} = 12V$	2.7	4.5	8.4	$\Omega$
$R_{DS(ON)\_PD\_HS}$	High-side pulldown switch resistance	$I_{GHx} = 100 mA$ ; $V_{GVDD} = 12V$	0.5	1.1	2.4	$\Omega$
$R_{DS(ON)\_PU\_LS}$	Low-side pullup switch resistance	$I_{GLx} = 100 mA$ ; $V_{GVDD} = 12V$	2.7	4.5	8.3	$\Omega$
$R_{DS(ON)\_PD\_LS}$	Low-side pulldown switch resistance	$I_{GLx} = 100 mA$ ; $V_{GVDD} = 12V$	0.5	1.1	2.8	$\Omega$
$I_{DRIVEP\_HS}$	High-side peak source gate current	$V_{GSHx} = 12V$	550	1000	1575	mA
$I_{DRIVEN\_HS}$	High-side peak sink gate current	$V_{GSHx} = 0V$	1150	2000	2675	mA
$I_{DRIVEP\_LS}$	Low-side peak source gate current	$V_{GSLx} = 12V$	550	1000	1575	mA
$I_{DRIVEN\_LS}$	Low-side peak sink gate current	$V_{GSLx} = 0V$	1150	2000	2675	mA
$R_{PD\_LS}$	Low-side passive pull down	GLx to LSS	80	100	120	$k\Omega$

## 6.5 Electrical Characteristics (continued)

4.5 V  $\leq$   $V_{PVDD}$   $\leq$  60 V,  $-40^\circ C \leq T_J \leq 150^\circ C$  (unless otherwise noted). Typical limits apply for  $T_A = 25^\circ C$ ,  $V_{PVDD} = 12 V$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT		
$R_{PDSA\_HS}$		High-side semiactive pull down	$GH_x$ to $SH_x$ , $V_{GSH_x} = 2V$		8	10	12.5	$k\Omega$
<b>BOOTSTRAP DIODES</b>								
$V_{BOOTD}$	Bootstrap diode forward voltage	$I_{BOOT} = 100 \mu A$			0.8	V		
		$I_{BOOT} = 100 mA$			1.6	V		
$R_{BOOTD}$	Bootstrap dynamic resistance ( $\Delta V_{BOOTD} / \Delta I_{BOOT}$ )	$I_{BOOT} = 100 mA$ and $50 mA$	4.5	5.5	9	$\Omega$		
<b>LOGIC-LEVEL INPUTS (SCL, SDA, SPEED/WAKE, EXT_WD, HALL_IN)</b>								
$V_{IL}$	Input logic low voltage	$AVDD = 3.3V, 5V$			$0.25*AV_{DD}$	V		
$V_{IH}$	Input logic high voltage	$AVDD = 3.3V, 5V$			$0.65*AV_{DD}$	V		
$V_{HYS}$	Input hysteresis		50	500	800	$mV$		
$I_{IL}$	Input logic low current	$AVDD = 3.3V, 5V$			-0.15	$\mu A$		
$I_{IH}$	Input logic high current	$AVDD = 3.3V, 5V$			-0.3	$\mu A$		
$R_{PD\_SPEED}$	Input pulldown resistance	SPEED/WAKE pin To GND	0.6	1	1.4	$M\Omega$		
<b>LOGIC-LEVEL INPUTS (DRVOFF)</b>								
$V_{IL}$	Input logic low voltage				0.8	V		
$V_{IH}$	Input logic high voltage				2.2	V		
$V_{HYS}$	Input hysteresis		200	400	650	$mV$		
$I_{IL}$	Input logic low current	Pin Voltage = 0 V	-1	0	1	$\mu A$		
$I_{IH}$	Input logic high current	Pin Voltage = 5 V	7	20	35	$\mu A$		
$R_{PD\_DRVOFF}$	Input pulldown resistance	DRVOFF To GND	100	200	300	$k\Omega$		
<b>OPEN-DRAIN OUTPUTS (nFAULT, FG, nMCU_RST)</b>								
$V_{OL}$	Output logic low voltage	$I_{OD} = -5 mA$			0.4	V		
$I_{OZ}$	Output logic high current	$V_{OD} = 3.3 V$			0	$0.5 \mu A$		
<b>SPEED INPUT - ANALOG MODE</b>								
$V_{ANA\_FS}$	Analog full-speed voltage		2.95	3	3.05	V		
$V_{ANA\_RES}$	Analog voltage resolution				732	$\mu V$		
<b>SPEED INPUT - PWM MODE</b>								
$f_{PWM}$	PWM input frequency		0.01	100		kHz		
$Res_{PWM}$	PWM input resolution	$f_{PWM} = 0.01$ to $0.35$ kHz	11	12	13	bits		
		$f_{PWM} = 0.35$ to $2$ kHz	12	13	14	bits		
		$f_{PWM} = 2$ to $3.5$ kHz	11	11.5	12	bits		
		$f_{PWM} = 3.5$ to $7$ kHz	13	13.5	14	bits		
		$f_{PWM} = 7$ to $14$ kHz	12	12.5	13	bits		
		$f_{PWM} = 14$ to $29.2$ kHz	11	11.5	12	bits		
		$f_{PWM} = 29.3$ to $60$ kHz	10	10.5	11	bits		
		$f_{PWM} = 60$ to $95$ kHz	8	9	10	bits		
<b>SPEED INPUT - FREQUENCY MODE</b>								
$f_{PWM\_FREQ}$	PWM input frequency range	Duty cycle = 50%	3	32767		Hz		
<b>SLEEP MODE</b>								
$V_{EN\_SL}$	Analog voltage to enter sleep mode	SPEED_MODE = 00b (analog mode)			40	$mV$		
$V_{EX\_SL}$	Analog voltage to exit sleep mode				2.6	V		
$t_{DET\_ANA}$	Time needed to detect wake up signal on SPEED/WAKE pin	SPEED_MODE = 00b (analog mode), $V_{SPEED/WAKE} > V_{EX\_SL}$	0.5	1	1.5	$\mu s$		

## 6.5 Electrical Characteristics (continued)

4.5 V  $\leq$   $V_{PVDD}$   $\leq$  60 V,  $-40^\circ\text{C} \leq T_J \leq 150^\circ\text{C}$  (unless otherwise noted). Typical limits apply for  $T_A = 25^\circ\text{C}$ ,  $V_{PVDD} = 12\text{ V}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{WAKE}$	Wakeup time from sleep mode	$V_{SPEED/WAKE} > V_{EX\_SL}$ to DVDD voltage available, SPEED_MODE = 00b (analog mode)		3	5	ms
$t_{EX\_SL\_DR\_ANA}$	Time taken to drive motor after exiting from sleep mode	SPEED_MODE = 00b (analog mode) $V_{SPEED/WAKE} > V_{EX\_SL}$ , ISD detection disabled		30		ms
$t_{DET\_PWM}$	Time needed to detect wake up signal on SPEED pin	SPEED_MODE = 01b (PWM mode) or 11b (Frequency mode), $V_{SPEED/WAKE} > V_{IH}$	0.5	1	1.5	$\mu\text{s}$
$t_{WAKE\_PWM}$	Wakeup time from sleep mode	$V_{SPEED/WAKE} > V_{IH}$ to DVDD voltage available and release nFault, SPEED_MODE = 01b (PWM mode) or 11b (Frequency mode)		3	5	ms
$t_{EX\_SL\_DR\_PWM}$	Time taken to drive motor after wakeup from sleep state	SPEED_MODE = 01b (PWM mode) $V_{SPEED/WAKE} > V_{IH}$ , ISD detection disabled		30		ms
$t_{DET\_SL\_ANA}$	Time needed to detect sleep command	SPEED_MODE = 00b (analog mode) $V_{SPEED/WAKE} < V_{EN\_SL}$ , SLEEP_ENTRY_TIME = 00b or 01b	0.5	1	2	ms
$t_{DET\_SL\_PWM}$	Time needed to detect sleep command	SPEED_MODE = 01b (PWM mode) or 11b (Frequency mode), $V_{SPEED/WAKE} < V_{IL}$ (PWM mode and Frequency mode), SLEEP_ENTRY_TIME = 00b	0.035	0.05	0.065	ms
		SPEED_MODE = 01b (PWM mode), or 11b (Frequency mode), $V_{SPEED/WAKE} < V_{IL}$ (PWM mode and Frequency mode), SLEEP_ENTRY_TIME = 01b	0.14	0.2	0.26	ms
		SPEED_MODE = 01b (PWM mode) or 11b (Frequency mode) or 00b (analog mode), $V_{SPEED/WAKE} < V_{IL}$ (PWM mode and Frequency mode), $V_{SPEED/WAKE} < V_{EN\_SL}$ (analog mode), SLEEP_ENTRY_TIME = 10b	14	20	26	ms
		SPEED_MODE = 01b (PWM mode) or 11b (Frequency mode) or 00b (analog mode), $V_{SPEED/WAKE} < V_{IL}$ (PWM mode and Frequency mode), $V_{SPEED/WAKE} < V_{EN\_SL}$ (analog mode), SLEEP_ENTRY_TIME = 11b	140	200	260	ms
$t_{EN\_SL}$	Time needed to stop driving motor after detecting sleep command	$V_{SPEED/WAKE} < V_{EN\_SL}$ (analog mode) or $V_{SPEED/WAKE} < V_{IL}$ (PWM and frequency mode)		1	2	ms
<b>STANDBY MODE</b>						
$t_{EX\_SB\_DR\_ANA}$	Time taken to drive motor after exiting standby mode	SPEED_MODE = 00b (analog mode) $V_{SPEED} > V_{EN\_SB}$ , ISD detection disabled		6		ms
$t_{EX\_SB\_DR\_PWM}$	Time taken to drive motor after exiting standby mode	SPEED_MODE = 01b (PWM mode) $V_{SPEED} > V_{IH}$ , ISD detection disabled		6		ms
$t_{DET\_SB\_ANA}$	Time needed to detect standby mode	SPEED_MODE = 00b (analog mode) $V_{SPEED} < V_{EN\_SB}$	0.5	1	2	ms

## 6.5 Electrical Characteristics (continued)

4.5 V  $\leq$   $V_{PVDD}$   $\leq$  60 V,  $-40^\circ\text{C} \leq T_J \leq 150^\circ\text{C}$  (unless otherwise noted). Typical limits apply for  $T_A = 25^\circ\text{C}$ ,  $V_{PVDD} = 12\text{ V}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{EN\_SB\_PWM}$	Time needed to detect standby command	SPEED_MODE = 01b (PWM mode) or 11b (Frequency mode), $V_{SPEED} < V_{IL}$ , SLEEP_ENTRY_TIME = 00b	0.035	0.05	0.065	ms
		SPEED_MODE = 01b (PWM mode) or 11b (Frequency mode), $V_{SPEED} < V_{IL}$ , SLEEP_ENTRY_TIME = 01b	0.14	0.2	0.26	ms
		SPEED_MODE = 01b (PWM mode) or 11b (Frequency mode), $V_{SPEED} < V_{IL}$ , SLEEP_ENTRY_TIME = 10b	14	20	26	ms
		SPEED_MODE = 01b (PWM mode) or 11b (Frequency mode), $V_{SPEED} < V_{IL}$ , SLEEP_ENTRY_TIME = 11b	140	200	260	ms
$t_{EN\_SB\_DIG}$	Time needed to detect standby mode	SPEED_MODE = 10b (I <sup>2</sup> C mode), SPEED_CMD = 0		1	2	ms
$t_{EN\_SB}$	Time needed to stop driving motor after detecting standby command	$V_{SPEED} < V_{EN\_SL}$ (analog mode) or $V_{SPEED} < V_{IL}$ (PWM mode) or SPEED command = 0 (I <sup>2</sup> C mode)		1	2	ms

### PROTECTION CIRCUITS

$V_{AVDD\_UVLO}$	Regulator undervoltage lockout (AVDD-UVLO)	Supply rising	2.6	2.7	2.8	V
		Supply falling	2.6	2.7	2.8	V
$V_{AVDD\_UVLO\_HYS}$	Regulator UVLO hysteresis	Rising to falling threshold	150	190	240	mV
$t_{AVDD\_UVLO\_DEG}$	Regulator UVLO deglitch time				5	$\mu\text{s}$
$V_{DVDD\_UVLO}$	Digital regulator undervoltage lockout (DVDD-UVLO)	Supply rising	1.2	1.28	1.32	V
$V_{DVDD\_UVLO}$	Digital regulator undervoltage lockout (DVDD-UVLO)	Supply falling	1.18	1.23	1.3	V
$V_{PVDD\_UV}$	PVDD undervoltage lockout threshold	$V_{PVDD}$ rising	4.3	4.4	4.5	V
		$V_{PVDD}$ falling	4	4.1	4.25	
$V_{PVDD\_UV\_HYS}$	PVDD undervoltage lockout hysteresis	Rising to falling threshold	225	265	325	mV
$t_{PVDD\_UV\_DG}$	PVDD undervoltage deglitch time		10	20	30	$\mu\text{s}$
$V_{AVDD\_POR}$	AVDD supply POR threshold	AVDD rising	2.7	2.85	3.0	V
		AVDD falling	2.5	2.65	2.8	
$V_{AVDD\_POR\_HYS}$	AVDD POR hysteresis	Rising to falling threshold	170	200	250	mV
$t_{AVDD\_POR\_DG}$	AVDD POR deglitch time		7	12	22	$\mu\text{s}$
$V_{GVDD\_UV}$	GVDD undervoltage threshold	$V_{GVDD}$ rising	7.3	7.5	7.8	V
		$V_{GVDD}$ falling	6.4	6.7	6.9	V
$V_{GVDD\_UV\_HYS}$	GVDD undervoltage hysteresis	Rising to falling threshold	800	900	1000	mV
$t_{GVDD\_UV\_DG}$	GVDD undervoltage deglitch time		5	10	15	$\mu\text{s}$
$V_{BST\_UV}$	Bootstrap undervoltage threshold	$V_{BSTx} - V_{SHx}$ ; $V_{BSTx}$ rising	3.9	4.45	5	V
		$V_{BSTx} - V_{SHx}$ ; $V_{BSTx}$ falling	3.7	4.2	4.8	V
$V_{BST\_UV\_HYS}$	Bootstrap undervoltage hysteresis	Rising to falling threshold	150	220	285	mV

## 6.5 Electrical Characteristics (continued)

4.5 V  $\leq$   $V_{PVDD}$   $\leq$  60 V,  $-40^\circ\text{C} \leq T_J \leq 150^\circ\text{C}$  (unless otherwise noted). Typical limits apply for  $T_A = 25^\circ\text{C}$ ,  $V_{PVDD} = 12\text{ V}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
$t_{BST\_UV\_DG}$	Bootstrap undervoltage deglitch time	2	4	6	$\mu\text{s}$	
$V_{DS\_LVL}$	$SEL_{\_VDS\_LVL} = 0000$	0.04	0.06	0.08	V	
	$SEL_{\_VDS\_LVL} = 0001$	0.09	0.12	0.15	V	
	$SEL_{\_VDS\_LVL} = 0010$	0.14	0.18	0.23	V	
	$SEL_{\_VDS\_LVL} = 0011$	0.19	0.24	0.29	V	
	$SEL_{\_VDS\_LVL} = 0100$	0.23	0.3	0.37	V	
	$SEL_{\_VDS\_LVL} = 0101$	0.3	0.36	0.43	V	
	$SEL_{\_VDS\_LVL} = 0110$	0.35	0.42	0.5	V	
	$SEL_{\_VDS\_LVL} = 0111$	0.4	0.48	0.56	V	
	$SEL_{\_VDS\_LVL} = 1000$	0.5	0.6	0.7	V	
	$SEL_{\_VDS\_LVL} = 1001$	0.65	0.8	0.9	V	
	$SEL_{\_VDS\_LVL} = 1010$	0.85	1	1.15	V	
	$SEL_{\_VDS\_LVL} = 1011$	1	1.2	1.34	V	
	$SEL_{\_VDS\_LVL} = 1100$	1.2	1.4	1.58	V	
	$SEL_{\_VDS\_LVL} = 1101$	1.4	1.6	1.78	V	
	$SEL_{\_VDS\_LVL} = 1110$	1.6	1.8	2	V	
	$SEL_{\_VDS\_LVL} = 1111$	1.7	2	2.2	V	
$V_{SENSE\_LVL}$	$V_{SENSE}$ overcurrent protection threshold	LSS to GND pin = 0.5V	0.48	0.5	0.52	V
$t_{DS\_BLK}$	$V_{DS}$ overcurrent protection blanking time		0.5	1	2.7	$\mu\text{s}$
$t_{DS\_DG}$	$V_{DS}$ and $V_{SENSE}$ overcurrent protection deglitch time		1.5	3	5	$\mu\text{s}$
$t_{SD\_SINK\_DIG}$	DRVOFF peak sink current duration		3	5	7	$\mu\text{s}$
$t_{SD\_DIG}$	DRVOFF digital shutdown delay		0.5	1.5	2.2	$\mu\text{s}$
$t_{SD}$	DRVOFF analog shutdown delay		7	14	21	$\mu\text{s}$
$T_{OTSD}$	Thermal shutdown temperature	$T_J$ rising	160	170	187	$^\circ\text{C}$
$T_{HYS}$	Thermal shutdown hysteresis		16	20	23	$^\circ\text{C}$
<b>I<sup>2</sup>C Serial Interface</b>						
$V_{I2C\_L}$	LOW-level input voltage		-0.5	0.3*AVD D	V	
$V_{I2C\_H}$	HIGH-level input voltage		0.7*AVD D	5.5	V	
$V_{I2C\_HYS}$	Hysteresis		0.05*AV DD		V	
$V_{I2C\_OL}$	LOW-level output voltage	open-drain at 2mA sink current	0	0.4	V	
$I_{I2C\_OL}$	LOW-level output current	$V_{I2C\_OL} = 0.6\text{V}$		6	mA	
$I_{I2C\_IL}$	Input current on SDA and SCL		-10 <sup>(1)</sup>	10 <sup>(1)</sup>	$\mu\text{A}$	
$C_i$	Capacitance for SDA and SCL			10	pF	
$t_{of}$	Output fall time from $V_{I2C\_H}$ (min) to $V_{I2C\_L}$ (max)	Standard Mode		250 <sup>(2)</sup>	ns	
		Fast Mode		250 <sup>(2)</sup>	ns	
$t_{SP}$	Pulse width of spikes that must be suppressed by the input filter	Fast Mode	0	50 <sup>(3)</sup>	ns	
<b>EEPROM</b>						
$EE_{Prog}$	Programing voltage		1.35	1.5	1.65	V
$EE_{RET}$	Retention	$T_A = 25^\circ\text{C}$		100	Years	
		$T_J = -40$ to $150^\circ\text{C}$		10	Years	

## 6.5 Electrical Characteristics (continued)

4.5 V ≤  $V_{PVDD}$  ≤ 60 V,  $-40^\circ\text{C} \leq T_J \leq 150^\circ\text{C}$  (unless otherwise noted). Typical limits apply for  $T_A = 25^\circ\text{C}$ ,  $V_{PVDD} = 12\text{ V}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
EE <sub>END</sub>	Endurance	$T_J = -40$ to $150^\circ\text{C}$	1000			Cycles
		$T_J = -40$ to $85^\circ\text{C}$	20000			Cycles

- (1) If AVDD is switched off, I/O pins must not obstruct the SDA and SCL lines.
- (2) The maximum  $t_f$  for the SDA and SCL bus lines (300 ns) is longer than the specified maximum  $t_{of}$  for the output stages (250 ns). This allows series protection resistors ( $R_s$ ) to be connected between the SDA/SCL pins and the SDA/SCL bus lines without exceeding the maximum specified  $t_f$ .
- (3) Input filters on the SDA and SCL inputs suppress noise spikes of less than 50 ns

## 6.6 Characteristics of the SDA and SCL bus for Standard and Fast mode

over operating free-air temperature range (unless otherwise noted)

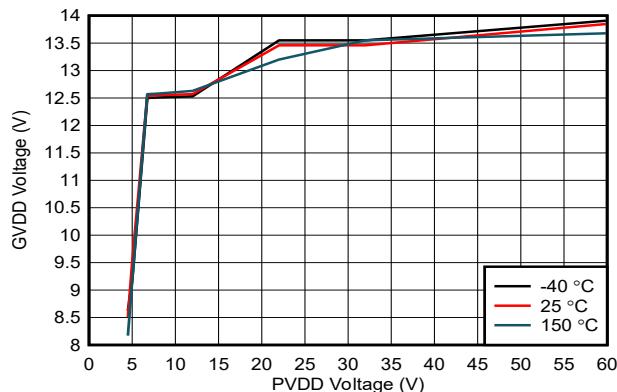
PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
<b>Standard-mode</b>						
$f_{SCL}$	SCL clock frequency		0	100		kHz
$t_{HD\_STA}$	Hold time (repeated) START condition	After this period, the first clock pulse is generated	4			$\mu\text{s}$
$t_{LOW}$	LOW period of the SCL clock		4.7			$\mu\text{s}$
$t_{HIGH}$	HIGH period of the SCL clock		4			$\mu\text{s}$
$t_{SU\_STA}$	Set-up time for a repeated START condition		4.7			$\mu\text{s}$
$t_{HD\_DAT}$	Data hold time (1)	I2C bus devices	0 (2)		(3)	$\mu\text{s}$
$t_{SU\_DAT}$	Data set-up time		250			ns
$t_r$	Rise time for both SDA and SCL signals			1000		ns
$t_f$	Fall time of both SDA and SCL signals (2) (5) (6) (7)			300		ns
$t_{SU\_STO}$	Set-up time for STOP condition		4			$\mu\text{s}$
$t_{BUF}$	Bus free time between STOP and START condition		4.7			$\mu\text{s}$
$C_b$	Capacitive load for each bus line (8)			400		pF
$t_{VD\_DAT}$	Data valid time (9)			3.45 (3)		$\mu\text{s}$
$t_{VD\_ACK}$	Data valid acknowledge time (10)			3.45 (3)		$\mu\text{s}$
$V_{nL}$	Noise margin at the LOW level	For each connected device (including hysteresis)	0.1*AVDD			V
$V_{nh}$	Noise margin at the HIGHlevel	For each connected device (including hysteresis)	0.2*AVDD			V
<b>Fast-mode</b>						
$f_{SCL}$	SCL clock frequency		0	400		KHz
$t_{HD\_STA}$	Hold time (repeated) START condition	After this period, the first clock pulse is generated	0.6			$\mu\text{s}$
$t_{LOW}$	LOW period of the SCL clock		1.3			$\mu\text{s}$
$t_{HIGH}$	HIGH period of the SCL clock		0.6			$\mu\text{s}$
$t_{SU\_STA}$	Set-up time for a repeated START condition		0.6			$\mu\text{s}$
$t_{HD\_DAT}$	Data hold time (1)		0 (2)		(3)	$\mu\text{s}$
$t_{SU\_DAT}$	Data set-up time		100 (4)			ns
$t_r$	Rise time for both SDA and SCL signals		20	300		ns
$t_f$	Fall time of both SDA and SCL signals (2) (5) (6) (7)		20 x (AVDD/5.5V)	300		ns

over operating free-air temperature range (unless otherwise noted)

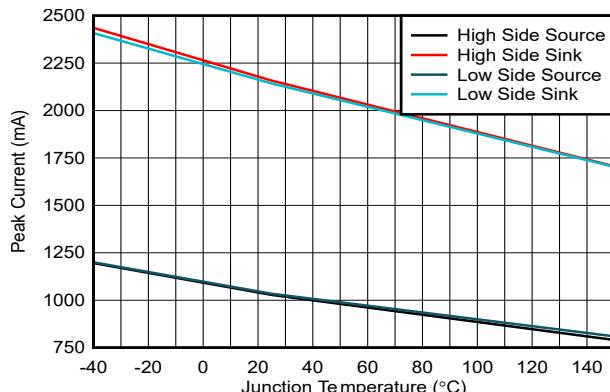
PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$t_{SU\_STO}$	Set-up time for STOP condition		0.6			μs
$t_{BUF}$	Bus free time between STOP and START condition		1.3			μs
$C_b$	Capacitive load for each bus line <sup>(8)</sup>		400			pF
$t_{VD\_DAT}$	Data valid time <sup>(9)</sup>		0.9 <sup>(3)</sup>			μs
$t_{VD\_ACK}$	Data valid acknowledge time <sup>(10)</sup>		0.9 <sup>(3)</sup>			μs
$V_{nL}$	Noise margin at the LOW level	For each connected device (including hysteresis)	0.1*AVD D			V
$V_{nh}$	Noise margin at the HIGHlevel	For each connected device (including hysteresis)	0.2*AVD D			V

- (1)  $t_{HD\_DAT}$  is the data hold time that is measured from the falling edge of SCL, applies to data in transmission and the acknowledge.
- (2) A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the  $V_{IH(min)}$  of the SCL signal) to bridge the undefined region of the falling edge of SCL.
- (3) The maximum  $t_{HD\_DAT}$  could be 3.45 μs and .9 μs for Standard-mode and Fast-mode, but must be less than the maximum of  $t_{VD\_DAT}$  or  $t_{VD\_ACK}$  by a transition time. This maximum must only be met if the device does not stretch the LOW period ( $t_{LOW}$ ) of the SCL signal. If the clock stretched the SCL, the data must be valid by the set-up time before it releases the clock.
- (4) A Fast-mode I2C-bus device can be used in a Standard-mode I2C-bus system, but the requirement  $t_{SU\_DAT}$  250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line  $t_{r(max)} + t_{SU\_DAT} = 1000 + 250 = 1250$  ns (according to the Standard-mode I2C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.
- (5) If mixed with HS-mode devices, faster fall times according to Table 10 are allowed.
- (6) The maximum  $t_f$  for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage  $t_f$  is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified  $t_f$ .
- (7) In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.
- (8) The maximum bus capacitance allowable may vary from the value depending on the actual operating voltage and frequency of the application.
- (9)  $t_{VD\_DAT}$  = time for data signal from SCL LOW to SDA output (HIGH or LOW, depending on which one is worse).
- (10)  $t_{VD\_ACK}$  = time for Acknowledgement signal from SCL LOW to SDA output (HIGH or LOW, depending on which one is worse).

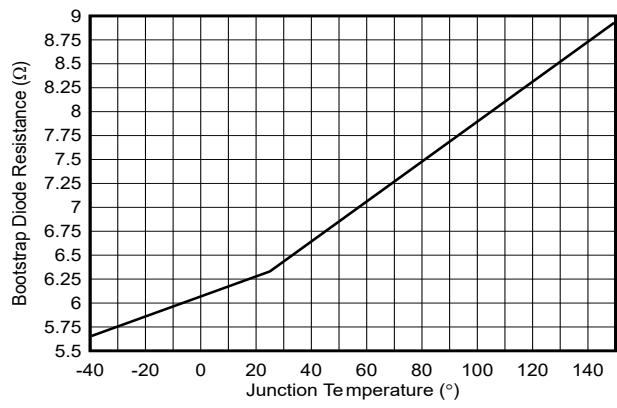
## 6.7 Typical Characteristics



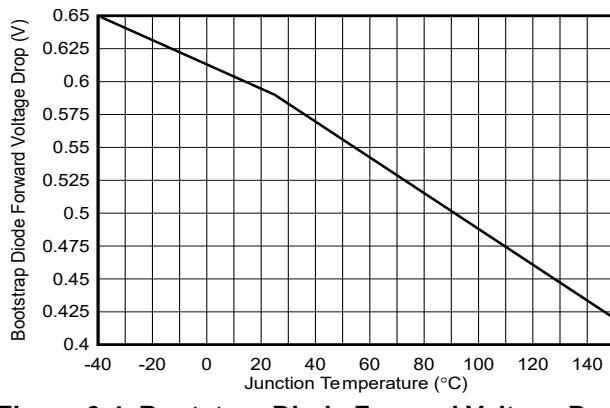
**Figure 6-1. GVDD Voltage over PVDD Voltage**



**Figure 6-2. Driver Peak Current over Junction Temperature**



**Figure 6-3. Bootstrap Diode Resistance over Junction Temperature**



**Figure 6-4. Bootstrap Diode Forward Voltage Drop over Junction Temperature**

## 7 Detailed Description

### 7.1 Overview

The MCF8329HS-Q1 provides a code-free sensorless FOC solution with an integrated three-phase gate driver for driving high-speed brushless-DC motors. Motor current is sensed using an integrated current sensing amplifier and one external sense resistor in a single shunt configuration. The device can operate from a single power supply and integrates an LDO that generates the necessary voltage rails for the device and can be used to power external circuits.

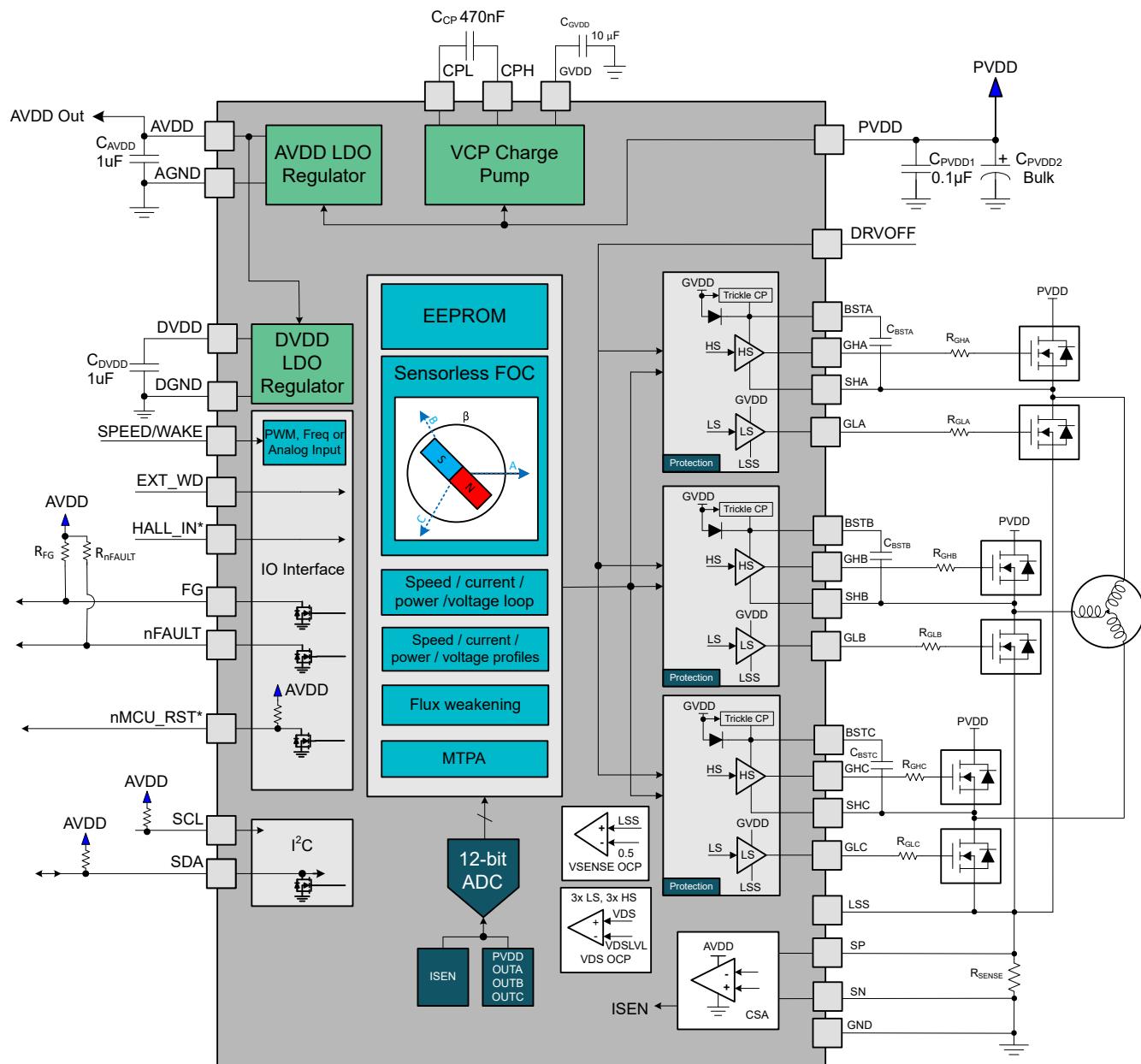
MCF8329HS-Q1 implements single shunt sensorless FOC; therefore, an external microcontroller is not required to spin the brushless DC motor. The algorithm is implemented in a fixed-function state machine, so no coding is needed. The algorithm is highly configurable through register settings ranging from motor start-up behavior to closed-loop operation. Register settings can be stored in non-volatile EEPROM, which allows the device to operate stand-alone once it has been configured. The device receives a reference command through a PWM input, analog voltage, frequency input, or I<sup>2</sup>C command. The device can be configured to control motor speed (speed control) DC input power (power control) or the quadrature (q-) axis current (current control) or directly the voltage applied (v<sub>q</sub> and v<sub>d</sub>) to the motor (modulation index control or open loop voltage control).

In-built protection features include power-supply undervoltage lockout (PVDD\_UVLO), regulator undervoltage lockout (GVDD\_UV), bootstrap undervoltage lockout (BST\_UV), VDS overcurrent protection (OCP), sense resistor overcurrent protection (SEN\_OCP), motor lock detection and overtemperature shutdown (OTSD). Fault events are indicated by the nFAULT pin with detailed fault information available in the status registers.

A standard I<sup>2</sup>C provides a simple method for configuring the various device settings and reading fault diagnostic information through an external controller.

The MCF8329HS-Q1 device is available in a 0.5mm pin pitch, wettable flank, WQFN surface-mount package. The WQFN package size is 6mm × 4mm with a height of 0.8mm.

## 7.2 Functional Block Diagram



\*HALL\_IN and nMCU\_RST are mux'ed functions on pin 30

Figure 7-1. MCF8329HS-Q1 Functional Block Diagram

## 7.3 Feature Description

Table 7-1 lists the recommended values of the external components for the driver.

**Table 7-1. MCF8329HS-Q1 External Components**

COMPONENTS	PIN 1	PIN 2	RECOMMENDED
$C_{PVDD1}$	PVDD	GND	X7R, 0.1 $\mu$ F, >2x PVDD-rated
$C_{PVDD2}$	PVDD	GND	$\geq 10\mu$ F, >2x PVDD-rated
$C_{CP}$	CPH	CPL	X7R, 470nF, PVDD-rated
$C_{AVDD}$	AVDD	AGND	X7R, 1 $\mu$ F or 2.2 $\mu$ F, 10V
$C_{GVDD}$	GVDD	GND	X7R, $\geq 10\mu$ F, 30V
$C_{DVDD}$	DVDD	DGND	X7R, 1 $\mu$ F, 10V
$C_{BSTx}$	BSTx	SHx	X7R, 1 $\mu$ F, 25V
$R_{nFAULT}$	1.8 to 5 V Supply	nFAULT	5.1k $\Omega$ , Pullup resistor
$R_{FG}$	1.8 to 5 V Supply	FG	5.1k $\Omega$ , Pullup resistor
$R_{SDA}$	1.8 to 5 V Supply	SDA	5.1k $\Omega$ , Pullup resistor
$R_{SCL}$	1.8 to 5 V Supply	SCL	5.1k $\Omega$ , Pullup resistor

### Note

1. AVDD and DVDD capacitors should have an effective capacitance between 0.5 $\mu$ F and 2.8 $\mu$ F after operating voltage (AVDD or DVDD) and temperature derating.
2. The internal pull-up resistor (to AVDD) for both FG and nFAULT pins can be enabled by configuring PULLUP\_ENABLE to 1b. Any change to this bit needs to be written to EEPROM followed by a power recycle to take effect. When PULLUP\_ENABLE is set to 1b, no external pull-up resistor should be provided.
3. SPEED/WAKE pin has an internal pull-down resistor of 1-M $\Omega$ . In analog speed input mode, a suitable R-C filter can be added externally to reduce noise. In PWM speed input mode, SPEED\_PIN\_GLITCH\_FILTER can be appropriately configured for glitch rejection.

### 7.3.1 Three Phase BLDC Gate Drivers

The MCF8329HS-Q1 device integrates three half-bridge gate drivers, each capable of driving high-side and low-side N-channel power MOSFETs. A charge pump is used to generate the GVDD to supply the correct gate bias voltage across a wide operating voltage range. The low side gate outputs are driven directly from GVDD, while the high side gate outputs are driven using a bootstrap circuit with an integrated diode, and an internal trickle charge pump provides support for 100% duty cycle operation.

### 7.3.2 Gate Drive Architecture

The gate driver device use a complimentary, push-pull topology for both the high-side and low-side drivers. This topology allows for both a strong pullup and pulldown of the external MOSFET gates. The low side gate drivers are supplied directly from the GVDD regulator supply. For the high-side gate drivers a bootstrap diode and capacitor are used to generate the floating high-side gate voltage supply. The bootstrap diode is integrated and an external bootstrap capacitor is used on the BSTx pin. To support 100% duty cycle control, a trickle charge pump is integrated into the device. The trickle charge pump is connected to the BSTx node to prevent voltage drop due to the leakage currents of the driver and external MOSFET.

The high-side gate driver has semi-active pull down and low side gate has passive pull down to help prevent the external MOSFET from turning ON during sleep state or when power supply is disconnected.

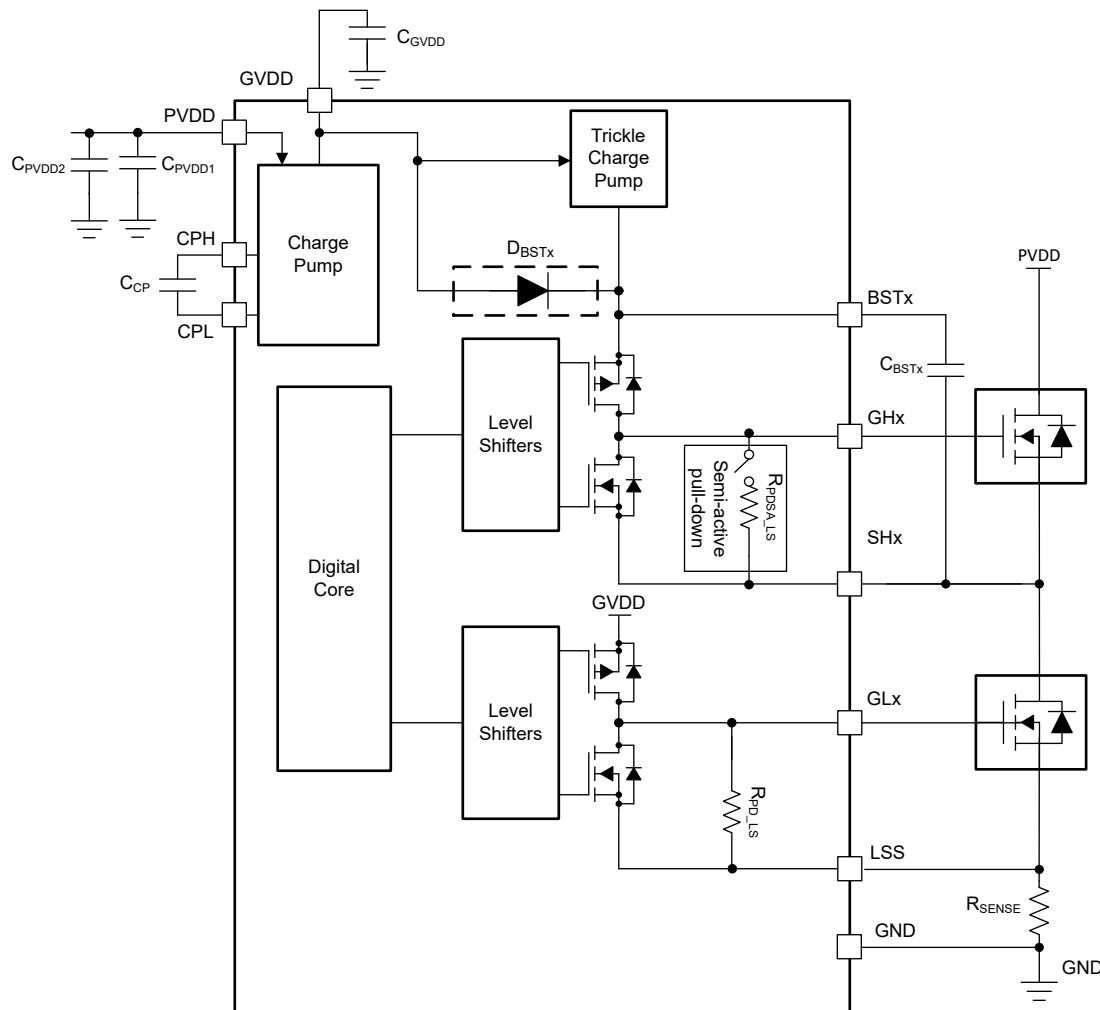


Figure 7-2. Gate Driver Block Diagram

#### 7.3.2.1 Dead time and Cross Conduction Prevention

The MCF8329HS-Q1 provides digital dead time insertion between the high side and low side PWM signals, to prevent both external MOSFETs of each half-bridge from switching on at the same time. Digital dead time can be adjusted by configuring the EEPROM register DIG\_DEAD\_TIME.

The applied dead time depends on the internal clock frequency configured by CLOCK\_FREQUENCY. Refer to the *Dead time vs clock frequency* table for more details.

#### 7.3.3 AVDD Linear Voltage Regulator

A 3.3V or 5V (configured by AVDD\_VOL\_SEL), 50mA linear regulator is integrated into the MCF8329HS-Q1 and is available for use by external circuitry. This regulator can provide the supply voltage for a low-power MCU or other circuitry with low supply current requirements. The output of the AVDD regulator is bypassed near the AVDD pin with a X7R, 1 $\mu$ F or 2.2 $\mu$ F, 10V ceramic capacitor routed back to the AGND pin.

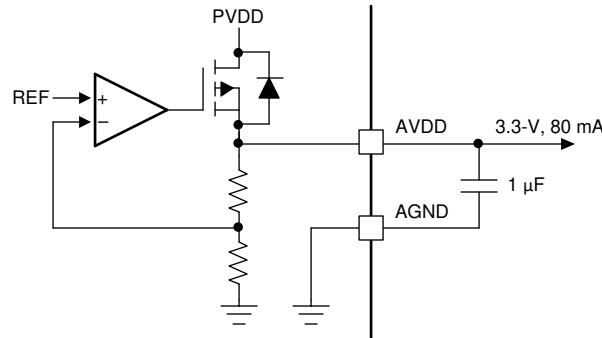


Figure 7-3. AVDD Linear Regulator Block Diagram

The power dissipated in the device by the AVDD linear regulator can be calculated as shown in [Equation 1](#),

$$P = (V_{PVDD} - V_{AVDD}) \times I_{AVDD} \quad (1)$$

For example, at a  $V_{PVDD}$  of 24V, drawing 20mA out of AVDD (output at 3.3V) results in power dissipation as shown in [Equation 2](#),

$$P = (24 \text{ V} - 3.3 \text{ V}) \times 20 \text{ mA} = 414 \text{ mW} \quad (2)$$

### 7.3.4 Low-Side Current Sense Amplifier

MCF8329HS-Q1 integrates a high-performance low-side current sense amplifier for current measurements using a low-side shunt resistor. Low-side current measurements are used for multiple control features and protections in MCF8329HS-Q1. The current sense amplifiers feature configurable gain (5 V/V, 10 V/V, 20 V/V, and 40 V/V) through EEPROM setting. The current sense amplifier can support sensing bidirectional current through the low-side shunt resistor.

MCF8329HS-Q1 internally generates common mode voltage of  $V_{REF}/2$  to obtain maximum resolution for current measurement for both the direction of current.  $V_{REF}$  is an internally generated reference voltage having a typical value of 3 V.

Use [Equation 3](#) to design the value of the shunt resistor ( $R_{SENSE}$ ) connected between SP and SN, for the range of current ( $I$ ) through the low side single shunt and the selected current sense amplifier gain configured by EEPROM bits CSA\_GAIN.

$$R_{SENSE} = \frac{V_{SO} - \frac{V_{REF}}{2}}{CSA\_GAIN \times I} \quad (3)$$

**Note**

1. TI recommends designing the shunt resistor  $R_{SENSE}$  value to limit the current sense amplifier output voltage ( $V_{SO}$ ) between 0.25V and 3V across the operating range of low-side single shunt resistor current ( $I$ ) at the selected gain of CSA\_GAIN. Appropriately size the shunt resistor power rating based on the  $I^2R_{SENSE}$  losses with sufficient margin.
2. SINGLE\_SHUNT\_BLANKING\_TIME can be used to set the blanking window for current sampling (after a PWM edge) till the sensed current settles to a noise-free, steady value. A higher SINGLE\_SHUNT\_BLANKING\_TIME reduces noise in sensed current but will also reduce the maximum modulation index that can be applied - SINGLE\_SHUNT\_BLANKING\_TIME should be suitably set to optimize between maximum modulation index (motor speed) and minimal noise in sensed current.
3. DYNAMIC\_SAMPLING\_EN can be set to 1b to enable dynamic current sampling to reduce the current harmonics caused by blanking time; when dynamic current sampling is enabled there maybe a DC offset in motor phase currents.

### 7.3.5 Device Interface Modes

MCF8329HS-Q1 supports the I<sup>2</sup>C interface to provide end application design suited for either flexibility or simplicity. Along with the I<sup>2</sup>C interface, the device supports I/O pins like FG, nFAULT, EXT\_WD, HALL\_IN, nMCU\_RST, SPEED/WAKE, DRVOFF.

#### 7.3.5.1 Interface - Control and Monitoring

- **DRVOFF:** When DRVOFF pin is driven 'High', MCF8329HS-Q1 turns off all external MOSFETs by putting the gate drivers into the pull-down state. When DRVOFF is driven 'Low', MCF8329HS-Q1 returns to normal state of operation, as if restarting the motor. DRVOFF does not cause the device to go to sleep or standby mode; the digital core is still active.
- **SPEED/WAKE:** The SPEED/WAKE pin is used to control motor speed (or power or current or modulation index) and wake up MCF8329HS-Q1 from sleep mode. SPEED/WAKE pin can be configured to accept PWM, frequency or analog control input signals. The pin is used to enter and exit from sleep and standby mode.
- **EXT\_WD:** The EXT\_WD pin can be used to provide a watchdog signal input from an external MCU for monitoring the MCU operation.
- **nMCU\_RST:** The nMCU\_RST pin provides an active low signal to reset an external MCU when a watchdog fault occurs.
- **HALL\_IN:** The HALL\_IN pin (mux'ed with nMCU\_RST) can be used to provide a digital Hall input signal for redundancy in motor lock detection.
- **FG:** The FG pin provides pulses which are proportional to motor speed (see [Section 7.3.22](#)).
- **nFAULT:** The nFAULT pin provides fault status in device or motor operation.

#### 7.3.5.2 I<sup>2</sup>C Interface

The MCF8329HS-Q1 supports an I<sup>2</sup>C serial communication interface that allows an external controller to send and receive data. This I<sup>2</sup>C interface lets the external controller configure the EEPROM and read detailed fault and motor state information. The I<sup>2</sup>C bus is a two-wire interface using the SCL and SDA pins which are described as follows:

- The SCL pin is the clock signal input.
- The SDA pin is the data input and output.

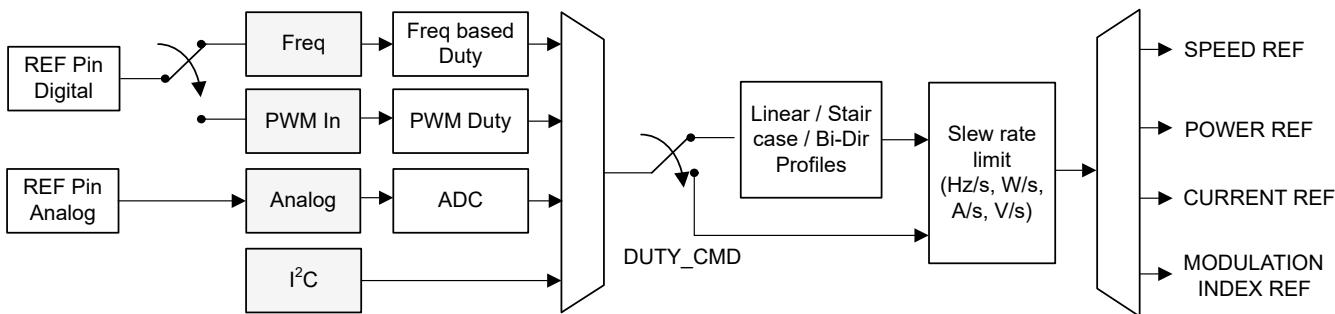
### 7.3.6 Motor Control Input Options

The MCF8329HS-Q1 offers four ways of controlling the motor:

1. SPEED Control: In speed control mode, the speed of the motor is controlled using a closed loop PI control according to the input reference.
2. POWER Control: In power control mode, the DC input power of the inverter power stage is controlled using a closed loop PI control according to the input reference.
3. CURRENT Control: In current control mode, the torque controlling current ( $i_q$ ) is controlled using a closed loop PI control according to the input reference. In this mode the speed/power control loop is disabled.
4. MODULATION INDEX Control (VOLTAGE Control): In voltage control mode, the voltage applied to the motor is controlled according to the input reference.

The device can accept four types of input reference signal as configured by SPEED\_MODE.

- PWM input on SPEED/WAKE pin by varying duty cycle of input signal
- Frequency input on SPEED/WAKE pin by varying frequency of input signal
- Analog input on SPEED/WAKE pin by varying amplitude of input signal
- Over I<sup>2</sup>C by configuring DIGITAL\_SPEED\_CTRL

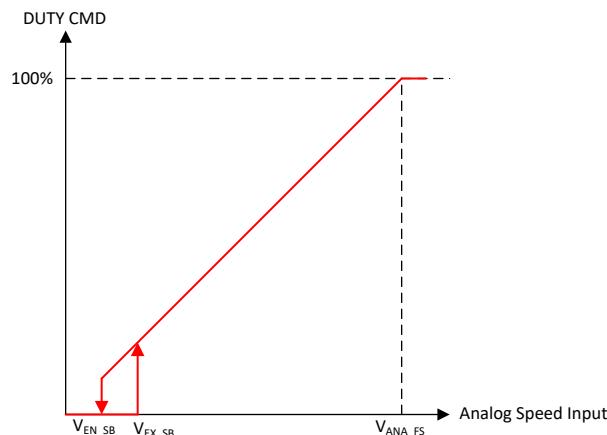


**Figure 7-4. Multiplexing the Reference Input Command**

The signal path from REF (SPEED/WAKE) pin input (or I<sup>2</sup>C based speed input) to output reference (SPEED REF or POWER REF or CURRENT REF or MODULATION INDEX REF) shown in [Figure 7-4](#).

#### 7.3.6.1 Analog-Mode Motor Control

Analog input based motor control can be configured by setting SPEED\_MODE to 00b. In this mode, the duty command (DUTY\_CMD) varies with the analog voltage input ( $V_{SPEED}$ ) on the SPEED/WAKE pin. When  $0 < V_{SPEED} < V_{EN\_SB}$ , DUTY\_CMD is set to zero and the motor is stopped. When  $V_{EN\_SB} < V_{SPEED} < V_{ANA\_FS}$ , DUTY\_CMD varies linearly with  $V_{SPEED}$  as shown in [Figure 7-5](#). When  $V_{SPEED} > V_{ANA\_FS}$ , DUTY\_CMD is clamped to 100%.



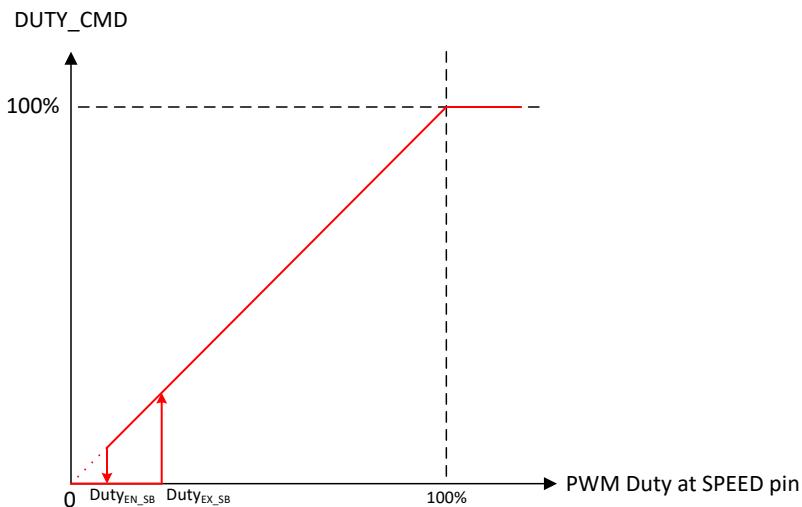
**Figure 7-5. Analog-Mode Speed Control**

### 7.3.6.2 PWM-Mode Motor Control

PWM-based motor control can be configured by setting SPEED\_MODE to 01b. In this mode, the PWM duty cycle applied to the SPEED/WAKE pin can be varied from 0 to 100%, and duty command (DUTY\_CMD) varies linearly with the applied PWM duty cycle. When  $0 \leq \text{Duty}_{\text{SPEED}} \leq \text{Duty}_{\text{EN\_SB}}$ , DUTY\_CMD is set to zero. When  $\text{Duty}_{\text{EX\_SB}} \leq \text{Duty}_{\text{SPEED}} \leq 100\%$ , DUTY\_CMD varies linearly with Duty<sub>SPEED</sub> as shown in Figure 7-6. Duty<sub>EX\_SB</sub> and Duty<sub>EN\_SB</sub> are the standby entry and exit thresholds - refer Section 7.4.1.2 for more information on Duty<sub>EX\_SB</sub> and Duty<sub>EN\_SB</sub>. The frequency of the PWM input signal applied to the SPEED/WAKE pin is defined as f<sub>PWM</sub> and the range for this frequency can be configured through SPEED\_RANGE\_SEL.

**Note**

1. f<sub>PWM</sub> is the frequency of the PWM signal the device can accept at the SPEED/WAKE pin to control motor speed. It does not correspond to the PWM output frequency that is applied to the motor phases. The PWM output frequency can be configured through PWM\_FREQ\_OUT (see Section 7.3.18).
2. SLEEP\_ENTRY\_TIME should be set longer than the off time in the PWM signal ( $V_{\text{SPEED}} < V_{\text{IL}}$ ) at the lowest duty input. For example, if f<sub>PWM</sub> is 10 kHz and the lowest duty input is 2%, SLEEP\_ENTRY\_TIME should be more than 98  $\mu\text{s}$  to ensure there is no unintended sleep/standby entry.



**Figure 7-6. PWM-Mode Motor Control**

### 7.3.6.3 Frequency-Mode Motor Control

Frequency-based motor control is configured by setting SPEED\_MODE to 11b. In this mode, duty command varies linearly as a function of the frequency of the square wave input at the SPEED (SPEED/WAKE) pin. When  $0 \leq \text{Freq}_{\text{SPEED}} \leq \text{Freq}_{\text{EN\_SB}}$ , DUTY\_CMD is set to zero. When  $\text{Freq}_{\text{EX\_SB}} \leq \text{Freq}_{\text{SPEED}} \leq \text{INPUT\_MAXIMUM\_FREQ}$ , DUTY\_CMD varies linearly with Freq<sub>SPEED</sub> as shown in Figure 7-7. Freq<sub>EX\_SB</sub> and Freq<sub>EN\_SB</sub> are the standby entry and exit thresholds - refer Section 7.4.1.2 for more information on Freq<sub>EX\_SB</sub> and Freq<sub>EN\_SB</sub>. Input frequency greater than INPUT\_MAXIMUM\_FREQ clamps the DUTY\_CMD to 100%.

**Note**

TI recommends a logic low signal on the SPEED/WAKE pin to provide a zero reference in frequency mode control.

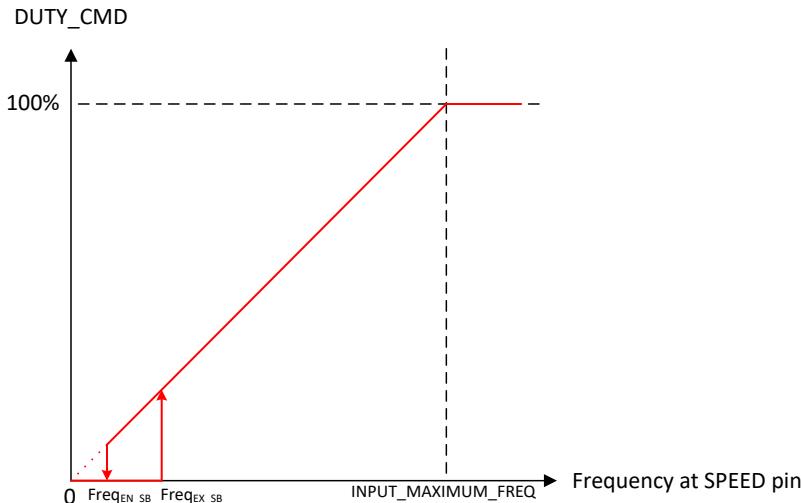


Figure 7-7. Frequency-Mode Motor Control

#### 7.3.6.4 I<sup>2</sup>C based Motor Control

I<sup>2</sup>C based serial interface can be used for motor control by setting SPEED\_MODE to 10b. In this mode, the duty command can be written directly into DIGITAL\_SPEED\_CTRL register. The sleep entry and exit are controlled through SLEEP/WAKE as described in [Table 7-7](#).

#### 7.3.6.5 Input Control Signal Profiles

MCF8329HS-Q1 supports three different kinds of profiles (linear, step, forward-reverse) to convert the DUTY\_CMD to the reference control signal. The input control reference signal can be motor speed, DC input power, motor current ( $i_q$ ), or motor voltage (modulation index control) as configured by CTRL\_MODE. The different profiles can be configured through REF\_PROFILE\_CONFIG. When REF\_PROFILE\_CONFIG is set to 00b, the profiler is not applied and the input reference is same as the duty command as explained in [Section 7.3.6.5.5](#).

In speed control mode, the profiler output REF\_X corresponds to percentage of Maximum Speed (configured by MAX\_SPEED) as shown in [Equation 4](#). In power control mode, the profiler output REF\_X corresponds to percentage of Maximum Power (configured by MAX\_POWER) as shown in [Equation 5](#). In the current control mode ( $i_q$  control) the profiler output REF\_X corresponds to the percentage of ILIMIT as shown in [Equation 6](#). In voltage control mode (Modulation index control mode) REF\_X corresponds to the percentage of  $V_d$  and  $V_q$  modulation index applied voltage to the motor as shown in [Equation 7](#).

$$SPEED\ REF(Hz) = \frac{REF\_X}{256} \times \text{Maximum Speed (Hz)} \quad (4)$$

$$POWER\ REF(W) = \frac{REF\_X}{256} \times \text{Maximum Power (W)} \quad (5)$$

$$CURRENT\ (i_q)\ REF(A) = \frac{REF\_X}{256} \times ILIMIT\ (A) \quad (6)$$

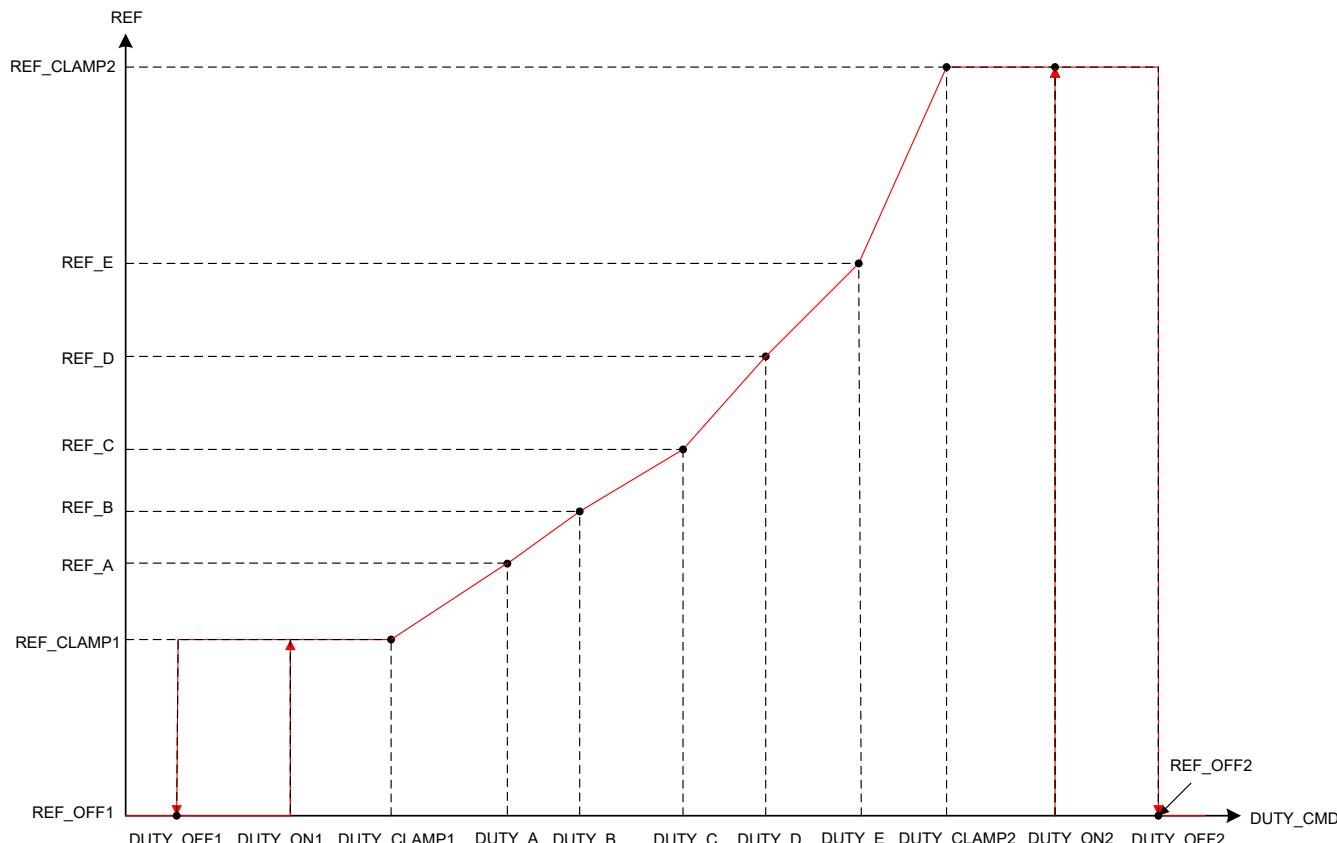
$$MODULATION\ INDEX\ REF(V_s) = \frac{REF\_X}{256} \times 100\% \quad (7)$$

### 7.3.6.5.1 Linear Control Profiles

#### Note

For all three profiles (linear, step, forward/reverse),

- When MCF8329HS-Q1 is configured as a sleep device, a zero input reference (0-V in analog mode, 0% duty in PWM mode, `DIGITAL_SPEED_CTRL` = 0b in I<sup>2</sup>C mode or 0-Hz in frequency mode) will stop the motor.
- When MCF8329HS-Q1 is configured as a standby device, a zero input command will result in motor operating at reference level (speed, power, current or voltage) set by `REF_OFF1`.



**Figure 7-8. Linear Control Profiles**

Linear control profiles can be configured by setting `REF_PROFILE_CONFIG` to 01b. Linear profiles feature input control references which change linearly between `REF_CLAMP1` and `REF_CLAMP2` with different slopes which can be set by configuring `DUTY_x` and `REF_x` combination.

- `DUTY_OFF1` configures the duty command below which the reference will be `REF_OFF1`.
- `DUTY_OFF1` and `DUTY_ON1` configures a hysteresis around reference control input `REF_CLAMP1` and `REF_OFF1` as shown in Figure 7-8.
- `DUTY_CLAMP1` configures the duty command till which reference will be constant with a value `REF_CLAMP1`. `DUTY_CLAMP1` can be placed anywhere between `DUTY_OFF1` and `DUTY_A`.
- `DUTY_A` configures the duty command for reference `REF_A`. The reference changes from `REF_CLAMP1` to `REF_A` linearly between `DUTY_CLAMP1` and `DUTY_A`. `DUTY_A` to `DUTY_E` has to be in the same order as shown in Figure 7-8.
- `DUTY_B` configures the duty command for reference `REF_B`. The reference changes linearly between `DUTY_A` and `DUTY_B`.

- DUTY\_C configures the duty command for reference REF\_C. The reference changes linearly between DUTY\_B and DUTY\_C.
- DUTY\_D configures the duty command for reference REF\_D. The reference changes linearly between DUTY\_C and DUTY\_D.
- DUTY\_E configures the duty command for reference REF\_E. The reference changes linearly between DUTY\_D and DUTY\_E.
- DUTY\_CLAMP2 configures the duty command above which the reference will be constant at REF\_CLAMP2. REF\_CLAMP2 configures this constant reference between DUTY\_CLAMP2 and DUTY\_OFF2. The reference changes linearly between DUTY\_E and DUTY\_CLAMP2. DUTY\_CLAMP2 can be placed anywhere between DUTY\_E and DUTY\_OFF2.
- DUTY\_OFF2 and DUTY\_ON2 configures a hysteresis around reference control input REF\_CLAMP2 and REF\_OFF2 as shown in [Figure 7-8](#).
- DUTY\_OFF2 configures the duty command above which the reference will change from REF\_CLAMP2 to REF\_OFF2.

#### 7.3.6.5.2 Staircase Control Profiles

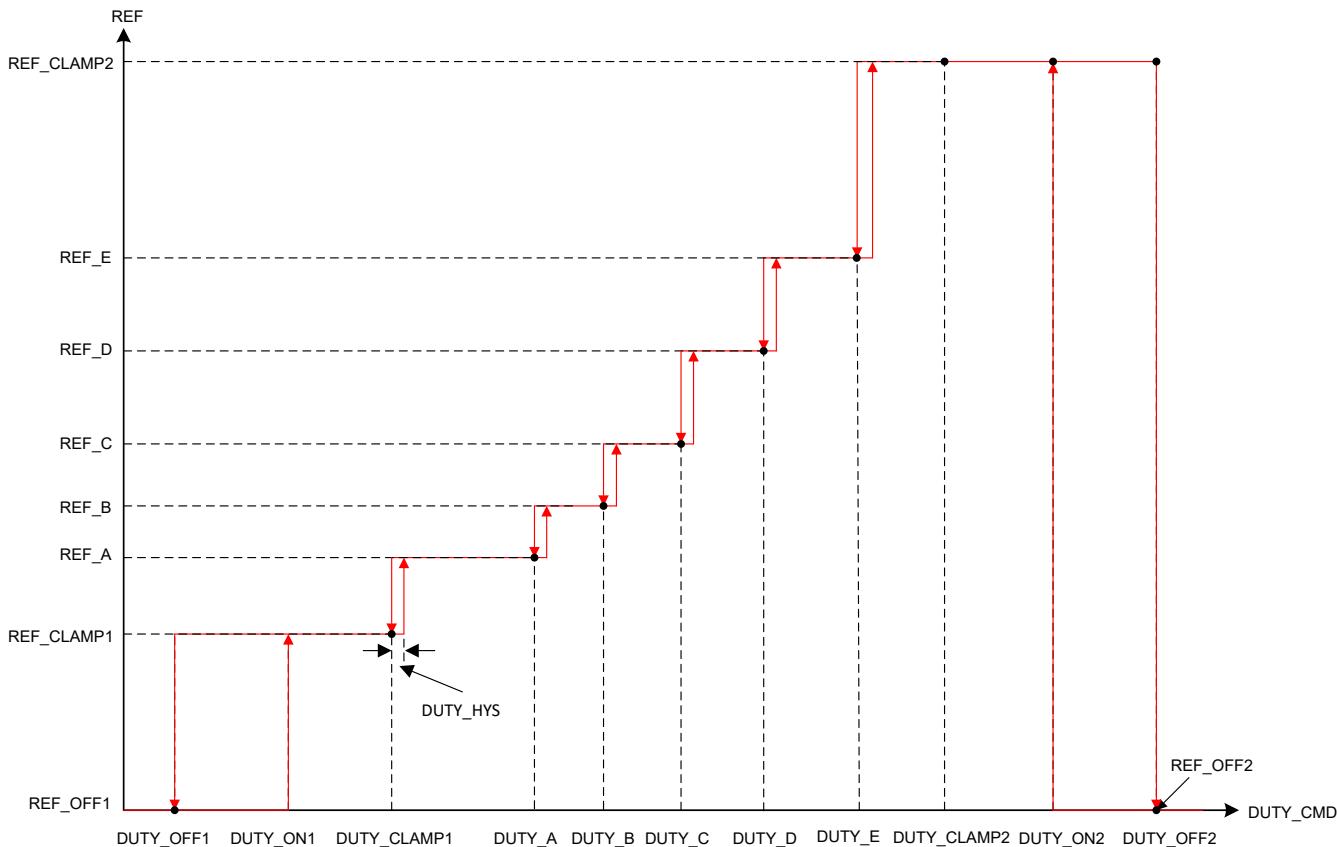


Figure 7-9. Staircase Control Profiles

Staircase control profiles can be configured by setting REF\_PROFILE\_CONFIG to 10b. Staircase profiles feature input control reference changes in steps between REF\_CLAMP1 and REF\_CLAMP2, by configuring DUTY\_x and REF\_x.

- DUTY\_OFF1 configures the duty command below which the reference will be REF\_OFF1.
- DUTY\_OFF1 and DUTY\_ON1 configures a hysteresis around reference control input REF\_CLAMP1 and REF\_OFF1 as shown in [Figure 7-9](#).

- DUTY\_CLAMP1 configures the duty command till which reference will be constant. REF\_CLAMP1 configures this constant reference between DUTY\_OFF1 and DUTY\_CLAMP1. DUTY\_CLAMP1 can be placed anywhere between DUTY\_OFF1 and DUTY\_A.
- DUTY\_A configures the duty command for reference REF\_A. There is a step change in reference from REF\_CLAMP1 to REF\_A at DUTY\_CLAMP1. DUTY\_A to DUTY\_E has to be in the same order as shown in [Figure 7-9](#).
- DUTY\_B configures the duty command for reference REF\_B. There is a step change in reference from REF\_A to REF\_B at DUTY\_A.
- DUTY\_C configures the duty command for reference REF\_C. There is a step change in reference from REF\_B to REF\_C at DUTY\_B.
- DUTY\_D configures the duty command for reference REF\_D. There is a step change in reference from REF\_C to REF\_D at DUTY\_C.
- DUTY\_E configures the duty command for reference REF\_E. There is a step change in reference from REF\_D to REF\_E at DUTY\_D.
- DUTY\_CLAMP2 configures the duty command above which the reference will be constant at REF\_CLAMP2. REF\_CLAMP2 configures this constant reference between DUTY\_CLAMP2 and DUTY\_OFF2. There is a step change in reference from REF\_E to REF\_CLAMP2 at DUTY\_E. DUTY\_CLAMP2 can be placed anywhere between DUTY\_E and DUTY\_OFF2.
- DUTY\_OFF2 and DUTY\_ON2 configures a hysteresis around reference control input REF\_CLAMP2 and REF\_OFF2 as shown in [Figure 7-9](#).
- DUTY\_OFF2 configures the duty command above which the reference will change from REF\_CLAMP2 to REF\_OFF2.
- DUTY\_HYS configures the hysteresis during every step change at DUTY\_CLAMP1, DUTY\_A to DUTY\_E.

### 7.3.6.5.3 Forward-Reverse Profiles

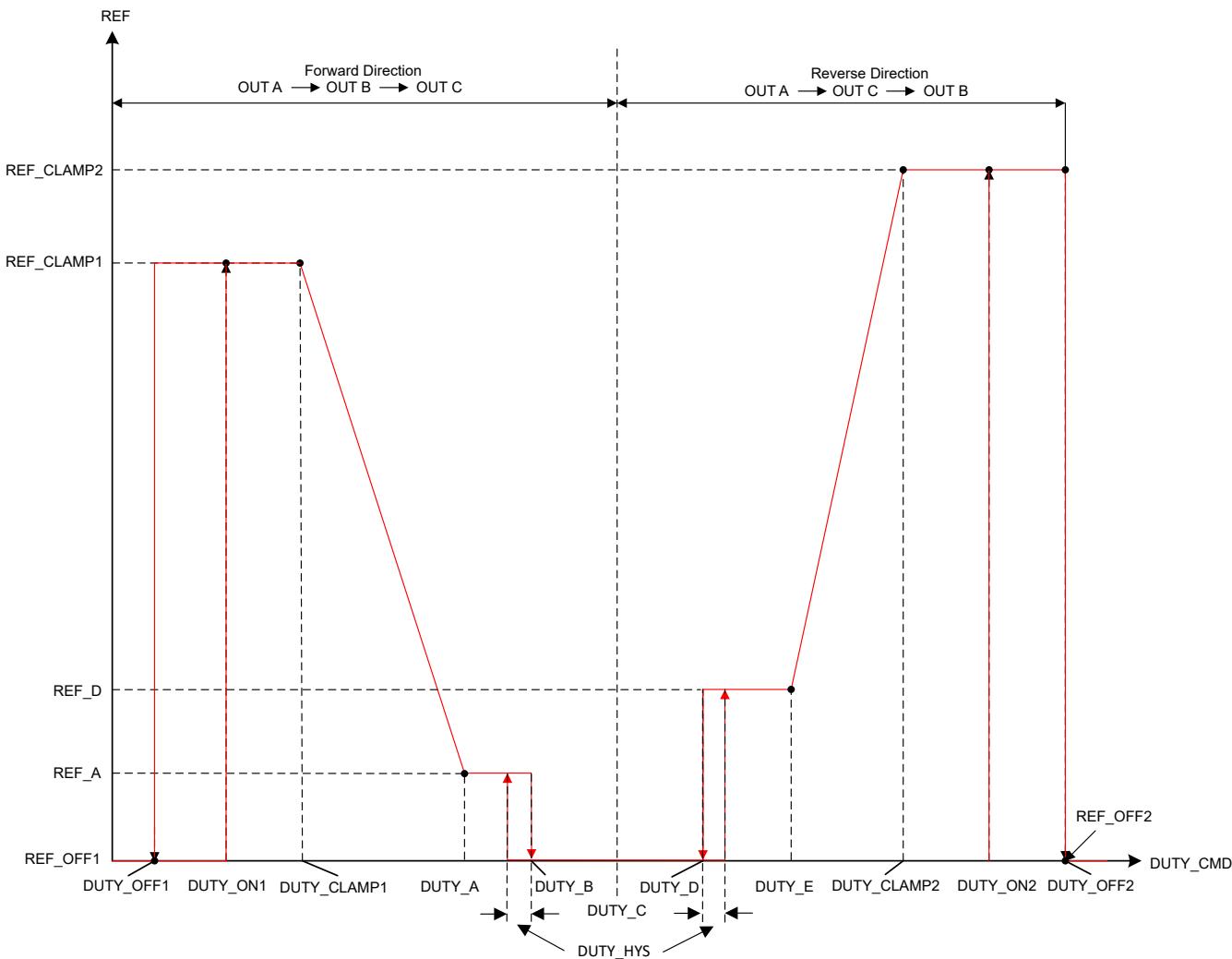


Figure 7-10. Forward Reverse Control Profiles

Forward-Reverse control profiles can be configured by setting REF\_PROFILE\_CONFIG to 11b. Forward-Reverse profiles feature direction change through adjusting the duty command. DUTY\_C configures duty command at which the direction will be changed. The Forward-Reverse speed profile can be used to eliminate the separate signal used to control the motor direction.

#### Note

The direction change functionality through DIR\_INPUT bits is disabled in forward reverse profile mode.

- DUTY\_OFF1 configures the duty command below which the reference will be REF\_OFF1.
- DUTY\_OFF1 and DUTY\_ON1 configures a hysteresis around reference control input REF\_CLAMP1 and REF\_OFF1 as shown in [Figure 7-10](#).
- DUTY\_CLAMP1 configures the duty command till which reference will be constant. REF\_CLAMP1 configures this constant reference between DUTY\_OFF1 and DUTY\_CLAMP1. DUTY\_CLAMP1 can be placed anywhere between DUTY\_OFF1 and DUTY\_A.
- DUTY\_A configures the duty command for reference REF\_A. The reference changes linearly between DUTY\_CLAMP1 and DUTY\_A. DUTY\_A to DUTY\_E has to be in the same order as shown in [Figure 7-10](#).

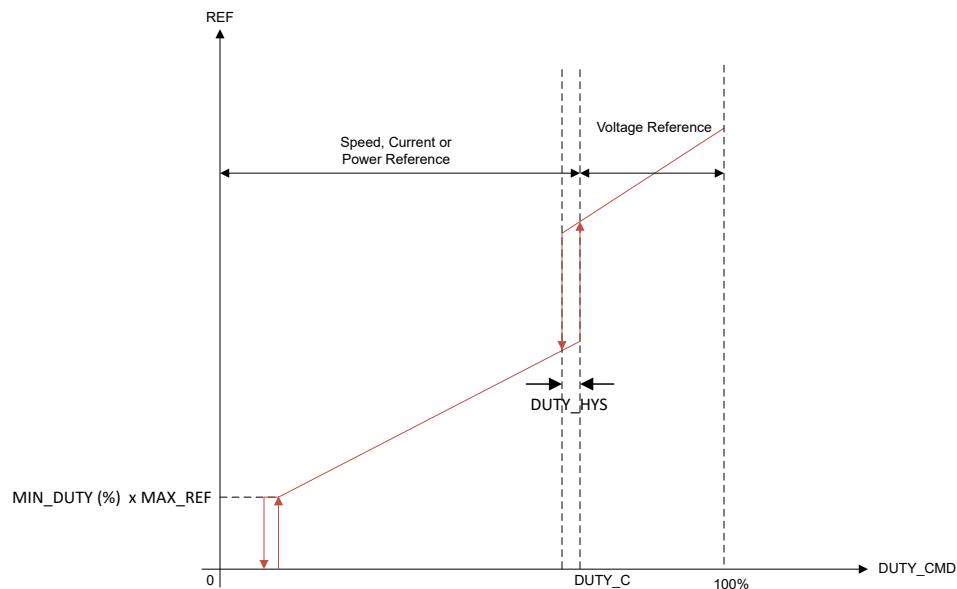
- DUTY\_B configures the duty command above which MCF8329HS-Q1 will be in off state. The reference remains constant at REF\_A between DUTY\_A and DUTY\_B.
- DUTY\_C configures the duty command at which the direction is changed
- DUTY\_D configures the duty command above which the MCF8329HS-Q1 will be in running state in the reverse direction. REF\_D configures constant reference between DUTY\_D and DUTY\_E.
- DUTY\_E configures the duty command above which reference changes linearly between DUTY\_E and DUTY\_CLAMP2.
- DUTY\_CLAMP2 configures the duty command above which the reference will be constant at REF\_CLAMP2. REF\_CLAMP2 configures this constant reference between DUTY\_CLAMP2 and DUTY\_OFF2. DUTY\_CLAMP2 can be placed anywhere between DUTY\_E and DUTY\_OFF2.
- DUTY\_OFF2 and DUTY\_ON2 configures a hysteresis around reference control input REF\_CLAMP2 and REF\_OFF2 as shown in [Figure 7-10](#).
- DUTY\_OFF2 configures the duty command above which the reference changes in the reverse direction from REF\_CLAMP2 to REF\_OFF2.
- DUTY\_HYS configures the hysteresis during step change at DUTY\_B and DUTY\_D.

#### 7.3.6.5.4 Multi-Reference Mode Operation

**Note**

The multi-reference (mixed) mode operation is available only when REF\_PROFILE\_CONFIG is set 01b (linear profile) or 10b (staircase profile).

MCF8329HS-Q1 provides the option of multi-reference mode operation when MIXED\_MODE\_CONFIG is set to 01b or 10b. When MIXED\_MODE\_CONFIG is set to 01b, MCF8329HS-Q1 operates in speed, current or power reference mode till DUTY\_CMD reaches DUTY\_C and then switches to voltage reference mode from DUTY\_C till 100% duty command as shown in [Figure 7-11](#).



**Figure 7-11. Multi-Reference Mode Operation (when MIXED\_MODE\_CONFIG = 01b)**

Conversely, MCF8329HS-Q1 operates in voltage reference mode till DUTY\_C and then switches to speed, current or power reference from DUTY\_C till 100% duty command when MIXED\_MODE\_CONFIG is set to 10b as shown in [Figure 7-12](#).

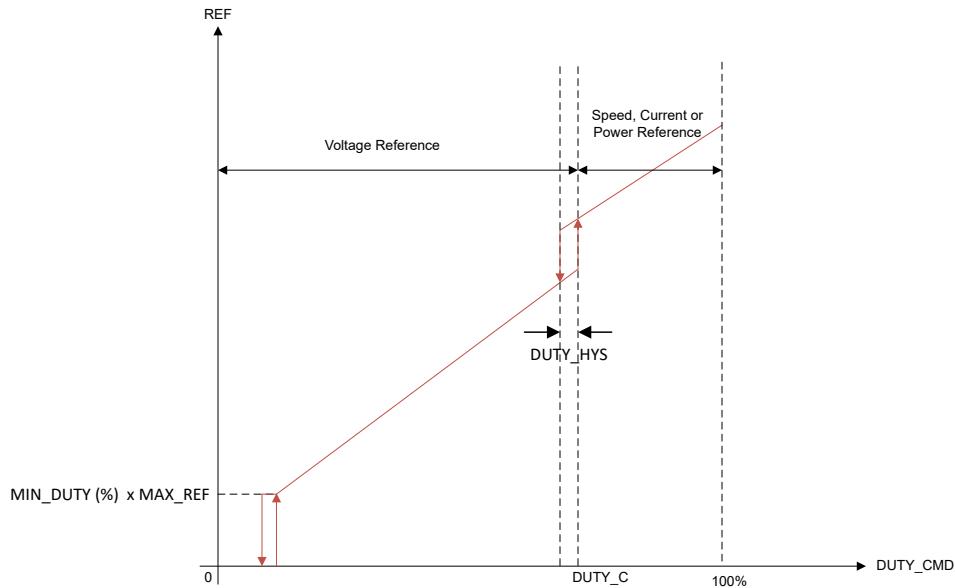


Figure 7-12. Multi-Reference Mode Operation (when MIXED\_MODE\_CONFIG = 10b)

#### 7.3.6.5.5 Input Reference Transfer Function without Profiler

The input reference can be a speed, power, current or voltage command as configured by CTRL\_MODE.

##### Note

- In this mode, if  $\text{MIN\_DUTY} < \text{REF\_CLAMP1}$ , the minimum reference is set by  $\text{REF\_CLAMP1}$  and not  $\text{MIN\_DUTY}$ . For example, if  $\text{MIN\_DUTY}$  is set to 1% and  $\text{REF\_CLAMP1}$  set to 5%, the minimum reference is  $\text{REF\_CLAMP1} \times \text{MAX\_REFERENCE}$ .  $\text{MAX\_REFERENCE}$  can be  $\text{MAX\_SPEED}$ ,  $\text{MAX\_POWER}$ ,  $\text{ILIMIT}$  or 100% depending on input reference mode.
- Set  $\text{MIN\_DUTY} > \text{REF\_CLAMP1}$  for using  $\text{MIN\_DUTY}$  to set the minimum reference.

#### Speed Reference Transfer Function

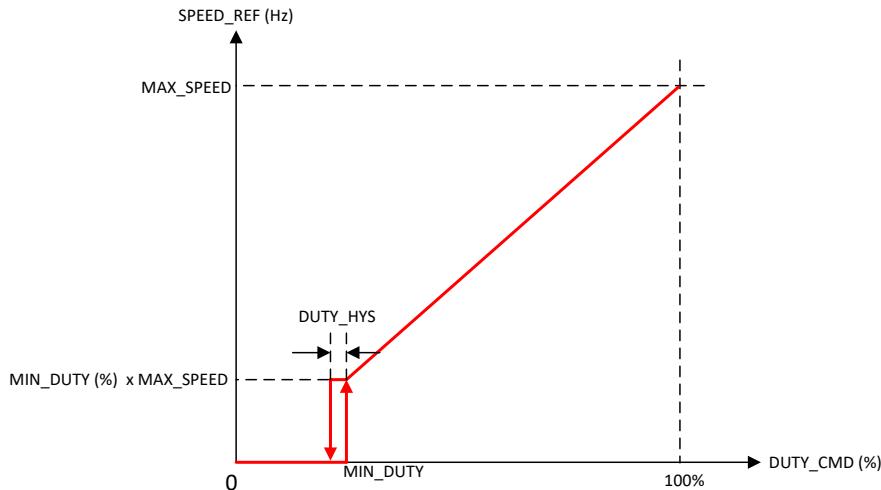
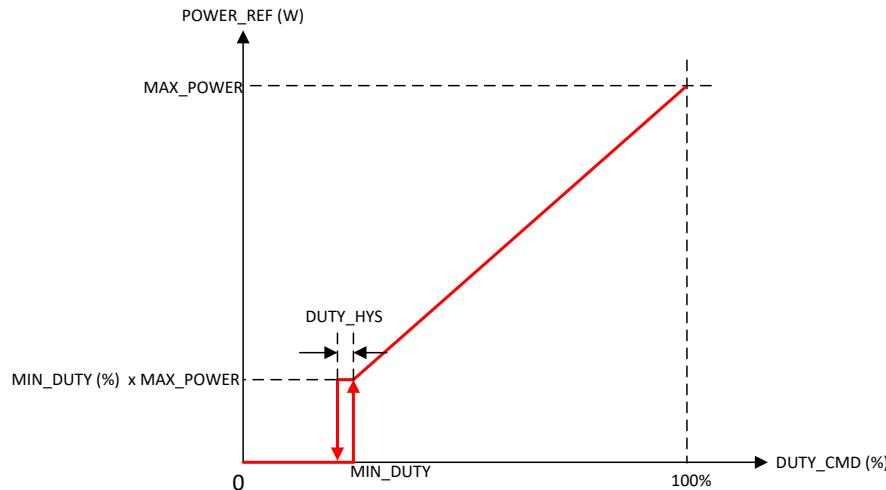


Figure 7-13. Speed Reference Transfer Function

Figure 7-13 shows the relationship between DUTY\_CMD and SPEED\_REF. MAX\_SPEED sets the SPEED\_REF at DUTY\_CMD of 100%. MIN\_DUTY sets the minimum SPEED\_REF ( $\text{MIN\_DUTY} \times$

MAX\_SPEED). If MAX\_SPEED is set to 0-Hz, SPEED\_REF is clamped to zero (irrespective of DUTY\_CMD) and motor is in stopped state.

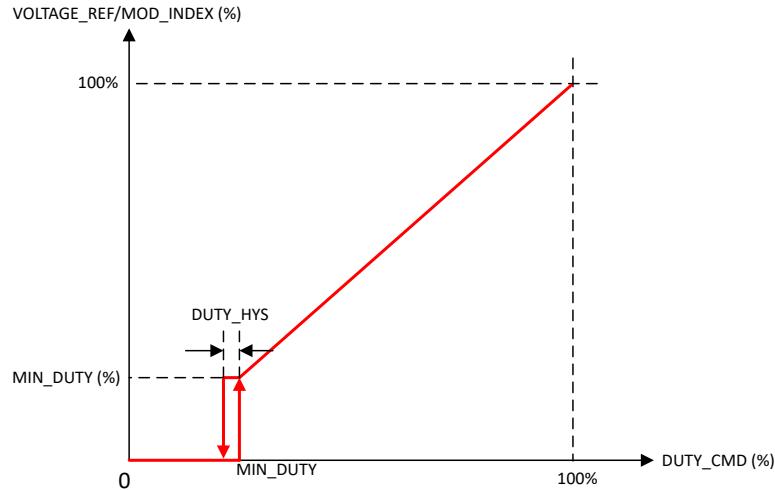
### Power Reference Transfer Function



**Figure 7-14. Power Reference Transfer Function**

Figure 7-14 shows the relationship between DUTY\_CMD and POWER\_REF. MAX\_POWER sets the POWER\_REF at DUTY\_CMD of 100%. MIN\_DUTY sets the minimum POWER\_REF (MIN\_DUTY x MAX\_POWER). If MAX\_POWER is set to 0-W, POWER\_REF is clamped to zero (irrespective of DUTY\_CMD) and motor is in stopped state.

### Voltage Reference Transfer Function



**Figure 7-15. Voltage Reference Transfer Function**

In voltage reference mode, the phase voltage applied to motor is proportional to the DUTY\_CMD (from MIN\_DUTY to 100%) as shown in Figure 7-15. For DUTY\_CMD less than MIN\_DUTY, the applied voltage to motor is clamped to zero.

### Current Input Transfer Function

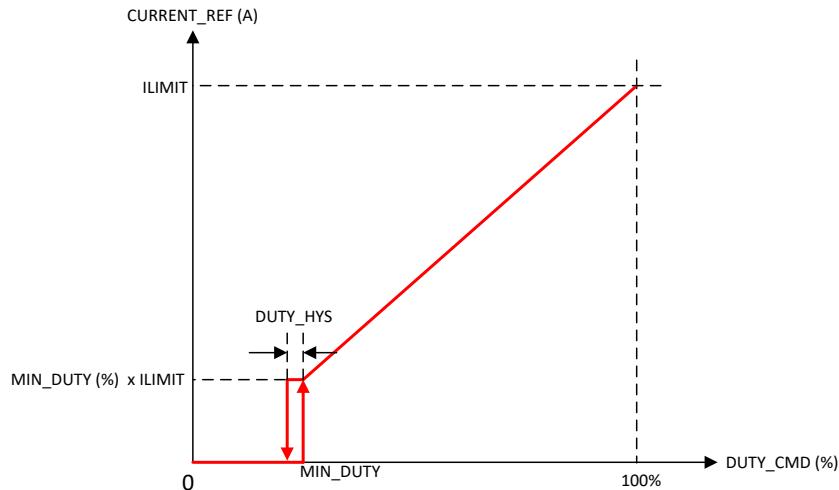


Figure 7-16. Current Reference Transfer Function

Figure 7-16 shows the relationship between DUTY\_CMD and CURRENT\_REF. ILIMIT sets the CURRENT\_REF at DUTY\_CMD of 100%. MIN\_DUTY sets the minimum CURRENT\_REF (MIN\_DUTY x ILIMIT).

### 7.3.7 Bootstrap Capacitor Initial Charging

MCF8329HS-Q1 provides a way to precharge the bootstrap capacitor during start-up. The algorithm uses a sequence to charge each phase bootstrap capacitor by turning on the external low side MOSFETs using PWM turn on pulses on GLx pins as shown in Figure 7-17. In the charging sequence, the low side MOSFET is switched at a frequency set by PWM FREQUENCY with an on time of  $t_{LS\_ON\_BC}$  (5% on time duty cycle). Each phase is charged for a period equal to one third of BST\_CHRG\_TIME.

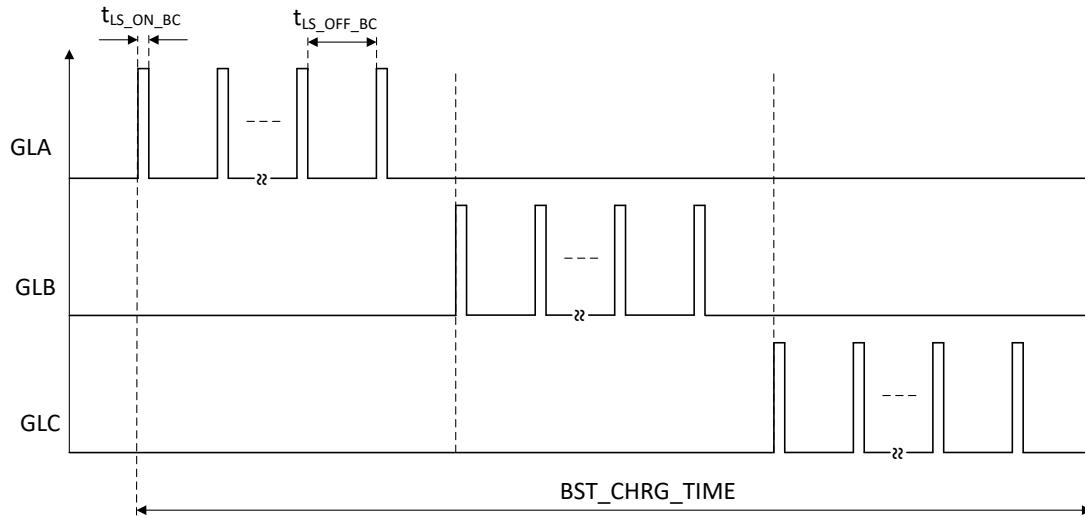
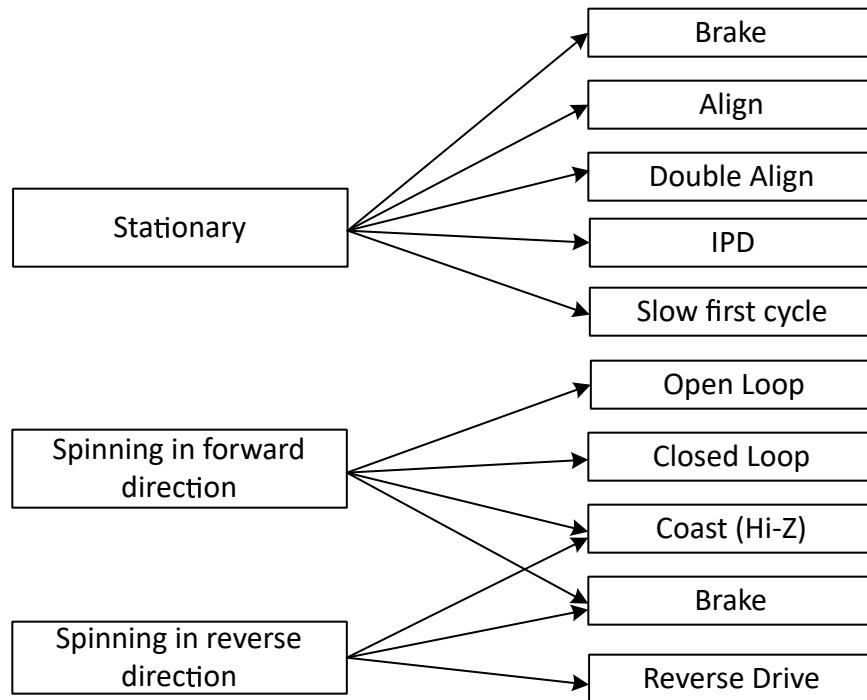


Figure 7-17. Bootstrap Capacitor Precharging at Start-up

### 7.3.8 Starting the Motor Under Different Initial Conditions

The motor can be in one of three states when MCF8329HS-Q1 begins the start-up process. The motor may be stationary, spinning in the forward direction, or spinning in the reverse direction. The MCF8329HS-Q1 includes a number of features to allow for reliable motor start-up under all of these conditions. Figure 7-18 shows the motor start-up flow for each of the three initial motor states.



**Figure 7-18. Starting the motor under different initial conditions**

**Note**

"Forward" means "spinning in the same direction as the commanded direction", and "Reverse" means "spinning in the opposite direction as the commanded direction".

#### 7.3.8.1 Case 1 – Motor is Stationary

If the motor is stationary, the commutation must be initialized to be in phase with the position of the motor. The MCF8329HS-Q1 provides various options to initialize the commutation logic to the motor position and reliably start the motor.

- The align and double align techniques force the motor into alignment by applying a voltage across a particular motor phase to force the motor to rotate in alignment with this phase.
- Initial position detect (IPD) determines the position of the motor based on the deterministic inductance variation, which is often present in BLDC motors.
- The slow first cycle method starts the motor by applying a low frequency cycle to align the rotor position to the applied commutation by the end of one electrical rotation.

MCF8329HS-Q1 also provides a configurable brake option to ensure the motor is stationary before initiating one of the above start-up methods. Device enters open loop acceleration after going through the configured start-up method.

#### 7.3.8.2 Case 2 – Motor is Spinning in the Forward Direction

If the motor is spinning forward (same direction as the commanded direction) with sufficient speed (BEMF), the MCF8329HS-Q1 resynchronizes with the spinning motor and continues commutation by going directly to closed loop operation. If the motor speed is too low for closed loop operation, MCF8329HS-Q1 enters open loop operation to accelerate the motor till it reaches sufficient speed to enter closed loop operation. By resynchronizing to the spinning motor, the user achieves the fastest possible start-up time for this initial condition. This resynchronization feature can be enabled or disabled through RESYNC\_EN. If resynchronization is disabled, the MCF8329HS-Q1 can be configured to wait for the motor to coast to a stop and/or apply a brake. After the motor has stopped spinning, the motor start-up sequence proceeds as in Case 1, considering the motor is stationary.

### 7.3.8.3 Case 3 – Motor is Spinning in the Reverse Direction

If the motor is spinning in the reverse direction (the opposite direction as the commanded direction), the MCF8329HS-Q1 provides several methods to change the direction and drive the motor to the target reference in the commanded direction.

The reverse drive method allows the motor to be driven so that it decelerates through zero speed. The motor achieves the shortest possible spin-up time when spinning in the reverse direction.

If reverse drive is not enabled, then the MCF8329HS-Q1 can be configured to wait for the motor to coast to a stop and/or apply a brake. After the motor has stopped spinning, the motor start-up sequence proceeds as in Case 1, considering the motor is stationary.

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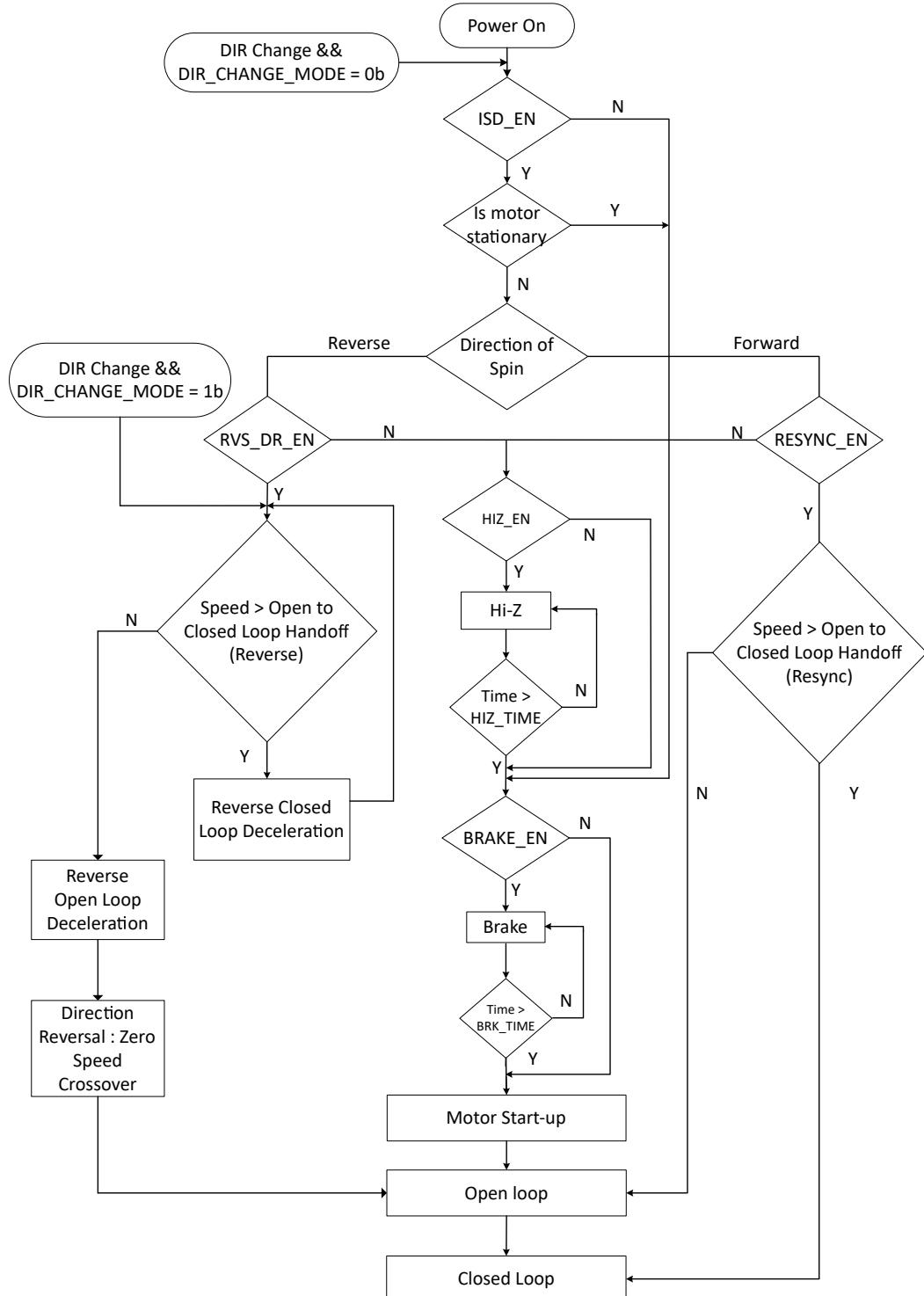
#### Note

Take care when using the reverse drive or brake feature to ensure that the current is limited to an acceptable level and that the supply voltage does not surge as a result of energy being returned to the power supply.

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### 7.3.9 Motor Start Sequence (MSS)

Figure 7-19 shows the motor-start sequence implemented in the MCF8329HS-Q1 device.



**Figure 7-19. Motor Starting-up Flow**

<b>Power-On State</b>	This is the initial state of the Motor Start Sequence (MSS). The MSS starts in this state on initial power-up or whenever the MCF8329HS-Q1 comes out of standby or sleep mode.
<b>DIR Change &amp;&amp; DIR_CHANGE_MODE = 0b Judgement</b>	In MCF8329HS-Q1, if direction change command is detected and DIR_CHANGE_MODE is set to 0b during any state (including closed loop), the device re-starts the MSS.
<b>ISD_EN Judgement</b>	After power-on, the MCF8329HS-Q1 MSS enters the ISD_EN judgement where it checks to see if the initial speed detect (ISD) function is enabled (ISD_EN = 1b). If ISD is disabled, the MSS proceeds directly to the BRAKE_EN judgement. If ISD is enabled, MSS advances to the ISD (Is Motor Stationary) state.
<b>ISD State</b>	The MSS determines the initial condition (speed, direction of spin) of the motor (see <a href="#">Initial Speed Detect (ISD)</a> ). If motor is deemed to be stationary (motor BEMF < STAT_DETECT_THR), the MSS proceeds to BRAKE_EN judgement. If the motor is not stationary, MSS proceeds to verify the direction of spin.
<b>Direction of Spin Judgement</b>	The MSS determines whether the motor is spinning in the forward or the reverse direction. If the motor is spinning in the forward direction, the MCF8329HS-Q1 proceeds to the RESYNC_EN judgement. If the motor is spinning in the reverse direction, the MSS proceeds to the RVS_DR_EN judgement.
<b>RESYNC_EN Judgement</b>	If RESYNC_EN is set to 1b, MCF8329HS-Q1 proceeds to Speed > Open to Closed Loop Handoff (Re-sync) judgement. If RESYNC_EN is set to 0b, MSS proceeds to HIZ_EN judgement.  If motor speed > FW_DRV_RESYN_THR, MCF8329HS-Q1 uses the speed and position information from the ISD state to transition to the closed loop state (see <a href="#">Motor Resynchronization</a> ) directly. If motor speed < FW_DRV_RESYN_THR, MCF8329HS-Q1 transitions to open loop state.
<b>RVS_DR_EN Judgement</b>	The MSS checks to see if the reverse drive function is enabled (RVS_DR_EN = 1). If it is enabled, the MSS transitions to check speed of the motor in reverse direction. If the reverse drive function is not enabled, the MSS advances to the HIZ_EN judgement.
<b>Speed &gt; Open to Closed Loop Handoff (Reverse) Judgement</b>	The MSS checks to see if the reverse speed is high enough for MCF8329HS-Q1 to decelerate in closed loop. Till the speed (in reverse direction) is high enough, MSS stays in reverse closed loop deceleration. If speed is too low, then the MSS transitions to reverse open loop deceleration.
<b>Reverse Closed Loop, Open Loop Deceleration and Zero Speed Crossover</b>	The MCF8329HS-Q1 resynchronizes in the reverse direction, decelerates the motor in closed loop till motor speed falls below the handoff threshold. (see <a href="#">Reverse Drive</a> ). When motor speed in reverse direction is too low, the MCF8329HS-Q1 switches to open-loop, decelerates the motor in open-loop, crosses zero speed, and accelerates in the forward direction in open-loop before entering closed loop operation after motor speed is sufficiently high.
<b>HIZ_EN Judgement</b>	The MSS checks to determine whether the coast (Hi-Z) function is enabled (HIZ_EN =1). If the coast function is enabled, the MSS advances to the coast routine. If the coast function is disabled, the MSS advances to the BRAKE_EN judgement.
<b>Coast (Hi-Z) Routine</b>	The device coasts the motor by turning OFF all six MOSFETs for a certain time configured by HIZ_TIME.
<b>BRAKE_EN Judgement</b>	The MSS checks to determine whether the brake function is enabled (BRAKE_EN =1). If the brake function is enabled, the MSS advances to the brake routine. If the brake function is disabled, the MSS advances to the motor start-up state (see <a href="#">Section 7.3.9.4</a> ).

<b>Brake Routine</b>	MCF8329HS-Q1 implements a brake by turning on all three low-side MOSFETS for BRK_TIME.
<b>Closed Loop State</b>	In this state, the MCF8329HS-Q1 drives the motor with FOC.

**Note**

User should ensure adequate start up time to fully charge the bootstrap capacitors. One option to charge the boot capacitor is by providing enough time with low side brake at start up. Another option is to use the bootstrap precharging routine. The device will initiate ISD only after bootstrap voltage crosses the UVLO threshold.

#### 7.3.9.1 Initial Speed Detect (ISD)

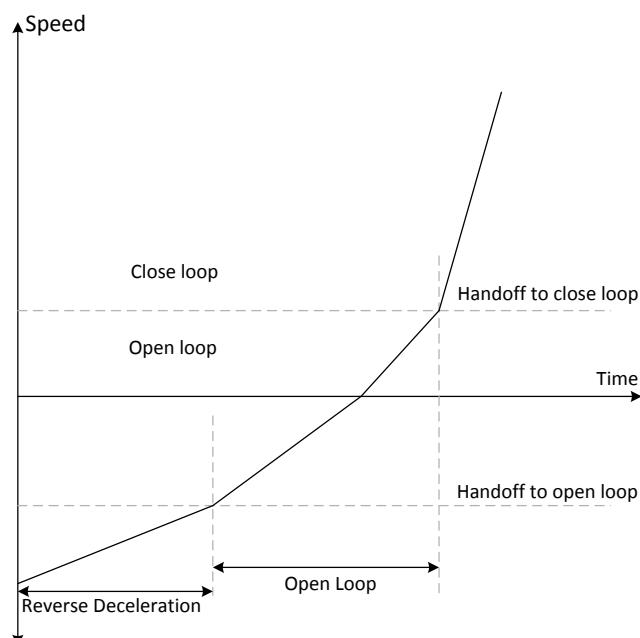
The ISD function is used to identify the initial condition of the motor and is enabled by setting ISD\_EN to 1b. The initial speed, position and direction is determined by sampling the phase voltage through the internal ADC. ISD can be disabled by setting ISD\_EN to 0b. If the function is disabled (ISD\_EN set to 0b), the MCF8329HS-Q1 does not perform the initial speed detect function and proceeds to check if the brake routine (BRAKE\_EN) is enabled.

#### 7.3.9.2 Motor Resynchronization

The motor resynchronization function works when the ISD and resynchronization functions are both enabled and the device determines that the initial state of the motor is spinning in the forward direction (same direction as the commanded direction). The speed and position information measured during ISD are used to initialize the drive state of the MCF8329HS-Q1, which can transition directly into closed loop (or open loop if motor speed is not sufficient for closed loop operation) state without needing to stop the motor. In the MCF8329HS-Q1, motor resynchronization can be enabled/disabled through RESYNC\_EN bit. If motor resynchronization is disabled, the device proceeds to check if the motor coast (Hi-Z) routine is enabled.

#### 7.3.9.3 Reverse Drive

The MCF8329HS-Q1 uses the reverse drive function to change the direction of the motor rotation when ISD\_EN and RVS\_DR\_EN are both set to 1b and the ISD determines the motor spin direction to be opposite to that of the commanded direction. Reverse drive includes synchronizing with the motor speed in the reverse direction, reverse decelerating the motor through zero speed, changing direction, and accelerating in open loop in forward (or commanded) direction until the device transitions into closed loop in forward direction (see [Figure 7-20](#)).



**Figure 7-20. Reverse Drive Function**

#### 7.3.9.3.1 Reverse Drive Tuning

The speed at which motor would enter the open loop in reverse direction can be configured using REV\_DRV\_HANDOFF\_THR. For a smooth transition without jerks or loss of synchronism, user can configure an appropriate current limit when the motor is spinning in open loop during speed reversal using REV\_DRV\_OPEN\_LOOP\_CURRENT. The open loop acceleration rate for the forward direction during speed reversal is defined using REV\_DRV\_OPEN\_LOOP\_ACCEL\_A1. The reverse drive open loop deceleration rate, when the motor is decelerating in the opposite direction to zero speed, can be configured as a percentage of reverse drive open loop acceleration using REV\_DRV\_OPEN\_LOOP\_DEC.

#### 7.3.9.4 Motor Start-up

There are different options available for motor start-up from a stationary position and these options can be configured by MTR\_STARTUP. In align and double align mode, the motor is aligned to a known position by injecting a DC current. In IPD mode, the rotor position is estimated by applying 6 different high-frequency pulses. In slow first cycle mode, the motor is started by applying a low frequency cycle.

##### 7.3.9.4.1 Align

Align is enabled by configuring MTR\_STARTUP to 00b. The MCF8329HS-Q1 aligns the motor by injecting a DC current through a particular phase pattern for a certain time configured by ALIGN\_TIME. In the MCF8329HS-Q1, the current limit during align is configured through ALIGN\_OR\_SLOW\_CURRENT\_ILIMIT.

A fast change in the phase current can result in a sudden change in the driving torque and this can result in acoustic noise. To avoid this, the MCF8329HS-Q1 ramps up the current from 0 to the current limit at a configurable ramp rate set by ALIGN\_SLOW\_RAMP\_RATE. At the end of align routine the motor, is aligned at the known position.

##### 7.3.9.4.2 Double Align

Double align is enabled by configuring MTR\_STARTUP to 01b. Single align is not reliable when the initial position of the rotor is 180° out of phase with the applied phase pattern. In this case, it is possible to have start-up failures using single align. In order to improve the reliability of align based start-up, the MCF8329HS-Q1 provides the option of double align start-up. In double align start-up, MCF8329HS-Q1 uses a phase pattern for the second align that is 90° ahead of the first align phase pattern. In double align, relevant parameters like align time, current limit, ramp rate are the same as in the case of single align - two different phase patterns are applied in succession with the same parameters to ensure that the motor will be aligned to a known position irrespective of initial rotor position.

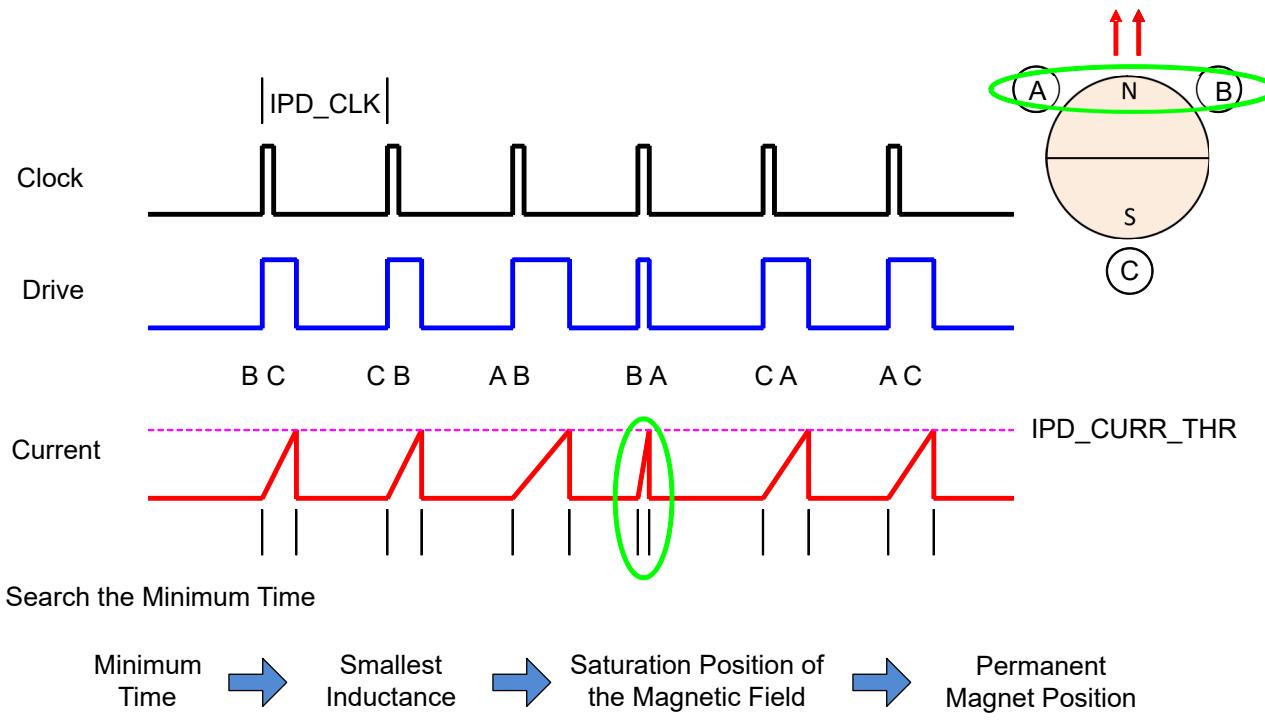
##### 7.3.9.4.3 Initial Position Detection (IPD)

Initial Position Detection (IPD) can be enabled by configuring MTR\_STARTUP to 10b. In IPD, inductive sense method is used to determine the initial position of the motor using the spatial variation in the motor inductance.

Align or double align may result in the motor spinning in the reverse direction before starting open loop acceleration. IPD can be used in such applications where reverse rotation of the motor is unacceptable. IPD does not wait for the motor to align with the commutation and therefore can allow for a faster motor start-up sequence. IPD works well when the inductance of the motor varies as a function of position. IPD works by pulsing current in to the motor and hence can generate acoustics which must be taken into account when determining the best start-up method for a particular application.

##### 7.3.9.4.3.1 IPD Operation

IPD operates by sequentially applying six different phase patterns according to the following sequence: BC-> CB-> AB-> BA-> CA-> AC (see [Figure 7-21](#)). When the current reaches the threshold configured by IPD\_CURR\_THR, the MCF8329HS-Q1 stops driving the particular phase pattern and measures the time taken to reach the current threshold from when the particular phase pattern was applied. Thus, the time taken to reach IPD\_CURR\_THR is measured for all six phase patterns - this time varies as a function of the inductance in the motor windings. The state with the shortest time represents the state with the minimum inductance. The minimum inductance is because of the alignment of the north pole of the motor with this particular driving state.

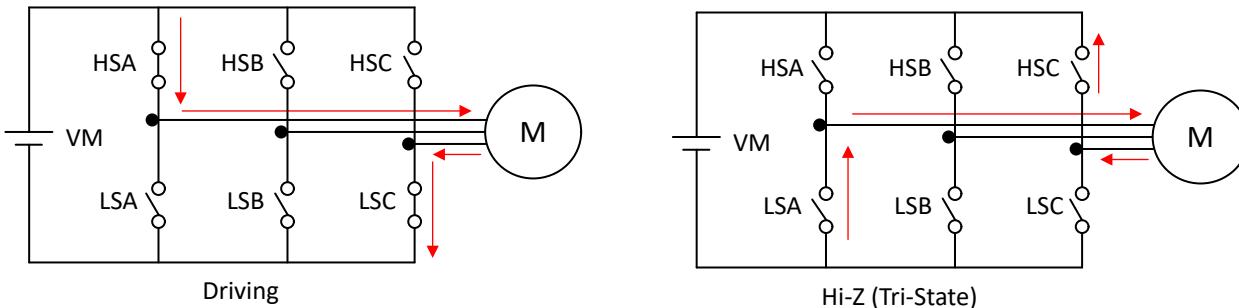


**Figure 7-21. IPD Function**

#### 7.3.9.4.3.2 IPD Release

IPD release uses Hi-Z mode, both the high-side (HSA) and low-side (LSC) MOSFETs are turned OFF and the current recirculates through the body diodes back to the power supply (see [Figure 7-22](#)).

The Hi-Z mode during IPD release can result in a voltage increase on motor DC supply voltage VM ( $V_{PVDD}$ ). The user must manage this with an appropriate selection of either a clamp circuit or by providing sufficient capacitance between  $V_{PVDD}$  and GND to absorb the energy.



**Figure 7-22. IPD Release Hi-Z mode**

#### 7.3.9.4.3.3 IPD Advance Angle

After the initial position is detected, the MCF8329HS-Q1 begins driving the motor in open loop at an angle specified by IPD\_ADV\_ANGLE.

Advancing the drive angle anywhere from 0° to 180° results in positive torque. Advancing the drive angle by 90° results in maximum initial torque. Applying maximum initial torque could result in uneven acceleration to the rotor. Select the IPD\_ADV\_ANGLE to allow for smooth acceleration in the application (see [Figure 7-23](#)).

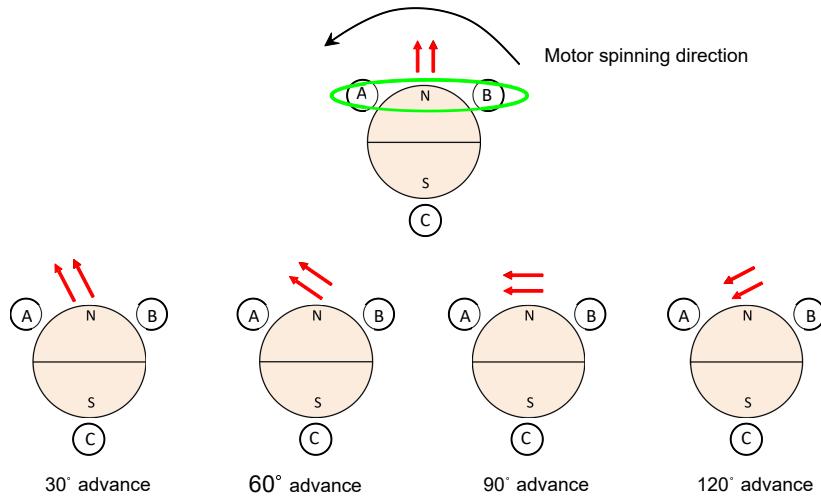


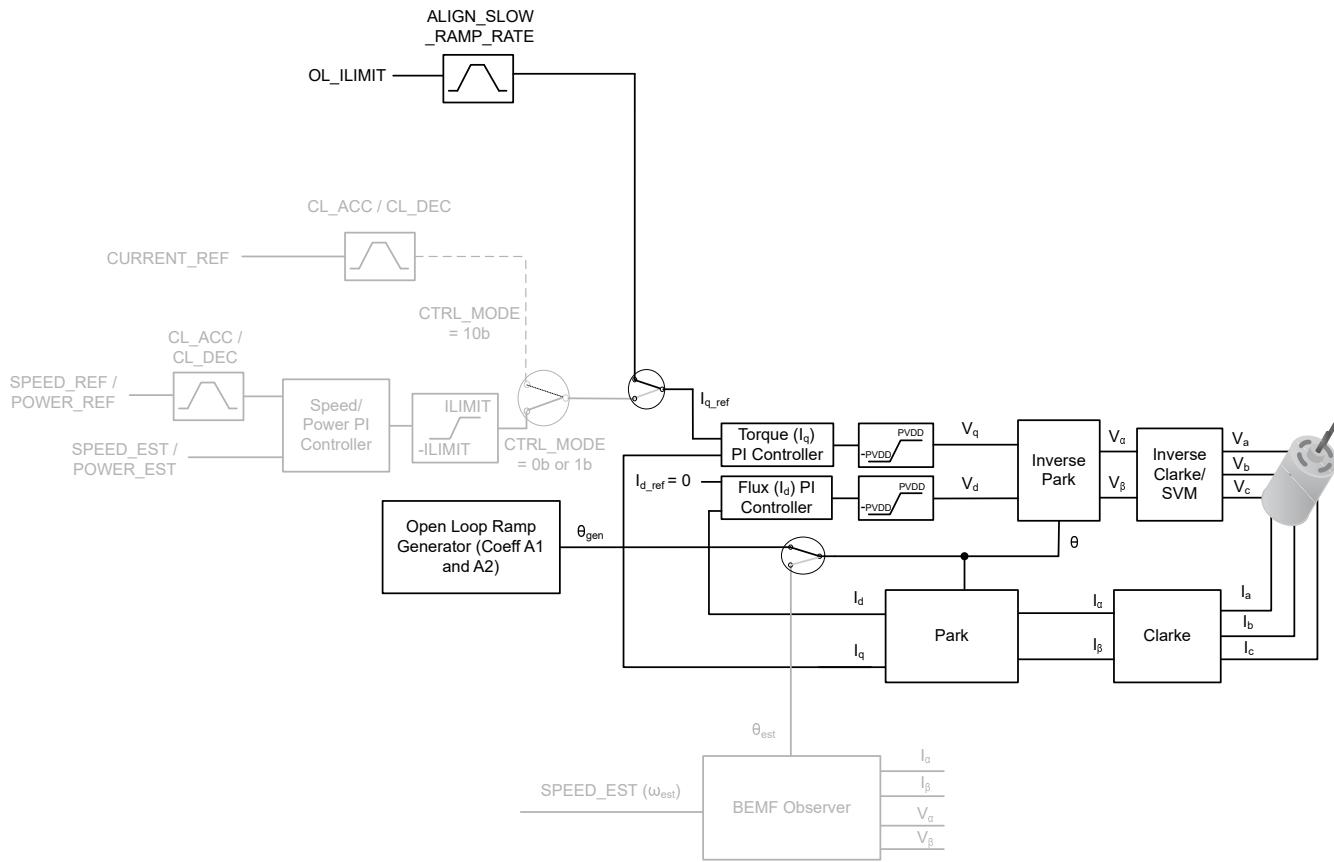
Figure 7-23. IPD Advance Angle

#### 7.3.9.4.4 Slow First Cycle Startup

Slow First Cycle start-up is enabled by configuring MTR\_STARTUP to 11b. In slow first cycle start-up, the MCF8329HS-Q1 starts motor commutation at a frequency defined by SLOW\_FIRST\_CYC\_FREQ. The frequency configured is used only for first cycle, and then the motor commutation follows acceleration profile configured by open loop acceleration coefficients A1 and A2. The slow first cycle frequency has to be configured to be slow enough to allow motor to synchronize with the commutation sequence. This mode is useful when fast startup is desired as it significantly reduces the align time.

#### 7.3.9.4.5 Open Loop

Upon completing the motor position initialization with either align, double align, IPD or slow first cycle, the MCF8329HS-Q1 begins to accelerate the motor in open loop. During open loop, the speed is increased with a fixed current limit. In open loop, the control PI loops for  $I_q$  and  $I_d$  actively control the currents. The angle during open loop is provided from the ramp generator as shown in Figure 7-24.



**Figure 7-24. Open Loop**

In MCF8329HS-Q1, the current limit threshold is configured through OL\_ILIMIT. The function of the open-loop operation is to drive the motor to a speed at which the motor generates sufficient BEMF to allow the back-EMF observer to accurately detect the position of the rotor. The motor is accelerated in open loop and speed at any given time is determined by [Equation 8](#). In MCF8329HS-Q1, open loop acceleration coefficients, A1 and A2 are configured through OL\_ACC\_A1 and OL\_ACC\_A2 respectively.

$$\text{Speed}(t) = A1 * t + 0.5 * A2 * t^2 \quad (8)$$

#### 7.3.9.4.6 Transition from Open to Closed Loop

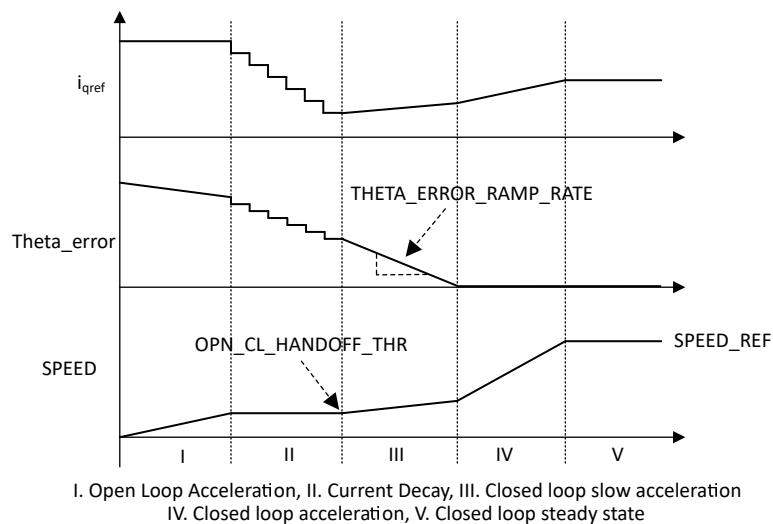
Once the motor has reached a sufficient speed for the back-EMF observer to estimate the angle and speed of the motor, the MCF8329HS-Q1 transitions into closed loop state. This handoff speed is automatically determined based on the measured back-EMF and motor speed. Users also have an option to manually set the handoff speed by configuring OPN\_CL\_HANDOFF\_THR and setting AUTO\_HANDOFF\_EN to 0b. In order to have smooth transition and avoid speed transients, the theta\_error ( $\Theta_{\text{gen}} - \Theta_{\text{est}}$ ) is decreased linearly after transition. The ramp rate of theta\_error reduction can be configured using THETA\_ERROR\_RAMP\_RATE. If the current limit set during the open loop is high and if it is not reduced before transition to closed loop, the motor speed may momentarily rise to higher values than SPEED\_REF after transition into closed loop. In order to avoid such speed variations, configure the IQ\_RAMP\_DOWN\_EN to 1b, so that  $i_{q\_ref}$  decreases prior to transition into closed loop. However if the final speed reference (SPEED\_REF) is more than two times the open loop to closed loop hand off speed (OPN\_CL\_HANDOFF\_THR), then  $i_{q\_ref}$  is not decreased independent of the IQ\_RAMP\_DOWN\_EN setting, to enable faster motor acceleration.

After hand off to closed loop at a sufficient speed, there could be still some theta error, as the estimators may not be fully aligned. A slow acceleration can be used after the open loop to closed loop transition, ensuring that the theta error reduces to zero. The slow acceleration can be configured using CL\_SLOW\_ACC.

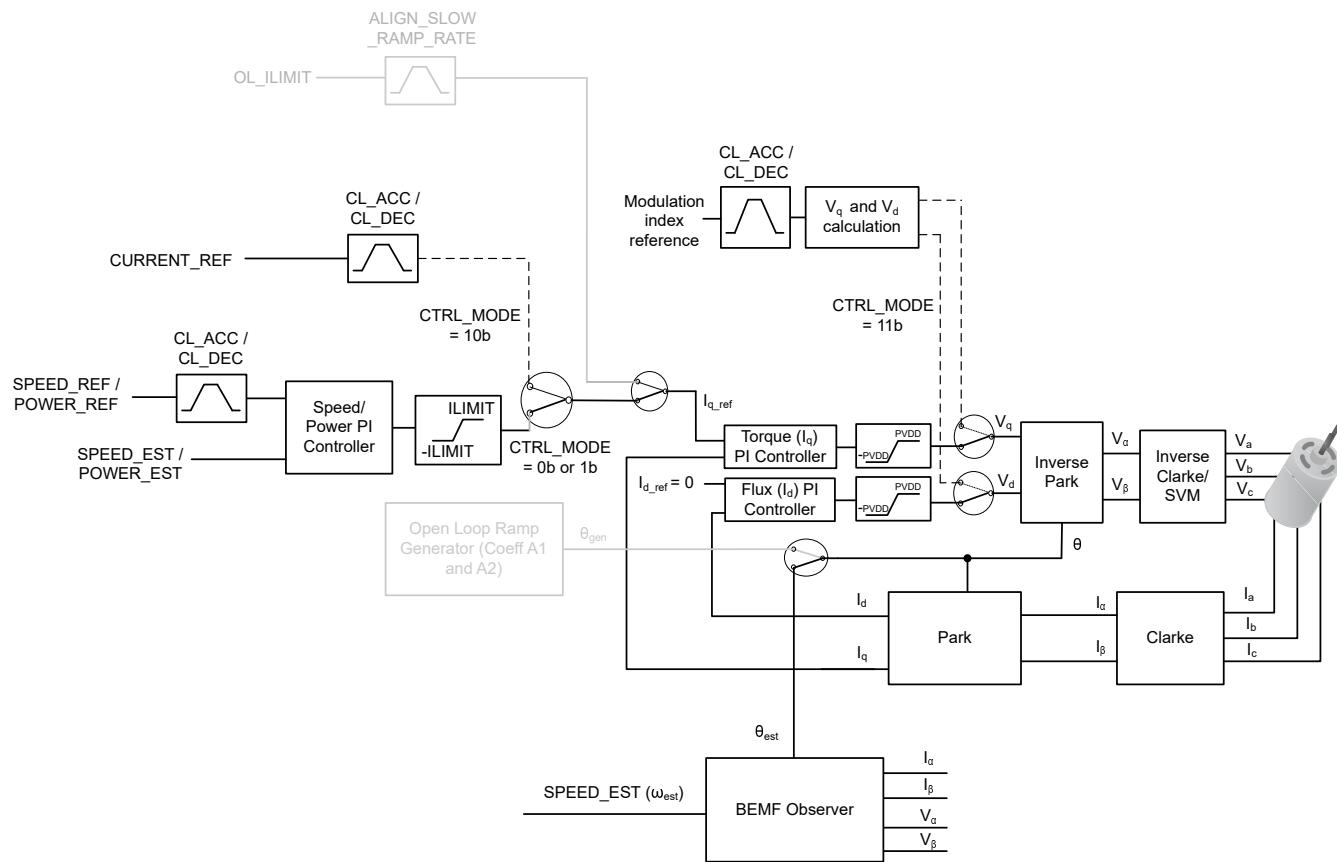
Figure 7-25 shows the control sequence in open to closed loop transition. The current  $i_{q\text{ref}}$  reduces to a lower value in current decay region, if IQ\_RAMP\_DOWN\_EN is set to 1b. If IQ\_RAMP\_DOWN\_EN is set to 0b, then the current decay region will not be present in the transition sequence.

**Note**

Iq ramp down is available (irrespective of IQ\_RAMP\_DOWN\_EN setting) only in speed control mode (CTRL\_MODE = 00b)



**Figure 7-25. Control Sequence in Open to Closed Loop Transition**



**Figure 7-26. Open to Closed Loop Transition**

### 7.3.10 Closed Loop Operation

The MCF8329HS-Q1 drives the motor using Field Oriented Control (FOC) as shown in [Figure 7-27](#). In closed loop operation, the motor angle ( $\Theta_{est}$ ) and speed ( $\omega_{est}$ ) are estimated using the back-EMF observer. The speed and current regulation are achieved using PI control loop. In order to achieve maximum efficiency, the direct axis current is set to zero ( $I_{d\_ref} = 0$ ), which will ensure that stator and rotor field are orthogonal ( $90^\circ$  out of phase) to each other. If flux weakening or MTPA is enabled  $I_{d\_ref}$  can be zero or a negative value during closed loop operation.

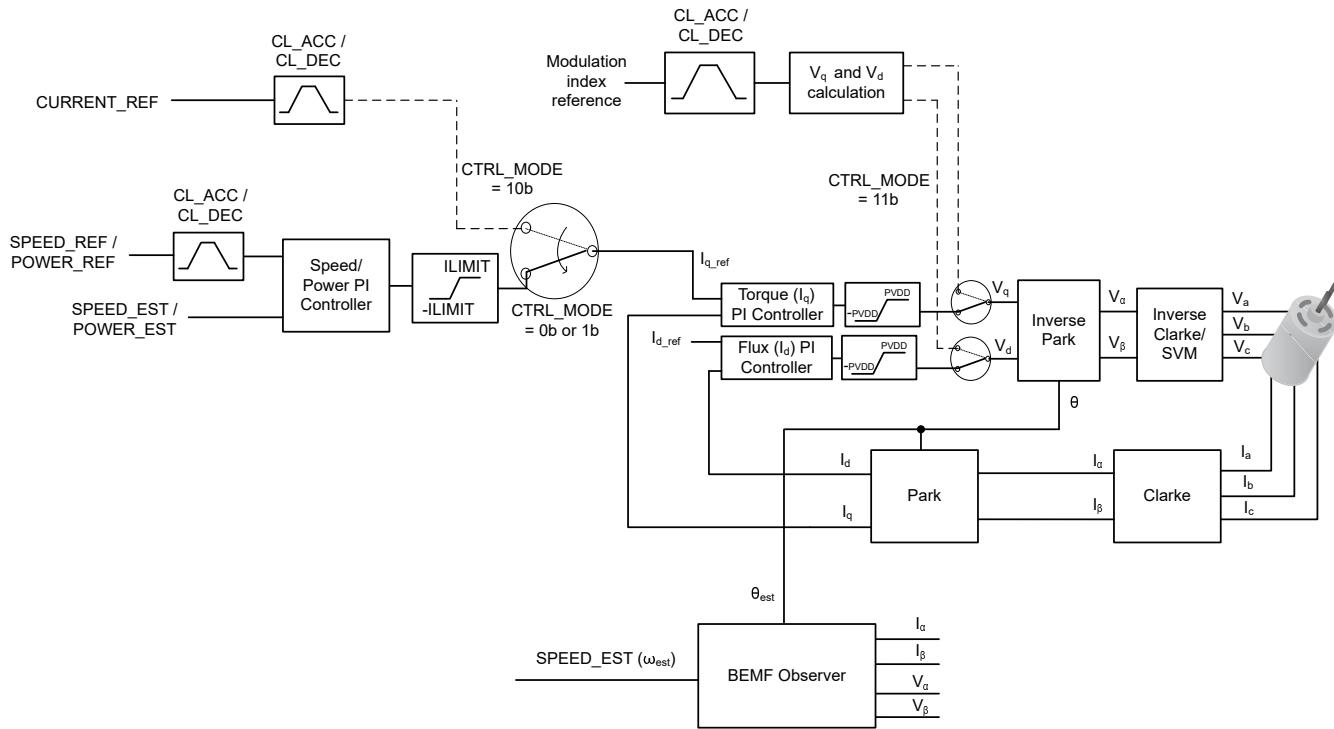
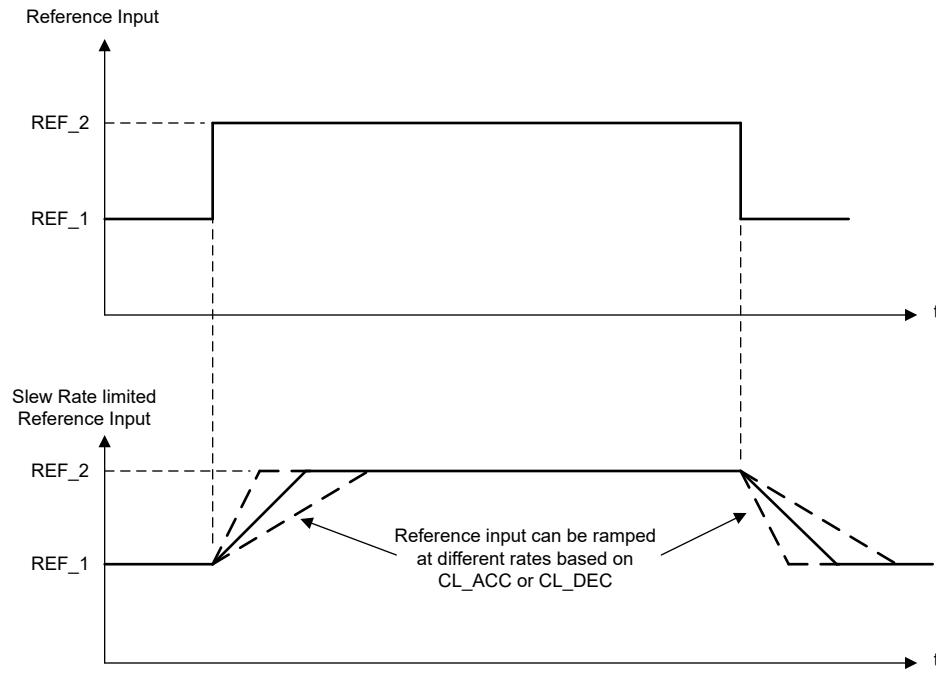


Figure 7-27. Closed Loop FOC Control

#### 7.3.10.1 Closed loop accelerate

During closed loop acceleration/deceleration, MCF8329HS-Q1 provides the option of configuring the slew rate of the reference input. This allows for a linear change in reference input (speed or power or current or modulation index) even when there is a step change in reference input (from Analog, PWM, Frequency or I<sup>2</sup>C) as seen in [Figure 7-28](#). This slew rate can be configured so as to prevent sudden changes in the torque applied to the motor which could result in acoustic noise. The closed loop acceleration/deceleration slew rate parameter, CL\_ACC/CL\_DEC, sets the slew rate of the reference during acceleration and deceleration (when AVS is not active) respectively.

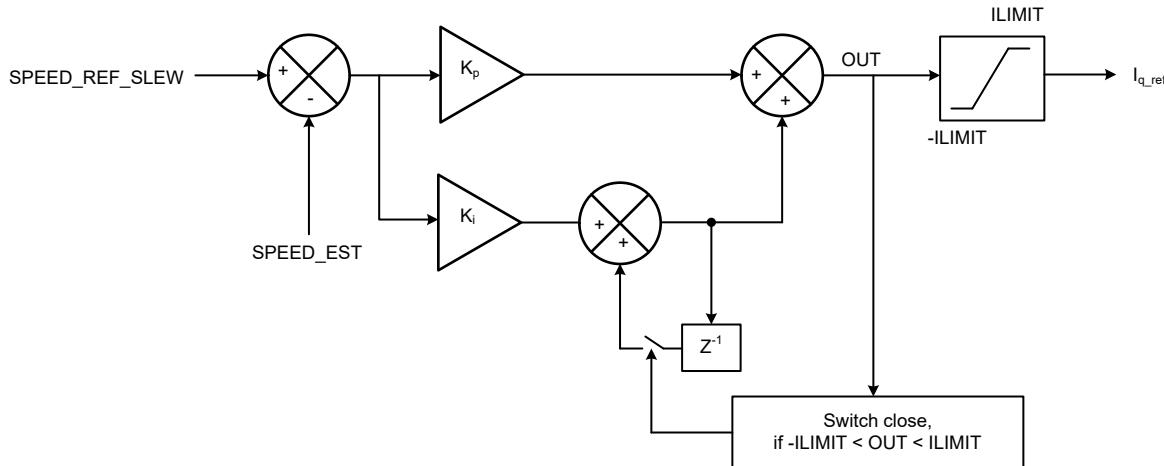


**Figure 7-28. Closed Loop Acceleration/Deceleration Slew Rate**

#### 7.3.10.2 Speed PI Control

The integrated speed control loop helps maintain a constant speed over varying operating conditions. The  $K_p$  and  $K_i$  coefficients are configured through SPD\_LOOP\_KP and SPD\_LOOP\_KI. The output of the speed loop is used to generate the current reference for torque control ( $I_{q\_ref}$ ). The output of the speed loop is limited to implement a current limit. The current limit is set by configuring ILIMIT. When output of the speed loop saturates, the integrator is disabled to prevent integral wind-up.

SPEED\_REF\_SLEW is derived from the duty command input, reference (speed) profiles and closed loop acceleration/deceleration rates configured by the user and SPEED\_EST is the estimated speed from the back-EMF observer.

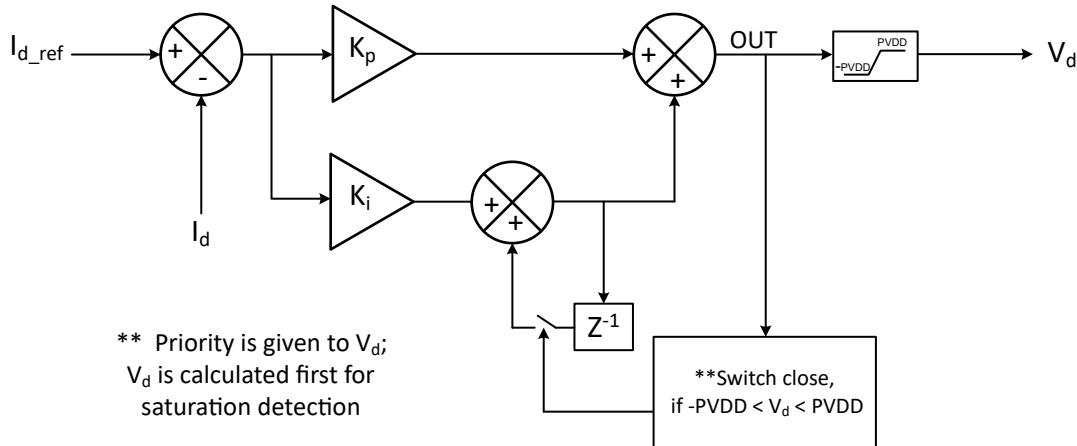


**Figure 7-29. Speed PI Control**

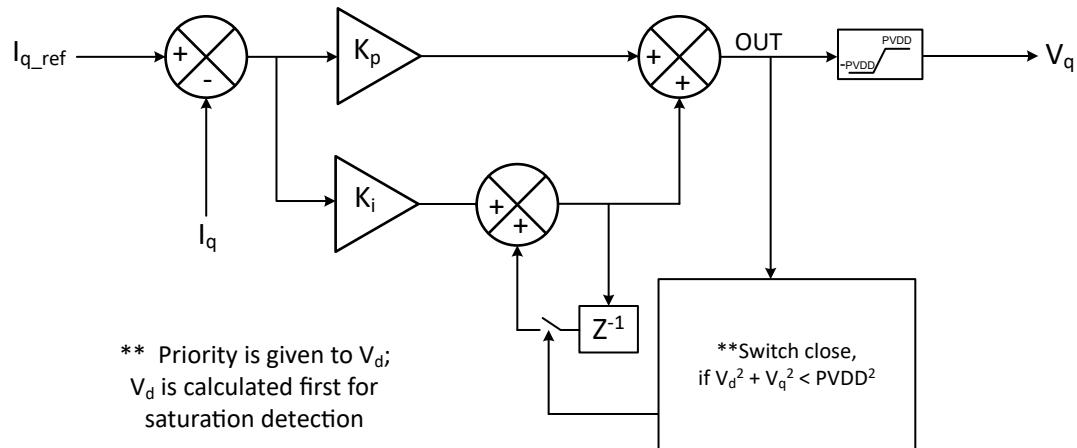
#### 7.3.10.3 Current PI Control

The MCF8329HS-Q1 has two PI controllers, one each for  $I_d$  and  $I_q$  to control flux and torque separately.  $K_p$  and  $K_i$  coefficients are the same for both PI controllers and are configured through CURR\_LOOP\_KP and

CURR\_LOOP\_KI. The outputs of the current control loops are used to generate voltage signals  $V_d$  and  $V_q$  to be applied to the motor. The outputs of the current loops are clamped to supply voltage, PVDD.  $I_d$  current PI loop is executed first and output of  $I_d$  current PI loop  $V_d$  is checked for saturation. When the output of the current loop saturates, the integration is disabled to prevent integral wind-up.



**Figure 7-30.  $I_d$  Current PI Control**



**Figure 7-31.  $I_q$  Current PI Control**

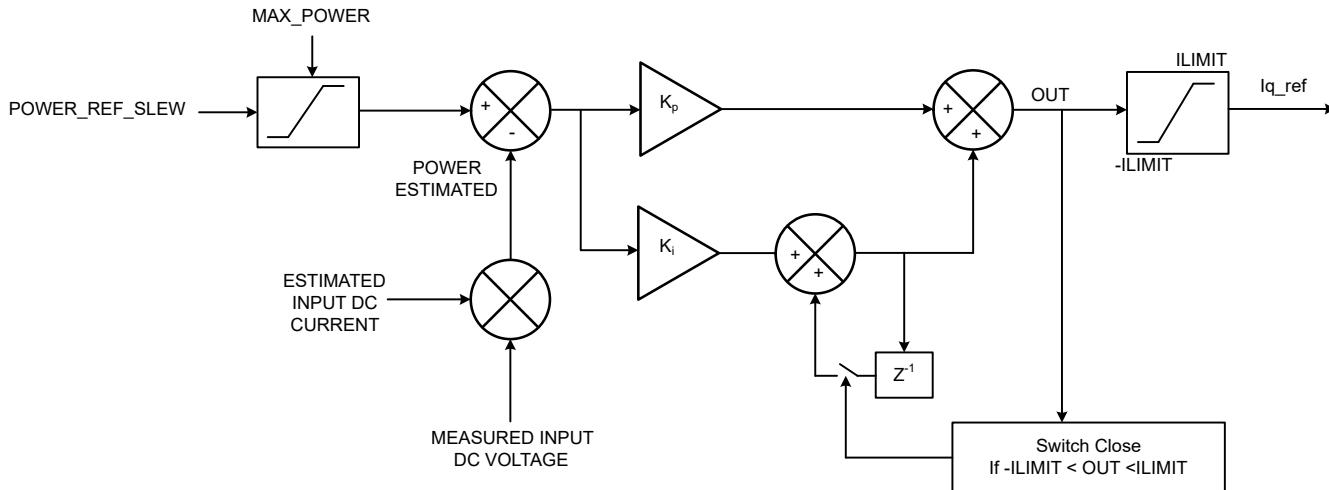
#### 7.3.10.4 Overmodulation

MCF8329HS-Q1 provides overmodulation to operate the motor at a higher speed at the same PVDD voltage by increasing the applied fundamental phase voltage by suitably modifying the applied PWM pattern. This feature can be enabled by setting OVERMODULATION\_ENABLE to 1b.

#### 7.3.10.5 Power Loop

MCF8329HS-Q1 provides an option of regulating the (input DC) power instead of motor speed for a closed loop power control. Input power regulation (instead of motor speed) mode is selected by setting CTRL\_MODE to 01b. The maximum power that MCF8329HS-Q1 can draw from the DC input supply is set by MAX\_POWER. The  $K_p$  and  $K_i$  coefficients for power loop are configured through SPD\_LOOP\_KP and SPD\_LOOP\_KI.

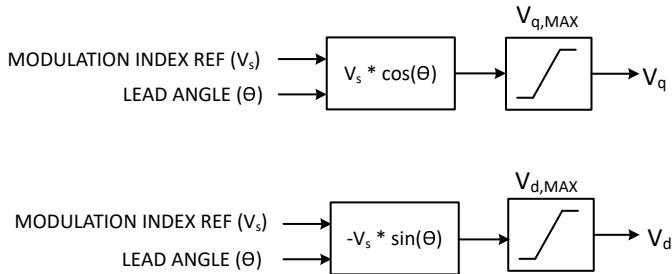
$$POWER\ REF(W) = DUTY\ CMD \times \text{Maximum Power (W)} \quad (9)$$



**Figure 7-32. Closed Loop Power Control**

#### 7.3.10.6 Modulation Index Control

MCF8329HS-Q1 provides voltage control mode, selected by setting CTRL\_MODE to 11b. The closed loop speed control, power control and current control ( $i_q$  and  $i_d$ ) are disabled in this mode. The applied  $V_q$  and  $V_d$  are controlled directly using the user defined modulation index reference voltage (VOLTAGE REF) and the lead angle setting. The VOLTAGE REF varies from MIN\_DUTY to 100%.



**Figure 7-33. Open Loop Voltage Control**

#### Note

1. The maximum modulation index ( $V_s$ ) supported in modulation control mode depends on DIG\_DEAD\_TIME, SINGLE\_SHUNT\_BLANKING\_TIME, and PWM\_FREQ\_OUT settings.

#### 7.3.10.7 Motor Speed Limit

MCF8329HS-Q1 provides the option of limiting the motor speed to a user configured limit. When SPEED\_LIMIT\_ENABLE is set to 1b, irrespective of the input reference mode (current, power or voltage) and operating conditions like (VM, load), MCF8329HS-Q1 limits the motor speed to MAX\_SPEED by restricting the input DC power, motor phase current or voltage (depending on input reference mode). When speed limit is active (motor speed limited at MAX\_SPEED), the acceleration/deceleration rate is set by CL\_SLOW\_ACC instead of CL\_ACC/CL\_DEC to minimize chattering around the MAX\_SPEED value. When the speed limit condition becomes inactive (motor speed < MAX\_SPEED), acceleration/deceleration rate reverts to CL\_ACC/CL\_DEC.

#### 7.3.10.8 Input DC Power Limit

MCF8329HS-Q1 provides the option of limiting the power that the motor driver can draw from the input DC source (VM). When BUS\_POWER\_LIMIT\_ENABLE is set to 1b, irrespective of the input reference mode (speed, current, or voltage) and operating conditions like (VM, load), MCF8329HS-Q1 limits the input DC power to MAX\_POWER by restricting the motor speed, current or voltage (depending on input reference mode). When

power limit is active (input DC power limited at MAX\_POWER), the acceleration/deceleration rate is set by CL\_SLOW\_ACC instead of CL\_ACC/CL\_DEC to minimize chattering around the MAX\_POWER value. When the power limit condition becomes inactive (input DC power < MAX\_POWER), acceleration/deceleration rate reverts to CL\_ACC/CL\_DEC.

### 7.3.11 Maximum Torque Per Ampere (MTPA) Control

PMSM or BLDC motors with magnetic saliency produces a reluctance torque from the difference between the direct-d axis inductance and the quadrature q-axis inductance. The maximum efficiency of the IPM motors can be achieved by proper selection of the current vector ratio between magnetic torque current and reluctance torque current in the total current. MCF8329HS-Q1 provides the maximum torque per ampere control and in that, for a given bus current, it is possible to obtain the best torque performance by setting the d axis current reference as a function of the q axis current reference as per the equation below.

$$i_{d\_MTPA} = \frac{\psi_m}{2(L_q - L_d)} \left( 1 - \sqrt{1 + \frac{4(L_q - L_d)^2 i_q^2}{\psi_m^2}} \right) \quad (10)$$

$L_d$  and  $L_q$  are inductance of the d and q axis respectively.  $i_q$  is the Q-axis current and  $\psi_m$  is the BEMF constant. In case of motors without saliency in the rotor, the inductances of d and q axis are the same and hence the point of maximum torque is always the one where d-axis current reference is 0. For motors with saliency, the d-axis reference can be set as a function of the q-axis reference as derived in the equation above so as to generate the maximum torque for any current drawn from the DC bus.

### 7.3.12 Flux Weakening Control

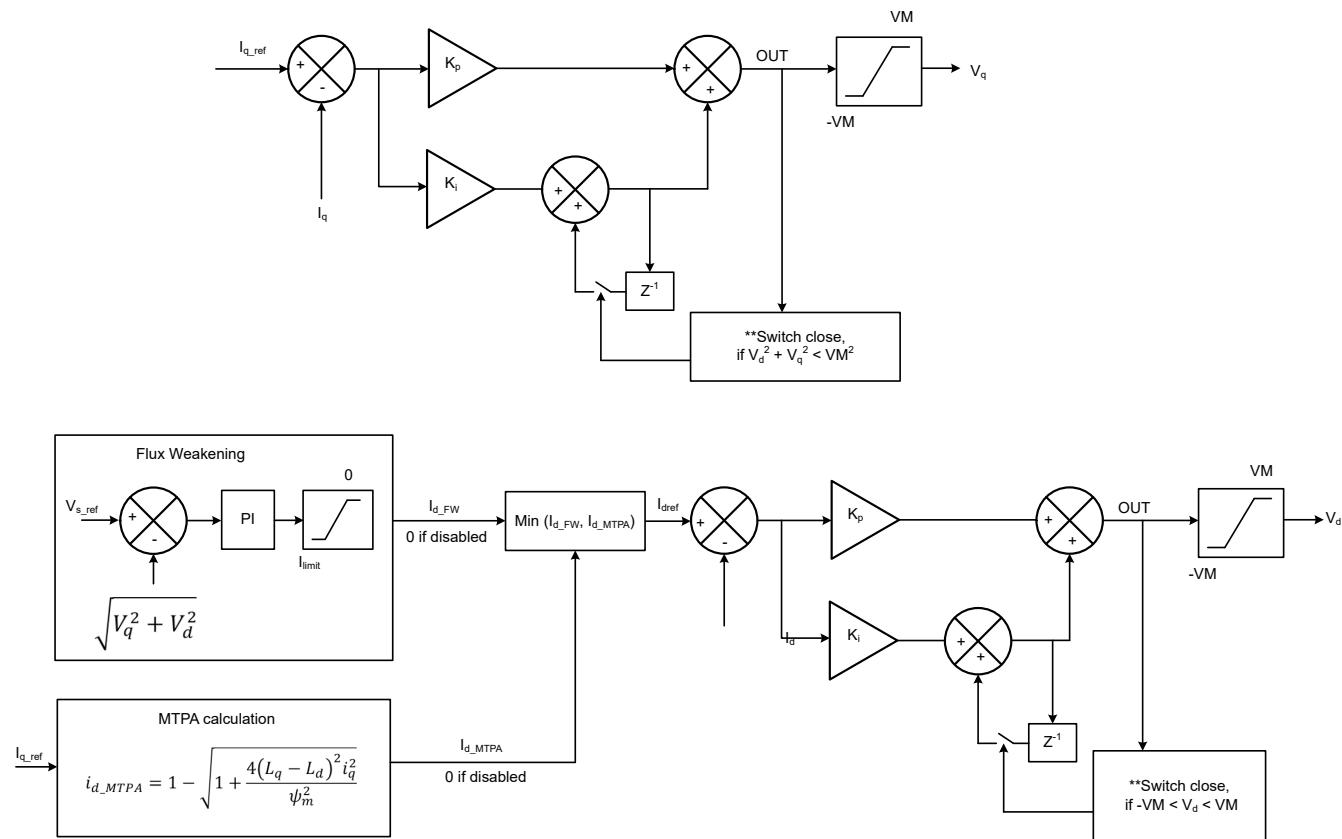
PMSM motors can be operated not only in the constant torque region below the base speed (normally rated speed) but also in the constant power region above the base speed, but the base speed can be varied according to current and voltage limitation. MCF8329HS-Q1 provides a flux weakening control, to increase the speed beyond the motor rated speed. The flux weakening can be enabled by setting 1b to FLUX\_WEAKENING\_EN. The flux weakening control uses a PI control loop as shown in Figure 7-34, to create the  $I_{d\_ref}$ .  $K_p$  and  $K_i$  coefficients for flux weakening loop are configured through FLUX\_WEAKENING\_KP and FLUX\_WEAKENING\_KI.

The absolute maximum value of flux weakening current reference ( $I_{d\_FW}$ ) can be limited as a percentage of ILIMIT by configuring FLUX\_WEAKENING\_CURRENT\_RATIO. If FLUX\_WEAKENING\_CURRENT\_RATIO = 0b, then only circular limit is in place, in that case  $i_q^2 + i_d^2$  is limited to ILIMIT. If  $I_{d\_FW}$  absolute value increases then  $i_q$  is reduced to meet circular limit.

User can configure the modulation index reference,  $V_{s\_ref}$  (shown in Equation 11) below that the flux weakening is not active and  $I_{d\_FW}$  is made to zero. The configuration is available in the bits FLUX\_WEAKENING\_REFERENCE.

$$V_{s\_ref} = \sqrt{V_{q\_ref}^2 + V_{d\_ref}^2} \quad (11)$$

The  $I_{d\_ref}$  can be zero or minimum of  $i_d$  reference from flux weakening or MTPA.



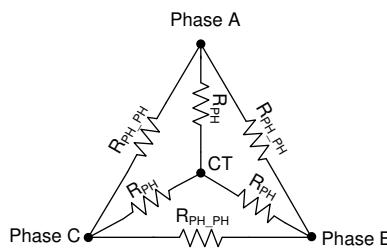
**Figure 7-34. Flux Weakening Control**

### 7.3.13 Motor Parameters

The MCF8329HS-Q1 uses the motor resistance, motor inductance and motor back-EMF constant to estimate motor position when operating in closed loop. The MCF8329HS-Q1 has the capability of measuring back-EMF constant in the offline state (see [Motor Parameter Extraction Tool \(MPET\)](#)). Offline measurement of back-EMF constant, when enabled, takes place before normal motor operation. The user can also disable the offline measurement and configure motor parameters through EEPROM.

#### 7.3.13.1 Motor Resistance

For a wye-connected motor, the motor phase resistance refers to the resistance from the phase output to the center tap,  $R_{PH}$  (denoted as  $R_{PH}$  in [Table 7-2](#)). For a delta-connected motor, the motor phase resistance refers to the equivalent phase to center tap in the wye configuration in [Table 7-2](#).



**Figure 7-35. Motor Resistance**

For both the delta-connected and the wye-connected motor, the easy way to get the equivalent  $R_{PH}$  is to measure the resistance between two phase terminals ( $R_{PH\_PH}$ ), and then divide this value by two,  $R_{PH} = \frac{1}{2} R_{PH\_PH}$ . In wye-connected motor, if user has access to center tap (CT),  $R_{PH}$  can also be measured between center tap (CT) and phase terminal.

Configure the motor resistance ( $R_{PH}$ ) to a nearest value from Table 7-2.

Table 7-2. Motor Resistance Look-Up Table

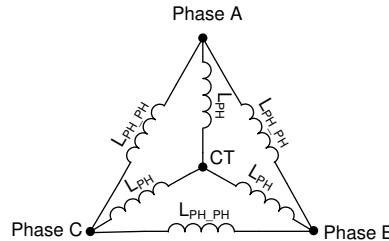
MOTOR_RES (HEX)	$R_{PH}$ ( $\Omega$ )						
0x00	Reserved	0x40	0.017	0x80	0.17	0xC0	1.7
0x01	0.001	0x41	0.0175	0x81	0.175	0xC1	1.75
0x02	0.0011	0x42	0.018	0x82	0.18	0xC2	1.8
0x03	0.0012	0x43	0.0185	0x83	0.185	0xC3	1.85
0x04	0.0013	0x44	0.019	0x84	0.19	0xC4	1.9
0x05	0.0014	0x45	0.0195	0x85	0.195	0xC5	1.95
0x06	0.0015	0x46	0.02	0x86	0.2	0xC6	2
0x07	0.0016	0x47	0.021	0x87	0.21	0xC7	2.1
0x08	0.0017	0x48	0.022	0x88	0.22	0xC8	2.2
0x09	0.0018	0x49	0.023	0x89	0.23	0xC9	2.3
0x0A	0.0019	0x4A	0.024	0x8A	0.24	0xCA	2.4
0x0B	0.002	0x4B	0.025	0x8B	0.25	0xCB	2.5
0x0C	0.0021	0x4C	0.026	0x8C	0.26	0xCC	2.6
0x0D	0.0022	0x4D	0.027	0x8D	0.27	0xCD	2.7
0x0E	0.0023	0x4E	0.028	0x8E	0.28	0xCE	2.8
0x0F	0.0024	0x4F	0.029	0x8F	0.29	0xCF	2.9
0x10	0.0025	0x50	0.03	0x90	0.3	0xD0	3
0x11	0.0026	0x51	0.031	0x91	0.31	0xD1	3.1
0x12	0.0027	0x52	0.032	0x92	0.32	0xD2	3.2
0x13	0.0028	0x53	0.033	0x93	0.33	0xD3	3.3
0x14	0.0029	0x54	0.034	0x94	0.34	0xD4	3.4
0x15	0.003	0x55	0.035	0x95	0.35	0xD5	3.5
0x16	0.0032	0x56	0.036	0x96	0.36	0xD6	3.6
0x17	0.0034	0x57	0.037	0x97	0.37	0xD7	3.7
0x18	0.0036	0x58	0.038	0x98	0.38	0xD8	3.8
0x19	0.0038	0x59	0.039	0x99	0.39	0xD9	3.9
0x1A	0.004	0x5A	0.04	0x9A	0.4	0xDA	4
0x1B	0.0042	0x5B	0.042	0x9B	0.42	0xDB	4.25
0x1C	0.0044	0x5C	0.044	0x9C	0.44	0xDC	4.5
0x1D	0.0046	0x5D	0.046	0x9D	0.46	0xDD	4.75
0x1E	0.0048	0x5E	0.048	0x9E	0.48	0xDE	5
0x1F	0.005	0x5F	0.05	0x9F	0.5	0xDF	5.25
0x20	0.0052	0x60	0.052	0xA0	0.52	0xE0	5.5
0x21	0.0054	0x61	0.054	0xA1	0.54	0xE1	5.75
0x22	0.0056	0x62	0.056	0xA2	0.56	0xE2	6
0x23	0.0058	0x63	0.058	0xA3	0.58	0xE3	6.25
0x24	0.006	0x64	0.06	0xA4	0.6	0xE4	6.5
0x25	0.0062	0x65	0.062	0xA5	0.62	0xE5	7
0x26	0.0064	0x66	0.064	0xA6	0.64	0xE6	7.5
0x27	0.0066	0x67	0.066	0xA7	0.66	0xE7	8
0x28	0.0068	0x68	0.068	0xA8	0.68	0xE8	8.5
0x29	0.007	0x69	0.07	0xA9	0.7	0xE9	9
0x2A	0.0072	0x6A	0.072	0xAA	0.72	0xEA	9.5

**Table 7-2. Motor Resistance Look-Up Table (continued)**

MOTOR_RES (HEX)	R <sub>PH</sub> (Ω)						
0x2B	0.0074	0x6B	0.074	0xAB	0.74	0xEB	10
0x2C	0.0076	0x6C	0.076	0xAC	0.76	0xEC	10.5
0x2D	0.0078	0x6D	0.078	0xAD	0.78	0xED	11
0x2E	0.008	0x6E	0.08	0xAE	0.8	0xEE	11.5
0x2F	0.0085	0x6F	0.085	0xAF	0.82	0xEF	12
0x30	0.009	0x70	0.09	0xB0	0.9	0xF0	12.5
0x31	0.0095	0x71	0.095	0xB1	0.95	0xF1	13
0x32	0.01	0x72	0.1	0xB2	1	0xF2	13.5
0x33	0.0105	0x73	0.105	0xB3	1.05	0xF3	14
0x34	0.011	0x74	0.11	0xB4	1.1	0xF4	14.5
0x35	0.0115	0x75	0.115	0xB5	1.15	0xF5	15
0x36	0.012	0x76	0.12	0xB6	1.2	0xF6	15.5
0x37	0.0125	0x77	0.125	0xB7	1.25	0xF7	16
0x38	0.013	0x78	0.13	0xB8	1.3	0xF8	16.5
0x39	0.0135	0x79	0.135	0xB9	1.35	0xF9	17
0x3A	0.014	0x7A	0.14	0xBA	1.4	0xFA	17.5
0x3B	0.0145	0x7B	0.145	0xBB	1.45	0xFB	18
0x3C	0.015	0x7C	0.15	0xBC	1.5	0xFC	18.5
0x3D	0.0155	0x7D	0.155	0xBD	1.55	0xFD	19
0x3E	0.016	0x7E	0.16	0xBE	1.6	0xFE	19.5
0x3F	0.0165	0x7F	0.165	0xBF	1.65	0xFF	20

### 7.3.13.2 Motor Inductance

For a wye-connected motor, the motor phase inductance refers to the inductance from the phase output to the center tap,  $L_{PH}$  (denoted as  $L_{PH}$  in [Table 7-3](#)). For a delta-connected motor, the motor phase inductance refers to the equivalent phase to center tap in the wye configuration in [Table 7-3](#).


**Figure 7-36. Motor Inductance**

For both the delta-connected motor and the wye-connected motor, the easy way to get the equivalent  $L_{PH}$  is to measure the inductance between two phase terminals ( $L_{PH\_PH}$ ), and then divide this value by two,  $L_{PH} = \frac{1}{2} L_{PH\_PH}$ . In wye-connected motor, if user has access to center tap (CT),  $L_{PH}$  can also be measured between center tap (CT) and phase terminal.

Configure the motor inductance ( $L_{PH}$ ) to a nearest value from [Table 7-3](#).

**Table 7-3. Motor Inductance Look-Up Table**

MOTOR_IND (HEX)	L <sub>PH</sub> (mH)						
0x00	Reserved	0x40	0.017	0x80	0.17	0xC0	1.7
0x01	0.001	0x41	0.0175	0x81	0.175	0xC1	1.75

Table 7-3. Motor Inductance Look-Up Table (continued)

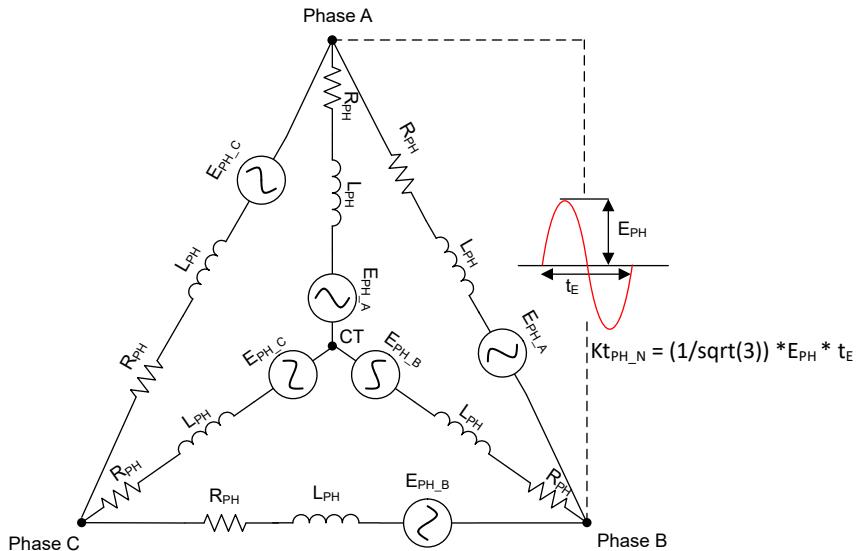
MOTOR_IND (HEX)	L <sub>PH</sub> (mH)						
0x02	0.0011	0x42	0.018	0x82	0.18	0xC2	1.8
0x03	0.0012	0x43	0.0185	0x83	0.185	0xC3	1.85
0x04	0.0013	0x44	0.019	0x84	0.19	0xC4	1.9
0x05	0.0014	0x45	0.0195	0x85	0.195	0xC5	1.95
0x06	0.0015	0x46	0.02	0x86	0.2	0xC6	2
0x07	0.0016	0x47	0.021	0x87	0.21	0xC7	2.1
0x08	0.0017	0x48	0.022	0x88	0.22	0xC8	2.2
0x09	0.0018	0x49	0.023	0x89	0.23	0xC9	2.3
0x0A	0.0019	0x4A	0.024	0x8A	0.24	0xCA	2.4
0x0B	0.002	0x4B	0.025	0x8B	0.25	0xCB	2.5
0x0C	0.0021	0x4C	0.026	0x8C	0.26	0xCC	2.6
0x0D	0.0022	0x4D	0.027	0x8D	0.27	0xCD	2.7
0x0E	0.0023	0x4E	0.028	0x8E	0.28	0xCE	2.8
0x0F	0.0024	0x4F	0.029	0x8F	0.29	0xCF	2.9
0x10	0.0025	0x50	0.03	0x90	0.3	0xD0	3
0x11	0.0026	0x51	0.031	0x91	0.31	0xD1	3.1
0x12	0.0027	0x52	0.032	0x92	0.32	0xD2	3.2
0x13	0.0028	0x53	0.033	0x93	0.33	0xD3	3.3
0x14	0.0029	0x54	0.034	0x94	0.34	0xD4	3.4
0x15	0.003	0x55	0.035	0x95	0.35	0xD5	3.5
0x16	0.0032	0x56	0.036	0x96	0.36	0xD6	3.6
0x17	0.0034	0x57	0.037	0x97	0.37	0xD7	3.7
0x18	0.0036	0x58	0.038	0x98	0.38	0xD8	3.8
0x19	0.0038	0x59	0.039	0x99	0.39	0xD9	3.9
0x1A	0.004	0x5A	0.04	0x9A	0.4	0xDA	4
0x1B	0.0042	0x5B	0.042	0x9B	0.42	0xDB	4.25
0x1C	0.0044	0x5C	0.044	0x9C	0.44	0xDC	4.5
0x1D	0.0046	0x5D	0.046	0x9D	0.46	0xDD	4.75
0x1E	0.0048	0x5E	0.048	0x9E	0.48	0xDE	5
0x1F	0.005	0x5F	0.05	0x9F	0.5	0xDF	5.25
0x20	0.0052	0x60	0.052	0xA0	0.52	0xE0	5.5
0x21	0.0054	0x61	0.054	0xA1	0.54	0xE1	5.75
0x22	0.0056	0x62	0.056	0xA2	0.56	0xE2	6
0x23	0.0058	0x63	0.058	0xA3	0.58	0xE3	6.25
0x24	0.006	0x64	0.06	0xA4	0.6	0xE4	6.5
0x25	0.0062	0x65	0.062	0xA5	0.62	0xE5	7
0x26	0.0064	0x66	0.064	0xA6	0.64	0xE6	7.5
0x27	0.0066	0x67	0.066	0xA7	0.66	0xE7	8
0x28	0.0068	0x68	0.068	0xA8	0.68	0xE8	8.5
0x29	0.007	0x69	0.07	0xA9	0.7	0xE9	9
0x2A	0.0072	0x6A	0.072	0xAA	0.72	0xEA	9.5
0x2B	0.0074	0x6B	0.074	0xAB	0.74	0xEB	10
0x2C	0.0076	0x6C	0.076	0xAC	0.76	0xEC	10.5
0x2D	0.0078	0x6D	0.078	0xAD	0.78	0xED	11

**Table 7-3. Motor Inductance Look-Up Table (continued)**

MOTOR_IND (HEX)	L <sub>PH</sub> (mH)						
0x2E	0.008	0x6E	0.08	0xAE	0.8	0xEE	11.5
0x2F	0.0085	0x6F	0.085	0xAF	0.82	0xEF	12
0x30	0.009	0x70	0.09	0xB0	0.9	0xF0	12.5
0x31	0.0095	0x71	0.095	0xB1	0.95	0xF1	13
0x32	0.01	0x72	0.1	0xB2	1	0xF2	13.5
0x33	0.0105	0x73	0.105	0xB3	1.05	0xF3	14
0x34	0.011	0x74	0.11	0xB4	1.1	0xF4	14.5
0x35	0.0115	0x75	0.115	0xB5	1.15	0xF5	15
0x36	0.012	0x76	0.12	0xB6	1.2	0xF6	15.5
0x37	0.0125	0x77	0.125	0xB7	1.25	0xF7	16
0x38	0.013	0x78	0.13	0xB8	1.3	0xF8	16.5
0x39	0.0135	0x79	0.135	0xB9	1.35	0xF9	17
0x3A	0.014	0x7A	0.14	0xBA	1.4	0xFA	17.5
0x3B	0.0145	0x7B	0.145	0xBB	1.45	0xFB	18
0x3C	0.015	0x7C	0.15	0xBC	1.5	0xFC	18.5
0x3D	0.0155	0x7D	0.155	0xBD	1.55	0xFD	19
0x3E	0.016	0x7E	0.16	0xBE	1.6	0xFE	19.5
0x3F	0.0165	0x7F	0.165	0xBF	1.65	0xFF	20

### 7.3.13.3 Motor Back-EMF constant

The back-EMF constant describes the motor phase-to-neutral back-EMF voltage as a function of the motor speed. For a wye-connected motor, the motor BEMF constant refers to the BEMF as a function of time from the phase output to the center tap,  $Kt_{PH\_N}$  (denoted as  $Kt_{PH\_N}$  in [Table 7-4](#)). For a delta-connected motor, the motor BEMF constant refers to the equivalent phase to center tap in the wye configuration in [Table 7-4](#).


**Figure 7-37. Motor back-EMF constant**

For both the delta-connected motor and the wye-connected motor, the easy way to get the equivalent  $Kt_{PH\_N}$  is to measure the peak value of BEMF on scope for one electrical cycle between two phase terminals ( $E_{PH}$ ), and then multiply by time duration of one electrical cycle and in order to convert from phase-to-phase to phase-to-neutral divide by  $\sqrt{3}$  as shown in [Equation 12](#).

$$Kt_{PH\_N} = \frac{1}{\sqrt{3}} \times E_{PH} \times t_E \quad (12)$$

Configure the motor BEMF constant ( $Kt_{PH\_N}$ ) to a nearest value from [Table 7-4](#).

**Table 7-4. Motor BEMF Constant Look-Up Table**

MOTOR_BEMF_CONST (HEX)	Kt <sub>PH_N</sub> (mV/Hz)	MOTOR_BEMF_CONST (HEX)	Kt <sub>PH_N</sub> (mV/Hz)	MOTOR_BEMF_CONST (HEX)	Kt <sub>PH_N</sub> (mV/Hz)	MOTOR_BEMF_CONST (HEX)	Kt <sub>PH_N</sub> (mV/Hz)
0x00	Self Measurement (see <a href="#">Section 7.3.14</a> )	0x40	1.7	0x80	17	0xC0	170
0x01	0.1	0x41	1.75	0x81	17.5	0xC1	175
0x02	0.11	0x42	1.8	0x82	18	0xC2	180
0x03	0.12	0x43	1.85	0x83	18.5	0xC3	185
0x04	0.13	0x44	1.9	0x84	19	0xC4	190
0x05	0.14	0x45	1.95	0x85	19.5	0xC5	195
0x06	0.15	0x46	2	0x86	20	0xC6	200
0x07	0.16	0x47	2.1	0x87	21	0xC7	210
0x08	0.17	0x48	2.2	0x88	22	0xC8	220
0x09	0.18	0x49	2.3	0x89	23	0xC9	230
0x0A	0.19	0x4A	2.4	0x8A	24	0xCA	240
0x0B	0.2	0x4B	2.5	0x8B	25	0xCB	250
0x0C	0.21	0x4C	2.6	0x8C	26	0xCC	260
0x0D	0.22	0x4D	2.7	0x8D	27	0xCD	270
0x0E	0.23	0x4E	2.8	0x8E	28	0xCE	280
0x0F	0.24	0x4F	2.9	0x8F	29	0xCF	290
0x10	0.25	0x50	3	0x90	30	0xD0	300
0x11	0.26	0x51	3.1	0x91	31	0xD1	310
0x12	0.27	0x52	3.2	0x92	32	0xD2	320
0x13	0.28	0x53	3.3	0x93	33	0xD3	330
0x14	0.29	0x54	3.4	0x94	34	0xD4	340
0x15	0.3	0x55	3.5	0x95	35	0xD5	350
0x16	0.32	0x56	3.6	0x96	36	0xD6	360
0x17	0.34	0x57	3.7	0x97	37	0xD7	370
0x18	0.36	0x58	3.8	0x98	38	0xD8	380
0x19	0.38	0x59	3.9	0x99	39	0xD9	390
0x1A	0.4	0x5A	4	0x9A	40	0xDA	400
0x1B	0.42	0x5B	4.2	0x9B	42	0xDB	425
0x1C	0.44	0x5C	4.4	0x9C	44	0xDC	450
0x1D	0.46	0x5D	4.6	0x9D	46	0xDD	475
0x1E	0.48	0x5E	4.8	0x9E	48	0xDE	500
0x1F	0.5	0x5F	5	0x9F	50	0xDF	525
0x20	0.52	0x60	5.2	0xA0	52	0xE0	550
0x21	0.54	0x61	5.4	0xA1	54	0xE1	575
0x22	0.56	0x62	5.6	0xA2	56	0xE2	600
0x23	0.58	0x63	5.8	0xA3	58	0xE3	625
0x24	0.6	0x64	6	0xA4	60	0xE4	650
0x25	0.62	0x65	6.2	0xA5	62	0xE5	700

**Table 7-4. Motor BEMF Constant Look-Up Table (continued)**

MOTOR_BEMF_CONST (HEX)	Kt <sub>PH_N</sub> (mV/Hz)						
0x26	0.64	0x66	6.4	0xA6	64	0xE6	750
0x27	0.66	0x67	6.6	0xA7	66	0xE7	800
0x28	0.68	0x68	6.8	0xA8	68	0xE8	850
0x29	0.7	0x69	7	0xA9	70	0xE9	900
0x2A	0.72	0x6A	7.2	0xAA	72	0xEA	950
0x2B	0.74	0x6B	7.4	0xAB	74	0xEB	1000
0x2C	0.76	0x6C	7.6	0xAC	76	0xEC	1050
0x2D	0.78	0x6D	7.8	0xAD	78	0xED	1100
0x2E	0.8	0x6E	8	0xAE	80	0xEE	1150
0x2F	0.85	0x6F	8.5	0xAF	85	0xEF	1200
0x30	0.9	0x70	9	0xB0	90	0xF0	1250
0x31	0.95	0x71	9.5	0xB1	95	0xF1	1300
0x32	1	0x72	10	0xB2	100	0xF2	1350
0x33	1.05	0x73	10.5	0xB3	105	0xF3	1400
0x34	1.1	0x74	11	0xB4	110	0xF4	1450
0x35	1.15	0x75	11.5	0xB5	115	0xF5	1500
0x36	1.2	0x76	12	0xB6	120	0xF6	1550
0x37	1.25	0x77	12.5	0xB7	125	0xF7	1600
0x38	1.3	0x78	13	0xB8	130	0xF8	1650
0x39	1.35	0x79	13.5	0xB9	135	0xF9	1700
0x3A	1.4	0x7A	14	0xBA	140	0xFA	1750
0x3B	1.45	0x7B	14.5	0xBB	145	0xFB	1800
0x3C	1.5	0x7C	15	0xBC	150	0xFC	1850
0x3D	1.55	0x7D	15.5	0xBD	155	0xFD	1900
0x3E	1.6	0x7E	16	0xBE	160	0xFE	1950
0x3F	1.65	0x7F	16.5	0xBF	165	0xFF	2000

### 7.3.14 Motor Parameter Extraction Tool (MPET)

The MCF8329HS-Q1 uses motor winding resistance, motor winding inductance and Back-EMF constant to estimate motor position in closed loop operation. The MPET routine measures motor back EMF constant and mechanical load inertia and frictional coefficients. Offline measurement of parameters takes place before normal motor operation. TI recommends to estimate the motor parameters before motor start-up to minimize the impact caused due to possible parameter variations.

Figure 7-38 shows the sequence of operation in the MPET routine. The MPET routine is entered when either the MPET\_CMD bit is set to 1b or a non-zero target speed is set. The MPET routine consists of three steps namely, Open Loop Acceleration, Current Ramp Down and Coasting. Each one of these steps are executed if the condition shown in Figure 7-38 evaluates to TRUE; if the condition evaluates to FALSE, the algorithm bypasses that particular step and moves on to the next step in the sequence. Once all the steps are completed (or bypassed), the algorithm exits the MPET routine. If target speed is set to a non-zero value, the algorithm begins the start-up and acceleration sequence (to target speed reference) once MPET routine is exited.

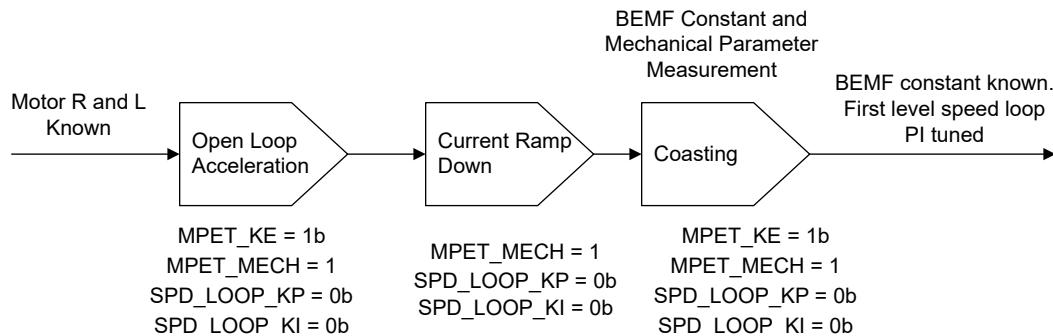


Figure 7-38. MPET Sequence

TI proprietary MPET routine includes following sequence of operation.

- **Open loop Acceleration:** The MPET routine runs align and then open loop acceleration if the back-EMF constant or mechanical parameter measurement are enabled by setting MPET\_KE = 1b and MPET\_MECH = 1b. The MPET routine incorporates the sequences for mechanical parameter measurement, if the speed loop PI constants are defined as zero, even if MPET\_MECH = 0b. This routine uses normal motor operation open loop configuration parameters. The speed slew rate is set by OL\_ACC\_A1 and OL\_ACC\_A2, current reference is set by OL\_ILIMIT and speed reference is set by OPN\_CL\_HANDOFF\_THR.
- **Current Ramp Down:** After open loop acceleration, if the mechanical parameter measurement is enabled, then the MPET routine optimizes the motor current to lower value sufficient to support the load. If mechanical parameter measurement is disabled (MPET\_MECH = 0b, or non-zero speed loop PI parameters) then the MPET will not have the current ramp down sequence.
- **Coasting:** MPET routine completes the sequence by allowing the motor to coast by enabling Hi-Z. The motor back EMF and indicative values of mechanical parameters are measured during the motor coasting period. If the motor back EMF is lower than the threshold defined in STAT\_DETECT\_THR, the MPET\_BEMF\_FAULT is generated.

#### Selecting the parameters from EEPROM or MPET

The MPET estimated values are available in the MTR\_PARAMS Register. Setting the MPET\_WRITE\_SHADOW bit to 1, writes the MPET estimated values to the shadow registers and the user-configured (from EEPROM) values in MOTOR\_BEMF\_CONST, SPD\_LOOP\_KP and SPD\_LOOP\_KI shadow registers will be overwritten by the estimated values from MPET. If any of the shadow registers are initialized to zero (from EEPROM registers), the MPET estimated values are used for those registers independent of the MPET\_WRITE\_SHADOW setting. The MPET calculates the current loop KP and KI by using the user entered resistance and inductance. The MPET does an estimation of the mechanical parameters including the inertia and frictional coefficient at the shaft (includes both motor and shaft coupled load). These values are used to set an initial values speed loop KP and KI. The estimated speed loop KP and KI setting can be used as an initial setting only and TI recommends to tune these parameters on application by the user based on the performance requirement.

#### Note

1. FG signal is not accurate during MPET.
2. If CURRENT\_LOOP\_KP and CURRENT\_LOOP\_KI are set to zero, then MCF8329HS-Q1 automatically calculates these coefficients using motor resistance and inductance values.

#### 7.3.15 Single Hall Sensor Operation

MCF8329HS-Q1 provides the option of redundant motor lock detection using a single digital Hall input - this can be enabled by setting HALL\_EN to 1b. MCF8329HS-Q1 uses the digital Hall input on HALL\_IN pin to detect motor lock condition (in open and closed loop states) and to measure the motor speed; when HALL\_SNS\_STARTUP\_EN is set to 1b, the Hall input is also used to adjust the open loop acceleration rate. If no Hall edge transition is observed on HALL\_IN pin for 500ms when HALL\_EN is set to 1b and input reference

is set to a non-zero value, MCF8329HS-Q1 asserts a motor lock fault and takes protective action as per MTR\_LCK\_MODE.

**Note**

- This is an optional feature - when HALL\_EN is set 0b, MCF8329HS-Q1 operates in sensorless mode using only the integrated observer for motor control and lock detection.
- Set HALL\_ANGLE\_REF = 0h to auto calibrate the Hall sensor offset.
- When HALL\_EN is set to 1b, external MCU reset signal (nMCU\_RST) during watchdog fault is unavailable since the Hall input functionality is mux'ed on the same GPIO pin as nMCU\_RST.

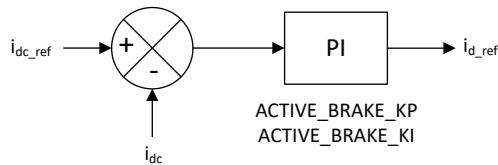
### 7.3.16 Anti-Voltage Surge (AVS)

When a motor is driven, energy is transferred from the power supply into the motor. Some of this energy is stored in the form of inductive and mechanical energy. If the speed command suddenly drops such that the BEMF voltage generated by the motor is greater than the voltage that is applied to the motor, then the mechanical energy of the motor is returned to the power supply and the  $V_{PVDD}$  voltage surges. The AVS feature works to prevent this voltage surge on  $V_{PVDD}$  and can be enabled by setting AVS\_EN to 1b. AVS can be disabled by setting AVS\_EN to 0b.

### 7.3.17 Active Braking

Decelerating the motor quickly requires the motor mechanical energy to be extracted from the rotor in a fast and controlled manner. However, the DC supply voltage increases if the motor mechanical energy is returned to the power supply during the deceleration process. MCF8329HS-Q1 is capable of decelerating the motor quickly without pumping energy back into the supply voltage by using a novel technique called active braking. ACTIVE\_BRAKE\_EN is set to 1b to enable active braking and prevent DC bus voltage spike during fast motor deceleration. Active braking can also be used during reverse drive (see [Section 7.3.9.3](#)) or motor stop (see [Section 7.3.21.4](#)) to reduce the motor speed quickly without DC voltage spike.

The maximum limit on the current sourced from the DC bus ( $i_{dc\_ref}$ ) during active braking can be configured using ACTIVE\_BRAKE\_CURRENT\_LIMIT. The power flow control during active braking is achieved by using both Q-axis ( $i_q$ ) and D-axis ( $i_d$ ) components of current. The D-axis current reference ( $i_{d\_ref}$ ) is generated from the error between DC bus current limit ( $i_{dc\_ref}$ ) and the estimated DC bus current ( $i_{dc}$ ) using a PI controller. The  $i_{dc}$  value is estimated from the measured phase currents, phase voltage and DC bus voltage, using power balance equation (equating the instantaneous DC bus power to sum of all three instantaneous phase power assuming 100% efficiency). During active braking, the DC bus current limit ( $i_{dc\_ref}$ ) starts from zero and linearly increases to ACTIVE\_BRAKE\_CURRENT\_LIMIT with current slew rate as defined by ACTIVE\_BRAKE\_BUS\_CURRENT\_SLEW\_RATE. The gain constants of PI controller can be configured using ACTIVE\_BRAKE\_KP and ACTIVE\_BRAKE\_KI. [Figure 7-39](#) shows the active braking id current control loop.



**Figure 7-39. Active Braking Current Control Loop for  $i_{d\_ref}$**

ACTIVE\_BRAKE\_SPEED\_DELTA\_LIMIT\_ENTRY sets the minimum difference between the initial and target speed above which active braking is entered. For example, consider ACTIVE\_BRAKE\_SPEED\_DELTA\_LIMIT\_ENTRY is set to 10%; if the initial speed is 100% and target speed is set to 95%, MCF8329HS-Q1 uses AVS instead of active braking to reach 95% speed since the difference in commanded speed change (5%) is less than ACTIVE\_BRAKE\_SPEED\_DELTA\_LIMIT\_ENTRY (10%).

**Note**

1. ACTIVE\_BRAKE\_SPEED\_DELTA\_LIMIT\_ENTRY is applicable only during deceleration in forward direction and not used during direction change.
2. During active (or closed loop) braking,  $I_{q\_ref}$  is clamped to -ILIMIT. This ( $I_{q\_ref}$  being clamped to -ILIMIT) can result in the speed PI loop getting saturated and SPEED\_LOOP\_SATURATION bit getting set to 1b during deceleration. This bit is automatically set to 0b once the deceleration is completed and the speed PI loop is out of saturation. Hence, speed loop saturation fault is to be ignored during deceleration.
3. Active braking is only available in speed control mode.
4. Active braking is completed when difference between current speed and target speed is <10%.

### 7.3.18 Output PWM Switching Frequency

MCF8329HS-Q1 provides the option to configure the output PWM switching frequency of the MOSFETs through PWM\_FREQ\_OUT. PWM\_FREQ\_OUT has a range of 10-80 kHz. In order to select optimal output PWM switching frequency, user has to make tradeoff between the current ripple and the switching losses. Generally, motors having lower L/R ratio require higher PWM switching frequency to reduce current ripple.

### 7.3.19 Dead Time Compensation

Dead time is inserted between the switching instants of high-side and low-side MOSFET in a half bridge leg to avoid shoot-through condition. Due to dead time insertion, the expected voltage and applied voltage at the phase node differ based on the phase current direction. The phase node voltage distortion introduces undesired distortion in the phase current causing audible noise. The distortion in current waveform due to dead time appear as sixth harmonic of fundamental frequency in the dq reference frame. The MCF8329HS-Q1 integrates a proprietary dead time compensation, so that the current distortion due to dead time is alleviated. The dead time compensation can be enabled or disabled by configuring DEADTIME\_COMP\_EN. Even when DEADTIME\_COMP\_EN is set to 1b (compensation enabled), dead time compensation is disabled when motor electrical frequency exceeds 108-Hz.

### 7.3.20 Voltage Sense Scaling

The MCF8329HS-Q1 integrates dynamic voltage scaling to improve the resolution of phase voltage and DC bus voltage sensing. The DC bus voltage is sensed at the PVDD pin. The motor phase voltages and DC bus voltage are sensed using an integrated voltage divider with a configurable scaling of 5V/V or 10V/V or 20V/V to limit the sense voltage to less than 3V across operating voltage. Setting the bit DYNAMIC\_VOLTAGE\_GAIN\_EN = 0b disables dynamic voltage scaling and MCF8329HS-Q1 uses BUS\_VOLT setting to configure the voltage scaling. Setting the bit DYNAMIC\_VOLTAGE\_GAIN\_EN = 1b enables dynamic voltage scaling and MCF8329HS-Q1 senses the DC bus voltage during motor start-up and selects the appropriate voltage scaling of 5V/V or 10V/V or 20V/V.

### 7.3.21 Motor Stop Options

The MCF8329HS-Q1 provides different options for stopping the motor which can be configured by MTR\_STOP.

#### 7.3.21.1 Coast (Hi-Z) Mode

Coast (Hi-Z) mode is configured by setting MTR\_STOP to 00b. When motor stop command is received, the MCF8329HS-Q1 turns off all the external MOSFETs creating Hi-Z state at the phase motor terminals. When the MCF8329HS-Q1 transitions from driving the motor into a Hi-Z state, the inductive current in the motor windings continues to flow and the energy returns to the power supply through the body diodes in the MOSFET output stage (see example [Figure 7-40](#)).

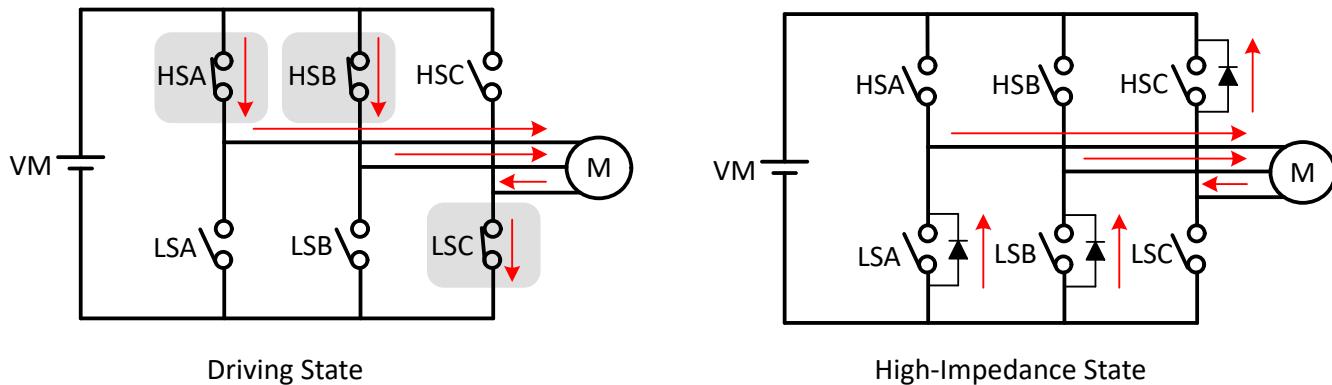


Figure 7-40. Coast (Hi-Z) Mode

In this example, current is applied to the motor through the high-side phase-A MOSFET (HSA), high-side phase-B MOSFET(HSB) and returned through the low-side phase-C MOSFET (LSC). When motor stop command is received all 6 MOSFETs transition to Hi-Z state and the inductive energy returns to supply through body diodes of MOSFETs LSA, LSB and HSC.

#### 7.3.21.2 Recirculation Mode

Recirculation mode is configured by setting MTR\_STOP to 001b. In order to prevent the inductive energy from returning to DC input supply during motor stop, the MCF8329HS-Q1 allows current to circulate within the external MOSFETs by selectively turning OFF some of the active (ON) MOSFETs for a certain time (auto calculated recirculation time to allow the inductive current to decay to zero) before transitioning into Hi-Z by turning OFF the remaining MOSFETs.

Depending on the phase voltage pattern at the time of receiving the stop command, either low-side (see Figure 7-41) or high-side recirculation (see Figure 7-42) will be used to stop the motor without sending the inductive energy back to the DC input supply.

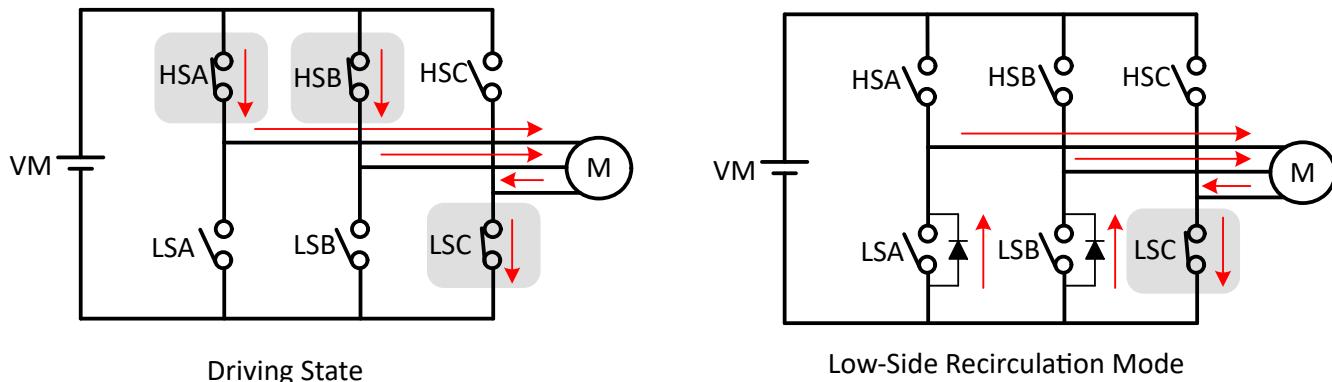


Figure 7-41. Low-Side Recirculation

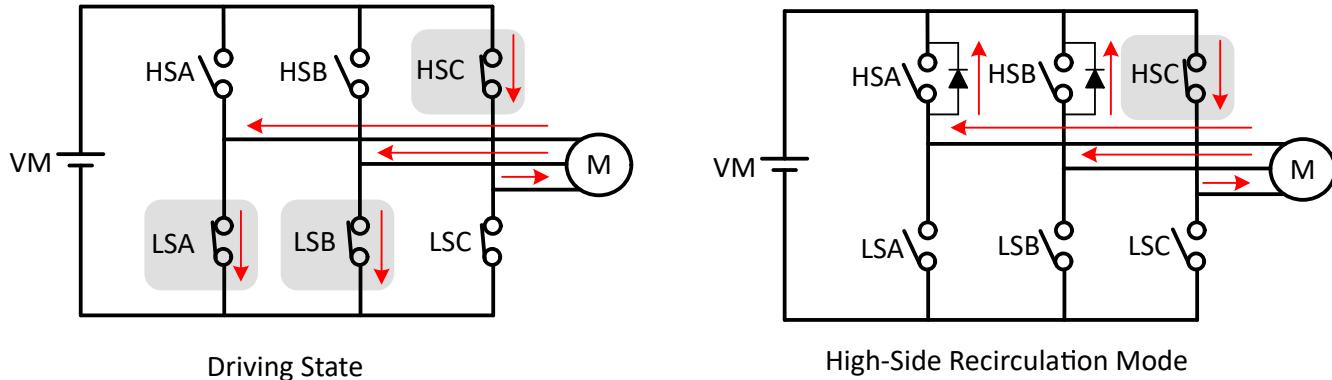


Figure 7-42. High-Side Recirculation

**Note**

1. Recirculation stop is not supported when the motor is in flux weakening zone or MTPA or in active brake mode, and when motor is in any of these states then recirculation stop mode is over written with Hi-Z.
2. Recirculation mode is not supported in modulation index control mode and TI recommends to use other stop modes if modulation index control mode is used.

### 7.3.21.3 Low-Side Braking

Low-side braking mode is configured by setting MTR\_STOP to 01b. When a motor stop command is received, the output speed is reduced to a value defined by BRAKE\_SPEED\_THRESHOLD prior to turning all low-side MOSFETs ON (see example Figure 7-43) for a time configured by MTR\_STOP\_BRK\_TIME. If the motor speed is below BRAKE\_SPEED\_THRESHOLD prior to receiving stop command, then the MCF8329HS-Q1 transitions directly into the brake state. After applying the brake for MTR\_STOP\_BRK\_TIME, the MCF8329HS-Q1 transitions into the Hi-Z state by turning OFF all MOSFETs.

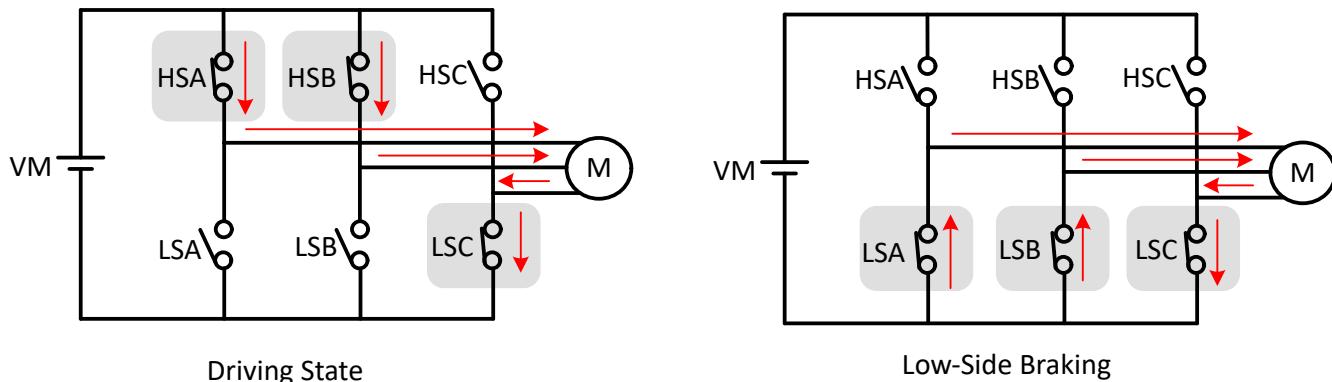


Figure 7-43. Low-Side Braking

The MCF8329HS-Q1 can also enter low-side braking through BRAKE pin input. When BRAKE pin is pulled to HIGH state, the output speed is reduced to a value defined by BRAKE\_SPEED\_THRESHOLD prior to turning all low-side MOSFETs ON. In this case, MCF8329HS-Q1 stays in low-side brake state till BRAKE pin changes to LOW state. When BRAKE pin is pulled to HIGH state without a run command (REF is set to 0), then MCF8329HS-Q1 turns ON all low-side MOSFETs immediately.

### 7.3.21.4 Active Spin-Down

Active spin down mode is configured by setting MTR\_STOP to 10b. When a motor stop command is received, the MCF8329HS-Q1 reduces SPEED\_REF to ACT\_SPIN\_THR and then transitions to Hi-Z state by turning all

MOSFETs OFF. The advantage of this mode is that by reducing SPEED\_REF, the motor is decelerated to lower speed thereby reducing the phase currents before entering Hi-Z. Now, when the motor transitions into Hi-Z state, the energy transfer to the power supply is reduced. The threshold ACT\_SPIN\_THR needs to be configured high enough for MCF8329HS-Q1 to not lose synchronization with the motor.

### 7.3.22 FG Configuration

The MCF8329HS-Q1 provides information about the motor speed through the Frequency Generate (FG) pin. In MCF8329HS-Q1, the FG pin output is configured through FG\_CONFIG. When FG\_CONFIG is configured to 0b, the FG output is active as long as the MCF8329HS-Q1 is driving the motor. When FG\_CONFIG is configured to 1b, the MCF8329HS-Q1 provides an FG output as long as the MCF8329HS-Q1 is driving the motor and also during coasting until the motor back-EMF falls below the threshold configured by FG\_BEMF\_THRESHOLD.

#### 7.3.22.1 FG Output Frequency

The FG output frequency can be configured by FG\_DIV. Many applications require the FG output to provide a pulse for every mechanical rotation of the motor. Different FG\_DIV configurations can accomplish this for 2-pole up to 30-pole motors.

Figure 7-44 shows the FG output when MCF8329HS-Q1 has been configured to provide FG pulses thrice every electrical cycle, once every electrical cycle (2 poles), once every two electrical cycle (4 poles), once every three electrical cycles (6 poles), once every four electrical cycles (8 poles), and so on.

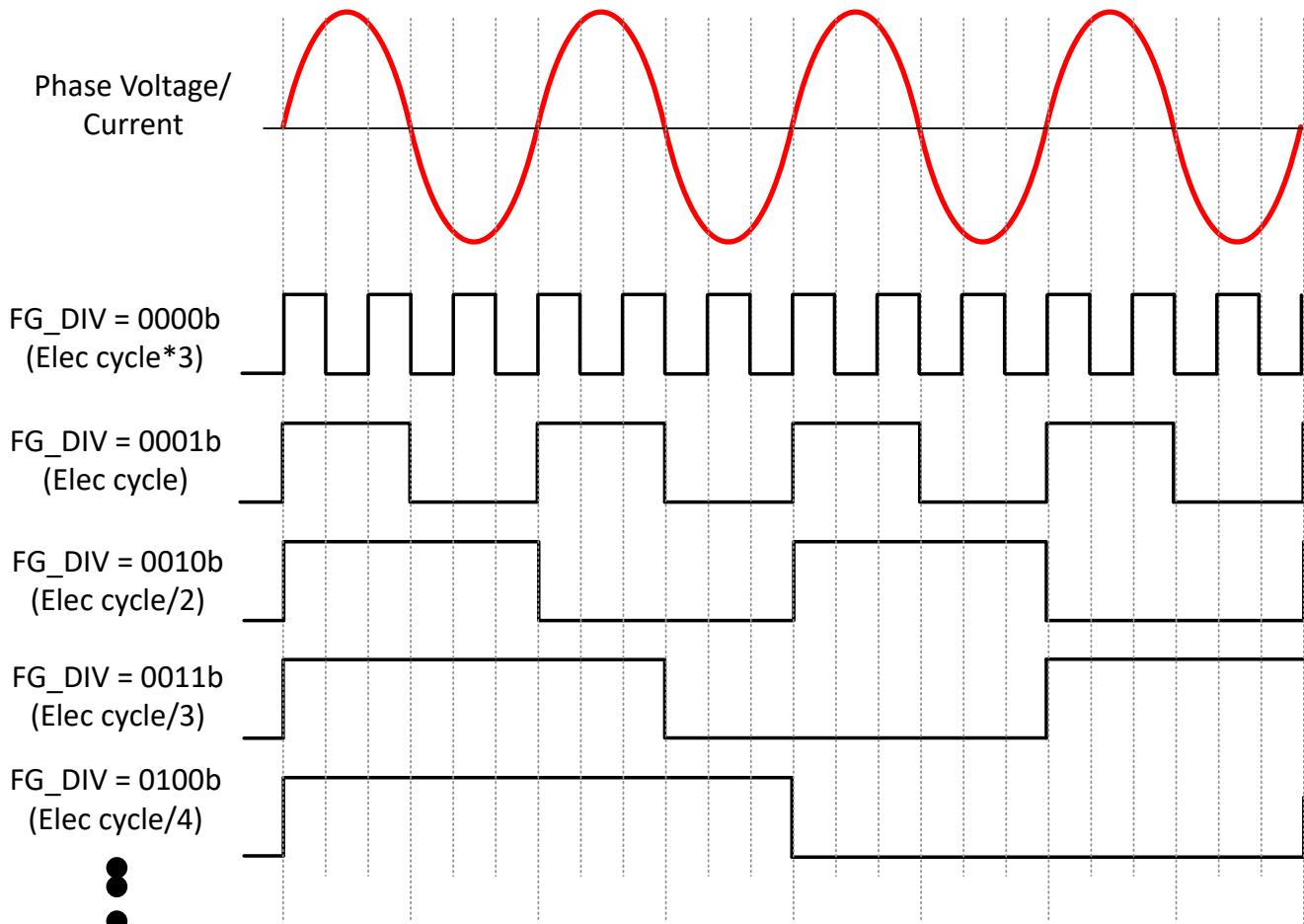


Figure 7-44. FG Frequency Divider

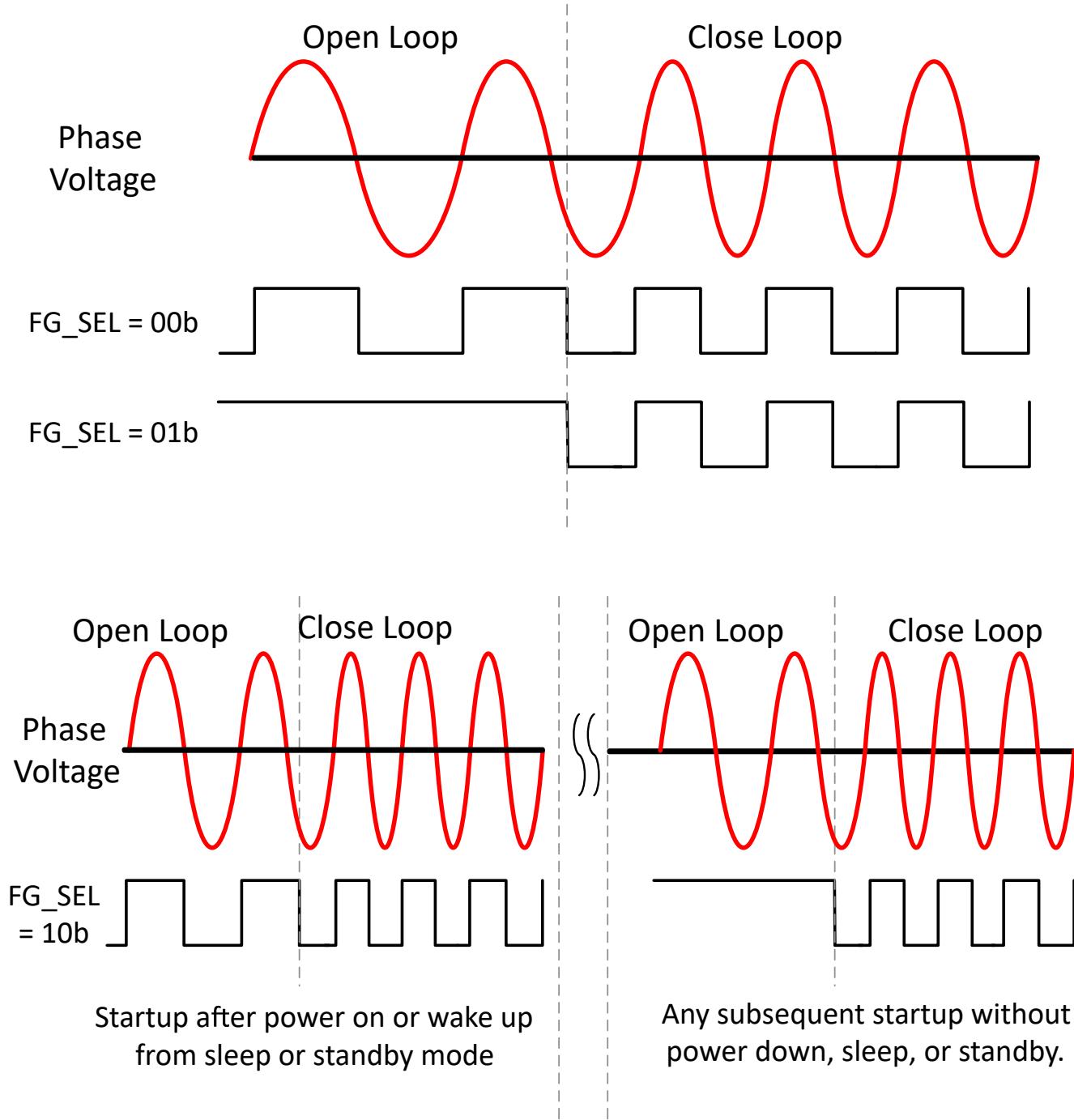
### 7.3.22.2 FG in Open-Loop

During closed loop (commutation) operation, the driving speed (FG output frequency) and the actual motor speed are synchronized. During open-loop operation, however, FG may not reflect the actual motor speed. The open loop and closed loop here refers to the motor commutation method and not referred to closed loop speed or power control.

The MCF8329HS-Q1 provides three options for controlling the FG output during open loop, as shown in [Figure 7-45](#). The selection of these options is configured through FG\_SEL.

If FG\_SEL is set to,

- 00b : Output FG in ISD, open loop and closed loop.
- 01b : Output FG in only closed loop. FG pin will be Hi-Z (high with external pull up) during open loop.
- 10b: The FG output will reflect the driving frequency during open loop operation in the first motor start-up cycle after power-on, sleep/standby; FG will be Hi-Z (high with external pull up) during open loop operation in subsequent start-up cycles.



**Figure 7-45. FG Behavior During Open Loop**

#### 7.3.22.3 FG During Motor Stop

The FG pin state when the motor stops rotating can be defined using FG\_IDLE\_CONFIG. The motor stop is decided by FG\_BEMF\_THR.

#### 7.3.22.4 FG Behavior During Fault

The FG behavior during faults (those reported on nFAULT pin) can be configured using FG\_FAULT\_CONFIG.

In addition to reporting fault status on FG, MCF8329HS-Q1 also provides the option of reporting the fault type on FG pin by encoding the fault type information as a unique duty cycle at 1Hz frequency as shown in [Figure 7-46](#).

Eight types of faults can be reported on FG pin - loss of phase (no motor), motor lock, over current (VDS, VSNS, lock current limits), PVDD over voltage, PVDD under voltage, over temperature, external MCU (watchdog and I<sup>2</sup>C CRC) and dry run.

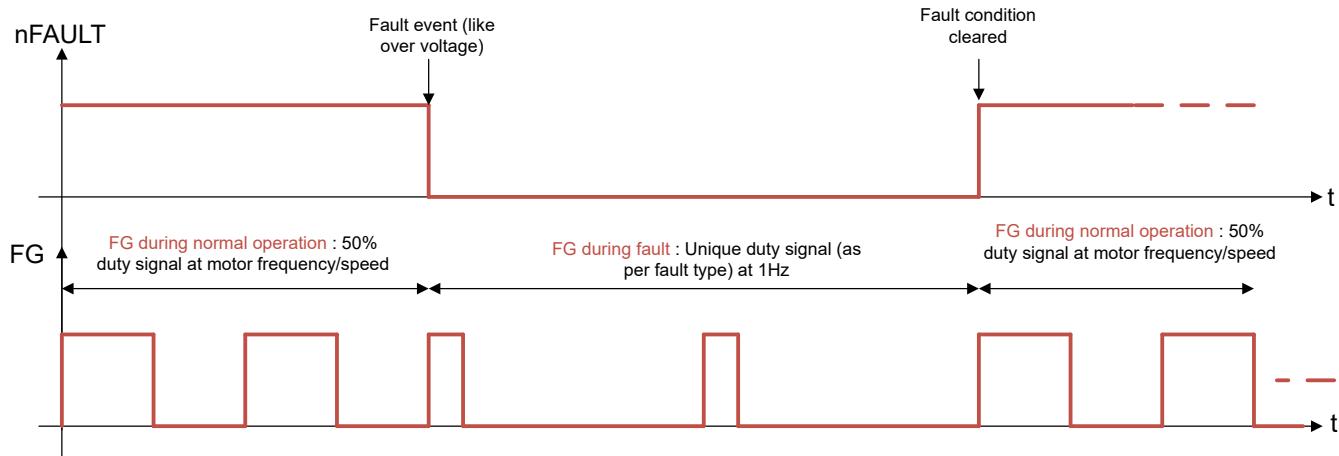


Figure 7-46. Fault Indication over FG

The duty cycle and priority (1 being the highest) associated with each fault type indicated on FG pin is as shown in [Table 7-5](#),

Table 7-5. Duty cycle and Priority for Fault Indication on FG pin

Fault Type	Duty Cycle	Priority
Loss of phase	10	1
Over current	20	2
Motor lock	30	3
Dry run	90	4
External MCU	80	5
Over temperature	70	6
PVDD under voltage	40	7
PVDD over voltage	60	8

If FG\_FAULT\_CONFIG is set to,

- 00b: FG pin pulled low on fault.
- 01b: FG pin in Hi-Z (high with external pull up) on reported faults.
- 10b: FG reports fault type as a unique duty cycle at 1Hz
- 11b: FG active till BEMF drops below BEMF threshold defined by FG\_BEMF\_THRESHOLD if FG\_CONFIG is set to 1b

#### Note

Fault type reporting on FG pin is not available in case of retry faults with retry time < 1s (FG signal time period for fault type reporting) or when a particular type of fault is configured in 'report only' mode.

#### 7.3.23 Protections

The MCF8329HS-Q1 is protected from a host of fault events including motor lock, PVDD undervoltage, AVDD undervoltage, GVDD undervoltage, bootstrap undervoltage, overtemperature and overcurrent events. [Table 7-6](#) summarizes the response, recovery modes, gate driver status, reporting mechanism for different faults.

**Note**

1. Actionable and report only faults (latched or retry) are always reported on nFAULT pin (as logic low).
2. Priority order for multi-fault scenarios is latched > slower retry time fault > faster retry time fault > report only fault. For example, if a latched and retry fault happen simultaneously, the device stays latched in fault mode until user issues clear fault command by writing 1b to CLR\_FLT or through a power recycle. If two retry faults with different retry times happen simultaneously, the device retries only after the longer (slower) retry time lapses.
3. Recovery refers only to state of gate driver after the fault condition is removed. Automatic indicates that the device automatically recovers (and gate driver outputs and hence external FETs are active) when retry time lapses after the fault condition is removed. Latched indicates that the device waits for clearing of fault condition (by writing 1b to CLR\_FLT bit) or through a power recycle.
4. The GVDD undervoltage, BST under voltage, VDS OCP, SENSE OCP faults can take up to 200ms after fault response (gate driver outputs pulled low to put the external FETs in Hi-Z) to be reported on nFAULT pin (as logic low).
5. Latched faults can take up to 200ms after CLR\_FLT command is issued (over I<sup>2</sup>C) to be cleared.
6. CLR\_FLT command (over I<sup>2</sup>C) will clear all the faults (and corresponding fault status bits) including latched, automatic recovery (retry) and report only faults.
7. When device resumes normal operation after retry time (of an automatic recovery fault) lapses, fault status bits of all automatic recovery (retry) and report only faults set to 1b are cleared (reset to 0b) automatically.

**Table 7-6. Fault Action and Response**

FAULT	CONDITION	CONFIGURATION	REPORT	GATE DRIVER	LOGIC	RECOVERY
PVDD under-voltage (PVDD_UV)	$V_{PVDD} < V_{PVDD\_UV}$	—	nFAULT	Disabled	Disabled	Automatic: $V_{PVDD} > V_{PVDD\_UV}$
AVDD POR (AVDD_POR)	$V_{AVDD} < V_{AVDD\_POR}$	—	nFAULT	Disabled	Disabled	Automatic: $V_{AVDD} > V_{AVDD\_POR}$
GVDD under-voltage (GVDD_UV)	$V_{GVDD} < V_{GVDD\_UV}$	GVDD_UV_MODE = 0b	nFAULT and GATE_DRIVER_FAULT_STATUS Register	Pulled Low <sup>(1)</sup>	Active	Latched: CLR_FLT
		GVDD_UV_MODE = 1b	nFAULT and GATE_DRIVER_FAULT_STATUS Register	Pulled Low <sup>(1)</sup>	Active	Retry: $t_{LCK\_RETRY}$
BSTx under-voltage (BST_UV)	$V_{BSTx} - V_{SHx} < V_{BST\_UV}$	DIS_BST_FLT = 0b BST_UV_MODE = 0b	nFAULT and GATE_DRIVER_FAULT_STATUS Register	Pulled Low <sup>(1)</sup>	Active	Latched: CLR_FLT
		DIS_BST_FLT = 0b BST_UV_MODE = 1b	nFAULT and GATE_DRIVER_FAULT_STATUS Register	Pulled Low <sup>(1)</sup>	Active	Retry: $t_{LCK\_RETRY}$
V <sub>DS</sub> overcurrent (VDS_OCP)	$V_{DS} > V_{SEL\_VDS\_LVL}$	DIS_VDS_FLT = 0b VDS_FLT_MODE = 0b	nFAULT and GATE_DRIVER_FAULT_STATUS Register	Pulled Low <sup>(1)</sup>	Active	Latched: CLR_FLT
		DIS_VDS_FLT = 0b VDS_FLT_MODE = 1b	nFAULT and GATE_DRIVER_FAULT_STATUS Register	Pulled Low <sup>(1)</sup>	Active	Retry: $t_{LCK\_RETRY}$

Table 7-6. Fault Action and Response (continued)

FAULT	CONDITION	CONFIGURATION	REPORT	GATE DRIVER	LOGIC	RECOVERY
V <sub>SENSE</sub> overcurrent (SEN_OCP) V <sub>SENSE</sub> overcurrent (SEN_OCP)	V <sub>SP</sub> > V <sub>SENSE_LVL</sub>	DIS_SNS_FLT = 0b SNS_FLT_MODE = 0b	nFAULT and GATE_DRIVER_FAULT_STATUS Register	Pulled Low <sup>(1)</sup>	Active	Latched: CLR_FLT
		DIS_SNS_FLT = 0b SNS_FLT_MODE = 1b	nFAULT and GATE_DRIVER_FAULT_STATUS Register	Pulled Low <sup>(1)</sup>	Active	Retry: t <sub>LCK_RETRY</sub>
3 Motor Lock (MTR_LCK)	Motor lock: Abnormal Speed; No Motor Lock; Abnormal BEMF	MTR_LCK_MODE = 000b	nFAULT and CONTROLLER_FAULT_STATUS register	Pulled Low <sup>(1)</sup> (MOSFETs in Hi-Z)	Active	Latched: CLR_FLT
		MTR_LCK_MODE = 001b or 010b	nFAULT and CONTROLLER_FAULT_STATUS register	Low side brake	Active	Latched: CLR_FLT
		MTR_LCK_MODE = 011b	nFAULT and CONTROLLER_FAULT_STATUS register	Pulled Low <sup>(1)</sup> (MOSFETs in Hi-Z)	Active	Retry: t <sub>LCK_RETRY</sub>
		MTR_LCK_MODE = 100b or 101b	nFAULT and CONTROLLER_FAULT_STATUS register	Low side brake	Active	Retry: t <sub>LCK_RETRY</sub>
		MTR_LCK_MODE = 110b	nFAULT and CONTROLLER_FAULT_STATUS register	Active	Active	No action
		MTR_LCK_MODE = 111b	None	Active	Active	No action
Hardware Lock-Detection Current Limit (HW_LOCK_ILIMIT)	Phase Current > HW_LOCK_ILIMIT	HW_LOCK_ILIMIT_MODE = 000b	nFAULT and CONTROLLER_FAULT_STATUS register	Pulled Low <sup>(1)</sup> (MOSFETs in Hi-Z)	Active	Latched: CLR_FLT
		HW_LOCK_ILIMIT_MODE = 001b or 010b	nFAULT and CONTROLLER_FAULT_STATUS register	Low-side brake	Active	Latched: CLR_FLT
		HW_LOCK_ILIMIT_MODE = 011b	nFAULT and CONTROLLER_FAULT_STATUS register	Pulled Low <sup>(1)</sup> (MOSFETs in Hi-Z)	Active	Retry: t <sub>LCK_RETRY</sub>
		HW_LOCK_ILIMIT_MODE = 100b or 101b	nFAULT and CONTROLLER_FAULT_STATUS register	Low-side brake	Active	Retry: t <sub>LCK_RETRY</sub>
		HW_LOCK_ILIMIT_MODE = 110b	nFAULT and CONTROLLER_FAULT_STATUS register	Active	Active	No action
		HW_LOCK_ILIMIT_MODE = 111b	None	Active	Active	No action

**Table 7-6. Fault Action and Response (continued)**

FAULT	CONDITION	CONFIGURATION	REPORT	GATE DRIVER	LOGIC	RECOVERY
ADC based Lock-Detection Current Limit (LOCK_ILIMIT)	Phase Current > LOCK_ILIMIT	LOCK_ILIMIT_MODE = 000b	nFAULT and CONTROLLER_FAULT_STATUS register	Pulled Low <sup>(1)</sup> (MOSFETs in Hi-Z)	Active	Latched: CLR_FLT
		LOCK_ILIMIT_MODE = 001b or 010b	nFAULT and CONTROLLER_FAULT_STATUS register	Low-side brake	Active	Latched: CLR_FLT
		LOCK_ILIMIT_MODE = 011b	nFAULT and CONTROLLER_FAULT_STATUS register	Pulled Low <sup>(1)</sup> (MOSFETs in Hi-Z)	Active	Retry: t <sub>LCK_RETRY</sub>
		LOCK_ILIMIT_MODE = 100b or 101b	nFAULT and CONTROLLER_FAULT_STATUS register	Low-side brake	Active	Retry: t <sub>LCK_RETRY</sub>
		LOCK_ILIMIT_MODE = 110b	nFAULT and CONTROLLER_FAULT_STATUS register	Active	Active	No action
		LOCK_ILIMIT_MODE = 111b	None	Active	Active	No action
MPET Back-EMF Fault (MPET_BEMF_FAULT)	Motor Back EMF < STAT_DETECT_THR	MPET_CMD = 1 or MPET_KE = 1	nFAULT and CONTROLLER_FAULT_STATUS register	Hi-Z	Active	Latched: CLR_FLT
Maximum V <sub>PVDD</sub> (over-voltage) fault	V <sub>PVDD</sub> > MAX_VM_MOTOR, if MAX_VM_MOTOR ≠ 000b	MAX_VM_MODE = 0b	nFAULT and CONTROLLER_FAULT_STATUS register	Pulled Low <sup>(1)</sup> (MOSFETs in Hi-Z)	Active	Latched: CLR_FLT
		MAX_VM_MODE = 1b	nFAULT and CONTROLLER_FAULT_STATUS register	Pulled Low <sup>(1)</sup> (MOSFETs in Hi-Z)	Active	Automatic: (V <sub>VM</sub> < MAX_VM_MOTOR - VOLTAGE_HYSTERE SIS) V
Minimum V <sub>PVDD</sub> (under-voltage) fault	V <sub>PVDD</sub> < MIN_VM_MOTOR, if MIN_VM_MOTOR ≠ 000b	MIN_VM_MODE = 0b	nFAULT and CONTROLLER_FAULT_STATUS register	Pulled Low <sup>(1)</sup> (MOSFETs in Hi-Z)	Active	Latched: CLR_FLT
		MIN_VM_MODE = 1b	nFAULT and CONTROLLER_FAULT_STATUS register	Pulled Low <sup>(1)</sup> (MOSFETs in Hi-Z)	Active	Automatic: (V <sub>VM</sub> > MIN_VM_MOTOR + VOLTAGE_HYSTERE SIS) V
Current Loop Saturation	Indication of current loop saturation due to lower V <sub>VM</sub>	SATURATION_FLAG_S_EN = 1b	nFAULT and CONTROLLER_FAULT_STATUS register	Active; motor speed/power/current may not reach reference	Active	Automatic: motor will reach reference operating point upon exiting saturation
Speed/power Loop Saturation	Indication of speed/power loop saturation due to lower V <sub>VM</sub> , lower ILIMIT setting etc.,	SATURATION_FLAG_S_EN = 1b	nFAULT and CONTROLLER_FAULT_STATUS register	Active; motor speed/power may not reach reference	Active	Automatic: motor will reach reference operating point upon exiting saturation

Table 7-6. Fault Action and Response (continued)

FAULT	CONDITION	CONFIGURATION	REPORT	GATE DRIVER	LOGIC	RECOVERY
External Watchdog Fault	Time between watchdog tickles > EXT_WD_CONFIG	EXT_WD_EN = 1b EXT_WD_FAULT_M_ODE = 0b and LIMP_HOME_EN = 0b	nFAULT and CONTROLLER_FAULT_STATUS register	Active	Active	No action
		EXT_WD_EN = 1b EXT_WD_FAULT_M_ODE = 0b and LIMP_HOME_EN = 1b	nFAULT and CONTROLLER_FAULT_STATUS register	Active (reference latched at current value till CLRFLT)	Active	Latched: CLRFLT
		EXT_WD_EN = 1b EXT_WD_FAULT_M_ODE = 1b and LIMP_HOME_EN = 0b	nFAULT and CONTROLLER_FAULT_STATUS register	Pulled Low (MOSFETs in Hi-Z)	Active	Latched: CLRFLT
		EXT_WD_EN = 1b EXT_WD_FAULT_M_ODE = 1b and LIMP_HOME_EN = 1b	nFAULT and CONTROLLER_FAULT_STATUS register	Active (reference latched at REF_OFF 1)	Active	Latched: CLRFLT
EEPROM Fault	Indicates EEPROM contents error/mismatch; content evaluation happens whenever a EEPROM read is issued	EEP_FAULT_MODE = 0b	nFAULT and CONTROLLER_FAULT_STATUS register	Pulled Low (MOSFETs in Hi-Z)	Active	Latched: CLRFLT
		EEP_FAULT_MODE = 1b	nFAULT and CONTROLLER_FAULT_STATUS register	Active	Active	No action
I <sup>2</sup> C CRC Fault	Indicates error in I <sup>2</sup> C transaction as a CRC mismatch	I2C_CRC_ERR_MODE = 0b	nFAULT and CONTROLLER_FAULT_STATUS register	Pulled Low (MOSFETs in Hi-Z)	Active	Latched: CLRFLT
		I2C_CRC_ERR_MODE = 1b	nFAULT and CONTROLLER_FAULT_STATUS register	Active	Active	No action
Dry Run Detection	Refer Section 7.3.23.14	DRY_RUN_MODE = 00b	None	Active	Active	No action
		DRY_RUN_MODE = 01b	nFAULT and CONTROLLER_FAULT_STATUS register	Active	Active	No action
		DRY_RUN_MODE = 10b	nFAULT and CONTROLLER_FAULT_STATUS register	Pulled Low (MOSFETs in Hi-Z)	Active	Retry: tLCK_RETRY
		DRY_RUN_MODE = 11b	nFAULT and CONTROLLER_FAULT_STATUS register	Pulled Low (MOSFETs in Hi-Z)	Active	Latched: CLRFLT

**Table 7-6. Fault Action and Response (continued)**

FAULT	CONDITION	CONFIGURATION	REPORT	GATE DRIVER	LOGIC	RECOVERY
Thermal shutdown (TSD)	$T_J > T_{TSD}$	OTS_AUTO_RECCOVERY = 0b	nFAULT and GATE_DRIVER_FAULT_STATUS Register	Pulled Low (MOSFETs in Hi-Z) <sup>(1)</sup>	Active	Latched: CLR_FLT
		OTS_AUTO_RECCOVERY = 1b	nFAULT and GATE_DRIVER_FAULT_STATUS Register	Pulled Low (MOSFETs in Hi-Z) <sup>(1)</sup>	Active	Automatic: $T_J < T_{OTSD} - T_{HYS}$

(1) Pulled Low: GHx and GLx are actively pulled low by the gate driver

#### Note

Any fault reporting on nFAULT pin or CONTROLLER\_FAULT\_STATUS register or GATE\_DRIVER\_FAULT\_STATUS register can have a latency up to 200ms.

#### 7.3.23.1 PVDD Supply Undervoltage Lockout (PVDD\_UV)

If at any time the power supply voltage on the PVDD pin falls below the  $V_{PVDD\_UV}$  threshold for longer than the  $t_{PVDD\_UV\_DG}$  time, the device detects a PVDD undervoltage event. After detecting the undervoltage condition, the gate driver is disabled, the charge pump is disabled, the internal digital logic is disabled, and the nFAULT pin is driven low. Normal operation starts again (the gate driver becomes operable and the nFAULT pin is released) when the PVDD pin rises above  $V_{PVDD\_UV}$ .

#### 7.3.23.2 AVDD Power on Reset (AVDD\_POR)

If at any time the supply voltage on the AVDD pin falls below the  $V_{AVDD\_POR}$  threshold for longer than the  $t_{AVDD\_POR\_DG}$  time, the device enters an inactive state, disabling the gate driver, the charge pump, and the internal digital logic, and nFAULT is driven low. Normal operation (digital logic operational) requires AVDD to exceed  $V_{AVDD\_POR}$  level.

#### 7.3.23.3 GVDD Undervoltage Lockout (GVDD\_UV)

If at any time the voltage on the GVDD pin falls lower than the  $V_{GVDD\_UV}$  threshold voltage for longer than the  $t_{GVDD\_UV\_DG}$  time, the device detects a GVDD undervoltage event. After detecting the GVDD\_UV undervoltage event, all of the gate driver outputs are driven low to disable the external MOSFETs, the charge pump is still running and nFAULT pin is driven low.

The device can be configured in a latched fault state or retry mode upon a GVDD\_UV condition using the GVDD\_UV\_MODE bit. With GVDD\_UV\_MODE = 0b, normal operation resumes after the GVDD\_UV condition is cleared and a clear fault command is issued through the CLR\_FLT bit. With GVDD\_UV\_MODE = 1b, normal operation resumes after the GVDD\_UV condition is cleared and a time period of  $t_{LCK\_RETRY}$  is elapsed.

#### 7.3.23.4 BST Undervoltage Lockout (BST\_UV)

If at any time the voltage across BSTx and SHx pins falls lower than the  $V_{BST\_UV}$  threshold voltage for longer than the  $t_{BST\_UV\_DG}$  time, the device detects a BST undervoltage event. After detecting the BST\_UV event, all of the gate driver outputs are driven low to disable the external MOSFETs, and nFAULT pin is driven low. BST\_UV can be disabled by configuring DIS\_BST\_FLT to 1b.

The device can be configured in a latched fault state or retry mode upon a BST\_UV condition using the BST\_UV\_MODE bit. With BST\_UV\_MODE = 0b, normal operation resumes after the BST\_UV condition is cleared and a clear fault command is issued through the CLR\_FLT bit. With BST\_UV\_MODE = 1b, normal operation resumes after the BST\_UV condition is cleared and a time period of  $t_{LCK\_RETRY}$  is elapsed.

### 7.3.23.5 MOSFET VDS Overcurrent Protection (VDS\_OCP)

The device has adjustable VDS voltage monitors to detect overcurrent or short-circuit conditions on the external power MOSFETs. A MOSFET overcurrent event is sensed by monitoring the VDS voltage drop across the external MOSFET  $R_{DS(on)}$ . The high-side VDS monitors measure between the PVDD and SHx pins and the low-side VDS monitors measure between the SHx and LSS pins. If the voltage across external MOSFET exceeds the threshold set by SEL\_VDS\_LVL for longer than the  $t_{DS\_DG}$  deglitch time, a  $V_{DS\_OCP}$  event is recognized. After detecting the VDS overcurrent event, all of the gate driver outputs are driven low to disable the external MOSFETs and nFAULT pin is driven low.  $V_{DS\_OCP}$  can be disabled by configuring DIS\_VDS\_FLT to 1b.

The device can be configured in a latched fault state or retry mode upon a  $V_{DS\_OCP}$  event using the VDS\_FLT\_MODE bit. With VDS\_FLT\_MODE = 0b, normal operation resumes after the  $V_{DS\_OCP}$  condition is cleared and a clear fault command is issued through the CLR\_FLT bit. With VDS\_FLT\_MODE = 1b, normal operation resumes after the  $V_{DS\_OCP}$  condition is cleared and a time period of  $t_{LCK\_RETRY}$  is elapsed. FET-wise VDS fault information is available in GATE\_DRIVER\_FAULT\_STATUS register.

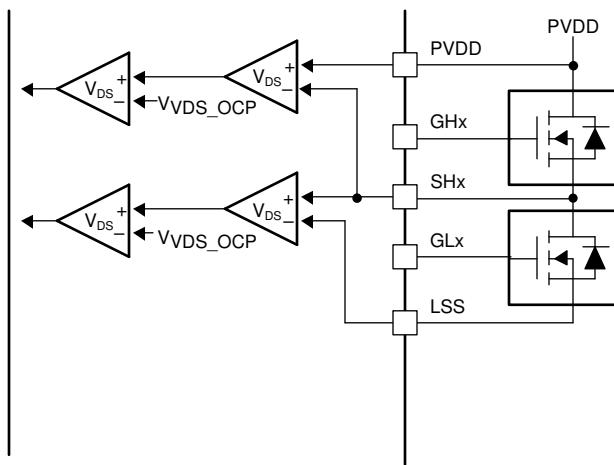


Figure 7-47. VDS Monitors

### 7.3.23.6 VSENSE Overcurrent Protection (SEN\_OCP)

Overcurrent is also monitored by sensing the voltage drop across the external current sense resistor between LSS and GND pin. If at any time the voltage on the LSS input exceeds the VSEN\_OCP threshold for longer than the  $t_{DS\_DG}$  deglitch time, a SEN\_OCP event is recognized. After detecting the SEN\_OCP overcurrent event, all of the gate driver outputs are driven low to disable the external MOSFETs and nFAULT pin is driven low. The  $V_{SENSE}$  threshold is fixed at 0.5V.  $V_{SEN\_OCP}$  can be disabled by configuring DIS\_SNS\_FLT to 1b.

The device can be configured in a latched fault state or retry mode upon a  $V_{DS\_OCP}$  event using the SNS\_FLT\_MODE bit. With SNS\_FLT\_MODE = 0b, normal operation resumes after the  $V_{SEN\_OCP}$  condition is cleared and a clear fault command is issued through the CLR\_FLT bit. With SNS\_FLT\_MODE = 1b, normal operation resumes after the  $V_{SEN\_OCP}$  condition is cleared and a time period of  $t_{LCK\_RETRY}$  is elapsed.

### 7.3.23.7 Thermal Shutdown (OTSD)

If the die temperature exceeds the trip point of the thermal shutdown limit ( $T_{OTSD}$ ), an OTSD event is recognized. After detecting the OTSD overtemperature event, all of the gate driver outputs are driven low to disable the external MOSFETs, and nFAULT pin is driven low. The over temperature protection can be configured for a latched mode or automatic recovery mode by configuring OTS\_AUTO\_RECOVERY. In latched mode, normal operation resumes after the  $T_{OTSD}$  condition is cleared and a clear fault command is issued through the CLR\_FLT bit. In automatic recovery mode, normal operation resumes after the  $T_{OTSD}$  condition is cleared.

### 7.3.23.8 Hardware Lock Detection Current Limit (HW\_LOCK\_ILIMIT)

The hardware lock detection current limit function provides a configurable threshold for limiting the current to prevent damage to the system. The output of current sense amplifier is connected to hardware

comparator. If at any time, the voltage on the output of CSA exceeds HW\_LOCK\_ILIMIT threshold for a time longer than  $t_{HW\_LOCK\_ILIMIT}$ , a HW\_LOCK\_ILIMIT event is recognized and action is taken according to the HW\_LOCK\_ILIMIT\_MODE. The threshold is set through HW\_LOCK\_ILIMIT, the  $t_{HW\_LOCK\_ILIMIT}$  is set through the HW\_LOCK\_ILIMIT\_DEG. HW\_LOCK\_ILIMIT\_MODE bit can operate in four different modes: HW\_LOCK\_ILIMIT latched shutdown, HW\_LOCK\_ILIMIT automatic retry, HW\_LOCK\_ILIMIT report only, and HW\_LOCK\_ILIMIT disabled.

#### **7.3.23.8.1 HW\_LOCK\_ILIMIT Latched Shutdown (HW\_LOCK\_ILIMIT\_MODE = 00xb or 010b)**

When a HW\_LOCK\_ILIMIT event happens in this mode, the status of MOSFET will be configured by HW\_LOCK\_ILIMIT\_MODE and nFAULT is driven low. Status of MOSFETs during HW\_LOCK\_ILIMIT:

- MTR\_LCK\_MODE = 000b: All external MOSFETs are turned OFF, the gate driver outputs pulled low.
- MTR\_LCK\_MODE = 001b or 010b: All low-side MOSFETs (gate driver outputs) are turned ON.

The CONTROLLER\_FAULT and HW\_LOCK\_ILIMIT bits are set to 1b in the fault status registers. Normal operation resumes (gate driver operation and the nFAULT pin is released) when the HW\_LOCK\_ILIMIT condition clears and a clear fault command is issued through the CLR\_FLT bit.

#### **7.3.23.8.2 HW\_LOCK\_ILIMIT Automatic recovery (HW\_LOCK\_ILIMIT\_MODE = 011b or 10xb)**

When a HW\_LOCK\_ILIMIT event happens in this mode, the status of MOSFET will be configured by HW\_LOCK\_ILIMIT\_MODE and nFAULT is driven low. Status of MOSFET during HW\_LOCK\_ILIMIT:

- MTR\_LCK\_MODE = 011b: All external MOSFETs are turned OFF, the gate driver outputs pulled low.
- MTR\_LCK\_MODE = 100b or 101b: All low-side MOSFETs (gate driver outputs) are turned ON.

The CONTROLLER\_FAULT and HW\_LOCK\_ILIMIT bits are set to 1b in the fault status registers. Normal operation resumes automatically (gate driver operation and the nFAULT pin is released) after the  $t_{LCK\_RETRY}$  (configured by LCK\_RETRY) time lapses. The CONTROLLER\_FAULT and HW\_LOCK\_ILIMIT bits are reset to 0b after the  $t_{LCK\_RETRY}$  period expires.

#### **7.3.23.8.3 HW\_LOCK\_ILIMIT Report Only (HW\_LOCK\_ILIMIT\_MODE = 110b)**

No protective action is taken when a HW\_LOCK\_ILIMIT event happens in this mode. The hardware lock detection current limit event is reported by setting the CONTROLLER\_FAULT and HW\_LOCK\_ILIMIT bits to 1b in the fault status registers and nFAULT is pulled low. The gate drivers continue to operate. The external controller manages this condition by acting appropriately. The reporting clears when the HW\_LOCK\_ILIMIT condition clears and a clear fault command is issued through the CLR\_FLT bit.

#### **7.3.23.8.4 HW\_LOCK\_ILIMIT Disabled (HW\_LOCK\_ILIMIT\_MODE = 111b)**

No action is taken when a HW\_LOCK\_ILIMIT event happens in this mode.

### **7.3.23.9 Lock Detection Current Limit (LOCK\_ILIMIT)**

The lock detection current limit function provides a configurable threshold for limiting the current to prevent damage to the system. The MCF8329HS-Q1 continuously monitors the output of the current sense amplifier (CSA) through the ADC. If at any time, any phase current exceeds LOCK\_ILIMIT for a time longer than  $t_{LOCK\_ILIMIT}$ , a LOCK\_ILIMIT event is recognized and action is taken according to LOCK\_ILIMIT\_MODE. The threshold is set through LOCK\_ILIMIT and the  $t_{LOCK\_ILIMIT}$  is set through LOCK\_ILIMIT\_DEG. LOCK\_ILIMIT\_MODE can be set to four different modes: LOCK\_ILIMIT latched shutdown, LOCK\_ILIMIT automatic retry, LOCK\_ILIMIT report only and LOCK\_ILIMIT disabled.

#### **7.3.23.9.1 LOCK\_ILIMIT Latched Shutdown (LOCK\_ILIMIT\_MODE = 00xb or 010b)**

When a LOCK\_ILIMIT event happens in this mode, the status of external MOSFETs will be configured by LOCK\_ILIMIT\_MODE and nFAULT is driven low. Status of external MOSFETs driven from MCF8329HS-Q1 during LOCK\_ILIMIT:

- MTR\_LCK\_MODE = 000b: All external MOSFETs are turned OFF, the gate driver outputs pulled low.
- MTR\_LCK\_MODE = 001b or 010b: All low-side MOSFETs (gate driver outputs) are turned ON.

The CONTROLLER\_FAULT and LOCK\_ILIMIT bits are set to 1b in the fault status registers. Normal operation resumes (gate driver operation and the nFAULT pin is released) when the LOCK\_ILIMIT condition clears and a clear fault command is issued through the CLR\_FLT bit.

#### 7.3.23.9.2 *LOCK\_ILIMIT Automatic Recovery (LOCK\_ILIMIT\_MODE = 011b or 10xb)*

When a LOCK\_ILIMIT event happens in this mode, the status of external MOSFETs will be configured by LOCK\_ILIMIT\_MODE and nFAULT is driven low. Status of external MOSFETs driven from MCF8329HS-Q1 during LOCK\_ILIMIT:

- MTR\_LCK\_MODE = 011b: All external MOSFETs are turned OFF, the gate driver outputs pulled low.
- MTR\_LCK\_MODE = 100b or 101b: All low-side MOSFETs (gate driver outputs) are turned ON.

The CONTROLLER\_FAULT and LOCK\_ILIMIT bits are set to 1b in the fault status registers. Normal operation resumes automatically (gate driver operation and the nFAULT pin is released) after the  $t_{LCK\_RETRY}$  (configured by LCK\_RETRY) time lapses. The CONTROLLER\_FAULT and LOCK\_ILIMIT bits are reset to 0b after the  $t_{LCK\_RETRY}$  period expires.

#### 7.3.23.9.3 *LOCK\_ILIMIT Report Only (LOCK\_ILIMIT\_MODE = 110b)*

No protective action is taken when a LOCK\_ILIMIT event happens in this mode. The lock detection current limit event is reported by setting the CONTROLLER\_FAULT and LOCK\_ILIMIT bits to 1b in the fault status registers and nFAULT is pulled low. The gate drivers continue to operate. The external controller manages this condition by acting appropriately. The reporting clears when the LOCK\_ILIMIT condition clears and a clear fault command is issued through the CLR\_FLT bit.

#### 7.3.23.9.4 *LOCK\_ILIMIT Disabled (LOCK\_ILIMIT\_MODE = 111b)*

No action is taken when a LOCK\_ILIMIT event happens in this mode.

### 7.3.23.10 Motor Lock (MTR\_LCK)

The MCF8329HS-Q1 continuously checks for different motor lock conditions (see [Motor Lock Detection](#)) during motor operation. When one of the enabled lock condition happens, a MTR\_LCK event is recognized and action is taken according to the MTR\_LCK\_MODE.

MCF8329HS-Q1 locks can be enabled or disabled individually and retry times can be configured through LCK\_RETRY. MTR\_LCK\_MODE bit can operate in four different modes: MTR\_LCK latched shutdown, MTR\_LCK automatic retry, MTR\_LCK report only and MTR\_LCK disabled.

#### 7.3.23.10.1 *MTR\_LCK Latched Shutdown (MTR\_LCK\_MODE = 00xb or 010b)*

When a MTR\_LCK event happens in this mode, the status of external MOSFETs will be configured by MTR\_LCK\_MODE and nFAULT is driven low. Status of external MOSFETs during MTR\_LCK:

- MTR\_LCK\_MODE = 000b: All external MOSFETs are turned OFF, the gate driver outputs pulled low.
- MTR\_LCK\_MODE = 001b or 010b: All low-side MOSFETs (gate driver outputs) are turned ON.

The CONTROLLER\_FAULT, MTR\_LCK and respective motor lock condition bits are set to 1b in the fault status registers. Normal operation resumes (gate driver operation and the nFAULT pin is released) when the MTR\_LCK condition clears and a clear fault command is issued through the CLR\_FLT bit.

#### 7.3.23.10.2 *MTR\_LCK Automatic Recovery (MTR\_LCK\_MODE = 011b or 10xb)*

When a MTR\_LCK event happens in this mode, the status of MOSFETs will be configured by MTR\_LCK\_MODE and nFAULT is driven low. Status of MOSFETs during MTR\_LCK:

- MTR\_LCK\_MODE = 011b: All external MOSFETs are turned OFF, the gate driver outputs pulled low.
- MTR\_LCK\_MODE = 100b or 101b: All low-side MOSFETs (gate driver outputs) are turned ON.

The CONTROLLER\_FAULT, MTR\_LCK and respective motor lock condition bits are set to 1b in the fault status registers. Normal operation resumes automatically (gate driver operation and the nFAULT pin is released) after the  $t_{LCK\_RETRY}$  (configured by LCK\_RETRY) time lapses. The CONTROLLER\_FAULT, MTR\_LCK and respective motor lock condition bits are reset to 0b after the  $t_{LCK\_RETRY}$  period expires.

#### 7.3.23.10.3 MTR\_LCK Report Only (MTR\_LCK\_MODE = 110b)

No protective action is taken when a MTR\_LCK event happens in this mode. The motor lock event is reported by setting the CONTROLLER\_FAULT, MTR\_LCK and respective motor lock condition bits to 1b in the fault status registers and nFAULT pin is pulled low. The gate drivers continue to operate. The external controller manages this condition by acting appropriately. The reporting clears when the MTR\_LCK condition clears and a clear fault command is issued through the CLR\_FLT bit.

#### 7.3.23.10.4 MTR\_LCK Disabled (MTR\_LCK\_MODE = 111b)

No action is taken when a MTR\_LCK event happens in this mode.

### 7.3.23.11 Motor Lock Detection

The MCF8329HS-Q1 provides different lock detect mechanisms to determine if the motor is in a locked state. Multiple detection mechanisms work together to ensure the lock condition is detected quickly and reliably. In addition to detecting if there is a locked motor condition, the MCF8329HS-Q1 can also identify and take action if there is no motor connected to the system. Each of the lock detect mechanisms and the no-motor detection can be disabled by their respective register bits.

#### 7.3.23.11.1 Lock 1: Abnormal Speed (ABN\_SPEED)

MCF8329HS-Q1 monitors the speed continuously and at any time the speed exceeds LOCK\_ABN\_SPEED, an ABN\_SPEED lock event is recognized and action is taken according to the MTR\_LCK\_MODE.

The threshold is set through the LOCK\_ABN\_SPEED register. ABN\_SPEED lock can be enabled/disabled by LOCK1\_EN.

#### 7.3.23.11.2 Lock 2: Abnormal BEMF (ABN\_BEMF)

MCF8329HS-Q1 estimates back-EMF in order to run motor optimally in closed loop. This estimated back-EMF is compared against the expected back-EMF calculated using the estimated speed and the BEMF constant. Whenever motor is stalled the estimated back-EMF is inaccurate due to lower back-EMF at low speed. When the difference between estimated and expected back-EMF exceeds ABNORMAL\_BEMF\_THR, an abnormal BEMF fault is triggered and action is taken according to the MTR\_LCK\_MODE.

ABN\_BEMF lock can be enabled/disabled by LOCK2\_EN.

#### 7.3.23.11.3 Lock3: No-Motor Fault (NO\_MTR)

The MCF8329HS-Q1 continuously monitors phase currents on all three phases; if any phase current stays below NO\_MTR\_THR for 500ms during open loop, a NO\_MTR event is recognized. The response to the NO\_MTR event is configured through MTR\_LCK\_MODE. NO\_MTR lock can be enabled/disabled by LOCK3\_EN.

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#### Note

For a reliable detection of no-motor fault, ensure that the open loop time is sufficiently higher than 500 ms.

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### 7.3.23.12 MPET Faults

An error during BEMF constant measurement is reported using MPET\_BEMF\_FAULT. This fault gets triggered when the measured back EMF is less than the threshold set in STAT\_DETECT\_THR. One example of such fault scenario can be the motor stall while running in open loop due to incorrect open loop configuration used.

### 7.3.23.13 IPD Faults

The MCF8329HS-Q1 uses 12-bit timers to estimate the time during the current ramp up in IPD, when the motor start-up is configured as IPD (MTR\_STARTUP is set to 10b). During IPD, the algorithm checks for a successful current ramp-up to IPD\_CURR\_THR, starting with an IPD clock of 10MHz; if unsuccessful (timer overflow before current reaches IPD\_CURR\_THR), IPD is repeated with lower frequency clocks of 1MHz, 100kHz, and 10kHz sequentially. If the IPD timer overflows (current does not reach IPD\_CURR\_THR) with all the four clock frequencies, then the IPD\_T1\_FAULT gets triggered. The user can enable IPD timeout (IPD timer overflow) by setting IPD\_TIMEOUT\_FAULT\_EN to 1b.

IPD gives incorrect results if the next IPD pulse is commanded before the complete decay of current due to present IPD pulse. The MCF8329HS-Q1 can generate a fault called IPD\_FREQ\_FAULT during such a scenario by setting IPD\_FREQ\_FAULT\_EN to 1b. The IPD\_FREQ\_FAULT maybe triggered if the IPD frequency is too high for the IPD current limit or if the motor inductance is too high for the IPD frequency and IPD current limit.

#### 7.3.23.14 Dry Run Detection

MCF8329HS-Q1 provides the option of dry run detection when pumps are operating with insufficient fluid. Dry run is a dangerous operating condition that can damage pumps - timely detection and preventive action is necessary to protect pumps. Dry run is characterized by the motor operating continuously at a lower current/power than when operating with sufficient fluid. Dry run detection is enabled when DRY\_RUN\_MODE ≠ 00b. The threshold speed for dry run detection is configured by DRY\_RUN\_SPEED\_THR - even when enabled, dry run detection is active only when motor speed is higher than DRY\_RUN\_SPEED\_THR. The q-axis current threshold ( $I_{DRY\_RUN}$ ) for detecting dry run can either be fixed across motor speed (DRY\_RUN\_ILIM\_MODE = 0b) or variable (DRY\_RUN\_ILIM\_MODE = 1b).  $I_{DRY\_RUN}$  is fixed to DRY\_RUN\_ILIM when DRY\_RUN\_ILIM\_MODE = 0b. When DRY\_RUN\_ILIM\_MODE = 1b,  $I_{DRY\_RUN}$  varies with motor speed as shown in [Figure 7-49](#). The  $I_q$  current must be lower than  $I_{DRY\_RUN}$  for a deglitch time interval set by DRY\_RUN\_TDEG before dry run fault is triggered as shown in [Figure 7-48](#).

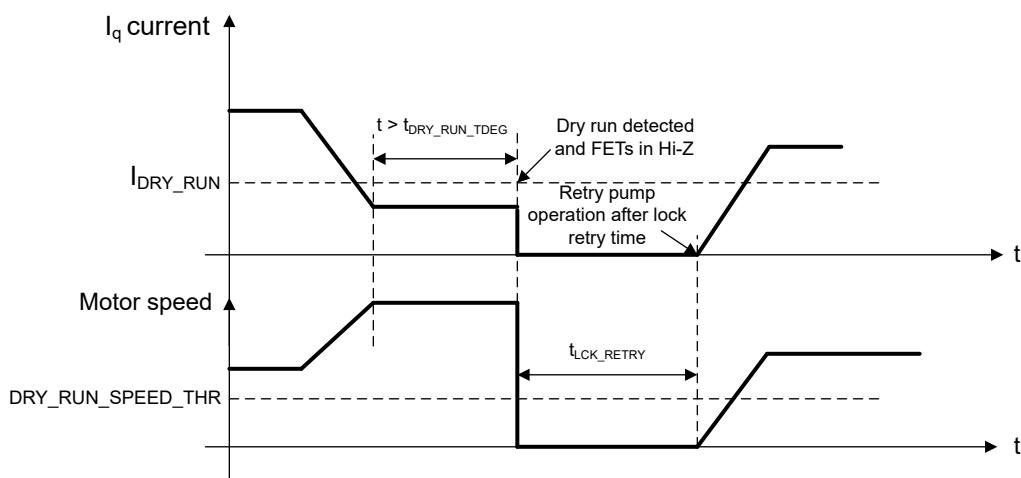


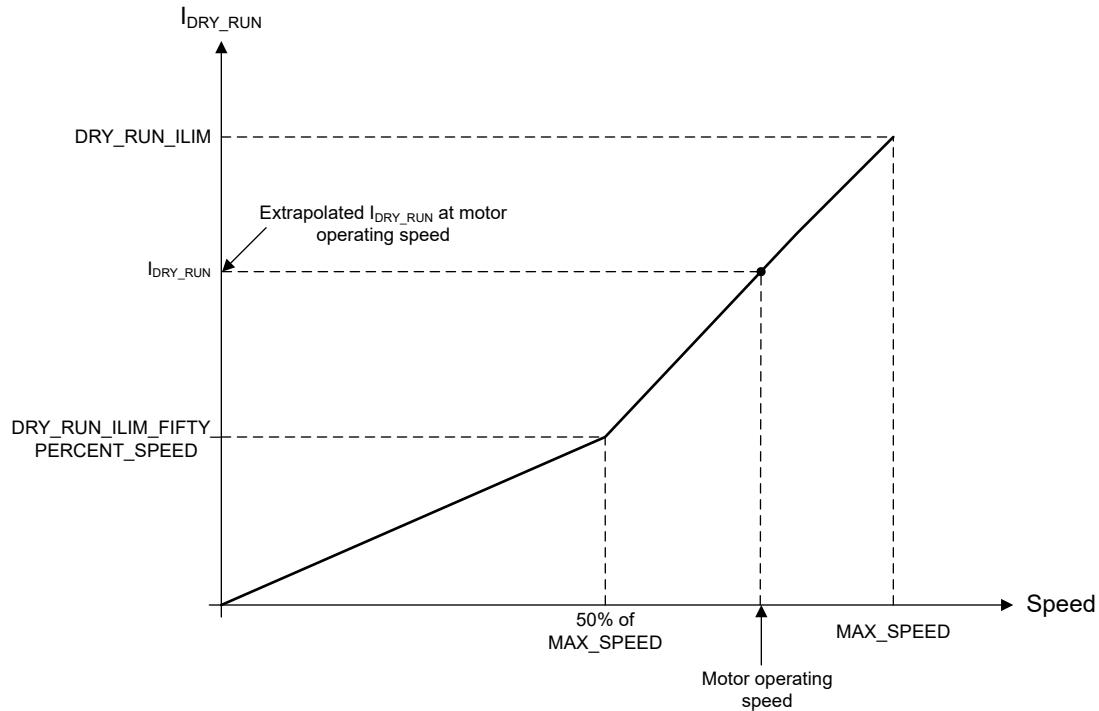
Figure 7-48. Dry Run Detection

On detection of dry run condition, action is taken based on DRY\_RUN\_MODE. If DRY\_RUN\_MODE is set to 11b, all external FETs are turned off (PWMS are pulled low), nFAULT is pulled low, CONTROLLER\_FAULT, DRY\_RUN bits are set to 1b until a clear fault command is issued by external MCU through the CLR\_FLT bit. If DRY\_RUN\_MODE is set to 10b, all external FETs are turned off (PWMS are pulled low), nFAULT is pulled low - normal operation resumes automatically (gate driver operation and the nFAULT pin is released) after the  $t_{LCK\_RETRY}$  (configured by LCK\_RETRY) time lapses. The CONTROLLER\_FAULT and DRY\_RUN bits are reset to 0b after the  $t_{LCK\_RETRY}$  period expires.

MCF8329HS-Q1 provides the option to vary  $I_{DRY\_RUN}$  as a function of motor speed to detect dry run in pumps that can operate at multiple speeds (or flow rates) during normal operation. User must set DRY\_RUN\_ILIM to the expected  $I_q$  current at 100% speed and DRY\_RUN\_ILIM\_FIFTY\_PERCENT\_SPEED to the expected  $I_q$  current at 50% speed. MCF8329HS-Q1 will use DRY\_RUN\_ILIM as  $I_{DRY\_RUN}$  when motor is at 100% speed and DRY\_RUN\_ILIM\_FIFTY\_PERCENT\_SPEED as  $I_{DRY\_RUN}$  when motor is at 50% speed. When motor is operating at other speeds, MCF8329HS-Q1 extrapolates  $I_{DRY\_RUN}$  as shown in [Figure 7-49](#).

#### Note

TI recommends subtracting 5-10% from expected  $I_q$  current for setting DRY\_RUN\_ILIM and DRY\_RUN\_ILIM\_FIFTY\_PERCENT\_SPEED to avoid false dry run faults (due to  $I_{DRY\_RUN}$  being set too high).



**Figure 7-49. Variable current threshold ( $I_{DRY\_RUN}$ ) for dry run detection**

## 7.4 Device Functional Modes

### 7.4.1 Functional Modes

#### 7.4.1.1 Sleep Mode

In sleep mode all gate drivers are disabled, the GVDD regulator is disabled, the AVDD regulator is disabled, the sense amplifier, and the I<sup>2</sup>C bus are disabled. The device can be configured to enter sleep (instead of standby) mode by configuring DEV\_MODE to 1b. The entry and exit from sleep state as described in [Table 7-7](#).

**Table 7-7. Conditions to Enter or Exit Sleep Modes**

INPUT REFERENCE COMMAND MODE	ENTER SLEEP, DEV_MODE = 1b	EXIT FROM SLEEP	ENTER STANDBY, DEV_MODE = 0b	EXIT FROM STANDBY
Analog input at SPEED/WAKE pin	$V_{SPEED/WAKE} < V_{EN\_SL}$ for $t_{DET\_SL\_ANA}$ if $SLEEP\_ENTRY\_TIME = 00b$ or $01b$ ; for $t_{DET\_SL\_PWM}$ if $SLEEP\_ENTRY\_TIME = 10b$ or $11b$	$V_{SPEED/WAKE} > V_{EX\_SL}$	$V_{SPEED/WAKE} < V_{EN\_SB}$	$V_{SPEED/WAKE} > V_{EX\_SB}$
PWM	$V_{SPEED/WAKE} < V_{IL}$ for $t_{DET\_SL\_PWM}$	$V_{SPEED/WAKE} > V_{IH}$ for $t_{DET\_PWM}$	$Duty_{SPEED/WAKE} < Duty_{EN\_SB}$ for $t_{DET\_SL\_PWM}$	$Duty_{SPEED/WAKE} > Duty_{EX\_SB}$ for $t_{DET\_PWM}$
Frequency	$V_{SPEED/WAKE} < V_{IL}$ for $t_{DET\_SL\_PWM}$	$V_{SPEED/WAKE} > V_{IH}$ for $t_{DET\_PWM}$	$Freq_{SPEED/WAKE} < Freq_{EN\_SB}$ for $t_{DET\_SL\_PWM}$	$Freq_{SPEED/WAKE} > Freq_{EX\_SB}$ for $t_{DET\_PWM}$
I <sup>2</sup> C	$V_{SPEED/WAKE} < V_{IL}$ and $DIGITAL\_SPEED\_CTRL = 0h$ for $t_{DET\_SL\_PWM}$	$V_{SPEED/WAKE} > V_{IH}$	$DIGITAL\_SPEED\_CTRL < DIGITAL\_SPEED\_CTRL_{E\_N\_SB}$	$DIGITAL\_SPEED\_CTRL > DIGITAL\_SPEED\_CTRL_{EX\_SB}$

#### Note

During power-up and power-down of the device, the nFAULT pin is held low as the internal regulators are disabled. After the regulators have been enabled, the nFAULT pin is automatically released.

#### 7.4.1.2 Standby Mode

In standby mode the gate driver, AVDD LDO and I<sup>2</sup>C bus are active. The device can be configured to enter standby mode by configuring DEV\_MODE to 0b. The device enters standby mode when the reference command after the profiler is zero.

The thresholds for entering and exiting standby mode in different input modes are as follows,

**Table 7-8. Standby Mode Entry/Exit Thresholds**

Control Input Source	Standby entry/exit thresholds	REF_PROFILE_CONFIG = 00b	REF_PROFILE_CONFIG ≠ 00b
Analog	$V_{EN\_SB}$ or $V_{EX\_SB}$	$V_{EX\_SB} = MIN\_DUTY \times V_{ANA\_FS}$ ; $V_{EN\_SB} = (MIN\_DUTY - DUTY\_HYS) \times V_{ANA\_FS}$	$REF\_X = 1\% \text{ of } MAX\_SPEED$ or $MAX\_POWER$ or $ILIMIT$ or $MODULATION\ INDEX$
PWM	$Duty_{EN\_SB}$ or $Duty_{EX\_SB}$	$Duty_{EX\_SB} = MIN\_DUTY$ ; $Duty_{EN\_SB} = MIN\_DUTY - DUTY\_HYS$	$REF\_X = 1\% \text{ of } MAX\_SPEED$ or $MAX\_POWER$ or $ILIMIT$ or $MODULATION\ INDEX$
I <sup>2</sup> C	$DIGITAL\_SPEED\_CTRL_{EN\_SB}$ or $DIGITAL\_SPEED\_CTRL_{EX\_SB}$	$DIGITAL\_SPEED\_CTRL_{EX\_SB} = MIN\_DUTY \times 32767$ ; $DIGITAL\_SPEED\_CTRL_{EN\_SB} = (MIN\_DUTY - DUTY\_HYS) \times 32767$	$REF\_X = 1\% \text{ of } MAX\_SPEED$ or $MAX\_POWER$ or $ILIMIT$ or $MODULATION\ INDEX$

**Table 7-8. Standby Mode Entry/Exit Thresholds (continued)**

Control Input Source	Standby entry/exit thresholds	REF_PROFILE_CONFIG = 00b	REF_PROFILE_CONFIG ≠ 00b
Frequency	Freq <sub>EN</sub> _SB or Freq <sub>EX</sub> _SB	Freq <sub>EX</sub> _SB = MIN_DUTY x INPUT_MAXIMUM_FREQ (subject to minimum of 3Hz); Freq <sub>EN</sub> _SB = (MIN_DUTY-DUTY_HYS) x INPUT_MAXIMUM_FREQ (subject to minimum of 3Hz)	REF_X = 1% of MAX_SPEED or MAX_POWER or ILIMIT or MODULATION INDEX

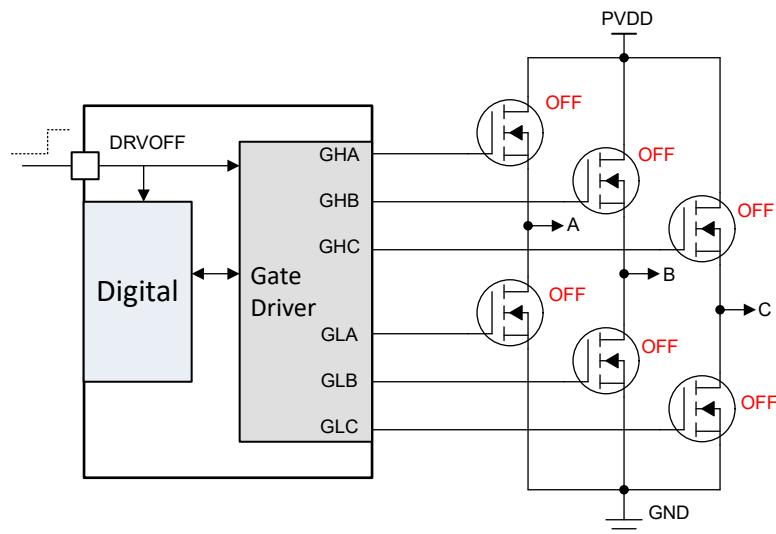
#### 7.4.1.3 Fault Reset (CLR\_FLT)

In the case of latched faults, the device goes into a partial shutdown state to help protect the power MOSFETs and system. When the fault condition clears, the device can go to the operating state again by setting the CLR\_FLT to 1b.

### 7.5 External Interface

#### 7.5.1 DRVOFF - Gate Driver Shutdown Functionality

When DRVOFF is driven high, the gate driver goes into shutdown. DRVOFF bypasses the digital control logic inside the device, and is connected directly to the gate driver output (see Figure 7-50). This pin provides a mechanism for externally monitored faults to disable gate driver by directly bypassing the internal control logic. When the MCF8329HS-Q1 detects logic high on the DRVOFF pin, the device disables the gate driver and puts the device into pull down mode (see Figure 7-51). The gate driver shutdown sequence proceeds as shown in Figure 7-51. When the gate driver initiates the shutdown sequence, the active driver pull down is applied at  $I_{SINK}$  current for the  $t_{SD\_SINK\_DIG}$  time, after which the gate driver moves to passive pull down mode.


**Figure 7-50. DRVOFF Gate Driver Output State**

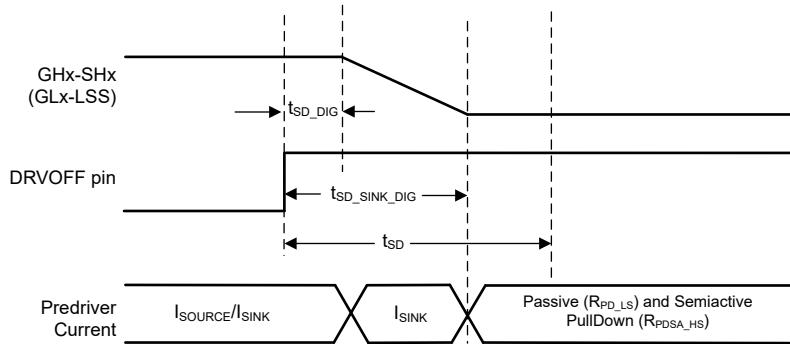


Figure 7-51. Gate Driver Shutdown Sequence

**Note**

Pulling the DRVOFF pin high does not cause the device to enter sleep or standby mode and the digital core is still active. The DRVOFF status is reported on DRV\_OFF bit and has a latency of up to 200ms between the pin status change to DRV\_OFF bit status update. The DRVOFF is not reported on nFAULT pin, however nFAULT pin can go low if a motor fault happens when DRVOFF goes to logic high during motor operation. When DRVOFF is pulled from high to low, MCF8329HS-Q1 execute motor start sequence (with a latency up to 200ms after pulling DRVOFF pin low) as described in [Section 7.3.9](#).

**7.5.2 Oscillator Source**

MCF8329HS-Q1 has a built-in oscillator that is used as the clock source for all digital peripherals and timing measurements. Default configuration for MCF8329HS-Q1 is to use the internal oscillator and it is sufficient to drive the motor without need for any external crystal or clock sources.

In order to improve EMI performance, MCF8329HS-Q1 provides the option of modulating the clock frequency by enabling Spread Spectrum Modulation (SSM) through SPREAD\_SPECTRUM\_MODULATION\_DIS.

**Note**

Spread spectrum modulation is not available (irrespective of SPREAD\_SPECTRUM\_MODULATION\_DIS) when CLOCK\_FREQUENCY is set to 00b (HIGH).

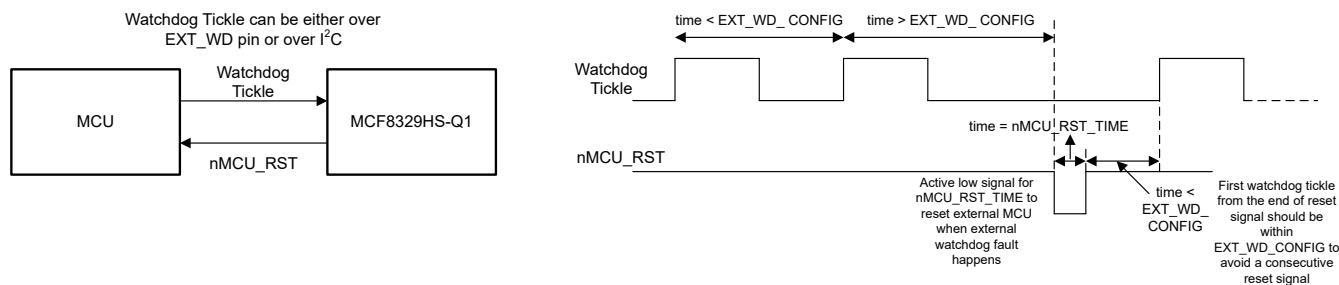
**7.5.3 External Watchdog with MCU Reset**

MCF8329HS-Q1 provides an external watchdog feature to monitor the health of an external MCU - EXT\_WD\_EN bit should be set to 1b to enable the external watchdog. When this feature is enabled, the device waits for a tickle (low to high transition in EXT\_WD pin or WATCHDOG\_TICKLE set to 1b over I<sup>2</sup>C) from the external watchdog input for a configured time interval; if the time interval between two consecutive tickles is longer than the configured watchdog wait time, a watchdog fault is triggered. The watchdog fault response can be configured using EXT\_WD\_FAULT\_MODE and LIMP\_HOME\_EN as shown in [Table 7-6](#). When LIMP\_HOME\_EN is set to 0b (limp home mode disabled), fault response is either report only (FETs active and driving motor at input reference) or latched (FETs in Hi-Z) depending on EXT\_WD\_FAULT\_MODE. The latched fault can be cleared by writing 1b to CLRFLT or by issuing a tickle on EXT\_WD pin or over I<sup>2</sup>C. When LIMP\_HOME\_EN is set to 1b (limp home mode enabled), fault response is either the input reference latched to current value or latched to REF\_OFF1 depending on EXT\_WD\_FAULT\_MODE - MCF8329HS-Q1 operates the motor at the latched input reference till 1b is written to CLRFLT or a tickle is issued on EXT\_WD pin or over I<sup>2</sup>C. Once the watchdog fault is cleared (by writing 1b to CLRFLT or by issuing a tickle on EXT\_WD pin or over I<sup>2</sup>C), MCF8329HS-Q1 exits the limp home mode and drives the motor to the input reference from the reference source configured by SPEED\_MODE (analog, PWM, I<sup>2</sup>C or frequency). When a watchdog timeout occurs, WATCHDOG\_FAULT bit is set to 1b. In case the next tickle arrives before the configured time interval elapses, the watchdog timer is reset and it begins to wait for the next tickle. This can be used to continuously

monitor the health of an external MCU (which is the external watchdog input) and place the MCF8329HS-Q1 in a known state, in case the external MCU is in a fault/hang state.

The external watchdog input is selected using `EXT_WD_INPUT_MODE` and can either be the `EXT_WD` pin or the  $I^2C$  interface. The time interval between two tickles to trigger a watchdog fault is configured by `EXT_WD_CONFIG`; there are 4 time settings - 100, 200, 500 and 1000ms for the `EXT_WD` pin based watchdog and 4 time settings - 1, 2, 5 and 10s for the  $I^2C$  based watchdog.

When a watchdog fault is triggered (irrespective of `EXT_WD_FAULT_MODE` and `LIMP_HOME_EN`), an active low signal is available on the `nMCU_RST` pin to reset the external MCU as shown in [Figure 7-52](#). The duration of this active low signal can be configured by `nMCU_RST_TIME` - 1ms or 10ms. MCF8329HS-Q1 waits for `EXT_WD_CONFIG` from the end of the active low signal duration before issuing another reset signal. During normal operation (no watchdog fault detected), `nMCU_RST` is pulled up to `AVDD` through an internal pull-up resistor.



**Figure 7-52. MCU Reset Signal on External Watchdog Fault**

#### Note

Watchdog should be disabled by setting `EXT_WD_EN` to 0b before changing `EXT_WD_CONFIG` configuration.

## 7.6 EEPROM access and I<sup>2</sup>C interface

### 7.6.1 EEPROM Access

MCF8329HS-Q1 has 1024 bits (16 rows of 64 bits each) of EEPROM, which are used to store the motor configuration parameters. Erase operations are row-wise (all 64 bits are erased in a single erase operation), but 32-bit write and read operations are supported. EEPROM can be written and read using the I<sup>2</sup>C serial interface but erase cannot be performed using I<sup>2</sup>C serial interface. The shadow/RAM registers corresponding to the EEPROM are located at addresses 0x000080-0x0000AE.

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#### Note

MCF8329HS-Q1 allows EEPROM write and read operations only when the motor is not spinning.

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#### 7.6.1.1 EEPROM Write

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#### Note

- EEPROM write should be issued only when device is in idle or fault state (motor not driven by device). PVDD should be  $\geq 6V$  throughout the EEPROM write process to ensure that all power rails (AVDD and DVDD) stay within datasheet specifications and EEPROM write is never interrupted due to any UVLO condition.
- TI does not recommend writing to EEPROM during every power-up/wake-up due to aging/write cycle limitations on number of EEPROM writes (20000 write cycles at  $T_J = 85^{\circ}\text{C}$ ). Repetitive register settings change can be done at shadow/RAM registers (0x000080-0x0000AE); only default configurations need to be written to EEPROM (at first power-up)

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In MCF8329HS-Q1, EEPROM write procedure is as follows,

1. Write register 0x000080 (ISD\_CONFIG) with ISD and reverse drive configuration like resync enable, reverse drive enable, stationary detect threshold, reverse drive handoff threshold etc.
2. Write register 0x000082 (REV\_DRIVE\_CONFIG) with reverse drive and active brake configuration like reverse drive open loop acceleration, active brake current limit, K<sub>p</sub>, K<sub>i</sub> values etc.
3. Write register 0x000084 (MOTOR\_STARTUP1) with motor start-up configuration like start-up method, IPD parameters, align parameters etc.
4. Write register 0x000086 (MOTOR\_STARTUP2) with motor start-up configuration like open loop acceleration, open loop current limit, first cycle frequency etc.
5. Write register 0x000088 (CLOSED\_LOOP1) with motor control configuration like closed loop acceleration, overmodulation enable, PWM frequency, FG signal configurations etc.
6. Write register 0x00008A (CLOSED\_LOOP2) with motor control configuration like motor winding resistance and inductance, motor stop options, brake speed threshold etc.
7. Write register 0x00008C (CLOSED\_LOOP3) with motor control configuration like motor BEMF constant, current loop K<sub>p</sub>, K<sub>i</sub> etc.
8. Write register 0x00008E (CLOSED\_LOOP4) with motor control configuration like speed loop K<sub>p</sub>, K<sub>i</sub> and maximum speed.
9. Write register 0x000090 (FAULT\_CONFIG1) with fault control configuration software and hardware current limits and actions, retry times etc.
10. Write register 0x000092 (FAULT\_CONFIG2) with fault control configuration like hardware current limit actions, OV, UV limits and actions, abnormal speed level, no motor threshold etc.
11. Write registers 0x000094 – 0x00009E (SPEED\_PROFILES1-6) with speed profile configuration like profile type, duty cycle, speed clamp level, duty cycle clamp level etc.
12. Write register 0x0000A0 (INT\_ALGO\_1) with miscellaneous configuration like ISD run time, stop time and timeout etc.
13. Write register 0x0000A2 (INT\_ALGO\_2) with miscellaneous configuration like flux weakening K<sub>p</sub>, K<sub>i</sub>, active brake current slew rate, closed loop slow acceleration etc.
14. Write registers 0x0000A4 (PIN\_CONFIG) with pin configuration for speed input mode (analog or PWM or Freq or I<sup>2</sup>C), Brake input, FG during idle and fault state config etc.

15. Write registers 0x0000A6 and 0x0000A8 (DEVICE\_CONFIG1 and DEVICE\_CONFIG2) with device configuration like device mode, dynamic voltage gain enable, I<sup>2</sup>C target address etc.
16. Write register 0x0000AA (PERI\_CONFIG1) with peripheral configuration like dead time, SSM enable etc.
17. Write registers 0x0000AC and 0x0000AE (GD\_CONFIG1 and GD\_CONFIG2) with gate driver configuration like slew rate, CSA gain, VDS level, mode etc.
18. Write 0x8A500000 into register 0x0000EA to write the shadow register(0x000080-0x0000AE) values into the EEPROM.
19. Wait for 750ms for the EEPROM write operation to complete.
20. After 750ms, read 0x0000EA register to ensure it has been reset to 0x0. This confirms that the EEPROM write process has been completed successfully.

Steps 1-17 can be selectively executed based on registers/parameters that need to be modified. After all shadow/RAM registers have been updated with the required values, steps 18-20 should be executed to write the contents of the shadow/RAM registers into the EEPROM.

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**Note**

EEPROM reserved bit field defaults settings must not be changed. To avoid changing the content of reserved bits, TI recommends using “read-modify-write” sequence to perform EEPROM write operation.

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#### 7.6.1.2 EEPROM Read

In MCF8329HS-Q1, EEPROM read procedure is as follows,

1. Write 0x40000000 into register 0x0000EA to read the EEPROM data into the shadow/RAM registers (0x000080-0x0000AE).
2. Wait for 100ms for the EEPROM read operation to complete.
3. Read the shadow/RAM register values, one or two registers at a time, using the I<sup>2</sup>C read command as explained in [Section 7.6.2](#). Shadow register addresses are in the range of 0x000080-0x0000AE. Register address increases in steps of 2 for 32-bit read operation (since each address is a 16-bit location).

#### 7.6.1.3 EEPROM Security

MCF8329HS-Q1 provides configurable read and write protection to EEPROM registers. The level of protection can be configured using EEPROM\_LOCK\_MODE as per following list,

- 00b : EEPROM read and write are allowed without a passcode
- 01b : EEPROM read and write need a valid passcode
- 10b : EEPROM read needs a valid passcode; EEPROM write is locked permanently
- 11b : EEPROM read and write are locked permanently

Passcode is a 15-bit field in the EEPROM denoted by EEPROM\_LOCK\_KEY in the DEVICE\_CONFIG1 register. EEPROM\_LOCK\_KEY is write accessible (when EEPROM\_LOCK\_MODE is set to 00b or 01b) but not read accessible.

When passcode based read/write protection is enabled (EEPROM\_LOCK\_MODE set to 01b or 10b), user has to write the passcode set in EEPROM\_LOCK\_KEY to USER\_EEPROM\_KEY bitfield after every power-up/wake-up before sending the first EEPROM read/write transaction over I<sup>2</sup>C. One valid passcode write after power-up/wake-up is sufficient for all subsequent EEPROM read/write transactions as long as there is no power reset, sleep mode entry, digital reset or incorrect passcode write. If an invalid passcode is written, the subsequent EEPROM read/write transactions are rejected - MCF8329HS-Q1 does not respond to the read/write requests. The read/write protection is applicable to EEPROM as well as the corresponding shadow/RAM locations. The EEPROM\_LOCK\_MODE as well as the passcode are part of the EEPROM registers and hence same level of read/write protection applies to these bit fields as configured by EEPROM\_LOCK\_MODE.

### 7.6.2 I<sup>2</sup>C Serial Interface

MCF8329HS-Q1 interfaces with an external MCU over an I<sup>2</sup>C serial interface. MCF8329HS-Q1 is an I<sup>2</sup>C target to be interfaced with a controller. External MCU can use this interface to read/write from/to any non-reserved register in MCF8329HS-Q1.

#### Note

For reliable communication, a 100- $\mu$ s delay should be used between every byte transferred over the I<sup>2</sup>C bus.

#### 7.6.2.1 I<sup>2</sup>C Data Word

The I<sup>2</sup>C data word format is shown in [Table 7-9](#).

**Table 7-9. I<sup>2</sup>C Data Word Format**

TARGET_ID	R/W	CONTROL WORD	DATA	CRC-8
A6 - A0	W0	CW23 - CW0	D15 / D31/ D63 - D0	C7 - C0

**Target ID and R/W Bit:** The first byte includes the 7-bit I<sup>2</sup>C target ID (0x01), followed by the read/write command bit. Every packet in MCF8329HS-Q1 the communication protocol starts with writing a 24-bit control word and hence the R/W bit is always 0.

**24-bit Control Word:** The Target Address is followed by a 24-bit control bit. The control word format is shown in [Table 7-10](#).

**Table 7-10. 24-bit Control Word Format**

OP_R/W	CRC_EN	DLEN	MEM_SEC	MEM_PAGE	MEM_ADDR
CW23	CW22	CW21- CW20	CW19 - CW16	CW15 - CW12	CW11 - CW0

Each field in the control word is explained in detail below.

**OP\_R/W – Read/Write:** R/W bit gives information on whether this is a read operation or write operation. Bit value 0 indicates it is a write operation. Bit value 1 indicates it is a read operation. For write operation, MCF8329HS-Q1 will expect data bytes to be sent after the 24-bit control word. For read operation, MCF8329HS-Q1 will expect an I<sup>2</sup>C read request with repeated start or normal start after the 24-bit control word.

**CRC\_EN – Cyclic Redundancy Check(CRC) Enable:** MCF8329HS-Q1 supports CRC to verify the data integrity. This bit controls whether the CRC feature is enabled or not.

**DLEN – Data Length:** DLEN field determines the length of the data that will be sent by external MCU to MCF8329HS-Q1. MCF8329HS-Q1 protocol supports three data lengths: 16-bit, 32-bit and 64-bit.

**Table 7-11. Data Length Configuration**

DLEN Value	Data Length
00b	16-bit
01b	32-bit
10b	64-bit
11b	Reserved

**MEM\_SEC – Memory Section:** Each memory location in MCF8329HS-Q1 is addressed using three separate entities in the control word – Memory Section, Memory Page, Memory Address. Memory Section is a 4-bit field which denotes the memory section to which the memory location belongs like RAM, ROM etc.

**MEM\_PAGE – Memory Page:** Memory page is a 4-bit field which denotes the memory page to which the memory location belongs.

**MEM\_ADDR – Memory Address:** Memory address is the last 12-bits of the address. The complete 22-bit address is constructed internally by MCF8329HS-Q1 using all three fields – Memory Section, Memory Page,

Memory Address. For memory locations 0x000000-0x000800, memory section is 0x0, memory page is 0x0 and memory address is the lowest 12 bits(0x000 for 0x000000, 0x080 for 0x000080 and 0x800 for 0x000800)

**Data Bytes:** For a write operation to MCF8329HS-Q1, the 24-bit control word is followed by data bytes. The DLEN field in the control word should correspond with the number of bytes sent in this section.

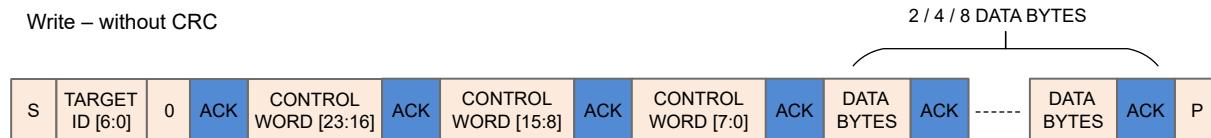
**CRC Byte:** If the CRC feature is enabled in the control word, CRC byte has to be sent at the end of a write transaction. Procedure to calculate CRC is explained in CRC Byte Calculation below.

### 7.6.2.2 I<sup>2</sup>C Write Operation

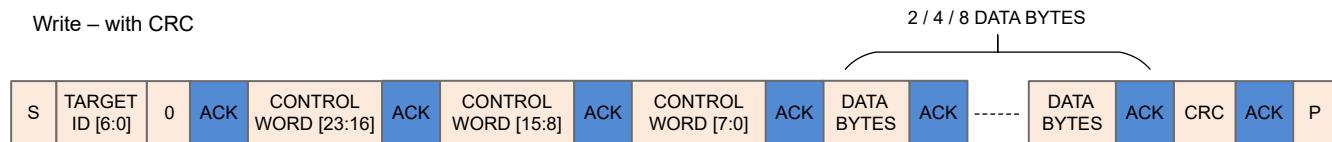
MCF8329HS-Q1 write operation over I<sup>2</sup>C involves the following sequence.

1. I<sup>2</sup>C start condition.
2. The sequence starts with I<sup>2</sup>C target start byte, made up of 7-bit target ID (0x01) to identify the MCF8329HS-Q1 along with the R/W bit set to 0.
3. The start byte is followed by 24-bit control word. Bit 23 in the control word has to be 0 as it is a write operation.
4. The 24-bit control word is then followed by the data bytes. The length of the data byte depends on the DLEN field.
  - a. While sending data bytes, the LSB byte is sent first. Refer below examples for more details.
  - b. 16-bit/32-bit write – The data sent is written to the address mentioned in Control Word.
  - c. 64-bit Write – 64-bit is treated as two 32-bit writes. The address mentioned in Control word is taken as Addr 0. Addr 1 is calculating internally by MCF8329HS-Q1 by incrementing Addr 0 by 2. A total of 8 data bytes are sent. The first 4 bytes (sent in LSB first way) are written to Addr 0 and the next 4 bytes are written to Addr 1.
5. If CRC is enabled, the packet ends with a CRC byte. CRC is calculated for the entire packet (Target ID + W bit, Control Word, Data Bytes).
6. I<sup>2</sup>C stop condition.

Write – without CRC



Write – with CRC



CRC includes {TARGET ID,0}, CONTROL WORD[23:0], DATA BYTES

**Figure 7-53. I<sup>2</sup>C Write Operation Sequence**

### 7.6.2.3 I<sup>2</sup>C Read Operation

MCF8329HS-Q1 read operation over I<sup>2</sup>C involves the following sequence.

1. I<sup>2</sup>C start condition.
2. The sequence starts with I<sup>2</sup>C target Start Byte.
3. The Start Byte is followed by 24-bit Control Word. Bit 23 in the control word has to be 1 as it is a read operation.
4. The control word is followed by a repeated start or normal start.
5. MCF8329HS-Q1 sends the data bytes on SDA. The number of bytes sent by MCF8329HS-Q1 depends on the DLEN field value in the control word.
  - a. While sending data bytes, the LSB byte is sent first. Refer the examples below for more details.

- b. 16-bit/32-bit Read – The data from the address mentioned in Control Word is sent back.
- c. 64-bit Read – 64-bit is treated as two 32-bit read. The address mentioned in Control Word is taken as Addr 0. Addr 1 is calculating internally by MCF8329HS-Q1 by incrementing Addr 0 by 2. A total of 8 data bytes are sent by MCF8329HS-Q1. The first 4 bytes (sent in LSB first way) are read from Addr 0 and the next 4 bytes are read from Addr 1.
- d. MCF8329HS-Q1 takes some time to process the control word and read data from the given address. This involves some delay. It is quite possible that the repeated start with Target ID will be NACK'd. If the I<sup>2</sup>C read request has been NACK'd by MCF8329HS-Q1, retry after few cycles. During this retry, it is not necessary to send the entire packet along with the control word. It is sufficient to send only the start condition with target ID and read bit.

6. If CRC is enabled, then MCF8329HS-Q1 sends an additional CRC byte at the end. If CRC is enabled, external MCU I<sup>2</sup>C controller has to read this additional byte before sending the stop bit. CRC is calculated for the entire packet (Target ID + W bit, Control Word, Target ID + R bit, Data Bytes).

7. I<sup>2</sup>C stop condition.

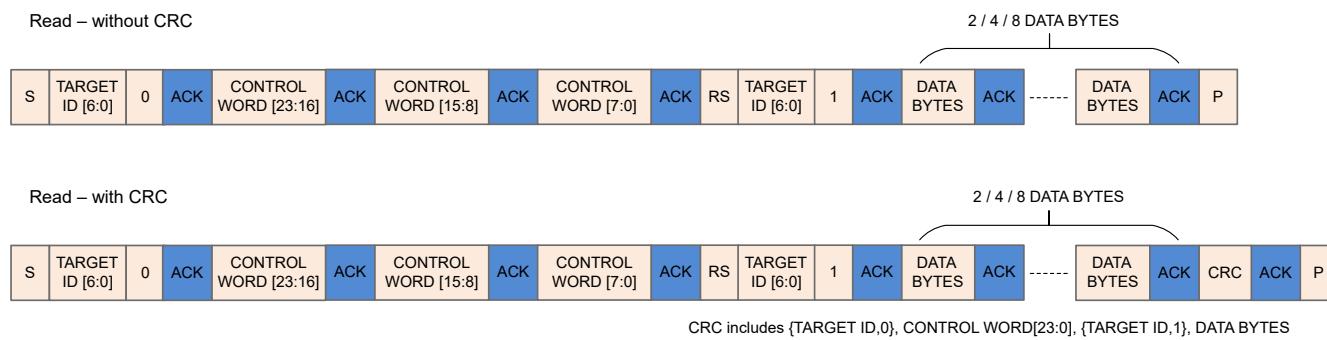


Figure 7-54. I<sup>2</sup>C Read Operation Sequence

#### 7.6.2.4 Examples of I<sup>2</sup>C Communication Protocol Packets

All values used in this example section are in hex format. I<sup>2</sup>C target ID used in the examples is 0x01.

**Example for 32-bit Write Operation:** Address – 0x00000080, Data – 0x1234ABCD, CRC Byte – 0x45 (Sample value; does not match with the actual CRC calculation)

Table 7-12. Example for 32-bit Write Operation Packet

Start Byte		Control Word 0				Control Word 1		Control Word 2		Data Bytes				CRC
Target ID	I <sup>2</sup> C Write	OP_R/W	CRC_E_N	DLEN	MEM_SEC	MEM_PAGE	MEM_DDR	MEM_ADDR	DB0	DB1	DB2	DB3	CRC Byte	
A6-A0	W0	CW23	CW22	CW21-CW20	CW19-CW16	CW15-CW12	CW11-CW8	CW7-CW0	D7-D0	D7-D0	D7-D0	D7-D0	C7-C0	
0x01	0x0	0x0	0x1	0x1	0x0	0x0	0x0	0x80	0xCD	0xAB	0x34	0x12	0x45	
0x02		0x50				0x00		0x80	0xCD	0xAB	0x34	0x12	0x45	

**Example for 64-bit Write Operation:** Address - 0x00000080, Data Address 0x00000080 - Data 0x01234567, Data Address 0x00000082 – Data 0x89ABCDEF, CRC Byte – 0x45 (Sample value; does not match with the actual CRC calculation)

Table 7-13. Example for 64-bit Write Operation Packet

Start Byte		Control Word 0				Control Word 1		Control Word 2		Data Bytes				CRC
Target ID	I <sup>2</sup> C Write	OP_R/W	CRC_EN	DLEN	MEM_SEC	MEM_PAGE	MEM_ADDR	MEM_ADDR	DB0 - DB7					CRC Byte
A6-A0	W0	CW23	CW22	CW21-CW20	CW19-CW16	CW15-CW12	CW11-CW8	CW7-CW0	[D7-D0] x 8					C7-C0

**Table 7-13. Example for 64-bit Write Operation Packet (continued)**

0x01	0x0	0x0	0x1	0x2	0x0	0x0	0x0	0x80	0x67452301EFCDAB89	0x45
0x02		0x60			0x00			0x80	0x67452301EFCDAB89	0x45

**Example for 32-bit Read Operation:** Address – 0x00000080, Data – 0x1234ABCD, CRC Byte – 0x56 (Sample value; does not match with the actual CRC calculation)

**Table 7-14. Example for 32-bit Read Operation Packet**

Start Byte		Control Word 0					Control Word 1		Control Word 2	Start Byte		Byte 0	Byte 1	Byte 2	Byte 3	Byte 4
Target ID	I <sup>2</sup> C Write	R/W	CRC_EN	DLEN	MEM_SEC	MEM_PAGE	MEM_ADDR	MEM_ADDR	Target ID	I <sup>2</sup> C Read	DB0	DB1	DB2	DB3	CRC Byte	
A6-A0	W0	CW23	CW22	CW21-CW20	CW19-CW16	CW15-CW12	CW11-CW8	CW7-CW0	A6-A0	W0	D7-D0	D7-D0	D7-D0	D7-D0	C7-C0	
0x01	0x0	0x1	0x1	0x1	0x0	0x0	0x0	0x80	0x01	0x1	0xCD	0xAB	0x34	0x12	0x56	
0x02		0xD0			0x00		0x80	0x03			0xCD	0xAB	0x34	0x12	0x56	

#### 7.6.2.5 Internal Buffers

MCF8329HS-Q1 uses buffers internally to store the data received on I<sup>2</sup>C. Highest priority is given to collecting data on the I<sup>2</sup>C Bus. There are 2 buffers (ping-pong) for I<sup>2</sup>C Rx Data and 2 buffers (ping-pong) for I<sup>2</sup>C Tx Data.

A write request from external MCU is stored in Rx Buffer 1 and then the parsing block is triggered to work on this data in Rx Buffer 1. While MCF8329HS-Q1 is processing a write packet from Rx Buffer 1, if there is another new read/write request, the entire data from the I<sup>2</sup>C bus is stored in Rx Buffer 2 and it will be processed after the current request.

MCF8329HS-Q1 can accommodate a maximum of two consecutive read/write requests. If MCF8329HS-Q1 is busy due to high priority interrupts, the data sent will be stored in internal buffers (Rx Buffer 1 and Rx Buffer 2). At this point, if there is a third read/write request, the Target ID will be NACK'd as the buffers are already full.

During read operations, the read request is processed and the read data from the register is stored in the Tx Buffer along with the CRC byte, if enabled. Now if the external MCU initiates an I<sup>2</sup>C Read (Target ID + R bit), the data from this Tx Buffer is sent over I<sup>2</sup>C. Since there are two Tx Buffers, register data from 2 MCF8329HS-Q1 reads can be buffered. Given this scenario, if there is a third read request, the control word will be stored in the Rx Buffer 1, but it will not be processed by MCF8329HS-Q1 as the Tx Buffers are full.

Once a data is read from Tx Buffer, the data is no longer stored in the Tx buffer. The buffer is cleared and it becomes available for the next data to be stored. If the read transaction was interrupted in between and if the MCU had not read all the bytes, external MCU can initiate another I<sup>2</sup>C read (only I<sup>2</sup>C read, without any control word information) to read all the data bytes from first.

#### 7.6.2.6 CRC Byte Calculation

An 8-bit CCIT polynomial ( $x^8 + x^2 + x + 1$ ) is used for CRC computation.

**CRC Calculation in Write Operation:** When the external MCU writes to MCF8329HS-Q1, if the CRC is enabled, the external MCU has to compute an 8-bit CRC byte and add the CRC byte at the end of the data. MCF8329HS-Q1 computes CRC using the same polynomial internally and if there is a mismatch, the write request is discarded. Input data for CRC calculation by external MCU for write operation are listed below:

1. Target ID + write bit.
2. Control word – 3 bytes
3. Data bytes – 2/4/8 bytes

**CRC Calculation in Read Operation:** When the external MCU reads from MCF8329HS-Q1, if the CRC is enabled, MCF8329HS-Q1 sends the CRC byte at the end of the data. The CRC computation in read operation involves the start byte, control words sent by external MCU along with data bytes sent by MCF8329HS-Q1. Input data for CRC calculation by external MCU to verify the data sent by MCF8329HS-Q1 are listed below :

1. Target ID + write bit
2. Control word – 3 bytes
3. Target ID + read bit
4. Data bytes – 2/4/8 bytes

## 8 EEPROM (Non-Volatile) Register Map

## 8.1 Algorithm\_Configuration Registers

Table 8-1 lists the memory-mapped registers for the Algorithm\_Configuration registers. All register offset addresses not listed in Table 8-1 should be considered as reserved locations and the register contents should not be modified.

Table 8-1. ALGORITHM\_CONFIGURATION Registers

Offset	Acronym	Register Name	Section
80h	ISD_CONFIG	ISD Configuration	Section 8.1.1
82h	REV_DRIVE_CONFIG	Reverse Drive Configuration	Section 8.1.2
84h	MOTOR_STARTUP1	Motor Startup Configuration1	Section 8.1.3
86h	MOTOR_STARTUP2	Motor Startup Configuration2	Section 8.1.4
88h	CLOSED_LOOP1	Close Loop Configuration1	Section 8.1.5
8Ah	CLOSED_LOOP2	Close Loop Configuration2	Section 8.1.6
8Ch	CLOSED_LOOP3	Close Loop Configuration3	Section 8.1.7
8Eh	CLOSED_LOOP4	Close Loop Configuration4	Section 8.1.8
94h	REF_PROFILES1	Reference Profile Configuration1	Section 8.1.9
96h	REF_PROFILES2	Reference Profile Configuration2	Section 8.1.10
98h	REF_PROFILES3	Reference Profile Configuration3	Section 8.1.11
9Ah	REF_PROFILES4	Reference Profile Configuration4	Section 8.1.12
9Ch	REF_PROFILES5	Reference Profile Configuration5	Section 8.1.13
9Eh	REF_PROFILES6	Reference Profile Configuration6	Section 8.1.14

Complex bit access types are encoded to fit into small table cells. Table 8-2 shows the codes that are used for access types in this section.

Table 8-2. Algorithm\_Configuration Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

### 8.1.1 ISD\_CONFIG Register (Offset = 80h) [Reset = 00000000h]

ISD\_CONFIG is shown in Figure 8-1 and described in Table 8-3.

Return to the [Summary Table](#).

Register to configure initial speed detect settings

Figure 8-1. ISD\_CONFIG Register

31	30	29	28	27	26	25	24
PARITY	ISD_EN	BRAKE_EN	HIZ_EN	RVS_DR_EN	RESYNC_EN	FW_DRV_RESYN_THR	
R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	
23	22	21	20	19	18	17	16
FW_DRV_RESYN_THR	ISD_BEMF_FILT_ENABLE		SINGLE_SHUNT_BLANKING_TIME		BRK_TIME		

**Figure 8-1. ISD\_CONFIG Register (continued)**

R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12
BRK_TIME		HIZ_TIME	
R/W-0h			R/W-0h
7	6	5	4
STAT_DETECT_THR	REV_DRV_HANDOFF_THR		REV_DRV_OPEN_LOOP_CURRENT
R/W-0h	R/W-0h		R/W-0h

**Table 8-3. ISD\_CONFIG Register Field Descriptions**

Bit	Field	Type	Reset	Description
31	PARITY	R	0h	Parity bit
30	ISD_EN	R/W	0h	ISD enable during MSS 0h = Disable 1h = Enable
29	BRAKE_EN	R/W	0h	Brake enable during MSS 0h = Disable 1h = Enable
28	HIZ_EN	R/W	0h	Hi-Z enable during MSS 0h = Disable 1h = Enable
27	RVS_DR_EN	R/W	0h	Reverse drive operation enable during MSS 0h = Disable 1h = Enable
26	RESYNC_EN	R/W	0h	Resynchronization enable during MSS 0h = Disable 1h = Enable
25-22	FW_DRV_RESYN_THR	R/W	0h	Minimum speed threshold for resynchronize to closed loop (% of MAX_SPEED) 0h = 5% 1h = 10% 2h = 15% 3h = 20% 4h = 25% 5h = 30% 6h = 35% 7h = 40% 8h = 45% 9h = 50% Ah = Not Applicable Bh = Not Applicable Ch = Not Applicable Dh = Not Applicable Eh = Not Applicable Fh = Not Applicable
21	ISD_BEMF_filt_ENABLE	R/W	0h	BEMF filter enable during ISD 0h = Disable 1h = Enable

Table 8-3. ISD\_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20-17	SINGLE_SHUNT_BLANKING_TIME	R/W	0h	Blanking time before current sampling from the PWM edge 0h = 0.25 $\mu$ s 1h = 0.5 $\mu$ s 2h = 0.75 $\mu$ s 3h = 1 $\mu$ s 4h = 1.25 $\mu$ s 5h = 1.5 $\mu$ s 6h = 1.75 $\mu$ s 7h = 2 $\mu$ s 8h = 2.25 $\mu$ s 9h = 2.5 $\mu$ s Ah = 2.75 $\mu$ s Bh = 3 $\mu$ s Ch = 3.5 $\mu$ s Dh = 4 $\mu$ s Eh = 5 $\mu$ s Fh = 6 $\mu$ s
16-13	BRK_TIME	R/W	0h	Brake time during MSS 0h = 10 ms 1h = 50 ms 2h = 100 ms 3h = 200 ms 4h = 300 ms 5h = 400 ms 6h = 500 ms 7h = 750 ms 8h = 1 s 9h = 2 s Ah = 3 s Bh = 4 s Ch = 5 s Dh = 7.5 s Eh = 10 s Fh = 15 s
12-9	HIZ_TIME	R/W	0h	Hi-Z time during MSS 0h = 10 ms 1h = 50 ms 2h = 100 ms 3h = 200 ms 4h = 300 ms 5h = 400 ms 6h = 500 ms 7h = 750 ms 8h = 1 s 9h = 2 s Ah = 3 s Bh = 4 s Ch = 5 s Dh = 7.5 s Eh = 10 s Fh = 15 s
8-6	STAT_DETECT_THR	R/W	0h	BEMF threshold to detect if motor is stationary 0h = 100 mV 1h = 150 mV 2h = 200 mV 3h = 500 mV 4h = 1000 mV 5h = 1500 mV 6h = 2000 mV 7h = 3000 mV

**Table 8-3. ISD\_CONFIG Register Field Descriptions (continued)**

Bit	Field	Type	Reset	Description
5-3	REV_DRV_HANDOFF_T HR	R/W	0h	Speed threshold for transitioning to open-loop during reverse drive (% of MAX_SPEED) 0h = 5% 1h = 10% 2h = 15% 3h = 20% 4h = 25% 5h = 30% 6h = 40% 7h = 50%
2-0	REV_DRV_OPEN_LOOP _CURRENT	R/W	0h	Open loop current limit during reverse drive (% of BASE_CURRENT) 0h = 5% 1h = 10% 2h = 15% 3h = 20% 4h = 25% 5h = 30% 6h = 40% 7h = 50%

### 8.1.2 REV\_DRIVE\_CONFIG Register (Offset = 82h) [Reset = 00000000h]

REV\_DRIVE\_CONFIG is shown in [Figure 8-2](#) and described in [Table 8-4](#).

[Return to the Summary Table.](#)

Register to configure reverse drive settings

**Figure 8-2. REV\_DRIVE\_CONFIG Register**

31	30	29	28	27	26	25	24
PARITY		REV_DRV_OPEN_LOOP_ACCEL_A1		BUS_CURRENT_LIMIT_EN_MIN_VOLTAGE			
R-0h		R/W-0h			R/W-0h		
23	22	21	20	19	18	17	16
BUS_CURRENT_LIMIT_EN_MIN_VOLTAGE		ACTIVE_BRAKE_CURRENT_LIMIT			ACTIVE_BRAKE_KP		
R/W-0h		R/W-0h			R/W-0h		
15	14	13	12	11	10	9	8
		ACTIVE_BRAKE_KP			ACTIVE_BRAKE_KI		
		R/W-0h			R/W-0h		
7	6	5	4	3	2	1	0
		ACTIVE_BRAKE_KI			R/W-0h		

**Table 8-4. REV\_DRIVE\_CONFIG Register Field Descriptions**

Bit	Field	Type	Reset	Description
31	PARITY	R	0h	Parity bit

Table 8-4. REV\_DRIVE\_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
30-27	REV_DRV_OPEN_LOOP _ACCEL_A1	R/W	0h	Open loop acceleration coefficient A1 during reverse drive 0h = 0.1 Hz/s 1h = 0.5 Hz/s 2h = 1 Hz/s 3h = 2.5 Hz/s 4h = 5 Hz/s 5h = 10 Hz/s 6h = 25 Hz/s 7h = 50 Hz/s 8h = 75 Hz/s 9h = 100 Hz/s Ah = 250 Hz/s Bh = 500 Hz/s Ch = 750 Hz/s Dh = 1000 Hz/s Eh = 5000 Hz/s Fh = 10000 Hz/s
26-23	BUS_CURRENT_LIMIT_E N_MIN_VOLTAGE	R/W	0h	Minimum PVDD voltage below which bus current limit is enabled (Applicable only if CTRL_MODE = 1h or BUS_POWER_LIMIT_ENABLE = 1) 0h = Bus current Limit is disabled 1h = 9 V 2h = 10 V 3h = 11 V 4h = 12 V 5h = 18 V 6h = 20 V 7h = 22 V 8h = 24 V 9h = 30 V Ah = 32 V Bh = 34 V Ch = 36 V Dh = 40 V Eh = 44 V Fh = 48 V
22-20	ACTIVE_BRAKE_CURRE NT_LIMIT	R/W	0h	Bus current limit during active braking (% of BASE_CURRENT) 0h = 10% 1h = 20% 2h = 30% 3h = 40% 4h = 50% 5h = 60% 6h = 70% 7h = 80%
19-10	ACTIVE_BRAKE_KP	R/W	0h	10-bit value for active braking PI loop Kp. Kp = ACTIVE_BRAKE_KP / 2 <sup>7</sup>
9-0	ACTIVE_BRAKE_KI	R/W	0h	10-bit value for active braking PI loop Ki. Ki = ACTIVE_BRAKE_KI / 2 <sup>9</sup>

### 8.1.3 MOTOR\_STARTUP1 Register (Offset = 84h) [Reset = 00000000h]

MOTOR\_STARTUP1 is shown in Figure 8-3 and described in Table 8-5.

Return to the [Summary Table](#).

Register to configure motor startup settings1

Figure 8-3. MOTOR\_STARTUP1 Register

31	30	29	28	27	26	25	24
PARITY	MTR_STARTUP			ALIGN_SLOW_RAMP_RATE		ALIGN_TIME	

**Figure 8-3. MOTOR\_STARTUP1 Register (continued)**

R-0h	R/W-0h				R/W-0h				R/W-0h
23	22	21	20	19	18	17	16		
ALIGN_TIME		ALIGN_OR_SLOW_CURRENT_ILIMIT				RESERVED			
R/W-0h				R/W-0h				R-0h	
15	14	13	12	11	10	9	8		
RESERVED		IPD_CURR_THR				RESERVED			
R-0h				R/W-0h				R-0h	
7	6	5	4	3	2	1	0		
IPD_ADV_ANGLE	IPD_REPEAT		RESERVED		IQ_RAMP_DO_WN_EN	ACTIVE_BRAKE_EN	RESERVED		
R/W-0h		R/W-0h		R-0h	R/W-0h		R/W-0h	R-0h	

**Table 8-5. MOTOR\_STARTUP1 Register Field Descriptions**

Bit	Field	Type	Reset	Description
31	PARITY	R	0h	Parity bit
30-29	MTR_STARTUP	R/W	0h	Motor startup mode 0h = Align 1h = Double Align 2h = IPD 3h = Slow first cycle
28-25	ALIGN_SLOW_RAMP RATE	R/W	0h	Align, slow first cycle and open loop current ramp rate 0h = 1 A/s 1h = 5 A/s 2h = 10 A/s 3h = 25 A/s 4h = 50 A/s 5h = 100 A/s 6h = 150 A/s 7h = 250 A/s 8h = 500 A/s 9h = 1000 A/s Ah = 2000 A/s Bh = 5000 A/s Ch = 10000 A/s Dh = 20000 A/s Eh = 50000 A/s Fh = No Limit A/s
24-21	ALIGN_TIME	R/W	0h	Align time 0h = 10 ms 1h = 50 ms 2h = 100 ms 3h = 200 ms 4h = 300 ms 5h = 400 ms 6h = 500 ms 7h = 750 ms 8h = 1 s 9h = 1.5 s Ah = 2 s Bh = 3 s Ch = 4 s Dh = 5 s Eh = 7.5 s Fh = 10 s

**Table 8-5. MOTOR\_STARTUP1 Register Field Descriptions (continued)**

Bit	Field	Type	Reset	Description
20-17	ALIGN_OR_SLOW_CUR RENT_ILIMIT	R/W	0h	Align or slow first cycle current limit (% of BASE_CURRENT) 0h = 5% 1h = 10% 2h = 15% 3h = 20% 4h = 25% 5h = 30% 6h = 40% 7h = 45% 8h = 50% 9h = 55% Ah = 60% Bh = 65% Ch = 70% Dh = 75% Eh = 80% Fh = 85%
16-14	RESERVED	R	0h	Reserved
13-10	IPD_CURR_THR	R/W	0h	IPD current threshold (% of BASE_CURRENT) 0h = Not Applicable 1h = Not Applicable 2h = Not Applicable 3h = 20% 4h = 26.7% 5h = 33.3% 6h = 40% 7h = 46.7% 8h = 53.3% 9h = 60% Ah = 66.7% Bh = 73.3% Ch = 80% Dh = 86.7% Eh = 93.3% Fh = 100%
9-8	RESERVED	R	0h	Reserved
7-6	IPD_ADV_ANGLE	R/W	0h	IPD advance angle 0h = 0° 1h = 30° 2h = 60° 3h = 90°
5-4	IPD_REPEAT	R/W	0h	Number of times IPD is executed 0h = 1 time 1h = average of 2 times 2h = average of 3 times 3h = average of 4 times
3	RESERVED	R	0h	Reserved
2	IQ_RAMP_DOWN_EN	R/W	0h	Q-axis current ramp-down enable during open-loop to closed-loop transition 0h = Disable 1h = Enable
1	ACTIVE_BRAKE_EN	R/W	0h	Active braking enable during deceleration 0h = Disable 1h = Enable
0	RESERVED	R	0h	Reserved

#### 8.1.4 MOTOR\_STARTUP2 Register (Offset = 86h) [Reset = 00000000h]

MOTOR\_STARTUP2 is shown in [Figure 8-4](#) and described in [Table 8-6](#).

Return to the [Summary Table](#).

Register to configure motor startup settings2

**Figure 8-4. MOTOR\_STARTUP2 Register**

31	30	29	28	27	26	25	24
PARITY	OL_ILIMIT				OL_ACC_A1		
R-0h	R/W-0h				R/W-0h		
23	22	21	20	19	18	17	16
OL_ACC_A1	OL_ACC_A2				AUTO_HANDOFF_EN	OPN_CL_HANDOFF_THR	
R/W-0h	R/W-0h				R/W-0h	R/W-0h	
15	14	13	12	11	10	9	8
OPN_CL_HANDOFF_THR			STANDBY_POWER			AUTO_HANDOFF_MIN_BEMF	
R/W-0h			R/W-0h			R/W-0h	
7	6	5	4	3	2	1	0
SLOW_FIRST_CYC_FREQ				RESERVED	THETA_ERROR_RAMP_RATE		
R/W-0h				R-0h	R/W-0h		

**Table 8-6. MOTOR\_STARTUP2 Register Field Descriptions**

Bit	Field	Type	Reset	Description
31	PARITY	R	0h	Parity bit
30-27	OL_ILIMIT	R/W	0h	Open-loop current limit (% of BASE_CURRENT) 0h = 5% 1h = 10% 2h = 15% 3h = 20% 4h = 25% 5h = 30% 6h = 40% 7h = 45% 8h = 50% 9h = 55% Ah = 60% Bh = 65% Ch = 70% Dh = 75% Eh = 80% Fh = 85%
26-23	OL_ACC_A1	R/W	0h	Open loop acceleration coefficient A1 0h = 0.1 Hz/s 1h = 0.5 Hz/s 2h = 1 Hz/s 3h = 2.5 Hz/s 4h = 5 Hz/s 5h = 10 Hz/s 6h = 25 Hz/s 7h = 50 Hz/s 8h = 75 Hz/s 9h = 100 Hz/s Ah = 250 Hz/s Bh = 500 Hz/s Ch = 750 Hz/s Dh = 1000 Hz/s Eh = 5000 Hz/s Fh = 10000 Hz/s

Table 8-6. MOTOR\_STARTUP2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
22-19	OL_ACC_A2	R/W	0h	Open loop acceleration coefficient A2 0h = 0 Hz/s <sup>2</sup> 1h = 0.5 Hz/s <sup>2</sup> 2h = 1 Hz/s <sup>2</sup> 3h = 2.5 Hz/s <sup>2</sup> 4h = 5 Hz/s <sup>2</sup> 5h = 10 Hz/s <sup>2</sup> 6h = 25 Hz/s <sup>2</sup> 7h = 50 Hz/s <sup>2</sup> 8h = 75 Hz/s <sup>2</sup> 9h = 100 Hz/s <sup>2</sup> Ah = 250 Hz/s <sup>2</sup> Bh = 500 Hz/s <sup>2</sup> Ch = 750 Hz/s <sup>2</sup> Dh = 1000 Hz/s <sup>2</sup> Eh = 5000 Hz/s <sup>2</sup> Fh = 10000 Hz/s <sup>2</sup>
18	AUTO_HANDOFF_EN	R/W	0h	Auto handoff enable for open loop to closed loop transition 0h = Disable 1h = Enable
17-13	OPN_CL_HANDOFF_TH_R	R/W	0h	Open-loop to closed-loop handoff threshold (% of MAX_SPEED) 0h = 1% 1h = 2% 2h = 3% 3h = 4% 4h = 5% 5h = 6% 6h = 7% 7h = 8% 8h = 9% 9h = 10% Ah = 11% Bh = 12% Ch = 13% Dh = 14% Eh = 15% Fh = 16% 10h = 17% 11h = 18% 12h = 19% 13h = 20% 14h = 22.5% 15h = 25% 16h = 27.5% 17h = 30% 18h = 32.5% 19h = 35% 1Ah = 37.5% 1Bh = 40% 1Ch = 42.5% 1Dh = 45% 1Eh = 47.5% 1Fh = 50%
12-11	STANDBY_POWER	R/W	0h	Standby board power consumption (when motor is not driven) 0h = 0.5 W 1h = 1 W 2h = 2 W 3h = 4 W

**Table 8-6. MOTOR\_STARTUP2 Register Field Descriptions (continued)**

Bit	Field	Type	Reset	Description
10-8	AUTO_HANDOFF_MIN_B EMF	R/W	0h	Minimum BEMF threshold required for auto handoff 0h = 0 mV 1h = 100 mV 2h = 200 mV 3h = 500 mV 4h = 1000 mV 5h = 2000 mV 6h = 2500 mV 7h = 3000 mV
7-4	SLOW_FIRST_CYC_FRE Q	R/W	0h	First cycle frequency in slow first cycle startup (% of MAX_SPEED) 0h = 0.1% 1h = 0.3% 2h = 0.5% 3h = 0.7% 4h = 1% 5h = 1.5% 6h = 2% 7h = 2.5% 8h = 3% 9h = 4% Ah = 5% Bh = 7.5% Ch = 10% Dh = 15% Eh = 20% Fh = 25%
3	RESERVED	R	0h	Reserved
2-0	THETA_ERROR_RAMP_ RATE	R/W	0h	Ramp rate for reducing difference between estimated angle and open loop angle during open loop to closed loop transition 0h = 0.01 deg/ms 1h = 0.05 deg/ms 2h = 0.1 deg/ms 3h = 0.2 deg/ms 4h = 0.5 deg/ms 5h = 1 deg/ms 6h = 2 deg/ms 7h = 4 deg/ms

### 8.1.5 CLOSED\_LOOP1 Register (Offset = 88h) [Reset = 00000000h]

CLOSED\_LOOP1 is shown in [Figure 8-5](#) and described in [Table 8-7](#).

Return to the [Summary Table](#).

Register to configure close loop settings1

**Figure 8-5. CLOSED\_LOOP1 Register**

31	30	29	28	27	26	25	24
PARITY	OVERMODULA TION_ENABLE			CL_ACC		RESERVED	
R-0h	R/W-0h			R/W-0h		R-0h	
23	22	21	20	19	18	17	16
		CL_DEC			PWM_FREQ_OUT		
		R/W-0h			R/W-0h		
15	14	13	12	11	10	9	8
PWM_FREQ_O UT	ESTIMATOR_FI LT_EN		FG_SEL		FG_DIV		
R/W-0h	R/W-0h		R/W-0h		R/W-0h		

Figure 8-5. CLOSED\_LOOP1 Register (continued)

7	6	5	4	3	2	1	0
FG_CONFIG		FG_BEMF_THR		AVS_EN	RESERVED	RESERVED	RESERVED
R/W-0h		R/W-0h		R/W-0h	R-0h	R-0h	R-0h

Table 8-7. CLOSED\_LOOP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R	0h	Parity bit
30	OVERMODULATION_ENABLE	R/W	0h	Over-modulation enable 0h = Disable 1h = Enable
29-25	CL_ACC	R/W	0h	Closed loop acceleration Speed control (Hz/s) Power control (W/s) Current control (0.1A/s) Modulation index control(0.01% modulation index/s) 0h = 0.5 1h = 1 2h = 2.5 3h = 5 4h = 7.5 5h = 10 6h = 20 7h = 40 8h = 60 9h = 80 Ah = 100 Bh = 200 Ch = 300 Dh = 400 Eh = 500 Fh = 600 10h = 700 11h = 800 12h = 1000 13h = 1250 14h = 1500 15h = 2000 16h = 2500 17h = 3000 18h = 4000 19h = 5000 1Ah = 6000 1Bh = 8000 1Ch = 10000 1Dh = 20000 1Eh = 40000 1Fh = No limit
24	RESERVED	R	0h	Reserved

**Table 8-7. CLOSED\_LOOP1 Register Field Descriptions (continued)**

Bit	Field	Type	Reset	Description
23-19	CL_DEC	R/W	0h	Closed loop deceleration Speed control (Hz/s) Power control (W/s) Current control (0.1A/s) Modulation index control(0.01% modulation index/s) 0h = 0.5 1h = 1 2h = 2.5 3h = 5 4h = 7.5 5h = 10 6h = 20 7h = 40 8h = 60 9h = 80 Ah = 100 Bh = 200 Ch = 300 Dh = 400 Eh = 500 Fh = 600 10h = 700 11h = 800 12h = 1000 13h = 1250 14h = 1500 15h = 2000 16h = 2500 17h = 3000 18h = 4000 19h = 5000 1Ah = 6000 1Bh = 8000 1Ch = 10000 1Dh = 20000 1Eh = 40000 1Fh = No limit
18-15	PWM_FREQ_OUT	R/W	0h	PWM output frequency 0h = 10 kHz 1h = 15 kHz 2h = 20 kHz 3h = 25 kHz 4h = 30 kHz 5h = 35 kHz 6h = 40 kHz 7h = 45 kHz 8h = 50 kHz 9h = 55 kHz Ah = 60 kHz Bh = 65 kHz Ch = 70 kHz Dh = 75 kHz Eh = 80 kHz Fh = Not Applicable
14	ESTIMATOR_FILT_EN	R/W	0h	Estimator filter enable (Note: May introduce control response delay) 0h = Disable 1h = Enable
13-12	FG_SEL	R/W	0h	Configure motor states when speed feedback is available on FG 0h = Output FG in ISD, open loop and closed loop 1h = Output FG in only closed loop 2h = Output FG in open loop for the first try 3h = Not Defined

Table 8-7. CLOSED\_LOOP1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11-8	FG_DIV	R/W	0h	FG division factor 0h = Commutation cycle, 3x of electrical 1h = Divide by 1 (2-pole motor mechanical speed) 2h = Divide by 2 (4-pole motor mechanical speed) 3h = Divide by 3 (6-pole motor mechanical speed) 4h = Divide by 4 (8-pole motor mechanical speed) 5h = Divide by 5 (10-pole motor mechanical speed) 6h = Divide by 6 (12-pole motor mechanical speed) 7h = Divide by 7 (14-pole motor mechanical speed) 8h = Divide by 8 (16-pole motor mechanical speed) 9h = Divide by 9 (18-pole motor mechanical speed) Ah = Divide by 10 (20-pole motor mechanical speed) Bh = Divide by 11 (22-pole motor mechanical speed) Ch = Divide by 12 (24-pole motor mechanical speed) Dh = Divide by 13 (26-pole motor mechanical speed) Eh = Divide by 14 (28-pole motor mechanical speed) Fh = Divide by 15 (30-pole motor mechanical speed)
7	FG_CONFIG	R/W	0h	FG output configuration 0h = FG active as long as motor is driven 1h = FG active till BEMF drops below BEMF threshold defined by FG_BEMF_THR
6-4	FG_BEMF_THR	R/W	0h	BEMF threshold above which speed feedback information is available on FG, calculated as voltage at SHx pin divided by voltage gain(refer BUS_VOLT). 0h = $\pm 1$ mV 1h = $\pm 2$ mV 2h = $\pm 5$ mV 3h = $\pm 10$ mV 4h = $\pm 20$ mV 5h = $\pm 30$ mV 6h = Not Applicable 7h = Not Applicable
3	AVS_EN	R/W	0h	AVS enable 0h = Disable 1h = Enable
2	RESERVED	R	0h	Reserved
1	RESERVED	R	0h	Reserved
0	RESERVED	R	0h	Reserved

#### 8.1.6 CLOSED\_LOOP2 Register (Offset = 8Ah) [Reset = 00000000h]

CLOSED\_LOOP2 is shown in [Figure 8-6](#) and described in [Table 8-8](#).

Return to the [Summary Table](#).

Register to configure close loop settings2

Figure 8-6. CLOSED\_LOOP2 Register

31	30	29	28	27	26	25	24
PARITY	RESERVED	MTR_STOP			MTR_STOP_BRK_TIME		
R-0h	R-0h	R/W-0h			R/W-0h		
23	22	21	20	19	18	17	16
ACT_SPIN THR				BRAKE_SPEED_THRESHOLD			
R/W-0h				R/W-0h			
15	14	13	12	11	10	9	8
MOTOR_RES							
R/W-0h							

**Figure 8-6. CLOSED\_LOOP2 Register (continued)**

7	6	5	4	3	2	1	0
MOTOR_IND							
R/W-0h							

**Table 8-8. CLOSED\_LOOP2 Register Field Descriptions**

Bit	Field	Type	Reset	Description
31	PARITY	R	0h	Parity bit
30	RESERVED	R	0h	Reserved
29-28	MTR_STOP	R/W	0h	Motor stop mode 0h = Hi-Z 1h = Low side braking 2h = Active spin down 3h = Reserved
27-24	MTR_STOP_BRK_TIME	R/W	0h	Brake time during motor stop 0h = 10 ms 1h = 50 ms 2h = 100 ms 3h = 200 ms 4h = 300 ms 5h = 400 ms 6h = 500 ms 7h = 750 ms 8h = 1 s 9h = 2 s Ah = 3 s Bh = 4 s Ch = 5 s Dh = 7.5 s Eh = 10 s Fh = 15 s
23-20	ACT_SPIN_THR	R/W	0h	Active spin-down speed threshold (% of MAX_SPEED) 0h = 100% 1h = 90% 2h = 80% 3h = 70% 4h = 60% 5h = 50% 6h = 45% 7h = 40% 8h = 35% 9h = 30% Ah = 25% Bh = 20% Ch = 15% Dh = 10% Eh = Not Applicable Fh = Not Applicable

Table 8-8. CLOSED\_LOOP2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19-16	BRAKE_SPEED_THRES_HOLD	R/W	0h	Speed threshold below which brake is applied for BRAKE pin and Motor stop mode (Low side Braking) (% of MAX_SPEED) 0h = 100% 1h = 90% 2h = 80% 3h = 70% 4h = 60% 5h = 50% 6h = 45% 7h = 40% 8h = 35% 9h = 30% Ah = 25% Bh = 20% Ch = 15% Dh = 10% Eh = Not Applicable Fh = Not Applicable
15-8	MOTOR_RES	R/W	0h	Motor phase resistance
7-0	MOTOR_IND	R/W	0h	Motor phase inductance

### 8.1.7 CLOSED\_LOOP3 Register (Offset = 8Ch) [Reset = 00000000h]

CLOSED\_LOOP3 is shown in [Figure 8-7](#) and described in [Table 8-9](#).

Return to the [Summary Table](#).

Register to configure close loop settings3

Figure 8-7. CLOSED\_LOOP3 Register

31	30	29	28	27	26	25	24
PARITY	MOTOR_BEMF_CONST						
R-0h	R/W-0h						
23	22	21	20	19	18	17	16
MOTOR_BEMF_CONST	CURR_LOOP_KP						
R/W-0h	R/W-0h						
15	14	13	12	11	10	9	8
CURR_LOOP_KP			CURR_LOOP_KI				
R/W-0h							R/W-0h
7	6	5	4	3	2	1	0
CURR_LOOP_KI				SPD_LOOP_KP			
R/W-0h							R/W-0h

Table 8-9. CLOSED\_LOOP3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R	0h	Parity bit
30-23	MOTOR_BEMF_CONST	R/W	0h	Motor BEMF constant
22-13	CURR_LOOP_KP	R/W	0h	10-bit Kp value for Q-axis and D-axis current PI loop. CURR_LOOP_KP is divided in 2 sections - SCALE(9:8) and VALUE(7:0). Kp = VALUE / 10^SCALE Set to 0 for auto calculation of current Kp and Ki

**Table 8-9. CLOSED\_LOOP3 Register Field Descriptions (continued)**

Bit	Field	Type	Reset	Description
12-3	CURR_LOOP_KI	R/W	0h	10-bit Ki value for Q-axis and D-axis current PI loop. CURR_LOOP_KI is divided in 2 sections - SCALE(9:8) and VALUE(7:0). $Ki = 1000 \times VALUE / 10^{SCALE}$ Set to 0 for auto calculation of current Kp and Ki
2-0	SPD_LOOP_KP	R/W	0h	3 MSB bits for speed loop/power loop Kp. SPD_LOOP_KP is divided in 2 sections - SCALE(9:8) and VALUE(7:0). $Kp = 0.01 \times VALUE / 10^{SCALE}$ .

**8.1.8 CLOSED\_LOOP4 Register (Offset = 8Eh) [Reset = 00000000h]**

CLOSED\_LOOP4 is shown in [Figure 8-8](#) and described in [Table 8-10](#).

Return to the [Summary Table](#).

Register to configure close loop settings4

**Figure 8-8. CLOSED\_LOOP4 Register**

31	30	29	28	27	26	25	24
PARITY					SPD_LOOP_KP		
R-0h					R/W-0h		
23	22	21	20	19	18	17	16
				SPD_LOOP_KI			
				R/W-0h			
15	14	13	12	11	10	9	8
SPD_LOOP_KI				MAX_SPEED			
R/W-0h				R/W-0h			
7	6	5	4	3	2	1	0
				MAX_SPEED			
				R/W-0h			

**Table 8-10. CLOSED\_LOOP4 Register Field Descriptions**

Bit	Field	Type	Reset	Description
31	PARITY	R	0h	Parity bit
30-24	SPD_LOOP_KP	R/W	0h	7 LSB bits for speed loop/power loop Kp. SPD_LOOP_KP is divided in 2 sections - SCALE(10:9) and VALUE(8:0). $Kp = 0.01 \times VALUE / 10^{SCALE}$ .
23-14	SPD_LOOP_KI	R/W	0h	10 bit value for speed loop/power loop Ki. SPD_LOOP_KI is divided in 2 sections - SCALE(9:8) and VALUE(7:0). $Ki = 0.1 \times VALUE / 10^{SCALE}$ .
13-0	MAX_SPEED	R/W	0h	Maximum motor speed in electrical Hz = MAX_SPEED/4 For example, if MAX_SPEED is 0x7D0(2000d), then maximum motor speed (Hz) is 2000/4 = 500Hz

**8.1.9 REF\_PROFILES1 Register (Offset = 94h) [Reset = 00000000h]**

REF\_PROFILES1 is shown in [Figure 8-9](#) and described in [Table 8-11](#).

Return to the [Summary Table](#).

Register to configure reference profile1

Figure 8-9. REF\_PROFILES1 Register

31	30	29	28	27	26	25	24
PARITY	REF_PROFILE_CONFIG				DUTY_ON1		
R-0h	R/W-0h				R/W-0h		
23	22	21	20	19	18	17	16
	DUTY_ON1				DUTY_OFF1		
	R/W-0h				R/W-0h		
15	14	13	12	11	10	9	8
	DUTY_OFF1				DUTY_CLAMP1		
	R/W-0h				R/W-0h		
7	6	5	4	3	2	1	0
	DUTY_CLAMP1				DUTY_A		
	R/W-0h				R/W-0h		

Table 8-11. REF\_PROFILES1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R	0h	Parity bit
30-29	REF_PROFILE_CONFIG	R/W	0h	Reference profile mode configuration 0h = Reference mode 1h = Linear mode 2h = Staircase mode 3h = Forward Reverse mode
28-21	DUTY_ON1	R/W	0h	Duty_ON1 Configuration Turn On duty cycle (%) = $\{(DUTY\_ON1/256) \times 100\}$
20-13	DUTY_OFF1	R/W	0h	Duty_OFF1 Configuration Turn Off duty cycle (%) = $\{(DUTY\_OFF1/256) \times 100\}$
12-5	DUTY_CLAMP1	R/W	0h	Duty_CLAMP1 Configuration duty cycle for clamping (%) = $\{(DUTY\_CLAMP1/256) \times 100\}$
4-0	DUTY_A	R/W	0h	5 MSB bits for Duty Cycle A

#### 8.1.10 REF\_PROFILES2 Register (Offset = 96h) [Reset = 00000000h]

REF\_PROFILES2 is shown in Figure 8-10 and described in Table 8-12.

Return to the [Summary Table](#).

Register to configure reference profile2

Figure 8-10. REF\_PROFILES2 Register

31	30	29	28	27	26	25	24
PARITY		DUTY_A			DUTY_B		
R-0h	R/W-0h				R/W-0h		
23	22	21	20	19	18	17	16
	DUTY_B				DUTY_C		
	R/W-0h				R/W-0h		
15	14	13	12	11	10	9	8
	DUTY_C				DUTY_D		
	R/W-0h				R/W-0h		

**Figure 8-10. REF\_PROFILES2 Register (continued)**

7	6	5	4	3	2	1	0
DUTY_D				DUTY_E			
R/W-0h				R/W-0h			

**Table 8-12. REF\_PROFILES2 Register Field Descriptions**

Bit	Field	Type	Reset	Description
31	PARITY	R	0h	Parity bit
30-28	DUTY_A	R/W	0h	3 LSB bits for Duty Cycle A Configuration Duty Cycle A (%) = $\{(DUTY\_A/256) \times 100\}$
27-20	DUTY_B	R/W	0h	Duty_B Configuration Duty cycle B (%) = $\{(DUTY\_B/256) \times 100\}$
19-12	DUTY_C	R/W	0h	Duty_C Configuration Duty cycle C (%) = $\{(DUTY\_C/256) \times 100\}$
11-4	DUTY_D	R/W	0h	Duty_D Configuration Duty cycle D (%) = $\{(DUTY\_D/256) \times 100\}$
3-0	DUTY_E	R/W	0h	4 MSB bits for Duty Cycle E

### 8.1.11 REF\_PROFILES3 Register (Offset = 98h) [Reset = 00000000h]

REF\_PROFILES3 is shown in [Figure 8-11](#) and described in [Table 8-13](#).

Return to the [Summary Table](#).

Register to configure reference profile3

**Figure 8-11. REF\_PROFILES3 Register**

31	30	29	28	27	26	25	24
PARITY	DUTY_E				DUTY_ON2		
R-0h	R/W-0h				R/W-0h		
23	22	21	20	19	18	17	16
DUTY_ON2				DUTY_OFF2			
R/W-0h				R/W-0h			
15	14	13	12	11	10	9	8
DUTY_OFF2				DUTY_CLAMP2			
R/W-0h				R/W-0h			
7	6	5	4	3	2	1	0
DUTY_CLAMP2				DUTY_HYS		RESERVED	
R/W-0h				R/W-0h		R-0h	

**Table 8-13. REF\_PROFILES3 Register Field Descriptions**

Bit	Field	Type	Reset	Description
31	PARITY	R	0h	Parity bit
30-27	DUTY_E	R/W	0h	4 LSB bits for Duty Cycle E Configuration Duty cycle E (%) = $\{(DUTY\_E/256) \times 100\}$
26-19	DUTY_ON2	R/W	0h	Duty_ON2 Configuration Turn On duty cycle (%) = $\{(DUTY\_ON2/256) \times 100\}$
18-11	DUTY_OFF2	R/W	0h	Duty_OFF2 Configuration Turn Off duty cycle (%) = $\{(DUTY\_OFF2/256) \times 100\}$
10-3	DUTY_CLAMP2	R/W	0h	Duty_CLAMP2 Configuration Duty cycle for clamping (%) = $\{(DUTY\_CLAMP2/256) \times 100\}$

Table 8-13. REF\_PROFILES3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-1	DUTY_HYS	R/W	0h	Input duty hysteresis 0h = 0% 1h = 1% 2h = 2% 3h = 3%
0	RESERVED	R	0h	Reserved

#### 8.1.12 REF\_PROFILES4 Register (Offset = 9Ah) [Reset = 00000000h]

REF\_PROFILES4 is shown in [Figure 8-12](#) and described in [Table 8-14](#).

Return to the [Summary Table](#).

Register to configure reference profile4

Figure 8-12. REF\_PROFILES4 Register

31	30	29	28	27	26	25	24
PARITY				REF_OFF1			
R-0h				R/W-0h			
23	22	21	20	19	18	17	16
REF_OFF1				REF_CLAMP1			
R/W-0h				R/W-0h			
15	14	13	12	11	10	9	8
REF_CLAMP1				REF_A			
R/W-0h				R/W-0h			
7	6	5	4	3	2	1	0
REF_A				REF_B			
R/W-0h				R/W-0h			

Table 8-14. REF\_PROFILES4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R	0h	Parity bit
30-23	REF_OFF1	R/W	0h	Turn off ref Configuration Turn off reference (% of Maximum Reference) = $\{(REF\_OFF1/256) \times 100\}$
22-15	REF_CLAMP1	R/W	0h	Ref Clamp1 Configuration Clamp ref (% of Maximum Reference) = $\{(REF\_CLAMP1/256) \times 100\}$
14-7	REF_A	R/W	0h	Ref A configuration Ref A (% of Maximum Reference) = $\{(REF\_A/256) \times 100\}$
6-0	REF_B	R/W	0h	7 MSB of REF_B configuration

#### 8.1.13 REF\_PROFILES5 Register (Offset = 9Ch) [Reset = 00000000h]

REF\_PROFILES5 is shown in [Figure 8-13](#) and described in [Table 8-15](#).

Return to the [Summary Table](#).

Register to configure reference profile5

Figure 8-13. REF\_PROFILES5 Register

31	30	29	28	27	26	25	24
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**Figure 8-13. REF\_PROFILES5 Register (continued)**

PARITY	REF_B	REF_C						
R-0h	R/W-0h	R/W-0h						
23	22	21	20	19	18	17	16	
REF_C		REF_D						
R/W-0h		R/W-0h						
15	14	13	12	11	10	9	8	
REF_D		REF_E						
R/W-0h		R/W-0h						
7	6	5	4	3	2	1	0	
REF_E		MIN_DUTY		MIXED_MODE_CONFIG		DUTY_COMMAND_FILTER	RESERVED	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	R-0h	

**Table 8-15. REF\_PROFILES5 Register Field Descriptions**

Bit	Field	Type	Reset	Description
31	PARITY	R	0h	Parity bit
30	REF_B	R/W	0h	1 LSB of REF_B configuration Ref B(% of Maximum Reference) = $\{(REF_B/256) \times 100\}$
29-22	REF_C	R/W	0h	Ref C configuration Ref C (% of Maximum Reference) = $\{(REF_C/256) \times 100\}$
21-14	REF_D	R/W	0h	Ref D configuration Ref D (% of Maximum Reference) = $\{(REF_D/256) \times 100\}$
13-6	REF_E	R/W	0h	Ref E Configuration Ref E(% of Maximum Reference) = $\{(REF_E/256)*100\}$
5-4	MIN_DUTY	R/W	0h	Minimum input duty threshold above which motor start (Applicable only if REF_PROFILE_CONFIG = 0h) 0h = 1% 1h = 3% 2h = 5% 3h = 10%
3-2	MIXED_MODE_CONFIG	R/W	0h	Mixed control mode configuration (Applicable only if REF_PROFILE_CONFIG = 1h or REF_PROFILE_CONFIG = 2h) 0h = User defined reference modes throughout the input duty range 1h = Modulation index control if input duty > DUTY_C + DUTY_HYST; configured CTRL_MODE if input duty < DUTY_C - DUTY_HYST 2h = configured CTRL_MODE if input duty > DUTY_C + DUTY_HYST; Modulation index control if input duty < DUTY_C - DUTY_HYST 3h = Not Applicable
1	DUTY_COMMAND_FILTER	R/W	0h	Input duty filter 0h = Filter on input duty is disabled 1h = Filter on input duty is enabled (0.4%)
0	RESERVED	R	0h	Reserved

#### 8.1.14 REF\_PROFILES6 Register (Offset = 9Eh) [Reset = 00000000h]

REF\_PROFILES6 is shown in [Figure 8-14](#) and described in [Table 8-16](#).

Return to the [Summary Table](#).

Register to configure reference profile6

Figure 8-14. REF\_PROFILES6 Register

31	30	29	28	27	26	25	24
PARITY	REF_OFF2						
R-0h	R/W-0h						
23	22	21	20	19	18	17	16
REF_OFF2	REF_CLAMP2						
R/W-0h	R/W-0h						
15	14	13	12	11	10	9	8
REF_CLAMP2	HALL_ANGLE_REF						RESERVED
R/W-0h	R/W-0h						
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

Table 8-16. REF\_PROFILES6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R	0h	Parity bit
30-23	REF_OFF2	R/W	0h	Turn off Ref Configuration Turn off Ref (% of Maximum Reference)) = {(REF_OFF2/256) × 100}
22-15	REF_CLAMP2	R/W	0h	Clamp Ref Configuration Clamp Ref (% of Maximum Reference) = {(REF_CLAMP2/256) × 100}
14-9	HALL_ANGLE_REF	R/W	0h	Hall sensor angle reference for offset calibration (degrees = HALL_ANGLE_REF × 360/63)
8-0	RESERVED	R	0h	Reserved

## 8.2 Fault\_Configuration Registers

**Table 8-17** lists the memory-mapped registers for the Fault\_Configuration registers. All register offset addresses not listed in **Table 8-17** should be considered as reserved locations and the register contents should not be modified.

**Table 8-17. FAULT\_CONFIGURATION Registers**

Offset	Acronym	Register Name	Section
90h	FAULT_CONFIG1	Fault Configuration1	<a href="#">Section 8.2.1</a>
92h	FAULT_CONFIG2	Fault Configuration2	<a href="#">Section 8.2.2</a>

Complex bit access types are encoded to fit into small table cells. **Table 8-18** shows the codes that are used for access types in this section.

**Table 8-18. Fault\_Configuration Access Type Codes**

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

### 8.2.1 FAULT\_CONFIG1 Register (Offset = 90h) [Reset = 00000000h]

FAULT\_CONFIG1 is shown in [Figure 8-15](#) and described in [Table 8-19](#).

Return to the [Summary Table](#).

Register to configure fault settings1

**Figure 8-15. FAULT\_CONFIG1 Register**

31	30	29	28	27	26	25	24
PARITY	ILIMIT				HW_LOCK_ILIMIT		
R-0h	R/W-0h				R/W-0h		
23	22	21	20	19	18	17	16
HW_LOCK_ILI MIT	LOCK_ILIMIT				EEP_FAULT_M ODE	LOCK_ILIMIT_MODE	
R/W-0h	R/W-0h				R/W-0h	R/W-0h	
15	14	13	12	11	10	9	8
LOCK_ILIMIT_MODE	LOCK_ILIMIT_DEG				LCK_RETRY		
R/W-0h	R/W-0h				R/W-0h		
7	6	5	4	3	2	1	0
LCK_RETRY	I2C_CRC_ERR _MODE	MTR_LCK_MODE				MIN_VM_MOD E	MAX_VM_MOD E
R/W-0h	R/W-0h	R/W-0h				R/W-0h	R/W-0h
		R/W-0h				SATURATION_FLAGS_EN	

**Table 8-19. FAULT\_CONFIG1 Register Field Descriptions**

Bit	Field	Type	Reset	Description
31	PARITY	R	0h	Parity bit

Table 8-19. FAULT\_CONFIG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
30-27	ILIMIT	R/W	0h	Phase current peak limit (% of BASE_CURRENT) 0h = 5% 1h = 10% 2h = 15% 3h = 20% 4h = 25% 5h = 30% 6h = 40% 7h = 45% 8h = 50% 9h = 55% Ah = 60% Bh = 65% Ch = 70% Dh = 75% Eh = 80% Fh = 85%
26-23	HW_LOCK_ILIMIT	R/W	0h	Comparator based lock detection current limit (% of BASE_CURRENT) 0h = 0% 1h = 6.7% 2h = 13.3% 3h = 20% 4h = 26.7% 5h = 33.3% 6h = 40% 7h = 46.7% 8h = 53.3% 9h = 60% Ah = 66.7% Bh = 73.3% Ch = 80% Dh = 86.7% Eh = 93.3% Fh = 100%
22-19	LOCK_ILIMIT	R/W	0h	ADC based lock detection current limit (% of BASE_CURRENT) 0h = 10% 1h = 15% 2h = 20% 3h = 25% 4h = 30% 5h = 40% 6h = 50% 7h = 55% 8h = 60% 9h = 65% Ah = 70% Bh = 75% Ch = 80% Dh = 85% Eh = 90% Fh = 95%
18	EEP_FAULT_MODE	R/W	0h	EEPROM error fault mode 0h = EEPROM fault causes latched fault; nFAULT is active; Gate driver is tristated 1h = EEPROM fault causes report only but no action is taken; nFAULT is active

**Table 8-19. FAULT\_CONFIG1 Register Field Descriptions (continued)**

Bit	Field	Type	Reset	Description
17-15	LOCK_ILIMIT_MODE	R/W	0h	Lock detection current limit fault mode 0h = Ilimit lock detection causes latched fault; nFAULT active; Gate driver is tristated 1h = Ilimit lock detection causes latched fault; nFAULT active; Gate driver is in low side brake mode (All low side FETs are turned ON) 2h = Ilimit lock detection causes latched fault; nFAULT active; Gate driver is in low side brake mode (All low side FETs are turned ON) 3h = Fault automatically cleared after LCK_RETRY time. Number of retries limited to AUTO_RETRY_TIMES. If number of retries exceed AUTO_RETRY_TIMES, fault is latched; Gate driver is tristated; nFAULT active 4h = Fault automatically cleared for AUTO_RETRY_TIMES after LCK_RETRY time; Gate driver is in low side brake mode (All low side FETs are turned ON); nFAULT active 5h = Fault automatically cleared after LCK_RETRY time. Number of retries limited to AUTO_RETRY_TIMES. If number of retries exceed AUTO_RETRY_TIMES, fault is latched; Gate driver is in low side brake mode (All low side FETs are turned ON); nFAULT active 6h = Ilimit lock detection current limit is in report only but no action is taken; nFAULT active 7h = ILIMIT LOCK is disabled
14-11	LOCK_ILIMIT_DEG	R/W	0h	Lock detection current limit fault deglitch time 0h = No deglitch 1h = 0.1 ms 2h = 0.2 ms 3h = 0.5 ms 4h = 1 ms 5h = 2.5 ms 6h = 5 ms 7h = 7.5 ms 8h = 10 ms 9h = 25 ms Ah = 50 ms Bh = 75 ms Ch = 100 ms Dh = 200 ms Eh = 500 ms Fh = 1000 ms
10-7	LCK_RETRY	R/W	0h	Lock detection fault retry time 0h = 300 ms 1h = 500 ms 2h = 1 s 3h = 2 s 4h = 3 s 5h = 4 s 6h = 5 s 7h = 6 s 8h = 7 s 9h = 8 s Ah = 9 s Bh = 10 s Ch = 11 s Dh = 12 s Eh = 13 s Fh = 14 s
6	I2C_CRC_ERR_MODE	R/W	0h	I2C CRC error fault mode 0h = CRC error on I2C causes latched fault; nFAULT is active; Gate driver is tristated 1h = CRC error on I2C causes report only but no action is taken; nFAULT is active

Table 8-19. FAULT\_CONFIG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-3	MTR_LCK_MODE	R/W	0h	Motor lock fault mode 0h = Motor lock detection causes latched fault; nFAULT active; Gate driver is tristated 1h = Motor lock detection causes latched fault; nFAULT active; Gate driver is in low side brake mode (All low side FETs are turned ON) 2h = Motor lock detection causes latched fault; nFAULT active; Gate driver is in low side brake mode (All low side FETs are turned ON) 3h = Fault automatically cleared after LCK_RETRY time. Number of retries limited to AUTO_RETRY_TIMES. If number of retries exceed AUTO_RETRY_TIMES, fault is latched; Gate driver is tristated; nFAULT active 4h = Fault automatically cleared for AUTO_RETRY_TIMES after LCK_RETRY time; Gate driver is in low side brake mode (All low side FETs are turned ON); nFAULT active 5h = Fault automatically cleared after LCK_RETRY time. Number of retries limited to AUTO_RETRY_TIMES. If number of retries exceed AUTO_RETRY_TIMES, fault is latched; Gate driver is in low side brake mode (All low side FETs are turned ON); nFAULT active 6h = Motor lock detection current limit is in report only but no action is taken; nFAULT active 7h = MTR LOCK is disabled
2	MIN_VM_MODE	R/W	0h	PVDD undervoltage fault recovery mode 0h = PVDD under voltage fault causes latched fault; nFAULT is active; Gate driver is tristated 1h = PVDD under voltage fault clears automatically if the PVDD voltage is more than (MIN_VM_MOTOR + VOLTAGE_HYSTERESIS); Gate driver is tristated; nFAULT active
1	MAX_VM_MODE	R/W	0h	PVDD overvoltage fault recovery mode 0h = PVDD over voltage fault causes latched fault; nFAULT is active; Gate driver is tristated 1h = PVDD over voltage fault clears automatically if the PVDD voltage is less than (MAX_VM_MOTOR - VOLTAGE_HYSTERESIS); Gate driver is tristated; nFAULT active
0	SATURATION_FLAGS_EN	R/W	0h	Current and speed loop saturation indication enable 0h = Disable 1h = Enable

### 8.2.2 FAULT\_CONFIG2 Register (Offset = 92h) [Reset = 00000000h]

FAULT\_CONFIG2 is shown in [Figure 8-16](#) and described in [Table 8-20](#).

Return to the [Summary Table](#).

Register to configure fault settings2

Figure 8-16. FAULT\_CONFIG2 Register

31	30	29	28	27	26	25	24
PARITY	LOCK1_EN	LOCK2_EN	LOCK3_EN	LOCK_ABN_SPEED		ABNORMAL_BEMF_THR	
R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h
23	22	21	20	19	18	17	16
ABNORMAL_BEMF_THR		NO_MTR_THR		HW_LOCK_ILIMIT_MODE			
R/W-0h		R/W-0h		R/W-0h			
15	14	13	12	11	10	9	8
HW_LOCK_ILIMIT_DEG		VOLTAGE_HYSTERESIS		MIN_VM_MOTOR			
R/W-0h		R/W-0h		R/W-0h			
7	6	5	4	3	2	1	0

**Figure 8-16. FAULT\_CONFIG2 Register (continued)**

MIN_VM_MOT OR	MAX_VM_MOTOR	AUTO_RETRY_TIMES
R/W-0h	R/W-0h	R/W-0h

**Table 8-20. FAULT\_CONFIG2 Register Field Descriptions**

Bit	Field	Type	Reset	Description
31	PARITY	R	0h	Parity bit
30	LOCK1_EN	R/W	0h	Lock 1 (abnormal speed fault) enable 0h = Disable 1h = Enable
29	LOCK2_EN	R/W	0h	Lock 2 (abnormal BEMF fault) enable 0h = Disable 1h = Enable
28	LOCK3_EN	R/W	0h	Lock 3 (no motor fault) enable 0h = Disable 1h = Enable
27-25	LOCK_ABN_SPEED	R/W	0h	Abnormal speed lock detection threshold (% of MAX_SPEED) 0h = 130% 1h = 140% 2h = 150% 3h = 160% 4h = 170% 5h = 180% 6h = 190% 7h = 200%
24-22	ABNORMAL_BEMF_THR	R/W	0h	Abnormal BEMF lock detection threshold (% of expected Back-EMF) Expected Back-EMF = MOTOR_BEMF_CONST × Estimated speed in Hz 0h = 40% 1h = 45% 2h = 50% 3h = 55% 4h = 60% 5h = 65% 6h = 67.5% 7h = 70%
21-19	NO_MTR_THR	R/W	0h	No motor fault condition is true if the motor phase current is less than NO_MTR_THR (% of BASE_CURRENT) 0h = 1% 1h = 2% 2h = 3% 3h = 4% 4h = 5% 5h = 7.5% 6h = 10% 7h = 20%

Table 8-20. FAULT\_CONFIG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18-16	HW_LOCK_ILIMIT_MODE	R/W	0h	<p>Hardware lock detection fault mode</p> <p>0h = Hardware Ilimit lock detection causes latched fault; nFAULT active; Gate driver is tristated</p> <p>1h = Hardware Ilimit lock detection causes latched fault; nFAULT active; Gate driver is in low side brake mode (All low side FETs are turned ON)</p> <p>2h = Hardware Ilimit lock detection causes latched fault; nFAULT active; Gate driver is in low side brake mode (All low side FETs are turned ON)</p> <p>3h = Fault automatically cleared after LCK_RETRY time. Number of retries limited to AUTO_RETRY_TIMES. If number of retries exceed AUTO_RETRY_TIMES, fault is latched; Gate driver is tristated; nFAULT active</p> <p>4h = Fault automatically cleared for AUTO_RETRY_TIMES after LCK_RETRY time; Gate driver is in low side brake mode (All low side FETs are turned ON); nFAULT active</p> <p>5h = Fault automatically cleared after LCK_RETRY time. Number of retries limited to AUTO_RETRY_TIMES. If number of retries exceed AUTO_RETRY_TIMES, fault is latched; Gate driver is in low side brake mode (All low side FETs are turned ON); nFAULT active</p> <p>6h = Hardware Ilimit lock detection current limit is in report only but no action is taken; nFAULT active</p> <p>7h = HARDWARE ILIMIT LOCK is disabled</p>
15-13	HW_LOCK_ILIMIT_DEG	R/W	0h	<p>Hardware lock detection current limit deglitch time</p> <p>0h = Not Applicable</p> <p>1h = Not Applicable</p> <p>2h = 2 <math>\mu</math>s</p> <p>3h = 3 <math>\mu</math>s</p> <p>4h = 4 <math>\mu</math>s</p> <p>5h = 5 <math>\mu</math>s</p> <p>6h = 6 <math>\mu</math>s</p> <p>7h = 7 <math>\mu</math>s</p>
12-11	VOLTAGE_HYSTERESIS	R/W	0h	<p>Hysteresis for PVDD overvoltage and undervoltage faults. Fault triggered at threshold, cleared at threshold <math>\pm</math> hysteresis (+ for UV, - for OV)</p> <p>0h = 1 V</p> <p>1h = 1.5 V</p> <p>2h = 2 V</p> <p>3h = 3 V</p>
10-7	MIN_VM_MOTOR	R/W	0h	<p>PVDD undervoltage fault threshold (minimum DC bus voltage for running motor)</p> <p>0h = No Limit</p> <p>1h = 6 V</p> <p>2h = 7 V</p> <p>3h = 8 V</p> <p>4h = 9 V</p> <p>5h = 12 V</p> <p>6h = 14 V</p> <p>7h = 16 V</p> <p>8h = 18 V</p> <p>9h = 20 V</p> <p>Ah = 24 V</p> <p>Bh = 26 V</p> <p>Ch = 28 V</p> <p>Dh = 30 V</p> <p>Eh = 32 V</p> <p>Fh = 36 V</p>

**Table 8-20. FAULT\_CONFIG2 Register Field Descriptions (continued)**

Bit	Field	Type	Reset	Description
6-3	MAX_VM_MOTOR	R/W	0h	PVDD overvoltage fault threshold (maximum DC bus voltage for running motor) 0h = No Limit 1h = 16 V 2h = 18 V 3h = 20 V 4h = 22 V 5h = 26 V 6h = 28 V 7h = 32 V 8h = 34 V 9h = 36 V Ah = 38 V Bh = 40 V Ch = 44 V Dh = 48 V Eh = 54 V Fh = 58 V
2-0	AUTO_RETRY_TIMES	R/W	0h	Automatic fault retry attempts. This is used only if any of the fault mode is configured as "retry" 0h = No Limit 1h = 2 2h = 3 3h = 5 4h = 7 5h = 10 6h = 15 7h = 20

## 8.3 Hardware\_Configuration Registers

Table 8-21 lists the memory-mapped registers for the Hardware\_Configuration registers. All register offset addresses not listed in Table 8-21 should be considered as reserved locations and the register contents should not be modified.

Table 8-21. HARDWARE\_CONFIGURATION Registers

Offset	Acronym	Register Name	Section
A4h	PIN_CONFIG	Hardware Pin Configuration	Section 8.3.1
A6h	DEVICE_CONFIG1	Device configuration1	Section 8.3.2
A8h	DEVICE_CONFIG2	Device configuration2	Section 8.3.3
AAh	PERI_CONFIG1	Peripheral Configuration1	Section 8.3.4
ACh	GD_CONFIG1	Gate Driver Configuration1	Section 8.3.5
AEh	GD_CONFIG2	Gate Driver Configuration2	Section 8.3.6

Complex bit access types are encoded to fit into small table cells. Table 8-22 shows the codes that are used for access types in this section.

Table 8-22. Hardware\_Configuration Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

### 8.3.1 PIN\_CONFIG Register (Offset = A4h) [Reset = 00000000h]

PIN\_CONFIG is shown in Figure 8-17 and described in Table 8-23.

Return to the [Summary Table](#).

Register to configure hardware pins

Figure 8-17. PIN\_CONFIG Register

31	30	29	28	27	26	25	24
PARITY	FLUX_WEAKENING_CURRENT_RATIO				LEAD_ANGLE		
R-0h	R/W-0h				R/W-0h		
23	22	21	20	19	18	17	16
LEAD_ANGLE	MAX_POWER						
R/W-0h	R/W-0h						
15	14	13	12	11	10	9	8
MAX_POWER					FG_IDLE_CONFIG		FG_FAULT_CO_NFIG
R/W-0h					R/W-0h		R/W-0h
7	6	5	4	3	2	1	0
FG_FAULT_CO_NFIG	HALL_SNS_ST_ARTUP_EN	HALL_EN	nMCU_RST	BRAKE_INPUT		SPEED_MODE	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h	

**Figure 8-17. PIN\_CONFIG Register (continued)**
**Table 8-23. PIN\_CONFIG Register Field Descriptions**

Bit	Field	Type	Reset	Description
31	PARITY	R	0h	Parity bit
30-28	FLUX_WEAKENING_CURRENT_RATIO	R/W	0h	Maximum flux weakening current reference (% of ILIMIT) 0h = Circular current limit 1h = 80% 2h = 70% 3h = 60% 4h = 50% 5h = 40% 6h = 30% 7h = 20%
27-22	LEAD_ANGLE	R/W	0h	Lead angle. In Modulation index control, positive value indicates the applied voltage is leading the BEMF, negative value indicates applied voltage is lagging the BEMF. In other modes, positive means positive id reference, negative means negative id reference Lead angle (degrees) 0- 31 = $1.5 \times \text{LEAD\_ANGLE}$ 32 - 63 = $1.5 \times (\text{LEAD\_ANGLE} - 64)$
21-11	MAX_POWER	R/W	0h	Maximum power (Watts) 0- 1023 = $1 \times \text{MAX\_POWER}$ 1024 - 2047 = $2 \times (\text{MAX\_POWER} - 1024) + 1024$
10-9	FG_IDLE_CONFIG	R/W	0h	FG configuration during motor idle state 0h = FG is set by last driven state 1h = FG is Hi-Z (Externally pulled up) 2h = FG is pulled to Low 3h = FG is Hi-Z (Externally pulled up)
8-7	FG_FAULT_CONFIG	R/W	0h	FG configuration during fault state. BEMF threshold defined by FG_BEMF_THR if FG_CONFIG 1 0h = FG is pulled to Low 1h = FG is Hi-Z (Externally pulled up) 2h = FG reports fault type as a unique duty cycle at 1 Hz 3h = FG active till BEMF drops below BEMF threshold defined by FG_BEMF_THR if FG_CONFIG is 1
6	HALL_SNS_STARTUP_EN	R/W	0h	Hall sensor-based motor startup enable 0h = Disable 1h = Enable
5	HALL_EN	R/W	0h	Hall sensor input enable 0h = Disable 1h = Enable
4	nMCU_RST	R/W	0h	External MCU reset signal duration during watchdog fault 0h = 1 ms 1h = 5 ms
3-2	BRAKE_INPUT	R/W	0h	Brake pin mode 0h = Not Applicable 1h = Override pin and brake according to BRAKE_PIN_MODE 2h = Override pin and do not brake / align 3h = Not Applicable
1-0	SPEED_MODE	R/W	0h	Configure reference command mode from speed/wake pin 0h = Analog mode 1h = Controlled by duty cycle of SPEED input pin 2h = Register override mode 3h = Controlled by frequency of SPEED input pin

### 8.3.2 DEVICE\_CONFIG1 Register (Offset = A6h) [Reset = 000XXXX0h]

 DEVICE\_CONFIG1 is shown in [Figure 8-18](#) and described in [Table 8-24](#).

Return to the [Summary Table](#).

Register to configure device

**Figure 8-18. DEVICE\_CONFIG1 Register**

31	30	29	28	27	26	25	24
PARITY	MTPA_EN	RESERVED	RESERVED		I2C_TARGET_ADDR		
R-0h	R/W-0h	R-0h		R-0h		R/W-0h	
23	22	21	20	19	18	17	16
	I2C_TARGET_ADDR				EEPROM_LOCK_KEY		
					R/W-0h		R/W-XXXh
15	14	13	12	11	10	9	8
			EEPROM_LOCK_KEY				R/W-XXXh
7	6	5	4	3	2	1	0
	EEPROM_LOCK_KEY		SLEW_RATE_I2C_PINS	PULLUP_ENABLE		BUS_VOLT	
			R/W-0h		R/W-0h		R/W-0h
	R/W-XXXh						

**Table 8-24. DEVICE\_CONFIG1 Register Field Descriptions**

Bit	Field	Type	Reset	Description
31	PARITY	R	0h	Parity bit
30	MTPA_EN	R/W	0h	Maximum Torque Per Ampere (MTPA) operation enable 0h = Disable 1h = Enable
29-28	RESERVED	R	0h	Reserved
27	RESERVED	R	0h	Reserved
26-20	I2C_TARGET_ADDR	R/W	0h	I2C target address
19-5	EEPROM_LOCK_KEY	R/W	0h	EEPROM lock access key. This value when read will always show 0
4-3	SLEW_RATE_I2C_PINS	R/W	0h	I2C pins slew rate configuration 0h = 4.8 mA 1h = 3.9 mA 2h = 1.86 mA 3h = 30.8 mA
2	PULLUP_ENABLE	R/W	0h	Internal pull-up to AVDD enable for nFAULT and FG pins 0h = Disable 1h = Enable
1-0	BUS_VOLT	R/W	0h	Maximum PVDD voltage configuration. Voltage gain = 20 V/V, BUS_VOLT = 60 Voltage gain = 10 V/V, BUS_VOLT = 30 Voltage gain = 5 V/V, BUS_VOLT = 15 0h = 15 V 1h = 30 V 2h = 60 V 3h = Not defined

### 8.3.3 DEVICE\_CONFIG2 Register (Offset = A8h) [Reset = 00000000h]

DEVICE\_CONFIG2 is shown in [Figure 8-19](#) and described in [Table 8-25](#).

Return to the [Summary Table](#).

Register to configure device

**Figure 8-19. DEVICE\_CONFIG2 Register**

31	30	29	28	27	26	25	24
PARITY	INPUT_MAXIMUM_FREQ						
R-0h	R/W-0h						
23	22	21	20	19	18	17	16
INPUT_MAXIMUM_FREQ							
R/W-0h							
15	14	13	12	11	10	9	8
SLEEP_ENTRY_TIME	LIMP_HOME_EN	DYNAMIC_VOLTAGE_GAIN_EN	DEV_MODE	PWM_DITHER_DEPTH	RESERVED		
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h		
7	6	5	4	3	2	1	0
RESERVED		EXT_WD_EN	EXT_WD_CONFIG	EXT_WD_INPULSE_MODE	EXT_WD_FAULT_MODE		
R-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	

**Table 8-25. DEVICE\_CONFIG2 Register Field Descriptions**

Bit	Field	Type	Reset	Description
31	PARITY	R	0h	Parity bit
30-16	INPUT_MAXIMUM_FREQ	R/W	0h	Speed pin input frequency configuration for frequency control mode that corresponds to 100% duty cycle Input duty cycle = Input frequency / INPUT_MAXIMUM_FREQ
15-14	SLEEP_ENTRY_TIME	R/W	0h	Sleep command detection time. (Refer Table: Conditions to Enter or Exit Sleep Modes) 0h = 50 µs 1h = 200 µs 2h = 20 ms 3h = 200 ms
13	LIMP_HOME_EN	R/W	0h	Limp home mode enable 0h = Disable 1h = Enable
12	DYNAMIC_VOLTAGE_GAIN_EN	R/W	0h	Dynamic voltage gain adjustment enable 0h = Disable 1h = Enable
11	DEV_MODE	R/W	0h	Device mode select 0h = Standby mode 1h = Sleep mode
10-9	PWM_DITHER_DEPTH	R/W	0h	PWM dither depth 0h = PWM dither disabled 1h = 5% 2h = 7.5% 3h = 10%
8	RESERVED	R	0h	Reserved
7-5	RESERVED	R	0h	Reserved
4	EXT_WD_EN	R/W	0h	External watchdog enable 0h = Disable 1h = Enable
3-2	EXT_WD_CONFIG	R/W	0h	Time between watchdog tickles (GPIO/I2C) 0h = 100 ms/1 s 1h = 200 ms/2 s 2h = 500 ms/5 s 3h = 1000 ms/10 s

Table 8-25. DEVICE\_CONFIG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	EXT_WD_INPUT_MODE	R/W	0h	External watchdog input source 0h = Watchdog tickle over I2C 1h = Watchdog tickle over GPIO
0	EXT_WD_FAULT_MODE	R/W	0h	External watchdog fault mode 0h = External watchdog fault causes report only but no action is taken; nFAULT is active 1h = External watchdog fault causes latched fault; nFAULT is active; Gate driver is tristated

### 8.3.4 PERI\_CONFIG1 Register (Offset = AAh) [Reset = 40000000h]

PERI\_CONFIG1 is shown in [Figure 8-20](#) and described in [Table 8-26](#).

Return to the [Summary Table](#).

Register to peripheral1

Figure 8-20. PERI\_CONFIG1 Register

31	30	29	28	27	26	25	24
PARITY	SPREAD_SPE CTRUM_MODU LATION_DIS	DIG_DEAD_TIME				CLOCK_FREQUENCY	
R-0h	R/W-1h	R/W-0h				R/W-0h	
23	22	21	20	19	18	17	16
VDC_FILTER	BUS_POWER_ LIMIT_ENABLE	DIR_INPUT		DIR_CHANGE_ MODE	SPEED_LIMIT_ ENABLE	RESERVED	
R/W-0h	R/W-0h	R/W-0h		R/W-0h	R/W-0h	R-0h	
15	14	13	12	11	10	9	8
ACTIVE_BRAKE_SPEED_DELTA_LIMIT_ENTRY		PWM_DITHER_ _MODE	PWM_DITHER_STEP		SPEED_RANG E_SEL	NO_MTR_FLT_ CLOSEDLOOP_ _DIS	
R/W-0h		R/W-0h	R/W-0h		R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
FLUX_WEAKENING_REFEREN CE	CTRL_MODE		SALIENCY_PERCENTAGE				
R/W-0h	R/W-0h		R/W-0h				

Table 8-26. PERI\_CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R	0h	Parity bit
30	SPREAD_SPECTRUM_M ODULATION_DIS	R/W	1h	Spread Spectrum Modulation (SSM) disable 0h = SSM is enabled 1h = SSM is disabled

**Table 8-26. PERI\_CONFIG1 Register Field Descriptions (continued)**

Bit	Field	Type	Reset	Description
29-26	DIG_DEAD_TIME	R/W	0h	PWM dead time configuration 0h = Not Applicable 1h = Not Applicable 2h = 100 ns 3h = 150 ns 4h = 200 ns 5h = 250 ns 6h = 300 ns 7h = 350 ns 8h = 400 ns 9h = 450 ns Ah = 500 ns Bh = 600 ns Ch = 700 ns Dh = 800 ns Eh = 900 ns Fh = 1000 ns
25-24	CLOCK_FREQUENCY	R/W	0h	System clock frequency configuration 0h = High 1h = Medium 2h = Low 3h = Reserved
23-22	VDC_FILTER	R/W	0h	PVDD voltage filter coefficient 0h = Disable 1h = Enable with default filter cut-off frequency 2h = Enable with filter cut-off frequency 100 Hz 3h = Enable with filter cut-off frequency 1000 Hz
21	BUS_POWER_LIMIT_ENABLE	R/W	0h	Bus power limit enable (Limits input DC bus power to MAX_POWER except if CTRL_MODE = 1h) 0h = Disable 1h = Enable
20-19	DIR_INPUT	R/W	0h	Direction (DIR) pin override 0h = Not Applicable 1h = Override DIR pin with clockwise rotation OUTA-OUTB-OUTC 2h = Override DIR pin with counter clockwise rotation OUTA-OUTC-OUTB 3h = Not Applicable
18	DIR_CHANGE_MODE	R/W	0h	Response to direction change command (Refer Figure: Motor Starting-up Flow) 0h = Follow motor stop options and ISD routine on detecting DIR change 1h = Change the direction through reverse drive while continuously driving the motor
17	SPEED_LIMIT_ENABLE	R/W	0h	Motor speed limit enable (Limits motor speed to MAX_SPEED except if CTRL_MODE = 0h) 0h = Disable 1h = Enable
16	RESERVED	R	0h	Reserved
15-13	ACTIVE_BRAKE_SPEED_DELTA_LIMIT_ENTRY	R/W	0h	Difference between final speed and present speed below which active braking will be applied (% of MAX_SPEED) 0h = 20% 1h = 30% 2h = 40% 3h = 50% 4h = 60% 5h = 70% 6h = 80% 7h = 90%
12	PWM_DITHER_MODE	R/W	0h	PWM dither mode 0h = Triangular mode 1h = Random mode

Table 8-26. PERI\_CONFIG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11-10	PWM_DITHER_STEP	R/W	0h	PWM dither step 0h = 1 1h = 2 2h = 5 3h = 10
9	SPEED_RANGE_SEL	R/W	0h	Frequency range selection for PWM duty mode reference input (SPEED_MODE = 1h) 0h = 325 Hz to 100 kHz speed PWM input 1h = 10 Hz to 325 Hz speed PWM input
8	NO_MTR_FLT_CLOSEDLOOP_OOP_DIS	R/W	0h	No motor fault detection enable in closed-loop 0h = Enable No motor fault in closed loop if LOCK2_EN is set to 0x1 1h = Disable No Motor fault in closed loop
7-6	FLUX_WEAKENING_REFERENCE	R/W	0h	Modulation index reference to be tracked in flux weakening mode 0h = 70% 1h = 80% 2h = 90% 3h = 95%
5-4	CTRL_MODE	R/W	0h	Control mode 0h = Speed control 1h = Power control 2h = Current control 3h = Modulation index control
3-0	SALIENCY_PERCENTAGE	R/W	0h	Motor saliency in percentage calculated as $((Lq-Ld) \times 100) / (4 \times (Lq+Ld))$ Example: Lq = 2mH and Ld = 1mH then SALIENCY_PERCENTAGE = 100/12 = 8.33 (Configure 8)

### 8.3.5 GD\_CONFIG1 Register (Offset = ACh) [Reset = 00000000h]

GD\_CONFIG1 is shown in Figure 8-21 and described in Table 8-27.

Return to the [Summary Table](#).

Register to configure gated driver settings1

Figure 8-21. GD\_CONFIG1 Register

31	30	29	28	27	26	25	24
PARITY	RESERVED				BST_CHRG_TIME		
R-0h	R-0h				R/W-0h		
23	22	21	20	19	18	17	16
SNS_FLT_MODE	VDS_FLT_MODE	BST_UV_MODE	GVDD_UV_MODE	AVDD_VOL_SEL	RESERVED	RESERVED	DIS_BST_FLT
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h	R-0h	R/W-0h
15	14	13	12	11	10	9	8
OTS_AUTO_RECCOVERY	RESERVED				DIS_SNS_FLT	DIS_VDS_FLT	
R/W-0h	R-0h				R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
RESERVED	SEL_VDS_LVL			RESERVED	CSA_GAIN		
R-0h	R/W-0h			R-0h	R/W-0h		

Table 8-27. GD\_CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R	0h	Parity bit

**Table 8-27. GD\_CONFIG1 Register Field Descriptions (continued)**

Bit	Field	Type	Reset	Description
30-26	RESERVED	R	0h	Reserved
25-24	BST_CHRG_TIME	R/W	0h	Bootstrap capacitor charging time 0h = 0 ms 1h = 3 ms 2h = 6 ms 3h = 12 ms
23	SNS_FLT_MODE	R/W	0h	Current sense overcurrent fault mode 0h = Current sense overcurrent fault causes latched fault; nFAULT active; Gate driver is tristated 1h = Fault automatically cleared after LCK_RETRY time. Number of retries limited to AUTO_RETRY_TIMES. If number of retries exceed AUTO_RETRY_TIMES, fault is latched; Gate driver is tristated; nFAULT active
22	VDS_FLT_MODE	R/W	0h	VDS overcurrent fault response mode 0h = VDS overcurrent fault causes latched fault; nFAULT active; Gate driver is tristated 1h = Fault automatically cleared after LCK_RETRY time. Number of retries limited to AUTO_RETRY_TIMES. If number of retries exceed AUTO_RETRY_TIMES, fault is latched; Gate driver is tristated; nFAULT active
21	BST_UV_MODE	R/W	0h	Bootstrap undervoltage fault mode 0h = Bootstrap undervoltage fault causes latched fault; nFAULT active; Gate driver is tristated 1h = Fault automatically cleared after LCK_RETRY time. Number of retries limited to AUTO_RETRY_TIMES. If number of retries exceed AUTO_RETRY_TIMES, fault is latched; Gate driver is tristated; nFAULT active
20	GVDD_UV_MODE	R/W	0h	GVDD undervoltage fault mode 0h = GVDD undervoltage fault causes latched fault; nFAULT active; Gate driver is tristated 1h = Fault automatically cleared after LCK_RETRY time. Number of retries limited to AUTO_RETRY_TIMES. If number of retries exceed AUTO_RETRY_TIMES, fault is latched; Gate driver is tristated; nFAULT active
19	AVDD_VOL_SEL	R/W	0h	AVDD voltage level selection 0h = 3.3 V 1h = 5 V
18	RESERVED	R	0h	Reserved
17	RESERVED	R	0h	Reserved
16	DIS_BST_FLT	R/W	0h	Bootstrap fault detection disable 0h = Enable BST fault 1h = Disable BST fault
15	OTS_AUTO_RECOVERY	R/W	0h	Over-temperature shutdown (OTS) auto recovery enable 0h = OTS fault causes latched fault; nFAULT active; Gate driver is tristated 1h = OTS fault clears automatically if (TJ < TOTSD – THYS); Gate driver is tristated; nFAULT active
14-10	RESERVED	R	0h	Reserved
9	DIS_SNS_FLT	R/W	0h	Current sense fault detection disable 0h = Enable SNS OCP fault 1h = Disable SNS OCP fault
8	DIS_VDS_FLT	R/W	0h	VDS fault detection disable 0h = Enable VDS fault 1h = Disable VDS fault
7	RESERVED	R	0h	Reserved

Table 8-27. GD\_CONFIG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-3	SEL_VDS_LVL	R/W	0h	VDS overcurrent protection threshold 0h = 0.06 V 1h = 0.12 V 2h = 0.18 V 3h = 0.24 V 4h = 0.3 V 5h = 0.36 V 6h = 0.42 V 7h = 0.48 V 8h = 0.6 V 9h = 0.8 V Ah = 1 V Bh = 1.2 V Ch = 1.4 V Dh = 1.6 V Eh = 1.8 V Fh = 2 V
2	RESERVED	R	0h	Reserved
1-0	CSA_GAIN	R/W	0h	Current Sense Amplifier (CSA) gain 0h = 5 V/V 1h = 10 V/V 2h = 20 V/V 3h = 40 V/V

### 8.3.6 GD\_CONFIG2 Register (Offset = AEh) [Reset = 00000000h]

GD\_CONFIG2 is shown in [Figure 8-22](#) and described in [Table 8-28](#).

Return to the [Summary Table](#).

Register to configure gated driver settings2

Figure 8-22. GD\_CONFIG2 Register

31	30	29	28	27	26	25	24
PARITY					RESERVED		
R-0h					R-0h		
23	22	21	20	19	18	17	16
				RESERVED			
R-0h					R-0h		
15	14	13	12	11	10	9	8
RESERVED				BASE_CURRENT			
R-0h				R/W-0h			
7	6	5	4	3	2	1	0
			BASE_CURRENT				
R/W-0h							

Table 8-28. GD\_CONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R	0h	Parity bit
30-15	RESERVED	R	0h	Reserved

**Table 8-28. GD\_CONFIG2 Register Field Descriptions (continued)**

Bit	Field	Type	Reset	Description
14-0	BASE_CURRENT	R/W	0h	Base current calculated based on gain settings Base current in Ampere = $1.5 / (RSENSE \times CSA\_GAIN)$ $BASE\_CURRENT = \text{Base current in Ampere} \times 32768 / 1200$ Example: for 30A, enter $30 \times 32768 / 1200 = 820$

## 8.4 Internal\_Algorithm\_Configuration Registers

Table 8-29 lists the memory-mapped registers for the Internal\_Algorithm\_Configuration registers. All register offset addresses not listed in Table 8-29 should be considered as reserved locations and the register contents should not be modified.

**Table 8-29. INTERNAL\_ALGORITHM\_CONFIGURATION Registers**

Offset	Acronym	Register Name	Section
A0h	INT_ALGO_1	Internal Algorithm Configuration1	Section 8.4.1
A2h	INT_ALGO_2	Internal Algorithm Configuration2	Section 8.4.2

Complex bit access types are encoded to fit into small table cells. Table 8-30 shows the codes that are used for access types in this section.

**Table 8-30. Internal\_Algorithm\_Configuration Access Type Codes**

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

### 8.4.1 INT\_ALGO\_1 Register (Offset = A0h) [Reset = 00000000h]

INT\_ALGO\_1 is shown in Figure 8-23 and described in Table 8-31.

Return to the [Summary Table](#).

Register to configure internal algorithm parameters1

**Figure 8-23. INT\_ALGO\_1 Register**

31	30	29	28	27	26	25	24
PARITY	ABNORMAL_BEMF_PERSISTENT_TIME	SPEED_PIN_GLITCH_FILTER	FAST_ISD_EN	ISD_STOP_TIME			
R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h			
23	22	21	20	19	18	17	16
ISD_RUN_TIME	ISD_TIMEOUT		DRY_RUN_TDEG		DRY_RUN_ILIM_FIFTY_PERCENT_SPEED		
R/W-0h	R/W-0h		R/W-0h		R/W-0h		
15	14	13	12	11	10	9	8
DRY_RUN_ILIM_FIFTY_PERCENT_SPEED		DRY_RUN_ILIM					
R/W-0h			R/W-0h				
7	6	5	4	3	2	1	0
DRY_RUN_SPEED_THR	DRY_RUN_ILIM_MODE	DRY_RUN_MODE		REV_DRV_OPEN_LOOP_DEC			
R/W-0h	R/W-0h	R/W-0h		R/W-0h			

**Table 8-31. INT\_ALGO\_1 Register Field Descriptions**

Bit	Field	Type	Reset	Description
31	PARITY	R	0h	Parity bit
30-29	ABNORMAL_BEMF_PERSISTENT_TIME	R/W	0h	Deglitch time for abnormal BEMF fault detection 0h = 2 electrical cycles 1h = 500 ms 2h = 1000 ms 3h = 2000 ms
28-27	SPEED_PIN_GLITCH_FILTER	R/W	0h	Glitch filter applied on SPEED/WAKE pin(Applicable when SPEED_MODE = 1h or SPEED_MODE =3h) 0h = No Glitch Filter 1h = 0.2 $\mu$ s 2h = 0.5 $\mu$ s 3h = 1.0 $\mu$ s
26	FAST_ISD_EN	R/W	0h	Fast speed detection enable during ISD 0h = Disable 1h = Enable
25-24	ISD_STOP_TIME	R/W	0h	Persistence time for declaring motor has stopped during ISD 0h = 1 ms 1h = 5 ms 2h = 50 ms 3h = 100 ms
23-22	ISD_RUN_TIME	R/W	0h	Persistence time for declaring motor is running during ISD 0h = 1 ms 1h = 5 ms 2h = 50 ms 3h = 100 ms
21-20	ISD_TIMEOUT	R/W	0h	Timeout in case ISD is unable to reliably detect speed or direction 0h = 500 ms 1h = 750 ms 2h = 1000 ms 3h = 2000 ms
19-17	DRY_RUN_TDEG	R/W	0h	Dry run fault detection deglitch time 0h = 10 s 1h = 30 s 2h = 1 min 3h = 2 min 4h = 3 min 5h = 5 min 6h = 10 min 7h = 15 min
16-13	DRY_RUN_ILIM_FIFTY_PERCENT_SPEED	R/W	0h	Current limit threshold for dry run detection at 50% of maximum speed (% of ILIMIT) 0h = 5% 1h = 7.5% 2h = 10% 3h = 12.5% 4h = 15% 5h = 17.5% 6h = 20% 7h = 22.5% 8h = 25% 9h = 27.5% Ah = 30% Bh = 32.5% Ch = 35% Dh = 40% Eh = 45% Fh = 50%

Table 8-31. INT\_ALGO\_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12-8	DRY_RUN_ILIM	R/W	0h	Current limit threshold for dry run detection (% of ILIMIT) 0h = 2.5% 1h = 5% 2h = 7.5% 3h = 10% 4h = 12.5% 5h = 15% 6h = 17.5% 7h = 20% 8h = 22.5% 9h = 25% Ah = 27.5% Bh = 30% Ch = 32.5% Dh = 35% Eh = 37.5% Fh = 40% 10h = 42.5% 11h = 45% 12h = 47.5% 13h = 50% 14h = 52.5% 15h = 55% 16h = 57.5% 17h = 60% 18h = 62.5% 19h = 65% 1Ah = 67.5% 1Bh = 70% 1Ch = 72.5% 1Dh = 75% 1Eh = 77.5% 1Fh = 80%
7-6	DRY_RUN_SPEED_THR	R/W	0h	Minimum speed threshold above which enable bit is active for dry run detection (% of MAX_SPEED) 0h = 25% 1h = 40% 2h = 50% 3h = 60%
5	DRY_RUN_ILIM_MODE	R/W	0h	Dry run detection current limit mode 0h = Current limit threshold is constant 1h = Current limit threshold varies with speed
4-3	DRY_RUN_MODE	R/W	0h	Dry run detection fault response mode 0h = Dry run detection is disabled 1h = Dry run detection fault is in report only but no action is taken; nFAULT active 2h = Fault automatically cleared after LCK_RETRY time. Number of retries limited to AUTO_RETRY_TIMES. If number of retries exceed AUTO_RETRY_TIMES, fault is latched; Gate driver is tristated; nFAULT active 3h = Dry run detection fault causes latched fault; nFAULT active; Gate driver is tristated
2-0	REV_DRV_OPEN_LOOP_DEC	R/W	0h	Open-loop deceleration rate in reverse drive (% of open-loop acceleration) 0h = 50% 1h = 60% 2h = 70% 3h = 80% 4h = 90% 5h = 100% 6h = 125% 7h = 150%

#### 8.4.2 INT\_ALGO\_2 Register (Offset = A2h) [Reset = 00000000h]

INT\_ALGO\_2 is shown in [Figure 8-24](#) and described in [Table 8-32](#).

Return to the [Summary Table](#).

Register to configure internal algorithm parameters2

**Figure 8-24. INT\_ALGO\_2 Register**

31	30	29	28	27	26	25	24
PARITY				FLUX_WEAKENING_KP			
R-0h				R/W-0h			
23	22	21	20	19	18	17	16
FLUX_WEAKENING_KP				FLUX_WEAKENING_KI			
R/W-0h				R/W-0h			
15	14	13	12	11	10	9	8
FLUX_WEAKENING_KI				FLUX_WEAKENING_EN		CL_SLOW_ACC	
R/W-0h				R/W-0h		R/W-0h	
7	6	5	4	3	2	1	0
CL_SLOW_ACC	ACTIVE_BRAKE_BUS_CURRENT_SLEW_RATE			EEPROM_LOCK_MODE		DYNAMIC_SA MPLING_EN	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

**Table 8-32. INT\_ALGO\_2 Register Field Descriptions**

Bit	Field	Type	Reset	Description
31	PARITY	R	0h	Parity bit
30-21	FLUX_WEAKENING_KP	R/W	0h	10-bit value for flux weakening Kp FLUX_WEAKENING_KP is divided in 2 sections - SCALE(9:8) and VALUE(7:0) Kp = 0.1 × VALUE / 10^SCALE.
20-11	FLUX_WEAKENING_KI	R/W	0h	10-bit value for flux weakening Ki FLUX_WEAKENING_KI is divided in 2 sections - SCALE(9:8) and VALUE(7:0) Ki = 10.0 × VALUE / 10^SCALE).
10	FLUX_WEAKENING_EN	R/W	0h	Flux weakening enable 0h = Disable 1h = Enable

Table 8-32. INT\_ALGO\_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9-6	CL_SLOW_ACC	R/W	0h	Closed loop acceleration when estimator is not yet fully aligned (Applicable only if CTRL_MODE = 0h) and acceleration/deacceleration during BUS_POWER_LIMIT_ENABLE =1h or SPEED_LIMIT_ENABLE = 1h Speed control (Hz/s) Power control (W/s) Current control (0.1A/s) Modulation index control(0.01% modulation index/s) 0h = 0.1 1h = 1 2h = 2 3h = 3 4h = 5 5h = 10 6h = 20 7h = 30 8h = 40 9h = 50 Ah = 100 Bh = 200 Ch = 500 Dh = 750 Eh = 1000 Fh = 2000
5-3	ACTIVE_BRAKE_BUS_CURRENT_SLEW_RATE	R/W	0h	Active braking bus current slew rate 0h = 10 A/s 1h = 50 A/s 2h = 100 A/s 3h = 250 A/s 4h = 500 A/s 5h = 1000 A/s 6h = 5000 A/s 7h = No Limit
2-1	EEPROM_LOCK_MODE	R/W	0h	EEPROM access lock mode 0h = EEPROM read and write allowed without a valid EEPROM_LOCK_KEY 1h = EEPROM read and write allowed with a valid EEPROM_LOCK_KEY 2h = EEPROM read allowed with a valid EEPROM_LOCK_KEY, write is locked permanently 3h = EEPROM read and write is locked permanently
0	DYNAMIC_SAMPLING_EN	R/W	0h	Dynamic sampling enable 0h = Dynamic sampling is disabled 1h = Dynamic sampling is enabled

## 9 RAM (Volatile) Register Map

## 9.1 Fault\_Status Registers

Table 9-1 lists the memory-mapped registers for the Fault\_Status registers. All register offset addresses not listed in Table 9-1 should be considered as reserved locations and the register contents should not be modified.

Table 9-1. FAULT\_STATUS Registers

Offset	Acronym	Register Name	Section
0h	GATE_DRIVER_FAULT_STATUS	Fault Status Register	Section 9.1.1
2h	CONTROLLER_FAULT_STATUS	Fault Status Register	Section 9.1.2
24Ch	EEPROM_FAULT_STATUS	EEPROM Fault Status Register	Section 9.1.3

Complex bit access types are encoded to fit into small table cells. Table 9-2 shows the codes that are used for access types in this section.

Table 9-2. Fault\_Status Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Reset or Default Value		
-n		Value after reset or the default value

### 9.1.1 GATE\_DRIVER\_FAULT\_STATUS Register (Offset = 0h) [Reset = 00000000h]

GATE\_DRIVER\_FAULT\_STATUS is shown in Figure 9-1 and described in Table 9-3.

Return to the [Summary Table](#).

Status of various gate driver faults

Figure 9-1. GATE\_DRIVER\_FAULT\_STATUS Register

31	30	29	28	27	26	25	24
DRIVER_FAULT	RESERVED	OTS_FAULT	OCP_VDS_FAULT	OCP_SNS_FAULT	BST_UV_FAULT	GVDD_UV_FLT	DRV_OFF
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED	VDS_LC_FAULT	VDS_LB_FAULT	VDS_LA_FAULT	RESERVED	VDS_HC_FAULT	VDS_HB_FAULT	VDS_HA_FAULT
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 9-3. GATE\_DRIVER\_FAULT\_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DRIVER_FAULT	R	0h	Indicates the logical OR of driver fault registers 0h = No Gate Driver fault condition is detected 1h = Gate Driver fault condition is detected
30	RESERVED	R	0h	Reserved

**Table 9-3. GATE\_DRIVER\_FAULT\_STATUS Register Field Descriptions (continued)**

Bit	Field	Type	Reset	Description
29	OTS_FAULT	R	0h	Overtemperature fault 0h = No overtemperature warning / shutdown is detected 1h = Overtemperature warning / shutdown is detected
28	OCP_VDS_FAULT	R	0h	Overcurrent VDS fault status 0h = No VDS fault condition is detected 1h = VDS fault condition is detected
27	OCP_SNS_FAULT	R	0h	Overcurrent sense fault status 0h = No overcurrent sense fault condition is detected 1h = Overcurrent sense fault condition is detected
26	BST_UV_FAULT	R	0h	Bootstrap undervoltage protection status 0h = No BST undervoltage fault condition is detected 1h = BST undervoltage fault condition is detected
25	GVDD_UV_FLT	R	0h	GVDD undervoltage fault status 0h = No GVDD undervoltage fault condition is detected 1h = GVDD undervoltage fault condition is detected
24	DRV_OFF	R	0h	DRV off status 0h = DRV is ON 1h = DRVOFF state detected
23-7	RESERVED	R	0h	Reserved
6	VDS_LC_FAULT	R	0h	VDS fault status on low-side switch of OUTC 0h = No VDS fault detected on low-side switch of OUTC 1h = VDS fault detected on low-side switch of OUTC
5	VDS_LB_FAULT	R	0h	VDS fault status on low-side switch of OUTB 0h = No VDS fault detected on low-side switch of OUTB 1h = VDS fault detected on low-side switch of OUTB
4	VDS_LA_FAULT	R	0h	VDS fault status on low-side switch of OUTA 0h = No VDS fault detected on low-side switch of OUTA 1h = VDS fault detected on low-side switch of OUTA
3	RESERVED	R	0h	Reserved
2	VDS_HC_FAULT	R	0h	VDS fault status on high-side switch of OUTC 0h = No VDS fault detected on high-side switch of OUTC 1h = VDS fault detected on high-side switch of OUTC
1	VDS_HB_FAULT	R	0h	VDS fault status on high-side switch of OUTB 0h = No VDS fault detected on high-side switch of OUTB 1h = VDS fault detected on high-side switch of OUTB
0	VDS_HA_FAULT	R	0h	VDS fault status on high-side switch of OUTA 0h = No VDS fault detected on high-side switch of OUTA 1h = VDS fault detected on high-side switch of OUTA

### 9.1.2 CONTROLLER\_FAULT\_STATUS Register (Offset = 2h) [Reset = 00000000h]

CONTROLLER\_FAULT\_STATUS is shown in [Figure 9-2](#) and described in [Table 9-4](#).

Return to the [Summary Table](#).

Status of various controller faults

**Figure 9-2. CONTROLLER\_FAULT\_STATUS Register**

31	30	29	28	27	26	25	24
CONTROLLER_FAULT	RESERVED	RESERVED	RESERVED	NO_MTR_PHA_SE_C	NO_MTR_PHA_SE_B	NO_MTR_PHA_SE_A	MPET_BEMF_FAULT
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
23	22	21	20	19	18	17	16
ABN_SPEED	ABN_BEMF	NO_MTR	MTR_LCK	LOCK_LIMIT	HW_LOCK_LIMIT	DCBUS_UNDER_VOLTAGE	DCBUS_OVER_VOLTAGE

Figure 9-2. CONTROLLER\_FAULT\_STATUS Register (continued)

R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
15	14	13	12	11	10	9	8
SPEED_LOOP_SATURATION	CURRENT_LOOP_SATURATION	MAX_SPEED_SATURATION	BUS_POWER_LIMIT_SATURATION	EEPROM_WRITE_LOCK_SET	EEPROM_READ_LOCK_SET	DRY_RUN_DETECTION_STATUS	RESERVED
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
RESERVED	I2C_CRC_FAULT_STATUS	EEPROM_ERR_STATUS	RESERVED	WATCHDOG_FAULT	RESERVED	RESERVED	RESERVED
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 9-4. CONTROLLER\_FAULT\_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CONTROLLER_FAULT	R	0h	Indicates the logical OR of controller fault status registers
30	RESERVED	R	0h	Reserved
29	RESERVED	R	0h	Reserved
28	RESERVED	R	0h	Reserved
27	NO_MTR_PHASE_C	R	0h	Indicates loss of Phase C causes no motor fault
26	NO_MTR_PHASE_B	R	0h	Indicates loss of Phase B causes no motor fault
25	NO_MTR_PHASE_A	R	0h	Indicates loss of Phase A causes no motor fault
24	MPET_BEMF_FAULT	R	0h	Indicates an error during BEMF constant measurement
23	ABN_SPEED	R	0h	Indicates abnormal speed motor lock condition
22	ABN_BEMF	R	0h	Indicates abnormal BEMF motor lock condition
21	NO_MTR	R	0h	Indicates no motor (loss of phase) fault
20	MTR_LCK	R	0h	Indicates when one of the motor lock (abnormal BEMF/speed, no motor) is triggered
19	LOCK_LIMIT	R	0h	Indicates Lock limit fault
18	HW_LOCK_LIMIT	R	0h	Indicates Hardware lock limit fault
17	DCBUS_UNDER_VOLTAGE	R	0h	Indicates configurable under voltage fault on PVDD
16	DCBUS_OVER_VOLTAGE	R	0h	Indicates configurable over voltage fault on PVDD
15	SPEED_LOOP_SATURATION	R	0h	Indicates speed loop saturation
14	CURRENT_LOOP_SATURATION	R	0h	Indicates current loop saturation
13	MAX_SPEED_SATURATION	R	0h	Indicates maximum speed limit saturation
12	BUS_POWER_LIMIT_SATURATION	R	0h	Indicates maximum (input DC bus) power limit saturation
11	EEPROM_WRITE_LOCK_SET	R	0h	Indicates EEPROM write lock is set
10	EEPROM_READ_LOCK_SET	R	0h	Indicates EEPROM read lock is set
9	DRY_RUN_DETECTION_STATUS	R	0h	Indicates dry run detection
8-7	RESERVED	R	0h	Reserved
6	I2C_CRC_FAULT_STATUS	R	0h	Indicates CRC fault in I2C packet
5	EEPROM_ERR_STATUS	R	0h	Indicates error in EEPROM

**Table 9-4. CONTROLLER\_FAULT\_STATUS Register Field Descriptions (continued)**

Bit	Field	Type	Reset	Description
4	RESERVED	R	0h	Reserved
3	WATCHDOG_FAULT	R	0h	indicates Watchdog fault
2	RESERVED	R	0h	Reserved
1	RESERVED	R	0h	Reserved
0	RESERVED	R	0h	Reserved

### 9.1.3 EEPROM\_FAULT\_STATUS Register (Offset = 24Ch) [Reset = 0000h]

EEPROM\_FAULT\_STATUS is shown in [Figure 9-3](#) and described in [Table 9-5](#).

Return to the [Summary Table](#).

EEPROM Fault Status Register

**Figure 9-3. EEPROM\_FAULT\_STATUS Register**

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED		EEPROM_CRC_FLT_STS		RESERVED		EEPROM_PARITY_FLT_STS	
R-0h		R-0h		R-0h		R-0h	
R-0h		R-0h		R-0h		R-0h	

**Table 9-5. EEPROM\_FAULT\_STATUS Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-5	RESERVED	R	0h	Reserved
4	EEPROM_CRC_FLT_STS	R	0h	EEPROM CRC error fault status 0h = EEPROM CRC Error fault condition is not detected 1h = EEPROM CRC Error fault condition is detected
3	RESERVED	R	0h	Reserved
2	EEPROM_PARITY_FLT_STS	R	0h	EEPROM parity error fault status 0h = EEPROM Parity error fault condition is not detected 1h = EEPROM Parity error fault condition is detected
1	RESERVED	R	0h	Reserved
0	RESERVED	R	0h	Reserved

## 9.2 System\_Status Registers

Table 9-6 lists the memory-mapped registers for the System\_Status registers. All register offset addresses not listed in Table 9-6 should be considered as reserved locations and the register contents should not be modified.

Table 9-6. SYSTEM\_STATUS Registers

Offset	Acronym	Register Name	Section
E4h	ALGO_STATUS	System Status Register	Section 9.2.1
E6h	MTR_PARAMS	System Status Register	Section 9.2.2
E8h	ALGO_STATUS_MPET	System Status Register	Section 9.2.3

Complex bit access types are encoded to fit into small table cells. Table 9-7 shows the codes that are used for access types in this section.

Table 9-7. System\_Status Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Reset or Default Value		
-n		Value after reset or the default value

### 9.2.1 ALGO\_STATUS Register (Offset = E4h) [Reset = 00000000h]

ALGO\_STATUS is shown in Figure 9-4 and described in Table 9-8.

Return to the [Summary Table](#).

Status of various system and algorithm parameters

Figure 9-4. ALGO\_STATUS Register

31	30	29	28	27	26	25	24
VOLT_MAG							
R-0h							
23	22	21	20	19	18	17	16
VOLT_MAG							
R-0h							
15	14	13	12	11	10	9	8
DUTY_CMD							
R-0h							
7	6	5	4	3	2	1	0
DUTY_CMD				RESERVED	SYS_ENABLE_FLAG	RESERVED	
R-0h				R-0h	R-0h	R-0h	

Table 9-8. ALGO\_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	VOLT_MAG	R	0h	16-bit value indicating the applied modulation index. Modulation index applied = (VOLT_MAG * 100 / 32768)%
15-4	DUTY_CMD	R	0h	12-bit value indicating input duty command in PWM/analog/frequency mode DUTY_CMD (%) = (DUTY_CMD/4095 * 100)%.

**Table 9-8. ALGO\_STATUS Register Field Descriptions (continued)**

Bit	Field	Type	Reset	Description
3	RESERVED	R	0h	Reserved
2	SYS_ENABLE_FLAG	R	0h	1 indicates GUI can control the register 0 indicates GUI is still copying default parameters from shadow memory
1-0	RESERVED	R	0h	Reserved

### 9.2.2 MTR\_PARAMS Register (Offset = E6h) [Reset = 00000000h]

MTR\_PARAMS is shown in [Figure 9-5](#) and described in [Table 9-9](#).

Return to the [Summary Table](#).

Status of various motor parameters

**Figure 9-5. MTR\_PARAMS Register**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								MOTOR_BEMF_CONST							
R-0h								R-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								RESERVED							
R-0h								R-0h							

**Table 9-9. MTR\_PARAMS Register Field Descriptions**

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-16	MOTOR_BEMF_CONST	R	0h	8-bit value indicating measured BEMF constant
15-8	RESERVED	R	0h	Reserved
7-0	RESERVED	R	0h	Reserved

### 9.2.3 ALGO\_STATUS\_MPET Register (Offset = E8h) [Reset = 00000000h]

ALGO\_STATUS\_MPET is shown in [Figure 9-6](#) and described in [Table 9-10](#).

Return to the [Summary Table](#).

Status of various MPET parameters

**Figure 9-6. ALGO\_STATUS\_MPET Register**

31	30	29	28	27	26	25	24
RESERVED	RESERVED	MPET_KE_STA_TUS	MPET_MECH_STATUS	RESERVED			
R-0h	R-0h	R-0h	R-0h	R-0h			
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							

Figure 9-6. ALGO\_STATUS\_MPET Register (continued)

R-0h

Table 9-10. ALGO\_STATUS\_MPET Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	RESERVED	R	0h	Reserved
29	MPET_KE_STATUS	R	0h	Indicates status of BEMF constant measurement 0h = Measurement of motor BEMF constant during MPET routine is not completed if BEMF constant measurement is initiated during MPET 1h = Measurement of motor BEMF constant during MPET routine is completed
28	MPET_MECH_STATUS	R	0h	Indicates status of mechanical parameter measurement 0h = Auto Calculation of Speed loop Kp, Ki values during MPET routine is not completed if mechanical parameters measurement(speed loop Kp, Ki values) is initiated during MPET 1h = Auto Calculation of Speed loop Kp, Ki values during MPET routine is completed
27-24	RESERVED	R	0h	Reserved
23-0	RESERVED	R	0h	Reserved

### 9.3 Algorithm\_Control Registers

Table 9-11 lists the memory-mapped registers for the Algorithm\_Control registers. All register offset addresses not listed in Table 9-11 should be considered as reserved locations and the register contents should not be modified.

**Table 9-11. ALGORITHM\_CONTROL Registers**

Offset	Acronym	Register Name	Section
ECh	ALGO_DEBUG1	Algorithm Control Register	Section 9.3.1
EEh	ALGO_DEBUG2	Algorithm Control Register	Section 9.3.2
F0h	CURRENT_PI	Current PI Controller used	Section 9.3.3
F2h	SPEED_PI	Speed PI controller used	Section 9.3.4
F4h	DAC_1	DAC1 Control Register	Section 9.3.5
F6h	EEPROM_SECURITY	EEPROM Security Control Register	Section 9.3.6

Complex bit access types are encoded to fit into small table cells. Table 9-12 shows the codes that are used for access types in this section.

**Table 9-12. Algorithm\_Control Access Type Codes**

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

#### 9.3.1 ALGO\_DEBUG1 Register (Offset = ECh) [Reset = 00000000h]

ALGO\_DEBUG1 is shown in Figure 9-7 and described in Table 9-13.

Return to the [Summary Table](#).

Algorithm control register for debug

**Figure 9-7. ALGO\_DEBUG1 Register**

31	30	29	28	27	26	25	24
OVERRIDE	DIGITAL_SPEED_CTRL						
R/W-0h	R/W-0h						
23	22	21	20	19	18	17	16
DIGITAL_SPEED_CTRL							
R/W-0h							
15	14	13	12	11	10	9	8
CLOSED_LOO_P_DIS	FORCE_ALIGN_EN	RESERVED	FORCE_IPD_EN	FORCE_ISD_EN	RESERVED	RESERVED	
R/W-0h	R/W-0h	R-0h	R/W-0h	R/W-0h	R-0h	R-0h	
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

Table 9-13. ALGO\_DEBUG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	OVERRIDE	R/W	0h	Use to control the reference input mode. If OVERRIDE = 0x1, reference command can be written by the user through I2C interface irrespective of SPEED_MODE setting. 0h = Reference input mode based on SPEED_MODE 1h = Reference input mode is Register override mode by using DIGITAL_SPEED_CTRL
30-16	DIGITAL_SPEED_CTRL	R/W	0h	Reference input when OVERRIDE is set 0x1 or SPEED_MODE is set to 0x2. Reference input = (DIGITAL_SPEED_CTRL/32768 *100)%
15	CLOSED_LOOP_DIS	R/W	0h	Use to disable closed loop 0h = Enable Closed Loop 1h = Disable Closed loop, motor commutation in open loop
14	FORCE_ALIGN_EN	R/W	0h	Force align state enable 0h = Disable Force Align state, device comes out of align state if MTR_STARTUP is selected as ALIGN or DOUBLE ALIGN 1h = Enable Force Align state, device stays in align state if MTR_STARTUP is selected as ALIGN or DOUBLE ALIGN
13	RESERVED	R	0h	Reserved
12	FORCE_IPD_EN	R/W	0h	Force IPD enable 0h = Disable Force IPD state, device comes out of IPD state if MTR_STARTUP is selected as IPD 1h = Enable Force IPD state, device stays in IPD state if MTR_STARTUP is selected as IPD
11	FORCE_ISD_EN	R/W	0h	Force ISD enable 0h = Disable Force ISD state, device comes out of ISD state if ISD_EN is set 1h = Enable Force ISD state, device stays in ISD state if ISD_EN is set
10	RESERVED	R	0h	Reserved
9-0	RESERVED	R	0h	Reserved

### 9.3.2 ALGO\_DEBUG2 Register (Offset = EEh) [Reset = 00000000h]

ALGO\_DEBUG2 is shown in [Figure 9-8](#) and described in [Table 9-14](#).

Return to the [Summary Table](#).

Algorithm control register for debug

Figure 9-8. ALGO\_DEBUG2 Register

31	30	29	28	27	26	25	24
RESERVED	RESERVED			RESERVED	CURRENT_LO_OP_DIS	FORCE_VD_CURRENT_LOOP_DIS	
R-0h	R-0h			R-0h	R/W-0h	R/W-0h	
23	22	21	20	19	18	17	16
FORCE_VD_CURRENT_LOOP_DIS							
R/W-0h							
15	14	13	12	11	10	9	8
FORCE_VQ_CURRENT_LOOP_DIS							
R/W-0h							
7	6	5	4	3	2	1	0
FORCE_VQ_CURRENT_LOOP_DIS	MPET_CMD	RESERVED	RESERVED	MPET_KE	MPET_MECH	MPET_WRITE_SHADOW	
R/W-0h	R/W-0h	R-0h	R-0h	R/W-0h	R/W-0h	R/W-0h	

**Figure 9-8. ALGO\_DEBUG2 Register (continued)**
**Table 9-14. ALGO\_DEBUG2 Register Field Descriptions**

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30-28	RESERVED	R	0h	Reserved
27	RESERVED	R	0h	Reserved
26	CURRENT_LOOP_DIS	R/W	0h	Use to control FORCE_VD_CURRENT_LOOP_DIS and FORCE_VQ_CURRENT_LOOP_DIS. If CURRENT_LOOP_DIS = '1', Current loop and speed loop are disabled 0h = Enable Current Loop 1h = Disable Current Loop
25-16	FORCE_VD_CURRENT_LOOP_DIS	R/W	0h	Sets Vd when current loop and speed loop are disabled If CURRENT_LOOP_DIS = 0b1, then Vd is control using FORCE_VD_CURRENT_LOOP_DIS mqRef = (FORCE_VD_CURRENT_LOOP_DIS /500) if FORCE_VD_CURRENT_LOOP_DIS < 500 (FORCE_VD_CURRENT_LOOP_DIS - 1024)/500 if FORCE_VD_CURRENT_LOOP_DIS > 524 Valid values: 0 to 500 and 524 to 1024
15-6	FORCE_VQ_CURRENT_LOOP_DIS	R/W	0h	Sets Vq when current loop and speed loop are disabled If CURRENT_LOOP_DIS = 0b1, then Vq is control using FORCE_VQ_CURRENT_LOOP_DIS mqRef = (FORCE_VQ_CURRENT_LOOP_DIS /500) if FORCE_VQ_CURRENT_LOOP_DIS < 500 (FORCE_VQ_CURRENT_LOOP_DIS - 1024)/500 if FORCE_VQ_CURRENT_LOOP_DIS > 524 Valid values: 0 to 500 and 524 to 1024
5	MPET_CMD	R/W	0h	Initiates motor parameter measurement routine when set to 1
4	RESERVED	R	0h	Reserved
3	RESERVED	R	0h	Reserved
2	MPET_KE	R/W	0h	Enables motor BEMF constant measurement during motor parameter measurement routine 0h = Disables Motor BEMF constant measurement during motor parameter measurement routine 1h = Enable Motor BEMF constant measurement during motor parameter measurement routine
1	MPET_MECH	R/W	0h	Enables motor mechanical parameter measurement during motor parameter measurement routine 0h = Disables Motor mechanical parameter measurement during motor parameter measurement routine 1h = Enable Motor mechanical parameter measurement during motor parameter measurement routine
0	MPET_WRITE_SHADOW	R/W	0h	Write measured parameters to shadow register when set to 0x1

### 9.3.3 CURRENT\_PI Register (Offset = F0h) [Reset = 00000000h]

CURRENT\_PI is shown in [Figure 9-9](#) and described in [Table 9-15](#).

Return to the [Summary Table](#).

Current PI controller used

**Figure 9-9. CURRENT\_PI Register**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CURRENT_LOOP_KI																CURRENT_LOOP_KP															
R-0h																R-0h															

**Table 9-15. CURRENT\_PI Register Field Descriptions**

Bit	Field	Type	Reset	Description
31-16	CURRENT_LOOP_KI	R	0h	10 bit value for current loop Ki Same Scaling as CURR_LOOP_KI
15-0	CURRENT_LOOP_KP	R	0h	10 bit value for current loop Kp Same Scaling as CURR_LOOP_KP

### 9.3.4 SPEED\_PI Register (Offset = F2h) [Reset = 00000000h]

SPEED\_PI is shown in [Figure 9-10](#) and described in [Table 9-16](#).

Return to the [Summary Table](#).

Speed PI controller used

**Figure 9-10. SPEED\_PI Register**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPEED_LOOP_KI															SPEED_LOOP_KP																
R-0h															R-0h																

**Table 9-16. SPEED\_PI Register Field Descriptions**

Bit	Field	Type	Reset	Description
31-16	SPEED_LOOP_KI	R	0h	10 bit value for Speed loop Ki Same Scaling as SPD_LOOP_KI
15-0	SPEED_LOOP_KP	R	0h	10 bit value for Speed loop Kp Same Scaling as SPD_LOOP_KP

### 9.3.5 DAC\_1 Register (Offset = F4h) [Reset = 00000000h]

DAC\_1 is shown in [Figure 9-11](#) and described in [Table 9-17](#).

Return to the [Summary Table](#).

DAC1 Control Register

**Figure 9-11. DAC\_1 Register**

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED			DACOUT1_ENUM_SCALING				DACOUT1_SCALING
R-0h			R/W-0h				R/W-0h
15	14	13	12	11	10	9	8
DACOUT1_SCALING			DACOUT1_UNI_POLAR	DACOUT1_VAR_ADDR			
R/W-0h			R/W-0h				R/W-0h
7	6	5	4	3	2	1	0
DACOUT1_VAR_ADDR							
R/W-0h							

**Table 9-17. DAC\_1 Register Field Descriptions**

Bit	Field	Type	Reset	Description
31-21	RESERVED	R	0h	Reserved

**Table 9-17. DAC\_1 Register Field Descriptions (continued)**

Bit	Field	Type	Reset	Description
20-17	DACOUT1_ENUM_SCALING	R/W	0h	Multiplication factor for DACOUT1 Algorithm variable extracted from the address contained in DACOUT1_VAR_ADDR multiplied with $2^{\text{DACOUT1\_ENUM\_SCALING}}$ . DACOUT1_ENUM_SCALING comes into effect only if DACOUT1_SCALING is 0x0
16-13	DACOUT1_SCALING	R/W	0h	Scaling factor for DACOUT1 Algorithm Variable extracted from the address contained in DACOUT1_VAR_ADDR scaled with DACOUT1_SCALING. Actual voltage depends on DACOUT1_UNIPOLAR. If DACOUT1_UNIPOLAR = 0x1, Actual Value= $((\text{DAC voltage} * \text{Per-unit base value}) / (3 * \text{DACOUT1\_SCALING}))$ If DACOUT1_UNIPOLAR = 0x0, Actual Value= $((\text{DAC voltage} - 1.5) * \text{Per-unit base value}) / ((1.5 * \text{DACOUT1\_SCALING}))$ Per-unit current base is 0.0375/Rsense (Rsense is current sense resistor in Ohms) A, Per-unit speed base is MAX_SPEED in Hz, Per-unit voltage base for DC Bus voltage is 60V, Per-unit voltage base for phase voltages is 60V/Sqrt(3) Note: For currents recommended DACOUT1_SCALING is 2/8, for voltages 8/8 and for speed information 7/8 0h = Treated as Enum with max value being 31 1h = 1 / 8 2h = 2 / 8 3h = 3 / 8 4h = 4 / 8 5h = 5 / 8 6h = 6 / 8 7h = 7 / 8 8h = 8 / 8 9h = 9 / 8 Ah = 10 / 8 Bh = 11 / 8 Ch = 12 / 8 Dh = 13 / 8 Eh = 14 / 8 Fh = 15 / 8
12	DACOUT1_UNIPOLAR	R/W	0h	Configures output of DACOUT1 If DACOUT2_UNIPOLAR = 0x1, Actual Value= $((\text{DAC2 voltage} * \text{Per-unit base value}) / (3 * \text{DACOUT2\_SCALING}))$ If DACOUT2_UNIPOLAR = 0x0, Actual Value= $((\text{DAC2 voltage} - 1.5) * \text{Per-unit base value}) / ((1.5 * \text{DACOUT2\_SCALING}))$ Per-unit current base is 0.0375/Rsense (Rsense is current sense resistor in Ohms) A, Per-unit speed base is MAX_SPEED in Hz, Per-unit voltage base for DC Bus voltage is 60V, Per-unit voltage base for phase voltages is 60V/Sqrt(3) Note: For currents recommended DACOUT1_SCALING is 2/8, for voltages 8/8 and for speed information 7/8 0h = Bipolar (Offset of 1.5 V) 1h = Unipolar (No Offset)
11-0	DACOUT1_VAR_ADDR	R/W	0h	12-bit address of variable to be monitored

### 9.3.6 EEPROM\_SECURITY Register (Offset = F6h) [Reset = 0000h]

EEPROM\_SECURITY is shown in Figure 9-12 and described in Table 9-18.

Return to the [Summary Table](#).

EEPROM Security Control Register

**Figure 9-12. EEPROM\_SECURITY Register**

15	14	13	12	11	10	9	8
RESERVED	USER_EEPROM_KEY						

**Figure 9-12. EEPROM\_SECURITY Register (continued)**

R-0h								R/W-0h	
7	6	5	4	3	2	1	0		
USER_EEPROM_KEY									
								R/W-0h	

**Table 9-18. EEPROM\_SECURITY Register Field Descriptions**

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14-0	USER_EEPROM_KEY	R/W	0h	User input key to unlock EEPROM for read/writes. Value in EEPROM_LOCK_KEY should be written here for unlocking EEPROM

## 9.4 Device\_Control Registers

Table 9-19 lists the memory-mapped registers for the Device\_Control registers. All register offset addresses not listed in Table 9-19 should be considered as reserved locations and the register contents should not be modified.

**Table 9-19. DEVICE\_CONTROL Registers**

Offset	Acronym	Register Name	Section
EAh	ALGO_CTRL1	Device Control Register	Section 9.4.1

Complex bit access types are encoded to fit into small table cells. Table 9-20 shows the codes that are used for access types in this section.

**Table 9-20. Device\_Control Access Type Codes**

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

### 9.4.1 ALGO\_CTRL1 Register (Offset = EAh) [Reset = 00000000h]

ALGO\_CTRL1 is shown in Figure 9-13 and described in Table 9-21.

Return to the [Summary Table](#).

Control settings

**Figure 9-13. ALGO\_CTRL1 Register**

31	30	29	28	27	26	25	24
EEPROM_WRT	EEPROM_READ	CLR_FLT	CLR_FLT_RET RY_COUNT	EEPROM_WRITE_ACCESS_KEY			
R/W-0h	R/W-0h	W-0h	W-0h	R/W-0h			
23	22	21	20	19	18	17	16
EEPROM_WRITE_ACCESS_KEY				RESERVED			
R/W-0h				R-0h			
15	14	13	12	11	10	9	8
RESERVED				WATCHDOG_T ICKLE	RESERVED	RESERVED	RESERVED
R-0h				W-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
RESERVED				RESERVED			
R-0h				R-0h			

**Table 9-21. ALGO\_CTRL1 Register Field Descriptions**

Bit	Field	Type	Reset	Description
31	EEPROM_WRT	R/W	0h	Write the configuration from RAM/shadow to EEPROM
30	EEPROM_READ	R/W	0h	Read the default configuration from EEPROM to RAM/shadow
29	CLR_FLT	W	0h	Clears all faults

**Table 9-21. ALGO\_CTRL1 Register Field Descriptions (continued)**

Bit	Field	Type	Reset	Description
28	CLR_FLT_RETRY_COUN T	W	0h	Clears automatic fault retry count
27-20	EEPROM_WRITE_ACCE SS_KEY	R/W	0h	EEPROM write access key (0xA5)
19-11	RESERVED	R	0h	Reserved
10	WATCHDOG_TICKLE	W	0h	RAM bit to tickle watchdog in I2C mode. 0x1 should be written to this bit by external controller every EXT_WDT_CFG. Device will reset this bit to 0x0.
9	RESERVED	R	0h	Reserved
8-1	RESERVED	R	0h	Reserved
0	RESERVED	R	0h	Reserved

## 9.5 Algorithm\_Variables Registers

**Table 9-22** lists the memory-mapped registers for the Algorithm\_Variables registers. All register offset addresses not listed in **Table 9-22** should be considered as reserved locations and the register contents should not be modified.

**Table 9-22. ALGORITHM\_VARIABLES Registers**

Offset	Acronym	Register Name	Section
18Ch	ALGORITHM_STATE	Current Algorithm State Register	<a href="#">Section 9.5.1</a>
190h	FG_SPEED_FDBK	FG Speed Feedback Register	<a href="#">Section 9.5.2</a>
192h	HALL_SPEED_FDBK	Hall Input Speed Feedback Register	<a href="#">Section 9.5.3</a>
42Eh	BUS_CURRENT	Calculated DC Bus Current Register	<a href="#">Section 9.5.4</a>
460h	PHASE_CURRENT_A	Measured Current on Phase A Register	<a href="#">Section 9.5.5</a>
462h	PHASE_CURRENT_B	Measured Current on Phase B Register	<a href="#">Section 9.5.6</a>
464h	PHASE_CURRENT_C	Measured Current on Phase C Register	<a href="#">Section 9.5.7</a>
479h	CSA_GAIN_FEEDBACK	CSA Gain Register	<a href="#">Section 9.5.8</a>
47Dh	VOLTAGE_GAIN_FEEDBACK	Voltage Gain Register	<a href="#">Section 9.5.9</a>
482h	PVDD_VOLTAGE	PVDD Voltage Register	<a href="#">Section 9.5.10</a>
48Ah	PHASE_VOLTAGE_VA	Phase A Voltage Register	<a href="#">Section 9.5.11</a>
48Ch	PHASE_VOLTAGE_VB	Phase B Voltage Register	<a href="#">Section 9.5.12</a>
48Eh	PHASE_VOLTAGE_VC	Phase C Voltage Register	<a href="#">Section 9.5.13</a>
4D8h	SIN_COMMUTATION_ANGLE	Sine of Commutation Angle	<a href="#">Section 9.5.14</a>
4DAh	COS_COMMUTATION_ANGLE	Cosine of Commutation Angle	<a href="#">Section 9.5.15</a>
504h	IALPHA	IALPHA Current Register	<a href="#">Section 9.5.16</a>
506h	IBETA	IBETA Current Register	<a href="#">Section 9.5.17</a>
508h	VALPHA	VALPHA Voltage Register	<a href="#">Section 9.5.18</a>
50Ah	VBETA	VBETA Voltage Register	<a href="#">Section 9.5.19</a>
514h	ID	Measured d-axis Current Register	<a href="#">Section 9.5.20</a>
516h	IQ	Measured q-axis Current Register	<a href="#">Section 9.5.21</a>
518h	VD	VD Voltage Register	<a href="#">Section 9.5.22</a>
51Ah	VQ	VQ Voltage Register	<a href="#">Section 9.5.23</a>
54Ch	IQ_REF_ROTOR_ALIGN	Align Current Reference	<a href="#">Section 9.5.24</a>
560h	SPEED_REF_OPEN_LOOP	Open Loop Speed Register	<a href="#">Section 9.5.25</a>
56Eh	IQ_REF_OPEN_LOOP	Open Loop Current Reference	<a href="#">Section 9.5.26</a>
5EEh	SPEED_REF_CLOSED_LOOP	Speed Reference Register	<a href="#">Section 9.5.27</a>
628h	POWER_FEED_BACK	Power Feedback	<a href="#">Section 9.5.28</a>
630h	ID_REF_CLOSED_LOOP	Reference for d-axis Current loop Register	<a href="#">Section 9.5.29</a>
632h	IQ_REF_CLOSED_LOOP	Reference q-axis for Current loop Register	<a href="#">Section 9.5.30</a>
6F0h	ISD_STATE	ISD State Register	<a href="#">Section 9.5.31</a>
6FAh	ISD_SPEED	ISD Speed Register	<a href="#">Section 9.5.32</a>
724h	IPD_STATE	IPD State Register	<a href="#">Section 9.5.33</a>
746h	IPD_ANGLE	Calculated IPD Angle Register	<a href="#">Section 9.5.34</a>
772h	ED	Estimated BEMF EQ Register	<a href="#">Section 9.5.35</a>
774h	EQ	Estimated BEMF ED Register	<a href="#">Section 9.5.36</a>
784h	SPEED_FDBK	Speed Feedback Register	<a href="#">Section 9.5.37</a>
788h	THETA_EST	Estimated rotor Position Register	<a href="#">Section 9.5.38</a>

Complex bit access types are encoded to fit into small table cells. [Table 9-23](#) shows the codes that are used for access types in this section.

**Table 9-23. Algorithm\_Variables Access Type Codes**

Access Type	Code	Description
Read Type		
R	R	Read
Reset or Default Value		
-n		Value after reset or the default value

### 9.5.1 ALGORITHM\_STATE Register (Offset = 18Ch) [Reset = 0000h]

ALGORITHM\_STATE is shown in [Figure 9-14](#) and described in [Table 9-24](#).

Return to the [Summary Table](#).

Current Algorithm State Register

**Figure 9-14. ALGORITHM\_STATE Register**

15	14	13	12	11	10	9	8
ALGORITHM_STATE							
R-0h							
7	6	5	4	3	2	1	0
ALGORITHM_STATE							
R-0h							

**Table 9-24. ALGORITHM\_STATE Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-0	ALGORITHM_STATE	R	0h	16-bit value indicating current state of device 00h = MOTOR_IDLE 01h = MOTOR_ISD 02h = MOTOR_TRISTATE 03h = MOTOR_BRAKE_ON_START 04h = MOTOR_IPD 05h = MOTOR_SLOW_FIRST_CYCLE 06h = MOTOR_ALIGN 07h = MOTOR_OPEN_LOOP 08h = MOTOR_CLOSED_LOOP_UNALIGNED 09h = MOTOR_CLOSED_LOOP_ALIGNED 0Ah = MOTOR_CLOSED_LOOP_ACTIVE_BRACING 0Bh = MOTOR_SOFT_STOP 0Ch = RESERED 0Dh = MOTOR_BRAKE_ON_STOP 0Eh = MOTOR_FAULT 0Fh = MOTOR_MPET_MOTOR_STOP_CHECK 10h = MOTOR_MPET_MOTOR_STOP_WAIT 11h = MOTOR_MPET_MOTOR_BRAKE 12h = MOTOR_MPET_ALGORITHM_PARAMETERS_INIT 13h = RESERED 14h = MOTOR_MPET_KE_MEASURE 15h = MOTOR_MPET_STALL_CURRENT_MEASURE 16h = MOTOR_MPET_TORQUE_MODE 17h = MOTOR_MPET_DONE 18h = MOTOR_MPET_FAULT

### 9.5.2 FG\_SPEED\_FDBK Register (Offset = 190h) [Reset = 00000000h]

FG\_SPEED\_FDBK is shown in [Figure 9-15](#) and described in [Table 9-25](#).

Return to the [Summary Table](#).

Speed Feedback from FG

**Figure 9-15. FG\_SPEED\_FDBK Register**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FG_SPEED_FDBK																															
R-0h																															

**Table 9-25. FG\_SPEED\_FDBK Register Field Descriptions**

Bit	Field	Type	Reset	Description
31-0	FG_SPEED_FDBK	R	0h	32-bit value indicating absolute (unsigned) value of estimated motor speed based on FG Estimated motor speed (in Hz) = (FG_SPEED_FDBK / 2 <sup>27</sup> ) * MAX_SPEED (in Hz)

### 9.5.3 HALL\_SPEED\_FDBK Register (Offset = 192h) [Reset = 00000000h]

HALL\_SPEED\_FDBK is shown in [Figure 9-16](#) and described in [Table 9-26](#).

Return to the [Summary Table](#).

Speed Feedback based on Hall Input

**Figure 9-16. HALL\_SPEED\_FDBK Register**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HALL_SPEED_FDBK																															
R-0h																															

**Table 9-26. HALL\_SPEED\_FDBK Register Field Descriptions**

Bit	Field	Type	Reset	Description
31-0	HALL_SPEED_FDBK	R	0h	32-bit value indicating absolute (unsigned) value of estimated motor speed based on Hall Input Estimated motor speed (in Hz) = (HALL_SPEED_FDBK / 2 <sup>27</sup> ) * MAX_SPEED (in Hz)

### 9.5.4 BUS\_CURRENT Register (Offset = 42Eh) [Reset = 00000000h]

BUS\_CURRENT is shown in [Figure 9-17](#) and described in [Table 9-27](#).

Return to the [Summary Table](#).

Calculated Supply Current Register

**Figure 9-17. BUS\_CURRENT Register**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BUS_CURRENT																															
R-0h																															

Table 9-27. BUS\_CURRENT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	BUS_CURRENT	R	0h	32-bit signed value indicating DC bus current. Negative value represented in two's complement DC bus current (in Amps) = (BUS_CURRENT / 2 <sup>27</sup> ) * Per-unit current base Per-unit current base is 0.0375/Rsense (Rsense is current sense resistor in Ohms) A

#### 9.5.5 PHASE\_CURRENT\_A Register (Offset = 460h) [Reset = 00000000h]

PHASE\_CURRENT\_A is shown in Figure 9-18 and described in Table 9-28.

Return to the [Summary Table](#).

Measured current on Phase A Register

Figure 9-18. PHASE\_CURRENT\_A Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHASE_CURRENT_A																															
R-0h																															

Table 9-28. PHASE\_CURRENT\_A Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHASE_CURRENT_A	R	0h	32-bit signed value indicating measured continuous Phase A current. Negative value represented in two's complement Phase A current (in Amps) = (PHASE_CURRENT_A / 2 <sup>27</sup> ) * Per-unit current base Per-unit current base is 0.0375/Rsense (Rsense is current sense resistor in Ohms) A

#### 9.5.6 PHASE\_CURRENT\_B Register (Offset = 462h) [Reset = 00000000h]

PHASE\_CURRENT\_B is shown in Figure 9-19 and described in Table 9-29.

Return to the [Summary Table](#).

Measured current on Phase B Register

Figure 9-19. PHASE\_CURRENT\_B Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHASE_CURRENT_B																															
R-0h																															

Table 9-29. PHASE\_CURRENT\_B Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHASE_CURRENT_B	R	0h	32-bit signed value indicating measured continuous Phase B current. Negative value represented in two's complement Phase B current (in Amps) = (PHASE_CURRENT_B / 2 <sup>27</sup> ) * Per-unit current base Per-unit current base is 0.0375/Rsense (Rsense is current sense resistor in Ohms) A

#### 9.5.7 PHASE\_CURRENT\_C Register (Offset = 464h) [Reset = 00000000h]

PHASE\_CURRENT\_C is shown in Figure 9-20 and described in Table 9-30.

Return to the [Summary Table](#).

Measured current on Phase C Register

**Figure 9-20. PHASE\_CURRENT\_C Register**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHASE_CURRENT_C																															
R-0h																															

**Table 9-30. PHASE\_CURRENT\_C Register Field Descriptions**

Bit	Field	Type	Reset	Description
31-0	PHASE_CURRENT_C	R	0h	32-bit signed value indicating measured continuous Phase C current. Negative value represented in two's complement Phase C current (in Amps) = (PHASE_CURRENT_C / 2 <sup>27</sup> ) * Per-unit current base Per-unit current base is 0.0375/Rsense (Rsense is current sense resistor in Ohms) A

### 9.5.8 CSA\_GAIN\_FEEDBACK Register (Offset = 479h) [Reset = 0000h]

CSA\_GAIN\_FEEDBACK is shown in [Figure 9-21](#) and described in [Table 9-31](#).

Return to the [Summary Table](#).

CSA Gain Register

**Figure 9-21. CSA\_GAIN\_FEEDBACK Register**

15	14	13	12	11	10	9	8
CSA_GAIN_FEEDBACK							
R-0h							
7	6	5	4	3	2	1	0
CSA_GAIN_FEEDBACK							
R-0h							

**Table 9-31. CSA\_GAIN\_FEEDBACK Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-0	CSA_GAIN_FEEDBACK	R	0h	16-bit value indicating the current sense gain 0h = 40V/V 1h = 20V/V 2h = 10V/V 3h = 5V/V

### 9.5.9 VOLTAGE\_GAIN\_FEEDBACK Register (Offset = 47Dh) [Reset = 0000h]

VOLTAGE\_GAIN\_FEEDBACK is shown in [Figure 9-22](#) and described in [Table 9-32](#).

Return to the [Summary Table](#).

Voltage Gain Register

**Figure 9-22. VOLTAGE\_GAIN\_FEEDBACK Register**

15	14	13	12	11	10	9	8
VOLTAGE_GAIN_FEEDBACK							
R-0h							
7	6	5	4	3	2	1	0

**Figure 9-22. VOLTAGE\_GAIN\_FEEDBACK Register (continued)**

VOLTAGE_GAIN_FEEDBACK	
R-0h	

**Table 9-32. VOLTAGE\_GAIN\_FEEDBACK Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-0	VOLTAGE_GAIN_FEEDBACK	R	0h	16-bit value indicating the voltage gain 0h = 60V 1h = 30V 2h = 15V

### 9.5.10 PVDD\_VOLTAGE Register (Offset = 482h) [Reset = 00000000h]

PVDD\_VOLTAGE is shown in [Figure 9-23](#) and described in [Table 9-33](#).

Return to the [Summary Table](#).

Supply voltage register

**Figure 9-23. PVDD\_VOLTAGE Register**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PVDD_VOLTAGE																															
R-0h																															

**Table 9-33. PVDD\_VOLTAGE Register Field Descriptions**

Bit	Field	Type	Reset	Description
31-0	PVDD_VOLTAGE	R	0h	32-bit value indicating PVDD voltage DC Bus Voltage (in Volts) = PVDD_VOLTAGE * 60 / 2 <sup>27</sup>

### 9.5.11 PHASE\_VOLTAGE\_VA Register (Offset = 48Ah) [Reset = 00000000h]

PHASE\_VOLTAGE\_VA is shown in [Figure 9-24](#) and described in [Table 9-34](#).

Return to the [Summary Table](#).

Phase A Voltage Register

**Figure 9-24. PHASE\_VOLTAGE\_VA Register**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHASE_VOLTAGE_VA																															
R-0h																															

**Table 9-34. PHASE\_VOLTAGE\_VA Register Field Descriptions**

Bit	Field	Type	Reset	Description
31-0	PHASE_VOLTAGE_VA	R	0h	32-bit signed value indicating measured A phase voltage during ISD. Negative value represented in two's complement Phase A voltage (in Volts) = PHASE_VOLTAGE_VA * 60 / (sqrt(3) * 2 <sup>27</sup> )

### 9.5.12 PHASE\_VOLTAGE\_VB Register (Offset = 48Ch) [Reset = 00000000h]

PHASE\_VOLTAGE\_VB is shown in [Figure 9-25](#) and described in [Table 9-35](#).

Return to the [Summary Table](#).

Phase B Voltage Register

**Figure 9-25. PHASE\_VOLTAGE\_VB Register**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHASE_VOLTAGE_VB																															
R-0h																															

**Table 9-35. PHASE\_VOLTAGE\_VB Register Field Descriptions**

Bit	Field	Type	Reset	Description
31-0	PHASE_VOLTAGE_VB	R	0h	32-bit signed value indicating measured B phase voltage during ISD. Negative value represented in two's complement. Phase B voltage (in Volts) = PHASE_VOLTAGE_VB * 60 / (sqrt(3) * 2 <sup>27</sup> )

### 9.5.13 PHASE\_VOLTAGE\_VC Register (Offset = 48Eh) [Reset = 00000000h]

PHASE\_VOLTAGE\_VC is shown in [Figure 9-26](#) and described in [Table 9-36](#).

Return to the [Summary Table](#).

Phase C Voltage Register

**Figure 9-26. PHASE\_VOLTAGE\_VC Register**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHASE_VOLTAGE_VC																															
R-0h																															

**Table 9-36. PHASE\_VOLTAGE\_VC Register Field Descriptions**

Bit	Field	Type	Reset	Description
31-0	PHASE_VOLTAGE_VC	R	0h	32-bit signed value indicating measured C phase voltage during ISD. Negative value represented in two's complement. Phase C voltage (in Volts) = PHASE_VOLTAGE_VC * 60 / (sqrt(3) * 2 <sup>27</sup> )

### 9.5.14 SIN\_COMMUTATION\_ANGLE Register (Offset = 4D8h) [Reset = 00000000h]

SIN\_COMMUTATION\_ANGLE is shown in [Figure 9-27](#) and described in [Table 9-37](#).

Return to the [Summary Table](#).

Sine of Commutation Angle

**Figure 9-27. SIN\_COMMUTATION\_ANGLE Register**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIN_COMMUTATION_ANGLE																															
R-0h																															

**Table 9-37. SIN\_COMMUTATION\_ANGLE Register Field Descriptions**

Bit	Field	Type	Reset	Description
31-0	SIN_COMMUTATION_ANGLE	R	0h	32-bit signed value indicating sine of rotor Angle. Negative value represented in two's complement. sin(rotor angle) = (SIN_COMMUTATION_ANGLE / 2 <sup>27</sup> )

### 9.5.15 COS\_COMMUTATION\_ANGLE Register (Offset = 4DAh) [Reset = 00000000h]

COS\_COMMUTATION\_ANGLE is shown in [Figure 9-28](#) and described in [Table 9-38](#).

Return to the [Summary Table](#).

Cosine of Commutation Angle

**Figure 9-28. COS\_COMMUTATION\_ANGLE Register**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COS_COMMUTATION_ANGLE																															
R-0h																															

**Table 9-38. COS\_COMMUTATION\_ANGLE Register Field Descriptions**

Bit	Field	Type	Reset	Description
31-0	COS_COMMUTATION_ANGLE	R	0h	32-bit signed value indicating cosine of rotor angle. Negative value represented in two's complement $\text{cos}(\text{rotor angle}) = (\text{COS_COMMUTATION_ANGLE} / 2^{27})$

### 9.5.16 IALPHA Register (Offset = 504h) [Reset = 00000000h]

IALPHA is shown in [Figure 9-29](#) and described in [Table 9-39](#).

Return to the [Summary Table](#).

IALPHA Current Register

**Figure 9-29. IALPHA Register**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IALPHA																															
R-0h																															

**Table 9-39. IALPHA Register Field Descriptions**

Bit	Field	Type	Reset	Description
31-0	IALPHA	R	0h	32-bit signed value indicating phase current in alpha- beta domain. Negative value represented in two's complement $I\text{Alpha} (\text{in Amps}) = (\text{IALPHA} / 2^{27}) * \text{Per-unit current base}$ Per-unit current base is $0.0375/\text{Rsense}$ (Rsense is current sense resistor in Ohms) A

### 9.5.17 IBETA Register (Offset = 506h) [Reset = 00000000h]

IBETA is shown in [Figure 9-30](#) and described in [Table 9-40](#).

Return to the [Summary Table](#).

IBETA Current Register

**Figure 9-30. IBETA Register**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IBETA																															
R-0h																															

**Table 9-40. IBETA Register Field Descriptions**

Bit	Field	Type	Reset	Description
31-0	IBETA	R	0h	32-bit signed value indicating phase current in alpha- beta domain. Negative value represented in two's complement $I\text{Beta} (\text{in Amps}) = (\text{IBETA} / 2^{27}) * \text{Per-unit current base}$ Per-unit current base is $0.0375/\text{Rsense}$ (Rsense is current sense resistor in Ohms) A

### 9.5.18 VALPHA Register (Offset = 508h) [Reset = 00000000h]

VALPHA is shown in [Figure 9-31](#) and described in [Table 9-41](#).

Return to the [Summary Table](#).

VALPHA Voltage Register

**Figure 9-31. VALPHA Register**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALPHA																															
R-0h																															

**Table 9-41. VALPHA Register Field Descriptions**

Bit	Field	Type	Reset	Description
31-0	VALPHA	R	0h	32-bit signed value indicating applied phase voltage in alpha-beta domain VALpha (in Volts) = (VALPHA / 2 <sup>27</sup> ) * 60 / sqrt(3)

### 9.5.19 VBETA Register (Offset = 50Ah) [Reset = 00000000h]

VBETA is shown in [Figure 9-32](#) and described in [Table 9-42](#).

Return to the [Summary Table](#).

VBETA Voltage Register

**Figure 9-32. VBETA Register**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VBETA																															
R-0h																															

**Table 9-42. VBETA Register Field Descriptions**

Bit	Field	Type	Reset	Description
31-0	VBETA	R	0h	32-bit signed value indicating applied phase voltage in alpha-beta domain. Negative value represented in two's complement VBeta (in Volts) = (VBETA / 2 <sup>27</sup> ) * 60 / sqrt(3)

### 9.5.20 ID Register (Offset = 514h) [Reset = 00000000h]

ID is shown in [Figure 9-33](#) and described in [Table 9-43](#).

Return to the [Summary Table](#).

Measured d-axis Current Register

**Figure 9-33. ID Register**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																															
R-0h																															

Table 9-43. ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ID	R	0h	32-bit signed value indicating d-axis(flux component) phase current in d-q domain. Negative value represented in two's complement Flux component phase current (in Amps) = (ID / 2 <sup>27</sup> ) * Per-unit current base Per-unit current base is 0.0375/Rsense (Rsense is current sense resistor in Ohms) A

#### 9.5.21 IQ Register (Offset = 516h) [Reset = 00000000h]

IQ is shown in Figure 9-34 and described in Table 9-44.

Return to the [Summary Table](#).

Measured q-axis Current Register

Figure 9-34. IQ Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IQ																															
R-0h																															

Table 9-44. IQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	IQ	R	0h	32-bit signed value indicating q-axis(torque component) phase current in d-q domain. Negative value represented in two's complement Torque component phase current (in Amps) = (IQ / 2 <sup>27</sup> ) * Per-unit current base Per-unit current base is 0.0375/Rsense (Rsense is current sense resistor in Ohms) A

#### 9.5.22 VD Register (Offset = 518h) [Reset = 00000000h]

VD is shown in Figure 9-35 and described in Table 9-45.

Return to the [Summary Table](#).

VD Voltage Register

Figure 9-35. VD Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VD																															
R-0h																															

Table 9-45. VD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VD	R	0h	32-bit signed value indicating applied phase voltage in d-q domain. Negative value represented in two's complement Vd (in Volts) = (VD / 2 <sup>27</sup> ) * 60 / sqrt(3)

#### 9.5.23 VQ Register (Offset = 51Ah) [Reset = 00000000h]

VQ is shown in Figure 9-36 and described in Table 9-46.

Return to the [Summary Table](#).

## VQ Voltage Register

**Figure 9-36. VQ Register**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VQ																															
R-0h																															

**Table 9-46. VQ Register Field Descriptions**

Bit	Field	Type	Reset	Description
31-0	VQ	R	0h	32-bit signed value indicating applied phase voltage in d-q domain. Negative value represented in two's complement Vq (in Volts) = $(VQ / 2^{27}) * 60 / \sqrt{3}$

**9.5.24 IQ\_REF\_ROTOR\_ALIGN Register (Offset = 54Ch) [Reset = 00000000h]**

IQ\_REF\_ROTOR\_ALIGN is shown in [Figure 9-37](#) and described in [Table 9-47](#).

Return to the [Summary Table](#).

Align Current Reference

**Figure 9-37. IQ\_REF\_ROTOR\_ALIGN Register**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IQ_REF_ROTOR_ALIGN																															
R-0h																															

**Table 9-47. IQ\_REF\_ROTOR\_ALIGN Register Field Descriptions**

Bit	Field	Type	Reset	Description
31-0	IQ_REF_ROTOR_ALIGN	R	0h	32-bit signed value indicating current reference during align state. Negative value represented in two's complement Current reference during Align State (in Amps) = $(IQ\_REF\_ROTOR\_ALIGN / 2^{27}) * \text{Per-unit current base}$ Per-unit current base is 0.0375/Rsense (Rsense is current sense resistor in Ohms) A

**9.5.25 SPEED\_REF\_OPEN\_LOOP Register (Offset = 560h) [Reset = 00000000h]**

SPEED\_REF\_OPEN\_LOOP is shown in [Figure 9-38](#) and described in [Table 9-48](#).

Return to the [Summary Table](#).

Speed at which motor transitions to close loop

**Figure 9-38. SPEED\_REF\_OPEN\_LOOP Register**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPEED_REF_OPEN_LOOP																															
R-0h																															

**Table 9-48. SPEED\_REF\_OPEN\_LOOP Register Field Descriptions**

Bit	Field	Type	Reset	Description
31-0	SPEED_REF_OPEN_LOOP	R	0h	32-bit signed value indicating open loop speed reference. Negative value represented in two's complement Speed reference during Open loop (in Hz) = $(SPEED\_REF\_OPEN\_LOOP / 2^{27}) * \text{MAX\_SPEED}$ (in Hz)

### 9.5.26 IQ\_REF\_OPEN\_LOOP Register (Offset = 56Eh) [Reset = 00000000h]

IQ\_REF\_OPEN\_LOOP is shown in Figure 9-39 and described in Table 9-49.

Return to the [Summary Table](#).

Open Loop Current Reference

**Figure 9-39. IQ\_REF\_OPEN\_LOOP Register**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IQ_REF_OPEN_LOOP																															
R-0h																															

**Table 9-49. IQ\_REF\_OPEN\_LOOP Register Field Descriptions**

Bit	Field	Type	Reset	Description
31-0	IQ_REF_OPEN_LOOP	R	0h	32-bit signed value indicating current reference during open loop. Negative value represented in two's complement. Current reference during Open loop (in Amps) = $(IQ\_REF\_OPEN\_LOOP / 2^{27}) * \text{Per-unit current base}$ Per-unit current base is 0.0375/Rsense (Rsense is current sense resistor in Ohms) A

### 9.5.27 SPEED\_REF\_CLOSED\_LOOP Register (Offset = 5EEh) [Reset = 00000000h]

SPEED\_REF\_CLOSED\_LOOP is shown in Figure 9-40 and described in Table 9-50.

Return to the [Summary Table](#).

Speed Reference Register

**Figure 9-40. SPEED\_REF\_CLOSED\_LOOP Register**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPEED_REF_CLOSED_LOOP																															
R-0h																															

**Table 9-50. SPEED\_REF\_CLOSED\_LOOP Register Field Descriptions**

Bit	Field	Type	Reset	Description
31-0	SPEED_REF_CLOSED_L OOP	R	0h	32-bit signed value indicating reference for closed loop. Negative value represented in two's complement. In speed control mode, speed reference in closed loop (in Hz) = $(SPEED\_REF\_CLOSED\_LOOP / 2^{27}) * \text{MAX\_SPEED}$ (in Hz). In power mode, power reference in closed loop (in Watts) = $(SPEED\_REF\_CLOSED\_LOOP / 2^{27}) * \text{MAX\_POWER}$ (in Watts). In current mode, Iq current reference in closed loop (in Amps) = $(SPEED\_REF\_CLOSED\_LOOP / 2^{27}) * \text{ILIMIT}$ (in Amps)

### 9.5.28 POWER\_FEED\_BACK Register (Offset = 628h) [Reset = 00000000h]

POWER\_FEED\_BACK is shown in Figure 9-41 and described in Table 9-51.

Return to the [Summary Table](#).

Power Feedback

**Figure 9-41. POWER\_FEED\_BACK Register**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
POWER_FEED_BACK																															
R-0h																															

**Table 9-51. POWER\_FEED\_BACK Register Field Descriptions**

Bit	Field	Type	Reset	Description
31-0	POWER_FEED_BACK	R	0h	32-bit signed value indicating power consumption. Negative value represented in two's complement Power Consumption (in Watts) = (POWER_FEED_BACK / 2 <sup>27</sup> ) * Per-unit power base Per-unit power base is (2.25/Rsense (Rsense is current sense resistor in Ohms) ) in watts

**9.5.29 ID\_REF\_CLOSED\_LOOP Register (Offset = 630h) [Reset = 00000000h]**

 ID\_REF\_CLOSED\_LOOP is shown in [Figure 9-42](#) and described in [Table 9-52](#).

[Return to the Summary Table.](#)
[Reference for Current Loop Register](#)
**Figure 9-42. ID\_REF\_CLOSED\_LOOP Register**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID_REF_CLOSED_LOOP																															
R-0h																															

**Table 9-52. ID\_REF\_CLOSED\_LOOP Register Field Descriptions**

Bit	Field	Type	Reset	Description
31-0	ID_REF_CLOSED_LOOP	R	0h	32-bit signed value indicating d-axis(flux component) phase current reference in closed loop . Negative value represented in two's complement Flux component phase current reference in closed loop (in Amps) = (ID / 2 <sup>27</sup> ) * Per-unit current base Per-unit current base is 0.0375/Rsense (Rsense is current sense resistor in Ohms) A

**9.5.30 IQ\_REF\_CLOSED\_LOOP Register (Offset = 632h) [Reset = 00000000h]**

 IQ\_REF\_CLOSED\_LOOP is shown in [Figure 9-43](#) and described in [Table 9-53](#).

[Return to the Summary Table.](#)
[Reference for Current Loop Register](#)
**Figure 9-43. IQ\_REF\_CLOSED\_LOOP Register**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IQ_REF_CLOSED_LOOP																															
R-0h																															

**Table 9-53. IQ\_REF\_CLOSED\_LOOP Register Field Descriptions**

Bit	Field	Type	Reset	Description
31-0	IQ_REF_CLOSED_LOOP	R	0h	32-bit signed value indicating q-axis(torque component) phase current reference in closed loop. Negative value represented in two's complement Torque component phase current reference in closed loop (in Amps) = (IQ / 2 <sup>27</sup> ) * Per-unit current base Per-unit current base is 0.0375/Rsense (Rsense is current sense resistor in Ohms) A

### 9.5.31 ISD\_STATE Register (Offset = 6F0h) [Reset = 0000h]

ISD\_STATE is shown in [Figure 9-44](#) and described in [Table 9-54](#).

Return to the [Summary Table](#).

ISD state Register

**Figure 9-44. ISD\_STATE Register**

15	14	13	12	11	10	9	8
ISD_STATE							
R-0h							
7	6	5	4	3	2	1	0
ISD_STATE							
R-0h							

**Table 9-54. ISD\_STATE Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-0	ISD_STATE	R	0h	16-bit value indicating current ISD state 0h = ISD_INIT 1h = ISD_MOTOR_STOP_CHECK 2h = ISD_ESTIM_INIT 3h = ISD_RUN_MOTOR_CHECK 4h = ISD_MOTOR_DIRECTION_CHECK 5h = ISD_COMPLETE 6h = ISD_FAULT

### 9.5.32 ISD\_SPEED Register (Offset = 6FAh) [Reset = 00000000h]

ISD\_SPEED is shown in [Figure 9-45](#) and described in [Table 9-55](#).

Return to the [Summary Table](#).

ISD Speed Register

**Figure 9-45. ISD\_SPEED Register**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ISD_SPEED																															
R-0h																															

**Table 9-55. ISD\_SPEED Register Field Descriptions**

Bit	Field	Type	Reset	Description
31-0	ISD_SPEED	R	0h	32-bit value indicating calculated absolute speed during ISD state Speed estimated during ISD (in Hz) = (ISD_SPEED / 2 <sup>27</sup> ) * MAX_SPEED (in Hz)

### 9.5.33 IPD\_STATE Register (Offset = 724h) [Reset = 0000h]

IPD\_STATE is shown in [Figure 9-46](#) and described in [Table 9-56](#).

Return to the [Summary Table](#).

IPD state Register

**Figure 9-46. IPD\_STATE Register**

15	14	13	12	11	10	9	8
IPD_STATE							

**Figure 9-46. IPD\_STATE Register (continued)**

R-0h							
7	6	5	4	3	2	1	0
IPD_STATE							
R-0h							

**Table 9-56. IPD\_STATE Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-0	IPD_STATE	R	0h	16-bit value indicating current IPD state 0h = IPD_INIT 1h = IPD_VECTOR_CONFIG 2h = IPD_RUN 3h = IPD_SLOW_RISE_CLOCK 4h = IPD_SLOW_FALL_CLOCK 5h = IPD_WAIT_CURRENT_DECAY 6h = IPD_GET_TIMES 7h = IPD_SET_NEXT_VECTOR 8h = IPD_CALC_SECTOR_RISE 9h = IPD_CALC_ROTOR_POSITION Ah = IPD_CALC_ANGLE Bh = IPD_COMPLETE Ch = IPD_FAULT

### 9.5.34 IPD\_ANGLE Register (Offset = 746h) [Reset = 00000000h]

IPD\_ANGLE is shown in [Figure 9-47](#) and described in [Table 9-57](#).

Return to the [Summary Table](#).

Calculated IPD Angle Register

**Figure 9-47. IPD\_ANGLE Register**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IPD_ANGLE																															
R-0h																															

**Table 9-57. IPD\_ANGLE Register Field Descriptions**

Bit	Field	Type	Reset	Description
31-0	IPD_ANGLE	R	0h	32-bit signed value indicating measured IPD angle. Negative value represented in two's complement IPD Angle (in degrees) = (IPD_ANGLE / $2^{27}$ ) * 360

### 9.5.35 ED Register (Offset = 772h) [Reset = 00000000h]

ED is shown in [Figure 9-48](#) and described in [Table 9-58](#).

Return to the [Summary Table](#).

Estimated BEMF EQ Register

**Figure 9-48. ED Register**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ED																															
R-0h																															

Table 9-58. ED Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ED	R	0h	32-bit signed value indicating estimated Back EMF along the D-Axis (Ed). Negative value represented in two's complement Ed (in Volts) = $(ED / 2^{27}) * 60 / \sqrt{3}$

### 9.5.36 EQ Register (Offset = 774h) [Reset = 00000000h]

EQ is shown in Figure 9-49 and described in Table 9-59.

Return to the [Summary Table](#).

Estimated BEMF ED Register

Figure 9-49. EQ Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EQ																															
R-0h																															

Table 9-59. EQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	EQ	R	0h	32-bit signed value indicating estimated Back EMF along the Q-Axis (Eq). Negative value represented in two's complement. Eq (in Volts) = $(EQ / 2^{27}) * 60 / \sqrt{3}$

### 9.5.37 SPEED\_FDBK Register (Offset = 784h) [Reset = 00000000h]

SPEED\_FDBK is shown in Figure 9-50 and described in Table 9-60.

Return to the [Summary Table](#).

Speed Feedback Register

Figure 9-50. SPEED\_FDBK Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPEED_FDBK																															
R-0h																															

Table 9-60. SPEED\_FDBK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SPEED_FDBK	R	0h	32-bit signed value indicating estimated motor speed. Negative value represented in two's complement Estimated motor speed (in Hz) = $(SPEED_FDBK / 2^{27}) * MAX\_SPEED$ (in Hz)

### 9.5.38 THETA\_EST Register (Offset = 788h) [Reset = 00000000h]

THETA\_EST is shown in Figure 9-51 and described in Table 9-61.

Return to the [Summary Table](#).

Estimated rotor Position Register

Figure 9-51. THETA\_EST Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
THETA_EST																															

**Figure 9-51. THETA\_EST Register (continued)**

R-0h

**Table 9-61. THETA\_EST Register Field Descriptions**

Bit	Field	Type	Reset	Description
31-0	THETA_EST	R	0h	32-bit signed value indicating estimated rotor angle. Angle should be modulo 360 degrees. For example if the estimated Angle value 380 degrees then it means $380\%360 = 20$ degrees Estimated rotor Angle (in degrees) = $(\text{THETA\_EST} / 2^{27}) * 360$

## 10 Typical Applications

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### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

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The MCPC029 device is used in sensorless or sensed 3-phase BLDC motor control. The driver provides a high performance, high-reliability, flexible solution for appliances, fans, pumps, residential and living fans and blowers. The following section shows a common application of the MCPC029 device. **Figure 7-3 to Figure 7-7** show the typical schematic of MCPC029 based motor control applications. The other features implemented are as below:

- VDD (3.3 V) power supply internally generated via LDO linear regulator
- Overcurrent protection using internal comparators connected to internal PGA output.
- Current sensing using internal PGA and ADCs
- Bus voltage monitoring using internal ADC
- Application temperature monitoring using internal ADC

1. **Figure 7-3** shows an application example using MCPC028 device to drive a 3-phase BLDC motor with three shunt configuration and sensorless InstaSPIN-FOC algorithm with three-phase voltage sensing.
2. **Figure 7-4** shows an application example using MCPC028 device to drive a 3-phase BLDC motor with single shunt configuration and sensorless InstaSPIN-FOC algorithm with three-phase voltage sensing.
3. **Figure 7-5** shows an application example using MCPC028 device to drive a 3-phase BLDC motor with three shunt configuration and typical sensorless FOC algorithm without three-phase voltage sensing.
4. **Figure 7-6** shows an application example using MCPC028 device to drive a 3-phase BLDC motor with single shunt configuration and typical sensorless FOC algorithm without three-phase voltage sensing.
5. **Figure 7-7** shows an application example using MCPC028 device to drive a 3-phase BLDC motor with three shunt configuration and hall sensor based FOC algorithm without three-phase voltage sensing.

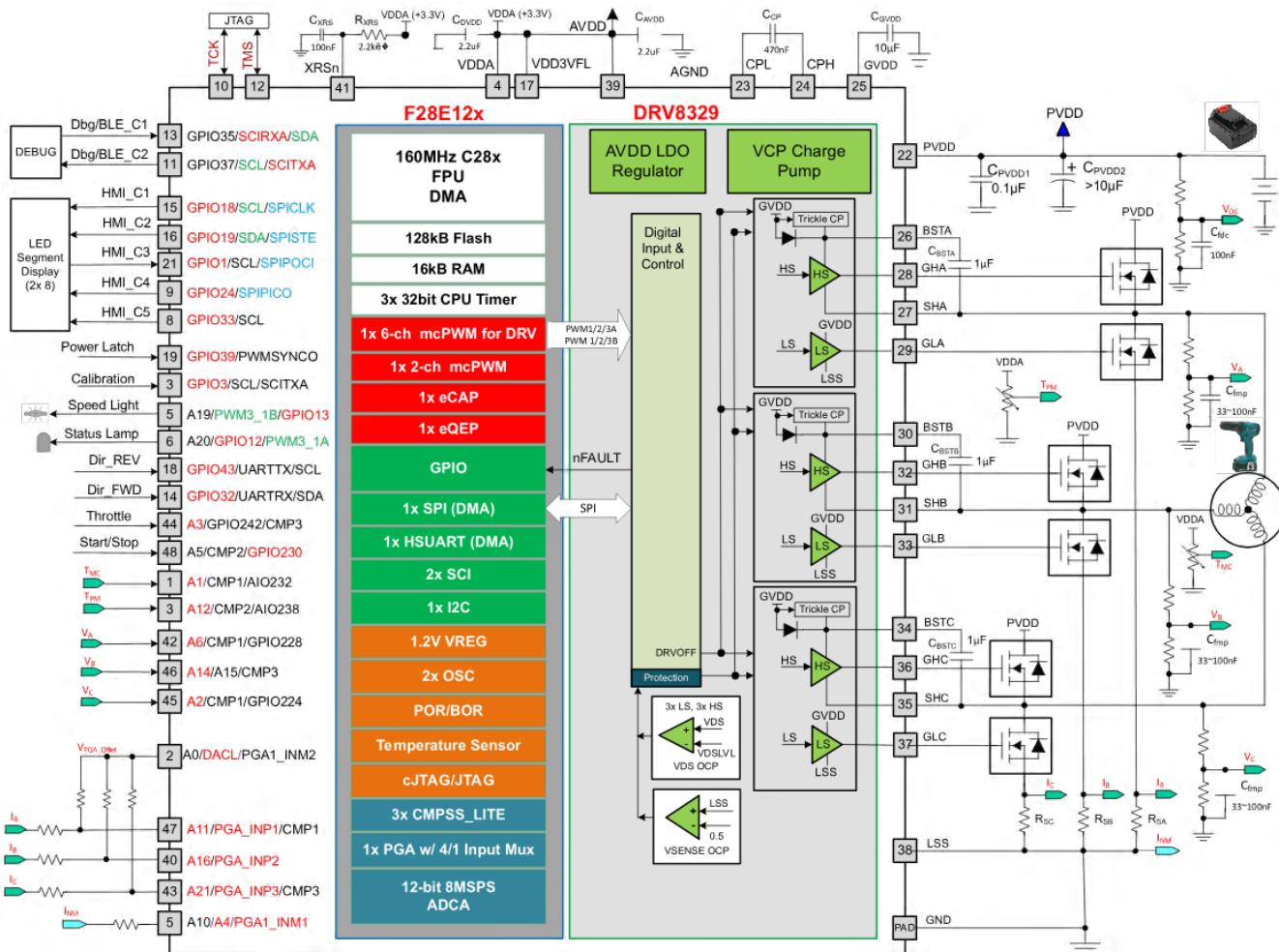
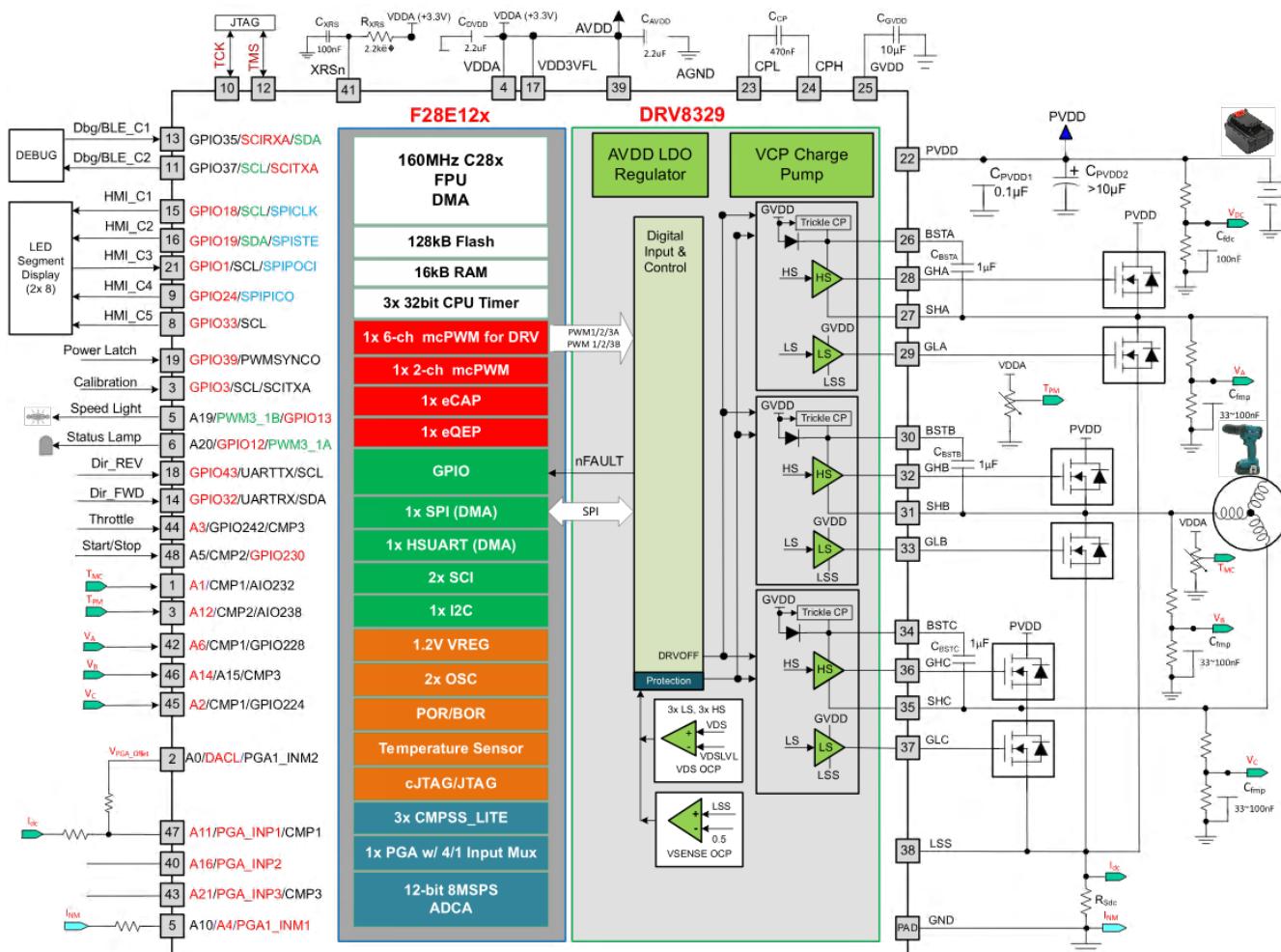


Figure 10-1. Typical Schematic of MCPC029 for Motor Control with Sensorless InstaSPIN-FOC and 3 Current Shunt Sensing



**Figure 10-2. Typical Schematic of MCPC029 for Motor Control with Sensorless InstaSPIN-FOC and Single Current Shunt Sensing**

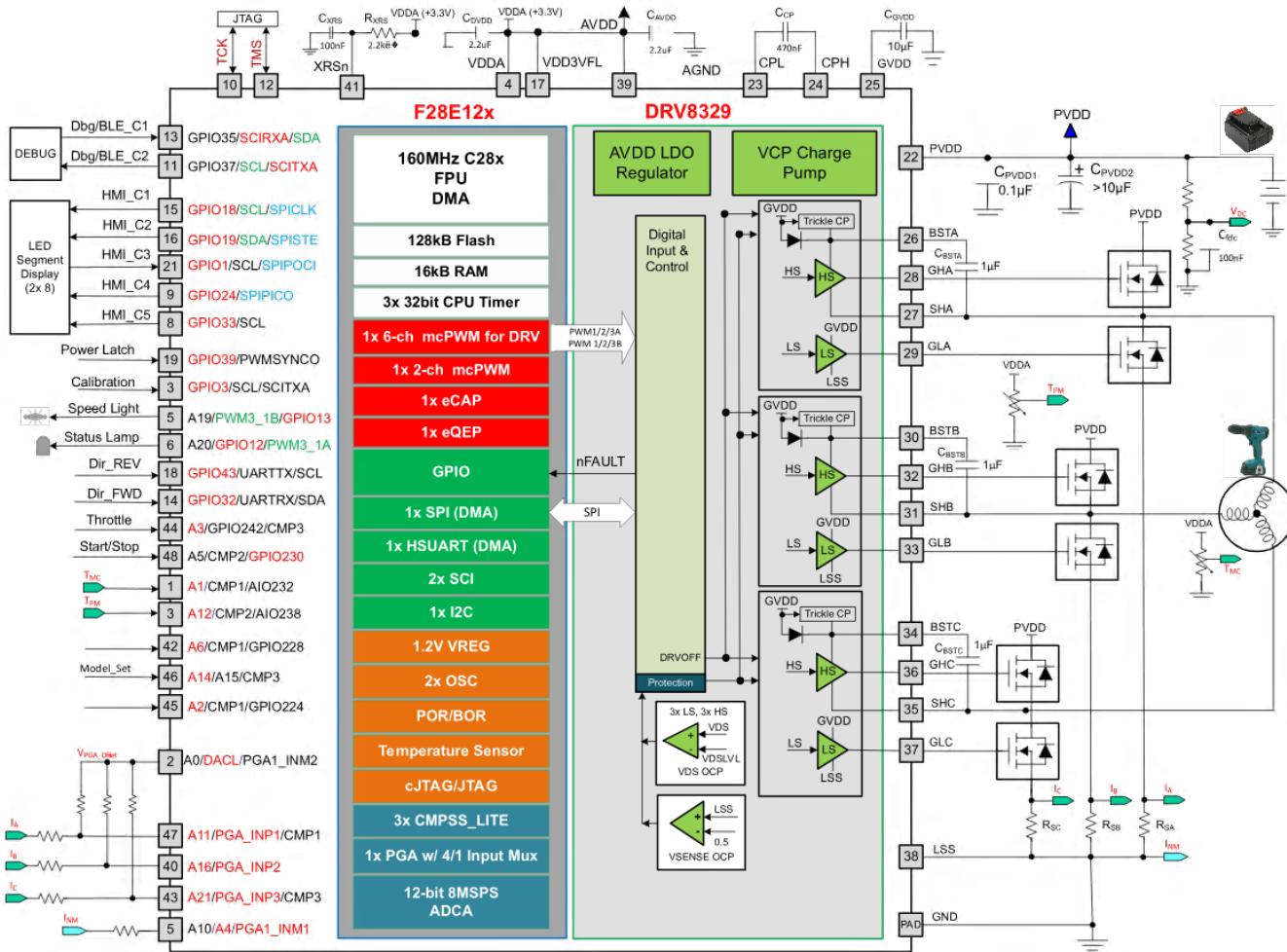


Figure 10-3. Typical Schematic of MCPC029 for Motor Control with Sensorless FOC and 3 Current Shunt Sensing

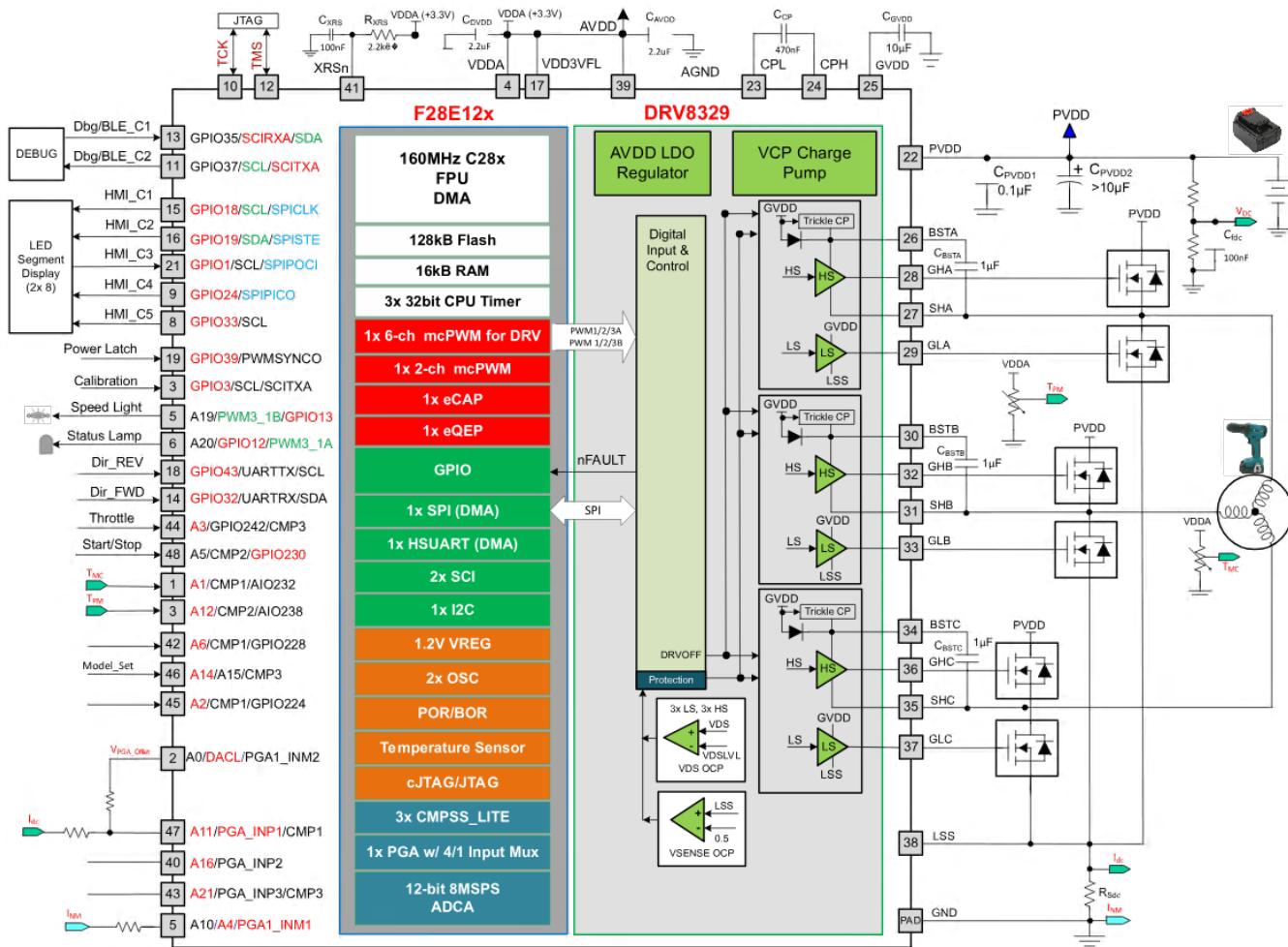
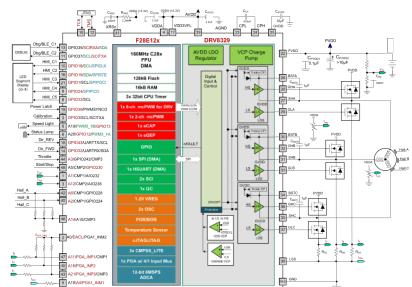


Figure 10-4. Typical Schematic of MCPC029 for Motor Control with Sensorless FOC and Single Current Shunt Sensing



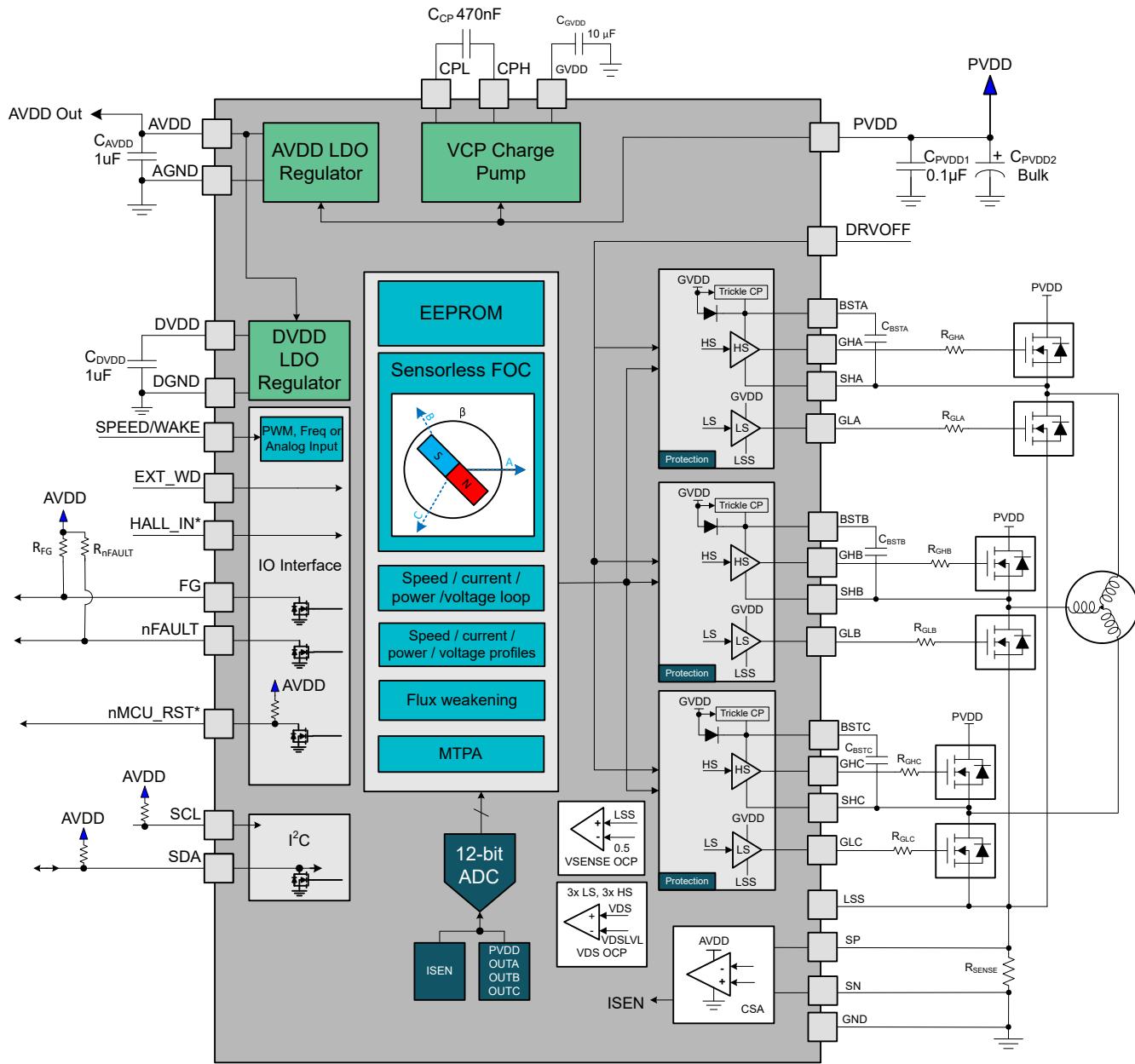
**Figure 10-5. Typical Schematic of MCPC029 for Motor Control with Hall based Sensored FOC and Three Current Shunt Sensing**

## 10.1 Application Information

The MCF8329HS-Q1 is used in 3-phase sensorless motor control applications such as oil/coolant/fuel/water pumps, HVAC blowers, sunroof modules and wipers.

## 10.2 Typical Applications

Figure 10-6 shows the typical schematic of MCF8329HS-Q1. Table 7-1 shows the recommended values of the external components for the driver.



\*HALL\_IN and nMCU\_RST are mux'ed functions on pin 30

Figure 10-6. Typical Schematic of MCF8329HS-Q1

### Detailed Design Procedure

Table below lists the example input parameters for the system design.

Table 10-1. Design parameters

DESIGN PARAMETERS	REFERENCE	EXAMPLE VALUE
Supply voltage	V <sub>PVDD</sub>	24 V
Motor peak current	I <sub>PEAK</sub>	20 A
PWM Frequency	f <sub>PWM</sub>	20 kHz
MOSFET VDS Slew Rate	SR	120 V/us
MOSFET input gate capacitance	Q <sub>G</sub>	54 nC

**Table 10-1. Design parameters (continued)**

DESIGN PARAMETERS	REFERENCE	EXAMPLE VALUE
MOSFET input gate capacitance	$Q_{GD}$	14 nC
Dead time	$t_{dead}$	200 ns
Overcurrent protection	$I_{OCP}$	30 A

### Bootstrap Capacitor and GVDD Capacitor Selection

The bootstrap capacitor must be sized to maintain the bootstrap voltage above the undervoltage lockout for normal operation. [Equation 13](#) calculates the maximum allowable voltage drop across the bootstrap capacitor:

$$\Delta V_{BSTX} = V_{GVDD} - V_{BOOTD} - V_{BSTUV} \quad (13)$$

$$\Delta V_{BSTX} = 12V - 0.85V - 4.45V = 6.7V$$

where

- $V_{GVDD}$  is the supply voltage of the gate drive
- $V_{BOOTD}$  is the forward voltage drop of the bootstrap diode
- $V_{BSTUV}$  is the threshold of the bootstrap undervoltage lockout

In the example, allowed voltage drop across bootstrap capacitor is 6.7V. TI generally recommends that ripple voltage on both the bootstrap capacitor and GVDD capacitor are minimized as much as possible. Many of commercial, industrial, and automotive applications use ripple value between 0.5V to 1V.

The total charge needed per switching cycle can be estimated with [Equation 14](#):

$$Q_{TOT} = Q_G + \frac{I_{LBS\_TRAN}}{f_{SW}} \quad (14)$$

$$Q_{TOT} = 54nC + 115\mu A/20kHz = 54nC + 5.8nC = 59.8nC$$

where

- $Q_G$  is the total MOSFET gate charge
- $I_{LBS\_TRAN}$  is the bootstrap pin leakage current
- $f_{SW}$  is the PWM frequency

The minimum bootstrap capacitor can then be estimated as below assuming 1V of  $\Delta V_{BSTX}$ :

$$C_{BST\_MIN} = \frac{Q_{TOT}}{\Delta V_{BSTX}} \quad (15)$$

$$C_{BST\_MIN} = 59.8nC / 1V = 59.8nF$$

The calculated value of minimum bootstrap capacitor is 59.8nF. Note that, this value of capacitance is needed at full bias voltage. In practice, the value of the bootstrap capacitor must be greater than calculated value to allow for situations where the power stage can skip pulse due to various transient conditions. TI recommends to use a 100nF bootstrap capacitor in this example. TI recommends to include enough margin and place the bootstrap capacitor as close to the BSTx and SHx pins as possible.

$$C_{GVDD} \geq 10 \times C_{BSTX} \quad (16)$$

$$C_{GVDD} = 10 \times 100nF = 1\mu F$$

For this example application, choose a 1 $\mu$ F  $C_{GVDD}$  capacitor. Choose a capacitor with a voltage rating at least twice the maximum voltage that the capacitor is exposed to because most ceramic capacitors lose significant capacitance when biased. This value also improves the long-term reliability of the system.

**Note**

For higher power system requiring 100% duty cycle support for longer duration TI recommends to use  $C_{BSTx}$  of  $\geq 1\mu F$  and  $C_{GVDD}$  of  $\geq 10\mu F$ .

**Gate Drive Current**

Selecting an appropriate gate drive current is essential when turning on or off power MOSFETs gates to switch motor current. The amount of gate drive current and input capacitance of the MOSFETs determines the drain-to-source voltage slew rate ( $V_{DS}$ ). Gate drive current can be sourced from GVDD into the MOSFET gate ( $I_{SOURCE}$ ) or sunk from the MOSFET gate into SHx or LSS ( $I_{SINK}$ ).

Using too high of a gate drive current can turn on MOSFETs too quickly which may cause excessive ringing,  $dV/dt$  coupling, or cross-conduction from switching large amounts of current. If parasitic inductances and capacitances exist in the system, voltage spiking or ringing may occur which can damage the MOSFETs or the MCF8329HS-Q1 device.

On the other hand, using too low of a gate drive current causes long  $V_{DS}$  slew rates. Turning on the MOSFETs too slowly may heat up the MOSFETs due to  $R_{DS,ON}$  switching losses.

The relationship between gate drive current  $I_{GATE}$ , MOSFET gate-to-drain charge  $Q_{GD}$ , and  $V_{DS}$  slew rate switching time  $t_{rise,fall}$  are described by the following equations:

$$SR_{DS} = \frac{V_{DS}}{t_{rise,fall}} \quad (17)$$

$$I_{GATE} = \frac{Q_{gd}}{t_{rise,fall}} \quad (18)$$

It is recommended to evaluate at lower gate drive currents and increase gate drive current settings to avoid damage from unintended operation during initial evaluation.

**Gate Resistor Selection**

The slew rate of the SHx connection will be dependent on the rate at which the gate of the external MOSFETs is controlled. The pull-up/pull-down strength of MCF8329HS-Q1 is fixed internally, hence the slew rate of gate voltage can be controlled with an external series gate resistor. In some applications, the gate charge of the MOSFET, which is the load on gate driver device, is significantly larger than the gate driver peak output current capability. In such applications, external gate resistors can limit the peak output current of the gate driver. External gate resistors are also used to dampen ringing and noise.

The specific parameters of the MOSFET, system voltage, and board parasitics will all affect the final SHx slew rate, so generally selecting an optimal value or configuration of external gate resistor is an iterative process.

To lower the gate drive current, a series resistor  $R_{GATE}$  can be placed on the gate drive outputs to control the current for the source and sink current paths. A single gate resistor will have the same gate path for source and sink gate current, so larger  $R_{GATE}$  values will yield similar SHx slew rates. Note that gate drive current varies by PVDD voltage, junction temperature, and process variation of the device.

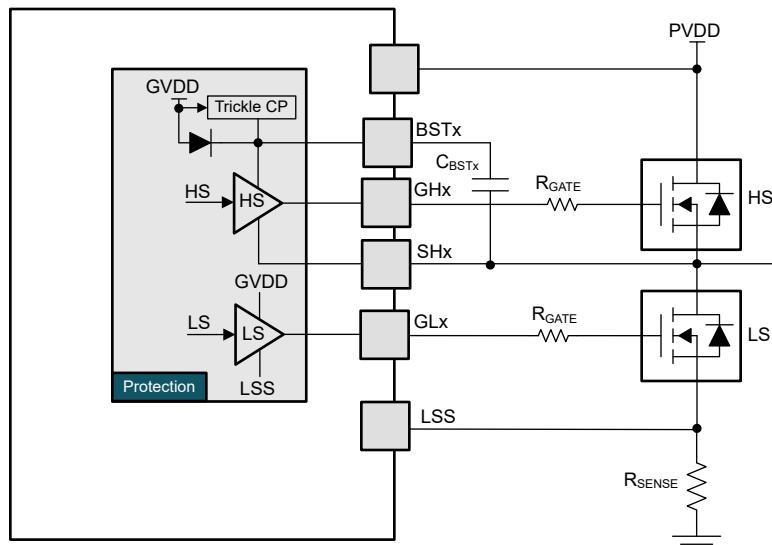


Figure 10-7. Gate driver outputs with series resistors

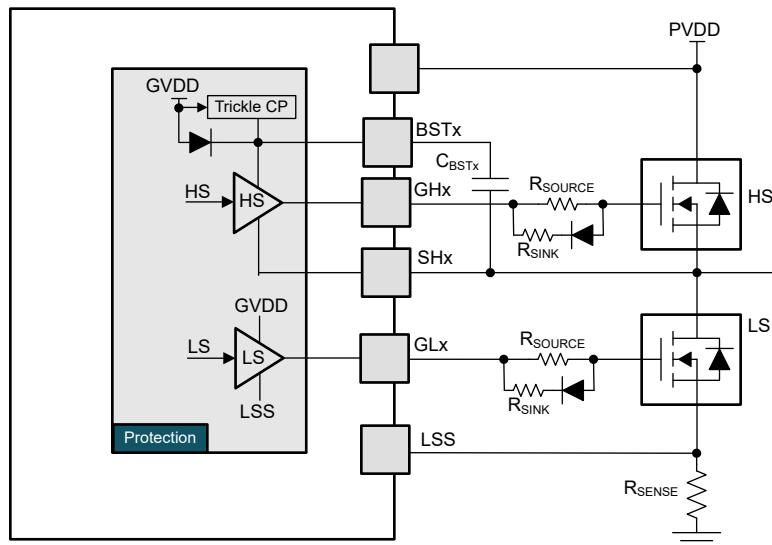


Figure 10-8. Gate driver outputs with separate source and sink current paths

Typically, it is recommended to have the sink current be twice the source current to implement a strong pull-down from gate to the source to ensure the MOSFET stays off while the opposite FET is switching. This can be implemented discretely by providing a separate path through a resistor for the source and sink currents by placing a diode and sink resistor ( $R_{SINK}$ ) in parallel to the source resistor ( $R_{SOURCE}$ ). Using the same value of source and sink resistors results in half the equivalent resistance for the sink path. This yields twice the gate drive sink current compared to the source current, and SHx will slew twice as fast when turning off the MOSFET.

### System Considerations in High Power Designs

Higher power system designs can require design and application considerations that are not regarded in lower power system designs. It is important to combat the volatile nature of higher power systems by implementing troubleshooting guidelines, external components and circuits, driver product features, or layout techniques. For more information, please visit the [System Design Considerations for High-Power Motor Driver Applications](#) application note.

### Capacitor Voltage Ratings

Use capacitors with voltage ratings that are 2x the supply voltage (PVDD, GVDD, AVDD, etc). Capacitors can experience up to half the rated capacitance due to poor DC voltage rating performance.

For example, since the bootstrap voltage is around 12 to 13-V with respect to SHx (BSTx-SHx) then the BSTx-SHx capacitor should be rated for 25-V or greater.

### External Power Stage Components

External components in the power stage are not required by design but are helpful in suppressing transients, managing inductor coil energy, mitigating supply pumping, dampening phase ringing, or providing strong gate-to-source pulldown paths. These components are used for system tuning and debuggability so the BLDC motor system is robust while avoiding damage to the MCF8329HS-Q1 device or external MOSFETs.

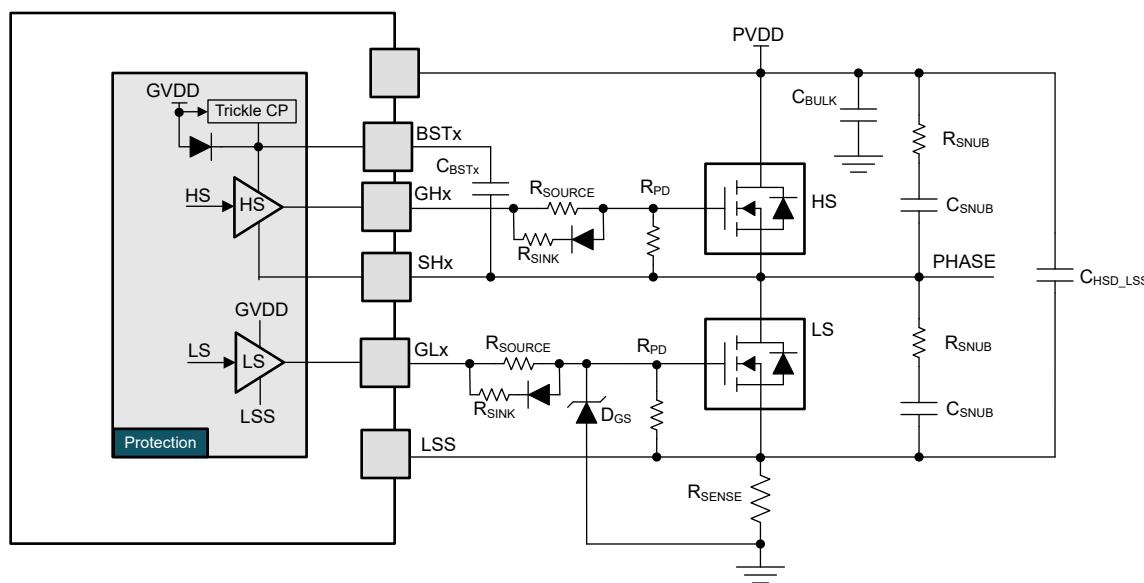


Figure 10-9. Optional external power stage components

Some examples of issues and external components that can resolve those issues are found in table below.

Table 10-2. Common issues and resolutions for power stage debugging

Issue	Resolution	Components
Gate drive current required is too large, resulting in very fast MOSFET $V_{DS}$ slew rate	Series resistors required for gate drive current adjustability	0-100 $\Omega$ series resistors (RGATE/RSOURCE) at gate driver outputs (GHx/GLx), optional sink resistor (RSINK) and diode in parallel with gate resistor for adjustable sink current
Ringing at phase's switch node (SHx) resulting in high EMI emissions	RC snubbers placed in parallel to each HS/LS MOSFET to dampen oscillations	Resistor (RSNUB) and Capacitor (CSNUB) placed parallel to the MOSFET, calculate RC values based on ringing frequency using <a href="#">Proper RC Snubber Design for Motor Drivers</a>
Negative transients at low-side source (LSS) below minimum specification	HS drain to LS source capacitor to suppress negative bouncing	0.01uF-1uF, PVDD-rated capacitor from PVDD-LSS (CHSD_LSS) placed near LS MOSFET's source
Negative transient at low-side gate (GLx) below minimum specification	Gate-to-ground Zener diode to clamp negative voltage	GVDD voltage rated Zener diode (DGS) with anode connected to GND and cathode connected to GLx

**Table 10-2. Common issues and resolutions for power stage debugging (continued)**

Issue	Resolution	Components
Extra protection required to ensure MOSFET is turned off if gate drive signals are Hi-Z	External gate-to-source pulldown resistors (after series gate resistors)	10 kΩ to 100 kΩ resistor (RPD) connected from gate to source for each MOSFET

## 10.3 Power Supply Recommendations

The MCF8329HS-Q1 is designed to operate from an input voltage supply (PVDD) range from 4.5 V to 60 V. A 10- $\mu$ F and 0.1- $\mu$ F ceramic capacitor rated for PVDD must be placed as close to the device as possible. In addition, a bulk capacitor must be included on the PVDD pin but can be shared with the bulk bypass capacitance for the external power MOSFETs. Additional bulk capacitance is required to bypass the external half-bridge MOSFETs and should be sized according to the application requirements.

### 10.3.1 Bulk Capacitance

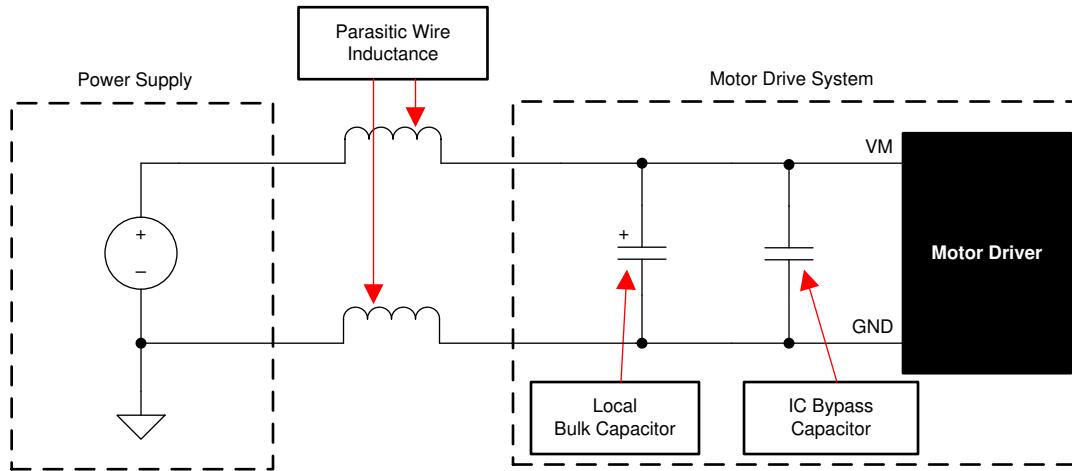
Having an appropriate local bulk capacitance is an important factor in motor drive system design. Designs generally benefit in having more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system
- The capacitance and current capability of the power supply
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple
- The type of motor used (brushed DC, brushless DC, stepper)
- The motor braking method

The inductance between the power supply and the motor drive system limits the rate at which current can change from the power supply. If the local bulk capacitance is too small, the system responds to excessive current demands or dumps from the motor with a change in PVDD voltage. When adequate bulk capacitance is used, the PVDD voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate bulk capacitor. The voltage rating for bulk capacitors needs to be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.


**Figure 10-10. Example Setup of Motor Drive System With External Power Supply**

## 10.4 Layout

### 10.4.1 Layout Guidelines

Bypass the PVDD pin to the GND pin using a low-ESR ceramic bypass capacitor with a recommended value of 0.1 $\mu$ F. Place this capacitor as close to the PVDD pin as possible with a thick trace or ground plane connected to

the GND pin. Additionally, bypass the PVDD pin using a bulk capacitor rated for PVDD. This component can be electrolytic. This capacitance must be at least 10 $\mu$ F.

Additional bulk capacitance is required to bypass the high current path on the external MOSFETs. This bulk capacitance should be placed such that it minimizes the length of any high current paths through the external MOSFETs. The connecting metal traces should be as wide as possible, with numerous vias connecting PCB layers. These practices minimize inductance and let the bulk capacitor deliver high current.

Place a low-ESR ceramic capacitor between the CPL and CPH pins. This capacitor should be 470nF, rated for PVDD, and be of type X7R.

The bootstrap capacitors (BSTx-SHx) should be placed closely to device pins to minimize loop inductance for the gate drive paths.

Bypass the AVDD pin to the AGND pin with a 1 $\mu$ F or 2.2 $\mu$ F low-ESR ceramic capacitor rated for 10V and of type X7R. Place this capacitor as close to the pin as possible and minimize the path from the capacitor to the AGND pin.

Bypass the DVDD pin to the GND pin with a 1 $\mu$ F or 2.2 $\mu$ F low-ESR ceramic capacitor rated for 10V and of type X7R. Place this capacitor as close to the pin as possible and minimize the path from the capacitor to the DGND pin.

AVDD and DVDD capacitors should have an effective capacitance between 0.5 $\mu$ F and 2.8 $\mu$ F after operating voltage (AVDD or DVDD) and temperature derating.

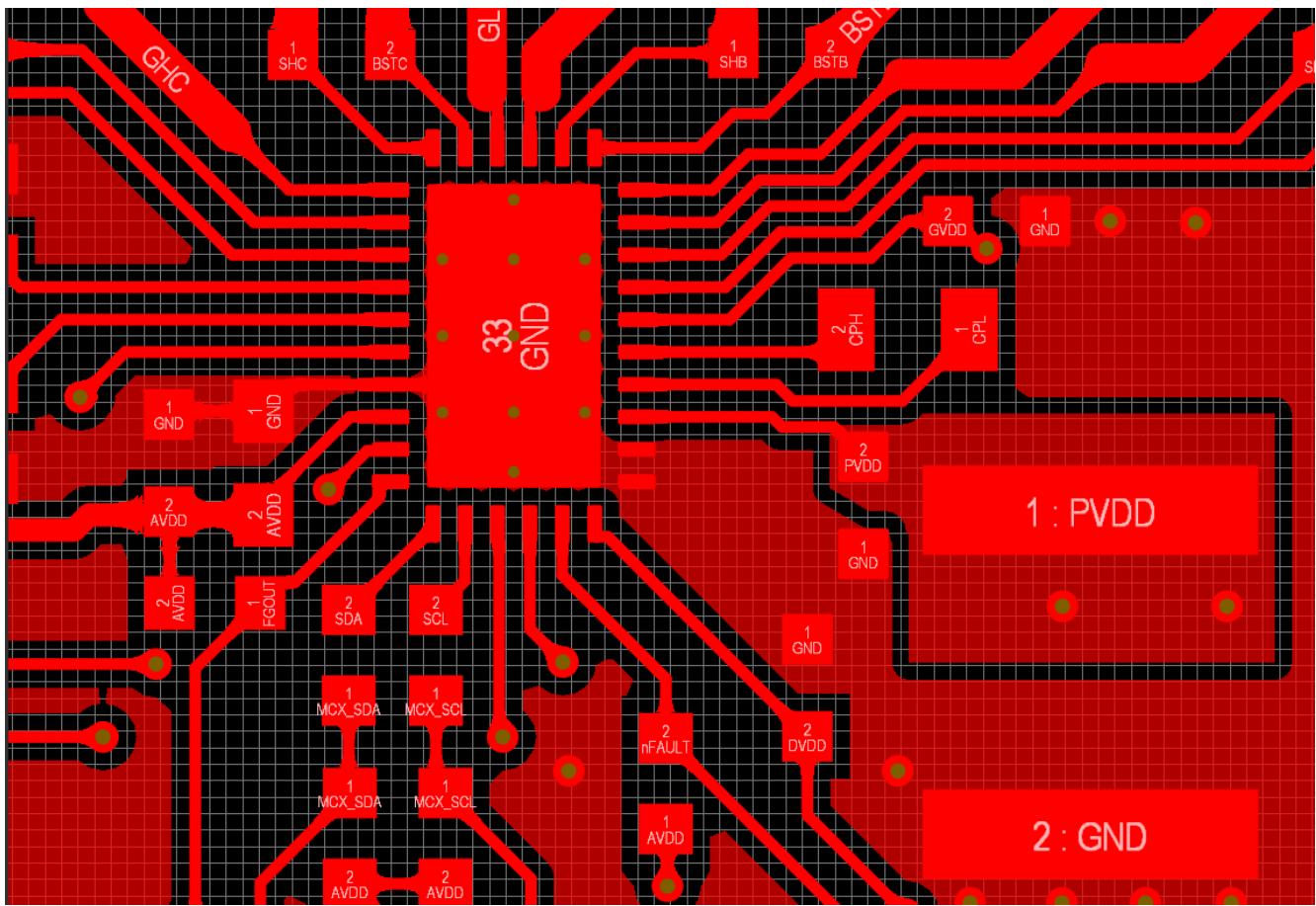
Minimize the loop length for the high-side and low-side gate drivers. The high-side loop is from the GHx pin of the device to the high-side power MOSFET gate, then follows the high-side MOSFET source back to the SHx pin. The low-side loop is from the GLx pin of the device to the low-side power MOSFET gate, then follows the low-side MOSFET source back to the GND pin.

When designing higher power systems, physics in the PCB layout can cause parasitic inductance, capacitance, and impedance that deter the performance of the system. Understanding the parasitic that are present in a higher power motor drive system can help designers mitigate their effects through good PCB layout. For more information, please visit the [System Design Considerations for High-Power Motor Driver Applications](#) and [Best Practices for Board Layout of Motor Drivers](#) application notes.

Gate drive traces (BSTx, GHx, SHx, GLx, LSS) should be at least 15-20mil wide and as short as possible to the MOSFET gates to minimize parasitic inductance and impedance. This helps supply large gate drive currents, turn MOSFETs on efficiently, and improves VGS and VDS monitoring. Ensure that the shunt resistor selected to monitor the low-side current from LSS to GND, is wide to minimize inductance introduced at the low-side source LSS.

Ensure grounds are connected through net-ties or wide resistors to reduce voltage offsets and maintain gate driver performance. The device thermal pad should be soldered to the PCB top-layer ground plane. Multiple vias should be used to connect to a large bottom-layer ground plane. The use of large metal planes and multiple vias helps dissipate the heat that is generated in the device. To improve thermal performance, maximize the ground area that is connected to the thermal pad ground across all possible layers of the PCB. Using thick copper pours can lower the junction-to-air thermal resistance and improve thermal dissipation from the die surface.

## 10.4.2 Layout Example



**Figure 10-11. Layout example of MCF8329HS-Q1**

### 10.4.3 Thermal Considerations

The MCF8329HS-Q1 has thermal shutdown (TSD) as previously described. A die temperature in excess of 150°C (minimally) disables the device until the temperature drops to a safe level.

Any tendency of the device to enter thermal shutdown is an indication of excessive power dissipation, insufficient heat-sinking, or too high an ambient temperature.

#### 10.4.3.1 Power Dissipation

The MCF8329HS-Q1 integrates a variety of circuits that contribute to total power losses. These power losses include standby power losses, GVDD power losses, AVDD power losses, DVDD power losses. At start-up and fault conditions, this current is much higher than normal running current; remember to take these peak currents and their duration into consideration. The maximum amount of power that the device can dissipate depends on ambient temperature and heat-sinking.

## 11 Device and Documentation Support

### 11.1 Documentation Support

#### 11.1.1 Related Documentation

- Refer to the application note [Power Delivery in Cordless Power Tools Using DRV8329](#)
- Refer to the application note [System Design Considerations for High-Power Motor Driver Applications](#)
- Refer to the E2E FAQ [How to Conduct a BLDC Schematic Review and Debug](#)
- Refer to the application note [Best Practices for Board Layout of Motor Drivers](#)
- Refer to the application note [QFN and SON PCB Attachment](#)
- Refer to the application note [Cut-Off Switch in High-Current Motor-Drive Applications](#)

### 11.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 11.3 Trademarks

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### 11.4 Electrostatic Discharge Caution

 This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 11.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated device. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

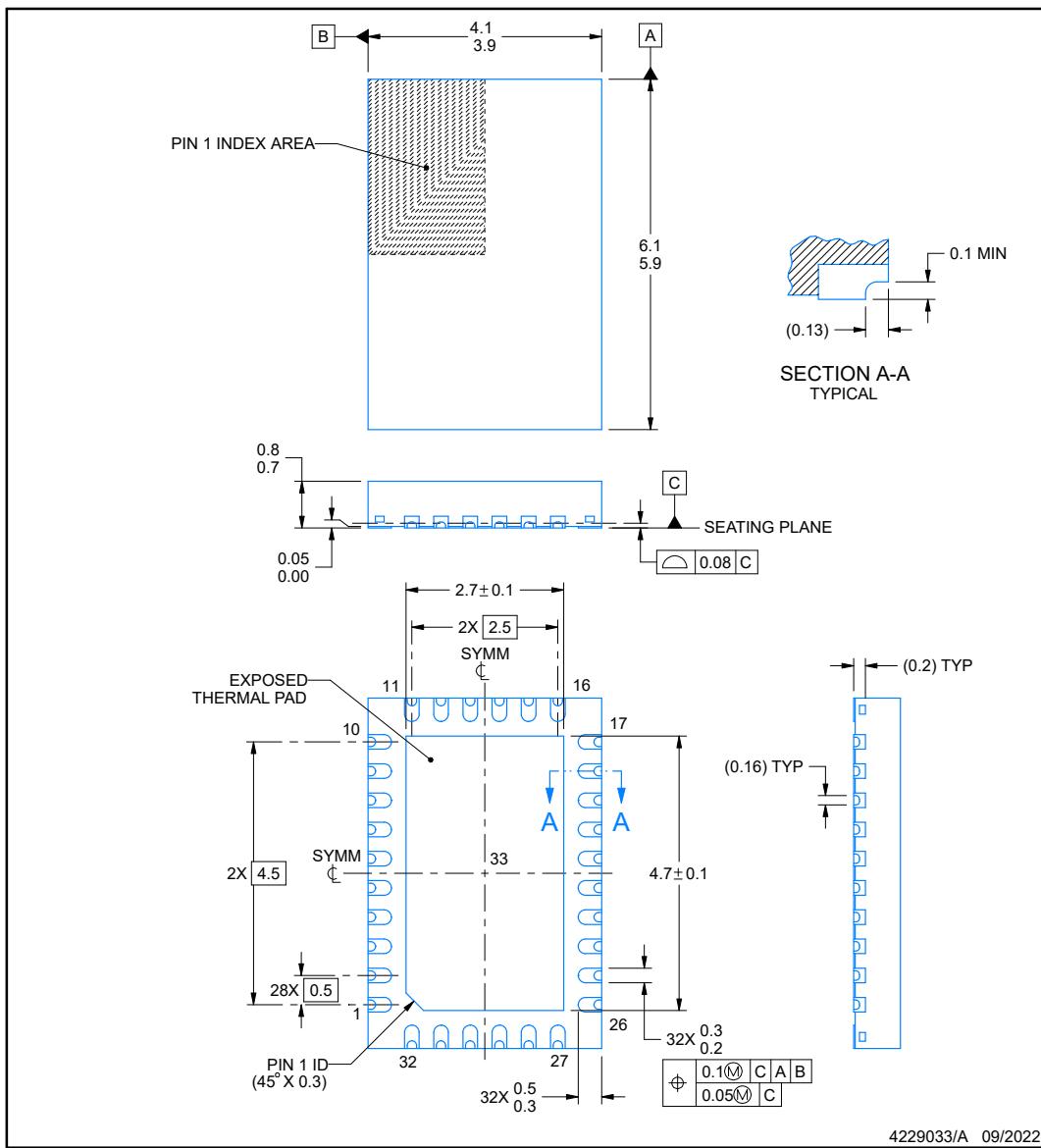
## RRY0032A



### PACKAGE OUTLINE

#### WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



4229033/A 09/2022

#### NOTES:

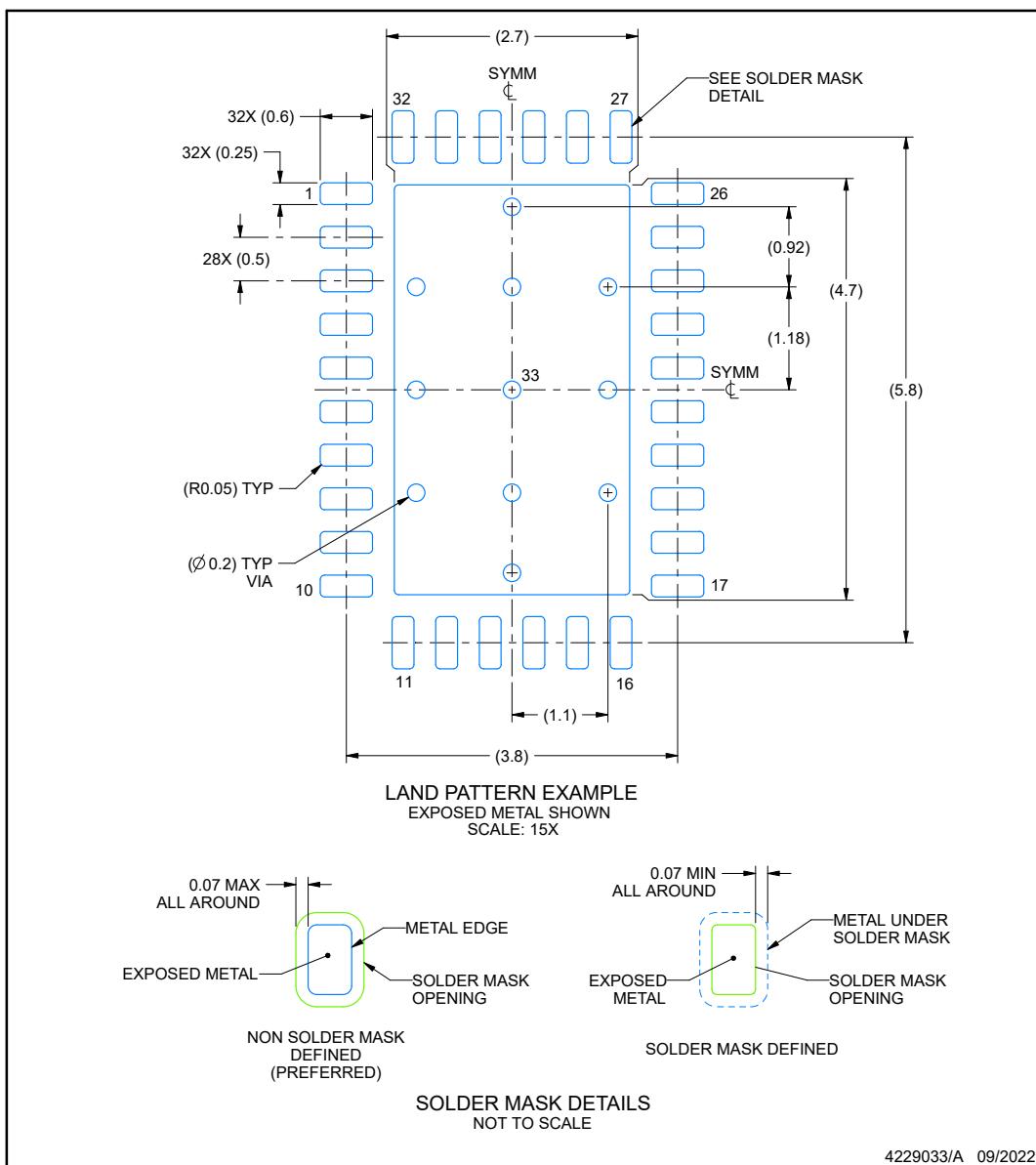
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

## EXAMPLE BOARD LAYOUT

**RRY0032A**

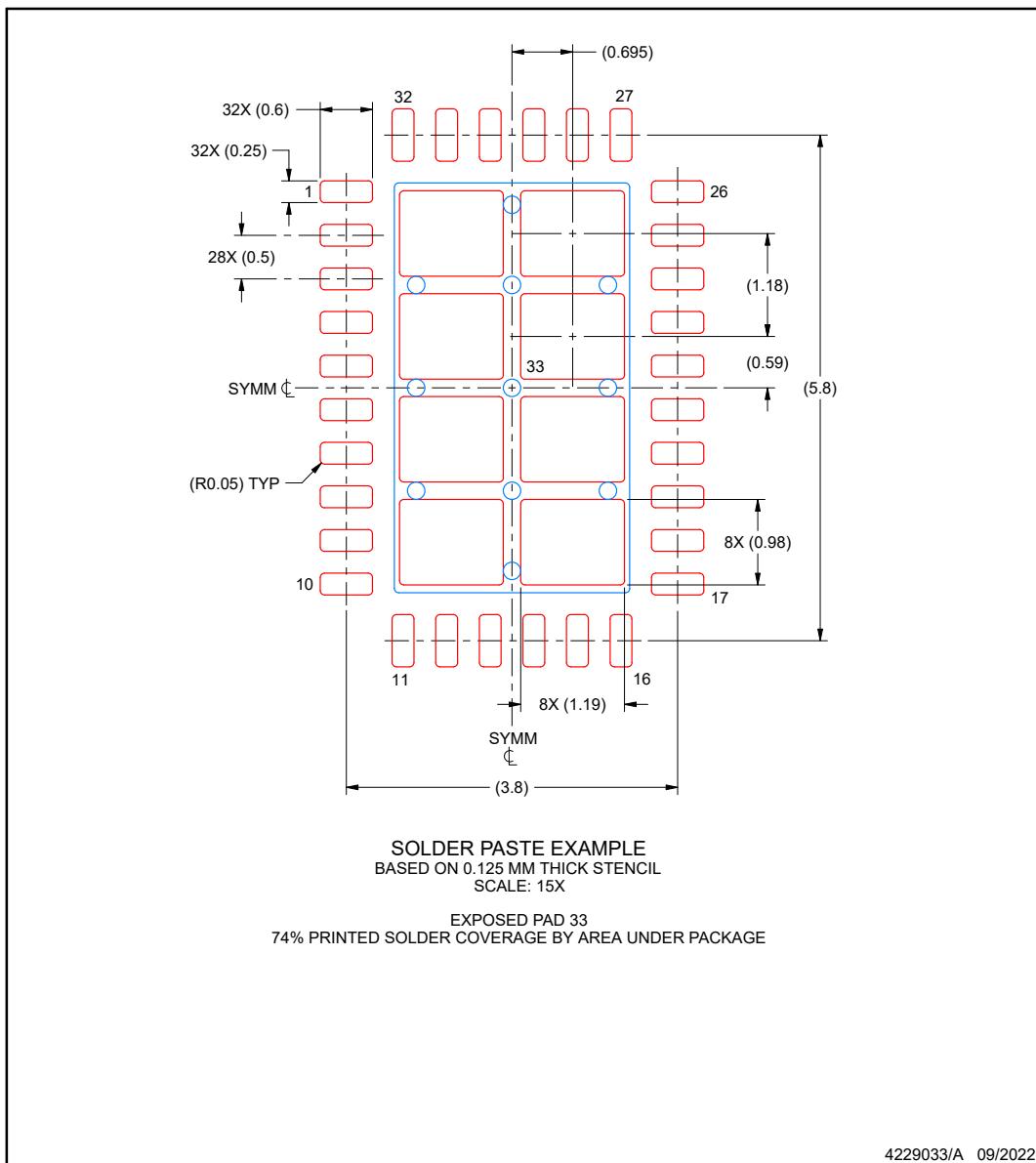
**WQFN - 0.8 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



**EXAMPLE STENCIL DESIGN**  
**RRY0032A** **WQFN - 0.8 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
MCF8329HSIQRRYRQ1	Active	Production	WQFN (RRY)   32	5000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MCF8329 HSIQ

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## GENERIC PACKAGE VIEW

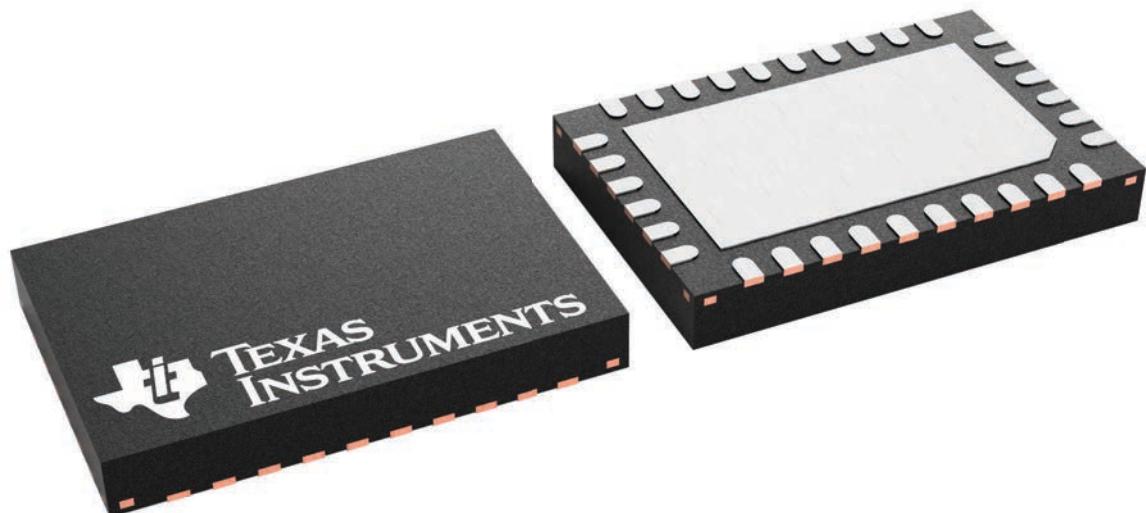
**RRY 32**

**WQFN - 0.8 mm max height**

**4 x 6, 0.5 mm pitch**

**PLASTIC QUAD FLATPACK - NO LEAD**

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4229624/A

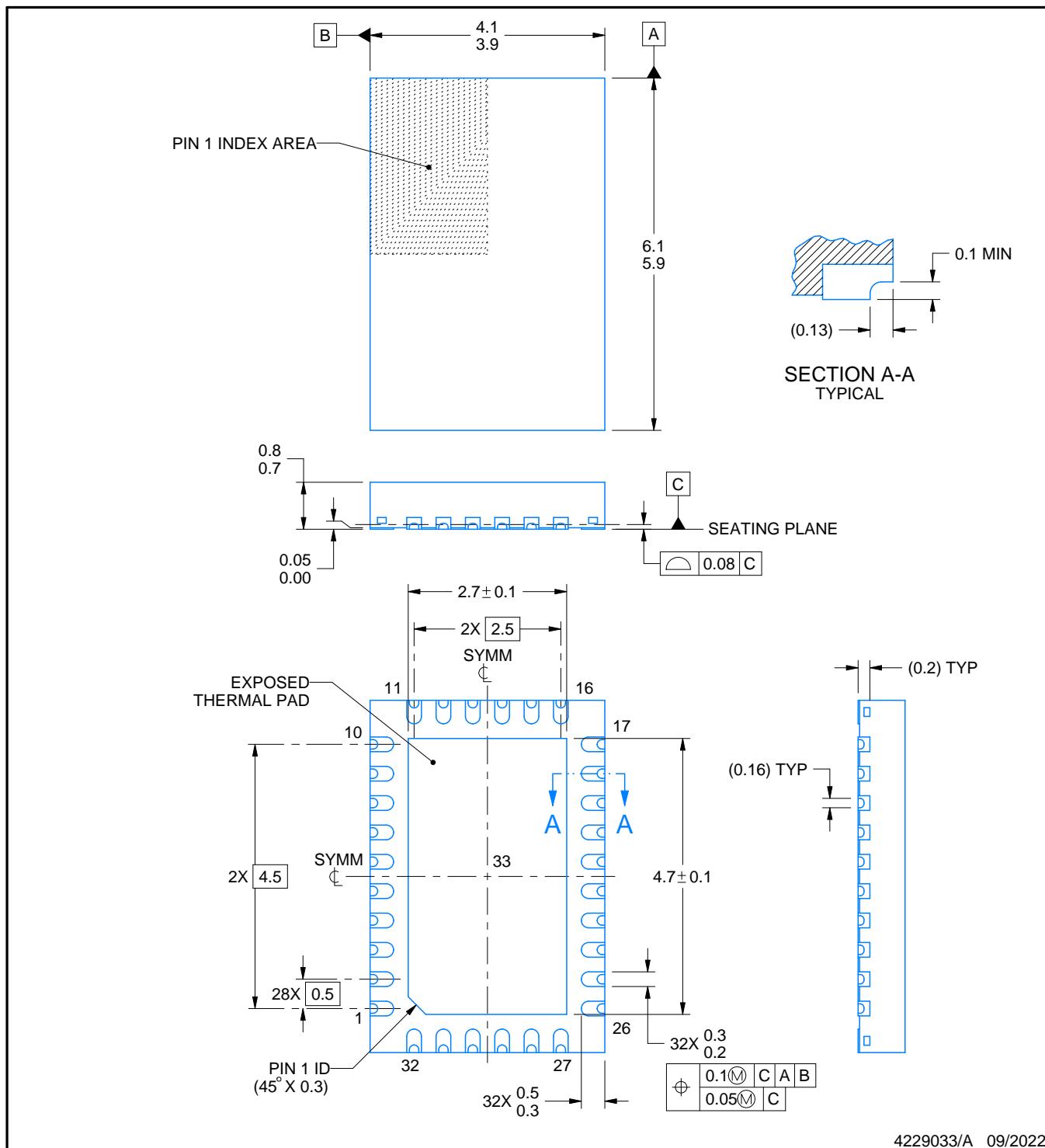
## PACKAGE OUTLINE

**RRY0032A**



## WQFN - 0.8 mm max height

#### PLASTIC QUAD FLATPACK - NO LEAD



4229033/A 09/2022

## NOTES:

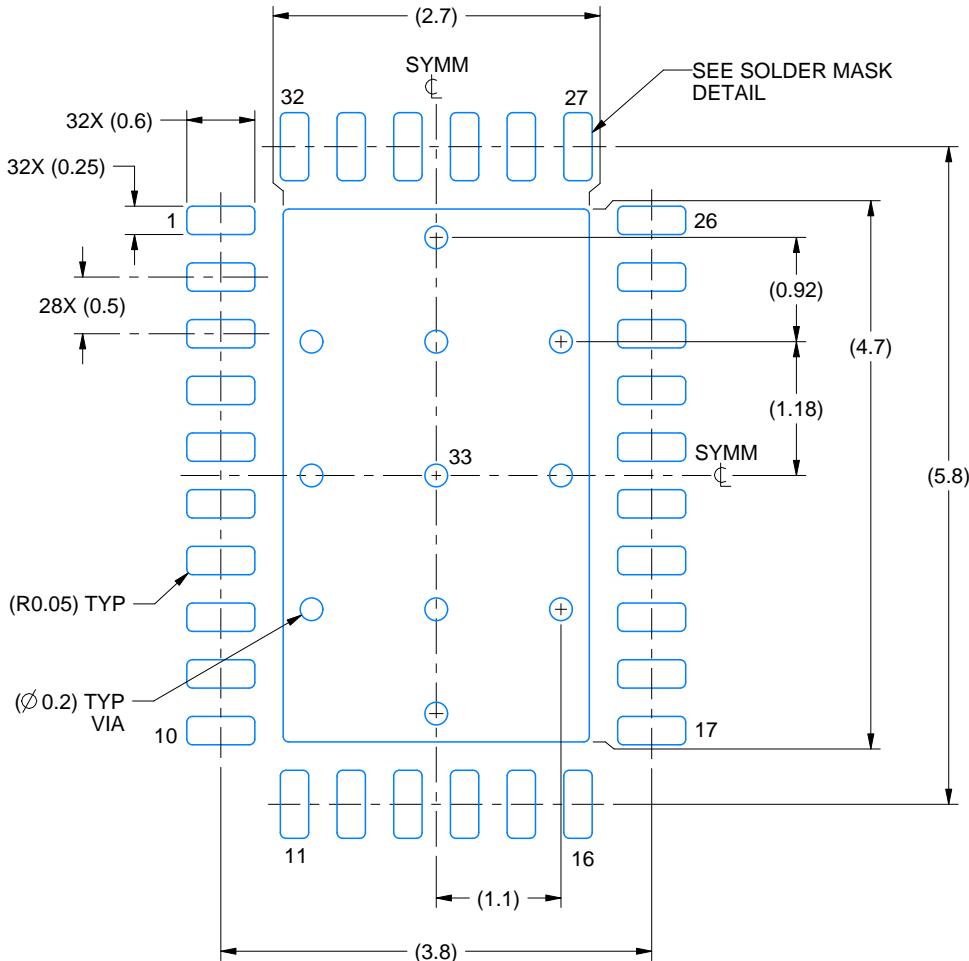
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

## EXAMPLE BOARD LAYOUT

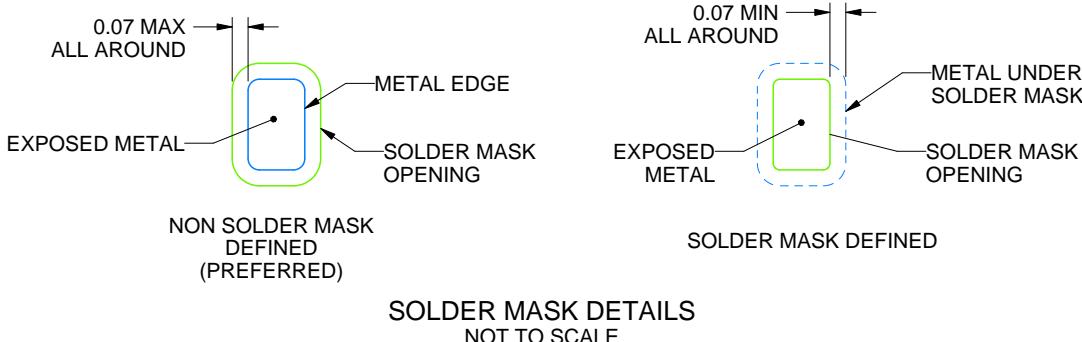
RRY0032A

## **WQFN - 0.8 mm max height**

#### PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 15X



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#### NOTES: (continued)

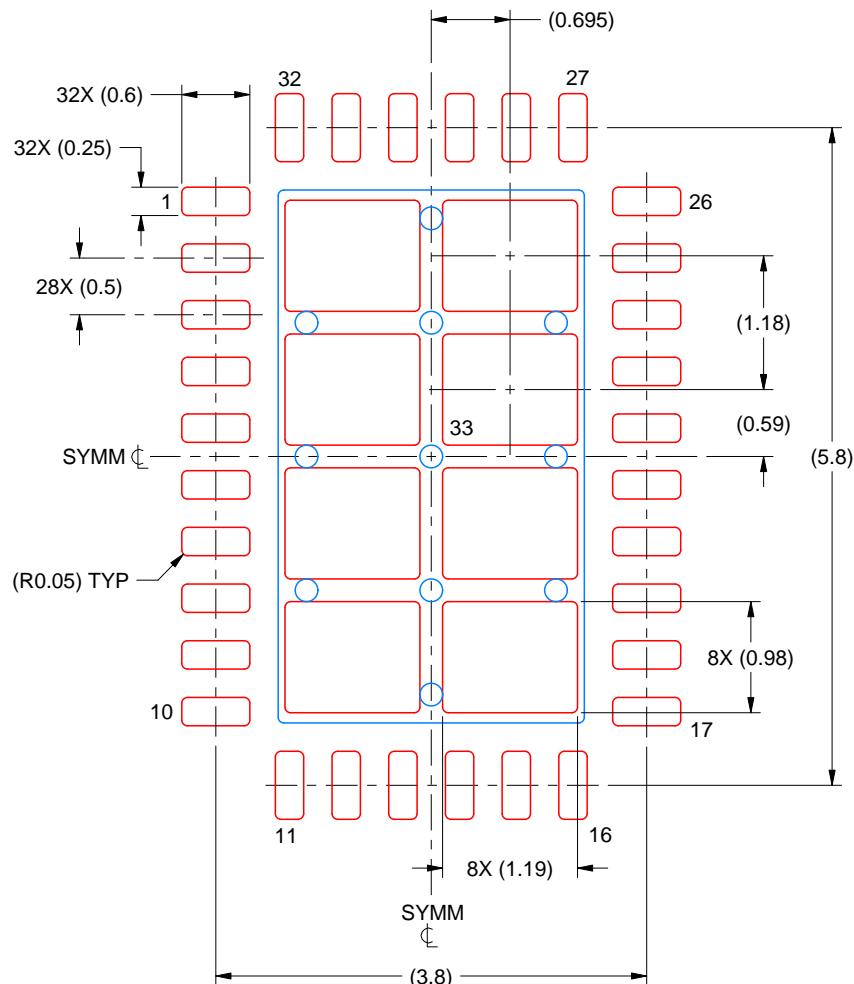
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

## EXAMPLE STENCIL DESIGN

RRY0032A

## **WQFN - 0.8 mm max height**

## PLASTIC QUAD FLATPACK - NO LEAD



**SOLDER PASTE EXAMPLE  
BASED ON 0.125 MM THICK STENCIL  
SCALE: 15X**

EXPOSED PAD 33  
74% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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#### NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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