

## LT1013x Dual Precision Operational Amplifier

### 1 Features

- Single-Supply Operation
  - Input Voltage Range Extends to Ground
  - Output Swings to Ground While Sinking Current
- Phase Reversal Protection
- Input Offset Voltage
  - 150  $\mu\text{V}$  Maximum at 25°C for LT1013AM
- Offset-Voltage Temperature Coefficient
  - 2  $\mu\text{V}/^\circ\text{C}$  Maximum for LT1013AM
- Input Offset Current
  - 0.8 nA Maximum at 25°C for LT1013AM
- High Gain
  - 1.5  $\text{V}/\mu\text{V}$  Minimum ( $R_L = 2 \text{ k}\Omega$ ) for LT1013AM
  - 0.8  $\text{V}/\mu\text{V}$  Minimum ( $R_L = 600 \text{ k}\Omega$ ) for LT1013AM
- Low Supply Current
  - 0.5 mA Maximum at  $T_A = 25^\circ\text{C}$  for LT1013AM
- Low Peak-to-Peak Noise Voltage
  - 0.55  $\mu\text{V}$  Typical
- Low Current Noise
  - 0.07  $\text{pA}/\sqrt{\text{Hz}}$  Typical
- For Die Only Option, See [LT1013-DIE](#)

### 2 Applications

- Thermocouple Amplifiers
- Low-Side Current Measurement
- Instrumentation Amplifiers

### 3 Description

The LT1013x devices are dual precision operational amplifiers, featuring high gain, low supply current, low noise, and low-offset-voltage temperature coefficient.

The LT1013x devices can be operated from a single 5-V power supply; the common-mode input voltage range includes ground, and the output can also swing to within a few millivolts of ground. Crossover distortion is eliminated. The LT1013x can be operated with both dual  $\pm 15\text{-V}$  and single 5-V supplies.

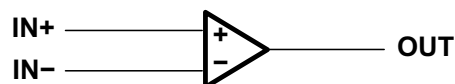
The LT1013C and LT1013D are characterized for operation from 0°C to 70°C. The LT1013DI is characterized for operation from  $-40^\circ\text{C}$  to 105°C. The LT1013M, LT1013AM, and LT1013DM are characterized for operation over the full military temperature range of  $-55^\circ\text{C}$  to 125°C.

**Device Information<sup>(1)</sup>**

PART NUMBER	PACKAGE (PINS)	BODY SIZE (NOM)
LT1013D LT1013DD	SOIC (8)	4.90 mm x 3.91 mm
LT1013P LT1013DP	PDIP (8)	9.81 mm x 6.35 mm
LT1013MFK LT1013AMFK	LCCC (20)	8.89 mm x 8.89 mm
LT1013MJG LT1013AMJG	CDIP (8)	9.60 mm x 6.67 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### Symbol (Each Amplifier)



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## 4 Revision History

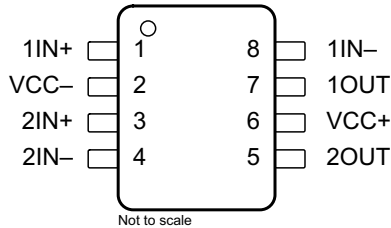
### Changes from Revision H (November 2004) to Revision I

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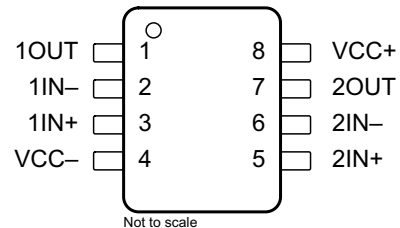
- |  |                      |
|--|----------------------|
| <ul style="list-style-type: none"> <li>Added <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i>, <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section. ....</li> <li>Removed <i>Ordering Information</i> table, see POA at the end of the data sheet .....</li> </ul> | <b>1</b><br><b>1</b> |
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## 5 Pin Configuration and Functions

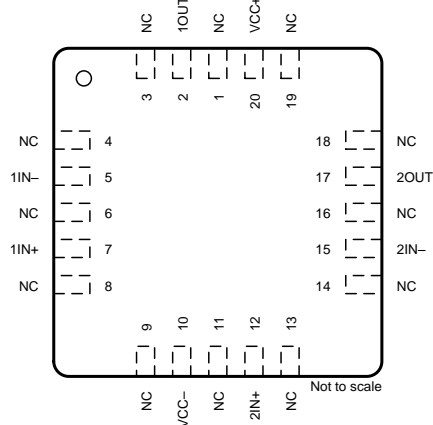
**LT1013 and LT1013D D Package  
8-Pin SOIC  
Top View**



**LT1013M and LT1013AM JG Package  
or LT1013 and LT1013D P Package  
8-Pin CDIP or PDIP  
Top View**



**LT1013M and LT1013AM FK Package  
20-Pin LCCC  
Top View**



### Pin Functions

NAME	PIN			I/O	DESCRIPTION
	SOIC	LCCC	CDIP, PDIP		
1IN+	1	7	3	I	Noninverting input for channel 1
1IN-	8	5	2	I	Inverting input for channel 1
1OUT	7	2	1	O	Output for channel 1
2IN+	3	12	5	I	Noninverting input for channel 2
2IN-	4	15	6	I	Inverting input for channel 2
2OUT	5	17	7	O	Output for channel 2
NC	—	1, 3, 4, 6, 8, 9, 11, 13, 14, 16, 18, 19	—	—	No internal connection
VCC+	6	20	8	—	Positive supply Voltage
VCC-	2	10	4	—	Negative supply Voltage

## 6 Specifications

### 6.1 Absolute Maximum Ratings

 over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
$V_{CC+} - V_{CC-}$	Supply voltage <sup>(2)</sup>	-0.3	44	V
$V_I$	Input voltage (any input)	$V_{CC-} - 5$	$V_{CC+}$	V
	Differential input voltage <sup>(3)</sup>		$\pm 30$	V
	Duration of short-circuit current at (or below) 25°C <sup>(4)</sup>	Unlimited		
	Case temperature for 60 s	FK package	260	°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 s	JG package	300	°C
$T_J$	Operating virtual junction temperature		150	°C
$T_{stg}$	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Supply voltage is  $V_{CC+}$  with respect to  $V_{CC-}$ .
- (3) Differential voltage is  $IN+$  with respect to  $IN-$ .
- (4) The output may be shorted to either supply.

### 6.2 ESD Ratings

		VALUE	UNIT
<b>LT1013 in D and P packages</b>			
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	$\pm 1000$
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	$\pm 500$
<b>LT1013D in D and P packages</b>			
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	$\pm 1000$
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	$\pm 500$

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{CC+} - V_{CC-}$	Supply voltage	5	30	V
$T_A$	Ambient temperature	LT1013C, LT1013D	0	70
		LT1013DI	-40	105
		LT1013M, LT1013AM, LT1013DM	-55	125
$V_{ICM}$	Input common-mode voltage	LT1013C, LT1013D, LT1013DI	$V_{CC-}$	$V_{CC+} - 2$
		LT1013M, LT1013AM, LT1013DM	$V_{CC-} + 0.1$	$V_{CC+} - 2$

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>	LT1013x				UNIT
	D (SOIC)	P (PDIP)	FK (LCCC)	JG (CDIP)	
	8 PINS	8 PINS	20 PINS	8 PINS	
R <sub>θJA</sub> Junction-to-ambient thermal resistance <sup>(2)(3)</sup>	101.6	49.5	—	—	°C/W
R <sub>θJC(top)</sub> Junction-to-case (top) thermal resistance	47.6	38.7	35.7 <sup>(4)</sup>	58.5 <sup>(4)</sup>	°C/W
R <sub>θJB</sub> Junction-to-board thermal resistance	42	26.7	34.8	82.9	°C/W
ψ <sub>JT</sub> Junction-to-top characterization parameter	8.3	15.9	—	—	°C/W
ψ <sub>JB</sub> Junction-to-board characterization parameter	41.5	26.6	—	—	°C/W
R <sub>θJC(bot)</sub> Junction-to-case (bottom) thermal resistance	—	—	4.0 <sup>(4)</sup>	10.8 <sup>(4)</sup>	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
- (2) Maximum power dissipation is a function of T<sub>J(max)</sub>, R<sub>θJA</sub>, and T<sub>A</sub>. The maximum allowable power dissipation at any allowable ambient temperature is P<sub>D</sub> = (T<sub>J(max)</sub> – T<sub>A</sub>) / R<sub>θJA</sub>. Operating at the absolute maximum T<sub>J</sub> of 150°C can affect reliability. Due to variation in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.
- (4) R<sub>θJC(top)</sub> and R<sub>θJC(bot)</sub> thermal impedances are calculated in accordance with MIL-STD-883 for LCCC and CDIP

## 6.5 Electrical Characteristics: LT1013C, ±15 V

at specified free-air temperature, V<sub>CC±</sub> = ±15 V, V<sub>IC</sub> = 0 (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T <sub>A</sub> <sup>(1)</sup>	MIN	TYP <sup>(2)</sup>	MAX	UNIT
V <sub>IO</sub> Input offset voltage	R <sub>S</sub> = 50 Ω	25°C		60	300	μV
		Full range			400	
α <sub>VIO</sub> Temperature coefficient of input offset voltage		Full range		0.4	2.5	μV/°C
	Long-term drift of input offset voltage	25°C		0.5		μV/mo
I <sub>IO</sub> Input offset current		25°C		0.2	1.5	nA
		Full range			2.8	
I <sub>IB</sub> Input bias current		25°C		–15	–30	nA
		Full range			–38	
V <sub>ICR</sub> Common-mode input voltage range	Recommended range	25°C	–15		13.5	V
		Full range	–15		13	
V <sub>OM</sub> Maximum peak output voltage swing	R <sub>L</sub> = 2 kΩ	25°C	±12.5	±14		V
		Full range	±12			
A <sub>VD</sub> Large-signal differential voltage amplification	V <sub>O</sub> = ±10 V, R <sub>L</sub> = 600 Ω	25°C	0.5	0.2		V/μV
	V <sub>O</sub> = ±10 V, R <sub>L</sub> = 2 kΩ	25°C	1.2	7		
		Full range	0.7			
CMRR Common-mode rejection ratio	V <sub>IC</sub> = –15 V to 13.5 V	25°C	97	114		dB
	V <sub>IC</sub> = –14.9 V to 13 V	Full range	94			
k <sub>SVR</sub> Supply-voltage rejection ratio (ΔV <sub>CC</sub> /ΔV <sub>IO</sub> )	V <sub>CC±</sub> = ±2 V to ±18 V	25°C	100	117		dB
		Full range	97			
Channel separation	V <sub>O</sub> = ±10 V, R <sub>L</sub> = 2 kΩ	25°C	120	137		dB
r <sub>id</sub> Differential input resistance		25°C	70	300		MΩ
r <sub>ic</sub> Common-mode input resistance		25°C		4		GΩ
I <sub>CC</sub> Supply current per amplifier		25°C		0.35	0.55	mA
		Full range			0.7	

- (1) Full range is 0°C to 70°C.
- (2) All typical values are at T<sub>A</sub> = 25°C.

## 6.6 Electrical Characteristics: LT1013C, 5 V

 at specified free-air temperature,  $V_{CC+} = 5\text{ V}$ ,  $V_{CC-} = 0$ ,  $V_O = 1.4\text{ V}$ ,  $V_{IC} = 0$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	$T_A^{(1)}$	MIN	TYP <sup>(2)</sup>	MAX	UNIT
$V_{IO}$	Input offset voltage	$R_S = 50\ \Omega$	25°C		90	450	$\mu\text{V}$
			Full range			570	
$I_{IO}$	Input offset current		25°C		0.3	2	nA
			Full range			6	
$I_{IB}$	Input bias current		25°C		-18	-50	nA
			Full range			-90	
$V_{ICR}$	Common-mode input voltage range	Recommended range	25°C	0		3.5	V
			Full range	0		3	
$V_{OM}$	Maximum peak output voltage swing	Output low, No load	25°C		15	25	V
			25°C		5	10	
			Full range			13	
			25°C		220	350	
			25°C	4	4.4		
			Full range	3.4	4		
$A_{VD}$	Large-signal differential voltage amplification	$V_O = 5\text{ mV to }4\text{ V}$ , $R_L = 500\ \Omega$	25°C		1		$\text{V}/\mu\text{V}$
			Full range			3.2	
$I_{CC}$	Supply current per amplifier		25°C		0.32	0.5	mA
			Full range			0.55	

(1) Full range is 0°C to 70°C.

 (2) All typical values are at  $T_A = 25^\circ\text{C}$ .

## 6.7 Electrical Characteristics: LT1013D, $\pm 15\text{ V}$

 at specified free-air temperature,  $V_{CC\pm} = \pm 15\text{ V}$ ,  $V_{IC} = 0$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	$T_A^{(1)}$	MIN	TYP <sup>(2)</sup>	MAX	UNIT
$V_{IO}$	Input offset voltage	$R_S = 50\ \Omega$	25°C		200	800	$\mu\text{V}$
			Full range			1000	
$\alpha_{VIO}$	Temperature coefficient of input offset voltage		Full range		0.7	5	$\mu\text{V}/^\circ\text{C}$
			Long-term drift of input offset voltage	25°C		0.5	
$I_{IO}$	Input offset current		25°C		0.2	1.5	nA
			Full range			2.8	
$I_{IB}$	Input bias current		25°C		-15	-30	nA
			Full range			-38	
$V_{ICR}$	Common-mode input voltage range	Recommended range	25°C	-15		13.5	V
			Full range	-15		13	
$V_{OM}$	Maximum peak output voltage swing	$R_L = 2\ \text{k}\Omega$	25°C	$\pm 12.5$	$\pm 14$		V
			Full range	$\pm 12$			
$A_{VD}$	Large-signal differential voltage amplification	$V_O = \pm 10\text{ V}$ , $R_L = 600\ \Omega$	25°C	0.5	2		$\text{V}/\mu\text{V}$
			25°C	1.2	7		
			Full range	0.7			
CMRR	Common-mode rejection ratio	$V_{IC} = -15\text{ V to }13.5\text{ V}$	25°C	97	114		dB
			Full range	94			
$k_{SVR}$	Supply-voltage rejection ratio ( $\Delta V_{CC}/\Delta V_{IO}$ )	$V_{CC+} = \pm 2\text{ V to } \pm 18\text{ V}$	25°C	100	117		dB
			Full range	97			
	Channel separation	$V_O = \pm 10\text{ V}$ , $R_L = 2\ \text{k}\Omega$	25°C	120	137		dB
$r_{id}$	Differential input resistance		25°C	70	300		$\text{M}\Omega$
$r_{ic}$	Common-mode input resistance		25°C		4		$\text{G}\Omega$
$I_{CC}$	Supply current per amplifier		25°C		0.35	0.55	mA
			Full range			0.6	

(1) Full range is 0°C to 70°C.

 (2) All typical values are at  $T_A = 25^\circ\text{C}$ .

## 6.8 Electrical Characteristics: LT1013D, 5 V

 at specified free-air temperature,  $V_{CC+} = 5\text{ V}$ ,  $V_{CC-} = 0$ ,  $V_O = 1.4\text{ V}$ ,  $V_{IC} = 0$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	$T_A^{(1)}$	MIN	TYP <sup>(2)</sup>	MAX	UNIT
$V_{IO}$	Input offset voltage	$R_S = 50\ \Omega$	25°C		250	950	$\mu\text{V}$
			Full range			1200	
$I_{IO}$	Input offset current		25°C		0.3	2	nA
			Full range			6	
$I_{IB}$	Input bias current		25°C		-18	-50	nA
			Full range			-90	
$V_{ICR}$	Common-mode input voltage range	Recommended range	25°C	0		3.5	V
			Full range	0		3	
$V_{OM}$	Maximum peak output voltage swing	Output low, No load	25°C		15	25	V
			25°C		5	10	
			Full range			13	
			25°C		220	350	
			25°C	4	4.4		
			Full range	3.4	4		
$A_{VD}$	Large-signal differential voltage amplification	$V_O = 5\text{ mV to }4\text{ V}$ , $R_L = 500\ \Omega$	25°C		1		$\text{V}/\mu\text{V}$
			Full range				
$I_{CC}$	Supply current per amplifier		25°C		0.32	0.5	mA
			Full range			0.55	

(1) Full range is 0°C to 70°C.

 (2) All typical values are at  $T_A = 25^\circ\text{C}$ .

## 6.9 Electrical Characteristics: LT1013DI, $\pm 15\text{ V}$

 at specified free-air temperature,  $V_{CC\pm} = \pm 15\text{ V}$ ,  $V_{IC} = 0$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	$T_A^{(1)}$	MIN	TYP <sup>(2)</sup>	MAX	UNIT
$V_{IO}$	Input offset voltage	$R_S = 50\ \Omega$	25°C		200	800	$\mu\text{V}$
			Full range			1000	
$\alpha_{VIO}$	Temperature coefficient of input offset voltage		Full range		0.7	5	$\mu\text{V}/^\circ\text{C}$
			Long-term drift of input offset voltage	25°C		0.5	
$I_{IO}$	Input offset current		25°C		0.2	1.5	nA
			Full range			2.8	
$I_{IB}$	Input bias current		25°C		-15	-30	nA
			Full range			-38	
$V_{ICR}$	Common-mode input voltage range	Recommended range	25°C	-15		13.5	V
			Full range	-15		13	
$V_{OM}$	Maximum peak output voltage swing	$R_L = 2\text{ k}\Omega$	25°C	$\pm 12.5$	$\pm 14$		V
			Full range	$\pm 12$			
$A_{VD}$	Large-signal differential voltage amplification	$V_O = \pm 10\text{ V}$ , $R_L = 600\ \Omega$	25°C	0.5	0.2		$\text{V}/\mu\text{V}$
			25°C	1.2	7		
			Full range	0.7			
CMRR	Common-mode rejection ratio	$V_{IC} = -15\text{ V to }13.5\text{ V}$	25°C	97	114		dB
			Full range	94			
$k_{SVR}$	Supply-voltage rejection ratio ( $\Delta V_{CC}/\Delta V_{IO}$ )	$V_{CC+} = \pm 2\text{ V to } \pm 18\text{ V}$	25°C	100	117		dB
			Full range	97			
	Channel separation	$V_O = \pm 10\text{ V}$ , $R_L = 2\text{ k}\Omega$	25°C	120	137		dB
$r_{id}$	Differential input resistance		25°C	70	300		$\text{M}\Omega$
$r_{ic}$	Common-mode input resistance		25°C		4		$\text{G}\Omega$
$I_{CC}$	Supply current per amplifier		25°C		0.35	0.55	mA
			Full range			0.6	

 (1) Full range is  $-40^\circ\text{C}$  to  $105^\circ\text{C}$ .

 (2) All typical values are at  $T_A = 25^\circ\text{C}$ .

## 6.10 Electrical Characteristics: LT1013DI, 5 V

 at specified free-air temperature,  $V_{CC+} = 5\text{ V}$ ,  $V_{CC-} = 0$ ,  $V_O = 1.4\text{ V}$ ,  $V_{IC} = 0$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	$T_A^{(1)}$	MIN	TYP <sup>(2)</sup>	MAX	UNIT
$V_{IO}$	Input offset voltage	$R_S = 50\ \Omega$	25°C		250	950	$\mu\text{V}$
			Full range			1200	
$I_{IO}$	Input offset current		25°C		0.3	2	nA
			Full range			6	
$I_{IB}$	Input bias current		25°C		-18	-50	nA
			Full range			-90	
$V_{ICR}$	Common-mode input voltage range	Recommended range	25°C	0		3.5	V
			Full range	0		3	
$V_{OM}$	Maximum peak output voltage swing	Output low, No load	25°C		15	25	V
			25°C		5	10	
			Full range			13	
			25°C		220	350	
			25°C	4	4.4		
			25°C	3.4	4		
$A_{VD}$	Large-signal differential voltage amplification	$V_O = 5\text{ mV to }4\text{ V}$ , $R_L = 500\ \Omega$	25°C		1		$\text{V}/\mu\text{V}$
			Full range			0.32	
$I_{CC}$	Supply current per amplifier		25°C				mA
			Full range				

 (1) Full range is  $-40^\circ\text{C}$  to  $105^\circ\text{C}$ .

 (2) All typical values are at  $T_A = 25^\circ\text{C}$ .

## 6.11 Electrical Characteristics: LT1013M, $\pm 15\text{ V}$

 at specified free-air temperature,  $V_{CC\pm} = \pm 15\text{ V}$ ,  $V_{IC} = 0$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	$T_A^{(1)}$	MIN	TYP <sup>(2)</sup>	MAX	UNIT
$V_{IO}$	Input offset voltage	$R_S = 50\ \Omega$	25°C		60	300	$\mu\text{V}$
			Full range			550	
$\alpha_{VIO}$	Temperature coefficient of input offset voltage		Full range		0.5	2.5 <sup>(3)</sup>	$\mu\text{V}/^\circ\text{C}$
			25°C		0.5		
$I_{IO}$	Input offset current		25°C		0.2	1.5	nA
			Full range			5	
$I_{IB}$	Input bias current		25°C		-15	-30	nA
			Full range			-45	
$V_{ICR}$	Common-mode input voltage range	Recommended range	25°C	-15		13.5	V
			Full range	-14.9		13	
$V_{OM}$	Maximum peak output voltage swing	$R_L = 2\text{ k}\Omega$	25°C	$\pm 12.5$	$\pm 14$		V
			Full range	$\pm 11.5$			
$A_{VD}$	Large-signal differential voltage amplification	$V_O = \pm 10\text{ V}$ , $R_L = 600\ \Omega$	25°C	0.5	2		$\text{V}/\mu\text{V}$
			25°C	1.2	7		
			Full range	0.25			
CMRR	Common-mode rejection ratio	$V_{IC} = -15\text{ V to }13.5\text{ V}$	25°C	97	117		dB
			Full range	94			
$k_{SVR}$	Supply-voltage rejection ratio ( $\Delta V_{CC}/\Delta V_{IO}$ )	$V_{CC+} = \pm 2\text{ V to } \pm 18\text{ V}$	25°C	100	117		dB
			Full range	97			
	Channel separation	$V_O = \pm 10\text{ V}$ , $R_L = 2\text{ k}\Omega$	25°C	120	137		dB
$r_{id}$	Differential input resistance		25°C	70	300		$\text{M}\Omega$
$r_{ic}$	Common-mode input resistance		25°C		4		$\text{G}\Omega$
$I_{CC}$	Supply current per amplifier		25°C		0.35	0.55	mA
			Full range			0.7	

 (1) Full range is  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ .

 (2) All typical values are at  $T_A = 25^\circ\text{C}$ .

(3) On products compliant to MIL-PRF-38535, Class B, this parameter is not production tested.

## 6.12 Electrical Characteristics: LT1013M, 5 V

 at specified free-air temperature,  $V_{CC+} = 5\text{ V}$ ,  $V_{CC-} = 0$ ,  $V_O = 1.4\text{ V}$ ,  $V_{IC} = 0$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	$T_A^{(1)}$	MIN	TYP <sup>(2)</sup>	MAX	UNIT
$V_{IO}$	Input offset voltage	$R_S = 50\ \Omega$	25°C		90	450	$\mu\text{V}$
			Full range		400	1500	
		$R_S = 50\ \Omega$ , $V_{IC} = 0.1\text{ V}$	125°C		200	750	
$I_{IO}$	Input offset current		25°C		0.3	2	nA
			Full range			10	
$I_{IB}$	Input bias current		25°C		-18	-50	nA
			Full range			-120	
$V_{ICR}$	Common-mode input voltage range	Recommended range	25°C	0		3.5	V
			Full range		0	3	
$V_{OM}$	Maximum peak output voltage swing	Output low, No load	25°C		15	25	V
			25°C		5	10	
			Full range			18	
			25°C		220	350	
			25°C	4	4.4		
			Full range	3.1	4		
$A_{VD}$	Large-signal differential voltage amplification	$V_O = 5\text{ mV to }4\text{ V}$ , $R_L = 500\ \Omega$	25°C		1		V/ $\mu\text{V}$
			Full range				
$I_{CC}$	Supply current per amplifier		25°C		0.32	0.5	mA
			Full range			0.65	

 (1) Full range is  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ .

 (2) All typical values are at  $T_A = 25^\circ\text{C}$ .

## 6.13 Electrical Characteristics: LT1013AM, $\pm 15\text{ V}$

 at specified free-air temperature,  $V_{CC\pm} = \pm 15\text{ V}$ ,  $V_{IC} = 0$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	$T_A^{(1)}$	MIN	TYP <sup>(2)</sup>	MAX	UNIT
$V_{IO}$	Input offset voltage	$R_S = 50\ \Omega$	25°C		40	150	$\mu\text{V}$
			Full range			300	
$\alpha_{VIO}$	Temperature coefficient of input offset voltage		Full range		0.4	2 <sup>(3)</sup>	$\mu\text{V}/^\circ\text{C}$
			25°C		0.4		
$I_{IO}$	Input offset current		25°C		0.15	0.8	nA
			Full range			2.5	
$I_{IB}$	Input bias current		25°C		-12	-20	nA
			Full range			-30	
$V_{ICR}$	Common-mode input voltage range	Recommended range	25°C	-15		13.5	V
			Full range		-14.9	13	
$V_{OM}$	Maximum peak output voltage swing	$R_L = 2\text{ k}\Omega$	25°C	$\pm 13$	$\pm 14$		V
			Full range		$\pm 12$		
$A_{VD}$	Large-signal differential voltage amplification	$V_O = \pm 10\text{ V}$ , $R_L = 600\ \Omega$	25°C	0.8	2.5		V/ $\mu\text{V}$
		$V_O = \pm 10\text{ V}$ , $R_L = 2\text{ k}\Omega$	25°C	1.5	8		
		Full range		0.5			
CMRR	Common-mode rejection ratio	$V_{IC} = -15\text{ V to }13.5\text{ V}$	25°C	100	117		dB
		$V_{IC} = -14.9\text{ V to }13\text{ V}$	Full range		97		
$k_{SVR}$	Supply-voltage rejection ratio ( $\Delta V_{CC}/\Delta V_{IO}$ )	$V_{CC+} = \pm 2\text{ V to } \pm 18\text{ V}$	25°C	103	120		dB
			Full range		100		
	Channel separation	$V_O = \pm 10\text{ V}$ , $R_L = 2\text{ k}\Omega$	25°C	123	140		dB
$r_{id}$	Differential input resistance		25°C	100	400		M $\Omega$
$r_{ic}$	Common-mode input resistance		25°C		5		G $\Omega$
$I_{CC}$	Supply current per amplifier		25°C		0.35	0.5	mA
			Full range			0.6	

 (1) Full range is  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ .

 (2) All typical values are at  $T_A = 25^\circ\text{C}$ .

(3) On products compliant to MIL-PRF-38535, Class B, this parameter is not production tested.

## 6.14 Electrical Characteristics: LT1013AM, 5 V

 at specified free-air temperature,  $V_{CC+} = 5\text{ V}$ ,  $V_{CC-} = 0$ ,  $V_O = 1.4\text{ V}$ ,  $V_{IC} = 0$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	$T_A^{(1)}$	MIN	TYP <sup>(2)</sup>	MAX	UNIT	
$V_{IO}$	Input offset voltage	$R_S = 50\ \Omega$	25°C		60	250	$\mu\text{V}$	
			Full range		250	900		
		$R_S = 50\ \Omega$ , $V_{IC} = 0.1\text{ V}$	125°C		120	450		
$I_{IO}$	Input offset current		25°C		0.2	1.3	nA	
			Full range			6		
$I_{IB}$	Input bias current		25°C		-15	-35	nA	
			Full range			-80		
$V_{ICR}$	Common-mode input voltage range	Recommended range	25°C	0		3.5	V	
			Full range		0	3		
$V_{OM}$	Maximum peak output voltage swing	Output low, No load	25°C		15	25	V	
			Output low, $R_L = 600\ \Omega$ to GND	25°C		5		10
			Full range					15
			Output low, $I_{\text{sink}} = 1\text{ mA}$	25°C		220		350
			Output high, No load	25°C	4	4.4		
			Output high, $R_L = 600\ \Omega$ to GND	25°C	3.4	4		
$A_{VD}$	Large-signal differential voltage amplification	$V_O = 5\text{ mV}$ to $4\text{ V}$ , $R_L = 500\ \Omega$	25°C		1		$\text{V}/\mu\text{V}$	
			Full range					
$I_{CC}$	Supply current per amplifier		25°C		0.31	0.45	mA	
			Full range			0.55		

 (1) Full range is  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ .

 (2) All typical values are at  $T_A = 25^\circ\text{C}$ .

## 6.15 Electrical Characteristics: LT1013DM, $\pm 15\text{ V}$

 at specified free-air temperature,  $V_{CC\pm} = \pm 15\text{ V}$ ,  $V_{IC} = 0$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	$T_A^{(1)}$	MIN	TYP <sup>(2)</sup>	MAX	UNIT
$V_{IO}$	Input offset voltage	$R_S = 50\ \Omega$	25°C		200	800	$\mu\text{V}$
			Full range			1000	
$\alpha_{VIO}$	Temperature coefficient of input offset voltage		Full range		0.5	2.5 <sup>(3)</sup>	$\mu\text{V}/^\circ\text{C}$
			Long-term drift of input offset voltage	25°C		0.5	
$I_{IO}$	Input offset current		25°C		0.2	1.5	nA
			Full range			5	
$I_{IB}$	Input bias current		25°C		-15	-30	nA
			Full range			-45	
$V_{ICR}$	Common-mode input voltage range	Recommended range	25°C	-15		13.5	V
			Full range		-14.9	13	
$V_{OM}$	Maximum peak output voltage swing	$R_L = 2\text{ k}\Omega$	25°C	$\pm 12.5$	$\pm 14$		V
			Full range		$\pm 11.5$		
$A_{VD}$	Large-signal differential voltage amplification	$V_O = \pm 10\text{ V}$ , $R_L = 600\ \Omega$	25°C	0.5	2	$\text{V}/\mu\text{V}$	
		$V_O = \pm 10\text{ V}$ , $R_L = 2\text{ k}\Omega$	25°C	1.2	7		
		Full range		0.25			
CMRR	Common-mode rejection ratio	$V_{IC} = -15\text{ V}$ to $13.5\text{ V}$	25°C	97	114	dB	
		$V_{IC} = -14.9\text{ V}$ to $13\text{ V}$	Full range		94		
$k_{SVR}$	Supply-voltage rejection ratio ( $\Delta V_{CC}/\Delta V_{IO}$ )	$V_{CC+} = \pm 2\text{ V}$ to $\pm 18\text{ V}$	25°C	100	117	dB	
			Full range		97		
	Channel separation	$V_O = \pm 10\text{ V}$ , $R_L = 2\text{ k}\Omega$	25°C	120	137	dB	
$r_{id}$	Differential input resistance		25°C	70	300	$\text{M}\Omega$	
$r_{ic}$	Common-mode input resistance		25°C		4	$\text{G}\Omega$	
$I_{CC}$	Supply current per amplifier		25°C		0.35	0.55	mA
			Full range			0.7	

 (1) Full range is  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ .

 (2) All typical values are at  $T_A = 25^\circ\text{C}$ .

(3) On products compliant to MIL-PRF-38535, Class B, this parameter is not production tested.

## 6.16 Electrical Characteristics: LT1013DM, 5 V

at specified free-air temperature,  $V_{CC+} = 5\text{ V}$ ,  $V_{CC-} = 0$ ,  $V_O = 1.4\text{ V}$ ,  $V_{IC} = 0$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	$T_A^{(1)}$	MIN	TYP <sup>(2)</sup>	MAX	UNIT
$V_{IO}$	Input offset voltage	$R_S = 50\ \Omega$	25°C		250	950	$\mu\text{V}$
			Full range		800	2000	
		$R_S = 50\ \Omega$ , $V_{IC} = 0.1\text{ V}$	125°C		560	1200	
$I_{IO}$	Input offset current		25°C		0.3	2	nA
			Full range			10	
$I_{IB}$	Input bias current		25°C		-18	-50	nA
			Full range			-120	
$V_{ICR}$	Common-mode input voltage range	Recommended range	25°C	0		3.5	V
			Full range		0		
$V_{OM}$	Maximum peak output voltage swing	Output low, No load	25°C		15	25	V
		Output low, $R_L = 600\ \Omega$ to GND	25°C		5	10	
			Full range				
		Output low, $I_{\text{sink}} = 1\text{ mA}$	25°C		220	350	
		Output high, No load	25°C	4	4.4		
		Output high, $R_L = 600\ \Omega$ to GND	25°C	3.4	4		
Full range			3.1				
$A_{VD}$	Large-signal differential voltage amplification	$V_O = 5\text{ mV}$ to $4\text{ V}$ , $R_L = 500\ \Omega$	25°C		1		$\text{V}/\mu\text{V}$
$I_{CC}$	Supply current per amplifier		25°C		0.32	0.5	mA
			Full range				

(1) Full range is  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ .

(2) All typical values are at  $T_A = 25^\circ\text{C}$ .

## 6.17 Operating Characteristics

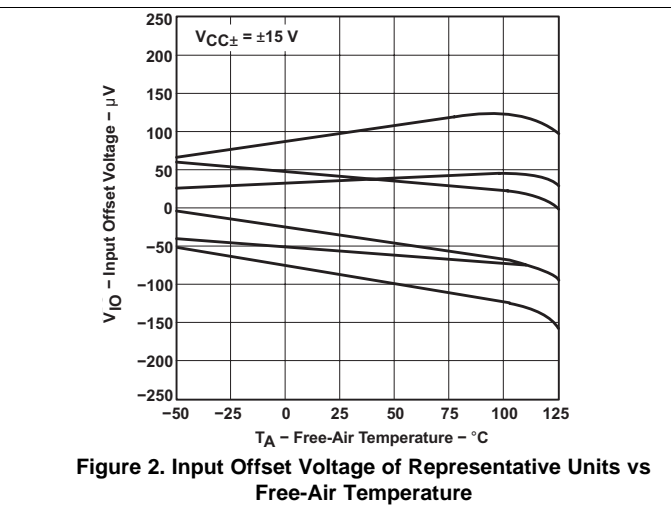
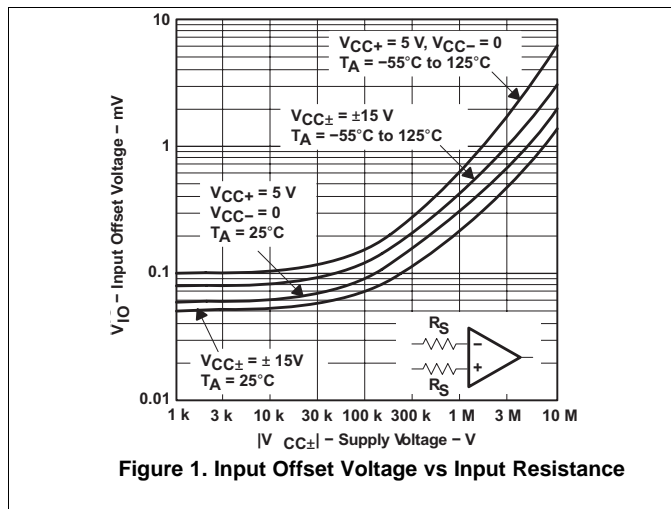
 $V_{CC\pm} = \pm 15\text{ V}$ ,  $V_{IC} = 0$ ,  $T_A = 25^\circ\text{C}$ 

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Slew rate		0.2	0.4		$\text{V}/\mu\text{s}$
$V_n$	Equivalent input noise voltage	$f = 10\text{ Hz}$		24		$\text{nV}/\sqrt{\text{Hz}}$
		$f = 1\text{ kHz}$		22		
$V_{N(\text{PP})}$	Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz}$ to $10\text{ Hz}$		0.55		$\mu\text{V}$
$I_n$	Equivalent input noise current	$f = 10\text{ Hz}$		0.07		$\text{pA}/\sqrt{\text{Hz}}$

## 6.18 Typical Characteristics

Table 1. Table of Graphs

			FIGURE
$V_{IO}$	Input offset voltage	vs Input Resistance	Figure 1
		vs Temperature	Figure 2
$\Delta V_{IO}$	Change in input offset voltage	vs Time	Figure 3
$I_{IO}$	Input offset current	vs Temperature	Figure 4
$I_{IB}$	Input bias current	vs Temperature	Figure 5
$V_{IC}$	Common-mode input voltage	vs Input bias current	Figure 6
$A_{VD}$	Differential voltage amplification	vs Load resistance	Figure 7, Figure 8
		vs Frequency	Figure 9, Figure 10
	Channel separation	vs Frequency	Figure 11
	Output saturation voltage	vs Temperature	Figure 12
CMRR	Common-mode rejection ratio	vs Frequency	Figure 13
$k_{SVR}$	Supply-voltage rejection ratio	vs Frequency	Figure 14
$I_{CC}$	Supply current	vs Temperature	Figure 15
$I_{OS}$	Short-circuit output current	vs Time	Figure 16
$V_n$	Equivalent input noise voltage	vs Frequency	Figure 17
$I_n$	Equivalent input noise current	vs Frequency	Figure 17
$V_{N(PP)}$	Peak-to-peak input noise voltage	vs Time	Figure 18
	Pulse response	Small signal	Figure 19, Figure 21
		Large signal	Figure 20, Figure 22, Figure 23
	Phase shift	vs Frequency	Figure 9



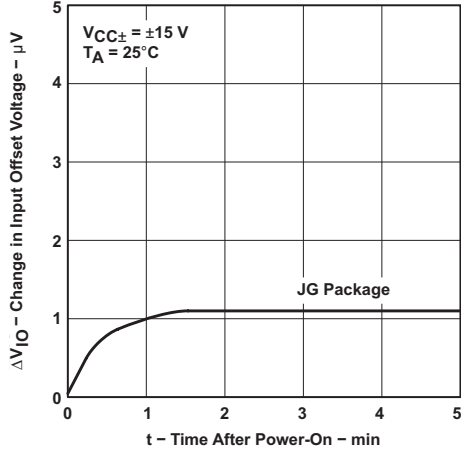


Figure 3. Warm-Up Change in Input Offset Voltage vs Time After Power On

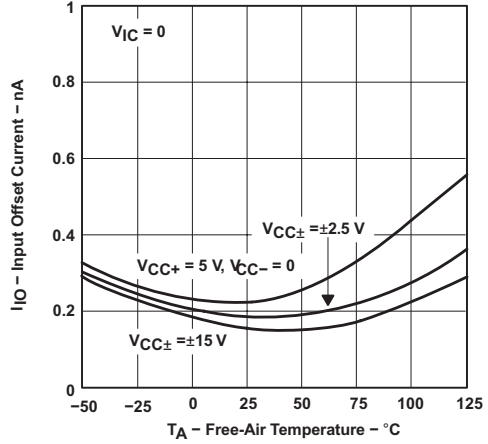


Figure 4. Input Offset Current vs Free-Air Temperature

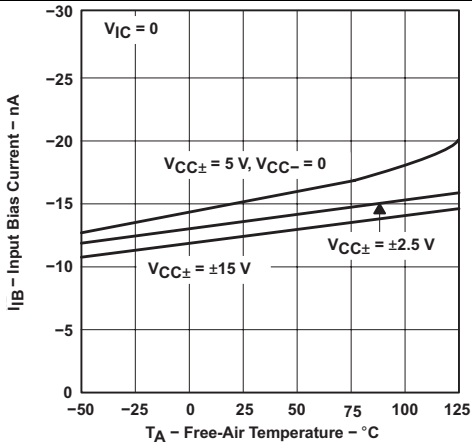


Figure 5. Input Bias Current vs Free-Air Temperature

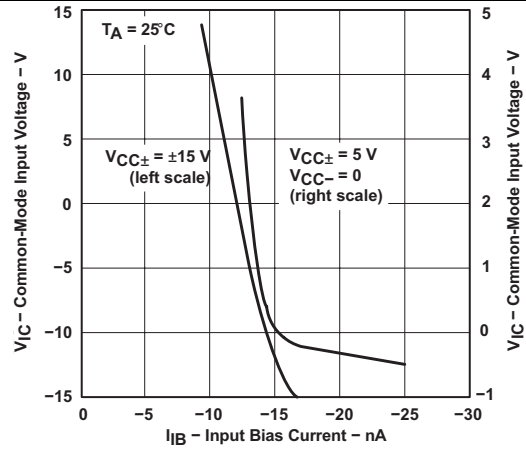


Figure 6. Common-Mode Input Voltage vs Input Bias Current

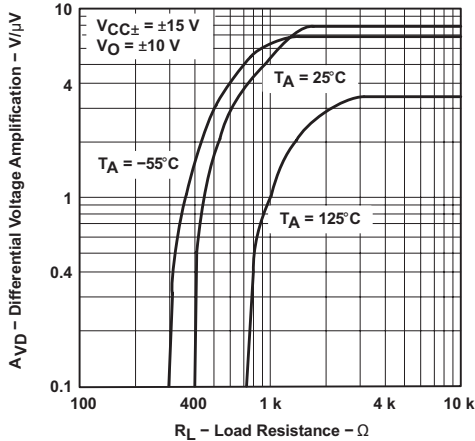


Figure 7. Differential Voltage Amplification vs Load Resistance

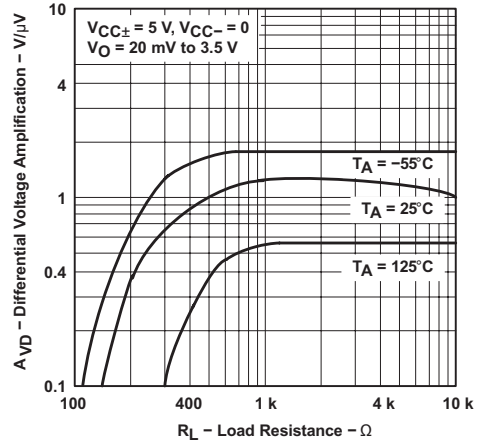


Figure 8. Differential Voltage Amplification vs Load Resistance

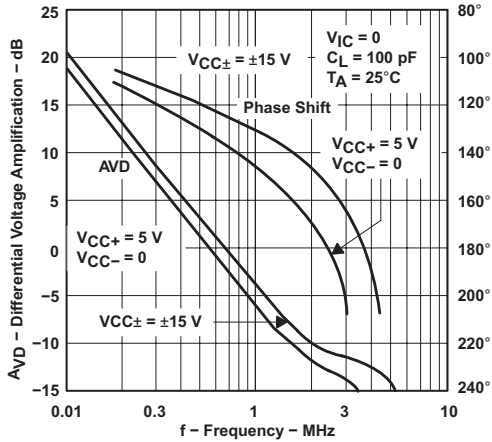


Figure 9. Differential Voltage Amplification and Phase Shift vs Frequency

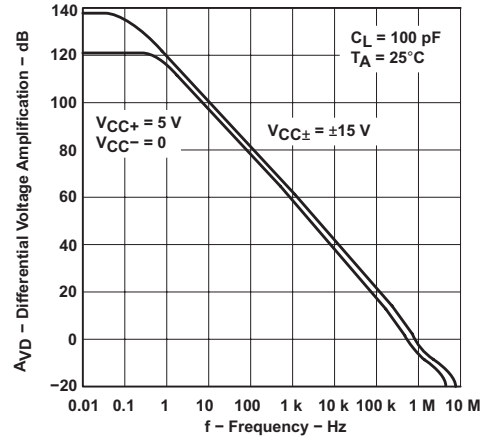


Figure 10. Differential Voltage Amplification vs Frequency

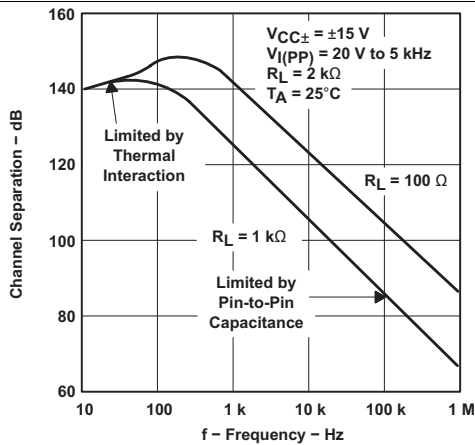


Figure 11. Channel Separation vs Frequency

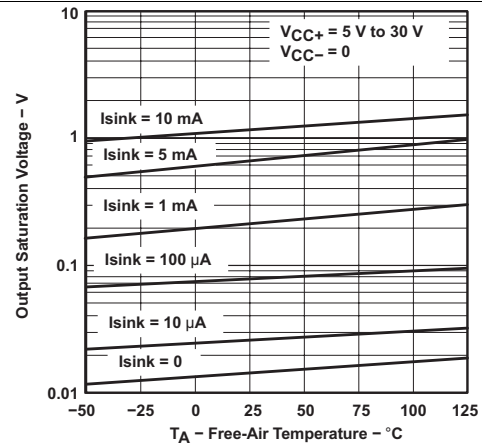


Figure 12. Output Saturation Voltage vs Free-Air Temperature

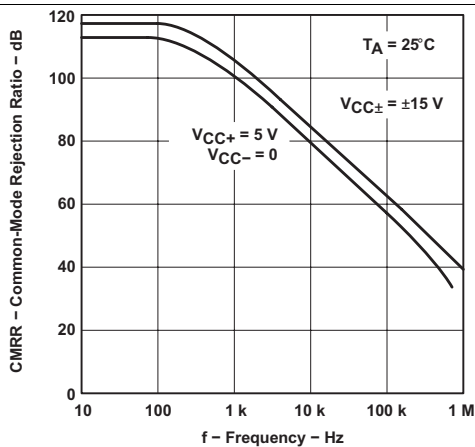


Figure 13. Common-Mode Rejection Ratio vs Frequency

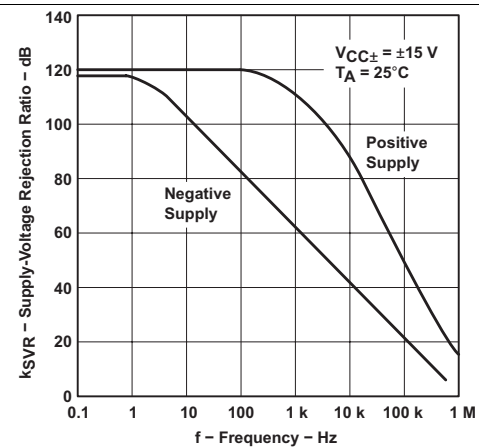


Figure 14. Supply-Voltage Rejection Ratio vs Frequency

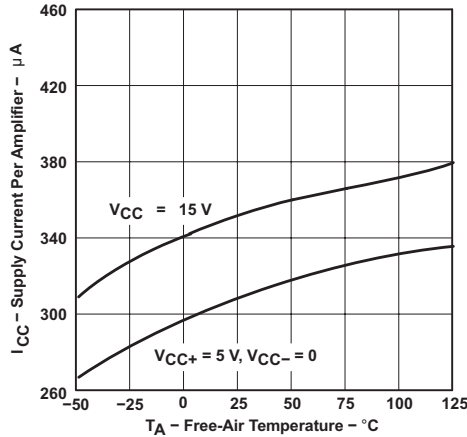


Figure 15. Supply Current vs Free-Air Temperature

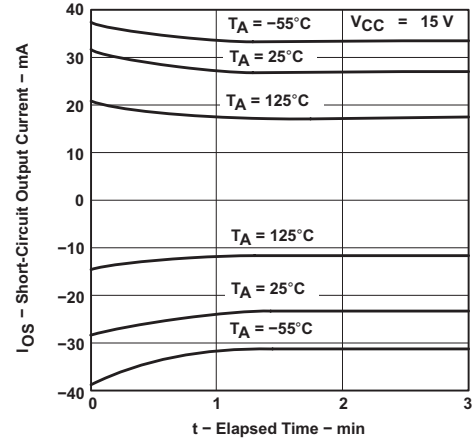


Figure 16. Short-Circuit Output Current vs Elapsed Time

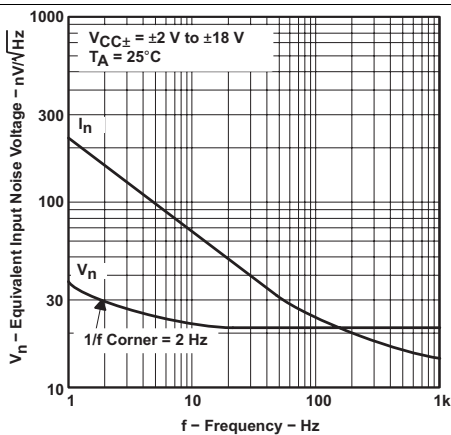


Figure 17. Equivalent Input Noise Voltage and Equivalent Input Noise Current vs Frequency

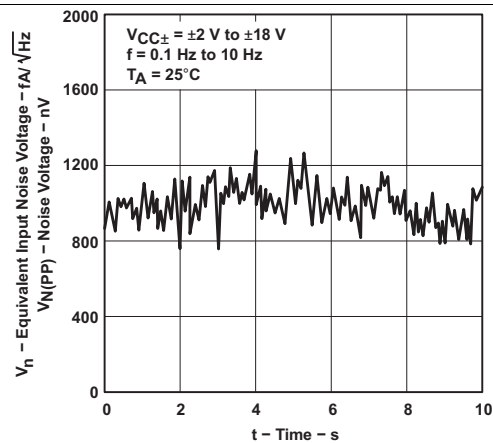


Figure 18. Peak-to-Peak Input Noise Voltage Over a 10-Second Period

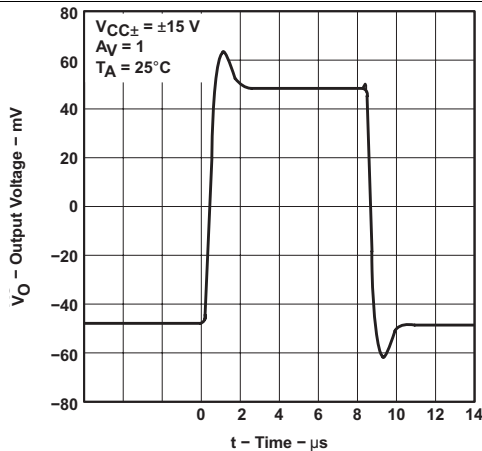


Figure 19. Voltage-Follower Small-Signal Pulse Response

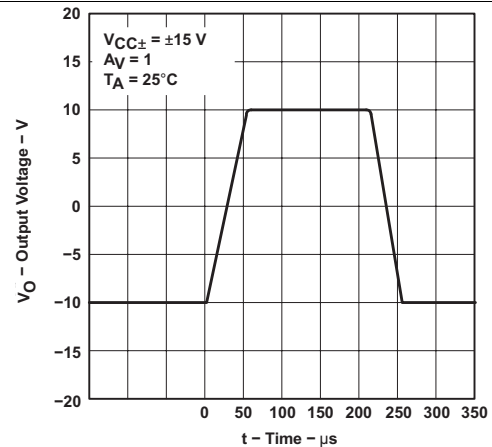
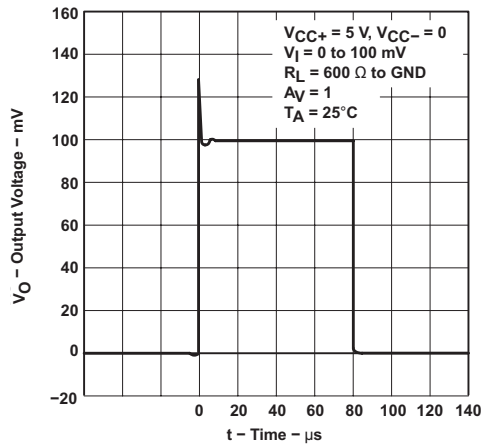
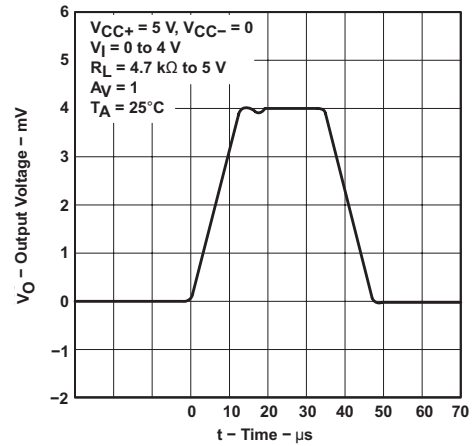
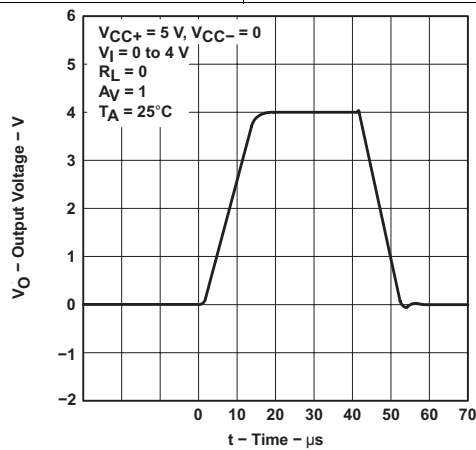


Figure 20. Voltage-Follower Large-Signal Pulse Response

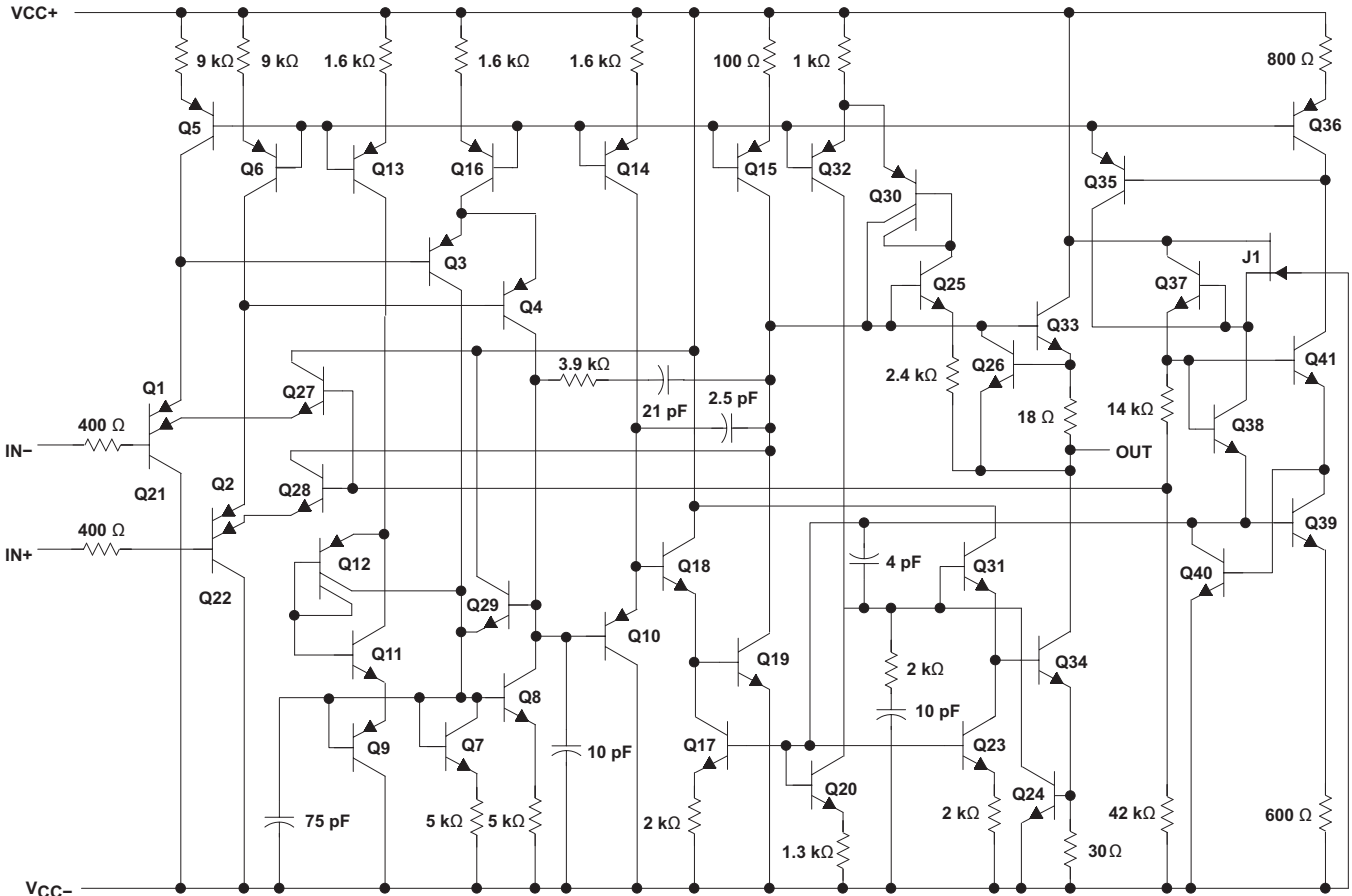

**Figure 21. Voltage-Follower Small-Signal Pulse Response**

**Figure 22. Voltage-Follower Large-Signal Pulse Response**

**Figure 23. Voltage-Follower Large-Signal Pulse Response**

## 7 Detailed Description

### 7.1 Overview

The LT1013x device is a dual operational amplifier with low natural  $V_{IO}$  without programming memory that can be erased. There are no side effects from active  $V_{IO}$  correction used by other op amps. The LT1013x has built-in protection for input voltage below  $V_{CC-}$ . However, an external resistance must be added to protect the LT1013x from input voltage greater than  $V_{CC+}$ .

### 7.2 Functional Block Diagram



Component values are nominal.

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### 7.3 Feature Description

#### 7.3.1 Input Resistors

For voltages less than  $V_{CC-}$ , a pair of 400-Ω resistors limit input current. These resistors have parasitic diodes to  $V_{CC+}$ . Therefore, external series resistance is needed if input voltage exceed  $V_{CC+}$ .

#### 7.3.2 Output Stage

High output is provided by Q33 emitter for low output impedance. Q26 provides active current limiting for sourcing current.

Low output is provided by Q34 collector for lower output voltage near  $V_{CC-}$  rail. Q24 provides active current limiting for sinking current.

## Feature Description (continued)

### 7.3.3 Low-Supply Operation

The minimum supply voltage for proper operation of the LT1013x is 3.4 V (three NiCad batteries). Typical supply current at this voltage is 290  $\mu$ A; therefore, power dissipation is only 1 mW per amplifier.

### 7.3.4 Output Phase Reversal Protection

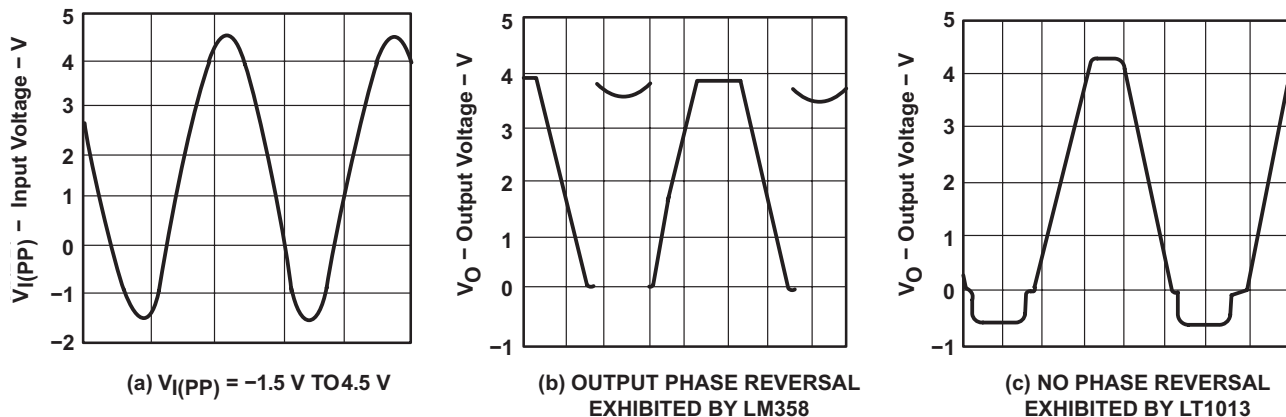
The LT1013x is fully specified for single-supply operation ( $V_{CC-} = 0$ ). The common-mode input voltage range includes ground, and the output swings to within a few millivolts of ground.

Furthermore, the LT1013x has specific circuitry that addresses the difficulties of single-supply operation, both at the input and at the output. At the input, the driving signal can fall below 0 V, either inadvertently or on a transient basis. If the input is more than a few hundred millivolts below ground, the LT1013x is designed to deal with the following two problems that can occur:

1. On many other operational amplifiers, when the input is more than a diode drop below ground, unlimited current flows from the substrate ( $V_{CC-}$  terminal) to the input, which can destroy the unit. On the LT1013x, the 400- $\Omega$  resistors in series with the input protect the device, even when the input is 5 V below ground.
2. When the input is more than 400 mV below ground (at  $T_A = 25^\circ\text{C}$ ), the input stage of similar operational amplifiers saturates, and phase reversal occurs at the output. This can cause lockup in servo systems. Because of unique phase-reversal protection circuitry (Q21, Q22, Q27, and Q28), the LT1013x outputs do not reverse, even when the inputs are at  $-1.5$  V (see [Figure 24](#)).

This phase-reversal protection circuitry does not function when the other operational amplifier on the LT1013x is driven hard into negative saturation at the output. Phase-reversal protection does not work on amplifier 1 when amplifier 2 output is in negative saturation nor on amplifier 2 when amplifier 1 output is in negative saturation.

At the output, other single-supply designs either cannot swing to within 600 mV of ground or cannot sink more than a few micro amperes while swinging to ground. The all-npn output stage of the LT1013x maintains its low output resistance and high-gain characteristics until the output is saturated. In dual-supply operations, the output stage is free of crossover distortion.

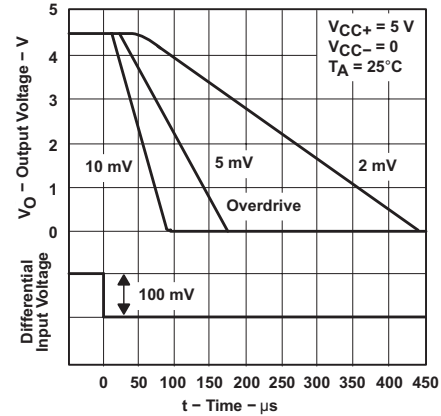
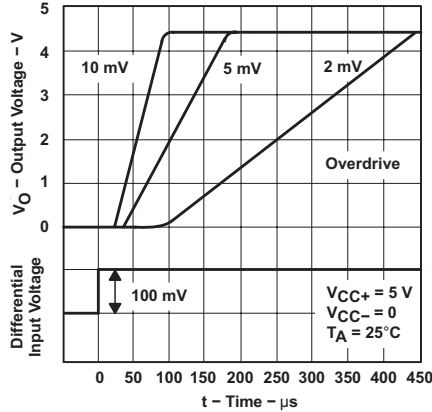


**Figure 24. Voltage-Follower Response With Input Exceeding the Negative Common-Mode Input Voltage Range**

**Feature Description (continued)**

**7.3.4.1 Comparator Applications**

The single-supply operation of the LT1013x is well suited for use as a precision comparator with TTL-compatible output. In systems using both operational amplifiers and comparators, the LT1013x can perform multiple duties (see [Figure 25](#) and [Figure 26](#)).



**Figure 25. Low-to-High-Level Output Response for Various Input Overdrives**

**Figure 26. High-to-Low-Level Output Response for Various Input Overdrives**

**7.4 Device Functional Modes**

The LT1013x dual operational amplifier amplifies a differential voltage applied to the inputs.

## 8 Application and Implementation

### NOTE

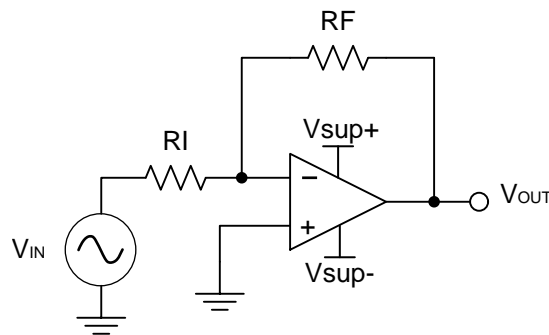
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

The LT1013x operational amplifiers are useful in a wide range of signal conditioning applications where high DC accuracy is needed.

### 8.2 Typical Application

A typical application for an operational amplifier is an inverting amplifier. This amplifier takes a positive voltage on the input and makes it a negative voltage of the same magnitude. In the same manner, it also makes negative voltages positive.



Copyright © 2016, Texas Instruments Incorporated

**Figure 27. Application Schematic**

#### 8.2.1 Design Requirements

The supply voltage must be chosen such that it is larger than the input voltage range and output range. For instance, this application scales a signal of  $\pm 0.5$  V to  $\pm 1.8$  V. Setting the supply at  $\pm 12$  V is sufficient to accommodate this application.

#### 8.2.2 Detailed Design Procedure

Determine the gain required by the inverting amplifier using [Equation 1](#) and [Equation 2](#):

$$A_v = \frac{V_{OUT}}{V_{IN}} \quad (1)$$

$$A_v = \frac{1.8}{-0.5} = -3.6 \quad (2)$$

Once the desired gain is determined, choose a value for  $R_I$  or  $R_F$ . Choosing a value in the  $k\Omega$  range is desirable because the amplifier circuit will use currents in the milliamp range. This ensures the part does not draw too much current. This example chooses  $10\text{ k}\Omega$  for  $R_I$ , which means  $36\text{ k}\Omega$  is used for  $R_F$ . This was determined by [Equation 3](#).

$$A_v = -\frac{R_F}{R_I} \quad (3)$$

## Typical Application (continued)

### 8.2.3 Application Curve

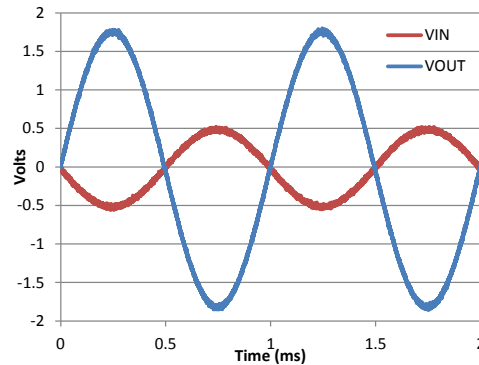


Figure 28. Input and Output Voltages of the Inverting Amplifier

## 9 Power Supply Recommendations

### CAUTION

Supply voltages larger than 44 V for a single supply, or outside the range of  $\pm 22$  V for a dual supply can permanently damage the device (see [Absolute Maximum Ratings](#)).

Place 0.1- $\mu$ F bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high impedance power supplies. For more detailed information on bypass capacitor placement, see [Layout](#).

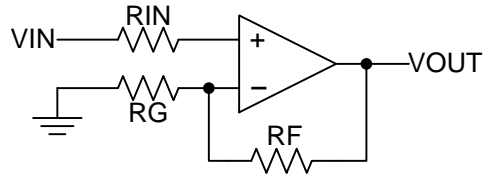
## 10 Layout

### 10.1 Layout Guidelines

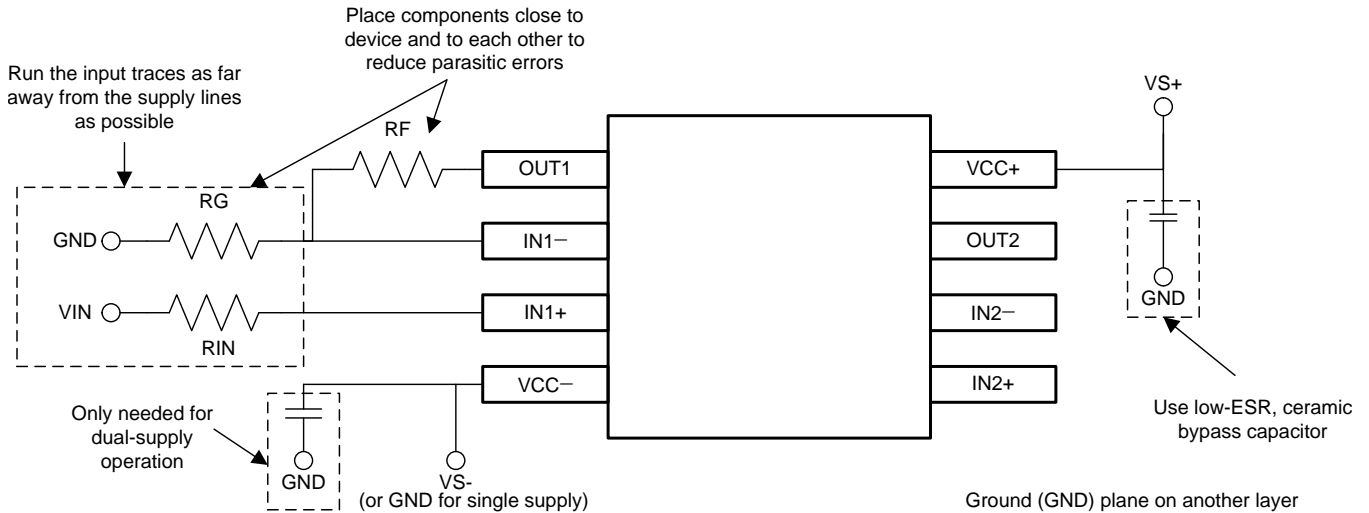
For best operational performance of the device, use quality PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1- $\mu$ F ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- Run the input traces as far away from the supply or output traces as possible to reduce parasitic coupling. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance, as shown in [Layout Guidelines](#).
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

## 10.2 Layout Examples



**Figure 29. Operational Amplifier Schematic for Noninverting Configuration**



**Figure 30. Operational Amplifier Board Layout for Noninverting Configuration**

## 11 Device and Documentation Support

### 11.1 Device Support

#### 11.1.1 Developmental Support

For developmental support, see the following:

[LT1013-DIE](#)

### 11.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 2. Related Links**

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LT1013	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
LT1013D	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
LT1013M	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
LT1013AM	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
LT1013-DIE	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 11.5 Trademarks

E2E is a trademark of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 11.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 11.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">5962-88760012A</a>	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 88760012A LT1013AMFKB
<a href="#">5962-8876001PA</a>	Active	Production	CDIP (JG)   8	50   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8876001PA LT1013AM
<a href="#">5962-88760022A</a>	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 88760022A LT1013MFKB
<a href="#">5962-8876002PA</a>	Active	Production	CDIP (JG)   8	50   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8876002PA LT1013M
<a href="#">LT1013AMFKB</a>	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 88760012A LT1013AMFKB
LT1013AMFKB.A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 88760012A LT1013AMFKB
<a href="#">LT1013AMJG</a>	Active	Production	CDIP (JG)   8	50   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	LT1013AMJG
LT1013AMJG.A	Active	Production	CDIP (JG)   8	50   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	LT1013AMJG
<a href="#">LT1013AMJGB</a>	Active	Production	CDIP (JG)   8	50   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8876001PA LT1013AM
LT1013AMJGB.A	Active	Production	CDIP (JG)   8	50   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8876001PA LT1013AM
<a href="#">LT1013CD</a>	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	1013C
LT1013CD.A	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	1013C
<a href="#">LT1013CDR</a>	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	1013C
LT1013CDR.A	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	1013C
<a href="#">LT1013CP</a>	Active	Production	PDIP (P)   8	50   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	LT1013CP
LT1013CP.A	Active	Production	PDIP (P)   8	50   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	LT1013CP
<a href="#">LT1013DD</a>	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	1013D
LT1013DD.A	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	1013D
<a href="#">LT1013DDR</a>	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	1013D
LT1013DDR.A	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	1013D

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">LT1013DID</a>	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	1013DI
LT1013DID.A	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	1013DI
<a href="#">LT1013DIDR</a>	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	1013DI
LT1013DIDR.A	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	1013DI
<a href="#">LT1013DIP</a>	Active	Production	PDIP (P)   8	50   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 105	(1013DI, LT1013DIP )
LT1013DIP.A	Active	Production	PDIP (P)   8	50   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 105	(1013DI, LT1013DIP )
<a href="#">LT1013DMD</a>	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	1013DM
LT1013DMD.A	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	1013DM
<a href="#">LT1013DMDG4</a>	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	1013DM
LT1013DMDG4.A	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	1013DM
<a href="#">LT1013DP</a>	Active	Production	PDIP (P)   8	50   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	LT1013DP
LT1013DP.A	Active	Production	PDIP (P)   8	50   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	LT1013DP
<a href="#">LT1013MFKB</a>	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 88760022A LT1013MFKB
LT1013MFKB.A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 88760022A LT1013MFKB
<a href="#">LT1013MJG</a>	Active	Production	CDIP (JG)   8	50   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	LT1013MJG
LT1013MJG.A	Active	Production	CDIP (JG)   8	50   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	LT1013MJG
<a href="#">LT1013MJGB</a>	Active	Production	CDIP (JG)   8	50   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8876002PA LT1013M
LT1013MJGB.A	Active	Production	CDIP (JG)   8	50   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8876002PA LT1013M

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF LT1013, LT1013M :**

- Catalog : [LT1013](#)
- Military : [LT1013M](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

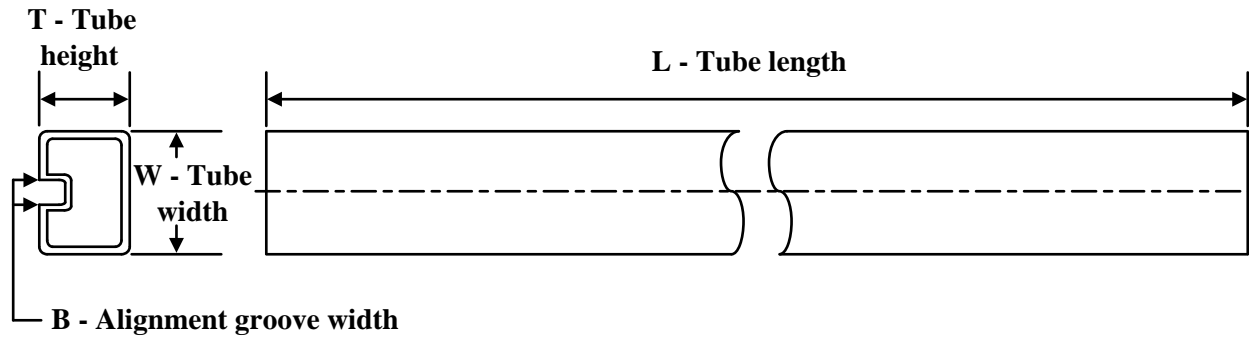

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LT1013CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LT1013DDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LT1013DIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LT1013DIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LT1013CDR	SOIC	D	8	2500	353.0	353.0	32.0
LT1013DDR	SOIC	D	8	2500	353.0	353.0	32.0
LT1013DIDR	SOIC	D	8	2500	353.0	353.0	32.0
LT1013DIDR	SOIC	D	8	2500	340.5	336.1	25.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-88760012A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-88760022A	FK	LCCC	20	55	506.98	12.06	2030	NA
LT1013AMFKB	FK	LCCC	20	55	506.98	12.06	2030	NA
LT1013AMFKB.A	FK	LCCC	20	55	506.98	12.06	2030	NA
LT1013CD	D	SOIC	8	75	507	8	3940	4.32
LT1013CD.A	D	SOIC	8	75	507	8	3940	4.32
LT1013CP	P	PDIP	8	50	506	13.97	11230	4.32
LT1013CP.A	P	PDIP	8	50	506	13.97	11230	4.32
LT1013DD	D	SOIC	8	75	507	8	3940	4.32
LT1013DD.A	D	SOIC	8	75	507	8	3940	4.32
LT1013DID	D	SOIC	8	75	507	8	3940	4.32
LT1013DID.A	D	SOIC	8	75	507	8	3940	4.32
LT1013DIP	P	PDIP	8	50	506	13.97	11230	4.32
LT1013DIP.A	P	PDIP	8	50	506	13.97	11230	4.32
LT1013DMD	D	SOIC	8	75	507	8	3940	4.32
LT1013DMD	D	SOIC	8	75	505.46	6.76	3810	4
LT1013DMD.A	D	SOIC	8	75	507	8	3940	4.32
LT1013DMD.A	D	SOIC	8	75	505.46	6.76	3810	4
LT1013DMDG4	D	SOIC	8	75	505.46	6.76	3810	4
LT1013DMDG4.A	D	SOIC	8	75	505.46	6.76	3810	4
LT1013DP	P	PDIP	8	50	506	13.97	11230	4.32
LT1013DP.A	P	PDIP	8	50	506	13.97	11230	4.32
LT1013MFKB	FK	LCCC	20	55	506.98	12.06	2030	NA
LT1013MFKB.A	FK	LCCC	20	55	506.98	12.06	2030	NA

## GENERIC PACKAGE VIEW

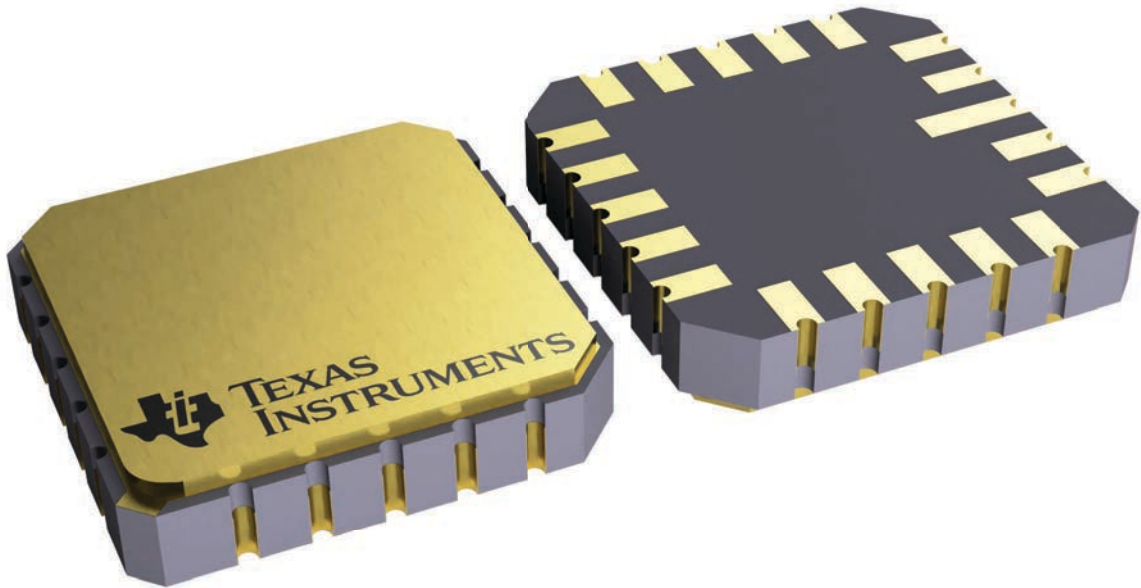
**FK 20**

**LCCC - 2.03 mm max height**

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4229370VA\



D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

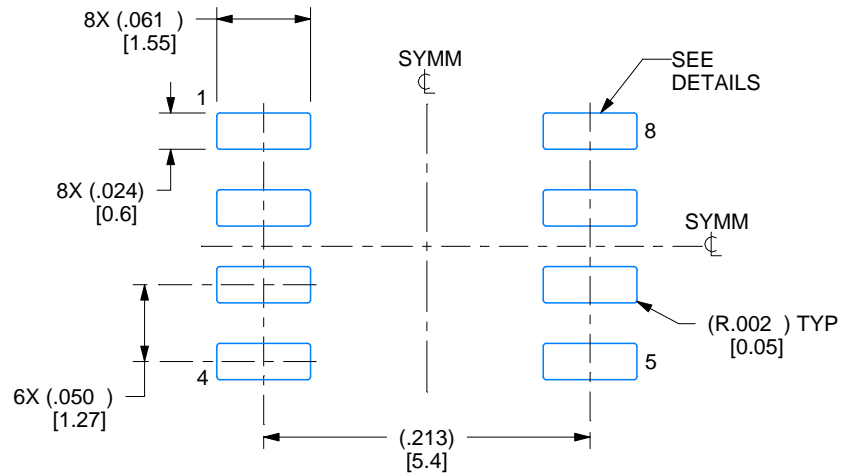
- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

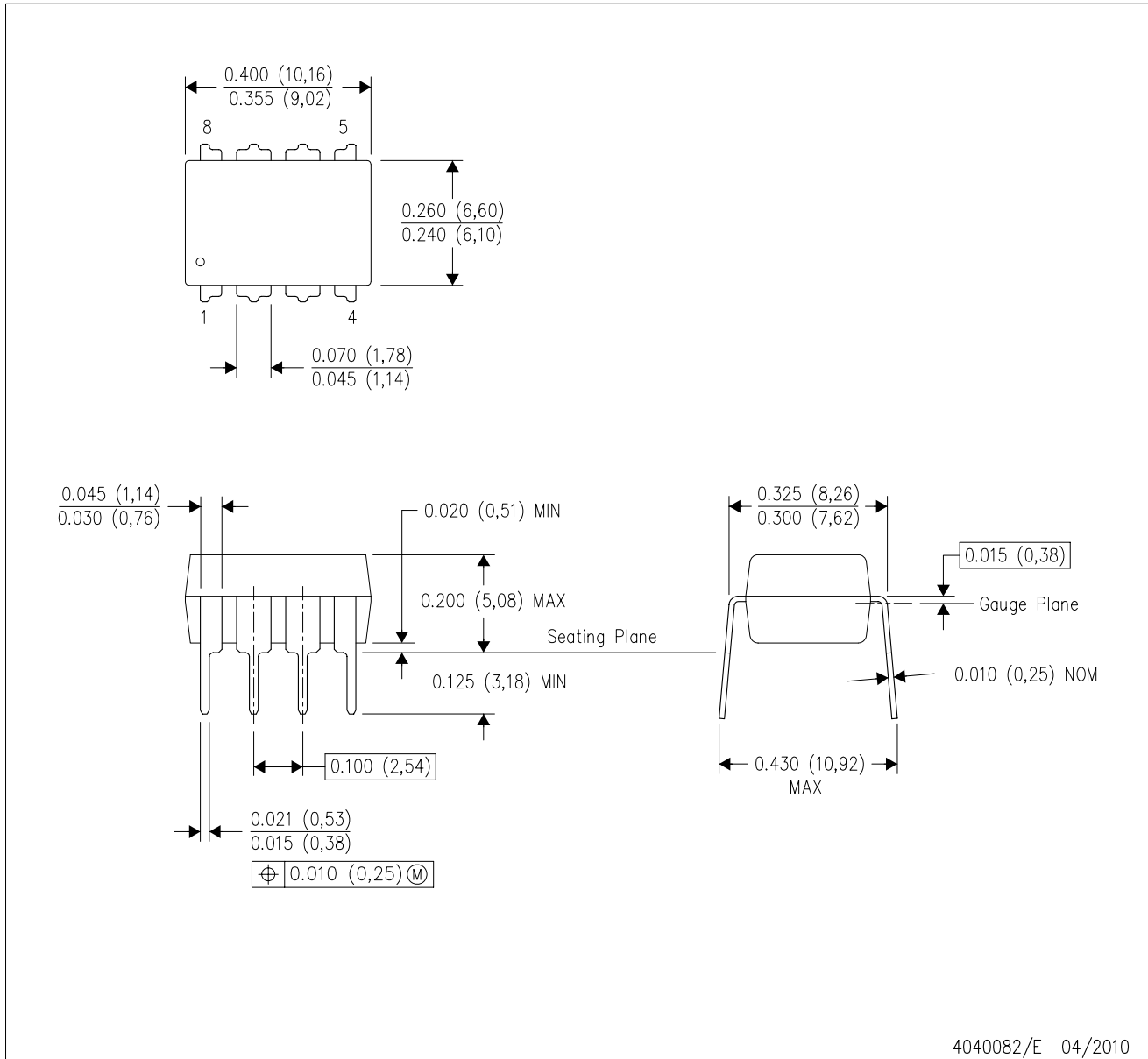
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



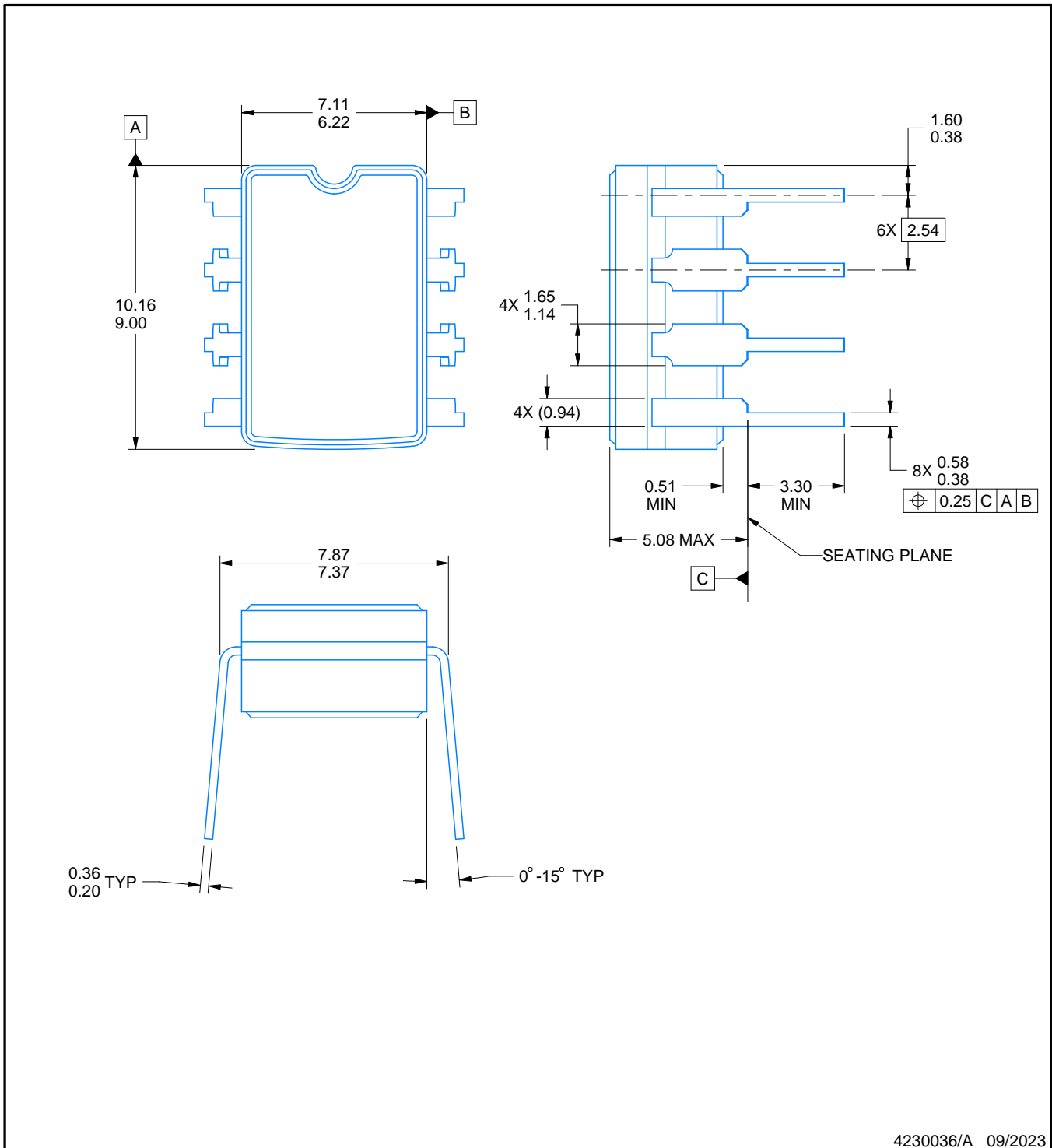
- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001 variation BA.

# PACKAGE OUTLINE

JG0008A

CDIP - 5.08 mm max height

CERAMIC DUAL IN-LINE PACKAGE



**NOTES:**

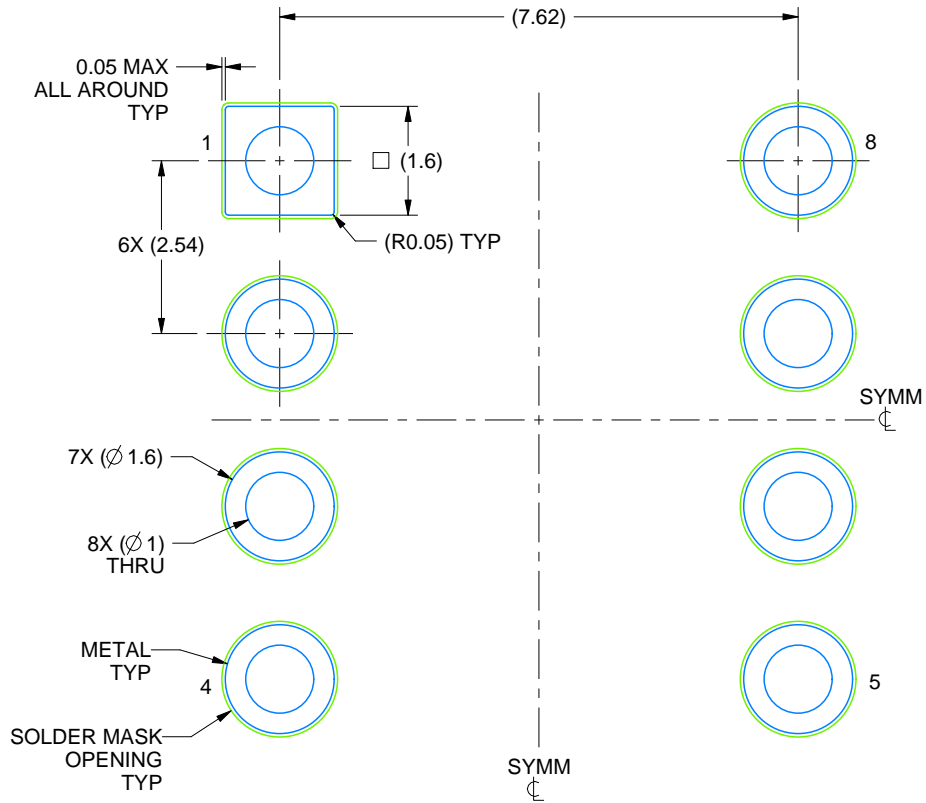
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package can be hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification.
5. Falls within MIL STD 1835 GDIP1-T8

# EXAMPLE BOARD LAYOUT

JG0008A

CDIP - 5.08 mm max height

CERAMIC DUAL IN-LINE PACKAGE



LAND PATTERN EXAMPLE  
NON SOLDER MASK DEFINED  
SCALE: 9X

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