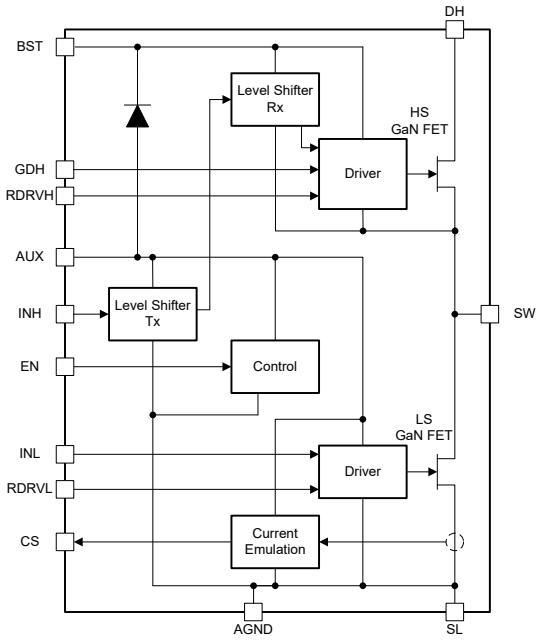
LMG2652H 650V 140mΩ GaN Half Bridge With Integrated Driver and Current Sense Emulation

1 Features

- GaN power-FET half bridge: 650V
- Low-side and high-side GaN FETs: 140mΩ
- Integrated gate drivers with low propagation delays: < 100ns
- Programmable turn-on slew rate control
- Current-sense emulation with high-bandwidth and high accuracy
- Low-side referenced (INH) and high-side referenced (GDH) high-side gate drive pins
- Low-side (INL) and high-side (INH) gate-drive interlock
- High-side (INH) gate-drive signal level shifter
- Smart-switched bootstrap diode function
- High-side start up: < 8µs
- Low-side and high-side cycle-by-cycle overcurrent protection
- Overtemperature protection
- AUX idle quiescent current: 250µA
- AUX standby quiescent current: 50µA
- BST idle quiescent current: 70µA
- 6mm × 8mm QFN package with dual thermal pads

2 Applications

- Mobile wall charger design
- USB wall power outlet
- AC/DC auxiliary power supplies
- Motor drives



Simplified Block Diagram

3 Description

The LMG2652H is a 650V 140mΩ GaN power-FET half bridge. The LMG2652H simplifies design, reduces component count, and reduces board space by integrating half-bridge power FETs, gate drivers, bootstrap FET, and high-side gate-drive level shifter in a 6mm × 8mm QFN package.

Programmable turn-on slew rates provide EMI and ringing control. The low-side current-sense emulation reduces power dissipation compared to the traditional current-sense resistor and allows the low-side thermal pad to connect to PCB power ground.

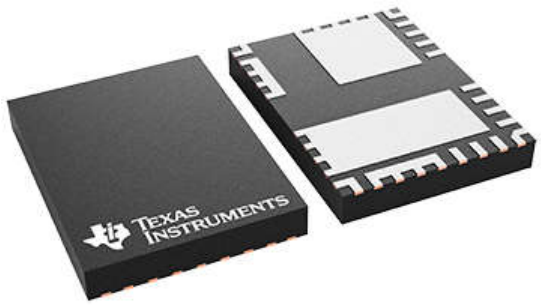
Control the high-side GaN power FET with either the low-side referenced gate-drive pin (INH) or the high-side referenced gate-drive pin (GDH). The high-side gate-drive signal level shifter reliably transmits the INH pin signal to the high-side gate driver in challenging power switching environments. The smart-switched GaN bootstrap FET has no diode forward-voltage drop, avoids overcharging the high-side supply, and has zero reverse-recovery charge.

The LMG2652H supports converter light-load efficiency requirements and burst-mode operation with low quiescent currents and fast start-up times. Protection features include FET turn-on interlock, under-voltage lockout (UVLO), cycle-by-cycle current limit, and over-temperature shut down. Ultra low slew rate setting supports motor drive applications.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
LMG2652H	RFB (VQFN, 19)	6.00mm × 8.00mm

(1) For more information, see Section 11.
(2) The package size (width × length) is a nominal value and includes pins, where applicable.



Package View

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4 Pin Configuration and Functions

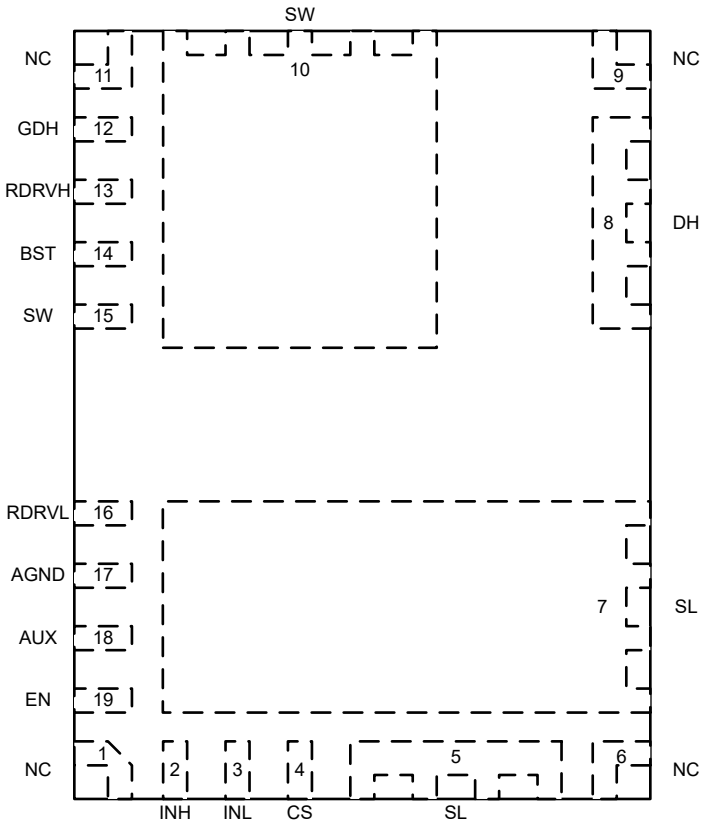


Figure 4-1. RFB Package, 19-Pin VQFN (Top View)

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
NC	1, 6, 9, 11	NC	Used to anchor QFN package to PCB. Pin must be soldered to a PCB landing pad. The PCB landing pad is non-solder mask defined pad and must not be physically connected to any other metal on the PCB.
INH	2	I	High-side gate-drive control input. Referenced to AGND. Signal is level shifted internally to the high-side GaN FET driver. There is a forward biased ESD diode from INH to AUX so avoid driving INH higher than AUX. Short this pin to AGND if GDH pin function is used.
INL	3	I	Low-side gate-drive control input. Referenced to AGND. There is a forward biased ESD diode from INL to AUX so avoid driving INL higher than AUX.
CS	4	O	Current-sense emulation output. Outputs scaled replica of the GaN FET current. Feed output current into a resistor to create a current sense voltage signal. Reference the resistor to the power supply controller IC local ground. This function replaces the external current sense resistor that is used in series with the low-side FET source.
SL	5, 7	P	Low-side GaN FET source. Low-side thermal pad. Internally connected to AGND.
DH	8	P	High-side GaN FET drain.
SW	10, 15	P	GaN FET half-bridge switch node between the high-side GaN FET source and low-side GaN FET drain. High-side thermal pad.
GDH	12	I	High-side gate-drive control input. Referenced to SW. Signal is connected directly to the high-side GaN FET driver. There is a forward biased ESD diode from GDH to BST so avoid driving GDH higher than BST. Short this pin to SW if INH pin function is used.
RDRVH	13	I	High-side drive strength control resistor. Set a resistance between RDRVH and SW to program the high-side GaN FET turn-on slew rate.

Table 4-1. Pin Functions (continued)

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
BST	14	P	Bootstrap voltage rail. High-side supply voltage. The bootstrap diode function between AUX and BST is internally provided. Connect an appropriately sized bootstrap capacitor between BST and SW.
RDRVL	16	I	Low-side drive strength control resistor. Set a resistance between RDRVL and AGND to program the low-side GaN FET turn-on slew rate.
AGND	17	G	Low-side analog ground. Internally connected to SL.
AUX	18	P	Auxiliary voltage rail. Low-side supply voltage. Connect a local bypass capacitor between AUX and AGND.
EN	19	I	Enable. Used to toggle between active and standby modes. The standby mode has reduced quiescent current to support converter light load efficiency targets. There is a forward biased ESD diode from EN to AUX so avoid driving EN higher than AUX.

(1) I = input, O = output, I/O = input or output, G = ground, P = power, NC = no connect

5 Specifications

5.1 Absolute Maximum Ratings

Unless otherwise noted: voltages are respect to AGND(1)

			MIN	MAX	UNIT
V_{DS}	Drain-source (DH to SW) or (SW to SL) voltage, FET off			650	V
$V_{DS(surge)}$	Drain-source (DH to SW) or (SW to SL) voltage, surge condition, FET off (2)			720	V
$V_{DS(tr)(surge)}$	Drain-source (DH to SW) or (SW to SL) transient ringing peak voltage, surge condition, FET off (2)			800	V
	Pin voltage to AGND	AUX	–0.3	30	V
		EN, INL, INH	–0.3	V_{AUX} + 0.3	V
		CS	–0.3	5.5	V
		RDRVL	–0.3	4	V
	Pin voltage to SW	BST	–0.3	30	V
		RDRVH	–0.3	4	V
		GDH	–0.3	V_{BST_SW} + 0.3	V
$I_{D(cnts)}$	Drain (DH to SW) & (SW to SL) continuous current, FET on		–7.5	Internally limited	A
$I_{D(pulse)(oc)}$	Drain (DH to SW) & (SW to SL) pulsed current during overcurrent response time(3)			18	A
$I_{S(cnts)}$	Source (SW to DH) & (SL to SW) continuous current, FET off			7.5	A
	Positive sink current	CS		10	mA
T_J	Operating junction temperature		–40	150	°C
T_{stg}	Storage temperature		–40	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) See Section 7.3.1 for more information on the GaN power FET switching capability.
(3) GaN power FET may self-limit below this value if it enters saturation.

5.2 ESD Ratings

Parameter				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	Pins 8 through 15	±1000	V
			Pins 1 through 7, Pins 16 through 19	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)		±500	V

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

Unless otherwise noted: voltages are respect to AGND

			MIN	NOM	MAX	UNIT
	Supply voltage	AUX	10		26	V
	Supply voltage to SW	BST	7.5		26	V
	Input voltage	EN, INL, INH	0		V_{AUX}	V
	Input voltage to SW	GDH	0		V_{BST_SW}	V

Unless otherwise noted: voltages are respect to AGND

			MIN	NOM	MAX	UNIT
V_{IH}	High-level input voltage	EN, INL, INH, GDH to SW	2.5			V
V_{IL}	Low-level input voltage				0.6	V
$I_{D(cnts)}$	Continuous current, FET on)		–6.1		6.1	A
C_{AUX}	AUX to AGND capacitance from external bypass capacitor		3 × C_{BST}			µF
C_{BST_SW}	BST to SW capacitance from external bypass capacitor		0.010			µF

5.4 Thermal Information

THERMAL METRIC(1)		LMG2652 RFB (VQFN) 19 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	22.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.20	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Electrical Characteristics

1) Symbol definitions: $V_{DS(ls)}$ = SW to SL voltage; $I_{DS(ls)}$ = SW to SL current; $V_{DS(hs)}$ = DH to SW voltage; $I_{D(hs)}$ = DH to SW current; I_{SW} = SW point current into device; 2) Unless otherwise noted: voltage, resistance, and capacitance are respect to AGND; –40°C ≤ T_J ≤ 125°C; $V_{DS(ls)}$ = 520V; $V_{DS(hs)}$ = 520V; 10V ≤ V_{AUX} ≤ 26V; 7.5V ≤ V_{BST_SW} ≤ 26V; V_{EN} = 5V; V_{INL} = 0V; V_{INH} = 0V; V_{GDH_SW} = 0V; R_{CS} = 100Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
GAN POWER FETS						
$R_{DS(on)}$	Drain-source (DH to SW) or (SW to SL) on resistance	V_{INL} or V_{INH} = 5V, I_D = 5.25A, T_J = 25°C		140		mΩ
		V_{INL} or V_{INH} = 5V, I_D = 5.25A, T_J = 125°C		255		
V_{SD}	Source-drain (SW to DH) or (SL to SW) third-quadrant voltage	SW to DH or SL to SW current = 0.525A		1.9		V
		SW to DH or SL to SW current = 5.25A		2.6		
I_{DSS}	Drain (DH to SW) or (SW to SL) leakage current	($V_{DS(ls)}$ = 0V, $V_{DS(hs)}$ = 650V) or ($V_{DS(hs)}$ = 0V, $V_{DS(ls)}$ = 650V), T_J = 25°C		2.3		μA
		($V_{DS(ls)}$ = 0V, $V_{DS(hs)}$ = 650V) or ($V_{DS(hs)}$ = 0V, $V_{DS(ls)}$ = 650V), T_J = 125°C		11.5		
Q_{OSS}	Output charge	($V_{DS(ls)}$ = 0V, $V_{DS(hs)}$ = 400V) or ($V_{DS(hs)}$ = 0V, $V_{DS(ls)}$ = 400V)		21.8		nC
C_{OSS}	Output capacitance			34.2		pF
E_{OSS}	Output capacitance stored energy			3.0		μJ
$C_{OSS,er}$	Energy related effective output capacitance			36.7		pF
$C_{OSS,tr}$	Time related effective output capacitance	($V_{DS(ls)}$ = 0V, $V_{DS(hs)}$ = 0V to 400V) or ($V_{DS(hs)}$ = 0V, $V_{DS(ls)}$ = 0V to 400V)		54.5		pF
Q_{RR}	Reverse recovery charge			0		nC
OVERCURRENT PROTECTION						
$I_{T(OC)}$	Overcurrent fault – threshold current		5.3	6.5	7.5	A
BOOTSTRAP RECTIFIER						
$R_{DS(on)}$	AUX to BST on resistance	V_{INL} = 5V, V_{AUX_BST} = 1V, T_J = 25°C		7		Ω
		V_{INL} = 5V, V_{AUX_BST} = 1V, T_J = 125°C		12		
	AUX to BST current limit	V_{INL} = 5V, V_{AUX_BST} = 7V	210	240	270	mA
	BST to AUX reverse current blocking threshold	V_{INL} = 5V		10.5		mA
CS						
	Current sense gain ($I_{CS(src)}$ / $I_{D(LS)}$)	V_{INL} = 5V, 0V ≤ V_{CS} ≤ 2V, 0A ≤ $I_{D(ls)}$< $I_{T(OC)(ls)}$		0.901		mA/A
	Current sense input offset current	V_{INL} = 5V, 0V ≤ V_{CS} ≤ 2V, 0A ≤ $I_{D(ls)}$< $I_{T(OC)(ls)}$	–56		56	mA
	Initial held output after overcurrent fault occurs while INL remains high	V_{INL} = 5V, 0V ≤ V_{CS} ≤ 2V			7	mA
	Final held output after overcurrent fault occurs while INL remains high	V_{INL} = 5V, 0V ≤ V_{CS} ≤ 2V	8.5	12	15.5	mA
	Output clamp voltage	V_{INL} = 5V, $I_{D(ls)}$ = 5.8A, CS sinking 5mA from external source		2.6		V
EN, INL, INH to AGND; GDH to SW						
V_{IT+}	Positive-going input threshold voltage		1.7		2.45	V
$V_{IT–}$	Negative-going input threshold voltage		0.7		1.3	V
	Input threshold voltage hysteresis			1		V
	Pull-down input resistance	0V ≤ V_{PIN} ≤ 3V	200	400	600	kΩ
	Pull-down input current	10V ≤ V_{PIN} ≤ 26V; V_{AUX} = 26V		10		μA
OVERTEMPERATURE PROTECTION						
	Temperature fault – postive-going threshold temperature		150	165		°C

5.5 Electrical Characteristics (continued)

1) Symbol definitions: $V_{DS(ls)}$ = SW to SL voltage; $I_{DS(ls)}$ = SW to SL current; $V_{DS(hs)}$ = DH to SW voltage; $I_{D(hs)}$ = DH to SW current; I_{SW} = SW point current into device; 2) Unless otherwise noted: voltage, resistance, and capacitance are respect to AGND; –40°C ≤ T_J ≤ 125°C; $V_{DS(ls)}$ = 520V; $V_{DS(hs)}$ = 520V; 10V ≤ V_{AUX} ≤ 26V; 7.5V ≤ V_{BST_SW} ≤ 26V; V_{EN} = 5V; V_{INL} = 0V; V_{INH} = 0V; V_{GDH_SW} = 0V; R_{CS} = 100Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Temperature fault – negative-going threshold temperature			150		°C
	Temperature fault – threshold temperature hysteresis			15		°C
AUX						
$V_{AUX,T+(UVLO)}$	UVLO – positive-going threshold voltage		8.9	9.3	9.7	V
	UVLO – negative-going threshold voltage		8.6	9.0	9.5	V
	UVLO – threshold voltage hysteresis			250		mV
	Standby quiescent current	V_{EN} = 0V		50	110	µA
	Quiescent current			250	400	µA
		V_{INL} = 5V, $I_{D(ls)}$ = 0A		1000		
	Operating current	V_{INL} = 0V or 5V, $V_{DS(ls)}$ = 0V, $I_{D(ls)}$ = 0A, f_{INL} = 500kHz		3.7		mA
BST						
$V_{BST\_SW,T+(UVLO)}$	V_{BST_SW} UVLO for FET to turn on – positive-going threshold voltage		6.7	7	7.4	V
	V_{BST_SW} UVLO for FET to stay on– negative-going threshold voltage		4.8	5.1	5.4	V
	Quiescent current			70	120	µA
		V_{INH} = 5V, $I_{D(hs)}$ = 0A		660		
		V_{GDH_SW} = 5V, $I_{D(hs)}$ = 0A		660		
	Operating current	V_{INH} = 0V or 5V, $V_{DS(hs)}$ = 0V, $I_{DS(hs)}$ = 0A; f_{INH} = 500kHz		2.2		mA
		V_{GDH_SW} = 0V or 5V, $V_{DS(hs)}$ = 0V, $I_{DS(hs)}$ = 0A; f_{GDH_SW} = 500kHz		2.2		

5.6 Switching Characteristics

1) Symbol definitions: $V_{DS(ls)}$ = SW to SL voltage; $I_{DS(ls)}$ = SW to SL current; $V_{DS(hs)}$ = DH to SW voltage; $I_{D(hs)}$ = DH to SW current; I_{SW} = SW point current into device; 2) Unless otherwise noted: voltage, resistance, and capacitance are respect to AGND; –40°C ≤ T_J ≤ 125°C; $V_{DS(ls)}$ = 520V; $V_{DS(hs)}$ = 520V; 10V ≤ V_{AUX} ≤ 26V; 7.5V ≤ V_{BST_SW} ≤ 26V; V_{EN} = 5V; V_{INL} = 0V; V_{INH} = 0V; R_{CS} = 100Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOW-SIDE GAN POWER FET						
$t_{d(on)(Idrain)(ls)}$	Drain current turn-on delay time	From V_{INL} > $V_{INL,IT+}$ to $I_{D(ls)}$ > 50mA, V_{BUS} = 400V, I_{SW} = 1.8A, at following low-side slew rate settings, see GaN Power FET Switching Parameters				
		slew rate setting 0 (slowest)		67	117	ns
		slew rate setting 1		45	71	
		slew rate setting 2		44	62	
		slew rate setting 3 (fastest)		35	51	
$t_{d(on)(ls)}$	Turn-on delay time	From V_{INL} > $V_{INL,IT+}$ to $V_{DS(ls)}$ < 390V, V_{BUS} = 400V, I_{SW} = 1.8A, at following low-side slew rate settings, see GaN Power FET Switching Parameters				
		slew rate setting 0 (slowest)		101	178	ns
		slew rate setting 1		59	98	
		slew rate setting 2		57	82	
		slew rate setting 3 (fastest)		41	60	
$t_{r(on)(ls)}$	Turn-on rise time	From $V_{DS(ls)}$ < 320V to $V_{DS(ls)}$ < 80V, V_{BUS} = 400V, I_{SW} = 1.8A, at following low-side slew rate settings, see GaN Power FET Switching Parameters				
		slew rate setting 0 (slowest)		111	136	ns
		slew rate setting 1		46	56	
		slew rate setting 2		11	15.5	
		slew rate setting 3 (fastest)		5	7	
$t_{d(off)(ls)}$	Turn-off delay time	From V_{INL} < $V_{INL,IT-}$ to $V_{DS(ls)}$ > 80V, V_{BUS} = 400V, I_{SW} = 1.8A, see GaN Power FET Switching Parameters		45	60	ns
$t_{f(off)(ls)}$	Turn-off fall time	From $V_{DS(ls)}$ > 80V to $V_{DS(ls)}$ > 320V, V_{BUS} = 400V, I_{SW} = 1.8A, see GaN Power FET Switching Parameters		20		ns
	Turn-on slew rate	From $V_{DS(ls)}$ < 320V to $V_{DS(ls)}$ < 80V, T_J = 25°C, V_{BUS} = 400V, I_{SW} = 1.8A, at following low-side slew rate settings, see GaN Power FET Switching Parameters				
		slew rate setting 0 (slowest)		2		V/ns
		slew rate setting 1		5		
		slew rate setting 2		23		
		slew rate setting 3 (fastest)		50		
HIGH-SIDE GAN POWER FET						

5.6 Switching Characteristics (continued)

1) Symbol definitions: $V_{DS(ls)}$ = SW to SL voltage; $I_{DS(ls)}$ = SW to SL current; $V_{DS(hs)}$ = DH to SW voltage; $I_{D(hs)}$ = DH to SW current; I_{SW} = SW point current into device; 2) Unless otherwise noted: voltage, resistance, and capacitance are respect to AGND; –40°C ≤ T_J ≤ 125°C; $V_{DS(ls)}$ = 520V; $V_{DS(hs)}$ = 520V; 10V ≤ V_{AUX} ≤ 26V; 7.5V ≤ V_{BST_SW} ≤ 26V; V_{EN} = 5V; V_{INL} = 0V; V_{INH} = 0V; R_{CS} = 100Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(on)}$ (Idrain) (hs,INH)	Drain current turn-on delay time	From V_{INH} > $V_{INH,IT+}$ to $I_{D(hs)}$ > 50mA, V_{BUS} = 400V, I_{SW} = –1.8A, at following high-side slew rate settings, see GaN Power FET Switching Parameters				
		slew rate setting 0 (slowest)		73	112	ns
		slew rate setting 1		45	67	
		slew rate setting 2		45	64	
		slew rate setting 3 (fastest)		34	48	
$t_{d(on)}$ (Idrain) (hs,GDH)	Drain current turn-on delay time	From V_{GDH} > $V_{GDH,IT+}$ to $I_{D(hs)}$ > 50mA, V_{BUS} = 400V, I_{SW} = –1.8A, at following high-side slew rate settings, see GaN Power FET Switching Parameters				
		slew rate setting 0 (slowest)		64	107	ns
		slew rate setting 1		42	66	
		slew rate setting 2		41	61	
		slew rate setting 3 (fastest)		32	50	
$t_{d(on)}$ (hs,INH)	Turn-on delay time	From V_{INH} > $V_{INH,IT+}$ to $V_{DS(hs)}$ < 390V, V_{BUS} = 400V, I_{SW} = –1.8A, at following high-side slew rate settings, see GaN Power FET Switching Parameters				
		slew rate setting 0 (slowest)		97	172	ns
		slew rate setting 1		55	94	
		slew rate setting 2		54	78	
		slew rate setting 3 (fastest)		38	57	
$t_{d(on)}$ (hs,GDH)	Turn-on delay time	From V_{GDH} > $V_{GDH,IT+}$ to $V_{DS(hs)}$ < 390V, V_{BUS} = 400V, I_{SW} = –1.8A, at following high-side slew rate settings, see GaN Power FET Switching Parameters				
		slew rate setting 0 (slowest)		125	191	ns
		slew rate setting 1		66	93	
		slew rate setting 2		62	79	
		slew rate setting 3 (fastest)		43	60	
$t_{r(on)(hs)}$	Turn-on rise time	From $V_{DS(hs)}$ < 320V to $V_{DS(hs)}$ < 80V, V_{BUS} = 400V, I_{SW} = –1.8A, at following high-side slew rate settings, see GaN Power FET Switching Parameters				
		slew rate setting 0 (slowest)		116	163	ns
		slew rate setting 1		46	62	
		slew rate setting 2		10	13	
		slew rate setting 3 (fastest)		4.5	6	
$t_{d(off)}$ (hs,INH)	Turn-off delay time	From V_{INH} < $V_{INH,IT-}$ to $V_{DS(hs)}$ > 80V, V_{BUS} = 400V, I_{SW} = –1.8A, see GaN Power FET Switching Parameters		40	55	ns
$t_{d(off)}$ (hs,GDH)	Turn-off delay time	From V_{GDH} < $V_{GDH,IT-}$ to $V_{DS(hs)}$ > 80V, V_{BUS} = 400V, I_{SW} = –1.8A, see GaN Power FET Switching Parameters		40	55	ns

5.6 Switching Characteristics (continued)

1) Symbol definitions: $V_{DS(ls)}$ = SW to SL voltage; $I_{DS(ls)}$ = SW to SL current; $V_{DS(hs)}$ = DH to SW voltage; $I_{D(hs)}$ = DH to SW current; I_{SW} = SW point current into device; 2) Unless otherwise noted: voltage, resistance, and capacitance are respect to AGND; –40°C ≤ T_J ≤ 125°C; $V_{DS(ls)}$ = 520V; $V_{DS(hs)}$ = 520V; 10V ≤ V_{AUX} ≤ 26V; 7.5V ≤ V_{BST_SW} ≤ 26V; V_{EN} = 5V; V_{INL} = 0V; V_{INH} = 0V; R_{CS} = 100Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{f(off)(hs)}$	Turn-off fall time	From $V_{DS(hs)}$ > 80V to $V_{DS(hs)}$ > 320V, V_{BUS} = 400V, I_{SW} = –1.8A, see GaN Power FET Switching Parameters		23		ns
	Turn-on slew rate	From $V_{DS(hs)}$ < 320V to $V_{DS(hs)}$ < 80V, T_J = 25°C, V_{BUS} = 400V, I_{SW} = –1.8A, at following high-side slew rate settings, see GaN Power FET Switching Parameters				
		slew rate setting 0 (slowest)		2		V/ns
		slew rate setting 1		5		
		slew rate setting 2		23		
		slew rate setting 3 (fastest)		50		
LOW-SIDE OVERCURRENT PROTECTION						
$t_{(OC)(ls)}$	Overcurrent fault response time, FET on before overcurrent	From $I_{D(ls)}$ > $I_{T(OC)(ls)}$ to $I_{D(ls)}$ < 0.5 × $I_{T(OC)(ls)}$, $I_{D(ls)}$ di/dt = 90A/µs		70	85	ns
$t_{(OC)(en)(ls)}$	Overcurrent fault response time, FET enabled into a short	$V_{DS(ls)}$ = 100V; From $I_{D(ls)}$ > $I_{T(OC)(ls)}$ to $I_{D(ls)}$ < 0.5 × $I_{T(OC)(ls)}$, at following slew rate setting				
		slew rate setting 0 (slowest)		265	330	ns
		slew rate setting 1		165	200	ns
		slew rate setting 2		160	200	ns
		slew rate setting 3 (fastest)		120	140	ns
HIGH-SIDE OVERCURRENT PROTECTION						
$t_{(OC)(hs)}$	Overcurrent fault response time, FET on before overcurrent	From $I_{D(hs)}$ > $I_{T(OC)(hs)}$ to $I_{D(hs)}$ < 0.5 × $I_{T(OC)(hs)}$, $I_{D(hs)}$ di/dt = 90 A/µs		60	70	ns
$t_{(OC)(en)(hs)}$	Overcurrent fault response time, FET enabled into a short	$V_{DS(hs)}$ = 100 V; From $I_{D(hs)}$ > $I_{T(OC)(hs)}$ to $I_{D(hs)}$ < 0.5 × $I_{T(OC)(hs)}$, at following slew rate setting				
		slew rate setting 0 (slowest)		225	325	ns
		slew rate setting 1		140	175	ns
		slew rate setting 2		130	170	ns
		slew rate setting 3 (fastest)		95	125	ns
CS						
t_r	Rise time	From $I_{CS(src)}$ > 0.1 × $I_{CS(src)(final)}$ to $I_{CS(src)}$ > 0.9 × $I_{CS(src)(final)}$, 0V ≤ V_{CS} ≤ 2V, Low-side enabled into a 1.8A load			30	ns
EN						
	EN wake-up time	From V_{EN} > V_{IT+} to $I_{D(ls)}$ > 10mA, V_{INL} = 5V		1.5		µs
BST						
	Start-up time from deep BST to SW discharge	From V_{BST_SW} > $V_{BST\_SW,T+(UVLO)}$ to high-side reacts to INH or GDH high level with V_{BST_SW} rising from 0V to 10V in 1µs		5		µs
	Start-up time from shallow BST to SW discharge	From V_{BST_SW} > $V_{BST\_SW,T+(UVLO)}$ to high-side reacts to INH or GDH high level with V_{BST_SW} rising from 5V to 10V in 0.5µs		3.2		µs

5.7 Typical Characteristics

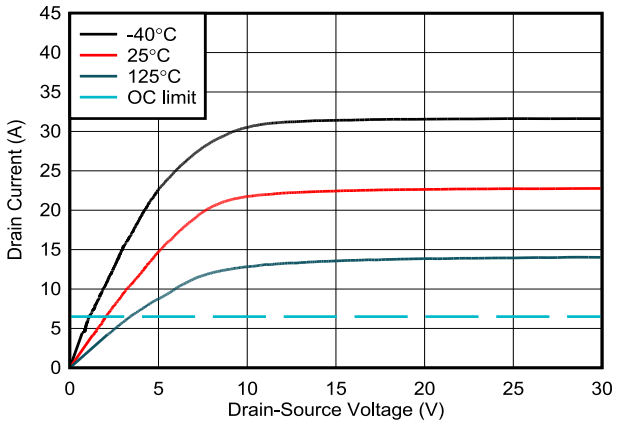


Figure 5-1. Drain Current vs Drain-Source Voltage

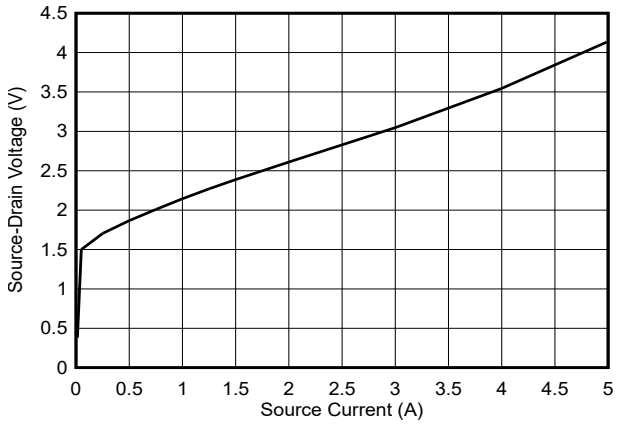


Figure 5-2. Off-State Source-Drain Voltage vs Source Current

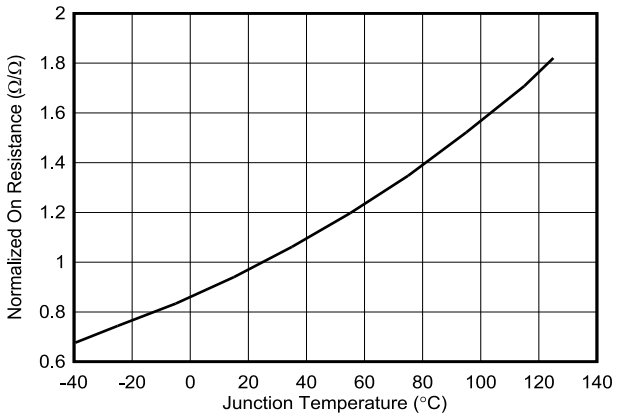


Figure 5-3. Normalized Drain-Source On-Resistance vs Junction Temperature

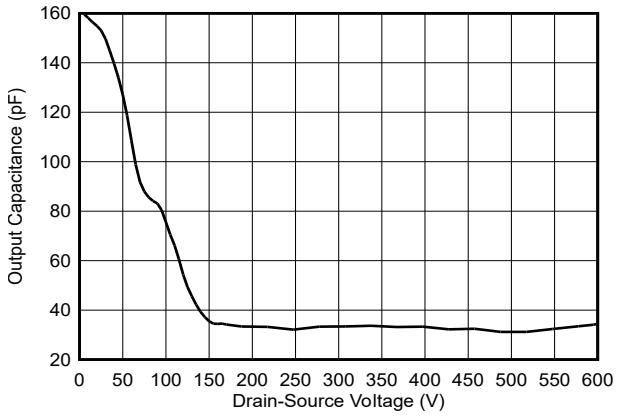


Figure 5-4. Output Capacitance vs Drain-Source Voltage

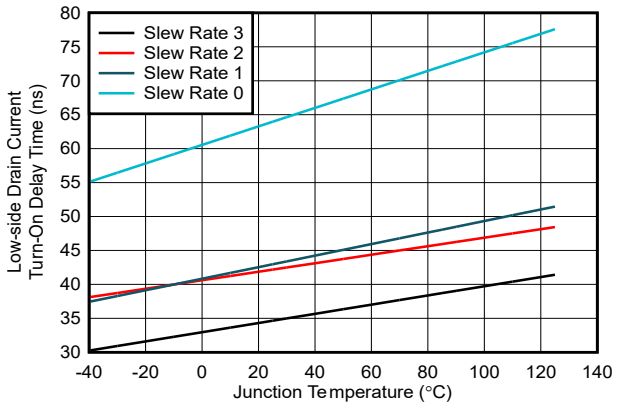


Figure 5-5. Low-Side Drain Current Turn-On Delay Time vs Junction Temperature

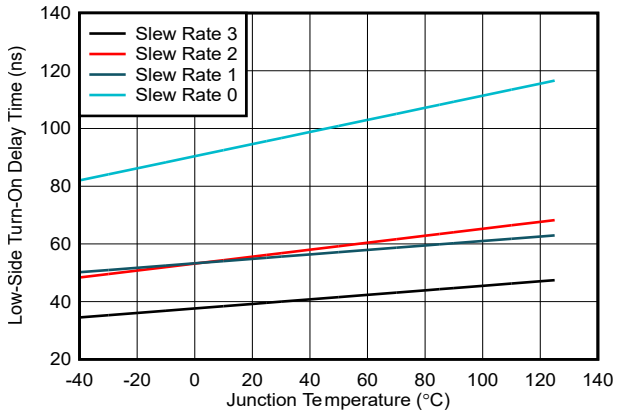


Figure 5-6. Low-Side Turn-On Delay Time vs Junction Temperature

5.7 Typical Characteristics (continued)

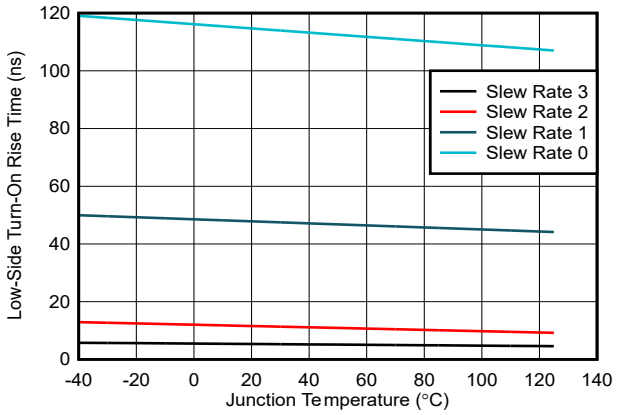


Figure 5-7. Low-Side Turn-On Rise Time vs Junction Temperature

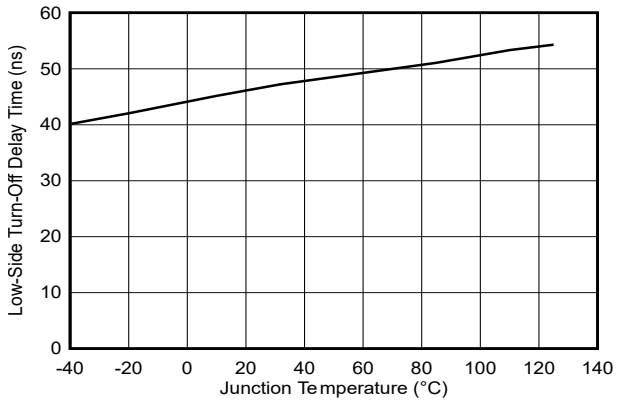


Figure 5-8. Low-Side Turn-Off Delay Time vs Junction Temperature

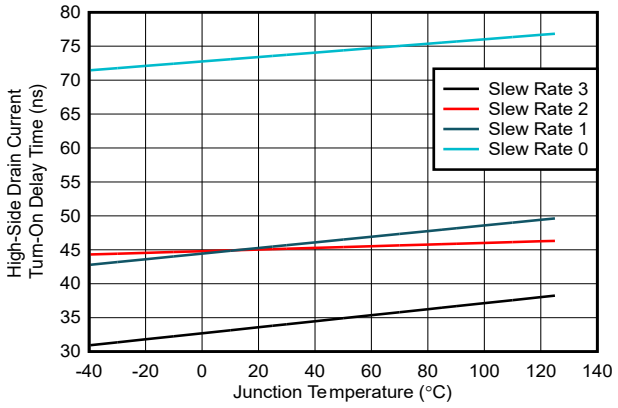


Figure 5-9. High-Side Drain Current Turn-On Delay Time vs Junction Temperature

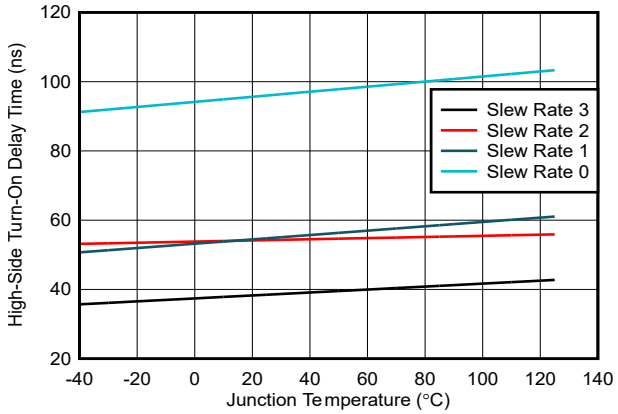


Figure 5-10. High-Side Turn-On Delay Time vs Junction Temperature

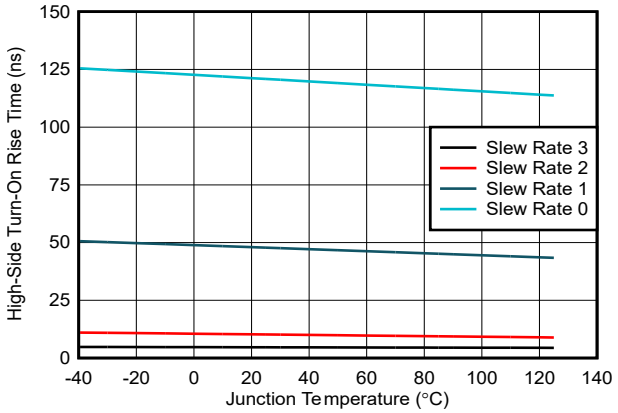


Figure 5-11. High-Side Turn-On Rise Time vs Junction Temperature

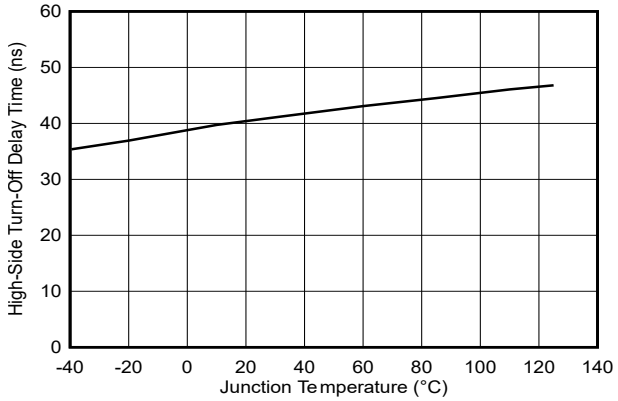


Figure 5-12. High-Side Turn-Off Delay Time vs Junction Temperature

5.7 Typical Characteristics (continued)

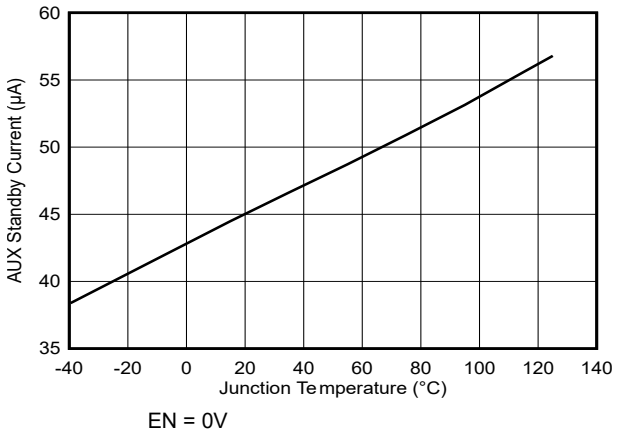


Figure 5-13. AUX Standby Current vs Junction Temperature

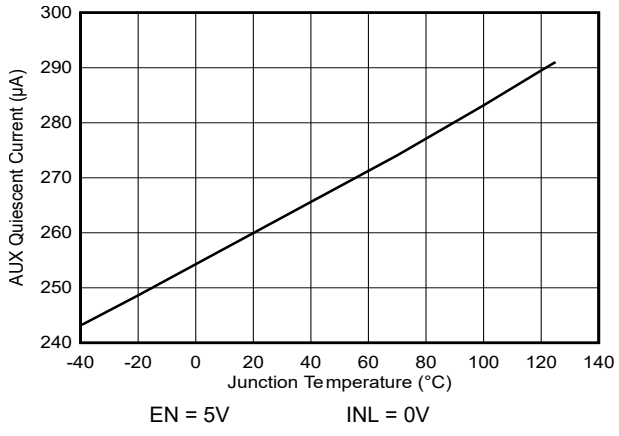


Figure 5-14. AUX Quiescent Current vs Junction Temperature

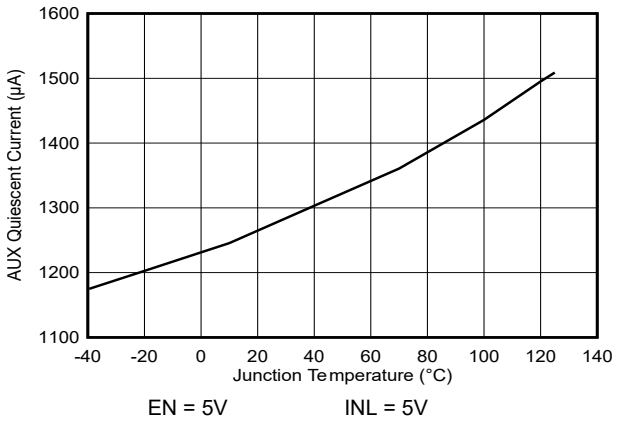


Figure 5-15. AUX Quiescent Current vs Junction Temperature

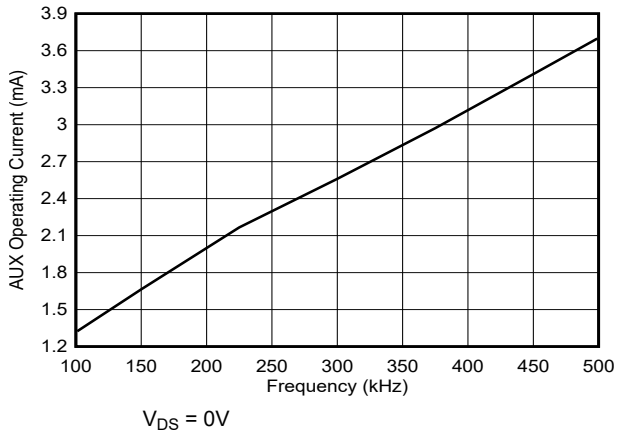


Figure 5-16. AUX Operating Current vs Frequency

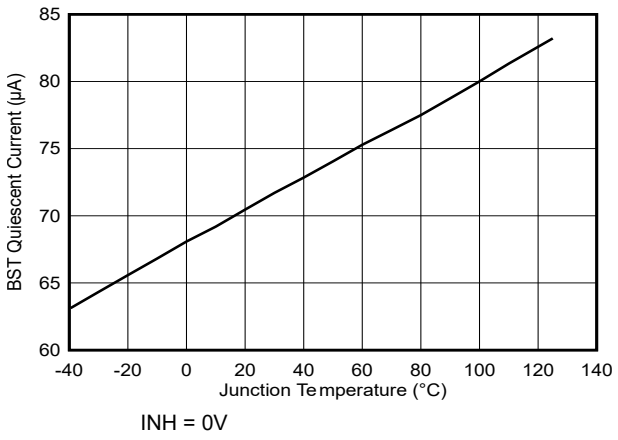


Figure 5-17. BST Quiescent Current vs Junction Temperature

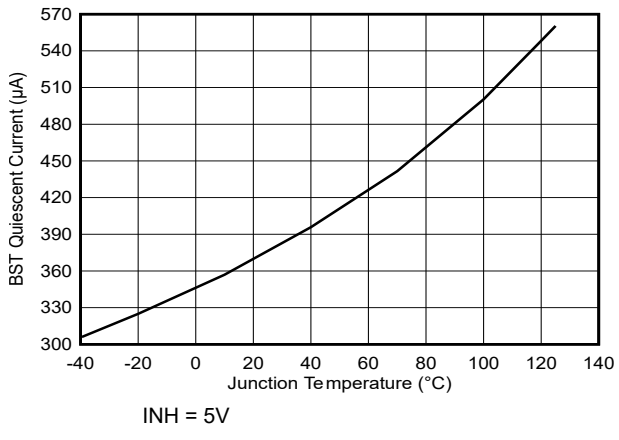


Figure 5-18. BST Quiescent Current vs Junction Temperature

5.7 Typical Characteristics (continued)

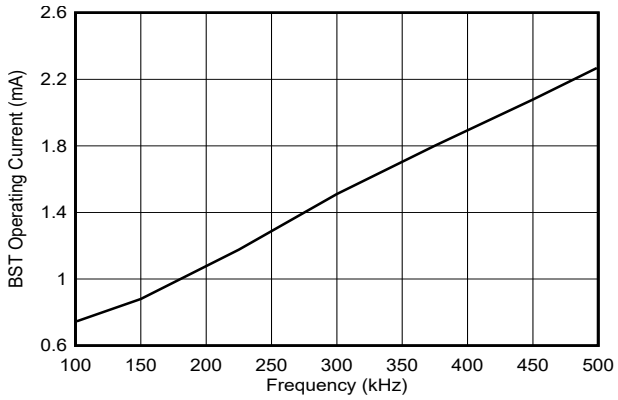


Figure 5-19. BST Operating Current vs Frequency

6 Parameter Measurement Information

6.1 GaN Power FET Switching Parameters

Figure 6-1 shows the circuit used in measuring the GaN power FET switching parameters. The circuit operates as a double-pulse tester. Consult external references for double-pulse tester details. The circuit is placed in the boost configuration to measure the low-side GaN switching parameters. The circuit is placed in the buck configuration to measure the high-side GaN switching parameters. The GaN FET not measured in each configuration (high-side in the boost and low-side in the buck) acts as the double-pulse tester diode and circulates the inductor current in the off-state, third-quadrant conduction mode. Table 6-1 shows the details for each configuration.

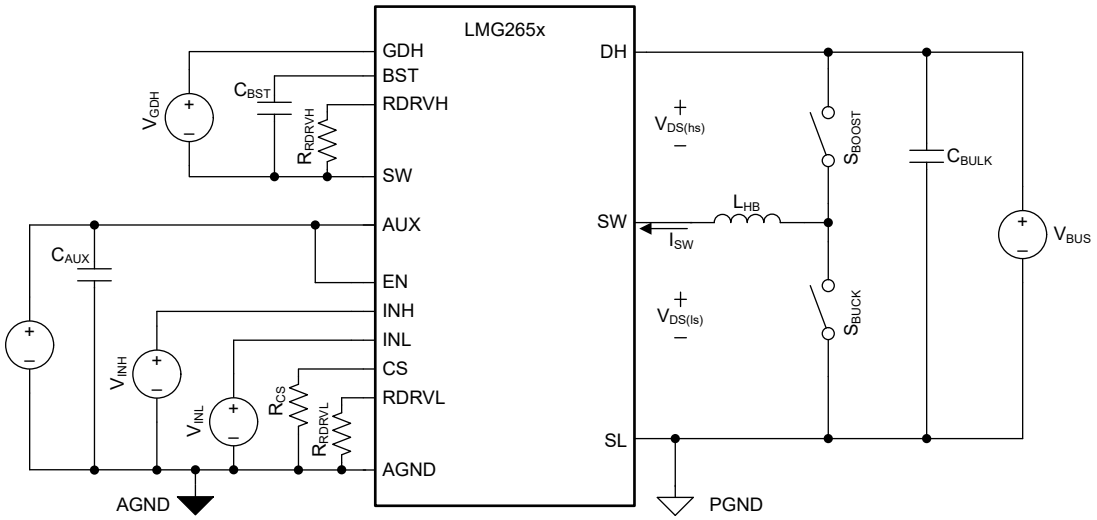


Figure 6-1. GaN Power FET Switching Parameters Test Circuit

Table 6-1. GaN Power FET Switching Parameters Test Circuit Configuration Details

CONFIGURATION	GaN FET UNDER TEST	GaN FET ACTING AS DIODE	S_{BOOST}	S_{BUCK}	V_{INL}	V_{INH}	V_{GDH}
Boost	Low-side	High-side	Closed	Open	Double-pulse waveform	0V	0V
Buck	High-side	Low-side	Open	Closed	0V	Double-pulse waveform	0V
Buck	High-side	Low-side	Open	Closed	0V	0V	Double-pulse waveform

Figure 6-2 shows the GaN power FET switching parameters.

The GaN power FET turn-on transition has three timing components: drain-current turn-on delay time $t_{d(on)(Idrain)}$, turn-on delay time $t_{d(on)}$, and turn-on rise time $t_{r(on)}$. Note that the turn-on rise time is the same as the V_{DS} 80% to 20% fall time. All three turn-on timing components are a function of the RDRVx pin setting.

The GaN power FET turn-off transition has two timing components: turn-off delay time $t_{d(off)}$, and turn-off fall time $t_{f(off)}$. Note that the turn-off fall time is the same as the V_{DS} 20% to 80% rise time. The turn-off timing components are independent of the RDRVx pin setting, but heavily dependent on the L_{HB} current.

The turn-on slew rate is measured over a turn-on rise time voltage delta (240V) to obtain a slew rate which is useful for EMI design. The RDRVx pin is used to program the slew rate.

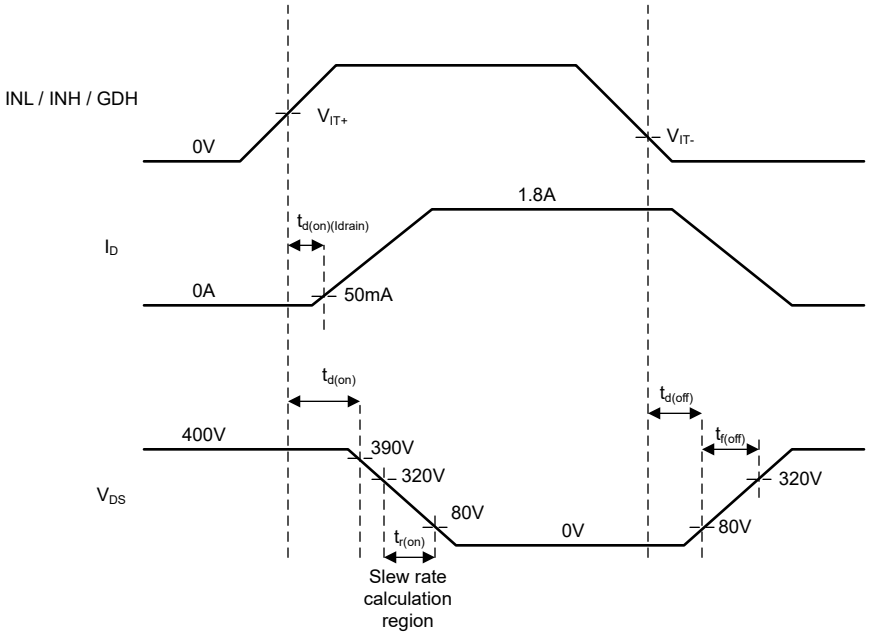


Figure 6-2. GaN Power FET Switching Parameters

7 Detailed Description

7.1 Overview

The LMG2652H is a highly-integrated 650V 140mΩ GaN power-FET half bridge intended for use in switch-mode power-supply applications. The LMG2652H combines the half-bridge power FETs, gate drivers, low-side current-sense emulation function, high-side gate-drive level shifter, and bootstrap diode function in a 6mm × 8mm QFN package.

The 650V rated GaN FETs support the high voltages encountered in off-line power switching applications. The GaN FETs low output-capacitive charge reduces both the time and energy needed for power converter switching and is the key characteristic needed to create small, efficient power converters.

The LMG2652H internal gate drivers regulate the GaN FET gate voltage for optimum on-resistance. Internal drivers also reduce total gate inductance and GaN FET common-source inductance for improved switching performance. The low-side / high-side GaN FET turn-on slew rates can be individually programmed to one of four discrete settings for design flexibility with respect to power loss, switching-induced ringing, and EMI.

Current-sense emulation places a scaled replica of the low-side drain current on the output of the CS pin. The CS pin terminates with a resistor to AGND to create the current-sense input signal to the external power supply controller. This CS pin resistor replaces the traditional current-sense resistor, placed in series with the low-side GaN FET source, at significant power and space savings. Furthermore, with no current-sense resistor in series with the GaN source, directly connect the low-side GaN FET thermal pad (SL pin) to the PCB power ground, improving system thermal performance.

The high-side GaN FET is controlled by both the low-side referenced INH pin and high-side referenced GDH pin, allowing the LMG2652H to interface with controllers that employ either high-side gate drive reference scheme. The internal high-side gate-drive level-shifter reliably transmits the INH signal to the high-side with minimal impact to device quiescent current and no impact to device start-up time.

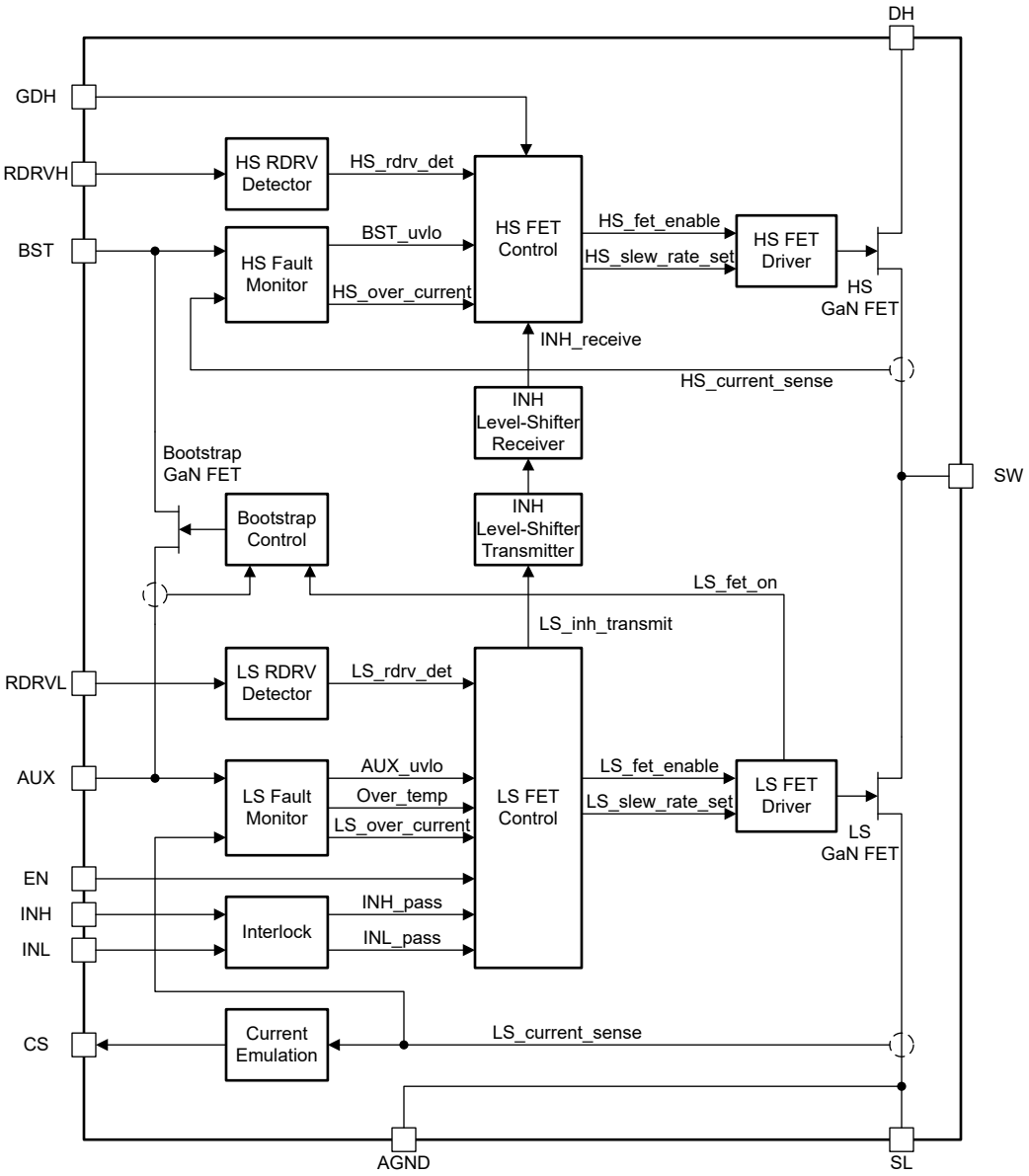
The bootstrap diode function between AUX and BST is implemented with a smart-switched GaN bootstrap FET. The switched GaN bootstrap FET allows more complete charging of the BST-to-SW capacitor since the on-state GaN bootstrap FET does not have the forward voltage drop of a traditional bootstrap diode. The smart-switched GaN bootstrap FET also avoids the traditional bootstrap diode problem of BST-to-SW capacitor overcharging due to off-state third-quadrant current flow in the low-side half-bridge GaN power FET. Finally, the bootstrap function has more efficient switching due to low capacitance and no reverse-recovery charge compared to the traditional bootstrap diode.

The AUX input supply wide voltage range is compatible with the corresponding wide range supply rail created by power supply controllers. The BST input supply range is even wider on the low end to account for capacitive droop in between bootstrap recharge cycles. Low AUX/BST idle quiescent currents and fast BST start-up time support converter burst-mode operation critical for meeting government light-load efficiency mandates. Further AUX quiescent current reduction is obtained by placing the device in standby mode with the EN pin.

The EN, INL, INH, and GDH control pins have high input impedance, low input threshold voltage, and maximum input voltage equal to the local supply pin voltage (AUX or BST to SW). This allows the pins to support both low voltage and high voltage input signals and be driven with low-power outputs.

The LMG2652H protection features are low-side or high-side under-voltage lockout (UVLO), INL/INH input gate-drive interlock, low-side or high-side cycle-by-cycle current limit, and low-side or high-side overtemperature shut down. The UVLO features also help achieve a well-behaved converter operation.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 GaN Power FET Switching Capability

Due to the long reign of the silicon FET as the dominant power-switch technology, many designers are unaware that the nameplate drain-source voltage cannot be used as an equivalent point to compare devices across technologies. The nameplate drain-source voltage of a silicon FET is set by the avalanche breakdown voltage. The nameplate drain-source voltage of a GaN FET is set by the long term compliance to data sheet specifications.

Exceeding the nameplate drain-source voltage of a silicon FET can lead to immediate and permanent damage. Meanwhile, the breakdown voltage of a GaN FET is much higher than the nameplate drain-source voltage. For example, the breakdown drain-source voltage of the LMG2652H GaN power FET is more than 800V which allows the LMG2652H to operate at conditions beyond an identically nameplate rated silicon FET.

The LMG2652H GaN power FET switching capability is explained with the assistance of Figure 7-1. The figure shows the drain-source voltage versus time for the LMG2652H GaN power FET for a single switch cycle in a switching application. No claim is made about the switching frequency or duty cycle.

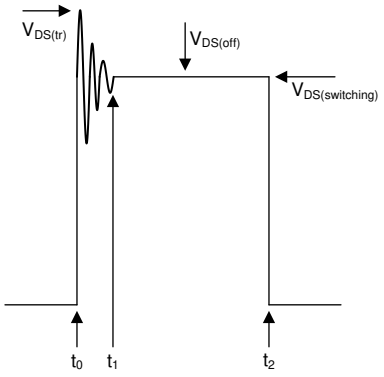


Figure 7-1. GaN Power FET Switching Capability

The waveform starts before t_0 with the FET in the on state. At t_0 the GaN FET turns off and parasitic elements cause the drain-source voltage to ring at a high frequency. The high frequency ringing damps out by t_1. Between t_1 and t_2 the FET drain-source voltage is set by the characteristic response of the switching application. The characteristic is shown as a flat line (plateau), but other responses are possible. At t_2 the GaN FET is turned on. For normal operation, the transient ring voltage is limited to 650V and the plateau voltage is limited to 520V. For rare surge events, the transient ring voltage limit is 800V and the plateau voltage limit is 720V.

7.3.2 Turn-On Slew-Rate Control

The turn-on slew rate of both the low-side and high-side GaN power FETs are individually programmed to one of four discrete settings. The low-side slew rate is programmed by the resistance between the RDRVL and AGND pins. The high-side slew rate is programmed by the resistance between the RDRVH and SW pins. The low-side slew-rate setting is determined one time during AUX power up when the AUX voltage goes above the AUX power-on reset voltage. The high-side slew-rate setting is determined one time during BST-to-SW power up when the BST-to-SW voltage goes above the BST power-on reset voltage. The slew-rate setting determination time is not specified but is around 0.4µs.

Table 7-1 shows the recommended typical resistance programming value for the four slew rate settings and the typical turn-on slew rate at each setting. As noted in the table, an open-circuit connection is acceptable for programming slew-rate setting 0 and a short-circuit connection (RDRVL shorted to AGND for the low-side turn-on slew rate) (RDRVH shorted to SW for the high-side turn-on slew rate) is acceptable for programming slew-rate setting 3.

Table 7-1. Slew-Rate Setting

TURN-ON SLEW RATE SETTING	RECOMMENDED TYPICAL PROGRAMMING RESISTANCE (kΩ)	TYPICAL TURN-ON SLEW RATE (V/ns)	COMMENT
0	120	2	Open-circuit connection for programming resistance is acceptable.
1	47	5	
2	22	23	
3	5.6	50	Short-circuit connection for programming resistance (RDRVL shorted to AGND for low-side slew rate) (RDRVH shorted to SW for high-side slew rate) is acceptable.

7.3.3 Current-Sense Emulation

The current-sense emulation function creates a scaled replica of the GaN power FET positive drain current at the output of the CS pin. The current-sense emulation gain, G_{CSE}, is 0.901mA output from the CS pin, I_{CS}, for every 1A passing into the drain of the low-side GaN power FET, I_D.

$$G_{CSE} = \frac{I_{CS}}{I_D} = \frac{0.901mA}{1A} = 0.000901 \quad (1)$$

The CS pin terminates with a resistor to AGND, R_{CS}, to create the current-sense voltage input signal to the external power supply controller.

R_{CS} is determined by solving for the traditional current-sense design resistance, $R_{CS(trad)}$, and multiplying by the inverse of G_{CSE}. The traditional current-sense design creates the current-sense voltage, $V_{CS(trad)}$, by passing the GaN power FET drain current, I_D, through $R_{CS(trad)}$. The LMG2652H creates the current-sense voltage, V_{CS}, by passing the CS pin output current, I_{CS}, through R_{CS}. The current-sense voltage must be the same for both designs.

$$V_{CS} = I_{CS} \times R_{CS} = V_{CS(trad)} = I_D \times R_{CS(trad)} \quad (2)$$

$$R_{CS} = \frac{I_D}{I_{CS}} \times R_{CS(trad)} = \frac{1}{G_{CSE}} \times R_{CS(trad)} \quad (3)$$

$$R_{CS} = 1110 \times R_{CS(trad)} \quad (4)$$

The CS pin is clamped internally to a typical 2.5V. The clamp protects vulnerable power-supply controller current-sense input pins from over voltage if, for example, the current sense resistor on the CS pin were to become disconnected.

Figure 7-2 shows the current-sense emulation operation. In both cycles, the CS pin current emulates the GaN power FET drain current while the GaN FET is enabled. The first cycle shows normal operation where the controller turns off the GaN power FET when the controller current-sense input threshold is tripped. The second cycle shows a fault situation where the LMG2652H overcurrent protection turns off the GaN power FET before the controller current-sense input threshold is tripped. In this second cycle, the LMG2652H avoids a hung controller IN pulse by generating a fast-ramping artificial current-sense emulation signal to trip the controller current-sense input threshold. The artificial signal persists until the IN pin goes to logic-low which indicates the controller is back in control of switch operation.

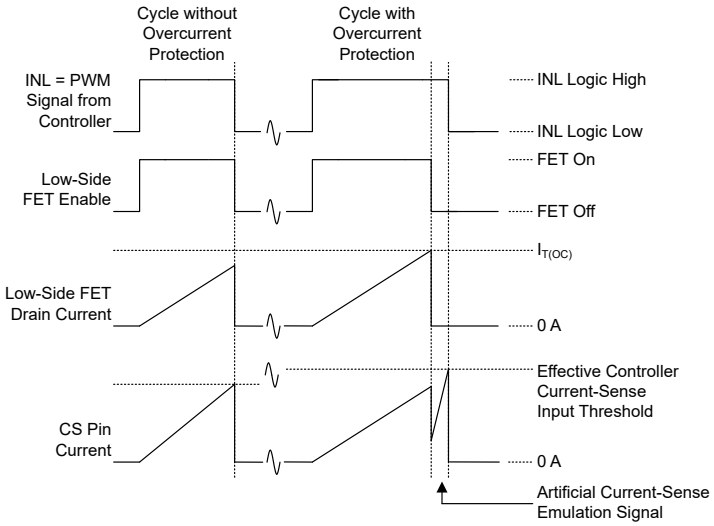


Figure 7-2. Current-Sense Emulation Operation

7.3.4 Bootstrap Diode Function

The internal bootstrap diode function is implemented with a smart-switched GaN bootstrap FET. The GaN bootstrap FET blocks current in both directions between AUX and BST when the GaN bootstrap FET is turned off.

The bootstrap diode function is active when the low-side GaN power FET is turned on and inactive when the low-side GaN power FET is turned off. The GaN bootstrap FET is held off in the bootstrap diode inactive phase. The GaN bootstrap FET turns on a single time at the beginning of the bootstrap active phase and is controlled as an ideal diode with diode current flowing from AUX to BST to charge the BST-to-SW capacitor. If a small reverse current from BST to AUX is detected after the GaN bootstrap FET is turned on, the GaN bootstrap FET is turned off for the remainder of the bootstrap active phase.

The bootstrap diode function implements a current limit to protect the GaN bootstrap FET when the BST-to-SW capacitor is significantly discharged at the beginning of the bootstrap active phase. If there is no current limit situation during the GaN bootstrap FET turn on, or if the bootstrap function drops out of current limit as the BST-to-SW capacitor charges, the current limit function is disabled for the remainder of the GaN bootstrap FET turn-on time. The current limit function is disabled to save quiescent current.

7.3.5 Input Control Pins (EN, INL, INH, GDH)

The EN pin is referenced to AGND and is used to toggle the device between the active and standby modes described in Section 7.4.

The INL pin is referenced to AGND and is used to turn the low-side GaN power FET on and off.

The INH pin is referenced to AGND and is used to turn the high-side GaN power FET on and off. The INH pin is compatible with controllers that use a low-side referenced gate drive signal to control the high-side GaN power FET.

The GDH pin is referenced to SW and is used to turn the high-side GaN power FET on and off. The GDH pin is compatible with controllers that use a high-side referenced signal to control the high-side GaN power FET.

The LMG2652H is intended to be used with either the INH pin or the GDH pin controlling the high-side GaN power FET. Short the unused pin to the reference of the pin (INH to AGND or GDH to SW).

The input control pins have a typical 1V input-voltage-threshold hysteresis for noise immunity. The pins also have a typical 400kΩ pull-down resistance to protect against floating inputs. The 400kΩ saturates for typical input voltages above 4V to limit the maximum input pull-down current to a typical 10uA. There are individual forward based ESD diodes from the EN, INL, and INH pins to the AUX pin. Avoid driving the EN, INL, and INH voltages higher than the AUX voltage. There is also a forward based ESD diode from the GDH pin to the BST pin. Avoid driving the GDH-to-SW voltage higher than the BST-to-SW voltage.

The following conditions block the INL turn-on action:

- Standby mode (as set by the EN pin above)
- INH in control of the INL/INH interlock
- AUX under-voltage lockout (UVLO)
- Low-side overtemperature protection
- Low-side GaN Power FET overcurrent protection

The following conditions block the INH turn-on action:

- Standby mode (as set by the EN pin above)
- INL in control of the INL/INH interlock
- AUX UVLO
- Low-side overtemperature protection
- BST UVLO
- High-side overcurrent protection

The following conditions block the GDH turn-on action:

- BST UVLO

- High-side overtemperature protection
- High-side overcurrent protection

Note that the low-side temperature protection blocks the INH pin while the high-side temperature protection blocks the GDH pin.

All the blocking conditions except the INL/INH interlock and the overcurrent protection act independently of the INL, INH, or GDH logic state. Figure 7-3 shows the operation of these control-input independent blocking conditions.

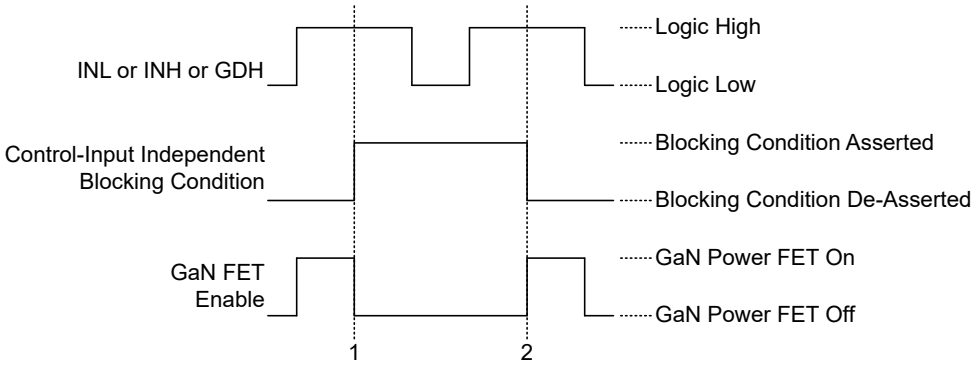


Figure 7-3. Control-Input-Independent Blocking Condition Operation

The INL/INH Interlock blocking action is described in Section 7.3.6. Meanwhile, the overcurrent protection blocking action only asserts after the control input turns on the respective GaN power FET of the control input. See Section 7.3.9 for the details.

7.3.6 INL - INH Interlock

The interlock function keeps the low-side and high-side GaN power FETs from simultaneously turning on when the INL and INH pins are both logic-high. Either the INL or the INH pin gains control of the interlock if either pin is logic high when the other pin is logic low. Once the INL or INH pin gains control of the interlock, the pin retains control as long as the pin remains logic high. Only the INL or INH pin in control of the interlock passes a logic-high signal through the interlock.

Note that there is no interlock feature regarding the GDH pin. This means it is possible to simultaneously turn on the low-side and high-side GaN power FETs if the INL and GDH pins are both logic-high.

7.3.7 AUX Supply Pin

The AUX pin is the input supply for the low-side internal circuits and is the power source to charge the BST-to-SW capacitor through the internal bootstrap diode function. The AUX external capacitance is recommended to be a ceramic capacitor that is at least three times larger than the BST-to-SW external capacitance over operating conditions.

7.3.7.1 AUX Power-On Reset

The AUX Power-On Reset disables all low-side functionality, including the INH pin function, if the AUX voltage is below the AUX Power-On Reset voltage. The AUX Power-On Reset voltage is not specified, but is around 5V. The AUX Power-On Reset initates the one-time determination of the low-side slew-rate setting programmed on the RDRVL pin if the AUX voltage goes above the AUX Power-On Reset voltage. The AUX Power-On Reset enables the low-side overtemperature protection function if the AUX voltage is above the AUX Power-On Reset voltage.

7.3.7.2 AUX Under-Voltage Lockout (UVLO)

The AUX UVLO blocks the INL pin from turning on the low-side GaN power FET and blocks the INH pin from turning on the high-side GaN power FET if the AUX voltage is below the AUX UVLO voltage. Figure 7-3 shows the AUX UVLO blocking operation. The AUX UVLO voltage is set higher than the BST UVLO voltage so the high-side GaN power FET can be operated when the low-side GaN power FET is operating. The voltage

separation between the AUX UVLO voltage and BST UVLO voltage accounts for operating conditions where the bootstrap charging of the BST-to-SW capacitor from the AUX supply is incomplete. The AUX UVLO voltage hysteresis prevents on-off chatter near the UVLO voltage trip point.

7.3.8 BST Supply Pin

The BST pin is the input supply for the high-side internal circuits. The BST pin and corresponding high-side circuits are referenced to the SW pin. The BST pin is powered by the low-side AUX Supply pin through the internal bootstrap diode function. The bootstrap function is inactive when the low-side GaN FET is off and the BST pin must rely on an external BST-to-SW capacitor for the BST power source.

Designing the BST-to-SW capacitance is a trade-off between high-side charge-up time and hold-up time. The BST-to-SW external capacitance is recommended to be a ceramic capacitor that is at least 10nF over operating conditions.

7.3.8.1 BST Power-On Reset

The BST Power-On Reset voltage is with respect to the SW pin. The BST Power-On Reset disables all high-side functionality if the BST-to-SW voltage is below the BST Power-On Reset voltage. The BST Power-On Reset voltage is not specified but is around 5V. The BST Power-On Reset initiates the one-time determination of the high-side slew-rate setting programmed on the RDRVH pin if the BST-to-SW voltage goes above the BST Power-On Reset voltage.

7.3.8.2 BST Under-Voltage Lockout (UVLO)

The BST UVLO voltage is with respect to the SW pin. The BST UVLO blocks both the INH and GDH pins from turning on the high-side GaN power FET if the BST-to-SW voltage is below the applicable BST UVLO voltage as described as follows. Figure 7-3 shows the BST UVLO blocking operation. The BST UVLO consists of two separate UVLO functions to create a two-level BST UVLO. The upper BST UVLO is called the BST Turn-On UVLO and only controls if the high-side GaN power FET is allowed to turn on. The lower BST UVLO is called the BST Turn-Off UVLO and only controls if the high-side GaN power FET is turned off after the high-side GaN power FET is already turned on. The operation of the two-level UVLO is not the same as a single UVLO with hysteresis.

Figure 7-4 shows the two-level BST UVLO operation. The BST Turn-On UVLO prevents the high-side GaN power FET from turning on, for INH or GDH logic-high, if the BST-to-SW voltage is below the BST Turn-On UVLO voltage (INH/GDH pulse #1, first portion of pulse #2, and pulse #5). After the high-side GaN power FET is successfully turned-on, the BST Turn-On UVLO is ignored and the BST Turn-Off UVLO output is watched for the remainder of the INH or GDH logic-high pulse (INH/GDH second portion of pulse #2, pulses #3, #4, and #6. The BST Turn-Off UVLO turns off the high-side GaN power FET for the remainder of the INH/GDH logic-high pulse if the BST-to-SW voltage falls below the BST Turn-Off UVLO voltage (INH/GDH pulse #6).

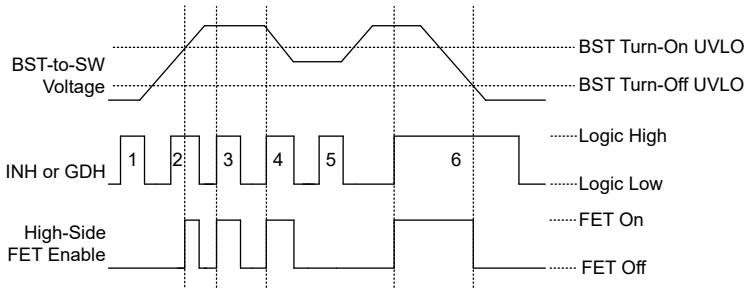


Figure 7-4. BST UVLO Operation

The effective voltage hysteresis of the two-level BST UVLO is the difference between the upper and lower BST UVLO voltages. A single-level BST UVLO can be implemented with the same hysteresis but allows subsequent high-side GaN power FET turn on anywhere in the hysteresis range. A single-level BST UVLO allows INH/GDH

pulse #5 to turn on the high-side GaN power. The two-level UVLO design prevents any turn on in the hysteresis range.

The two-level BST UVLO allows a wide hysteresis while making sure the BST-to-SW capacitor is adequately charged at the beginning of every INH or GDH pulse. The wide hysteresis allows a smaller BST-to-SW capacitor to be used which is useful for faster high-side start-up time. The adequate capacitor charge at the beginning of the INH or GDH pulse helps make sure the high-side GaN power FET is not turned-off early in the INH or GDH pulse which can create erratic converter operation.

7.3.9 Overcurrent Protection

The LMG2652H implements cycle-by-cycle overcurrent protection for both half-bridge GaN power FETs. Figure 7-5 shows the cycle-by-cycle overcurrent operation. Every INL or INH or GDH logic-high cycle turns on the controlled GaN power FET. If the GaN power FET drain current exceeds the overcurrent threshold current, the overcurrent protection turns off the GaN power FET for the remainder of the INL or INH or GDH logic-high duration.

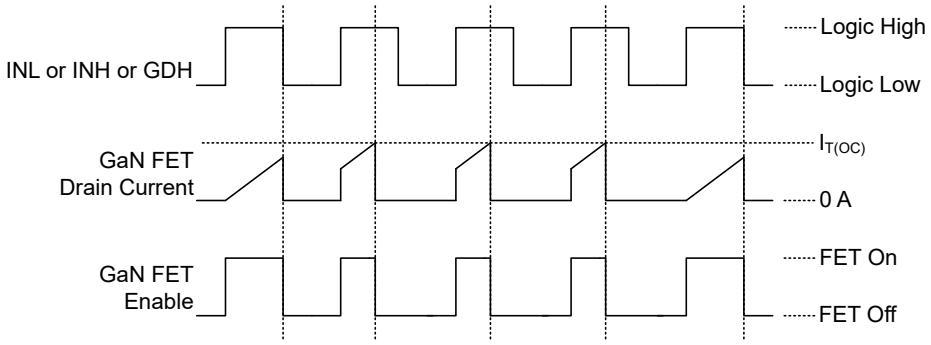


Figure 7-5. Cycle-by-Cycle Overcurrent Protection Operation

Cycle-by-cycle overcurrent protection minimizes system disruption because the event is not reported and because the protection allows the GaN power FET to turn on every INL or INH or GDH cycle.

As described in Section 7.3.3, after the low-side GaN power FET is turned off by the low-side overcurrent protection to prevent the controller from entering a hung state, an artificial CS pin current is produced.

7.3.10 Overtemperature Protection

The LMG2652H implements separate overtemperature protection for both the low-side and high-side device circuits. The low-side overtemperature protection blocks the INL pin from turning on the low-side GaN power FET and blocks the INH pin from turning on the high-side GaN power FET if the low-side temperature is above the overtemperature protection temperature. The high-side overtemperature protection blocks the GDH pin from turning on the high-side GaN power FET if the high-side temperature is above the overtemperature protection temperature. Figure 7-3 shows the overtemperature blocking operation. The overtemperature protection hysteresis avoids erratic thermal cycling.

The low-side overtemperature protection is enabled when the AUX voltage is above the AUX Power-On Reset voltage. The low AUX Power-On Reset voltage helps the overtemperature protection remain operational when the AUX rail droops during a power converter cool-down phase. The high-side overtemperature protection is enabled when the BST-to-SW voltage is above the BST Power-On Reset voltage.

7.4 Device Functional Modes

The LMG2652H has two modes of operation controlled by the EN pin. The device is in Active mode when the EN is logic high and in Standby mode when the EN pin is logic low. In active mode, the half-bridge GaN power FETs are controlled by the INL, INH, and GDH pins. In Standby mode, the INL and INH pins are ignored, the low-side GaN power FET and bootstrap diode are held off, the INH pin is blocked from turning on the high-side FET, and the AUX quiescent current is reduced to the AUX standby quiescent current. Note that in Standby mode the high-side GaN power FET can still be controlled by the GDH pin if the BST pin is powered by an external source.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The LMG2652H is a GaN power-FET half bridge with plug-and-play simplicity since it integrates the half-bridge FETs, FET gate drivers, high-side gate-drive level shifter, bootstrap diode function, and current-sense emulation in a single package. The integrated gate driver, low IN input threshold voltage, and wide AUX input-supply voltage allows the LMG2652H to seamlessly pair with common industry power-supply controllers.

8.2 Typical Application

8.2.1 LLC Application

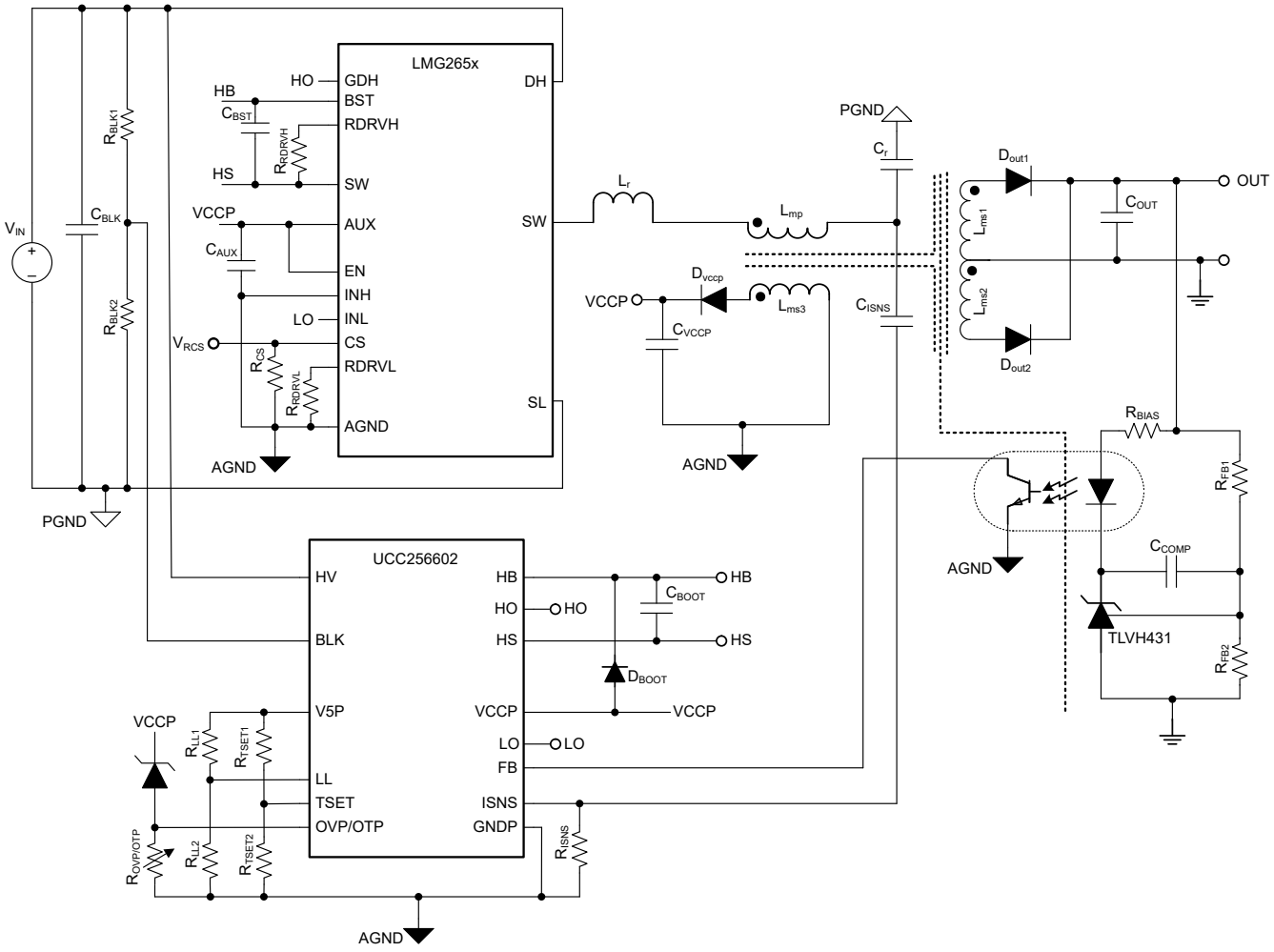


Figure 8-1. 200W LLC Converter Application

8.2.1.1 Design Requirements

Table 8-1. Design Specification

SPECIFICATION	VALUE
Input DC voltage range	365VDC to 410VDC
Output DC voltage	19.5V
Ouput rated current	10.3A
Output voltage ripple at 390VDC	120mVpp
Peak efficiency at 390VDC	93%

8.2.1.2 Detailed Design Procedure

The typical application shows the LMG2652H pairing a LLC controller to create a high-power-density, high-efficiency, 200W, LLC converter. The 200W LLC converter application is adapted from the typical application. This detailed design procedure focuses on the specifics of using the LMG2652H in the application.

8.2.1.3 Application Curves

The following waveform shows typical switching waveforms. The red trace is the switch-node voltage of LMG2652H, the green trace is the current-sense voltage across R_{ISNS}, and the blue trace is V_{OUT}.

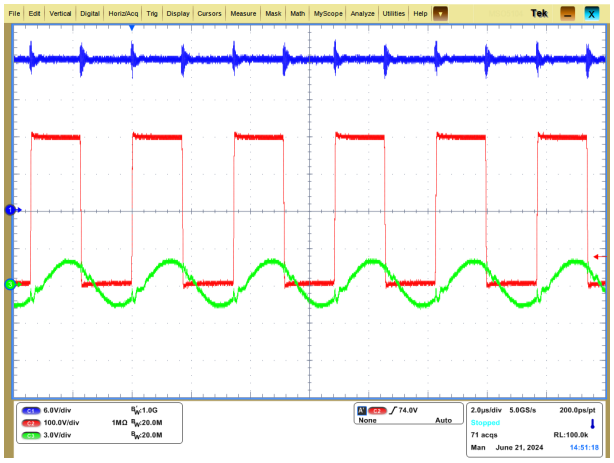


Figure 8-2. V_{IN} = 400VDC

8.2.2 AHB Application

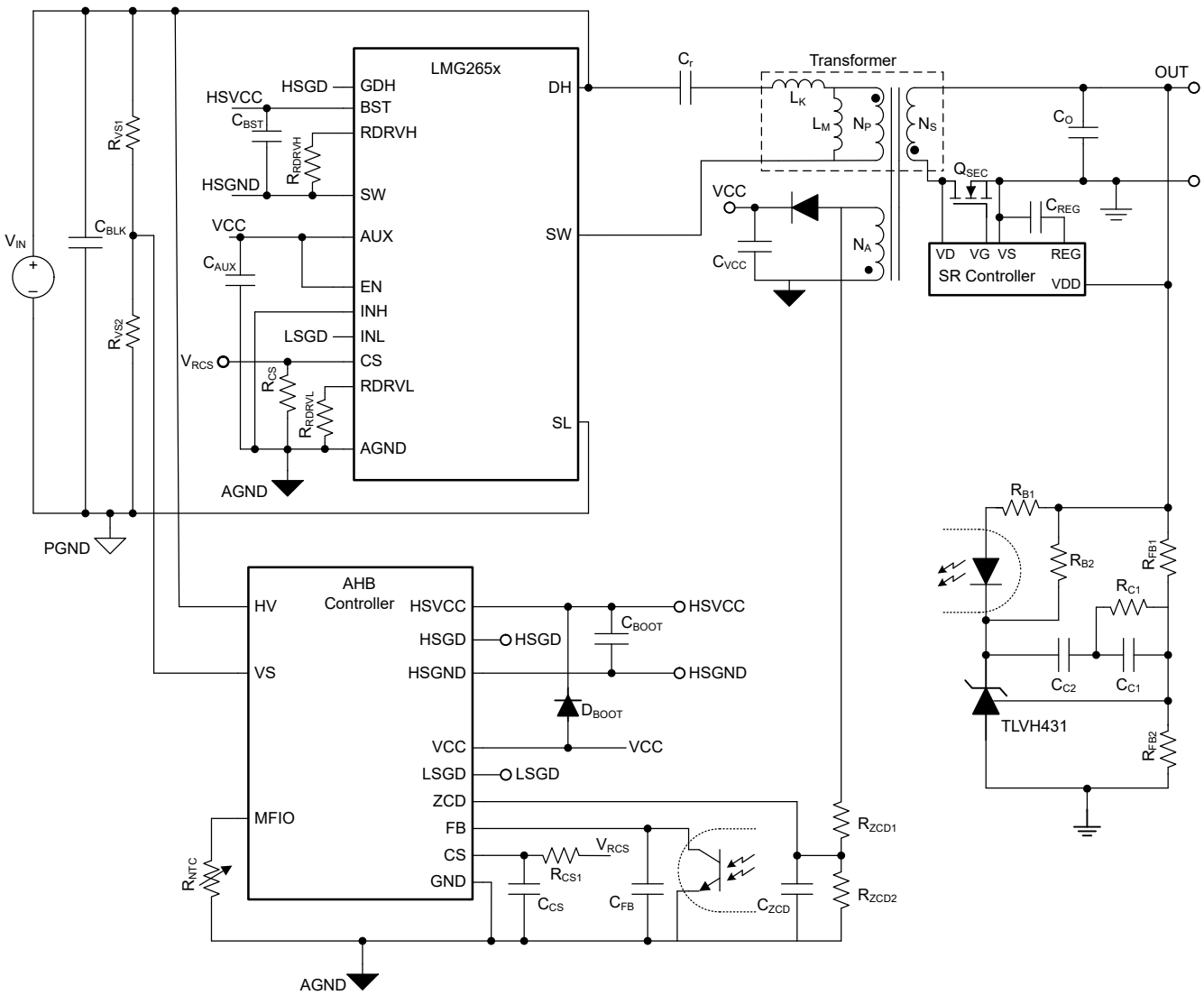


Figure 8-3. 140W AHB Converter Application

8.2.3 Motor Drives Application

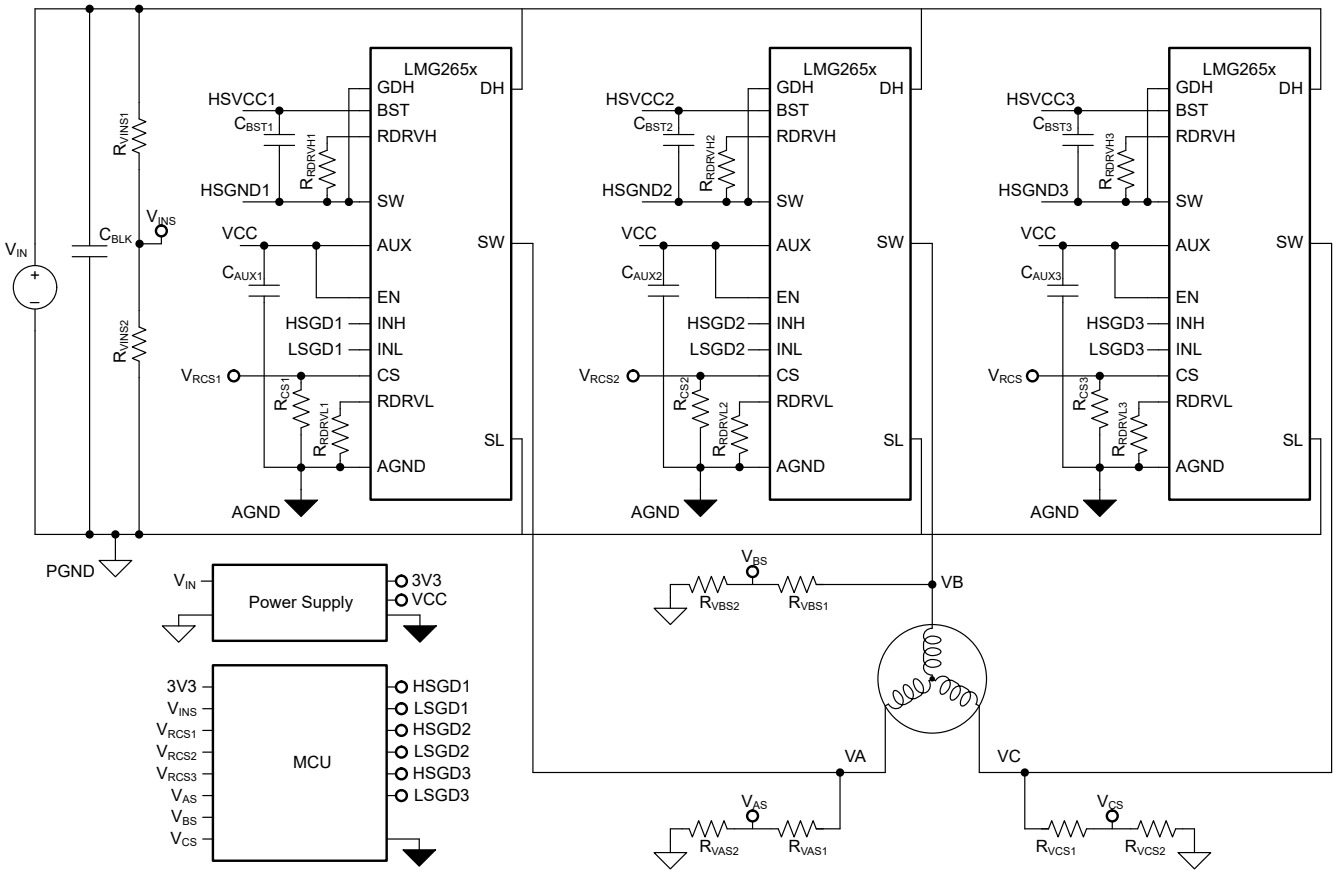


Figure 8-4. 5A Motor Drivers Application

8.3 Power Supply Recommendations

The LMG2652H operates from a single input supply connected to the AUX pin. The BST pin is powered internally by the AUX pin. The LMG2652H is intended to be operated from the same supply managed and used by the power supply controller. The wide recommended AUX voltage range of 10V to 26V overlaps common-controller supply-pin turn-on and UVLO voltage limits.

The AUX external capacitance is recommended to be a ceramic capacitor that is at least three-times larger than the BST-to-SW capacitance over operating conditions.

8.4 Layout

8.4.1 Layout Guidelines

8.4.1.1 Solder-Joint Stress Relief

Large QFN packages can experience high solder-joint stress. Several best practices are recommended to provide solder-joint stress relief. First, the instructions for the NC anchor pins found in Section 4 section must be followed. Second, all the board solder pads must be non-solder-mask defined (NSMD) as shown in the land pattern example within the Section 11 section. Finally, verify that any board trace that connects to an NSMD pad is less than 2/3 the width of the pad on the pad side where connected. The trace must maintain this 2/3 width limit for as long as the trace is not covered by solder mask. After the trace is under solder mask, there are no limits on the trace dimensions. All these recommendations are followed in Section 8.4.2.

8.4.1.2 Signal-Ground Connection

Design the power supply with separate signal and power grounds that only connect in one location. Connect the LMG2652H AGND pin to signal ground. Connect the LMG2652H SL pin and low-side thermal pad to power ground. The LMG2652H serves as the single connection point between the signal and power grounds since the AGND pin, SL pin, and low-side thermal pad are connected internally. Do not connect the signal and power grounds anywhere else on the board except as recommended in the next sentence.

8.4.1.3 CS Pin Signal

As seen with Equation 4, the current-sense signal impedance is three orders of magnitude higher than a traditional current-sense signal. This higher impedance has implications for current-sense signal noise susceptibility. Minimize routing the current-sense signal near any noisy traces. Place the current-sense resistor and any filtering capacitors at the far end of the trace next to the controller current-sense input pin.

8.4.2 Layout Example

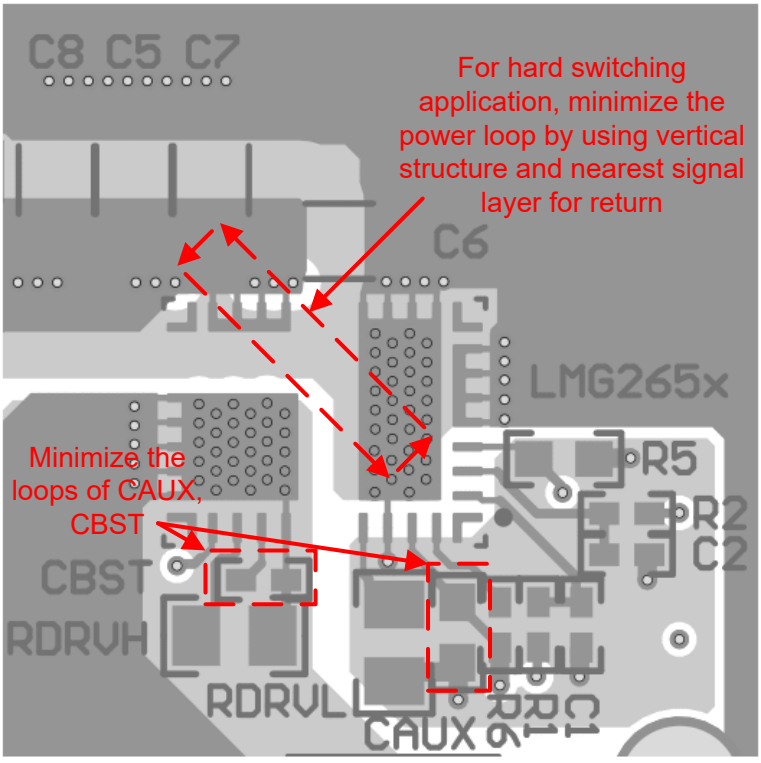


Figure 8-5. PCB Top Layer (Dark Grey) and Second-Layer (Light Grey) Layout

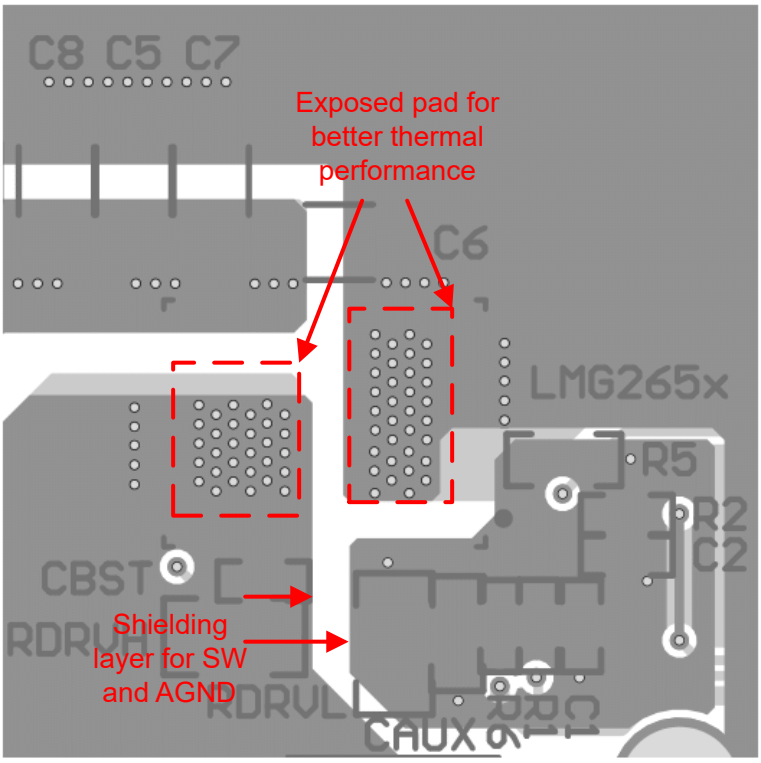


Figure 8-6. PCB Third-Layer (Dark Grey) and Bottom-Layer (Light Grey) Layout

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
February 2026	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMG2652HRFBR	Active	Production	VQFN (RFB) | 19	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-	LMG2652

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

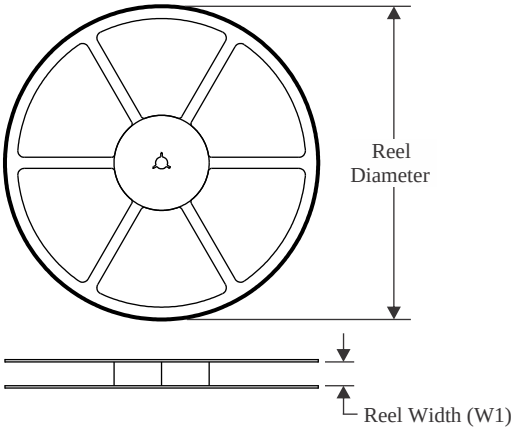
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

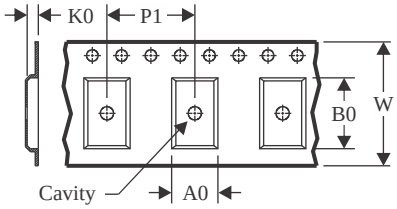
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

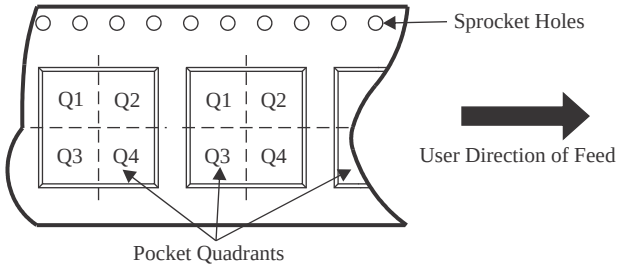


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

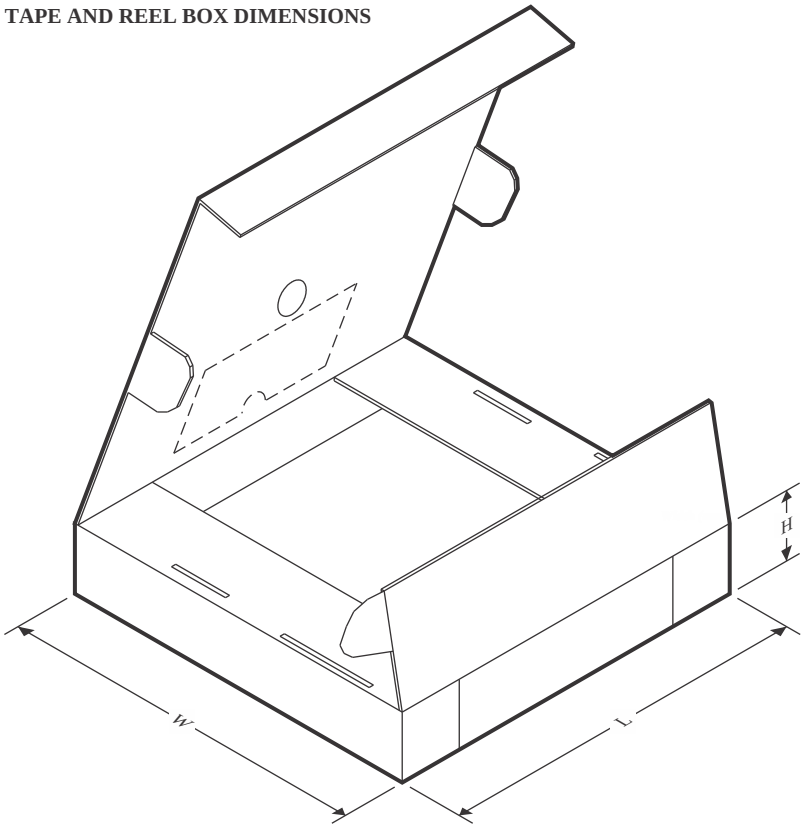
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMG2652HRFBR	VQFN	RFB	19	2000	330.0	16.4	6.3	8.3	1.34	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

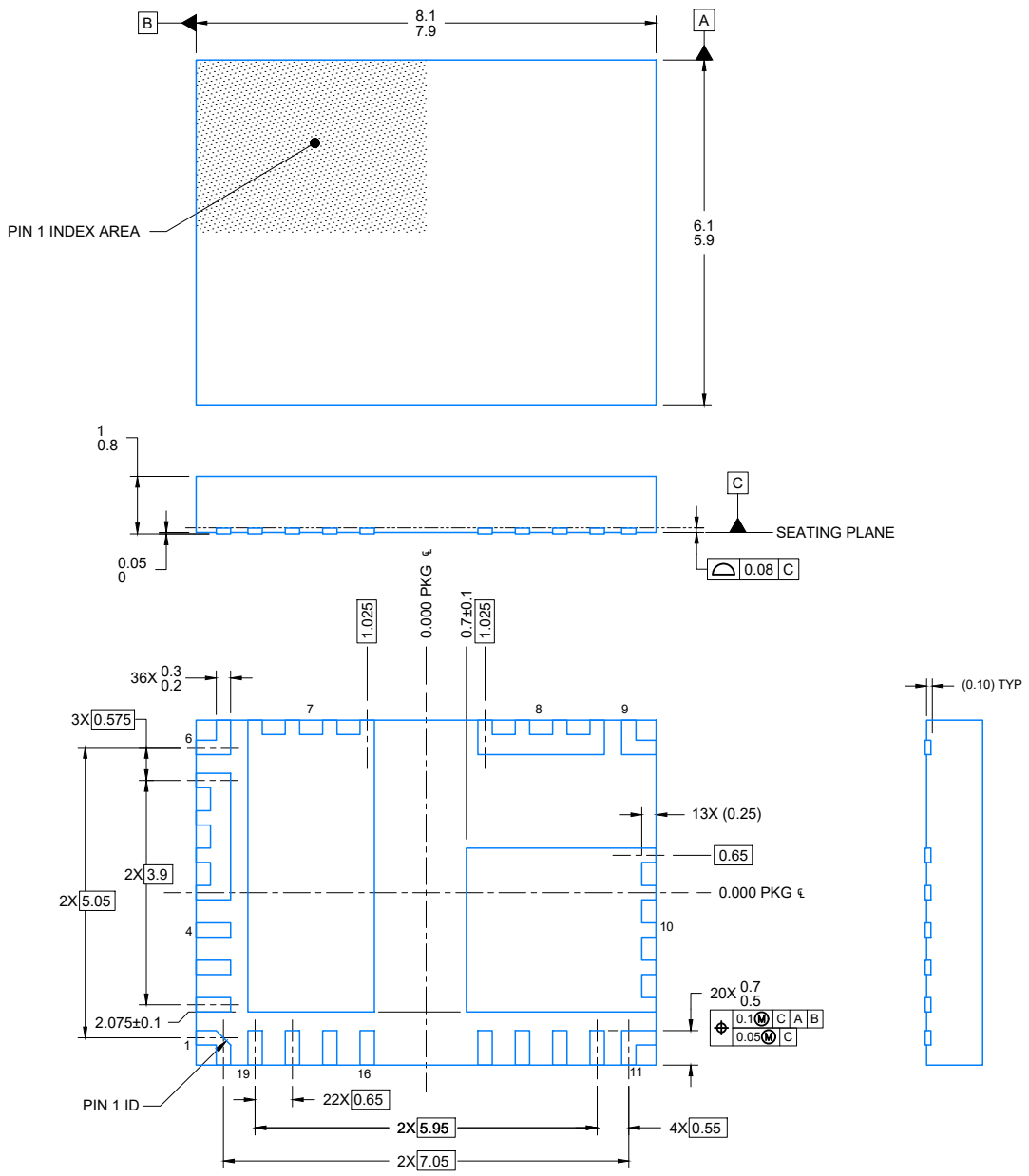
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMG2652HRFBR	VQFN	RFB	19	2000	367.0	367.0	38.0

PACKAGE OUTLINE

RFB0019A

VQFN - 1 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD



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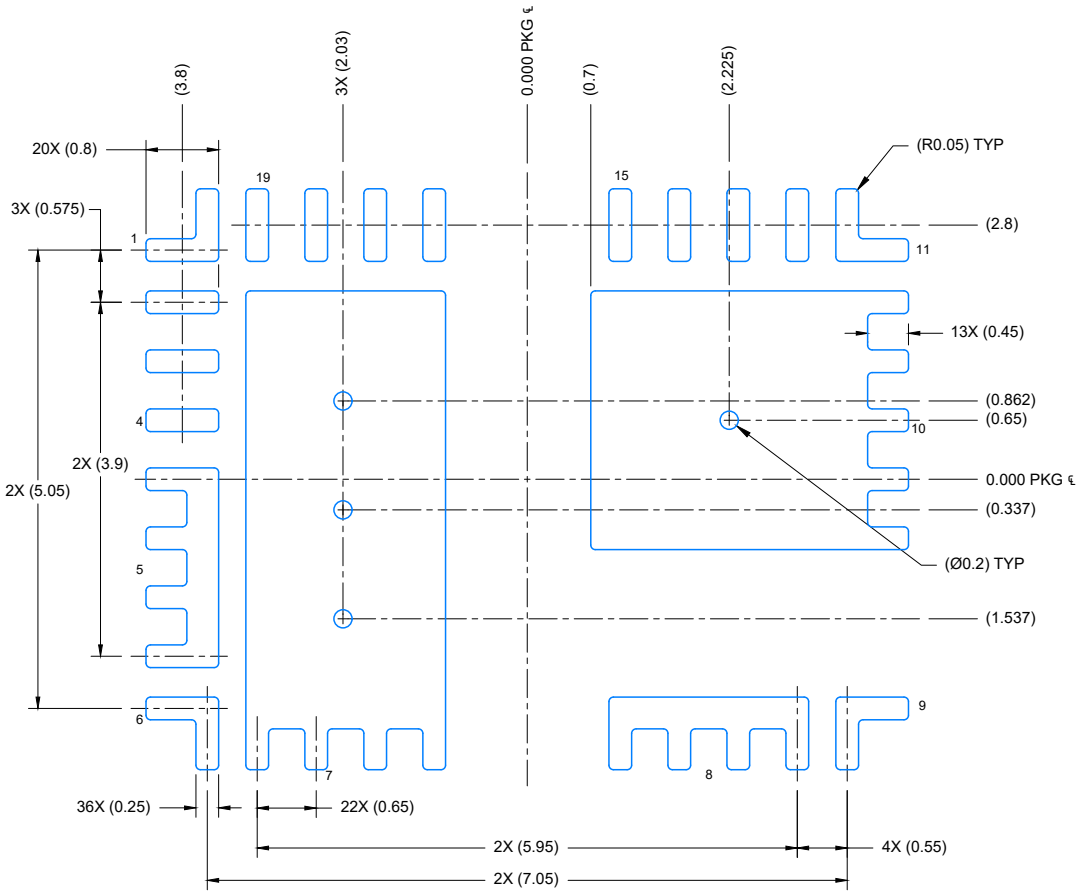
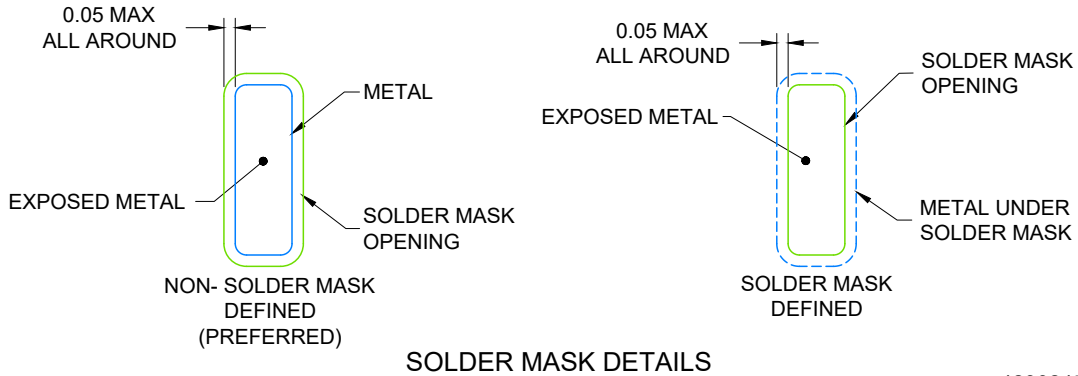
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 12X



SOLDER MASK DETAILS

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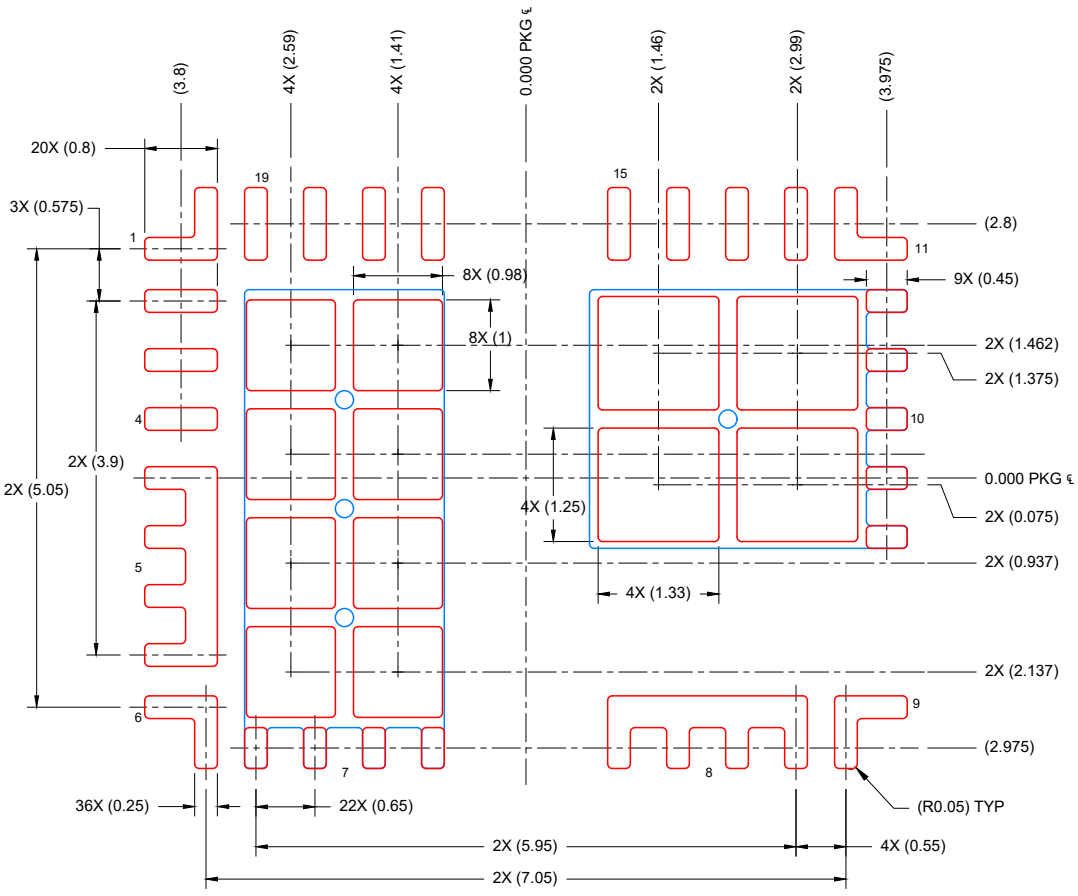
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 12X

4230245/C 01/2025

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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