

# LM27762 Low-Noise Positive and Negative Output Integrated Charge Pump Plus LDO

## 1 Features

- Generates low-noise adjustable positive supply voltage between 1.5V and 5V and negative supply voltage between -1.5V and -5V
- 2.7V to 5.5V input voltage range
- $\pm 250\text{mA}$  output current
- Inverting charge pump followed by negative LDO
- 2MHz low-noise fixed-frequency operation
- $2.5\Omega$  inverter output impedance,  $V_{IN} = 5\text{V}$
- 30mV at 100mA negative LDO dropout voltage,  $V_{OUT} = -5\text{V}$
- Positive LDO with 45mV dropout voltage at 100mA,  $V_{OUT} = 5\text{V}$
- 390 $\mu\text{A}$  quiescent current (typical)
- Shutdown quiescent current to 0.5 $\mu\text{A}$  (typical)
- Current limit and thermal protection
- Power-Good pin (active low)

## 2 Applications

- Hi-Fi audio headphone amplifiers
- Operational amplifier power biasing
- Powering data converters
- Wireless communication systems
- Interface power supplies
- Handheld instrumentation

## 3 Description

The LM27762 delivers very low-noise positive and negative outputs that are adjustable between  $\pm 1.5\text{V}$  and  $\pm 5\text{V}$ . Input voltage range is from 2.7V to 5.5V, and output current goes up to  $\pm 250\text{mA}$ . With an operating current of only 390 $\mu\text{A}$  and 0.5 $\mu\text{A}$  typical shutdown current, the LM27762 provides excellent performance for power amplifier and DAC bias and other high-current, low-noise negative voltage needs. The device provides a small design size with few external components.

Negative voltage is generated by a regulated inverting charge pump followed by a low-noise negative LDO. The inverting charge pump of the LM27762 device operates at 2MHz (typical) switching frequency to reduce output resistance and voltage ripple. Positive voltage is generated from the input by a low-noise positive LDO.

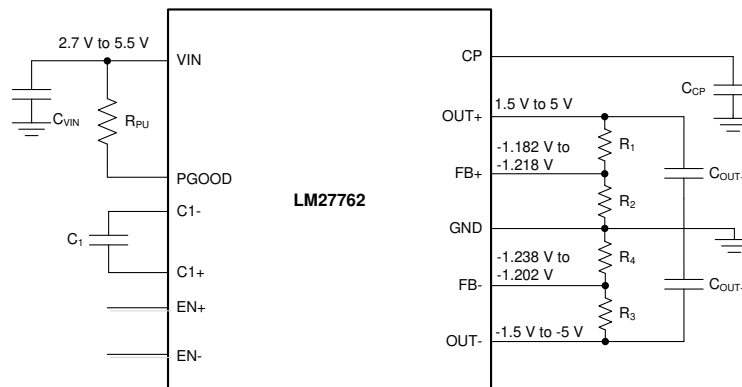
Positive and negative outputs of LM27762 have dedicated enable inputs. These outputs support independent timing for the positive and negative rails for specific system power-sequence needs. Enable inputs can be also shorted together and connected to the input voltage. The LM27762 has an optional Power-Good feature.

### Package Information

PART NUMBER	PACKAGE <sup>(1)</sup>	PACKAGE SIZE <sup>(2)</sup>
LM27762	DSS (WSON, 12)	3mm × 2mm

(1) For more information, see [Section 10](#).

(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematic

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## 4 Pin Configuration and Functions

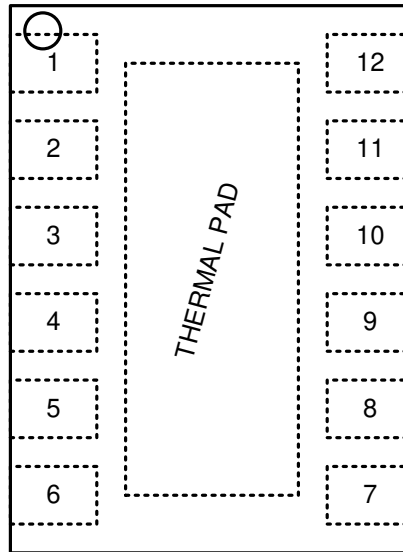


Figure 4-1. DSS Package, 12-Pin WSON With Thermal Pad (Top View)

Table 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
C1+	10	Power	Positive terminal for C <sub>1</sub>
C1–	9	Power	Negative terminal for C <sub>1</sub>
CP	5	Power	Negative unregulated output voltage
EN+	12	Input	Enable input for the positive LDO, Active high
EN–	8	Input	Enable input for the charge pump and negative LDO, Active high
FB+	2	Power	Feedback input. Connect FB+ to an external resistor divider between OUT+ and GND. <i>DO NOT</i> leave unconnected.
FB–	7	Power	Feedback input. Connect FB– to an external resistor divider between OUT– and GND. <i>DO NOT</i> leave unconnected.
GND	4	Ground	Ground
OUT+	11	Power	Regulated positive output voltage
OUT–	6	Power	Regulated negative output voltage
PGOOD	1	Output	Power Good flag; open drain; Logic 0 = power good, Logic 1 = power not good. Connect to ground if not used.
VIN	3	Power	Positive power supply input
Thermal Pad	—	Ground	Ground. <b>DO NOT</b> leave unconnected.

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup> <sup>(2)</sup>

	MIN	MAX	UNIT
VIN to GND or GND to VOUT		5.8	V
EN+, EN-	GND – 0.3	V <sub>IN</sub>	V
CPOUT, OUT+ and OUT- , continuous output current		300	mA
OUT+, OUT- short-circuit duration to GND <sup>(3)</sup>		1	s
Continuous power dissipation <sup>(4)</sup>	Internally limited		
T <sub>JMAX</sub> <sup>(4)</sup>		150	°C
Operating input voltage, V <sub>IN</sub>	2.7	5.5	V
Operating output current, I <sub>OUT</sub>	0	250	mA
Operating ambient temperature, T <sub>A</sub>	–40	85	°C
Operating junction temperature, T <sub>J</sub>	–40	125	°C
Storage temperature, T <sub>stg</sub>	–65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under [Section 5.3](#). Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) If Military/Aerospace specified devices are required, contact the TI Sales Office/Distributors for availability and specifications.
- (3) OUT may be shorted to GND for one second without damage. However, shorting OUT to VIN may damage the device and must be avoided. Also, for temperatures above T<sub>A</sub> = 85°C, V<sub>OUT</sub> must not be shorted to GND or VIN or device may be damaged.
- (4) Internal thermal shutdown circuitry protects the device from damage.

### 5.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub> Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±1000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±250	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Operating ambient temperature, T <sub>A</sub>	–40	85	°C
Operating junction temperature, T <sub>J</sub>	–40	125	°C

### 5.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		LM27762	UNIT
		DSS (WSON)	
		12 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	62.2	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	54.7	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	25.6	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	1.8	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	25.6	°C/W

THERMAL METRIC <sup>(1)</sup>		LM27762	
		DSS (WSO <sub>N</sub> )	
		12 PINS	
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	9.2	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.

## 5.5 Electrical Characteristics

Typical limits apply for T<sub>A</sub> = 25°C; minimum and maximum limits apply over the full temperature range. Unless otherwise specified V<sub>IN</sub> = 5 V, C<sub>IN</sub> = C<sub>OUT+</sub> = C<sub>OUT-</sub> = 2.2 μF, C<sub>1</sub> = 1 μF, C<sub>POUT</sub> = 4.7 μF.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I <sub>Q</sub>	Supply current	Open circuit, no load, EN+, EN– connected to VIN. <sup>(1)</sup>		390		μA
I <sub>SD</sub>	Shutdown supply current			0.5	5	μA
f <sub>SW</sub>	Switching frequency	V <sub>IN</sub> = 3.6 V	1.7	2	2.3	MHz
R <sub>NEG</sub>	Output resistance to C <sub>POUT</sub>	V <sub>IN</sub> = 5.5 V, I <sub>L</sub> = 100 mA		2.5		Ω
V <sub>LDO-</sub>	LDO dropout voltage	I <sub>L</sub> = 100 mA, V <sub>OUT-</sub> = –5 V		30		mV
PSRR	Power supply rejection ratio, OUT–	I <sub>L</sub> = 100 mA, V <sub>OUT-</sub> = –1.8 V, 10 kHz		50		dB
V <sub>N-</sub>	Output noise voltage	I <sub>L</sub> = 80 mA, 10 Hz to 100 kHz		22		μV <sub>RMS</sub>
V <sub>FB-</sub>	Feedback pin reference voltage		–1.238	–1.22	–1.202	V
V <sub>OUT-</sub>	Adjustable output voltage	5.5 V ≥ V <sub>IN</sub> ≥ 2.7 V	–5		–1.5	V
	Load regulation	0 to 250 mA, V <sub>OUT-</sub> = –1.8 V		34		μV/mA
	Line regulation	5 V ≥ V <sub>IN</sub> ≥ 2.7 V, I <sub>L</sub> = 50 mA		1.5		mV/V
V <sub>LDO+</sub>	LDO dropout voltage	I <sub>L</sub> = 100 mA, V <sub>OUT+</sub> = 5 V		45		mV
PSRR	Power supply rejection ratio, OUT+	I <sub>L</sub> = 100 mA, V <sub>OUT+</sub> = 1.8 V, 10 kHz		43		dB
V <sub>N+</sub>	Output noise voltage	I <sub>L</sub> = 80 mA, 10 Hz to 100 kHz		22		μV <sub>RMS</sub>
V <sub>FB+</sub>	Feedback pin reference voltage		1.182	1.2	1.218	V
V <sub>OUT+</sub>	Adjustable output voltage	5.5 V ≥ V <sub>IN</sub> ≥ 2.7 V	1.5		5	V
	Load regulation	0 to 250 mA, V <sub>OUT+</sub> = 1.8 V		11		μV/mA
	Line regulation	5 V ≥ V <sub>IN</sub> ≥ 2.7 V, I <sub>L</sub> = 50 mA		1.9		mV/V
V <sub>IH</sub>	Enable pin input voltage high	5.5 V ≥ V <sub>IN</sub> ≥ 2.7 V	1.2			V
V <sub>IL</sub>	Enable pin input voltage low	5.5 V ≥ V <sub>IN</sub> ≥ 2.7 V			0.4	V

(1) When VIN = 5.5V charge pump may enter PWM mode in hot conditions.

## 5.6 Typical Characteristics

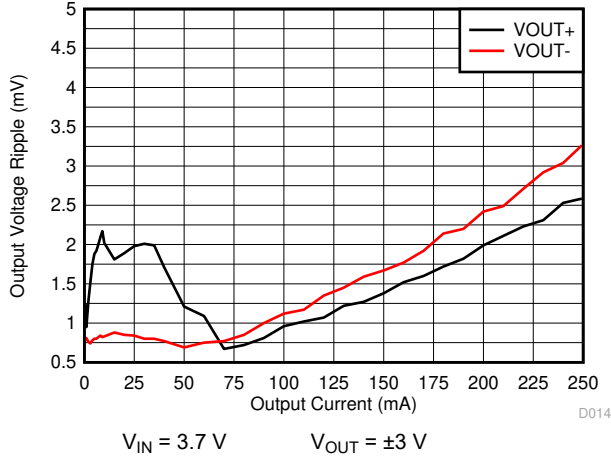


Figure 5-1. Output Voltage Ripple vs Output Current

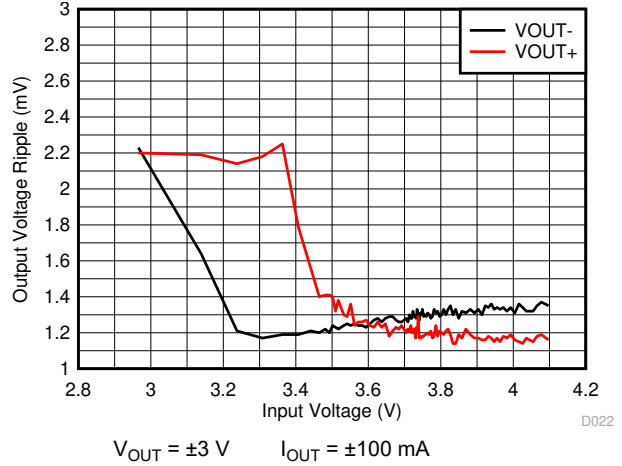


Figure 5-2. Output Voltage Ripple vs Input Voltage

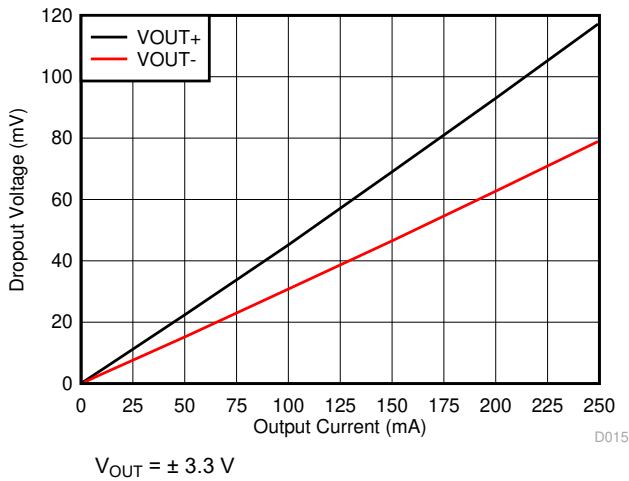


Figure 5-3. LDO Dropout Voltage vs Output Current

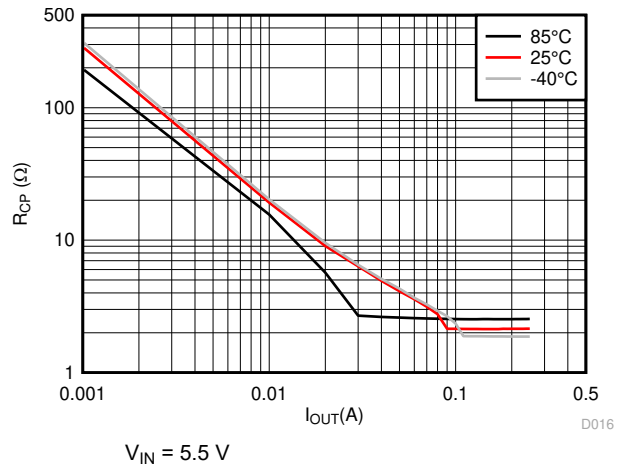


Figure 5-4. Charge Pump Output Resistance vs Output Current

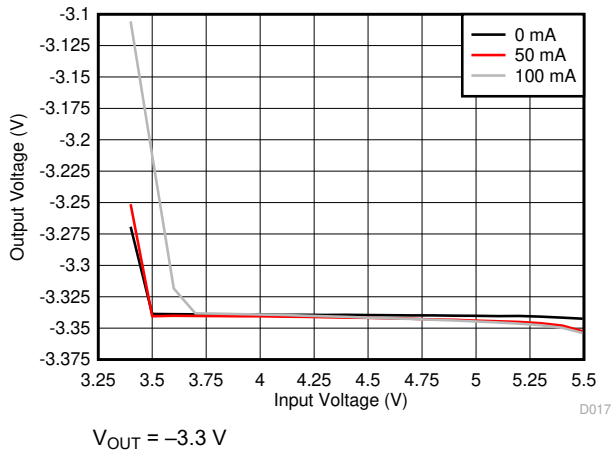


Figure 5-5. Line Regulation for OUT-

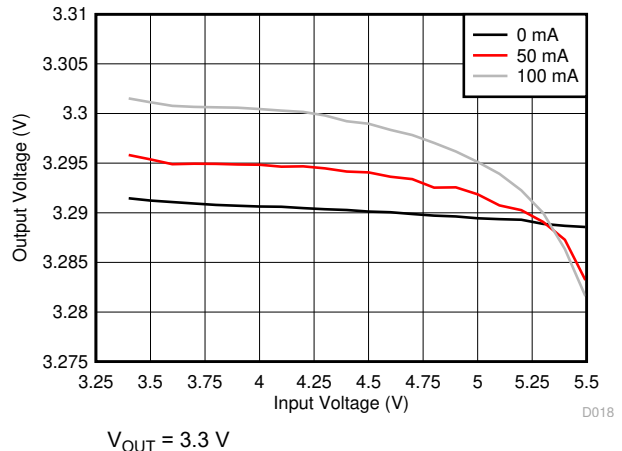


Figure 5-6. Line Regulation for OUT+

### 5.6 Typical Characteristics (continued)

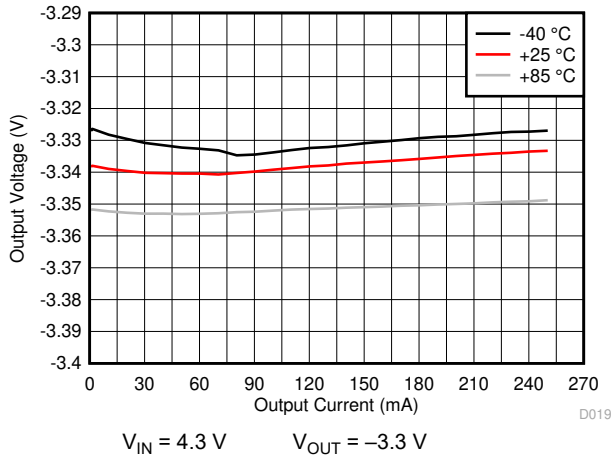


Figure 5-7. Load Regulation for OUT-

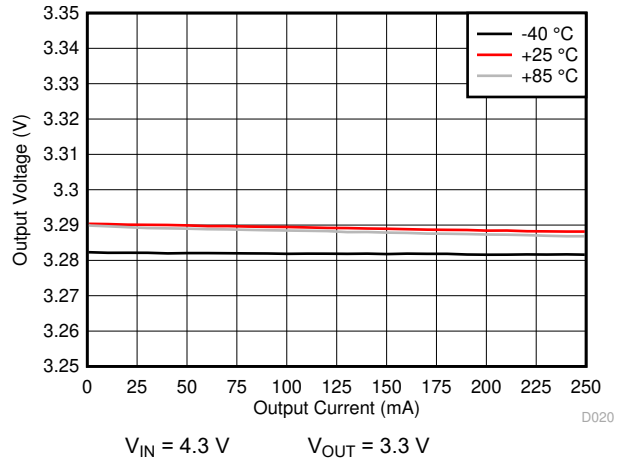


Figure 5-8. Load Regulation for OUT+

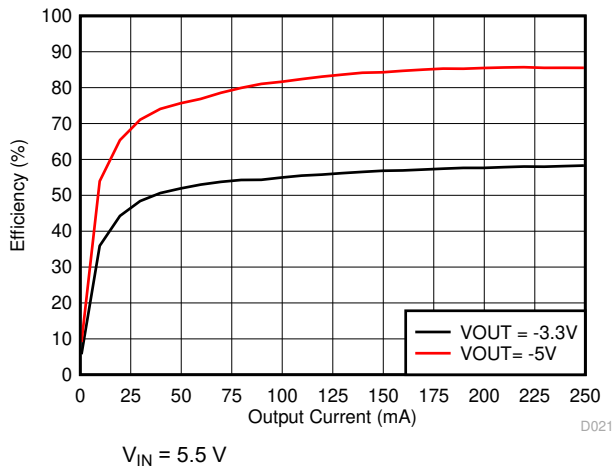


Figure 5-9. Efficiency for OUT-

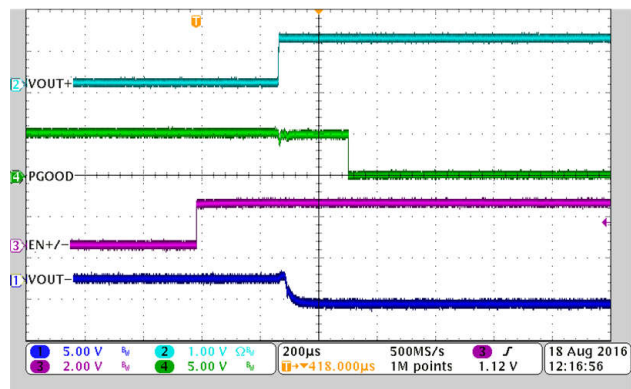


Figure 5-10. Start-Up

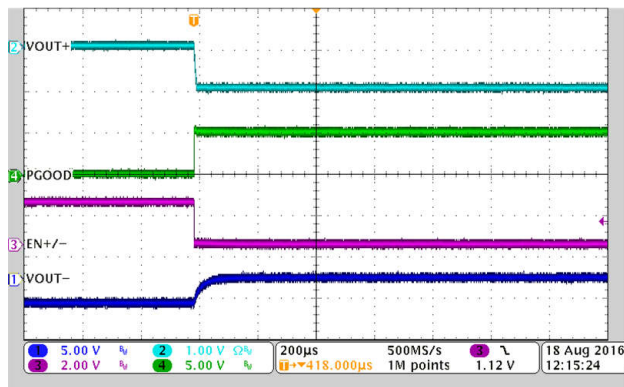


Figure 5-11. Shutdown

## 6 Detailed Description

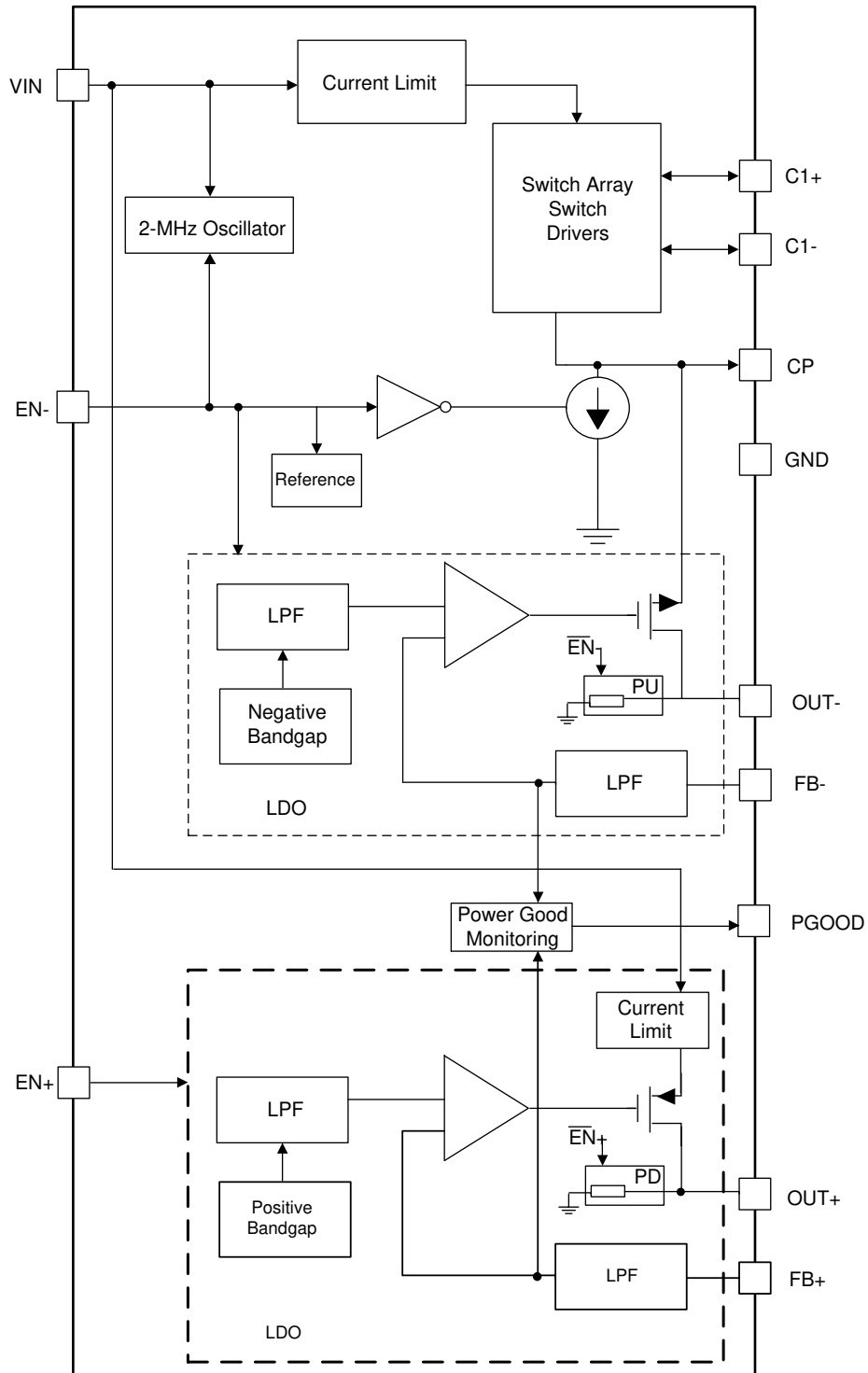
### 6.1 Overview

The LM27762 low-noise, inverting charge pump with both positive and negative LDOs delivers very low-noise adjustable positive and negative outputs between  $\pm 1.5$  V and  $\pm 5$  V. The output voltage levels of the positive and negative LDO are independently controllable with external resistors. Input voltage range of LM27762 is from 2.7 V to 5.5 V. Five low-cost capacitors are used in this circuit to provide up to  $\pm 250$  mA of output current. The LM27762 operates at 2-MHz (typical) switching frequency to reduce output resistance and voltage ripple. With an typical operating current of only 390  $\mu$ A and 0.5- $\mu$ A typical shutdown current, the LM27762 provides ideal performance for power amplifiers and DAC bias and other high-current, low-noise negative voltage needs.

The LM27762 device has an enable input (EN+) for the positive LDO and another enable input (EN-) for the negative charge pump and LDO. This supports independent timing for the positive and negative rails in system power sequence. Enable inputs can be also shorted together and connected to VIN. When LDO is disabled, output of the positive LDO has 50-k $\Omega$  pulldown to ground, and output of the negative LDO has 50-k $\Omega$  pullup to ground. The LM27762 has power good monitoring for OUT+ and OUT- outputs. The PGOOD pin is an open-drain output and requires an external pullup resistor. When the Power-Good feature is not used, the PGOOD pin can be connected to ground.



## 6.2 Functional Block Diagram



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## 6.3 Feature Description

### 6.3.1 Undervoltage Lockout

The LM27762 has an internal comparator that monitors the voltage at  $V_{IN}$  and forces the device into shutdown if the input voltage drops to 2.4 V. If the input voltage rises above 2.6 V, the LM27762 resumes normal operation.

### 6.3.2 Input Current Limit

The LM27762 contains current limit circuitry that protects the device in the event of excessive input current and/or output shorts to ground. The charge pump and positive LDO both have 500 mA (typical) input current limit when the output is shorted directly to ground. When the LM27762 is current limiting, power dissipation in the device is likely to be quite high. In this event, thermal cycling is expected.

### 6.3.3 PFM Operation

To minimize quiescent current during light load operation, the LM27762 allows PFM or pulse-skipping operation. By allowing the charge pump to switch less when the output current is low, the quiescent current drawn from the power source is minimized. The frequency of pulsed operation is not limited and can drop into the sub-2-kHz range when unloaded. As the load increases, the frequency of pulsing increases until it transitions to constant frequency. The fundamental switching frequency in the LM27762 is 2 MHz.

### 6.3.4 Output Discharge

In shutdown, the LM27762 actively pulls down on the outputs (OUT+, OUT–) of the device until the output voltage reaches GND.

### 6.3.5 Power-Good Output (PGOOD)

The LM27762 has monitoring for the OUT+ and OUT– output voltage levels and open-drain PGOOD output.

**Table 6-1. PGOOD (Active Low) Operation**

EN+	EN–	OUT+	OUT–	PGOOD
Low	Low	Do not care	Do not care	High
High	Low	< 95% of target value	Do not care	High
High	Low	> 95% of target value	Do not care	Low
Low	High	Do not care	< 95% of target value	High
Low	High	Do not care	> 95% of target value	Low
High	High	< 95% of target value	Do not care	High
High	High	Do not care	< 95% of target value	High
High	High	> 95% of target value	> 95% of target value	Low

### 6.3.6 Thermal Shutdown

The LM27762 implements a thermal shutdown mechanism to protect the device from damage due to overheating. When the junction temperature rises to 150°C (typical), the device switches into shutdown mode. The LM27762 releases thermal shutdown when the junction temperature is reduced to 130°C (typical).

Thermal shutdown is most often triggered by self-heating, which occurs when there is excessive power dissipation in the device and/or insufficient thermal dissipation. The LM27762 device power dissipation increases with increased output current and input voltage. When self-heating brings on thermal shutdown, thermal cycling is the typical result. Thermal cycling is the repeating process where the part self-heats, enters thermal shutdown (where internal power dissipation is practically zero), cools, turns on, and then heats up again to the thermal shutdown threshold. Thermal cycling is recognized by a pulsing output voltage and can be stopped by reducing the internal power dissipation (reduce input voltage and/or output current) or the ambient temperature. If thermal cycling occurs under desired operating conditions, thermal dissipation performance must be improved to accommodate the power dissipation of the device.

## 6.4 Device Functional Modes

### 6.4.1 Shutdown Mode

When enable pins (EN+, EN–) are low, both positive and negative outputs of LM27762 are disabled, and the device is in shutdown mode reducing the quiescent current to minimum level. In shutdown, the outputs of the LM27762 are pulled to ground (internal 50 kΩ between each OUT pin and ground).

### 6.4.2 Enable Mode

Applying a voltage greater than 1.2 V to the EN+ pin enables the positive LDO. Applying a voltage greater than 1.2 V to the EN– pin enables the negative CP and LDO. When enabled, the positive and negative output voltages are equal to levels set by external resistors. Care must be taken to both the positive LDO and the inverting charge pump followed by negative LDO have enough headroom. Power Good output PGOOD indicates the status of OUT+ and OUT– voltage levels.

## 7 Application and Implementation

### Note

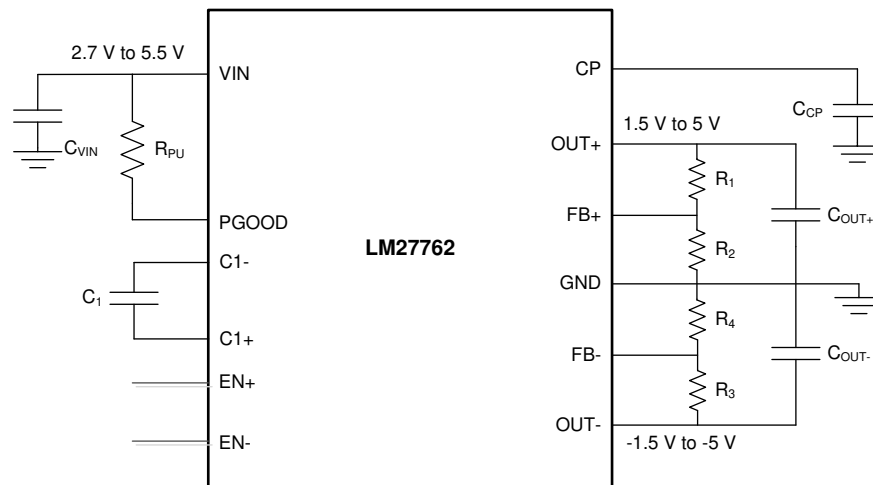
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 7.1 Application Information

The LM27762 input voltage range is from 2.7 V to 5.5 V. The positive LDO provides a positive voltage configurable with external gain setting resistors  $R_1$ ,  $R_2$ . The low-noise charge-pump voltage converter inverts the input voltage  $V$  to a negative output voltage. Charge pump is followed by the negative LDO which regulates a negative output voltage configurable with external gain setting resistors  $R_3$ ,  $R_4$ . Output voltage range is  $\pm 1.5$  V to  $\pm 5$  V. When selecting input ( $V_{IN}$ ) and output ( $OUT+$ ,  $OUT-$ ) voltages ranges, headroom required by the charge pump and LDOs must be considered. Charge-pump minimum headroom can be estimated based on the maximum load current and charge pump output resistance.

The device uses five low-cost capacitors to provide up to 250 mA of output current. The LM27762 operates at a 2-MHz oscillator frequency to reduce charge-pump output resistance and voltage ripple under heavy loads. When using the optional open-drain PGOOD feature, connect a 10-k $\Omega$  pullup resistor ( $R_{PU}$ ) to  $V_{IN}$ . Connect pin to ground if PGOOD is not used.

### 7.2 Typical Application



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**Figure 7-1. LM27762 Typical Application**

### 7.2.1 Design Requirements

The following example describes powering an amplifier driving high impedance headphones. Input voltage is from a smart-phone battery. Amplifier is driving 2-V<sub>RMS</sub> to 600-Ω stereo headphones.

**Table 7-1. Application Example Design Parameters**

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	3.3 V to 4.2 V
Output voltage	±3 V
Output current	10 mA (LM27762 capability 250 mA maximum)
C <sub>VIN</sub> , C <sub>OUT+</sub> , C <sub>OUT-</sub>	2.2 μF
C <sub>CP</sub>	4.7 μF
R <sub>PU</sub>	10 kΩ (optional, connect PGOOD pin to ground if feature is not used)

### 7.2.2 Detailed Design Procedure

#### 7.2.2.1 Positive Low-Dropout Linear Regulator and OUT+ Voltage Setting

LM27762 features a low-dropout, linear positive voltage regulator (LDO). The LDO output is rated for a current of 250 mA. This LDO allows the device to provide a very low noise output, low output voltage ripple, high PSRR, and low line or load transient response.

The positive output voltage of the LM27762 is externally configurable. The value of R<sub>1</sub> and R<sub>2</sub> determines the output voltage setting. The output voltage can be calculated using [Equation 1](#):

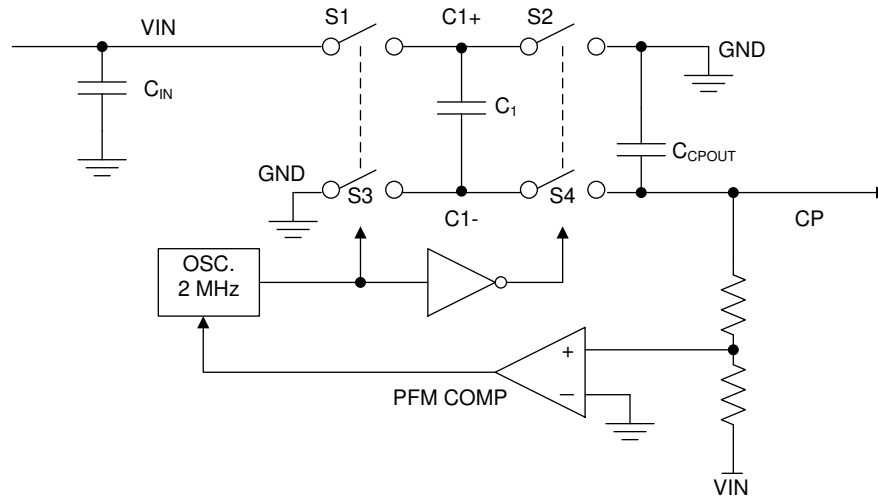
$$V_{OUT} = 1.2 \text{ V} \times (R_1 + R_2) / R_2 \quad (1)$$

The value for R<sub>2</sub> must be no less than 50 kΩ.

#### 7.2.2.2 Charge-Pump Voltage Inverter

The main application of the LM27762 is to generate a regulated negative supply voltage. The voltage inverter circuit uses only three external capacitors, and the LDO regulator circuit uses one additional output capacitor.

The voltage inverter portion of the LM27761 contains four large CMOS switches which are switched in sequence to invert the input supply voltage. Energy transfer and storage are provided by external capacitors. [Figure 7-2](#) shows the voltage switches S2 and S4 are open. In the second time interval, S1 and S3 are open; at the same time, S2 and S4 are closed, and C<sub>1</sub> is charging C<sub>CP</sub>. After a number of cycles, the voltage across C<sub>CP</sub> is pumped into V<sub>IN</sub>. Because the anode of C<sub>CP</sub> is connected to ground, the output at the cathode of C<sub>CP</sub> equals -(V<sub>IN</sub>) when there is no load current. When a load is added, the output voltage drop is determined by the parasitic resistance (R<sub>DSON</sub> of the MOSFET switches and the equivalent series resistance (ESR) of the capacitors) and the charge transfer loss between the capacitors.



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**Figure 7-2. Voltage Inverting Principle**

The output characteristic of this circuit can be approximated by an ideal voltage source in series with a resistance. The voltage source equals  $-(V_{IN})$ . The output resistance  $R_{OUT}$  is a function of the ON resistance of the internal MOSFET switches, the oscillator frequency, the capacitance, and the ESR of  $C_1$  and  $C_{CP}$ . Because the switching current charging and discharging  $C_1$  is approximately twice as the output current, the effect of the ESR of the pumping capacitor  $C_1$  is multiplied by four in the output resistance. The charge-pump output capacitor  $C_{CP}$  is charging and discharging at a current approximately equal to the output current; therefore, its ESR only counts once in the output resistance. A good approximation of charge-pump  $R_{OUT}$  is shown in Equation 2:

$$R_{OUT} = (2 \times R_{SW}) + [1 / (f_{SW} \times C_1)] + (4 \times ESR_{C1}) + ESR_{CCP} \quad (2)$$

where

- $R_{SW}$  is the sum of the ON resistance of the internal MOSFET switches shown in Figure 7-2.

High capacitance and low-ESR ceramic capacitors reduce the output resistance.

### 7.2.2.3 Negative Low-Dropout Linear Regulator and OUT– Voltage Setting

At the output of the inverting charge-pump the LM27762 features a low-dropout, linear negative voltage regulator (LDO). The LDO output is rated for a current of 250 mA. This negative LDO allows the device to provide a very low noise output, low output voltage ripple, high PSRR, and low line or load transient response.

The negative output voltage of the LM27762 is externally configurable. The value of  $R_3$  and  $R_4$  determines the output voltage setting. The output voltage can be calculated using Equation 1:

$$V_{OUT} = -1.22 \text{ V} \times (R_3 + R_4) / R_4 \quad (3)$$

The value for  $R_4$  must be no less than 50 k $\Omega$ .

### 7.2.2.4 External Capacitor Selection

The LM27762 requires 5 external capacitors for proper operation. Surface-mount multi-layer ceramic capacitors are recommended. These capacitors are small, inexpensive, and have very low ESR ( $\leq 15 \text{ m}\Omega$  typical). Tantalum capacitors, OS-CON capacitors, and aluminum electrolytic capacitors generally are not recommended for use with the LM27762 due to the high ESR compared to ceramic capacitors.

For most applications, ceramic capacitors with an X7R or X5R temperature characteristic are preferable for use with the LM27762. These capacitors have tight capacitance tolerances (as good as  $\pm 10\%$ ) and hold the value over temperature (X7R:  $\pm 15\%$  over  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ; X5R  $\pm 15\%$  over  $-55^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ).

Using capacitors with a Y5V or Z5U temperature characteristic is generally not recommended for the LM27762. These capacitors typically have wide capacitance tolerance (80%, ...20%) and vary significantly over temperature (Y5V: 22%,  $-82\%$  over  $-30^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  range; Z5U: 22%,  $-56\%$  over  $10^{\circ}\text{C}$  to  $85^{\circ}\text{C}$  range). Under some conditions a 1- $\mu\text{F}$ -rated Y5V or Z5U capacitor can have a capacitance as low as 0.1  $\mu\text{F}$ . Such detrimental deviation is likely to cause Y5V and Z5U capacitors to fail to meet the minimum capacitance requirements of the LM27762.

Net capacitance of a ceramic capacitor decreases with increased DC bias. This degradation can result in lower-than-expected capacitance on the input and/or output, resulting in higher ripple voltages and currents. Using capacitors at DC bias voltages significantly below the capacitor voltage rating usually minimizes DC bias effects. Consult capacitor manufacturers for information on capacitor DC bias characteristics.

Capacitance characteristics can vary quite dramatically with different application conditions, capacitor types, and capacitor manufacturers. TI strongly recommends that the LM27762 circuit be evaluated thoroughly early in the design-in process with the mass-production capacitor of choice. This action helps make sure that any such variability in capacitance does not negatively impact circuit performance.

#### **7.2.2.4.1 Charge-Pump Output Capacitor**

In typical applications, Texas Instruments recommends a 4.7- $\mu\text{F}$  low-ESR ceramic charge-pump output capacitor ( $C_{CP}$ ). Different output capacitance values can be used to reduce charge pump ripple, shrink the solution size, and/or cut the cost of the solution. However, changing the output capacitor may also require changing the flying capacitor or input capacitor to maintain good overall circuit performance.

In higher-current applications, a 10- $\mu\text{F}$ , 10-V low-ESR ceramic output capacitor is recommended. If a small output capacitor is used, the output ripple can become large during the transition between PFM mode and constant switching. To prevent toggling, a 2- $\mu\text{F}$  capacitance is recommended. For example, 10- $\mu\text{F}$ , 10-V output capacitor in a 0402 case size typically has only 2- $\mu\text{F}$  capacitance when biased to 5 V.

#### **7.2.2.4.2 Input Capacitor**

The input capacitor ( $C_2$ ) is a reservoir of charge that aids in a quick transfer of charge from the supply to the flying capacitors during the charge phase of operation. The input capacitor helps to keep the input voltage from drooping at the start of the charge phase when the flying capacitors are connected to the input. The input capacitor also filters noise on the input pin, keeping this noise out of the sensitive internal analog circuitry that is biased off the input line.

Input capacitance has a dominant and first-order effect on the input ripple magnitude. Increasing (decreasing) the input capacitance results in a proportional decrease (increase) in input voltage ripple. Input voltage, output current, and flying capacitance also affects input ripple levels to some degree.

In typical applications, a 4.7- $\mu\text{F}$  low-ESR ceramic capacitor is recommended on the input. When operating near the maximum load of 250 mA, after taking into the DC bias derating, a minimum recommended input capacitance is 2  $\mu\text{F}$  or larger. Different input capacitance values can be used to reduce ripple, shrink the design size, and cut the cost of the design.

#### **7.2.2.4.3 Flying Capacitor**

The flying capacitor ( $C_1$ ) transfers charge from the input to the output. Flying capacitance can impact both output current capability and ripple magnitudes. If flying capacitance is too small, the LM27762 can not be able to regulate the output voltage when load currents are high. If the flying capacitance is too large, the flying capacitor can overwhelm the input and charge pump output capacitors, resulting in increased input and output ripple.

In typical high-current applications, 0.47- $\mu\text{F}$  or 1- $\mu\text{F}$  10-V low-ESR ceramic capacitors are recommended for the flying capacitors. Polarized capacitors (tantalum, aluminum, electrolytic, and so forth) must not be used for the flying capacitor, as polarized capacitors can become reverse-biased during LM27762 operation.

#### 7.2.2.4.4 LDO Output Capacitor

The LDO output capacitor (COUT+, COUT-) value and the ESR affect stability, output ripple, output noise, PSRR and transient response. The LM27762 only requires the use of a 2.2-μF ceramic output capacitor for stable operation. For typical applications, a 2.2-μF ceramic output capacitor located close to the output is sufficient.

#### 7.2.2.5 Power Dissipation

The allowed power dissipation for any package is a measure of the ability of the device to pass heat from the junctions of the device to the heatsink and the ambient environment. Thus, the power dissipation is dependent on the ambient temperature and the thermal resistance across the various interfaces between the die junction and ambient air.

The maximum allowable power dissipation can be calculated by [Equation 4](#):

$$P_{D-MAX} = (T_{J-MAX} - T_A) / R_{\theta JA} \quad (4)$$

The actual power being dissipated in the device can be represented by [Equation 5](#):

$$P_D = P_{IN} - P_{OUT} = V_{IN} \times (-I_{OUT-} + I_{OUT+} + I_Q) - (V_{OUT+} \times I_{OUT+} + V_{OUT-} \times I_{OUT-}) \quad (5)$$

[Equation 4](#) and [Equation 5](#) establish the relationship between the maximum power dissipation allowed due to thermal consideration, the voltage drop across the device, and the continuous current capability of the device. These equations must be used to determine the optimum operating conditions for the device in a given application.

In lower power dissipation applications the maximum ambient temperature ( $T_{A-MAX}$ ) can be increased. In higher power dissipation applications the maximum ambient temperature ( $T_{A-MAX}$ ) can have to be derated.  $T_{A-MAX}$  can be calculated using [Equation 6](#):

$$T_{A-MAX} = T_{J-MAX-OP} - (R_{\theta JA} \times P_{D-MAX}) \quad (6)$$

where

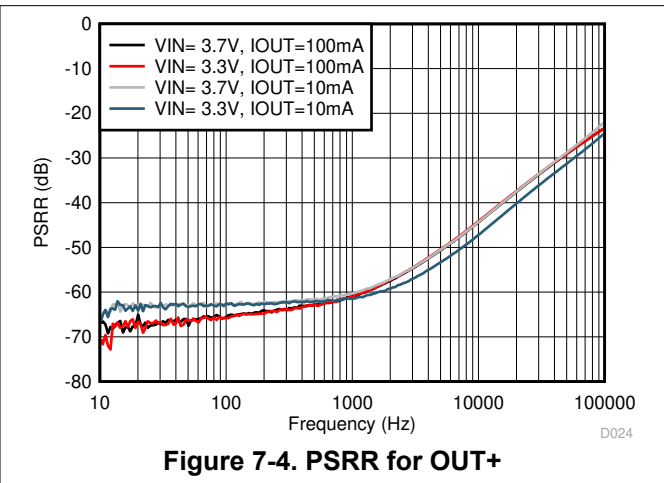
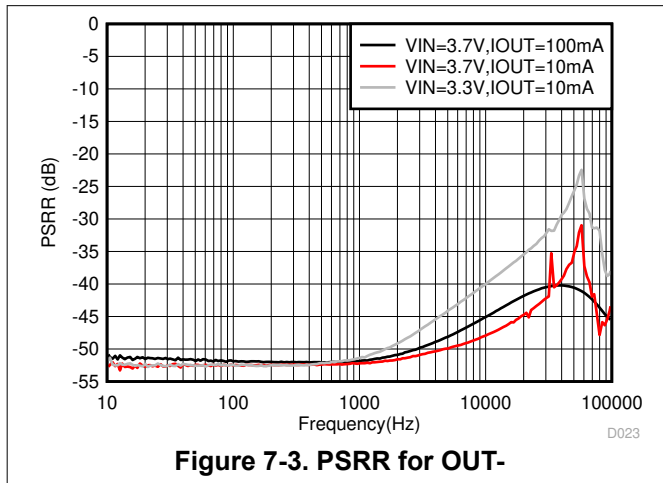
- $T_{J-MAX-OP}$  = maximum operating junction temperature (125°C)
- $P_{D-MAX}$  = the maximum allowable power dissipation
- $R_{\theta JA}$  = junction-to-ambient thermal resistance of the package

Alternately, if  $T_{A-MAX}$  cannot be derated, the power dissipation value must be reduced. This can be accomplished by reducing the input voltage as long as the minimum  $V_{IN}$  is not violated, or by reducing the output current, or some combination of the two.



### 7.2.3 Application Curves

Refer also to [Section 5.6](#).



### 7.3 Power Supply Recommendations

The LM27762 is designed to operate from an input voltage supply range between 2.7 V and 5.5 V. This input supply must be well regulated and capable of supplying the required input current. If the input supply is located far from the LM27762, additional bulk capacitance can be required in addition to the ceramic bypass capacitors.

### 7.4 Layout

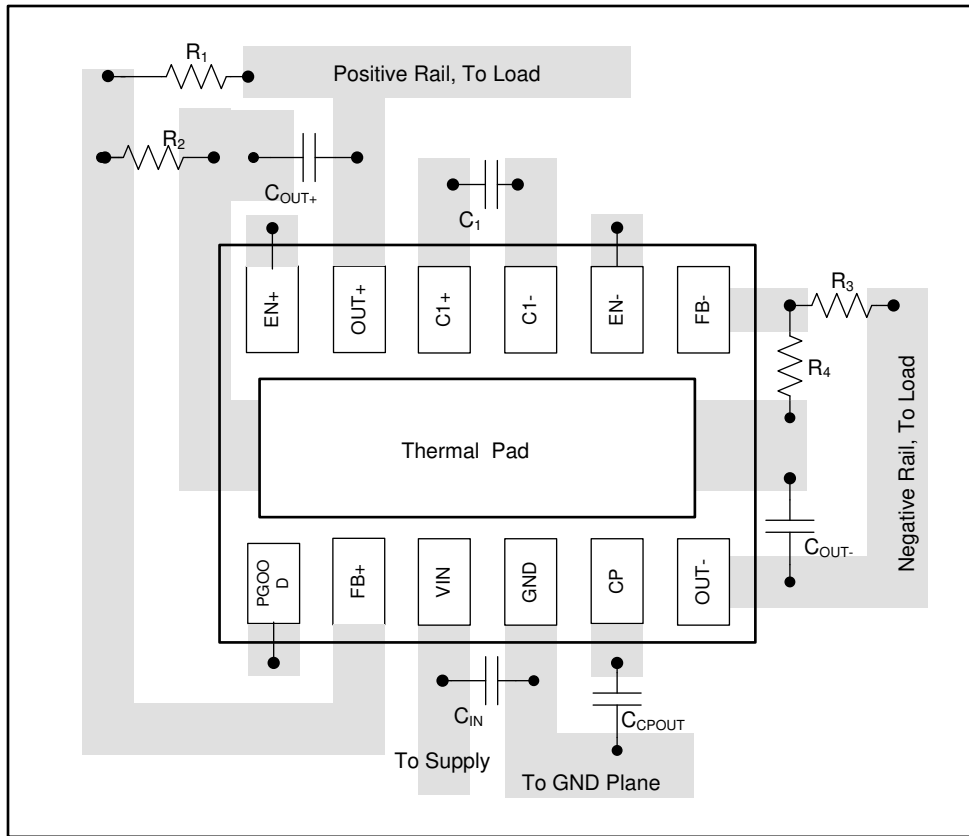
#### 7.4.1 Layout Guidelines

The high switching frequency and large switching currents of the LM27762 make the choice of layout important. Use the following steps as a reference to make sure the device is stable and maintains proper LED current regulation across the intended operating voltage and current range:

- Place  $C_{IN}$  on the top layer (same layer as the LM27762) and as close as possible to the device. Connecting the input capacitor through short, wide traces to both the VIN and GND pins reduces the inductive voltage spikes that occur during switching, which can corrupt the VIN line.
- Place  $C_{CPOUT}$  on the top layer (same layer as the LM27762) and as close as possible to the VOUT and GND pins. The returns for both  $C_{IN}$  and  $C_{CPOUT}$  must come together at one point, as close as possible to the GND pin. Connecting  $C_{CPOUT}$  through short, wide traces reduces the series inductance on the VCPOUT and GND pins that can corrupt the VCPOUT and GND lines and cause excessive noise in the device and surrounding circuitry.
- Place  $C_1$  on top layer (same layer as the LM27762) and as close as possible to the device. Connect the flying capacitor through short, wide traces to both the C1+ and C1– pins.
- Place  $C_{OUT+}$ ,  $C_{OUT-}$  on the top layer (same layer as the LM27762) and as close to the respective OUT pin as possible. For best performance the ground connection for  $C_{OUT}$  must connect back to the GND connection at the thermal pad of the device.
- Place  $R_1$  to  $R_4$  on the top layer (same layer as LM27762) and as close as possible to the respective FB pin. For best performance the ground connection of  $R_2$ ,  $R_4$  must connect back to the GND connection at the thermal pad of the device.

Connections using long trace lengths, narrow trace widths, or connections through vias must be avoided. These add parasitic inductance and resistance that results in inferior performance, especially during transient conditions.

**7.4.2 Layout Example**



**Figure 7-5. LM27762 Layout Example (Note: Pullup resistor for PGOOD not shown in example.)**

## 8 Device and Documentation Support

### 8.1 Documentation Support

#### 8.1.1 Related Documentation

[Using the LM27762EVM Evaluation Module user's guide](#)

### 8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 8.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 8.4 Trademarks

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### 8.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 8.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision B (February 2017) to Revision C (October 2025)</b>	<b>Page</b>
• Deleted all WEBENCH information from the data sheet.....	1
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1

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<b>Changes from Revision A (September 2016) to Revision B (February 2017)</b>	<b>Page</b>
• Added ulinks for WEBENCH .....	1

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## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">LM27762DSSR</a>	Active	Production	WSON (DSS)   12	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	L27762
LM27762DSSR.A	Active	Production	WSON (DSS)   12	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L27762
LM27762DSSRG4	Active	Production	WSON (DSS)   12	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L27762
LM27762DSSRG4.A	Active	Production	WSON (DSS)   12	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L27762
<a href="#">LM27762DSST</a>	Active	Production	WSON (DSS)   12	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	L27762
LM27762DSST.A	Active	Production	WSON (DSS)   12	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L27762

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM27762DSSR	WSON	DSS	12	3000	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1
LM27762DSSRG4	WSON	DSS	12	3000	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1
LM27762DSST	WSON	DSS	12	250	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1

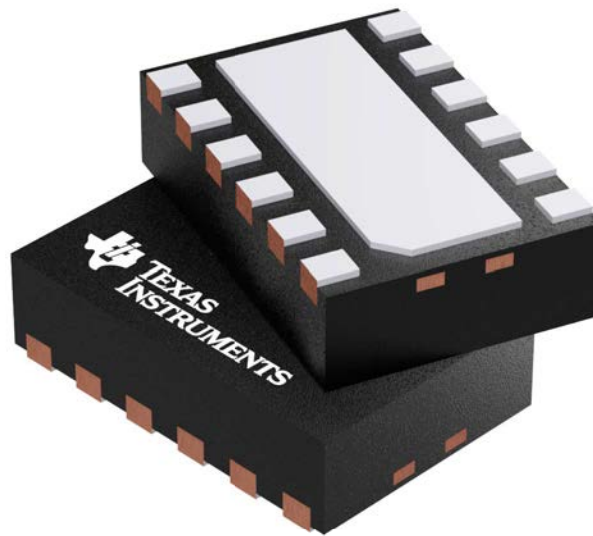


## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM27762DSSR	WSON	DSS	12	3000	210.0	185.0	35.0
LM27762DSSRG4	WSON	DSS	12	3000	210.0	185.0	35.0
LM27762DSST	WSON	DSS	12	250	210.0	185.0	35.0



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

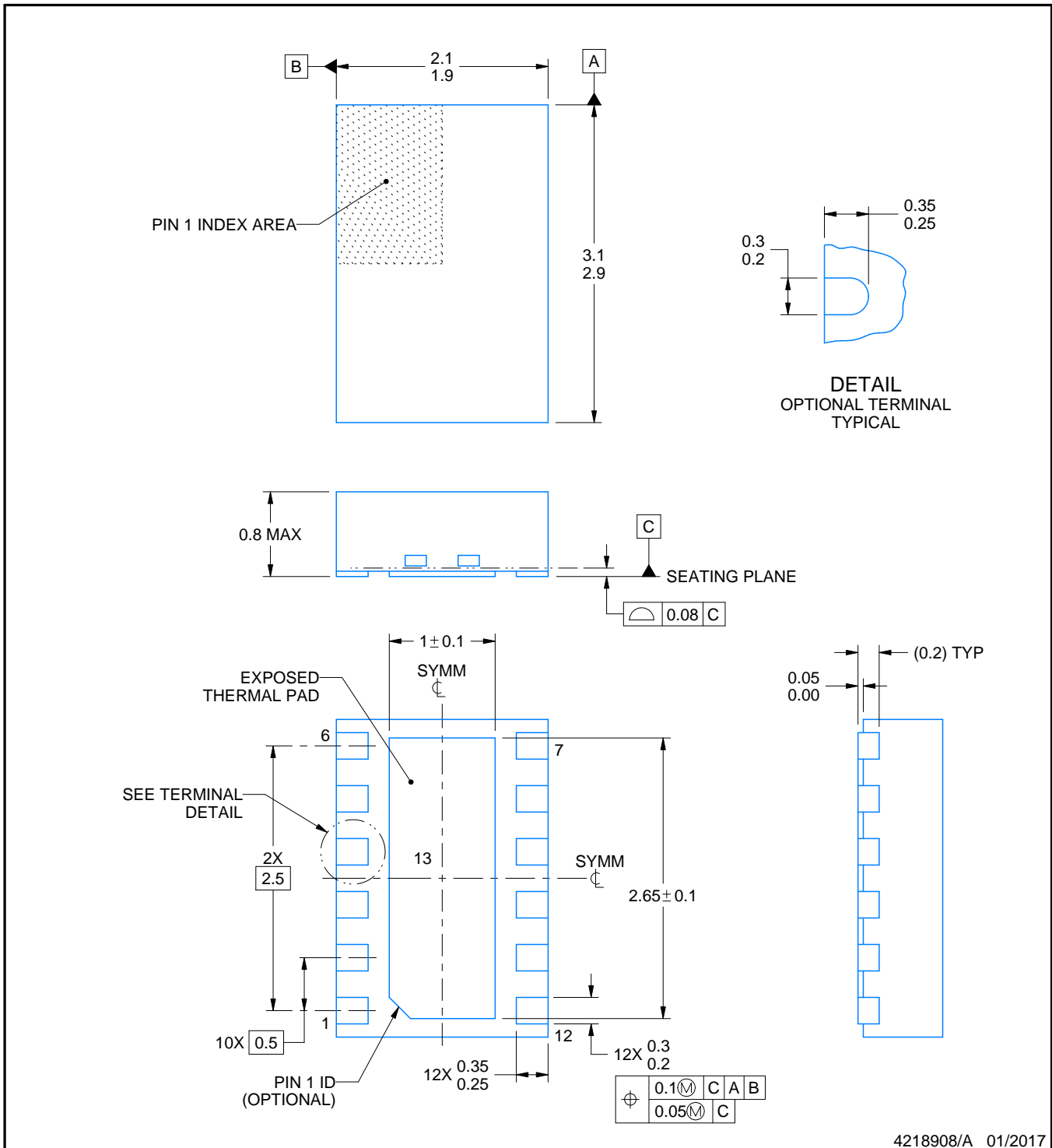
# DSS0012B



# PACKAGE OUTLINE

## WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



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### NOTES:

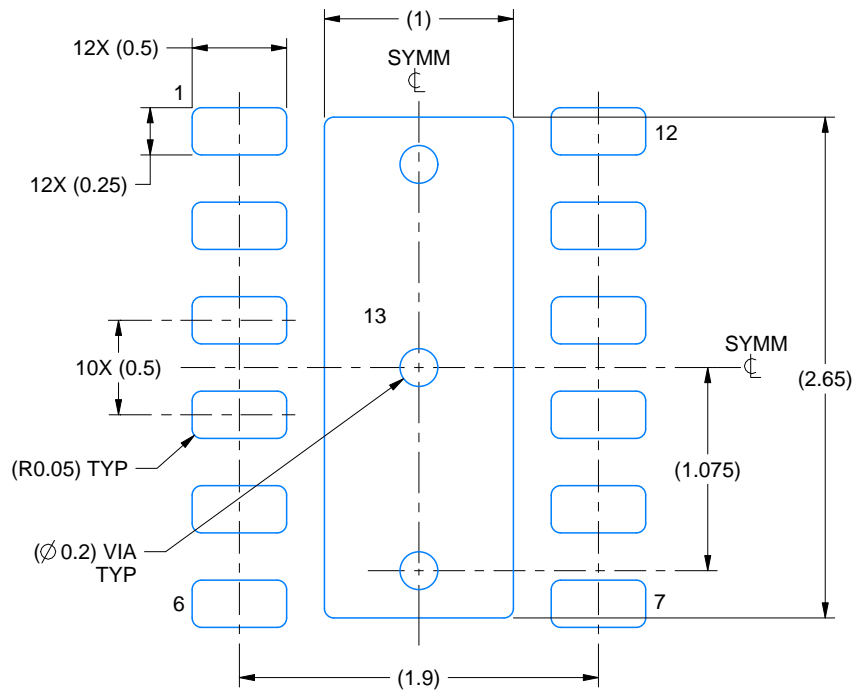
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

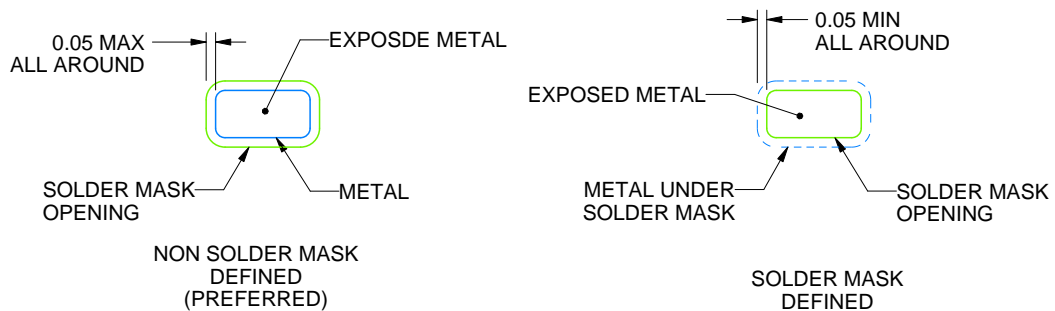
DSS0012B

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:25X



SOLDER MASK DETAILS

4218908/A 01/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



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