LM26400Y Dual 2-A, 500-kHz Wide Input Range Buck Regulator

1 Features

- Input Voltage Range of 3 V to 20 V
- Dual 2-A Output
- Output Voltage Down to 0.6 V
- Internal Compensation
- 500-kHz PWM Frequency
- Separate Enable Pins
- Separate Soft-Start Pins
- Frequency Foldback Protection
- 175-mΩ NMOS Switch
- Integrated Bootstrap Diodes
- Overcurrent Protection
- HTSSOP and WSON Packages
- Thermal Shutdown

2 Applications

- DTV-LCD
- Set-Top Boxes
- XDSL
- Automotive
- Computing Peripherals
- Industrial Controls
- Points-of-Load

3 Description

The LM26400Y device is a monolithic, two-output fixed-frequency PWM step-down DC-DC regulator, in a 16-pin WSON or thermally-enhanced HTSSOP package. With a minimum number of external components and internal loop compensation, the LM26400Y is easy to use.

The ability to drive 2-A loads with an internal 175-mΩ NMOS switch using state-of-the-art 0.5-µm BiCMOS technology results in a high-power density design. The world class control circuitry allows for an ON-time as low as 40 ns, thus supporting high-frequency conversion over the entire input range of 3 V to 20 V and down to an output voltage of only 0.6 V. The LM26400Y utilizes peak current-mode control and internal compensation to provide high-performance regulation over a wide range of line and load conditions. Switching frequency is internally set to 500 kHz, optimal for a broad range of applications in terms of size versus thermal tradeoffs.

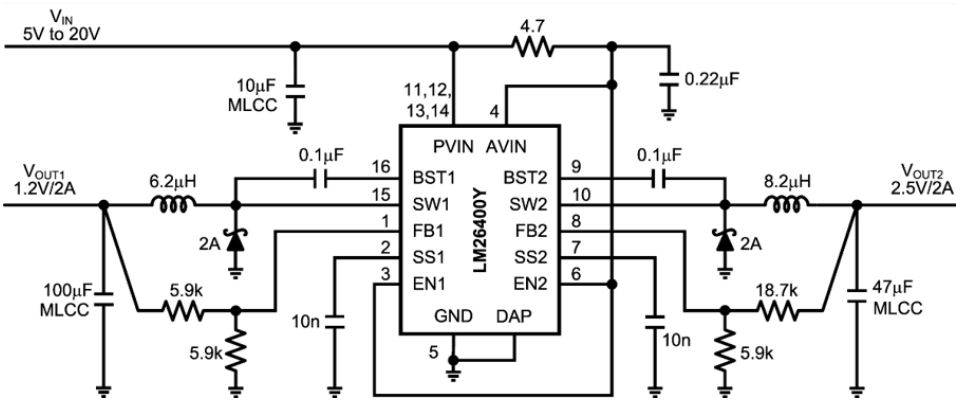
Given a nonsynchronous architecture, efficiencies above 90% are easy to achieve. External shutdown is included, enabling separate turnon and turnoff of the two channels. Additional features include programmable soft-start circuitry to reduce inrush current, pulse-by-pulse current limit and frequency foldback, integrated bootstrap structure, and thermal shutdown.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM26400Y	WSON (16)	5.00 mm × 5.00 mm
	HTSSOP (16)	4.40 mm × 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (April 2013) to Revision D — **Page**

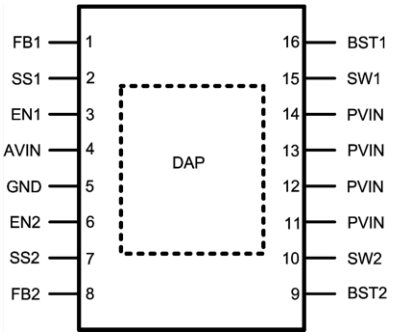
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1

Changes from Revision B (April 2013) to Revision C — **Page**

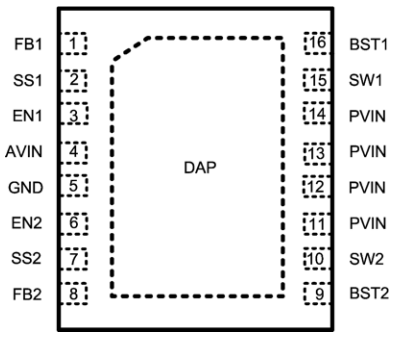
- Changed layout of National Data Sheet to TI format ... 18

5 Pin Configuration and Functions

PWP Package
16-Pin HTSSOP With PowerPAD IC Package
Top View



NHQ Package
16-Pin WSON
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
AVIN	4	PWR	Input supply for generating the internal bias used by the entire IC and for generating the internal bootstrap bias. Needs to be locally bypassed.
BST1	16	O	Supply rail for the gate drive of Channel 1's NMOS switch. A bootstrap capacitor should be placed between the BST1 and SW1 pins.
BST2	9	O	Supply rail for the gate drive of Channel 2's NMOS switch. A bootstrap capacitor should be placed between the BST2 and SW2 pins.
EN1	3	I	Enable control input for Channel 1. Logic high enables operation. Do not allow this pin to float or be greater than V_{IN} + 0.3 V.
EN2	6	I	Enable control input for Channel 2. Logic high enables operation. Do not allow this pin to float or be greater than V_{IN} + 0.3 V.
FB1	1	I	Feedback pin of Channel 1. Connect FB1 to an external voltage divider to set the output voltage of Channel 1.
FB2	8	I	Feedback pin of Channel 2. Connect FB2 to an external voltage divider to set the output voltage of Channel 2.
GND	5	PWR	Signal and Power ground pin. Kelvin connect the lower resistor of the feedback voltage divider to this pin for good load regulation.
PVIN	11, 12, 13,14	PWR	Input voltage of the power supply. Directly connected to the drain of the internal NMOS switch. Tie these pins together and connect to a local bypass capacitor.
SS1	2	I	Soft start pin of Channel 1. Connect a capacitor between this pin and ground to program the start up speed.
SS2	7	I	Soft start pin of Channel 2. Connect a capacitor between this pin and ground to program the start up speed.
SW2	10	O	Switch node of Channel 2. Connects to the inductor, catch diode, and bootstrap capacitor.
SW1	15	O	Switch node of Channel 1. Connects to the inductor, catch diode, and bootstrap capacitor.
Die Attach Pad	DAP	—	Must be connected to system ground for low thermal impedance and low grounding inductance.

6 Specifications

6.1 Absolute Maximum Ratings

See (1)(2)

	MIN	MAX	UNIT
AVIN, PVIN	–0.5	22	V
SWx Voltage	–0.5	22	V
BSTx Voltage	–0.5	26	V
BSTx to SW Voltage	–0.5	6	V
FBx Voltage	–0.5	3	V
ENx Voltage(3)	–0.5	22	V
SSx Voltage	–0.5	3	V
Junction Temperature		150	°C
Storage Temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) EN1 and EN2 pins should never be higher than V_{IN} + 0.3 V.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)(2)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) The human body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin. Test method is per JESD-22-A114.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
V_{IN}	3		20	V
Junction Temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		LM26400Y		UNIT
		PWP (HTSSOP)	NHQ (WSON)	
		16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance(2)(3)	39.4	27.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	24.5	27.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	18	9.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.7	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	17.8	10.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.1	2.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) Value is highly board-dependent. For comparison of package thermal performance only. Not recommended for prediction of junction temperature in real applications. See *Thermal Considerations* for more information.
(3) A standard board refers to a four-layer PCB with the size 4.5”x3”x0.063”. Top and bottom copper is 2 oz. Internal plane copper is 1 oz. For details refer to JESD51-7 standard. Mount package on a standard board and test per JESD51-7 standard.

6.5 Electrical Characteristics

Unless otherwise stated, the following conditions apply: AVIN = PVIN = V_{IN} = 5 V. Limits are for T_J = 25°C. Minimum and maximum limits are ensured through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{FB}	Voltages at FB1 and FB2 Pins	Feedback Loop Closed	T_J = 25°C		0.6		V
			T_J = 0°C to 85°C	0.591		0.611	
		Feedback Loop V Closed	T_J = 25°C		0.6		
			T_J = –40°C to 125°C	0.585		0.617	
ΔV_{FB_Line}	Line Regulation of FB1 and FB2 Voltages, Expressed as PPM Change Per Volt of V_{IN} Variation	V_{IN} = 3 V to 20 V			66		ppm/V
I_{FB}	Current in FB1 and FB2 Pins	V_{FB} = 0.6 V	T_J = 25°C		0.4		nA
			T_J = –40°C to 125°C			250	
V_{UVLO}	Undervoltage Lockout Threshold	V_{IN} Rising From 0 V	T_J = 25°C		2.7		V
			T_J = –40°C to 125°C			2.9	
		V_{IN} Falling From 3.3 V	T_J = 25°C		2.3		
			T_J = –40°C to 125°C	2			
V_{UVLO_HYS}	UVLO Hysteresis	T_J = 25°C			0.36		V
		T_J = –40°C to 125°C		0.2		0.55	
F_{SW}	Switching Frequency	T_J = 25°C			0.52		MHz
		T_J = –40°C to 125°C		0.39		0.65	
D_{MAX}	Maximum Duty Cycle	T_J = 25°C			96%		
		T_J = –40°C to 125°C		90%			
D_{MIN}	Minimum Duty Cycle				2%		
$R_{DS(ON)}$	ON-Resistance of Internal Power MOSFET	HTSSOP, 2-A Drain Current	T_J = 25°C		175		mΩ
			T_J = –40°C to 125°C			320	
		WSON, 2-A Drain Current	T_J = 25°C		194		
			T_J = –40°C to 125°C			350	
I_{CL}	Peak Current Limit of Internal MOSFET	T_J = 25°C			3		A
		T_J = –40°C to 125°C		2.5		4.5	
I_{SD}	Shutdown Current of AVIN Pin	EN1 = EN2 = 0 V			2		nA
I_Q	Quiescent Current of AVIN Pin (both channels are enabled but not switching)	EN1 = EN2 = 5 V, FB1 = FB2 = 0.7 V, T_J = –40°C to 125°C				4	mA
V_{EN_IH}	Input Logic High of EN1 and EN2 Pins	T_J = –40°C to 125°C		2.5			V
V_{EN_IL}	Input Logic Low of EN1 and EN2 Pins	T_J = –40°C to 125°C				0.4	V
I_{EN}	EN1 and EN2 Currents (sink or source)				5		nA
I_{SW_LEAK}	Switch Leakage Current Measured at SW1 and SW2 Pins	EN1 = EN2 = SWx = 0			1		µA
ΔΦ	Phase Shift Between SW1 and SW2 Rising Edges	Feedback Loop Closed. Continuous Conduction Mode.		170	180	19	deg
I_{SS}	SSx Pin Current	T_J = 25°C			16		µA
		T_J = –40°C to 125°C		11		21	
ΔI_{SS}	Difference Between SS1 and SS2 Currents	T_J = –40°C to 125°C				3	µA
V_{FB_F}	FB1 and FB2 Frequency Foldback Threshold				0.35		V
T_{SD}	Thermal Shutdown Threshold	Junction temperature rises.			165		°C
T_{SD_HYS}	Thermal Shutdown Hysteresis	Junction temperature falls from above T_{SD}.			15		°C

6.6 Typical Characteristics

Unless otherwise specified or thermal-shutdown related, T_A = 25°C for efficiency curves, loop gain plots and waveforms, and T_J = 25°C for all others.

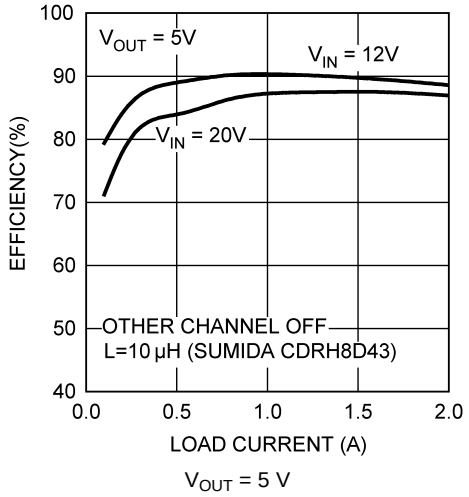


Figure 1. Efficiency

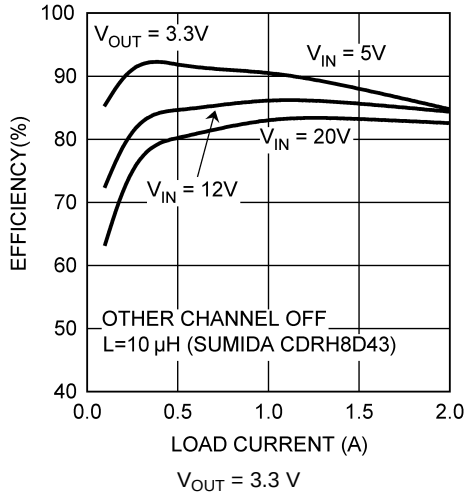


Figure 2. Efficiency

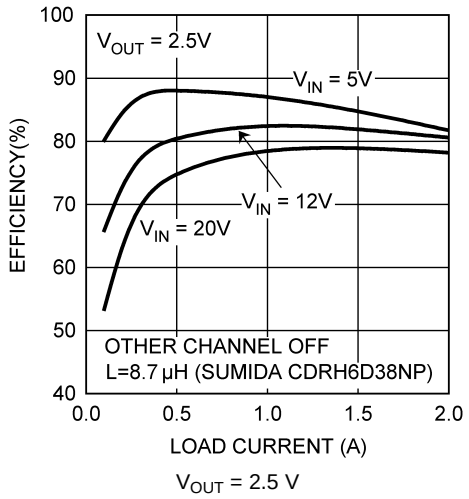


Figure 3. Efficiency

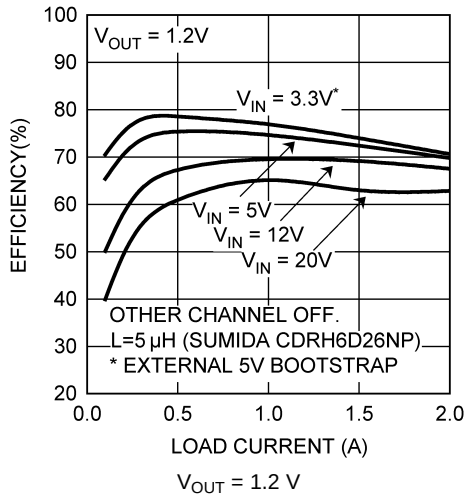


Figure 4. Efficiency

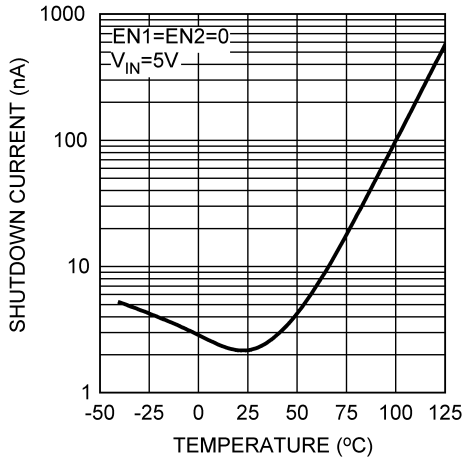


Figure 5. AVIN Shutdown Current vs Temperature

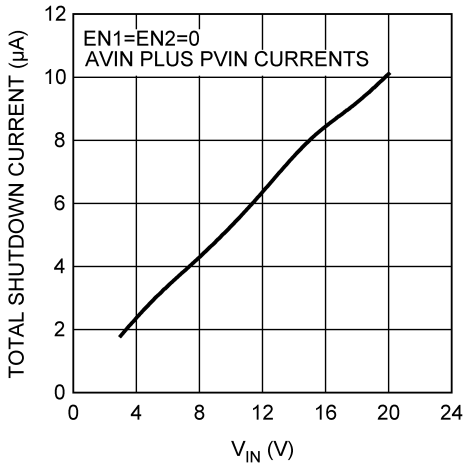


Figure 6. V_{IN} Shutdown Current vs V_{IN}

Typical Characteristics (continued)

Unless otherwise specified or thermal-shutdown related, T_A = 25°C for efficiency curves, loop gain plots and waveforms, and T_J = 25°C for all others.

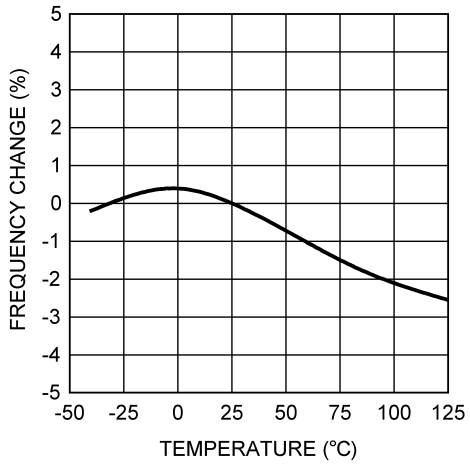


Figure 7. Switching Frequency vs Temperature

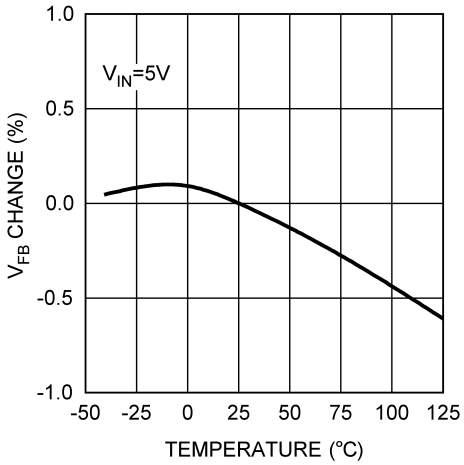


Figure 8. Feedback Voltage vs Temperature

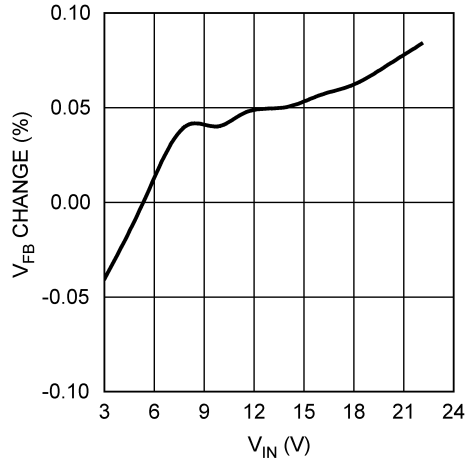


Figure 9. Feedback Voltage vs V_{IN}

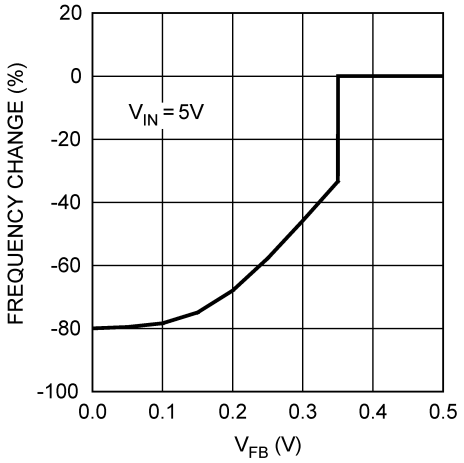


Figure 10. Frequency Foldback

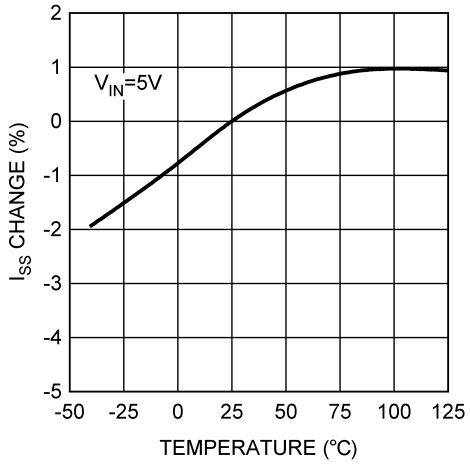


Figure 11. SS-Pin Current vs Temperature

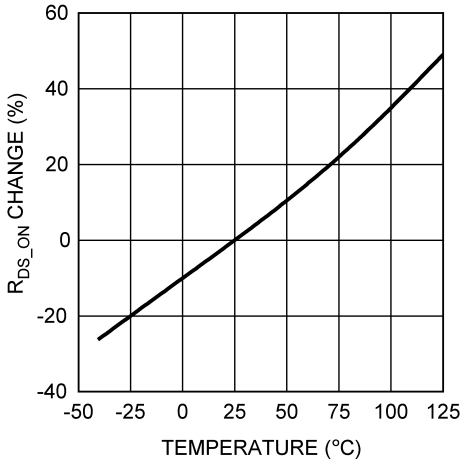


Figure 12. FET R_{DS_ON} vs Temperature

Typical Characteristics (continued)

Unless otherwise specified or thermal-shutdown related, T_A = 25°C for efficiency curves, loop gain plots and waveforms, and T_J = 25°C for all others.

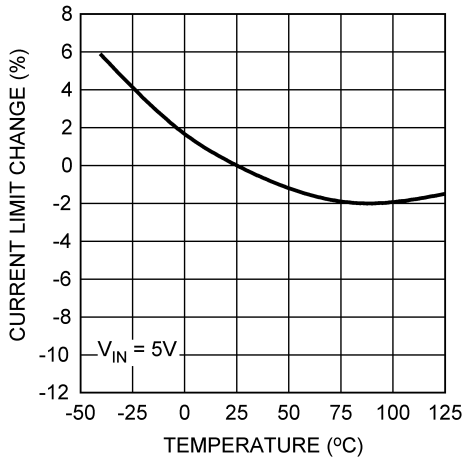


Figure 13. Switch Current Limit vs Temperature

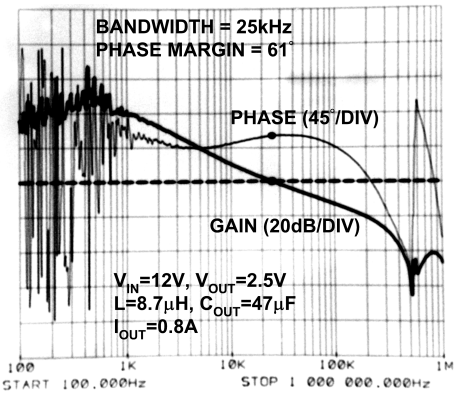


Figure 14. Loop Gain, CCM

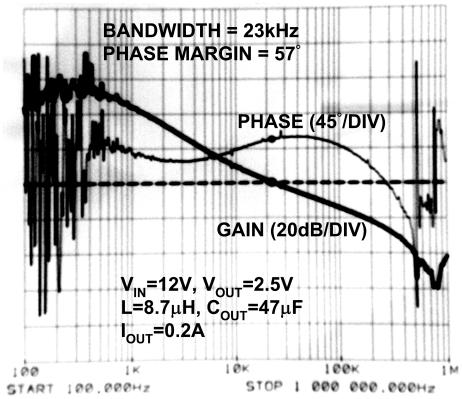


Figure 15. Loop Gain, DCM

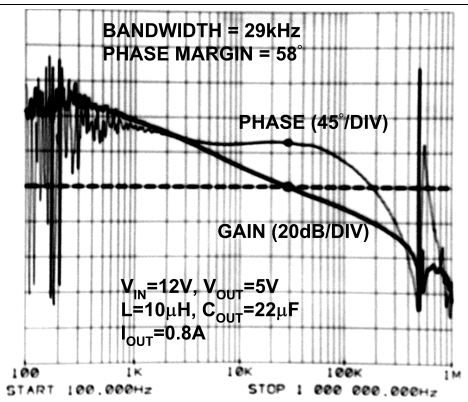


Figure 16. Loop Gain, CCM

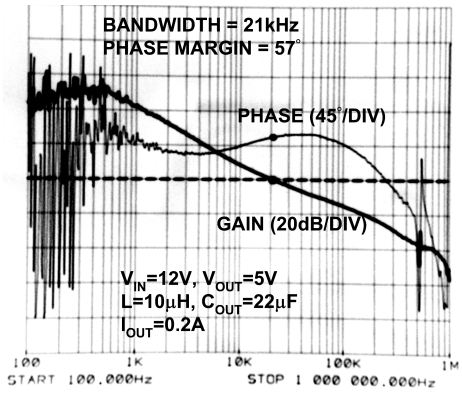


Figure 17. Loop Gain, DCM

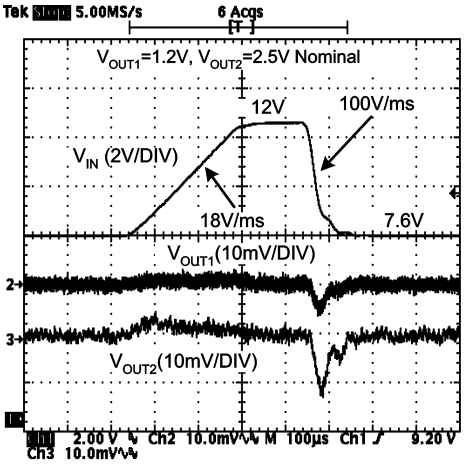


Figure 18. Line Transient Response

Typical Characteristics (continued)

Unless otherwise specified or thermal-shutdown related, T_A = 25°C for efficiency curves, loop gain plots and waveforms, and T_J = 25°C for all others.

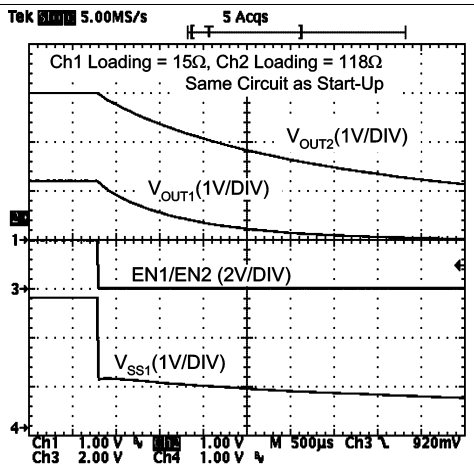


Figure 19. Shutdown

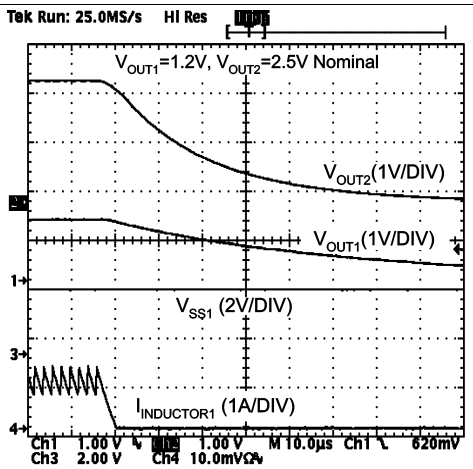


Figure 20. Thermal Shutdown

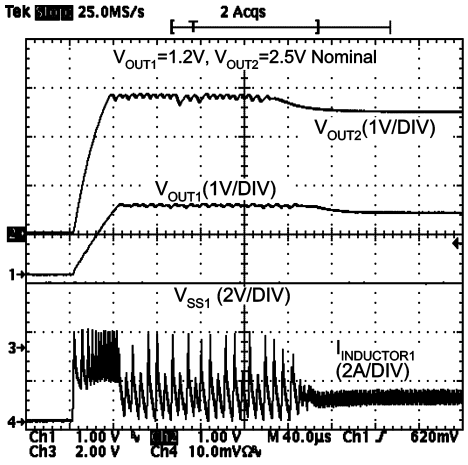


Figure 21. Recovery from Thermal Shutdown

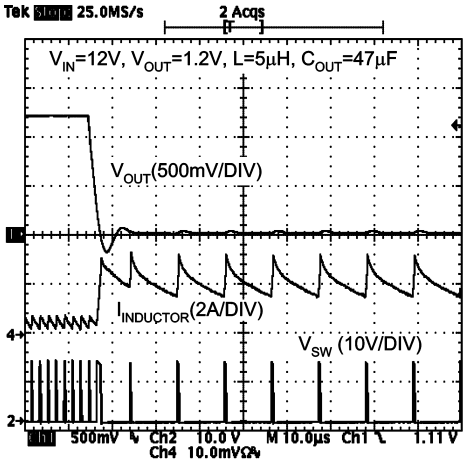


Figure 22. Short-Circuit Triggering

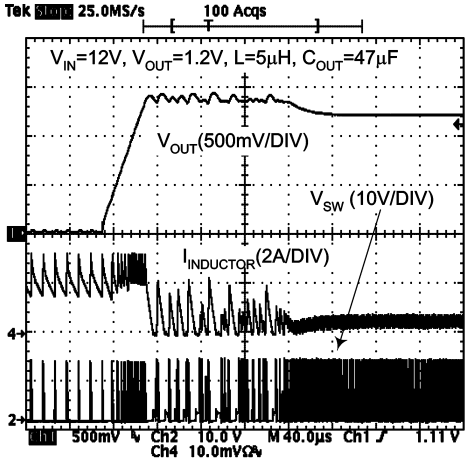


Figure 23. Short-Circuit Release

7 Detailed Description

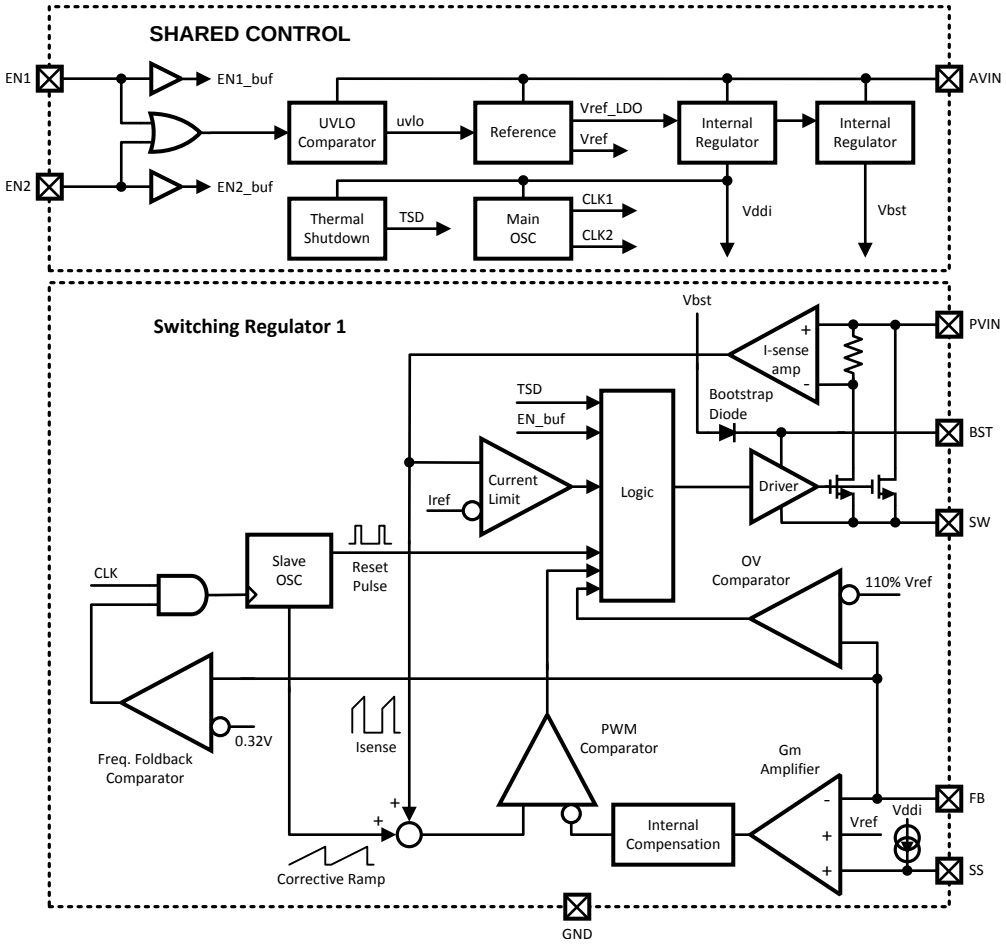
7.1 Overview

The LM26400Y device is a dual PWM peak-current mode buck regulator with two integrated power MOSFET switches. The part is designed to be easy to use. The two regulators are mostly identical and share the same input voltage and the same reference voltage (0.6 V). The two PWM clocks are of the same frequency but 180° out of phase. The two channels can have different soft-start ramp slopes and can be turned on and off independently.

Loop compensation is built in. The feedback loop design is optimized for ceramic output capacitors.

Since the power switches are built in, the achievable output current level also has to do with thermal environment of the specific application. The LM26400Y enters thermal shutdown when the junction temperature exceeds approximately 165°C.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Overcurrent Protection

The instantaneous switch current is limited to a typical of 3 Amperes. Any time the switch current reaches that value, the switch will be turned off immediately. This will result in a smaller duty cycle than normal, which will cause the output voltage to dip. The output voltage will continue drooping until the load draws a current that is equal to the peak-limited inductor current. As the output voltage droops, the FB pin voltage will also droop proportionally. When the FB voltage dips below 0.35 V or so, the PWM frequency will start to decrease. The lower the FB voltage the lower the PWM frequency. See Figure 10.

Feature Description (continued)

The frequency foldback helps two things. One is to prevent the switch current from running away as a result of the finite minimum ON-time (40 ns or so for the LM26400Y) and the small duty cycle caused by lowered output voltage due to the current limit. The other is it also helps reduce thermal stress both in the IC and the external diode.

The current limit threshold of the LM26400Y remains constant over all duty cycles.

One thing to pay attention to is that recovery from an overcurrent condition does not go through a soft-start process. This is because the reference voltage at the noninverting input of the error amplifier always sits at 0.6 V during the overcurrent protection. So if the overcurrent condition is suddenly removed, the regulator will bring the FB voltage back to 0.6 V as quickly as possible. This may cause an overshoot in the output voltage. Generally, the larger the inductor or the lower the output capacitance the more the overshoot, and vice versa. If the amount of such overshoot exceeds the allowed limit for a system, add a C_{FF} capacitor in parallel with the upper feedback resistor to eliminate the overshoot. See *Load Step Response* for more details on C_{FF}.

When one channel gets into overcurrent protection mode, the operation of the other channel will not be affected.

7.3.2 Loop Stability

To the first order approximation, the LM26400Y has a V_{FB}-to-Inductor Current transfer admittance (that is, ratio of inductor current to FB pin voltage, in frequency domain) close to the plot in Figure 24. The transfer admittance has a DC value of 104 dBS (dBS stands for decibel Siemens. The equivalent of 0 dBS is 1 Siemens.). There is a pole at 1 Hz and a zero at approximately 8 kHz. The plateau after the 8 kHz zero is about 27 dBS. There are also high frequency poles that are not shown in the figure. They include a double pole at 1.2 MHz or so, and another double pole at half the switching frequency. Depending on factors such as inductor ripple size and duty cycle, the double pole at half the switching frequency may become two separate poles near half the switching frequency.

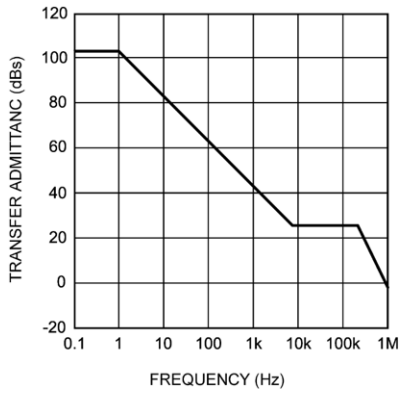


Figure 24. V_{FB}-to-Inductor Current Transfer Admittance

An easy strategy to build a stable loop with reasonable phase margin is to try to cross over from 20 kHz to 100 kHz, assuming the output capacitor is ceramic. When using pure ceramic capacitors at the output, simply use the following equation to find out the crossover frequency.

$$f_C = \frac{22S \times r}{6.28 \times C_{OUT}} \quad (1)$$

where

- 22S (22 Siemens) is the equivalent of the 27 dBS transfer admittance
- r is the ratio of 0.6 V to the output voltage

Use the same equation to find out the needed output capacitance for a given crossover frequency. Phase margin is typically between 50° and 60°. The above equation is only good for a crossover from 20 kHz to 100 kHz. A crossover frequency outside this range may result in lower phase margin and less accurate prediction by the above equation.

Example: V_{OUT} = 2.5 V, C_{OUT} = 36 µF, find out the crossover frequency.

Feature Description (continued)

Assume the crossover is from 20 kHz to 100 kHz. Then:

$$f_C = \frac{22S \times \frac{0.6V}{2.5V}}{6.28 \times 36\mu F} = 23\,kHz \quad (2)$$

The above analysis serves as a starting point. It is a good practice to always verify loop gain on bench.

7.3.3 Load Step Response

In general, the excursion in output voltage caused by a load step can be reduced by increasing the output capacitance. Besides that, increasing the small-signal loop bandwidth also helps. This can be achieved by adding a 27 nF or so capacitor (C_{FF}) in parallel with the upper feedback resistor (assuming the lower feedback resistor is 5.9 kΩ). See Figure 25 for an illustration.

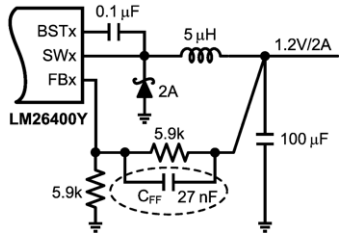


Figure 25. Adding a C_{FF} Capacitor

The responses to a load step from 0.2 A to 2 A with and without a C_{FF} are shown in Figure 26. The higher loop bandwidth as a result of C_{FF} reduces the total output excursion by about 80 mV.

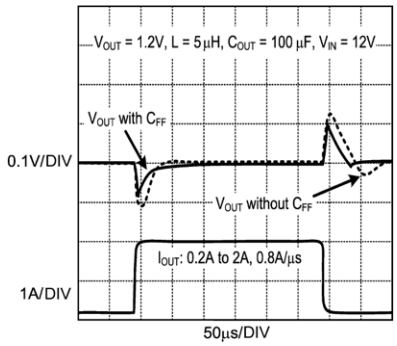


Figure 26. C_{FF} Improves Load Step Response

Use the following equation to calculate the new loop bandwidth:

$$f_C = \frac{22S}{6.28 \times C_{OUT}} \quad (3)$$

Again, the assumption is the crossover is from 20 kHz to 100 kHz.

In an extreme case where the load goes to less than 100 mA during a large load step, output voltage may exhibit extra undershoot. This usually happens when the load toggles high at the time V_{OUT} just ramps down to its regulation level from an overshoot. Figure 27 shows such a case where the load toggles between 1.7 A and only 50 mA.

Feature Description (continued)

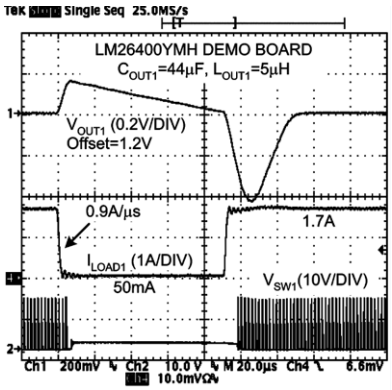


Figure 27. Extreme Load Step

In the example, the load first goes down to 50 mA quickly (0.9 A/µs), causing a 90-µs no-switching period, and then quickly goes up to 1.7 A when V_{OUT1} just hits its regulation level (1.2 V), resulting in a large dip of 440 mV in the output voltage.

If it is known in a system design that the load can go down to less than 100 mA during a load step, and that the load can toggle high any time after it toggles low, take the following measures to minimize the potential extra undershoot. First is to add the Cff mentioned above. Second is to increase the output capacitance.

For example, to meet a ±10% V_{OUT} excursion requirement for a 100 mA to 2-A load step, approximately 200 µF output capacitance is needed for a 1.2-V output, and about 44 µF is needed for a 5-V output.

7.4 Device Functional Modes

7.4.1 Start-Up and Shutdown

During a soft start, the ramp of the output voltage is proportional to the ramp of the SS pin. When the EN pin is pulled high, an internal 16-µA current source starts to charge the corresponding SS pin. The capacitance between the SS pin and ground determines how fast the SS voltage ramps up. The noninverting input of the transconductance error amplifier, that is, the moving reference during soft start, will be the lower of SS voltage and the 0.6-V reference (V_{REF}). So before SS reaches 0.6V, the reference to the error amplifier will be the SS voltage. When SS exceeds 0.6 V, the noninverting input of the transconductance amplifier will be a constant 0.6 V and that will be the time soft start ends. The SS voltage will continue to ramp all the way up to the internal 2.7-V supply voltage before leveling off.

To calculate the needed SS capacitance for a given soft-start duration, use Equation 4.

$$C_{SS} = \frac{I_{SS} \times t_{SS}}{V_{REF}} \quad (4)$$

where

- I_{SS} is SS pin charging current, typically 16 µA
- V_{REF} is the internal reference voltage, typically 0.6 V
- t_{SS} is the desired soft-start duration

For example, if 1 ms is the desired soft-start time, then the nominal SS capacitance should be 25 nF. Apply tolerances if necessary. Use the V_{FB} entry in *Electrical Characteristics* for the V_{REF} tolerance.

Device Functional Modes (continued)

Inductor current during soft start can be calculated by Equation 5.

$$I_{ind} = \frac{C_{OUT}}{C_{SS}} \times \frac{V_{OUT}}{V_{REF}} \times I_{SS} + I_{OUT}$$

where

- V_{OUT} is the target output voltage
- I_{OUT} is the load current during start-up
- C_{OUT} is the output capacitance (5)

For example, if the output capacitor is 10 µF, output voltage is 2.5 V, soft-start capacitor is 10 nF and there is no load, then the average inductor current during soft start will be 62.5 mA.

When EN pin is pulled below 0.4 V or so, the 16-µA current source will stop charging the SS pin. The SS pin will be discharged through a 330-Ω internal FET to ground. During this time, the internal power switch will remain turned off while the output is discharged by the load.

If EN is again pulled high before SS and output voltage are completely discharged, soft-start will begin with a non-zero reference and the level of the soft-start reference will be the lower of SS voltage and 0.6 V.

When the output is prebiased, the LM26400Y can usually start up successfully if there is at least a 2-V difference between the input voltage and the prebias. An output prebias condition refers to the case when the output is sitting at a non-zero voltage at the beginning of a start-up. The key to a successful start-up under such a situation is enough initial voltage across the bootstrap capacitor. When an output prebias condition is anticipated, the power supply designer should check the start-up behavior under the highest potential prebias.

A prebias condition caused by a glitch in the enable signal after start-up or by an input brownout condition normally is not an issue because the bootstrap capacitor holds its charge much longer than the output capacitors.

Due to the frequency foldback mechanism, the switching frequency during start-up will be lower than the normal value before V_{FB} reaches 0.35 V or so. See Figure 10.

It is generally okay to connect the EN pin to V_{IN} to simplify the system design. However, if the V_{IN} ramp is slow and the load current is relatively high during soft start, the V_{OUT} ramp may have a notch in it and a slight overshoot at the end of startup. This is due to the reduced load current handling capability of the LM26400Y for V_{IN} lower than 5 V. If this kind of behavior is a problem for the system designer, there are two solutions. One is to control the EN pin with a logic signal and do not pull the EN high until V_{IN} is above 5 V or so. Make sure the logic signal is never higher than V_{IN} by 0.3 V. The other is to use an external 5-V bootstrap bias if it is ready before V_{IN} hits 2.7 V or so. See *Low Input Voltage Considerations* for more information.

8 Application and Implementation

NOTE

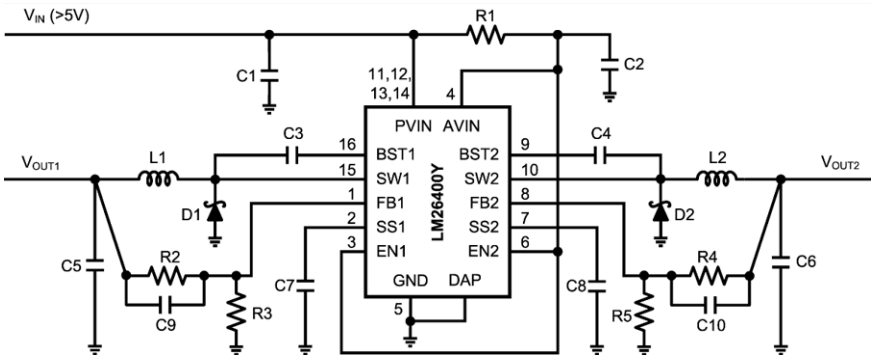
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM26400Y device will operate with input voltage from 3 V to 20 V and provide two regulated output voltages. The device is optimized for high-efficiency operation with minimum number of external components.

8.2 Typical Applications

8.2.1 LM26400Y Design Example 1



8.2.1.1 Design Requirements

The device must be able to operate at any voltage within the recommended operating range. The load current must be defined in order to properly size the inductor, input, and output capacitors .The inductor must be able to handle full expected load current as well as the peak current generated load transients and start-up.

8.2.1.2 Detailed Design Procedure

The best capacitors for use with the LM26400Y are multi-layer ceramic capacitors. They have the lowest ESR (equivalent series resistance) and highest resonance frequency which makes them optimum for use with high frequency switching converters. When selecting a ceramic capacitor, only X5R and X7R dielectric types should be used. Other types such as Z5U and Y5F have such severe loss of capacitance due to effects of temperature variation and applied voltage, they may provide as little as 20% of rated capacitance in many typical applications. Always consult capacitor manufacturer's data curves before selecting a capacitor. High-quality ceramic capacitors can be obtained from Taiyo-Yuden, AVX, and Murata.

Typical Applications (continued)

Table 1. Bill of Materials (Circuit 1, V_{IN} = 12 V±10%, Output1 = 1.2 V/2 A, Output2 = 2.5 V/2 A)

PART	DESCRIPTION	PART VALUES	PHYSICAL SIZE	PART NUMBER	MANUFACTURER
C1	Capacitor, Ceramic	10 µF, 16 V, X5R	1210	GRM32DR61C106KA01	Murata
C2	Capacitor, Ceramic	0.22 µF, 16 V, X5R	0603	EMK107BJ224KA-T	Taiyo Yuden
C3	Capacitor, Ceramic	0.1 µF, 6.3 V, X5R	0402	C1005X5R0J104K	TDK
C4	Capacitor, Ceramic	0.1 µF, 6.3 V, X5R	0402	C1005X5R0J104K	TDK
C5	Capacitor, Ceramic	100 µF, 6.3 V, X5R	1210	GRM32ER60J107ME20L	Murata
C6	Capacitor, Ceramic	47 µF, 6.3 V, X5R	1210	GRM32ER60J476ME20L	Murata
C7	Capacitor, Ceramic	0.012 µF, 6.3 V, X5R	0402	C0402C123K9PACTU	Kemet
C8	Capacitor, Ceramic	0.012 µF, 6.3 V, X5R	0402	C0402C123K9PACTU	Kemet
C9	Capacitor, Ceramic	0.027 µF, 6.3 V, X5R	0402	C0402C273K9PACTU	Kemet
C10	Capacitor, Ceramic	0.027 µF, 6.3 V, X5R	0402	C0402C273K9PACTU	Kemet
D1	Diode, Schottky	2 A, 30 V	SMB	MBRS230LT3G	ON Semiconductor
D2	Diode, Schottky	2 A, 30 V	SMB	MBRS230LT3G	ON Semiconductor
L1	Inductor	5 µH, 2.2 A	7 × 7 × 2.8 mm^3	CDRH6D26NP-5R0NC	Sumida
L2	Inductor	8.7 µH, 2.2 A	7 × 7 × 4 mm^3	CDRH6D38NP-8R7NC	Sumida
R1	Resistor	10 Ω, 1%	0402	CRCW040210R0FK	Vishay
R2	Resistor	5.9 kΩ, 1%	0402	CRCW04025K90FK	Vishay
R3	Resistor	5.9 kΩ, 1%	0402	CRCW04025K90FK	Vishay
R4	Resistor	18.7 kΩ, 1%	0402	CRCW040218K7FK	Vishay
R5	Resistor	5.9 kΩ, 1%	0402	CRCW04025K90FK	Vishay
U1	Regulator	Dual 2-A Buck	HTSSOP-16	LM26400YMH	Texas Instruments

Table 2. Bill of Materials (Circuit 1, V_{IN} = 7 V to 20 V, Output1 = 3.3 V/2 A, Output2 = 5 V/2 A)

PART	DESCRIPTION	PART VALUES	PHYSICAL SIZE	PART NUMBER	MANUFACTURER
C1	Capacitor, Ceramic	10 µF, 25 V, X5R	1812	GRM43DR61E106KA12	Murata
C2	Capacitor, Ceramic	0.22 µF, 25 V, X5R	0603	TMK107BJ224KA-T	Taiyo Yuden
C3	Capacitor, Ceramic	0.1 µF, 6.3 V, X5R	0402	C1005X5R0J104K	TDK
C4	Capacitor, Ceramic	0.1 µF, 6.3 V, X5R	0402	C1005X5R0J104K	TDK
C5	Capacitor, Ceramic	47 µF, 6.3 V, X5R	1210	GRM32ER60J476ME20	Murata
C6	Capacitor, Ceramic	33 µF, 6.3 V, X5R	1210	GRM32DR60J336ME19	Murata
C7	Capacitor, Ceramic	0.012 µF, 6.3 V, X5R	0402	C0402C123K9PACTU	Kemet
C8	Capacitor, Ceramic	0.012 µF, 6.3 V, X5R	0402	C0402C123K9PACTU	Kemet
C9	Capacitor, Ceramic	0.027 µF, 6.3 V, X5R	0402	C0402C273K9PACTU	Kemet
C10	Capacitor, Ceramic	0.027 µF, 6.3 V, X5R	0402	C0402C273K9PACTU	Kemet
D1	Diode, Schottky	2 A, 30 V	SMB	MBRS230LT3G	ON Semiconductor
D2	Diode, Schottky	2 A, 30 V	SMB	MBRS230LT3G	ON Semiconductor
L1	Inductor	10 µH, 3 A	8.3 × 8.3 × 4 mm^3	CDRH8D38NP-100NC	Sumida
L2	Inductor	15 µH, 3 A	8.3 × 8.3 × 4 mm^3	CDRH8D43/HP-150NC	Sumida
R1	Resistor	10 Ω, 1%	0402	CRCW040210R0FK	Vishay
R2	Resistor	26.7 kΩ, 1%	0402	CRCW040226K7FK	Vishay
R3	Resistor	5.9 kΩ, 1%	0402	CRCW04025K90FK	Vishay
R4	Resistor	43.2 kΩ, 1%	0402	CRCW040218K7FK	Vishay
R5	Resistor	5.9 kΩ, 1%	0402	CRCW04025K90FK	Vishay
U1	Regulator	Dual 2-A Buck	HTSSOP-16	LM26400YMH	Texas Instruments

8.2.1.3 Application Curves

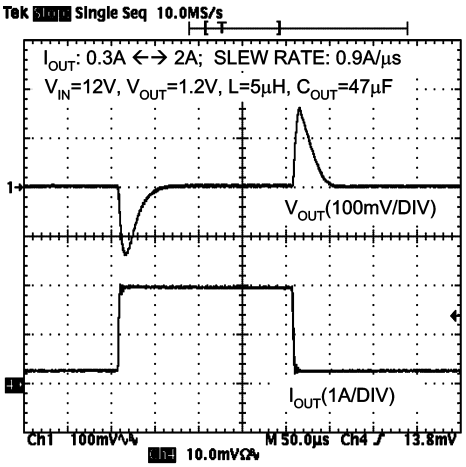


Figure 28. Load Step Response

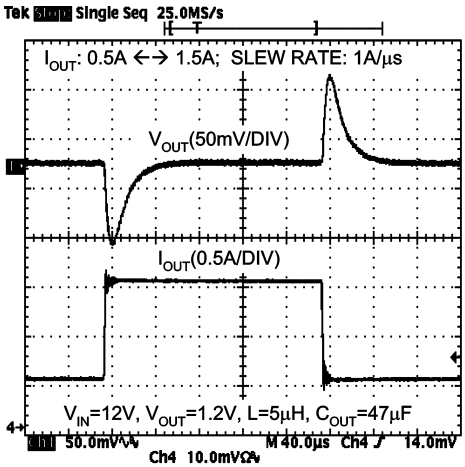


Figure 29. Load Step Response

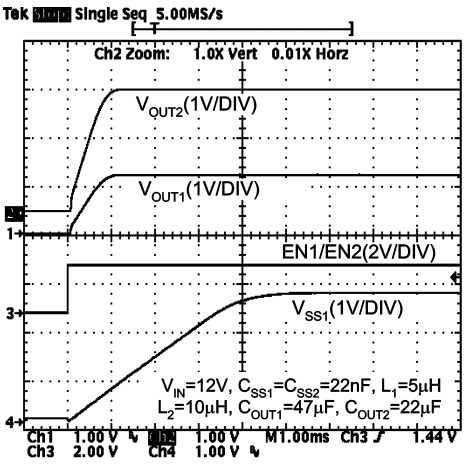


Figure 30. Start-Up (No Load)

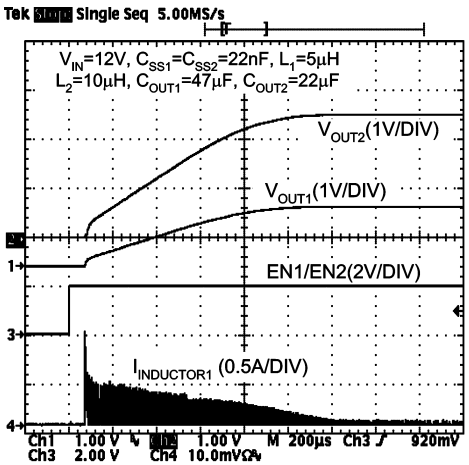


Figure 31. Start-Up (No Load)

8.2.2 LM26400Y Design Example 2

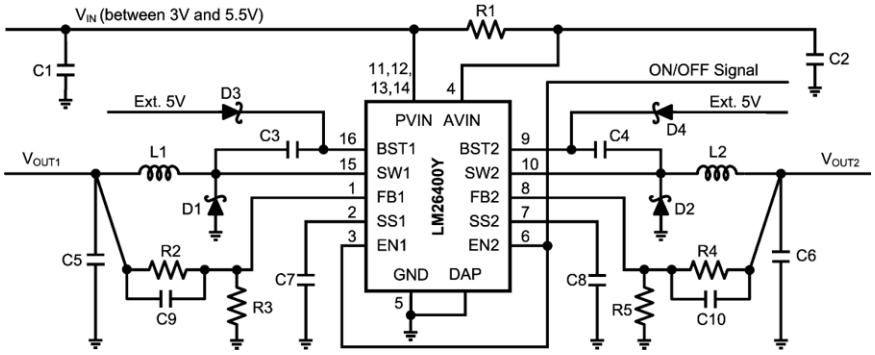


Table 3. Bill of Materials (Circuit 2, V_{IN} = 3 V to 5 V, Output1 = 1.2 V/2 A, Output2 = 1.8 V/2 A)

PART	DESCRIPTION	PART VALUES	PHYSICAL SIZE	PART NUMBER	MANUFACTURER
C1	Capacitor, Ceramic	10 µF, 6.3 V, X5R	1206	GRM319R60J106KE19	Murata
C2	Capacitor, Ceramic	0.22 µF, 6.3 V, X5R	0402	JMK105BJ224KV-F	Taiyo Yuden
C3	Capacitor, Ceramic	0.1 µF, 6.3 V, X5R	0402	C1005X5R0J104K	TDK
C4	Capacitor, Ceramic	0.1 µF, 6.3 V, X5R	0402	C1005X5R0J104K	TDK
C5	Capacitor, Ceramic	100 µF, 6.3 V, X5R	1210	GRM32ER60J107ME20L	Murata
C6	Capacitor, Ceramic	100 µF, 6.3 V, X5R	1210	GRM32ER60J107ME20L	Murata
C7	Capacitor, Ceramic	0.012 µF, 6.3 V, X5R	0402	C0402C123K9PACTU	Kemet
C8	Capacitor, Ceramic	0.012 µF, 6.3 V, X5R	0402	C0402C123K9PACTU	Kemet
C9	Capacitor, Ceramic	0.027 µF, 6.3 V, X5R	0402	C0402C273K9PACTU	Kemet
C10	Capacitor, Ceramic	0.027 µF, 6.3 V, X5R	0402	C0402C273K9PACTU	Kemet
D1	Diode, Schottky	2 A, 30 V	SMB	MBRS230LT3G	ON Semiconductor
D2	Diode, Schottky	2 A, 30 V	SMB	MBRS230LT3G	ON Semiconductor
L1	Inductor	5 µH, 2.2 A	7 × 7 × 2.8 mm^3	CDRH6D26NP-5R0NC	Sumida
L2	Inductor	5 µH, 2.2 A	7 × 7 × 2.8 mm^3	CDRH6D26NP-5R0NC	Sumida
R1	Resistor	10 Ω, 1%	0402	CRCW040210R0FK	Vishay
R2	Resistor	5.9 kΩ, 1%	0402	CRCW04025K90FK	Vishay
R3	Resistor	5.9 kΩ, 1%	0402	CRCW04025K90FK	Vishay
R4	Resistor	11.8 kΩ, 1%	0402	CRCW040211K8FK	Vishay
R5	Resistor	5.90 kΩ, 1%	0402	CRCW04025K90FK	Vishay
U1	Regulator	Dual 2-A Buck	HTSSOP-16	LM26400YMH	Texas Instruments

9 Power Supply Recommendations

9.1 Low Input Voltage Considerations

When V_{IN} is from 3 V to 5 V, TI recommends that an external bootstrap bias voltage and a Schottky diode be used to handle load currents up to 2 A. See Figure 32 for an illustration.

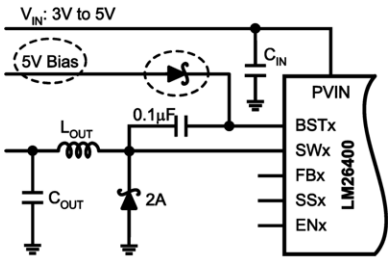


Figure 32. External Bootstrap for Low V_{IN}

The recommended voltage for the external bias is 5 V. Due to the absolute maximum rating of V_{BST} - V_{SW}, the external 5-V bias should not be higher than 6 V.

9.2 Programming Output Voltage

First make sure the required maximum duty cycle in steady state is less than 80% so that the regulator will not lose regulation. The datasheet lower limit for maximum duty cycle is about 90% over temperature (see *Electrical Characteristics* for the accurate value). The maximum duty cycle in steady state happens at low line and full load.

The output voltage is programmed through the feedback resistors R1 and R2, as illustrated in Figure 33.

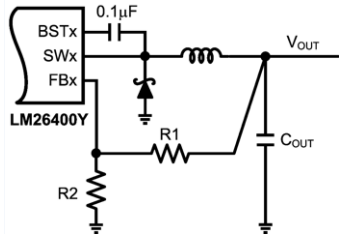


Figure 33. Programming Output Voltage

TI recommends that the lower feedback resistor R2 always be 5.9 kΩ. This simplifies the selection of the C_{FF} value (for an explanation of C_{FF}, see *Load Step Response*). The 5.9 kΩ is also a suitable R2 value in applications that need to increase the output voltage on the fly by paralleling another resistor with R2. Because the FB pin is 0.6 V during normal operation, the current through the feedback resistors is normally 0.6 V / 5.9 kΩ = 0.1 mA and the power dissipation in R2 is 0.6 V × 0.6 V / 5.9 kΩ = 61 µW - low enough for 0402 size or smaller resistors.

Use Equation 6 to determine the upper feedback resistor R1.

$$R1 = \left(\frac{V_{OUT}}{V_{FB}} - 1\right) \times R2 \tag{6}$$

To determine the maximum allowed resistor tolerance, use Equation 7:

$$\sigma = \frac{1}{1 - \frac{V_{FB}}{V_{OUT}}} \times 2 \times \frac{}{TOL - \phi} + 1 \tag{7}$$

where

- TOL is the set point accuracy of the regulator
- Φ is the tolerance of V_{FB}

Programming Output Voltage (continued)

Example:

V_{OUT} = 1.2 V, with a set-point accuracy of ±3.5%.

$$\sigma = \frac{1}{1+2\times\frac{1-\frac{0.6V}{1.2V}}{3.5\%-2\%}} = 1.48\% \quad (8)$$

Choose 1% resistors. R2 = 5.90 kΩ.

$$R1 = \left(\frac{1.2V}{0.6V} - 1\right)\times 5.90k\Omega = 5.90k\Omega \quad (9)$$

10 Layout

10.1 Layout Guidelines

There are mainly two considerations for PCB layout - thermal and electrical. For thermal details, see *Thermal Considerations*. Electrical wise, follow the rules below as much as possible. In general, the LM26400Y is a quite robust part in terms of insensitivity to different layout patterns or even abuses.

- Keep the input ceramic capacitor(s) as close to the PVIN pins as possible.
- Use internal ground planes when available.
- The SW pins are high current carrying pins so traces connected to them should be short and fat.
- Keep feedback resistors close to the FB pins.
- Keep the AVIN RC filter close to the AVIN pin.
- Keep the voltage feedback traces away from the switch nodes.
- Use six or more vias next to the ground pad of the catch diode.
- Use at least four vias next to the ground pad of output capacitors.
- Use at least four vias next to each pad of the input capacitors.

For low EMI emission, try not to assign large areas of copper to the noisy switch nodes as a heat sinking method. Instead, assign a lot of copper to the output nodes.

10.1.1 Thermal Shutdown

Whenever the junction temperature of the LM26400Y exceeds 165°C, the MOSFET switch will be kept off until the temperature drops below 150°C, at which point the regulator will go through a hard start to quickly raise the output voltage back to normal. Since it is a hard start, there will be an overshoot at the output. See Figure 20.

10.1.2 Power Loss Estimation

The total power loss in the LM26400Y comprises of three parts: the power FET conduction loss, the power FET switching loss, and the IC's housekeeping power loss. Use Equation 10 to estimate the conduction loss.

$$P_{CON} = I_{OUT}^2 \times R_{DS} \times \left(1+\frac{T_J - 25^\circ C}{200^\circ C}\right)\times\frac{V_{OUT}+0.5V}{V_{IN}+0.5V} \quad (10)$$

where

- T_J is the junction temperature or the target junction temperature if the former is unknown
- R_{DS} is the ON resistance of the internal FET at room temperature

Use 180 mΩ for R_{DS} if the actual value is unknown.

Use Equation 11 to estimate the switching loss.

$$P_{SW} = V_{IN} \times f_{SW} \times I_{OUT} \times 10\mu W/kHz/V/A \quad (11)$$

Another loss in the IC is the housekeeping loss. The loss is the power dissipated by circuitry in the IC other than the power FETs. The equation is:

$$P_{HK} = V_{IN} \times 4\,mA + 15\,mW \quad (12)$$

The 15 mW is gate drive loss. Do the calculation for both channels and find out the total power loss in the IC.

Layout Guidelines (continued)

$$P_{LOSS} = P_{CON1} + P_{SW1} + P_{CON2} + P_{SW2} + P_{HK} \quad (13)$$

The power loss calculation can help estimate the overall power supply efficiency.

Example:

V_{IN} = 12 V, V_{OUT1} = 1.2 V, I_{OUT1} = 2 A, V_{OUT2} = 2.5 V, I_{OUT2} = 2 A. Target junction temperature is 90°C.

So conduction loss in Channel 1 is:

$$P_{CON1} = (2A)^2 \times 180\,m\Omega \times \left(1 + \frac{90^\circ C - 25^\circ C}{200^\circ C}\right) \times \frac{1.2V + 0.5V}{12V + 0.5V}$$
$$= 0.13W \quad (14)$$

Conduction loss in Channel 2 is:

$$P_{CON2} = (2A)^2 \times 180\,m\Omega \times \left(1 + \frac{90^\circ C - 25^\circ C}{200^\circ C}\right) \times \frac{2.5V + 0.5V}{12V + 0.5V}$$
$$= 0.23W \quad (15)$$

Switching loss in either channel is:

$$P_{SW1} = P_{SW2} = 12V \times 520\,kHz \times 2A \times 10\,\mu W/kHz/V/A$$
$$= 0.13W \quad (16)$$

Housekeeping loss is:

$$P_{HK} = 12V \times 4\,mA + 15\,mW = 0.063W \quad (17)$$

Finally the total power loss in the LM26400Y is:

$$P_{LOSS} = 0.13W + 0.13W + 0.23W + 0.13W + 0.063W$$
$$= 0.68W \quad (18)$$

10.1.3 Inductor Selection

TI recommends an inductance value that gives a peak-to-peak ripple current of 0.4 A to 0.8 A. Too large of a ripple current can reduce the maximum achievable DC load current because the peak current of the switch is limited to a typical of 3 A. Too small of a ripple current can cause the regulator to oscillate due to the lack of inductor current ramp signal, especially under high input voltages. Use Equation 19 to determine inductance:

$$L = \frac{V_{OUT} + 0.5V}{V_{IN\_MAX} + 0.5V} \times \frac{V_{IN\_MAX} - V_{OUT}}{\Delta I \times f_{SW}}$$

where

- V_{IN_MAX} is the maximum input voltage of the application. (19)

The rated current of the inductor should be higher than the maximum DC load current. Generally speaking, the lower the DC resistance of the inductor winding, the higher the overall regulator efficiency.

Ferrite core inductors are recommended for less AC loss and less fringing magnetic flux. The drawback of ferrite core inductors is their quick saturation characteristic. Once the inductor gets saturated, its current can spike up very quickly if the switch is not turned off immediately. The current limit circuit has a propagation delay and so is oftentimes not fast enough to stop the saturated inductor from going above the current limit. This has the potential to damage the internal switch. So to prevent a ferrite core inductor from getting into saturation, the inductor saturation current rating should be higher than the switch current limit I_{CL}. The LM26400Y is quite robust in handling short pulses of current that is a few amps above the current limit. When a compromise has to be made, pick an inductor with a saturation current just above the lower limit of the I_{CL}. Be sure to validate the short-circuit protection over the intended temperature range.

To prevent the inductor from saturating over the entire –40°C to 125°C range, pick one with a saturation current higher than the upper limit of I_{CL} in *Electrical Characteristics*.

Inductor saturation current is usually lower when hot. So consult the inductor vendor if the saturation current rating is only specified at room temperature.

Layout Guidelines (continued)

Soft saturation inductors such as the iron powder types can also be used. Such inductors do not saturate suddenly and therefore are safer when there is a severe overload or even shorted output. Their physical sizes are usually smaller than the Ferrite core inductors. The downside is their fringing flux and higher power dissipation due to relatively high AC loss, especially at high frequencies.

Example:

V_{OUT} = 1.2 V; V_{IN} = 9 V to 14 V; I_{OUT} = 2 A maximum; Peak-to-peak Ripple Current ΔI = 0.6 A.

$$L = \frac{1.2V + 0.5V}{14V + 0.5V} \times \frac{14V - 1.2V}{0.6A \times 500kHz} = 5\mu H \quad (20)$$

Choose a 5-µH or so ferrite core inductor that has a saturation current around 3 A at room temperature. For example, Sumida's CDRH6D26NP-5R0NC.

If the maximum load current is significantly lower than 2 A, pick an inductor with the same saturation rating as a 2-A design but with a lowered DC current rating. That should result in a smaller inductor. There are not many choices, though. Another possibility is to use a soft saturation type inductor, whose size will be dominated by the DC current rating.

10.1.4 Output Capacitor Selection

Output capacitors in a buck regulator handles the AC current from the inductor and so have little ripple RMS current and their power dissipation is not a concern. The concern usually revolves around loop stability and capacitance retention.

The LM26400Y's internal loop compensation was designed around ceramic output capacitors. From a stability point of view, the lower the output voltage, the more capacitance is needed.

Below is a quick summary of temperature characteristics of some commonly used ceramic capacitors. So an X7R ceramic capacitor means its capacitance can vary ±15% over the temperature range of –55°C to 125°C.

Table 4. Capacitance Variation Over Temperature (Class II Dielectric Ceramic Capacitors)

LOW TEMPERATURE	HIGH TEMPERATURE	CAPACITANCE CHANGE RANGE
X: –55°C	5: +85°C	R: ±15%
Y: –30°C	6: +105°C	S: ±22%
Z: +10°C	7: +125°C	U: +22%, –56%
	8: +150°C	V: +22%, –82%

Besides the variation of capacitance over temperature, the actual capacitance of ceramic capacitors also vary, sometimes significantly, with applied DC voltage. Figure 34 illustrates such a characteristic of several ceramic capacitors of various physical sizes from Murata. Unless the DC voltage across the capacitor is going to be small relative to its rated value, going to too small a physical size will have the penalty of losing significant capacitance during circuit operation.

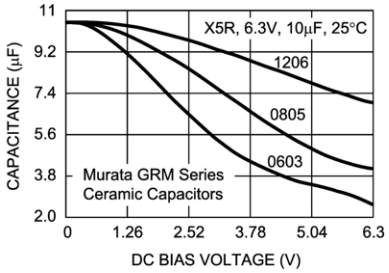


Figure 34. Capacitance vs Applied DC Voltage

The amount of output capacitance directly contributes to the output voltage ripple magnitude. A quick way to estimate the output voltage ripple is to multiply the inductor peak-to-peak ripple current by the impedance of the output capacitors. For example, if the inductor ripple current is 0.6 A peak-to-peak, and the output capacitance is 44 µF, then the output voltage ripple should be close to 0.6 A × $(6.28 \times 500\ \text{kHz} \times 44\ \mu\text{F})^{-1}$ = 4.3 mV. Sometimes when a large ceramic capacitor is used, the switching frequency may be higher than the capacitor's self resonance frequency. In that case, find out the true impedance at the switching frequency and then multiply that value by the ripple current to get the ripple voltage.

The amount of output capacitance also impacts the stability of the feedback loop. Refer to *Loop Stability* for guidelines.

10.1.5 Input Capacitor Selection

The input capacitors provide the AC current needed by the nearby power switch so that current provided by the upstream power supply does not carry a lot of AC content, generating less EMI. To the buck regulator in question, the input capacitor also prevents the drain voltage of the FET switch from dipping when the FET is turned on, therefore providing a healthy line rail for the LM26400Y to work with. Since typically most of the AC current is provided by the local input capacitors, the power loss in those capacitors can be a concern. In the case of the LM26400Y regulator, since the two channels operate 180° out of phase, the AC stress in the input capacitors is less than if they operated in phase. The measure for the AC stress is called input ripple RMS current. It is strongly recommended that at least one 4.7-µF ceramic capacitor be placed next to the PVIN pins. Bulk capacitors such as electrolytic capacitors or OSCON capacitors can be added to help stabilize the local line voltage, especially during large load transient events. As for the ceramic capacitors, use X7R , X6S, or X5R types. They maintain most of their capacitance over a wide temperature range. Try to avoid sizes smaller than 0805. Otherwise significant drop in capacitance may be caused by the DC bias voltage. See *Output Capacitor Selection* section for more information. The DC voltage rating of the ceramic capacitor should be higher than the highest input voltage.

Capacitor temperature is a major concern in board designs. While using a 4.7-µF or higher MLCC as the input capacitor is a good starting point, it is a good idea to check the temperature in the real thermal environment to make sure the capacitors are not over heated. Capacitor vendors may provide curves of ripple RMS current versus temperature rise, based on a designated thermal impedance. In reality, the thermal impedance may be very different. So it is always a good idea to check the capacitor temperature on the board.

Because the duty cycles of the two channels may overlap, calculation of the input ripple RMS current is a little tedious. Use Equation 21:

$$I_{irrm} = \sqrt{(I_1 - I_{av})^2 d1 + (I_2 - I_{av})^2 d2 + (I_1 + I_2 - I_{av})^2 d3}$$

where

- I_1 is Channel 1's maximum output current
- I_2 is Channel 2's maximum output current
- d1 is the non-overlapping portion of Channel 1's duty cycle, D_1
- d2 is the non-overlapping portion of Channel 2's duty cycle, D_2
- d3 is the overlapping portion of the two duty cycles
- I_{av} is the average input current, $I_{av} = I_1 \times D_1 + I_2 \times D_2$ (21)

To quickly determine the values of d1, d2, and d3, refer to the decision tree in Figure 35. To determine the duty cycle of each channel, use $D = V_{OUT}/V_{IN}$ for a quick result or use the following equation for a more accurate result.

$$D = \frac{V_{OUT} + 0.5V + I_{OUT} \times R_{DC}}{V_{IN} + 0.5V - I_{OUT} \times R_{DS}}$$

where

- R_{DC} is the winding resistance of the inductor
- R_{DS} is the ON-resistance of the MOSFET switch. (22)

Example:

V_{IN} = 5 V, V_{OUT1} = 3.3 V, I_{OUT1} = 2 A, V_{OUT2} = 1.2 V, I_{OUT2} = 1.5 A, R_{DS} = 170 mΩ, R_{DC} = 30 mΩ. (I_{OUT1} is the same as I_1 in the input ripple RMS current equation, I_{OUT2} is the same as I_2).

First, find out the duty cycles. Plug the numbers into the duty cycle equation and we get D1 = 0.75, and D2 = 0.33. Next, follow the decision tree in Figure 35 to find out the values of d1, d2, and d3. In this case, d1 = 0.5, d2 = D2 + 0.5 – D1 = 0.08, and d3 = D1 – 0.5 = 0.25. $I_{av} = I_{OUT1} \times D1 + I_{OUT2} \times D2 = 1.995$ A. Plug all the numbers into the input ripple RMS current equation and the result is $I_{irrm} = 0.77$ A.

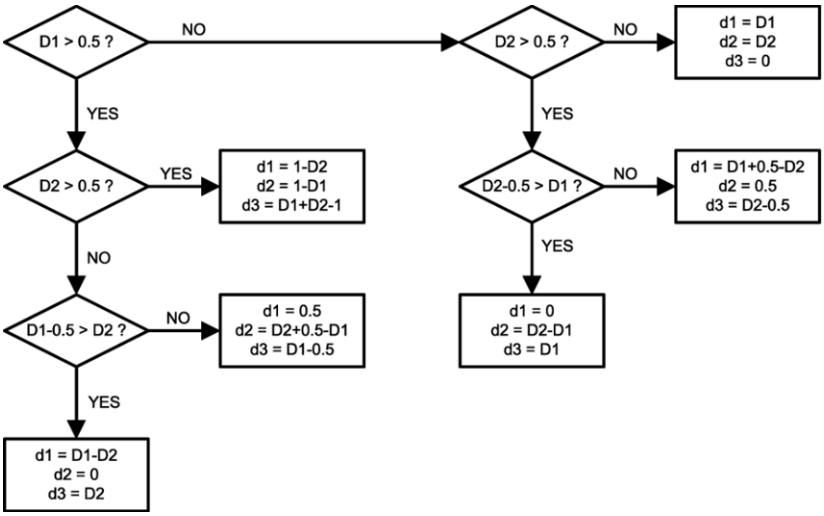


Figure 35. Determining d1, d2, and d3

10.1.6 Catch Diode Selection

The catch diode should be at least 2-A rated. The most stressful operation for the diode is usually when the output is shorted under high line. Always pick a Schottky diode for its lower forward drop and higher efficiency. The reverse voltage rating of the diode should be at least 25% higher than the highest input voltage. The diode junction temperature is a main concern here. Always validate the diode's junction temperature in the intended thermal environment to make sure its thermally derated maximum current is not exceeded. There are a few 2-A, 30-V surface mount Schottky diodes available in the market. Diodes have a negative temperature coefficient, so do not put two diodes in parallel to achieve a lower temperature rise. Current will be hogged by one of the diodes instead of shared by the two. Use a larger package for that purpose.

10.2 Layout Example

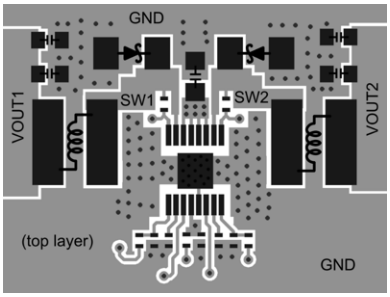


Figure 36. PCB Layout Example

10.3 Thermal Considerations

Due to the low thermal impedance from junction to the die-attach pad (or DAP, exposed metal at the bottom of the package), thermal performance heavily depends on PCB copper arrangement. The minimum requirement is to have a top-layer thermal pad that is exactly the same size as the DAP. There should be at least nine 8-mil thermal vias in the pad. The thermal vias should be connected to internal ground planes (if available) and to a ground plane on the bottom layer that is as large as allowed.

Thermal Considerations (continued)

In boards that have internal ground planes, extending the top-layer thermal pad outside the body of the package to form a "dogbone" shape offers little performance improvement. However, for two-layer boards, the dogbone shape on the top layer will provide significant help.

Predicting on paper with reasonable accuracy the junction temperature of the LM26400Y in a real-world application is still an art. Major factors that contribute to the junction temperature but not directly associated with the thermal performance of the LM26400Y itself include air speed, air temperature, nearby heating elements and arrangement of PCB copper connected to the DAP of the LM26400Y. The $R_{\theta JA}$ value published in the datasheet is based on a standard board design in a single heating element mode and measured in a standard environment. The real application is usually completely different from those conditions. So the actual $R_{\theta JA}$ will be significantly different from the datasheet number. The best approach is still to assign as much copper area as allowed to the DAP and prototype the design.

When prototyping the design, it is necessary to know the junction temperature of the LM26400Y to assess the thermal margin. The best way to measure the LM26400Y's junction temperature when the board is working in its usual mode is to measure the package-top temperature using an infrared thermal imaging camera. Look for the highest temperature reading across the case-top. Add two degrees to the measurement result and the number should be a pretty good estimate of the junction temperature. Due to the high temperature gradient across the case-top, the use of a thermal couple is generally not recommended. If a thermal couple has to be used, try to locate the hottest spot on the case-top first and then secure the thermal couple at exactly the same location. The thermal couple needs to be a light-gauge type (such as 40-gauge). Apply a small blob of thermal compound to the contact point and then secure the thermal couple on the case-top using thermally non-conductive glue.

If the maximum allowed junction temperature is exceeded, load current has to be lowered to bring the temperature back in specification. Or better thermal management such as more air flow needs to be provided.

As a summary, here is a list of important items to consider:

- Use multi-layer PC boards with internal ground planes.
- Use nine or more thermal vias to connect the top-layer thermal pad to internal ground planes and ground copper on the bottom layer.
- Generate as large a ground plane as allowable on outer layers, especially near the package.
- Use 2-oz. copper whenever possible.
- Try to spread out heat generating components.
- The inductors and diodes are heat generating components and should be connected to power or ground planes using many vias.

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM26400YMH/NOPB	Active	Production	HTSSOP (PWP) | 16	92 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L26400 YMH
LM26400YMH/NOPB.A	Active	Production	HTSSOP (PWP) | 16	92 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L26400 YMH
LM26400YMHX/NOPB	Active	Production	HTSSOP (PWP) | 16	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L26400 YMH
LM26400YMHX/NOPB.A	Active	Production	HTSSOP (PWP) | 16	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L26400 YMH
LM26400YSD/NOPB	Active	Production	WSON (NHQ) | 16	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-	L26400Y
LM26400YSD/NOPB.A	Active	Production	WSON (NHQ) | 16	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L26400Y
LM26400YSDE/NOPB	Active	Production	WSON (NHQ) | 16	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-	L26400Y
LM26400YSDE/NOPB.A	Active	Production	WSON (NHQ) | 16	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L26400Y

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

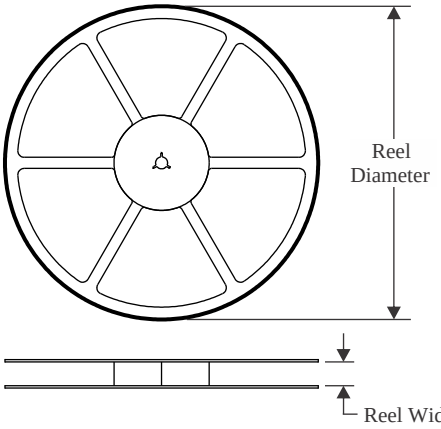
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

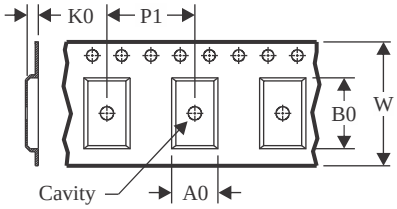
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

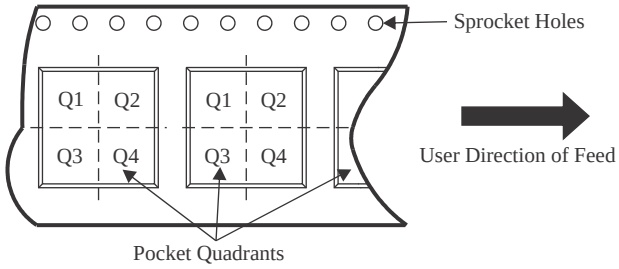


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

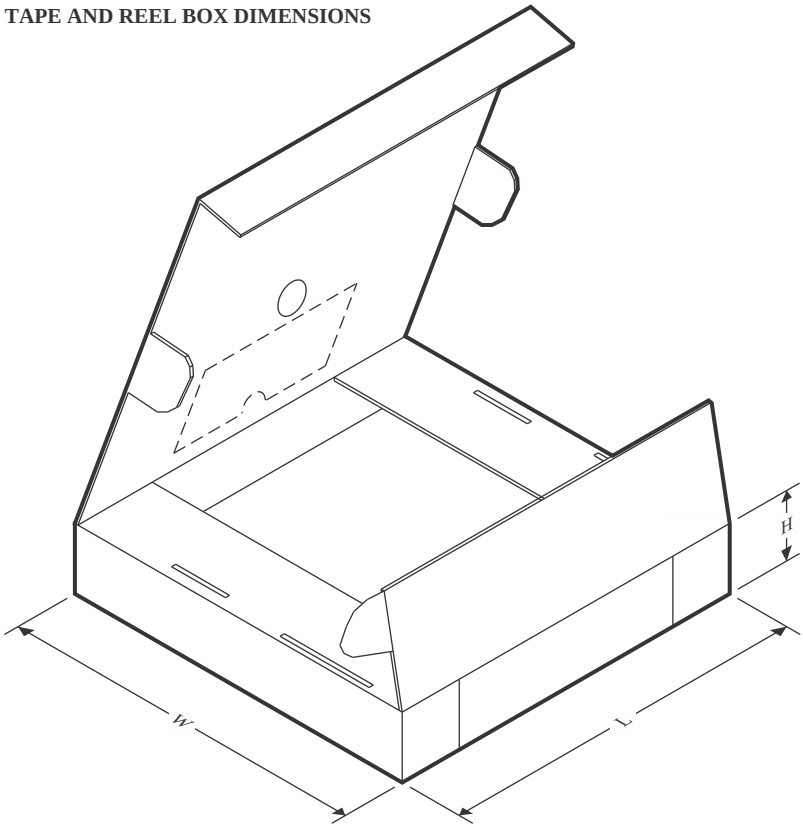
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM26400YMHX/NOPB	HTSSOP	PWP	16	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1
LM26400YSD/NOPB	WSON	NHQ	16	1000	177.8	12.4	5.3	5.3	1.3	8.0	12.0	Q1
LM26400YSDE/NOPB	WSON	NHQ	16	250	177.8	12.4	5.3	5.3	1.3	8.0	12.0	Q1

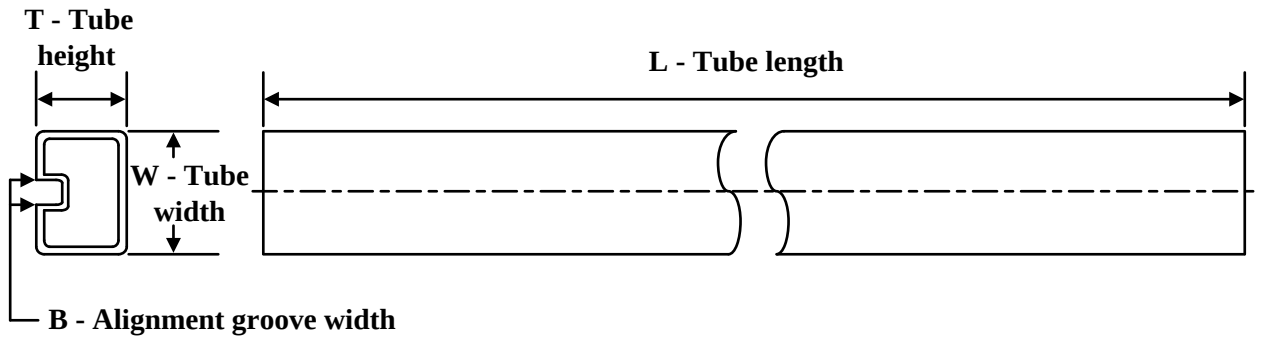
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM26400YMHX/NOPB	HTSSOP	PWP	16	2500	367.0	367.0	35.0
LM26400YSD/NOPB	WSON	NHQ	16	1000	210.0	185.0	35.0
LM26400YSDE/NOPB	WSON	NHQ	16	250	210.0	185.0	35.0

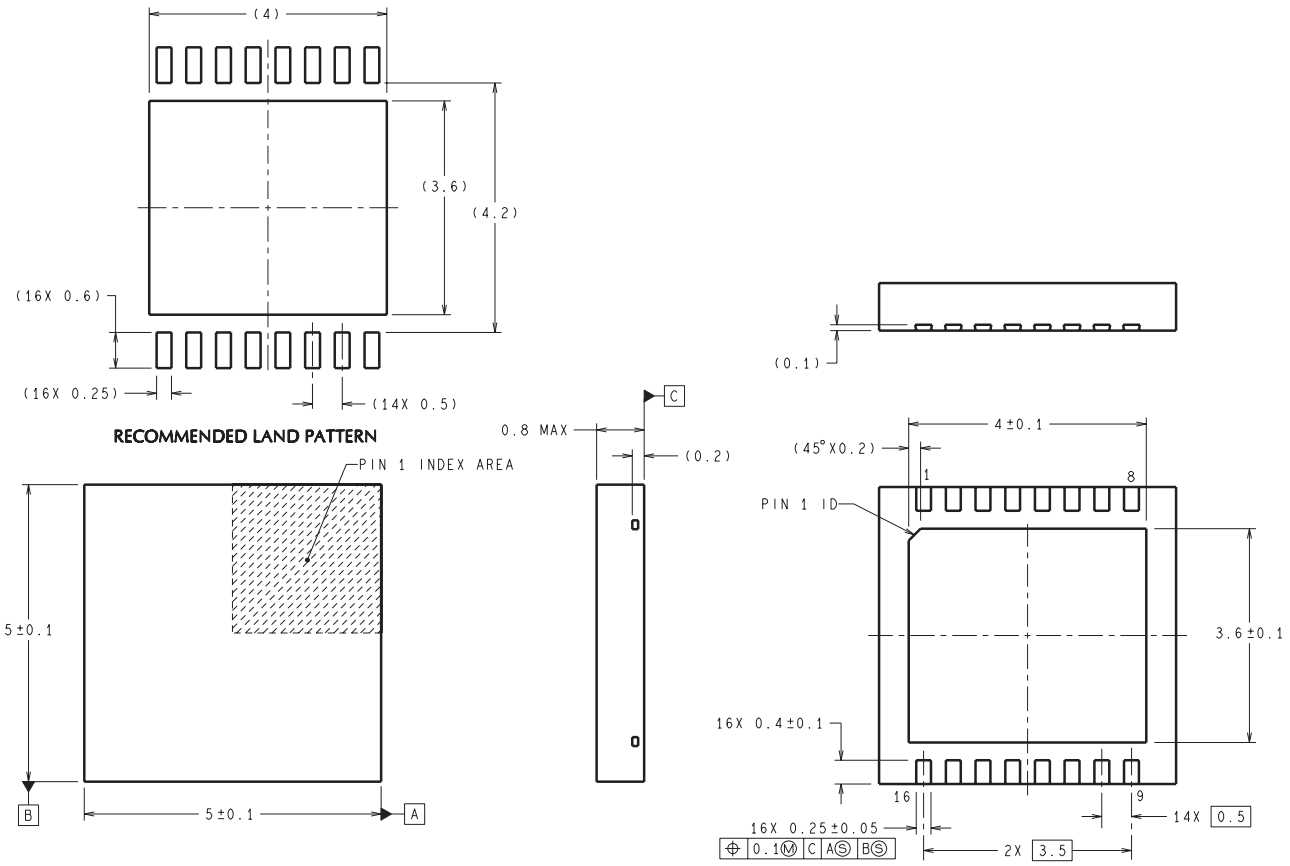
TUBE



*All dimensions are nominal

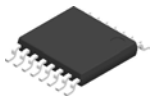
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM26400YMH/NOPB	PWP	HTSSOP	16	92	495	8	2514.6	4.06
LM26400YMH/NOPB.A	PWP	HTSSOP	16	92	495	8	2514.6	4.06

NHQ0016A



DIMENSIONS ARE IN MILLIMETERS

SDA16A (Rev A)

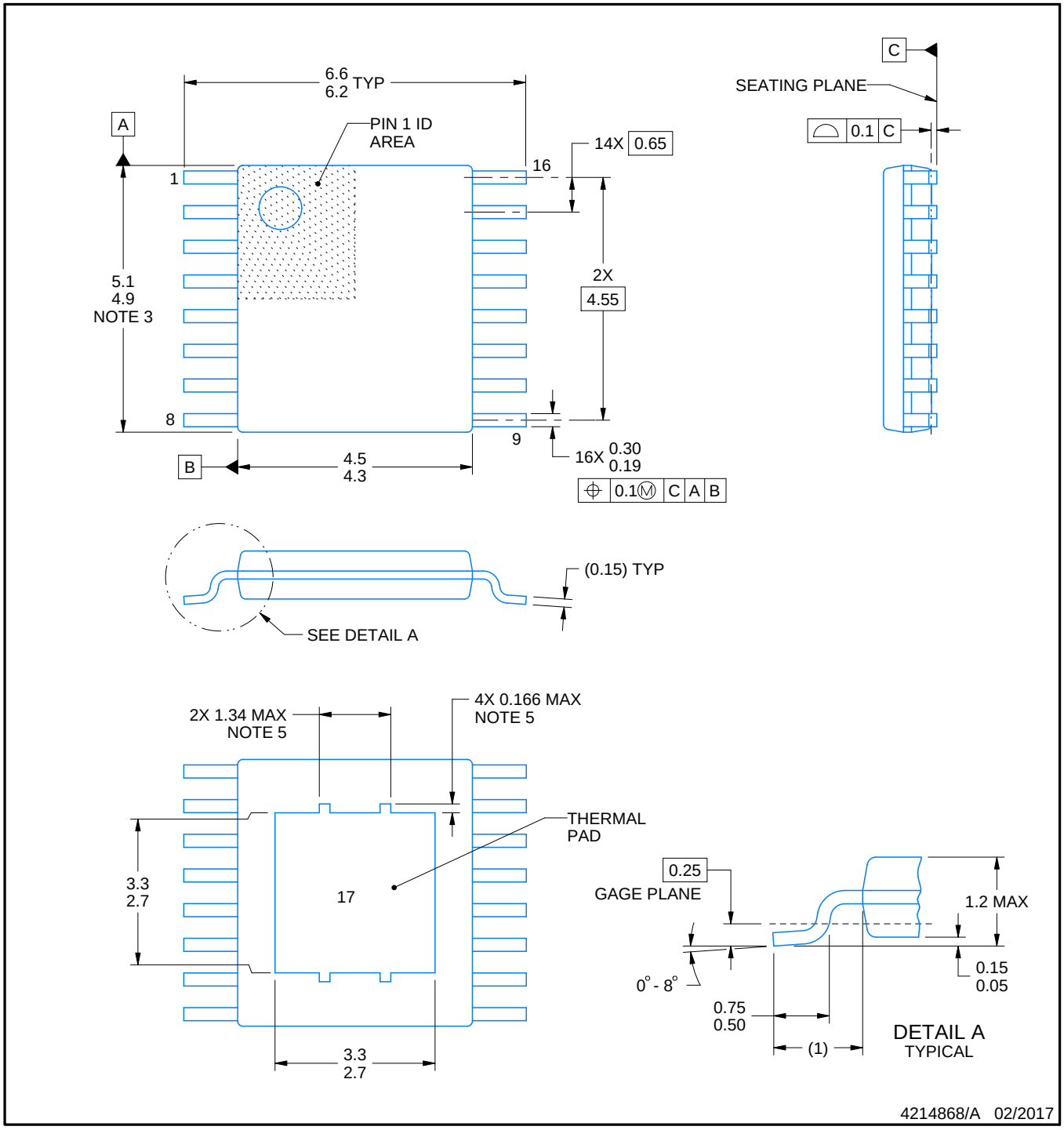


PACKAGE OUTLINE

PWP0016A

PowerPAD ™ HTSSOP - 1.2 mm max height

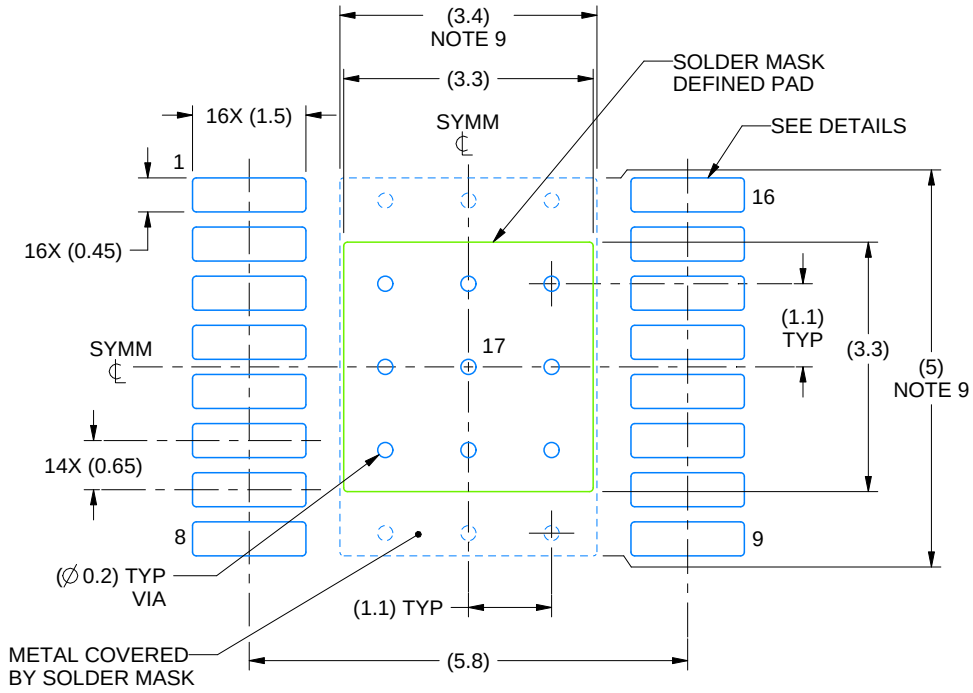
PLASTIC SMALL OUTLINE



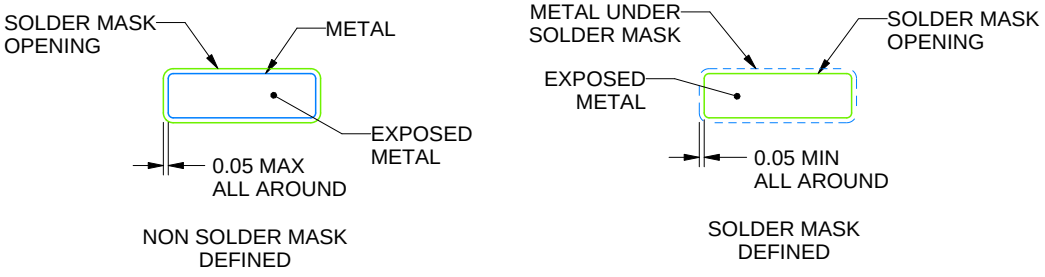
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:10X

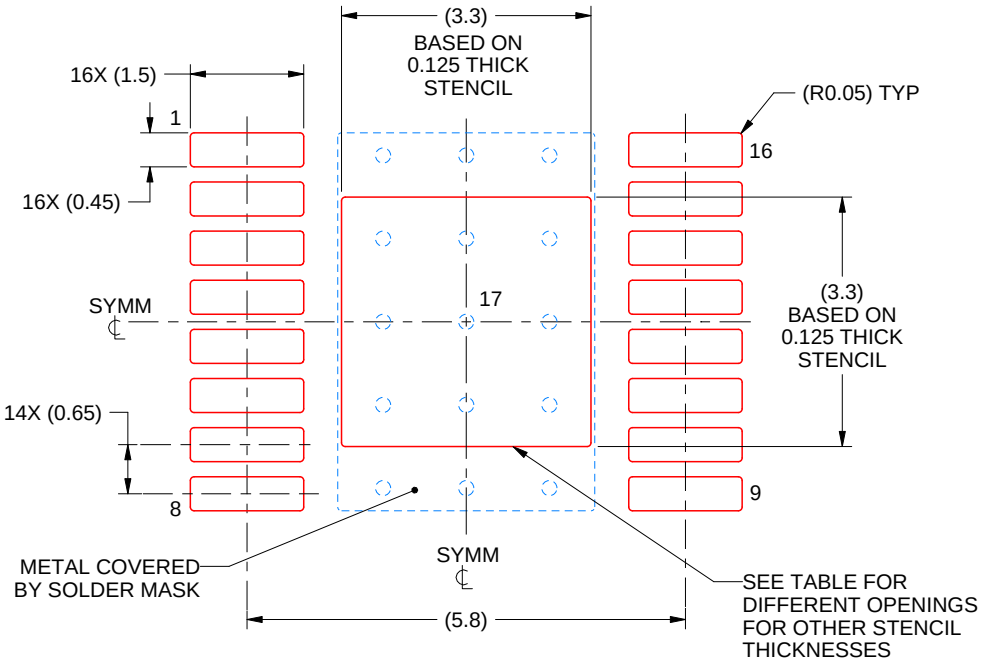


SOLDER MASK DETAILS
PADS 1-16

4214868/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.69 X 3.69
0.125	3.3 X 3.3 (SHOWN)
0.15	3.01 X 3.01
0.175	2.79 X 2.79

4214868/A 02/2017

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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