ISOW644x Robust-EMC, Reinforced, Quad-Channel Digital Isolator With Integrated DC-DC Converter

1 Features

- 150Mbps data rate
- Integrated DC-DC converter with best in class emissions.
- Emission optimized to meet CISPR 32 on 2 layer board
- Low output ripple: 30mV
- High efficiency output power
  - Selectable isolated output voltage of 3.3V or 5V
  - Efficiency at max load: 42.5%
  - Up to 0.55W output power
  - V_{ISO} accuracy of 10%
  - 5V to 5V: Max available load current = 110mA
  - 5V to 3.3V: Max available load current = 140mA
  - 3.3V to 3.3V: Max available load current = 60mA
- Low Propagation delay : 11ns typical
- Independent power supply for channel isolator and power converter
  - Logic supply (V_{DDL}): 2.25V to 5.5V
- Robust electromagnetic compatibility (EMC)
  - System-level ESD, EFT, and surge immunity
- High CMTI: 200kV/µs (Typ)
- Supports SPI up to: 25MHz at 5V, 20.8MHz at 3.3V
- Extended temperature range: –55°C to 125°C
- 16-pin wide body SOIC package
- Safety Related Certifications (Planned):
  - DIN EN IEC 60747-17 (VDE 0884-17)
  - UL 1577 component recognition program
  - IEC 62368-1, IEC 61010-1, IEC 60601-1 and GB 4943.1-2011 certifications

2 Applications

- Factory automation
- Motor control
- Grid infrastructure
- Medical equipment
- Test and measurement

3 Description

The ISOW644x family of devices are galvanically-isolated quad-channel digital isolator with an integrated high-efficiency power converter with best in class emissions. The integrated DC-DC converter provides up to 550mW of isolated power, eliminating the need for a separate isolated power supply in space-constrained isolated designs.

The high-efficiency of the power converter allows for operation at a wide operating ambient temperature range of –55°C to 125°C. The ISOW644x has been designed with enhanced protection features in mind, including soft-start to limit inrush current, over-voltage and under-voltage lock out, overload and short-circuit protection, and thermal shutdown.

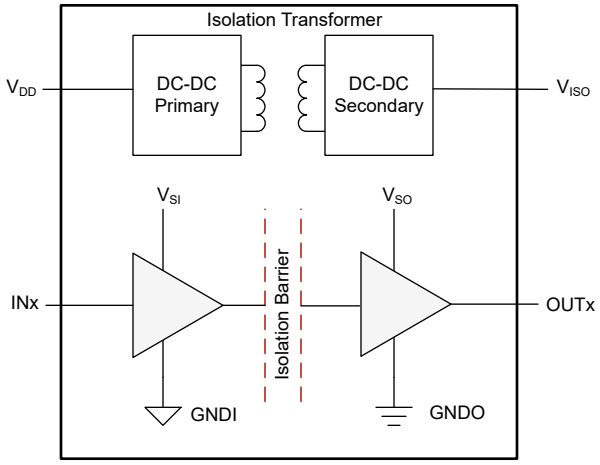
The ISOW644x family of devices provide high electromagnetic immunity while isolating CMOS or LVCMOS digital I/Os. The signal-isolation channel has a logic input and output buffer separated by a silicon dioxide (SiO_2) insulation barrier, whereas, power isolation uses on-chip transformers separated by thin film polymer as insulating material. There are five orderable configurations of four channel ISOW644x device using the last part number digit to note the number of reverse channels. For example, the ISOW6440 device has 4 forward channels and 0 reverse channels, while the ISOW6443 device has 1 forward channel and 3 reverse channels. If the input signal is lost, the default output is high for the ISOW644x devices without the F suffix and low for the ISOW644x devices with the F suffix. ISOW644xV can operate with different supply voltages on V_{DDL} and V_{DD} pins. These devices support 2.25V to 5.5V logic supply on V_{DDL} pin, that can be independent from the power converter supply (V_{DD}) of 3V to 5.5V.

Package Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)	PACKAGE SIZE(2)
ISOW6441	DWE (SOIC, 16)	10.30mm × 7.50mm	10.30mm × 10.30mm
ISOW6442			

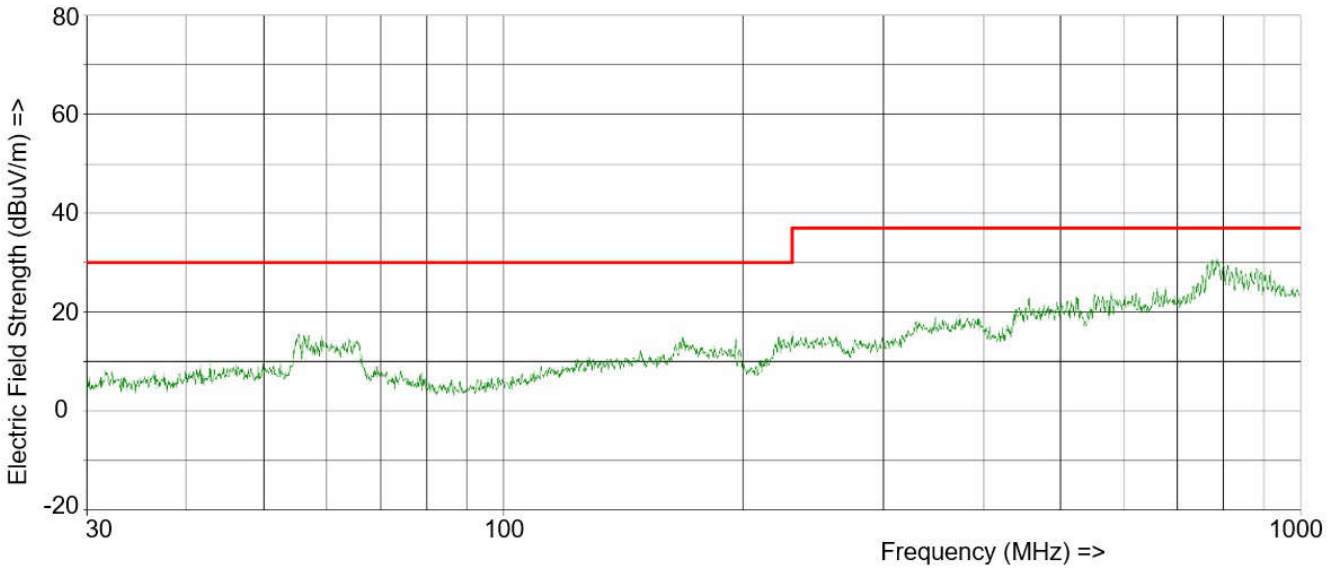
(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

ADVANCE INFORMATION



V_{DD} is the primary supply voltage referenced to GND1. V_{ISO} is the isolated supply voltage referenced to GND2.
V_{SI} and V_{SO} can be either V_{DD} or V_{ISO} depending on the channel direction.
V_{SI} is the input-side supply voltage referenced to GNDI and V_{SO} is the output-side supply voltage referenced to GNDO.

ISOW644x Simplified Schematic



ISOW644x CISPR-32 Radiated Emission With 140mA Load in 5V (Input) and 3V (Output) Mode

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4 Pin Configuration and Functions

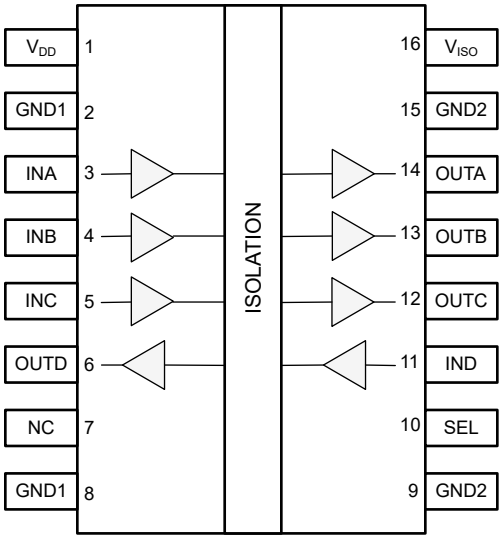

Figure 4-1. ISOW6441 DWE Package 16-Pin SOIC-WB Top View

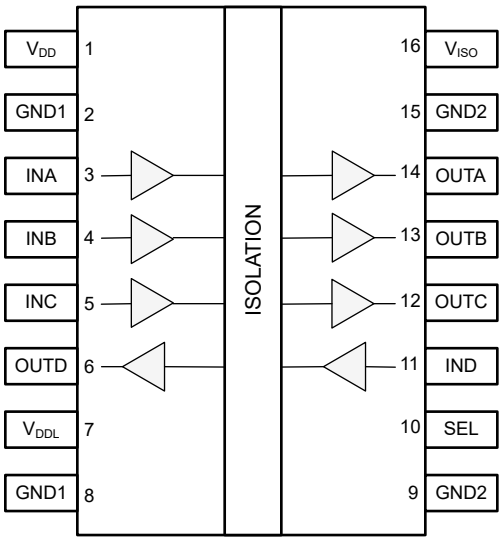

Figure 4-2. ISOW6441V DWE Package 16-Pin SOIC-WB Top View

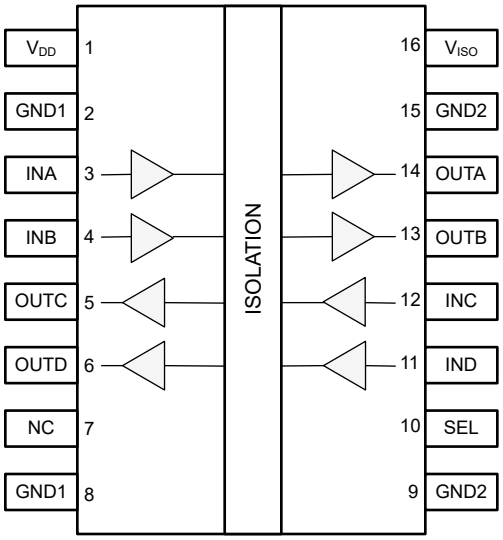

Figure 4-3. ISOW6442 DWE Package 16-Pin SOIC-WB Top View

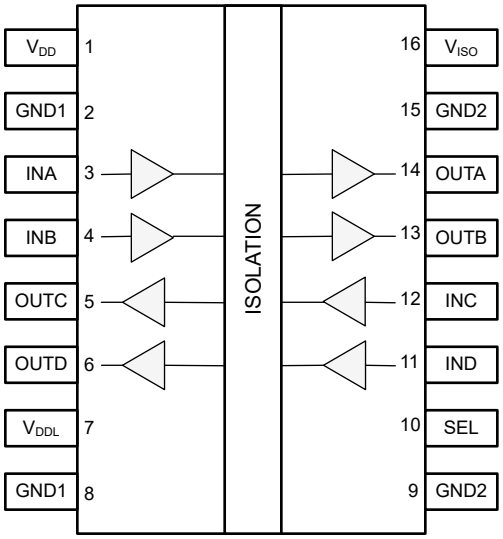

Figure 4-4. ISOW6442V DWE Package 16-Pin SOIC-WB Top View

Table 4-1. Pin Functions

PIN			Type[1]	DESCRIPTION
NAME	ISOW6441	ISOW6442		
GND1	2, 8	2, 8	—	Ground connection for V_{DD}
GND2	9, 15	9, 15	—	Ground connection for V_{ISO}
INA	3	3	I	Input channel A
INB	4	4	I	Input channel B
INC	5	12	I	Input channel C
IND	11	11	I	Input channel D
NC / V_{DDL}	7	7	—	Not connected for ISOW644x; and V_{DDL} for ISOW644xV. V_{DDL} is the supply for the Communication dies.
OUTA	14	14	O	Output channel A
OUTB	13	13	O	Output channel B
OUTC	12	5	O	Output channel C

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Table 4-1. Pin Functions (continued)

PIN			Type[1]	DESCRIPTION
NAME	ISOW6441	ISOW6442		
OUTD	6	6	O	Output channel D
SEL	10	10	I	V_{ISO} selection pin. V_{ISO} = V when SEL shorted to V_{ISO}. V_{ISO} = 3.3V, when SEL shorted to GND2 or when left floating. For more information see the *Section 7.4*.
V_{DD}	1	1	—	Supply voltage
V_{ISO}	16	16	—	Isolated supply voltage determined by SEL pin

(1) I = Input, O = Output, I/O = Input or Output

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
V_{DD}	Power converter supply voltage	–0.5	6	V
V_{ISO}	Isolated supply voltage	–0.5	6	V
V_{DDL}	Primary side logic supply voltage	–0.5	6	V
V	Voltage at INx, OUTx(3)	–0.5	6	V
	Voltage at SEL	–0.5	6	V
I_O	Maximum output current through data channels	–15	15	mA
T_J	Junction temperature	–55	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) V_{DD} and V_{DDL} are is with respect to the local ground pin (GND1 or GND2). All voltage values except differential I/O bus voltages are peak voltage values.
(3) V_{SI} = input side supply; Cannot exceed 6 V.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1) HBM ESD Classification Level 2	±2000	V
		Charged-device model (CDM), per AEC Q100-011 CDM ESD Classification Level C6	±1500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

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5.3 Recommended Operating Conditions

Over recommended operating conditions, typical values are at V_{DD} = V_{DDL} = 3.3 V and T_A =25°C (unless otherwise noted)

			MIN	NOM	MAX	UNIT
Power Converter						
V_{DD}	Power converter supply voltage	3.3 V operation	2.97	3.3	3.63	V
		5 V operation	4.5	5	5.5	V
$V_{DD(UVLO+)}$	Positive threshold when power converter supply is rising	Positive threshold when power converter supply is rising		2.65	2.86	V
$V_{DD(UVLO-)}$	Negative threshold when power converter supply is falling	Negative threshold when power converter supply is falling	2.44	2.56		V
$V_{DD(HYS)}$	Power converter supply voltage hysteresis	Power converter supply voltage hysteresis	78			mV
Channel Isolation						
V_{DDL} (3)	Channel logic supply voltage	2.5 V, 3.3 V, and 5 V operation	2.25		5.5	V
$V_{DDL(UVLO+)}$	Rising threshold of logic supply voltage			1.95	2.24	V
$V_{DDL(UVLO-)}$	Falling threshold of logic supply voltage		1.6	1.78		V
$V_{DDL(HYS)}$	Logic supply voltage hysteresis		100			mV
I_{OH}	High level output current(1)	V_{ISO} = 5 V	–4			mA
		V_{ISO} = 3.3 V	–2			mA
I_{OH}	High level output current(1)	V_{ISO} = 2.5 V	–1			mA
I_{OL}	Low level output current(1)	V_{ISO} = 5 V			4	mA
		V_{ISO} = 3.3 V			2	mA
I_{OL}	Low level output current(1)	V_{ISO} = 2.5 V			1	mA
V_{IH}	High-level input voltage(2)		0.7 × V_{SI}		V_{SI}	V
V_{IL}	Low-level input voltage(2)		0		0.3 × V_{SI}	V
DR	Data rate				150	Mbps
t_{PWRUP}	Channel isolator ready after power up			2.2		ms
T_A	Ambient temperature		–55		125	°C

(1) This current is for data output channel.
(2) V_{SI} = input side supply; V_{SO} = output side supply
(3) The channel outputs are in undetermined state when 1.89 V < V_{SI} < 2.25 V and 1.05 V < V_{SI} < 1.71 V

5.4 Thermal Information

THERMAL METRIC(1)		ISOW644x DWE (SOIC) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	58.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	28.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	32.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	18.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	31.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Maximum power dissipation (both sides)	V_{DD} = 5.5 V, V_{DDL} = 5.5 V, V_{ISO} = 5.5V, I_{ISO} = 90 mA, T_J = 150°C, T_A ≤ 80°C, C_L = 15 pF, input a 150Mbps 50% duty-cycle square wave			1.13	W
P_{D1}	Maximum power dissipation (side-1)				0.71	W
P_{D2}	Maximum power dissipation (side-2)				0.42	W

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5.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	External clearance(1)	Shortest terminal-to-terminal distance through air	>8	mm
CPG	External creepage(1)	Shortest terminal-to-terminal distance across the package surface	>8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance – capacitive signal isolation)	> 17	µm
		Minimum internal gap (internal clearance – transformer power isolation)	>120	
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	> 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 300 V_{RMS}	I-IV	
		Rated mains voltage ≤ 600 V_{RMS}	I-IV	
		Rated mains voltage ≤ 1000 V_{RMS}	I-III	
DIN VDE V 0884-11:2017-01				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	1500	V_{PK}
V_{IOWM}	Maximum working isolation voltage	AC voltage; Time dependent dielectric breakdown (TDDB) Test	1061	V_{RMS}
		DC voltage	1500	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$; t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$; t = 1 s (100% production)	7071	V_{PK}
V_{IMP}	Maximum impulse voltage ISOW644x(2)	Tested in air, 1.2/50-µs waveform per IEC 62368-1	8000	V_{PK}
V_{IOSM}	Maximum surge isolation voltage ISOW644x(2)	$V_{IOSM} \geq 1.3 \times V_{IMP}$; Tested in oil (qualification test), 1.2/50-µs waveform per IEC 62368-1	10400	V_{PK}
q_{pd}	Apparent charge(3)	Method a, after input/output safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10 s	≤ 5	pC
		Method a, after environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; ISOW644x: $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10 s	≤ 5	
		Method b1, at routine test (100% production) and preconditioning (type test), $V_{ini} = 1.2 \times V_{IOTM}$, t_{ini} = 1 s; ISOW644x: $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1 s	≤ 5	
C_{IO}	Barrier capacitance, input to output(4)	V_{IO} = 0.4 × sin (2πft), f = 1 MHz	3.5	pF
R_{IO}	Insulation resistance(4)	V_{IO} = 500 V, T_A = 25°C	> 10^{12}	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	> 10^{11}	
		V_{IO} = 500 V, T_S = 150°C	> 10^9	
	Pollution degree		2	
	Climatic category		55/125/21	
UL 1577				
$V_{ISO(UL)}$	Withstand isolation voltage	$V_{TEST} = V_{ISO(UL)}$= 5000 V_{RMS}, t = 60 s (qualification), $V_{TEST} = 1.2 \times V_{ISO(UL)}$ = 6000 V_{RMS}, t = 1 s (100% production)	5000	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a printed circuit board are used to help increase these specifications.
(2) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(3) Testing is carried out in oil to determine the intrinsic surge immunity of the isolation barrier.

(4) Apparent charge is electrical discharge caused by a partial discharge (pd).

5.7 Safety-Related Certifications

VDE	CSA	UL	CQC	TUV
Plan to certify according to DIN EN IEC 60747-17 (VDE 0884-17)	Plan to certify according to IEC 62368-1, IEC 61010-1 and IEC 60601	Plan to certify according to UL 1577 Component Recognition Program	Plan to certify according to GB4943.1	Plan to certify according to EN 61010-1 and EN 62368-1
Certificate planned	Certificate planned	Certificate planned	Certificate planned	Certificate planned

5.8 Safety Limiting Values

Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
16DWE						
I_S	Safety input, output, or supply current(1)	$R_{\theta JA}$ = 58.1°C/W, V_I = 5.5 V, T_J = 150°C, T_A = 25°C			390	mA
		$R_{\theta JA}$ = 58.1°C/W, V_I = 3.6 V, T_J = 150°C, T_A = 25°C			600	
P_S	Safety input, output, or total power(1)	$R_{\theta JA}$ = 58.1°C/W, T_J = 150°C, T_A = 25°C			2.15	W
T_S	Maximum safety temperature(1)				150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power respectively. The maximum limits of I_S and P_S should not be exceeded. These limits vary with the ambient temperature, T_A.
The junction-to-air thermal resistance, $R_{\theta JA}$, in the Thermal Information table is that of a device installed on a high-K test board for leaded surface-mount packages. Use the following equations to calculate the value for each parameter:
$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum allowed junction temperature.
$P_S = I_S \times V_I$, where V_I is the maximum input voltage.

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5.9 Electrical Characteristics - Power Converter

V_{DD} = 5V ±10% or 3V ±10%(over recommended operating conditions, unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD} = 5 V, V_{SEL} = V_{ISO}						
V_{ISO}	Isolated supply voltage	I_{ISO} = 0 to 55 mA	4.75	5	5.25	V
V_{ISO}	Isolated supply voltage	I_{ISO} = 0 to 110 mA	4.5	5	5.5	V
$V_{ISO(LINE)}$	DC line regulation	I_{ISO} = 55 mA, V_{DD} = 4.5 V to 5.5 V		18		mV/V
$V_{ISO(LOAD)}$	DC load regulation	I_{ISO} = 0 to 110 mA		1%		
EFF	Efficiency at maximum load current	I_{ISO} = 160 mA, C_{LOAD} = 0.1 µF || 10 µF; V_I = V_{DD} (ISOW644x); V_I =0 V (ISOW644x with F suffix).		42.5%		
$V_{ISO(RIP)}$	Output ripple on isolated supply (pk-pk)	20-MHz bandwidth, C_{LOAD} = 0.1 µF || 20 µF, I_{ISO} = 110 mA		30		mV
I_{ISO_SC}	DC current from V_{DD} supply under short circuit on V_{ISO}	V_{ISO} shorted to GND2		250		mA
V_{DD} = 5 V, V_{SEL} = GND2						
V_{ISO}	Isolated supply voltage	I_{ISO} = 0 to 70 mA	3.165	3.3	3.465	V
V_{ISO}	Isolated supply voltage	I_{ISO} = 0 to 140 mA	3	3.3	3.6	V
$V_{ISO(LINE)}$	DC line regulation	I_{ISO} = 70 mA, V_{DD} = 4.5 V to 5.5 V		13		mV/V
$V_{ISO(LOAD)}$	DC load regulation	I_{ISO} = 0 to 140 mA		1.5%		
EFF	Efficiency at maximum load current	I_{ISO} = 200 mA, C_{LOAD} = 0.1 µF || 10 µF; V_I = V_{DD} (ISOW644x); V_I =0 V (ISOW644x with F suffix).		36.3%		
$V_{ISO(RIP)}$	Output ripple on isolated supply (pk-pk)	20-MHz bandwidth , C_{LOAD} = 0.01 µF || 20 µF, I_{ISO} = 110 mA		25		mV
I_{ISO_SC}	DC current from V_{DD} supply under short circuit on V_{ISO}	V_{ISO} shorted to GND2		250		mA
V_{DD} = 3.3 V, V_{SEL} = GND2						
V_{ISO}	Isolated supply voltage	I_{ISO} = 0 to 30 mA	3.165	3.3	3.465	V
V_{ISO}	Isolated supply voltage	I_{ISO} = 0 to 60 mA	3	3.3	3.6	V
$V_{ISO(LINE)}$	DC line regulation	I_{ISO} = 30 mA, V_{DD} = 3.0 V to 3.6 V		11.5		mV/V
$V_{ISO(LOAD)}$	DC load regulation	I_{ISO} = 0 to 60 mA		0.8%		
EFF	Efficiency at maximum load current	I_{ISO} = 90 mA, C_{LOAD} = 0.1 µF || 10 µF; V_I = V_{DD} (ISOW644x); V_I =0 V (ISOW644x with F suffix).		40%		
$V_{ISO(RIP)}$	Output ripple on isolated supply (pk-pk)	20-MHz bandwidth, C_{LOAD} = 0.1 µF || 20 µF, I_{ISO} = 60 mA		15		mV
I_{ISO_SC}	DC current from V_{DD} supply under short circuit on V_{ISO}	V_{ISO} shorted to GND2		150		mA

5.10 Supply Current Characteristics - Power Converter

V_{DD} = 5 V ±10% or 3.3 V ±10%; VDDL Powered Internally (over recommended operating conditions unless otherwise noted).

PARAMETER	SUPPLY CURRENT	TEST CONDITIONS		MIN	TYP	MAX	UNIT
ISOW6441							
Power converter output current	I_{ISO}	V_{DD} = 5 V, V_{SEL} = V_{ISO} , V_I = V_{SI} V (ISOW6441); V_I = 0 (ISOW6441 with F suffix)	V_{DD} = 5 V±10% V_{SEL} = V_{ISO}	110	160		mA
Power converter supply current input	I_{DD}	V_{DD} = 5 V, V_{SEL} = V_{ISO} , V_I = V_{SI} V (ISOW6441); V_I = 0 (ISOW6441 with F suffix)	I_{LOAD} = 110 mA		260	340	mA
Power converter output current	I_{ISO}	V_{DD} = 5 V, V_{SEL} = GND2, V_I = V_{SI} V (ISOW6441); V_I = 0 (ISOW6441 with F suffix)	V_{DD} = 5 V±10% V_{SEL} = GND2	140	200		mA
Power converter supply current input	I_{DD}	V_{DD} = 5 V, V_{SEL} = GND2, V_I = V_{SI} V (ISOW6441); V_I = 0 (ISOW6441 with F suffix)	I_{LOAD} = 140 mA		250	310	mA
Power converter output current	I_{ISO}	V_{DD} = 3.3 V, V_{SEL} = GND2, V_I = V_{SI} V (ISOW6441); V_I = 0 (ISOW6441 with F suffix)	V_{DD} = 3.3 V±10% V_{SEL} = GND2	60	90		mA
Power converter supply current input	I_{DD}	V_{DD} = 3.3 V, V_{SEL} = GND2, V_I = V_{SI} V (ISOW6441); V_I = 0 (ISOW6441 with F suffix)	I_{LOAD} = 60mA		155	220	mA

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5.11 Electrical Characteristics Channel Isolator - V_{DD} = 5V, V_{DDL} = 5V, V_{ISO}=5V

V_{DDL}= 5V ±10% V_{DD} = 5V ±10% and V_{SEL}= V_{ISO} (over recommended operating conditions, unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Channel Isolation						
V_{ITH}	Input pin rising threshold				0.7 × V_{SI}	V
V_{ITL}	Input pin falling threshold		0.3 × V_{SI}			V
$V_{I(HYS)}$	Input pin threshold hysteresis (INx)		0.1 × V_{SI}			V
I_{IL}	Low level input current	V_{IL} = 0 at INx	–25			µA
I_{IH}	High level input current	V_{IH} = V_{SI} (1) at INx			25	µA
V_{OH}	High level output voltage	I_O = –4 mA, see Switching Characteristics Test Circuit and Voltage Waveforms	V_{SO} (1) – 0.4			V
V_{OL}	Low level output voltage	I_O = 4 mA, see Switching Characteristics Test Circuit and Voltage Waveforms			0.4	V
CMTI	Common mode transient immunity	V_I = V_{SI} or 0 V, V_{CM} = 1000 V; see Common-Mode Transient Immunity Test Circuit	100	200		kV/µs
C_i	Input Capacitance	V_I = V_{DDL} V_{DD} / 2 + 0.4×sin(2πft), f = 2 MHz, V_{DDL} V_{DD} = 5 V		2		pF

(1) V_{SI} = input side supply; V_{SO} = output side supply

5.12 Supply Current Characteristics Channel Isolator - V_{DD}, V_{DDL} = 5V, V_{ISO} = 5V

V_{DD}, V_{DDL} = 5 V ±10%, SEL shorted to VISO (over recommended operating conditions, unless otherwise specified), For devices without V_{DDL} pin the I_{DD} is sum of below mentioned I_{DD} and I_{DDL}

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISOW6441 Channel Supply Current							
Channel Supply current - DC signal	V_I = V_{CCI} (ISOW6441V); V_I = 0 V (ISOW6441V with F suffix)		I_{DDL}		3	4.6	mA
			I_{DD}		11	19	mA
	V_I = 0 V (ISOW6441V); V_I = V_{CCI} (ISOW6441V with F suffix)		I_{DDL}		9	10.6	mA
			I_{DD}		14	25	mA
Channel Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{DDL}		6	7.6	mA
			I_{DD}		13	22.5	mA
		10 Mbps	I_{DDL}		6	8.5	mA
			I_{DD}		16	27	mA
		100 Mbps	I_{DDL}		11.5	14.5	mA
			I_{DD}		47.3	73.5	mA
		150 Mbps	I_{DDL}				mA
			I_{DD}				mA
ISOW6442 Channel Supply Current							
Channel Supply current - DC signal	V_I = V_{CCI} (ISOW6442V); V_I = 0 V (ISOW6442V with F suffix)		I_{DDL}		2.5	3.1	mA
			I_{DD}		11.3	19.5	mA
	V_I = 0 V (ISOW6442V); V_I = V_{CCI} (ISOW6442V with F suffix)		I_{DDL}		6.4	7.5	mA
			I_{DD}		20.1	31.5	mA

V_{DD}, V_{DDL} = 5 V ±10%, SEL shorted to VISO (over recommended operating conditions, unless otherwise specified), For devices without V_{DDL} pin the I_{DD} is sum of below mentioned I_{DD} and I_{DDL}

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
Channel Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{DDL}		4.5	5.3	mA
			I_{DD}		16	25.5	mA
		10 Mbps	I_{DDL}		5.5	6.5	mA
			I_{DD}		18.2	29	mA
		100 Mbps	I_{DDL}		15.2	17.5	mA
			I_{DD}		40.1	61	mA
		150 Mbps	I_{DDL}				mA
			I_{DD}				mA

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5.13 Electrical Characteristics Channel Isolator - V_{DD} = 5V, V_{DDL} = 5V, V_{ISO}=3.3V

V_{DDL}= 5V ±10% V_{DD} = 5V ±10% and V_{SEL}= GND2 (over recommended operating conditions, unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Channel Isolation						
V_{ITH}	Input pin rising threshold				0.7 × V_{SI}	V
V_{ITL}	Input pin falling threshold		0.3 × V_{SI}			V
$V_{I(HYS)}$	Input pin threshold hysteresis (INx)		0.1 × V_{SI}			V
I_{IL}	Low level input current	V_{IL} = 0 at INx	–25			µA
I_{IH}	High level input current	V_{IH} = V_{SI} (1) at INx			25	µA
V_{OH}	High level output voltage	I_O = –2 mA, see Switching Characteristics Test Circuit and Voltage Waveforms	V_{SO} (1) – 0.3			V
V_{OL}	Low level output voltage	I_O = 2 mA, see Switching Characteristics Test Circuit and Voltage Waveforms			0.3	V
CMTI	Common mode transient immunity	V_I = V_{SI} or 0 V, V_{CM} = 1000 V; see Common-Mode Transient Immunity Test Circuit	100	200		kV/µs
C_i	Input Capacitance	V_I = V_{DDL} V_{DD} / 2 + 0.4×sin(2πft), f = 2 MHz, V_{DDL} V_{DD} = 5 V		2		pF

(1) V_{SI} = input side supply; V_{SO} = output side supply

5.14 Supply Current Characteristics Channel Isolator - V_{DD}, V_{DDL} = 5V, V_{ISO} = 3.3V

V_{DD} = 5 V ±10%, SEL shorted to GND (over recommended operating conditions, unless otherwise specified), For devices without V_{DDL} pin the I_{DD} is sum of below mentioned I_{DD} and I_{DDL}

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISOW6441 Channel Supply Current							
Channel Supply current - DC signal	V_I = V_{CCI} (ISOW6441V); V_I = 0 V (ISOW6441V with F suffix)		I_{DDL}		3	4.6	mA
			I_{DD}		9	14.5	mA
	V_I = 0 V (ISOW6441V); V_I = V_{CCI} (ISOW6441V with F suffix)		I_{DDL}		9	11	mA
			I_{DD}		12	18.5	mA
Channel Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{DDL}		6	7.6	mA
			I_{DD}		10	16.5	mA
		10 Mbps	I_{DDL}		6	8.5	mA
			I_{DD}		12	18.5	mA
		100 Mbps	I_{DDL}		12	14.5	mA
			I_{DDL}		12	14.5	mA
		150 Mbps	I_{DDL}				mA
			I_{DD}				mA
ISOW6442 Channel Supply Current							
Channel Supply current - DC signal	V_I = V_{CCI} (ISOW6442V); V_I = 0 V (ISOW6442V with F suffix)		I_{DDL}		2.5	3.1	mA
			I_{DD}		9	14.5	mA
	V_I = 0 V (ISOW6442V); V_I = V_{CCI} (ISOW6442V with F suffix)		I_{DDL}		6	7.5	mA
			I_{DD}		16	23.5	mA

V_{DD} = 5 V ±10%, SEL shorted to GND (over recommended operating conditions, unless otherwise specified), For devices without V_{DDL} pin the I_{DD} is sum of below mentioned I_{DD} and I_{DDL}

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
Channel Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{DDL}		5	5.5	mA
			I_{DD}		13	19	mA
		10 Mbps	I_{DDL}		6	6.5	mA
			I_{DD}		14	20.5	mA
		100 Mbps	I_{DDL}		15	17.5	mA
			I_{DD}		25	35	mA
		150 Mbps	I_{DDL}				mA
			I_{DD}				mA

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5.15 Electrical Characteristics Channel Isolator - V_{DD} = 3.3V, V_{DDL} = 3.3V, V_{ISO} = 3.3V

V_{DDL}= 3.3 V ±10% V_{DD}= 3.3 V ±10%(over recommended operating conditions, unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Channel Isolation						
V_{ITH}	Input pin rising threshold				0.7 × V_{SI}	V
V_{ITL}	Input pin falling threshold		0.3 × V_{SI}			V
$V_{I(HYS)}$	Input pin threshold hysteresis (INx)		0.1 × V_{SI}			V
I_{IL}	Low level input current	V_{IL} = 0 at INx	-25			µA
I_{IH}	High level input current	V_{IH} = V_{SI} (1) at INx			25	µA
V_{OH}	High level output voltage	I_O = –2 mA, see Switching Characteristics Test Circuit and Voltage Waveforms	V_{SO} (1) – 0.3			V
V_{OL}	Low level output voltage	I_O = 2 mA, see Switching Characteristics Test Circuit and Voltage Waveforms			0.3	V
CMTI	Common mode transient immunity	V_I = V_{SI} or 0 V, V_{CM} = 1000 V; see Common-Mode Transient Immunity Test Circuit	100	200		kV/µs
C_i	Input Capacitance	VI = V_{DDL} V_{DD} / 2 + 0.4×sin(2πft), f = 2MHz, V_{DDL} V_{DD} = 3.3V		2		pF

(1) V_{SI} = input side supply; V_{SO} = output side supply

5.16 Supply Current Characteristics Channel Isolator - V_{DD}, V_{DDL} = 3.3V, V_{ISO} = 3.3V

V_{DD}, V_{DDL} = 3.3 V ±10% (over recommended operating conditions, unless otherwise specified), For devices without V_{DDL} pin the I_{DD} is sum of below mentioned I_{DD} and I_{DDL}

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISOW6441 Channel Supply Current							
Channel Supply current - DC signal	V_I = V_{CCI} (ISOW6441V); V_I = 0 V (ISOW6441V with F suffix)		I_{DDL}		3.1	4.6	mA
			I_{DD}		11	20.5	mA
	V_I = 0 V (ISOW6441V); V_I = V_{CCI} (ISOW6441V with F suffix)		I_{DDL}		8.5	11	mA
			I_{DD}		15	27	mA
Channel Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{DDL}		5.8	7.5	mA
			I_{DD}		13	23.5	mA
		10 Mbps	I_{DDL}		6	8	mA
			I_{DD}		15	27	mA
		100 Mbps	I_{DDL}		10	12	mA
			I_{DD}		37	60	mA
		150 Mbps	I_{DDL}				mA
			I_{DD}				mA
ISOW6442 Channel Supply Current							
Channel Supply current - DC signal	V_I = V_{CCI} (ISOW6442V); V_I = 0 V (ISOW6442V with F suffix)		I_{DDL}		2.4	3	mA
			I_{DD}		11	20.5	mA
	V_I = 0 V (ISOW6442V); V_I = V_{CCI} (ISOW6442V with F suffix)		I_{DDL}		6	7.5	mA
			I_{DD}		20	34	mA

V_{DD}, V_{DDL} = 3.3 V ±10% (over recommended operating conditions, unless otherwise specified), For devices without V_{DDL} pin the I_{DD} is sum of below mentioned I_{DD} and I_{DDL}

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
Channel Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{DDL}		4.4	5.1	mA
			I_{DD}		16	27.5	mA
		10 Mbps	I_{DDL}		5	6	mA
			I_{DD}		18	30	mA
		100 Mbps	I_{DDL}		11	13	mA
			I_{DD}		33	52	mA
		150 Mbps	I_{DDL}				mA
			I_{DD}				mA

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5.17 Electrical Characteristics Channel Isolator - V_{DDL} = 2.5V

V_{DDL}= 2.5 V ±10% (over recommended operating conditions, unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Channel Isolation						
V_{ITH}	Input pin rising threshold				0.7 × V_{SI}	V
V_{ITL}	Input pin falling threshold		0.3 × V_{SI}			V
$V_{I(HYS)}$	Input pin threshold hysteresis (INx)		0.1 × V_{SI}			V
I_{IL}	Low level input current	V_{IL} = 0 at INx	-25			µA
I_{IH}	High level input current	V_{IH} = V_{SI} (1) at INx			25	µA
V_{OH}	High level output voltage	I_O = –2 mA, see Switching Characteristics Test Circuit and Voltage Waveforms	V_{SO} (1) – 0.3			V
V_{OL}	Low level output voltage	I_O = 2 mA, see Switching Characteristics Test Circuit and Voltage Waveforms			0.3	V
CMTI	Common mode transient immunity	V_I = V_{SI} or 0 V, V_{CM} = 1000 V; see Common-Mode Transient Immunity Test Circuit	100	200		kV/µs
C_i	Input Capacitance	VI = V_{DDL}/ 2 + 0.4×sin(2πft), f = 2MHz, V_{DDL} = 2.5V		2		pF

(1) V_{SI} = input side supply; V_{SO} = output side supply

5.18 Supply Current Characteristics Channel Isolator - V_{DDL} = 2.5V

V_{DDL}= 2.5 V ±10% (over recommended operating conditions, unless otherwise specified)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISOW6441 Channel Supply Current							
Channel Supply current - DC signal	V_I = V_{CCI} (ISOW6441); V_I = 0 V (ISOW6441 with F suffix)		I_{DDL}		3.5	4.5	mA
	V_I = 0 V (ISOW6441); V_I = V_{CCI} (ISOW6441 with F suffix)		I_{DDL}		9	10.5	mA
Channel Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{DDL}		6.3	7.4	mA
		10 Mbps	I_{DDL}		6.6	7.8	mA
		100 Mbps	I_{DDL}		9.2	10.7	mA
ISOW6442 Channel Supply Current							
Channel Supply current - DC signal	V_I = V_{CCI} (ISOW6442); V_I = 0 V (ISOW6442 with F suffix)		I_{DDL}		2.4	3	mA
	V_I = 0 V (ISOW6442); V_I = V_{CCI} (ISOW6442 with F suffix)		I_{DDL}		6.3	7.2	mA
Channel Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{DDL}		4.4	5.1	mA
		10 Mbps	I_{DDL}		4.9	5.7	mA
		100 Mbps	I_{DDL}		9.8	11.1	mA

5.19 Switching Characteristics - V_{DDL} = 5V, V_{ISO} = 5V

V_{ISO} = 5 V ±10%, V_{DD} V_{DDL} = 5 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Switching Characteristics Test Circuit and Voltage Waveforms	4.8	7.3	10.9	ns
PWD	Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$	See Switching Characteristics Test Circuit and Voltage Waveforms		0.3	2.2	ns
$t_{sk(o)}$	Channel-to-channel output skew time(2)	Same-direction channels			1.8	ns
$t_{sk(pp)}$	Part-to-part skew time(3)				3.2	ns
t_r	Output signal rise time	See Switching Characteristics Test Circuit and Voltage Waveforms			3	ns
t_f	Output signal fall time				3	ns
t_{DO}	Default output delay time from input power loss	Measured from the time V_{DDL} goes below 1.9 V at 10 mV/ns. See Switching Characteristics Test Circuit and Voltage Waveforms			0.1	µs
t_{ie}	Time interval error	2^{16} – 1 PRBS data at 100 Mbps;		0.3		ns

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

5.20 Switching Characteristics - V_{DDL} = 3.3V, V_{ISO} = 3.3V

V_{ISO} = 3.3 V ±10%, V_{DD} V_{DDL} = 3.3 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Switching Characteristics Test Circuit and Voltage Waveforms	4.8	7.8	13.3	ns
PWD	Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$	See Switching Characteristics Test Circuit and Voltage Waveforms		0.7	2.5	ns
$t_{sk(o)}$	Channel-to-channel output skew time(2)	Same-direction channels			1.8	ns
$t_{sk(pp)}$	Part-to-part skew time(3)				3.2	ns
t_r	Output signal rise time	See Switching Characteristics Test Circuit and Voltage Waveforms			4	ns
t_f	Output signal fall time				4	ns
t_{DO}	Default output delay time from input power loss	Measured from the time V_{DDL} goes below 1.9 V at 10 mV/ns. See Switching Characteristics Test Circuit and Voltage Waveforms			0.1	µs
t_{ie}	Time interval error	2^{16} – 1 PRBS data at 100 Mbps;		0.4		ns

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

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5.21 Switching Characteristics - V_{DDL} = 2.5V, V_{ISO} = 5V

V_{DDL} = 2.5 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Switching Characteristics Test Circuit and Voltage Waveforms	5	7.7	16	ns
PWD	Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$	See Switching Characteristics Test Circuit and Voltage Waveforms		1	3	ns
$t_{sk(o)}$	Channel-to-channel output skew time(2)	Same-direction channels			1.8	ns
$t_{sk(pp)}$	Part-to-part skew time(3)				3.2	ns
t_r	Output signal rise time	See Switching Characteristics Test Circuit and Voltage Waveforms			5	ns
t_f	Output signal fall time				5	ns
t_{DO}	Default output delay time from input power loss	Measured from the time V_{IO} or V_{ISOIN} goes below V_{DDL} goes below 1.9 V. See Switching Characteristics Test Circuit and Voltage Waveforms			0.1	µs
t_{ie}	Time interval error	2^{16} – 1 PRBS data at 100 Mbps;		0.7		ns

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

5.22 Switching Characteristics - V_{DDL} = 2.5V, V_{ISO} = 3.3V

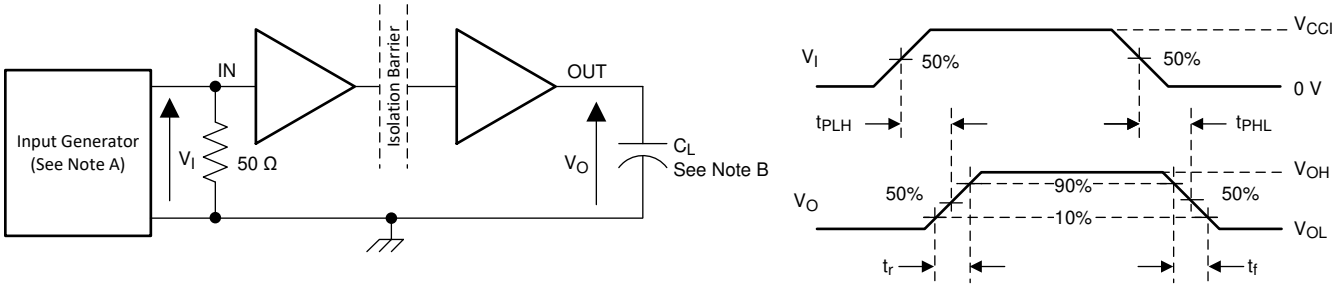
V_{DDL} = 2.5 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Switching Characteristics Test Circuit and Voltage Waveforms	6	8.75	16.5	ns
PWD	Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$	See Switching Characteristics Test Circuit and Voltage Waveforms		0.36	3	ns
$t_{sk(o)}$	Channel-to-channel output skew time(2)	Same-direction channels			1.8	ns
$t_{sk(pp)}$	Part-to-part skew time(3)				3.2	ns
t_r	Output signal rise time	See Switching Characteristics Test Circuit and Voltage Waveforms			5	ns
t_f	Output signal fall time				5	ns
t_{DO}	Default output delay time from input power loss	Measured from the time V_{DDL} goes below 1.9 V at 10 mV/ns. See Switching Characteristics Test Circuit and Voltage Waveforms			0.1	µs
t_{ie}	Time interval error	2^{16} – 1 PRBS data at 100 Mbps;		0.7		ns

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

6 Parameter Measurement Information

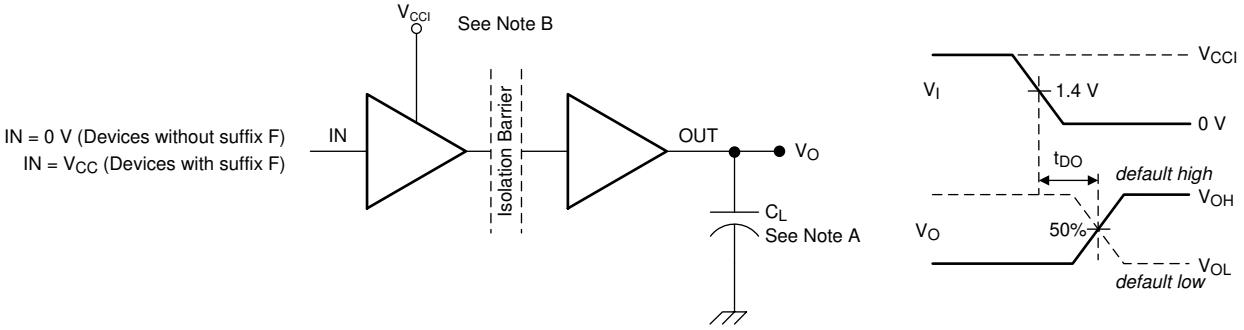
In the below images, V_{CCI} and V_{CCO} refers to the power supplies V_{DD} and V_{ISO}, respectively.



A. C_L = 15pF and The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50kHz, 50% duty cycle, t_r ≤ 3ns, t_f ≤ 3ns, Z_O = 50Ω. At the input, 50Ω resistor is required to terminate Input Generator signal. The 50Ω resistor is not needed in actual application.

B. B. C_L = 15pF and includes instrumentation and fixture capacitance within ±20%.

Figure 6-1. Switching Characteristics Test Circuit and Voltage Waveforms



Note

A. C_L = 15pF and includes instrumentation and fixture capacitance within ±20%.

Note

B. Power Supply Ramp Rate = 10mV/ns.

Figure 6-2. Default Output Delay Time Test Circuit and Voltage Waveforms

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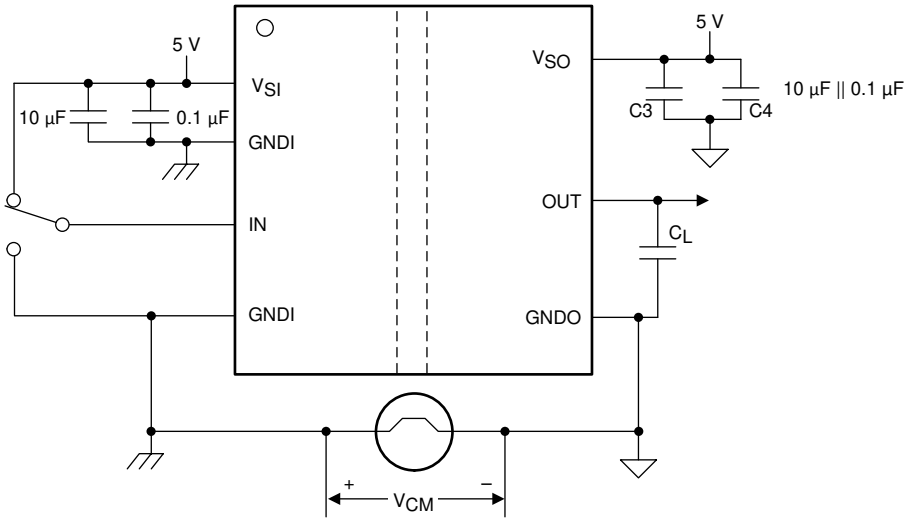

Note

C_L = 15pF and includes instrumentation and fixture capacitance within ±20%.

Note

Pass-fail criteria: Outputs must remain stable.

Figure 6-3. Common-Mode Transient Immunity Test Circuit

7 Detailed Description

7.1 Overview

The ISOW644x family of devices have low-noise, low-emissions isolated DC-DC converter, and four high-speed isolated data channels. Section 7.2 shows the functional block diagram of the ISOW644x device.

7.1.1 Power Isolation

The integrated isolated DC-DC converter uses advanced circuit and on-chip layout techniques to reduce radiated emissions and achieve up to 43.5% typical efficiency. The integrated transformer uses thin film polymer as the insulation barrier. Output voltage of power converter can be controlled to 3.3V or 5V using V_{SEL} pin. The output voltage, V_{ISO}, is monitored and feedback information is conveyed to the primary side for regulation. The duty cycle of the primary switching stage is adjusted accordingly. The fast feedback control loop of the power converter provides low overshoots and undershoots during load transients. Undervoltage lockout (UVLO) with hysteresis is integrated on the V_{DD} supply V_{DD} and V_{DDL} supplies which provides robust fails-safe system performance under noisy conditions. An integrated soft-start mechanism verifies controlled inrush current and avoids any overshoot on the output during power up.

7.1.2 Signal Isolation

The integrated signal isolation channels employ an ON-OFF keying (OOK) modulation scheme to transmit the digital data across a silicon-dioxide based isolation barrier. The transmitter sends a high frequency carrier across the barrier to represent one state and sends no signal to represent the other state. The receiver demodulates the signal after signal conditioning and produces the output through a buffer stage. The signal-isolation channels incorporate advanced circuit techniques to maximize the CMTI performance and minimize the radiated emissions from the high frequency carrier and IO buffer switching. To keep any noise coupling from power converter away from signal path, power supplies on side 1 for power converter (V_{DD})and signal path(V_{DDL}) are kept separate. For more details, refer to the Layout Guidelines section.

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7.2 Functional Block Diagram

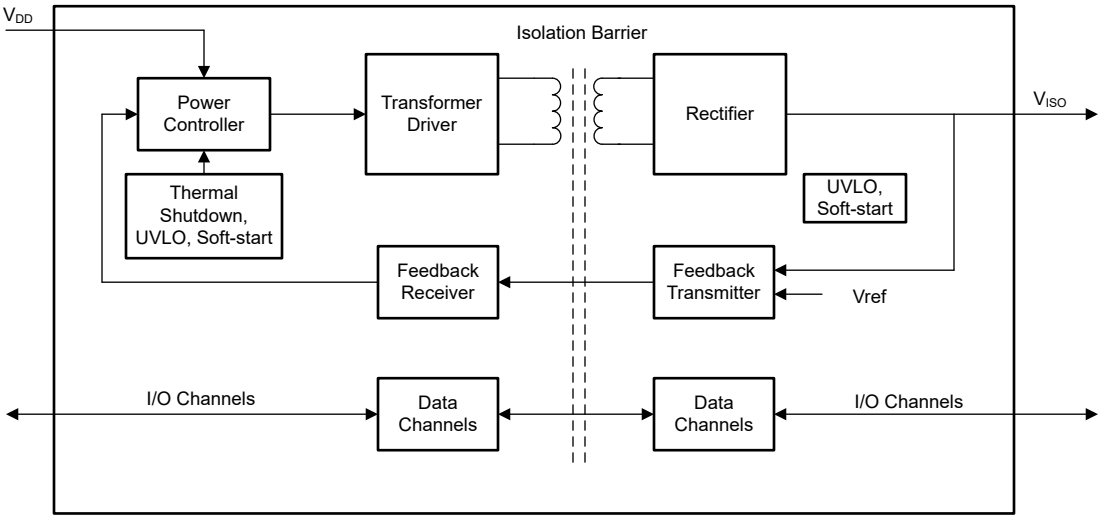

Figure 7-1. ISOW644x Block Diagram

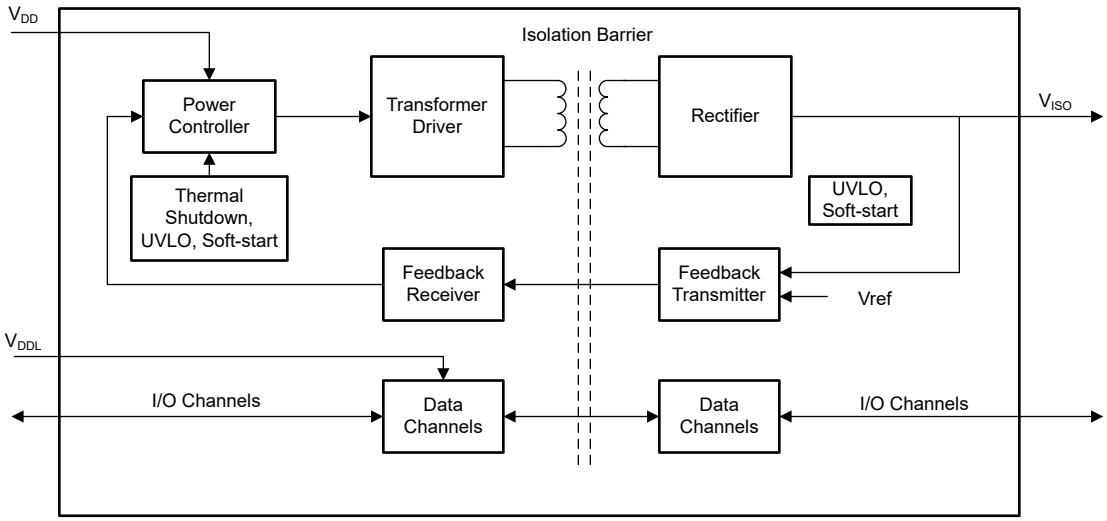

Figure 7-2. ISOW644xV Block Diagram

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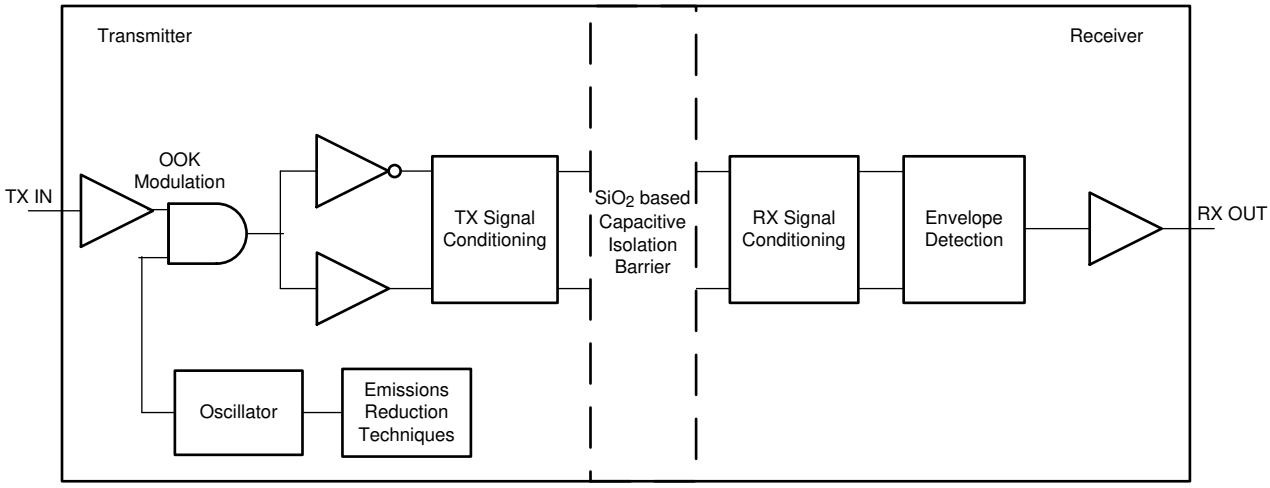

Figure 7-3. Conceptual Block Diagram of the Data Channel

Figure 7-4 shows a conceptual detail of how the OOK scheme works.

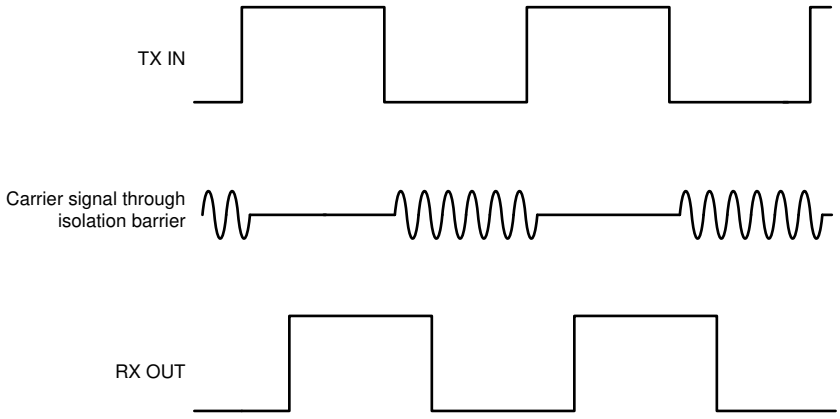

Figure 7-4. On-Off Keying (OOK) Based Modulation Scheme

7.3 Feature Description

The following table shows an overview of the device features.

Table 7-1. ISOW644xV Device Features

PART NUMBER [1]	CHANNEL DIRECTION	MAXIMUM DATA RATE	DEFAULT OUTPUT STATE	RATED ISOLATION [2]
ISOW6441V	3 forward, 1 reverse	150Mbps	High	$5kV_{RMS}$ / $7071V_{PK}$
ISOW6442V	2 forward, 2 reverse		High	

1. The F suffix is part of the orderable part number. See the *Section 11* section for the full orderable part number.
2. For detailed isolation ratings, see the Section 5.7 table.

7.3.1 Electromagnetic Compatibility (EMC) Considerations

The ISOW644x devices use emissions reduction schemes for the internal oscillator and advanced internal layout scheme to minimize radiated emissions at the system level.

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Many applications in harsh industrial environment are sensitive to disturbances such as electrostatic discharge (ESD), electrical fast transient (EFT), surge and electromagnetic emissions. These electromagnetic disturbances are regulated by international standards such as IEC 61000-4x and CISPR 32. Although system-level performance and reliability depends, to a large extent, on the application board design and layout, the ISOW644x device incorporate many chip-level design improvements for overall system robustness. Some of these improvements include:

- Robust ESD protection cells for input and output signal pins and inter-chip bond pads.
- Low-resistance connectivity of ESD cells to supply and ground pins.
- Enhanced performance of high voltage isolation capacitor for better tolerance of ESD, EFT and surge events.
- Bigger on-chip decoupling capacitors to bypass undesirable high energy signals through a low impedance path.
- PMOS and NMOS devices isolated from each other by using guard rings to avoid triggering of parasitic SCRs.
- Reduced common mode currents across the isolation barrier by providing purely differential internal operation.
- Power path and signal path separated to minimize internal high frequency coupling and allowing for an external filtering knob using ferrite beads available to further reduce emissions
- Reduced power converter switching frequency to 25Mhz to reduce strength of high frequency components in emissions spectrum

7.3.2 Power-Up and Power-Down Behavior

The ISOW644x device device has built-in UVLO on the V_{DD} and V_{DDL} supplies with positive-going and negative-going thresholds and hysteresis. The power converter supply (V_{DD}) needs to be above UVLO for the power converter to work. Logic supply (V_{DDL}) needs to be above UVLO for the signal path to work.

When the V_{DD} voltage crosses the positive-going UVLO threshold during power-up, the DC-DC converter initializes and the power converter duty cycle is increased in a controlled manner. This soft-start scheme limits primary peak currents drawn from the V_{DD} supply and charges the V_{ISO} output in a controlled manner, avoiding overshoots. Outputs of the isolated data channels are in an indeterminate state until the V_{DD} voltage crosses the positive-going UVLO threshold. When the UVLO positive-going threshold is crossed on the secondary side V_{ISO} pin, the feedback data channel starts providing feedback to the primary controller. The regulation loop takes over and the isolated data channels go to the normal state defined by the respective input channels or the default states. Design must consider a sufficient time margin (typically 10ms with 10µF load capacitance) to allow this power up sequence before valid data channels are accounted for system functionality.

When V_{DD} power is lost, the primary side DC-DC controller turns off when the UVLO lower threshold is reached. The V_{ISO} capacitor then discharges depending on the external load. The isolated data outputs on the V_{ISO} side are returned to the default state for the brief time that the V_{ISO} voltage takes to discharge to zero.

7.3.3 Protection Features

The ISOW644x devices have multiple protection features to create a robust system level design.

- The device is protected against output overload and short circuit. Output voltage starts dropping when the power converter is not able to deliver the current demanded during overload conditions. For a V_{ISO} short-circuit to ground, the duty cycle of the converter is limited to help protect against any damage.
- Thermal protection is also integrated to help prevent the device from getting damaged during overload and short-circuit conditions on the isolated output. Under these conditions, the device temperature starts to increase. When the temperature goes above 165°C, thermal shutdown activates and the primary controller turns off which removes the energy supplied to the V_{ISO} load, which causes the device to cool off. When the junction temperature goes below 150°C, the device starts to function normally. If an overload or output short-circuit condition prevails, this protection cycle is repeated. Care must be taken in the design to prevent the device junction temperatures from reaching such high values.

7.4 Device Functional Modes

Table 7-2 lists the supply configurations for these devices.

Table 7-2. Supply Configuration Function Table

V_{DD}	VSEL	V_{ISO}
5V	High (shorted to V_{ISO})	5V
5V	Low (shorted to GND2)	3.3V
3.3V	Low (shorted to GND2)	3.3V
3.3V	High (shorted to V_{ISO})	Not supported

Table 7-3. Device Functional Modes

INPUT SUPPLY (V_{DD})	INPUT (INx)	OUTPUT (OUTx)	COMMENTS
PU	H	H	Output channel assumes the logic state of the input
	L	L	
	Open	Default	Default mode(1) When INx is open, the corresponding output channel assumes logic based on default output mode of selected version
PD	X	Undetermined	

(1) In the default condition, the output is high for ISOW644x and low for ISOW644x with the F suffix.

Table 7-4 lists the channel isolators functional modes for these devices.

Table 7-4. Isolation Channel Function Table

CHANNEL INPUT SUPPLY (V_{CCI}) (1)	CHANNEL OUTPUT SUPPLY (V_{CCO}) (1)	INPUT (INx)	OUTPUT (OUTx)	COMMENTS
PU	PU	H	H	Normal Operation: A channel output assumes the logic state of the input.
		L	L	
		Open	Default	Default mode(2): When INx is open, the corresponding channel output goes to the default logic state.
		X	Z and Default	A low value of output enable causes the outputs of the same side to be high impedance and the output of opposite side to be fail-safe default state.
PD	PU	X	Default	Default mode(2): When V_{CCI} is unpowered, a channel output assumes the logic state based on the selected default option. When V_{CCI} transitions from unpowered to powered-up, a channel output assumes the logic state of the input. When V_{CCI} transitions from powered-up to unpowered, channel output assumes the selected default state.

(1) V_{CCI} = Input-side V_{DD} V_{DDL} or V_{ISO}; V_{CCO} = Output-side V_{DD} V_{DDL} or V_{ISO}; PU = Powered up (V_{DD} > 2.86V, V_{DDL} > 2.25V, V_{ISO}> 3V); PD = Powered down (V_{DD}<2.44V, V_{DDL} < 1.6V, V_{ISO} < 3V); X = Irrelevant; H = High level; L = Low level.
(2) In the default condition, the output is high for the ISOW644x device and low with the F suffix.

ADVANCE INFORMATION

7.4.1 Device I/O Schematics

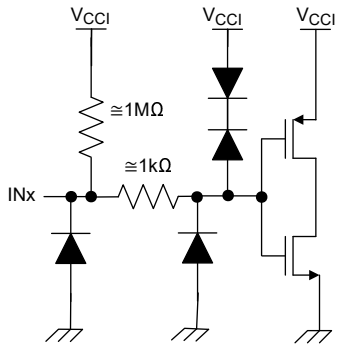

Figure 7-5. Input (INx) Default High (Device Without F Suffix Device) Schematics

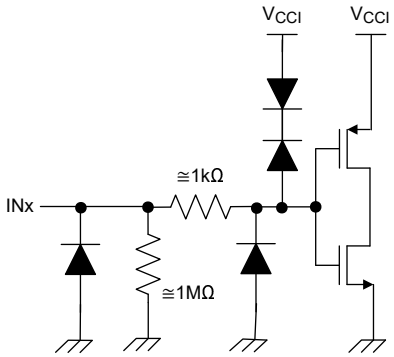

Figure 7-6. Input (INx) Default Low (Device With F Suffix Device) Schematics

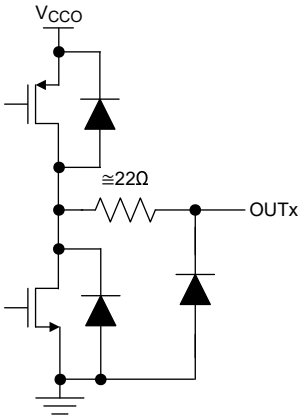

Figure 7-7. Output (OUTx) Schematics

ADVANCE INFORMATION

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The device is a high-performance, quad channel digital isolator with integrated DC-DC converter. Typically digital isolators require two power supplies isolated from each other to power up both sides of device. Due to the integrated DC-DC converter in the device, the isolated supply is generated inside the device that can be used to power isolated side of the device and peripherals on isolated side, thus saving board space. The device uses single-ended CMOS-logic switching technology. When designing with digital isolators, keep in mind that because of the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is Microcontroller, UART or SPI), and a data converter or a line transceiver, regardless of the interface type or standard.

The device is designed for applications that have limited board space and desire more integration. The device is also designed for very high voltage applications, where power transformers meeting the required isolation specifications are bulky and expensive.

8.2 Typical Application

The following table shows the typical schematic for SPI isolation.

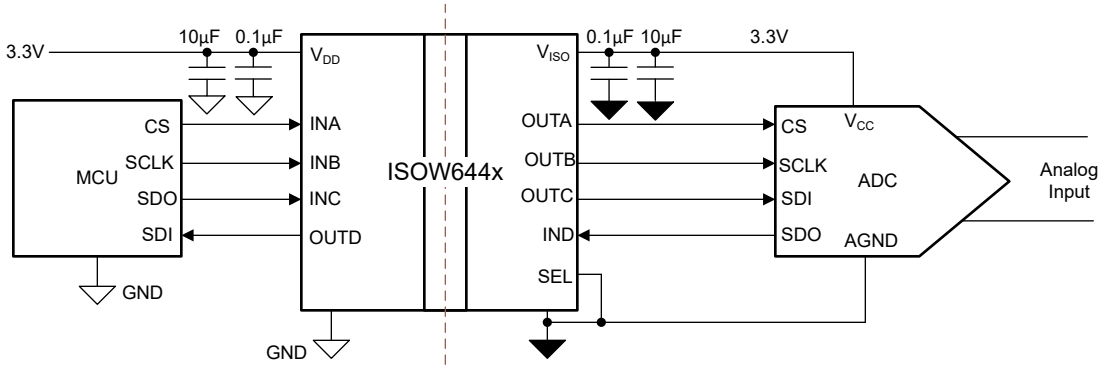

Figure 8-1. Isolated Power and SPI for ADC Sensing Application With ISOW6441

ADVANCE INFORMATION

8.2.1 Design Requirements

To design with this device, use the parameters listed in Table 8-1.

Table 8-1. Design Parameters

PARAMETER	VALUE
V_{DD} input voltage	3V to 5.5V
V_{DDL} input voltage	2.25V to 5.5V
V_{DD} decoupling capacitors	10µF + 1µF + 0.01µF + optional additional capacitance
V_{DDL} decoupling capacitors	0.1µF + optional additional capacitance
V_{ISO} decoupling capacitors	10µF + 1µF + 0.01µF + optional additional capacitance

Because of very-high current flowing through the ISOW6441 device V_{DD} and V_{ISO} supplies, higher decoupling capacitors typically provide better noise and ripple performance. Although a 10µF capacitor is adequate, higher decoupling capacitors (such as 47µF) on both the V_{ISO} and V_{DD} pins to the respective grounds are strongly recommended to achieve the best performance.

8.2.2 Detailed Design Procedure

The devices requires specific placement of external bypass capacitors and ferrite beads to operate at high performance. These low-ESR ceramic bypass capacitors must be placed as close to the chip pads as possible.

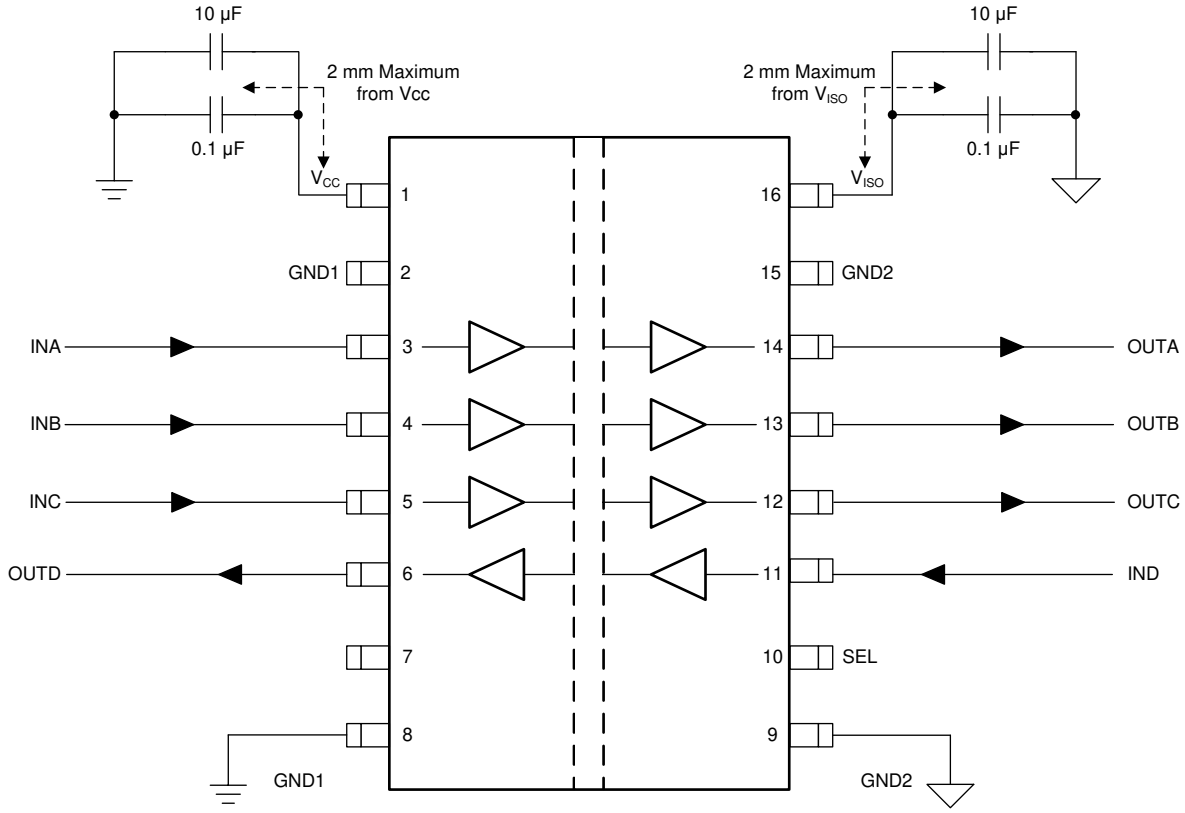

Figure 8-2. Typical ISOW6441 Circuit Hook-Up

8.3 Power Supply Recommendations

To help make sure that operation is reliable at data rates and supply voltages, adequate decoupling capacitors must be located as close to supply pins as possible.

The input supply (V_{DDL} andV_{DD}) must have an appropriate current rating to support output load and switching at the maximum data rate required by the end application. For more information, refer to the Section 8.2 section.

For an output load current of 110mA, have >600mA of input current limit and for lower output load currents, the input current limit can be proportionally lower.

8.4 Layout

8.4.1 Layout Guidelines

A low-cost two-layer PCB is sufficient to achieve good EMC performance:

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of the inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100pF/in^2.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links typically have margin to tolerate discontinuities such as vias.
- For Best EMC performance the 2 GND 1 pins must be shorted to the GND 1 plane, and similarly the 2 GND 2 pins must be shorted to the GND 2 plane.

If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep the layers symmetrical. This makes the stack mechanically stable and prevents warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

Because the device has no thermal pad to dissipate heat, the device dissipates heat through the respective GND pins. Verify that enough copper is present on both GND pins to prevent the internal junction temperature of the device from rising to unacceptable levels.

Below Layout Example shows the recommended placement and routing of device bypass capacitors. Below guidelines must be followed to meet application EMC requirements:

- High frequency bypass capacitors 100nF must be placed close to V_{DD} and V_{ISO} pins, less than 1mm distance away from device pins. This is very essential for optimised radiated emissions performance. Verify that these capacitors are 0402 size so that the capacitors offer least inductance (ESL).
- Bulk capacitors of at least 10µF must be placed on power converter input (V_{DD})
- Traces on V_{DD} and GND1 must be symmetric till bypass capacitors.
- Following the layout guidelines of EVM as much as possible is highly recommended for a low radiated emissions design.

8.4.1.1 PCB Material

For digital circuit boards operating at less than 150Mbps, (or rise and fall times greater than 1ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit board. This PCB is preferred over cheaper alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.

ADVANCE INFORMATION

8.4.2 Layout Example

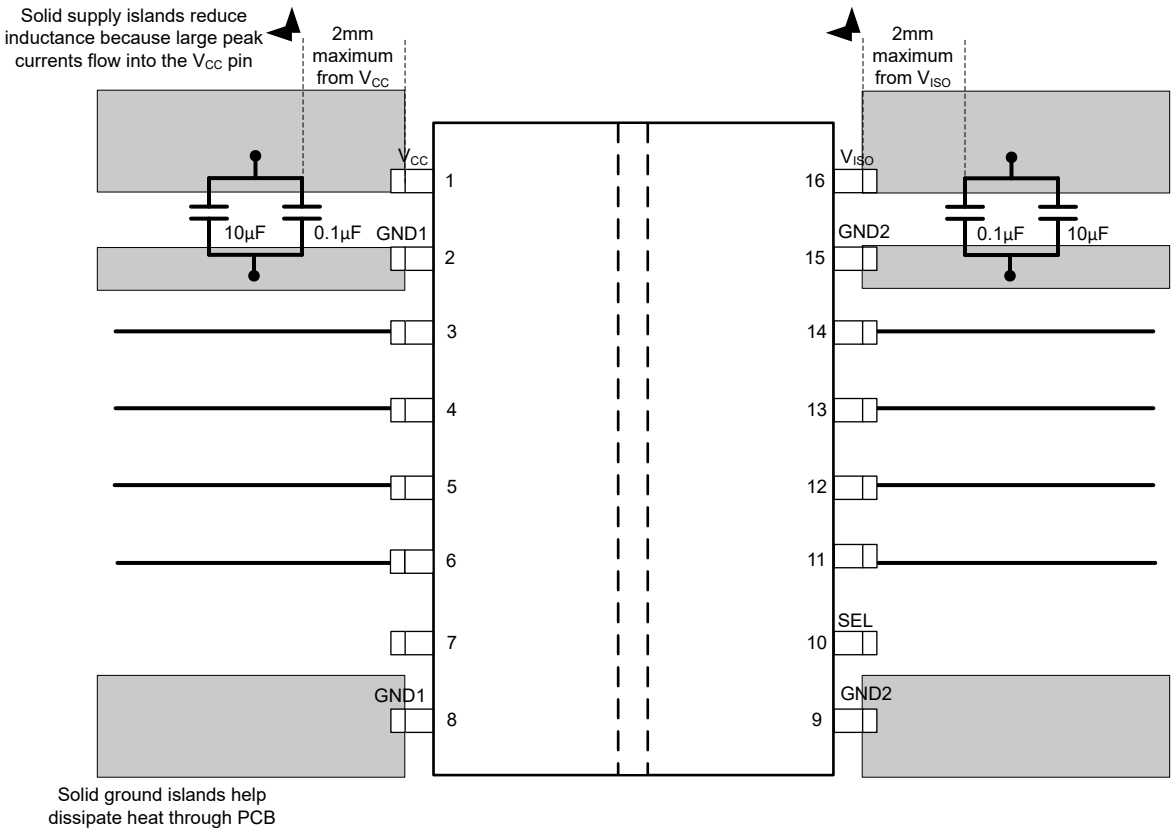

Figure 8-3. Layout example

ADVANCE INFORMATION

9 Device and Documentation Support

9.1 Device Support

9.1.1 Development Support

For development support, refer to:

- Isolated RS-485 With Integrated Signal and Power Reference Design
- Isolated RS-232 With Integrated Signal and Power Reference Design

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Digital Isolator Design Guide*, application note
- Texas Instruments, *Isolation Glossary*, application note

9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.5 Trademarks

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9.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
November 2025	*	Initial Release

ADVANCE INFORMATION

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/Ball material (4)	MSL rating/Peak reflow (5)	Op temp (°C)	Part marking (6)
XISOW6441DWER	Pre-Production		SOIC (DWE) | 16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	XISOW6441
XISOW6442DWER	Pre-Production		SOIC (DWE) | 16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	XISOW6442

(1) **Status:** For more details on status, see our product life cycle.
(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.
(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

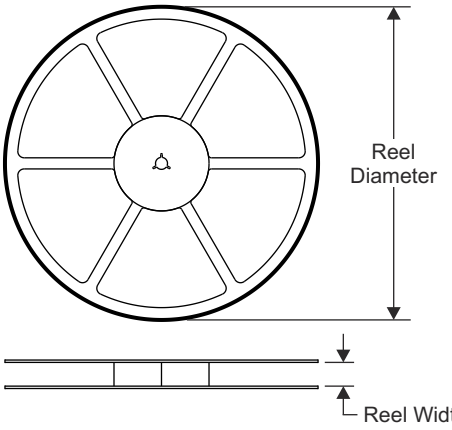
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

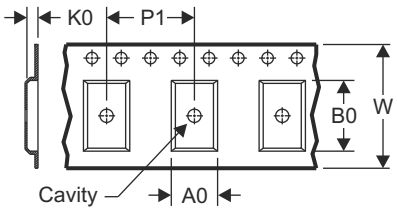
ADVANCE INFORMATION

11.1 Tape and Reel Information

REEL DIMENSIONS

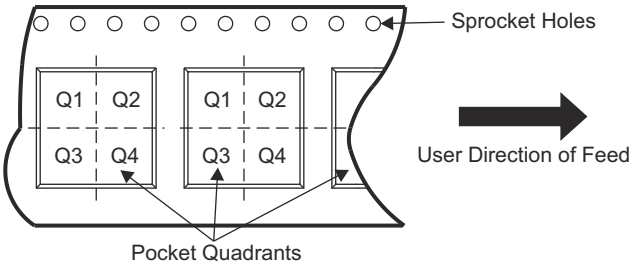


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

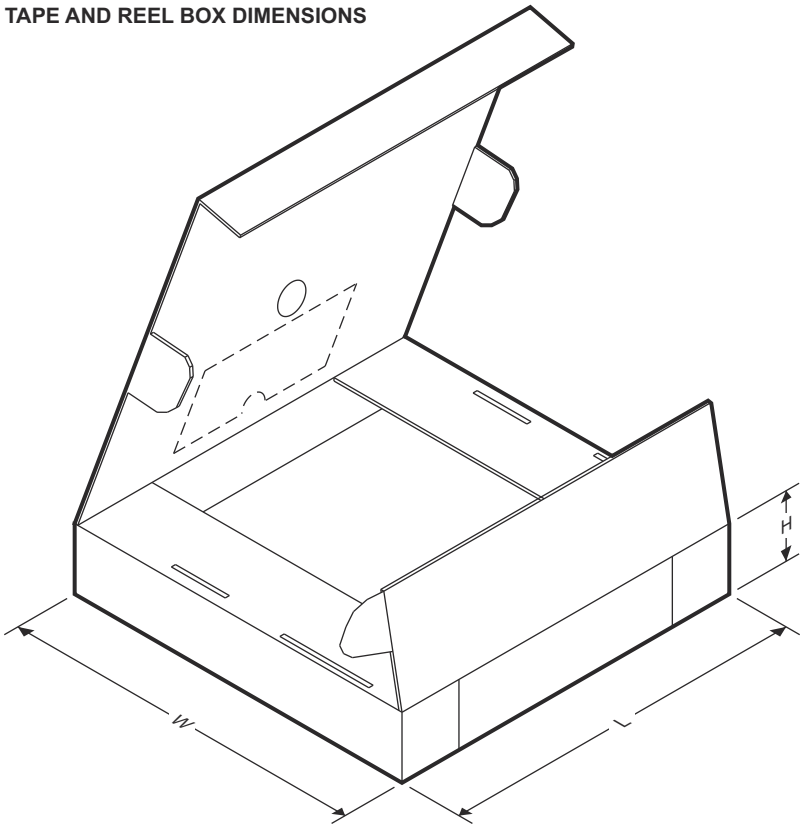
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
XISOW6441DWER	SOIC	DWE	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
XISOW6442DWER	SOIC	DWE	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

ADVANCE INFORMATION

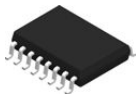
TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
XISOW6441DWER	SOIC	DWE	16	2000	350.0	350.0	43.0
XISOW6442DWER	SOIC	DWE	16	2000	350.0	350.0	43.0

ADVANCE INFORMATION

ADVANCE INFORMATION

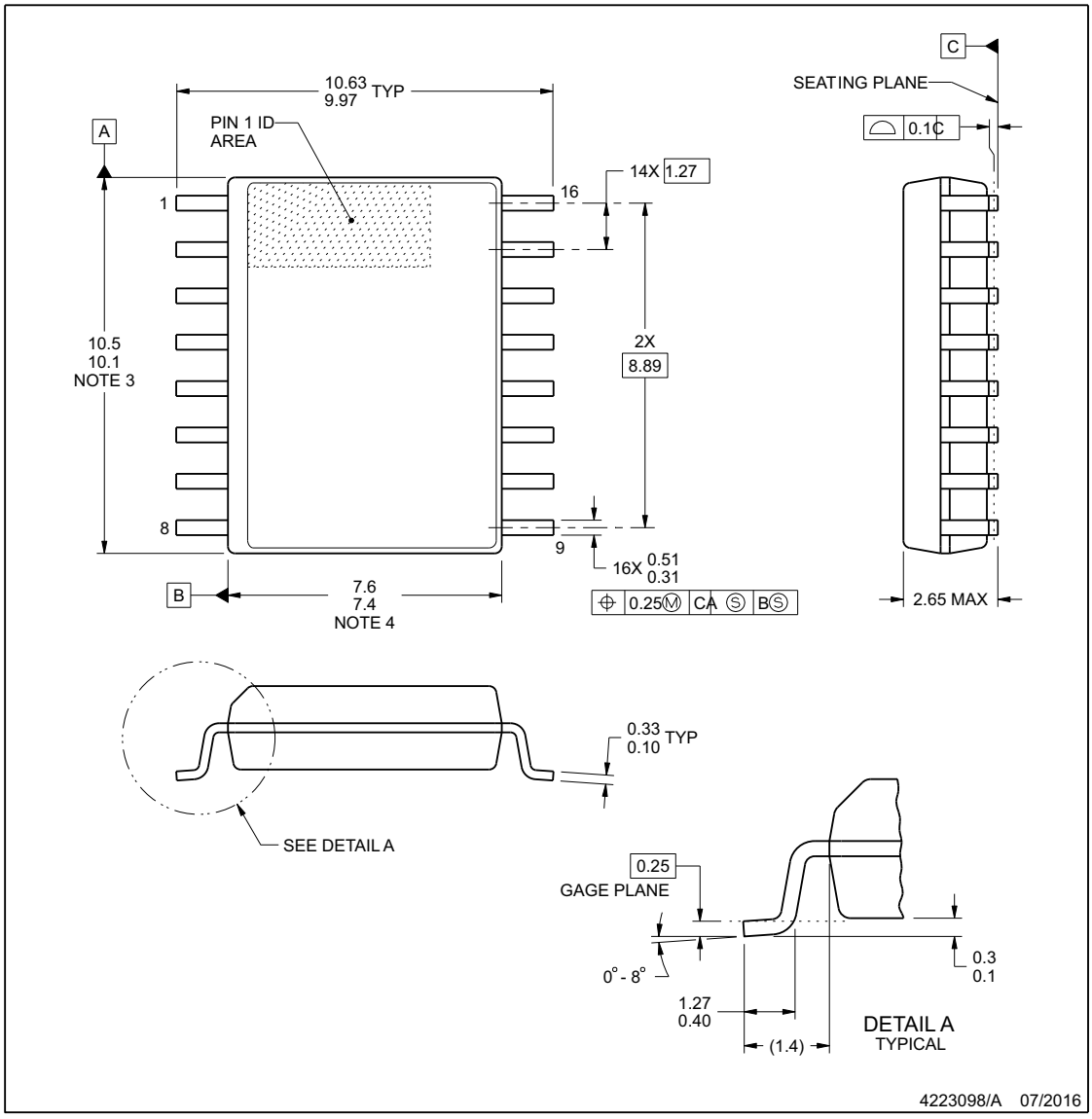


PACKAGE OUTLINE

DWE0016A

SOIC - 2.65 mm max height

SOIC



NOTES:

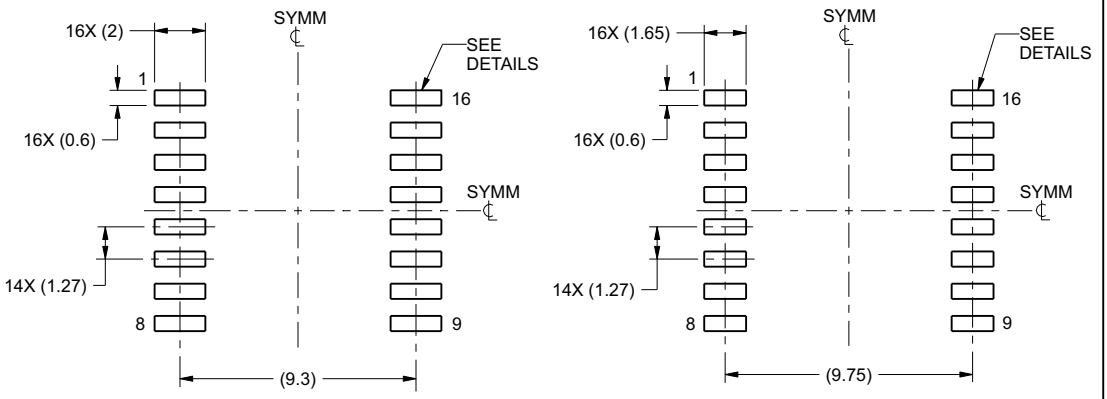
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DWE0016A

SOIC - 2.65 mm max height

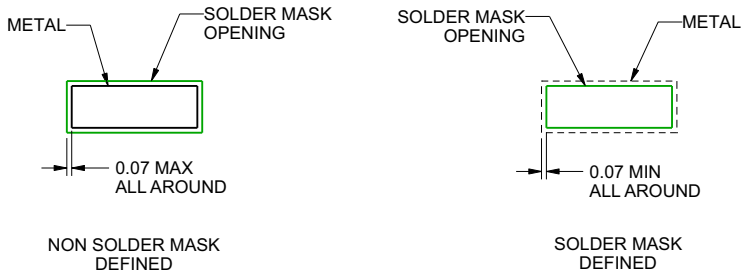
SOIC



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

LAND PATTERN EXAMPLE
SCALE:4X



NON SOLDER MASK DEFINED

SOLDER MASK DEFINED

SOLDER MASK DETAILS

4223098/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

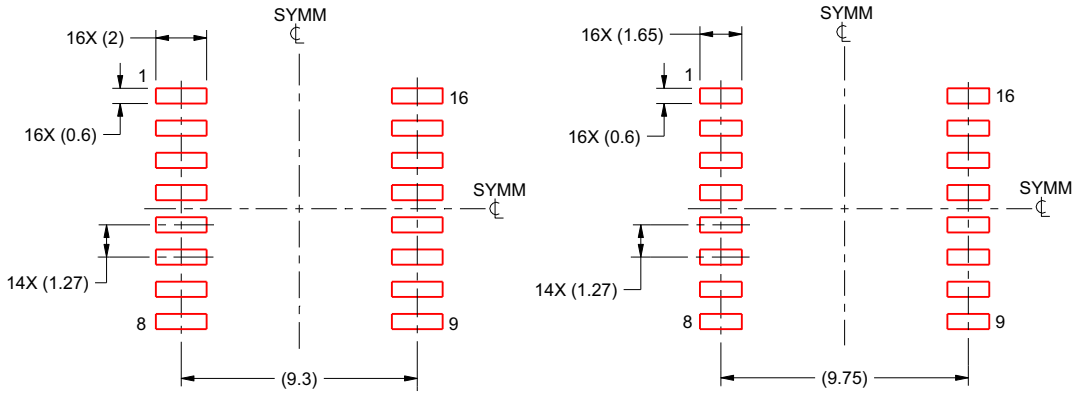
ADVANCE INFORMATION

ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

DWE0016A — SOIC - 2.65 mm max height

SOIC



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

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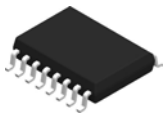
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

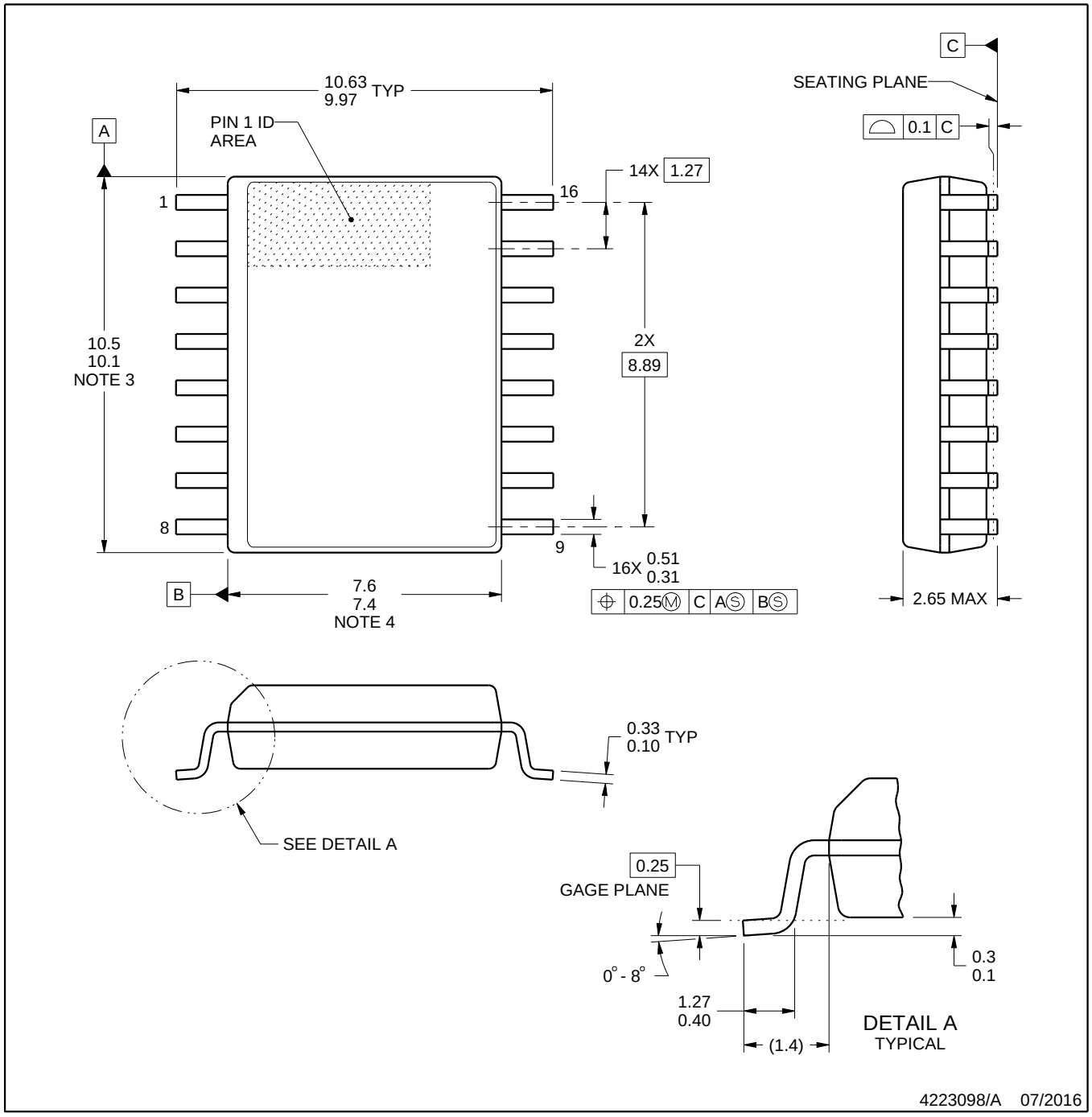


PACKAGE OUTLINE

DWE0016A

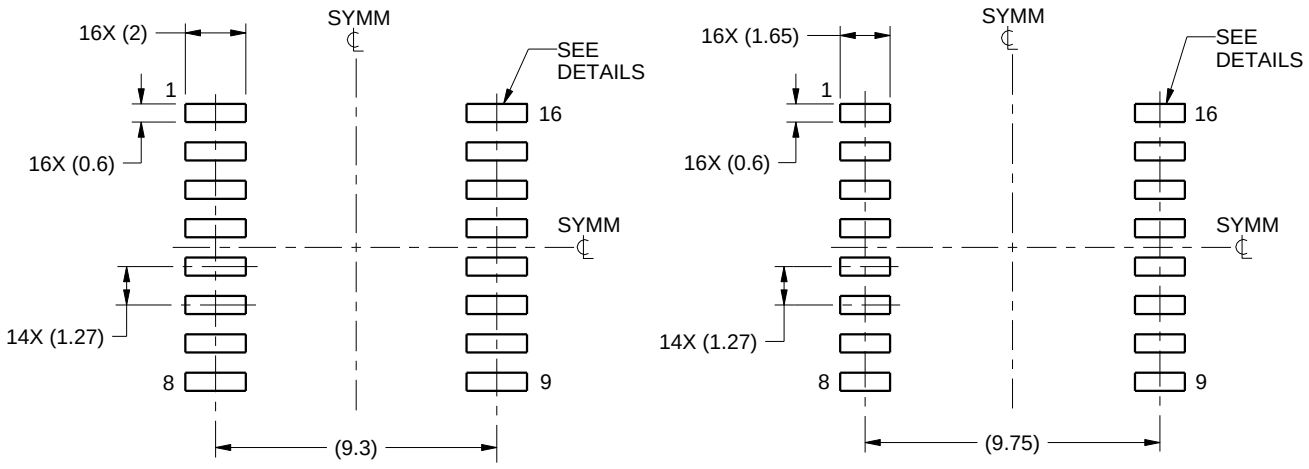
SOIC - 2.65 mm max height

SOIC



NOTES:

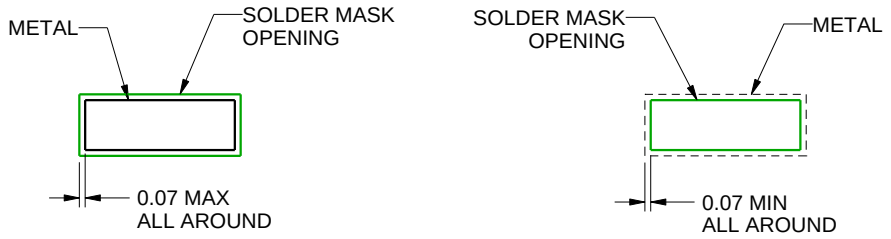
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

LAND PATTERN EXAMPLE
SCALE:4X



NON SOLDER MASK DEFINED

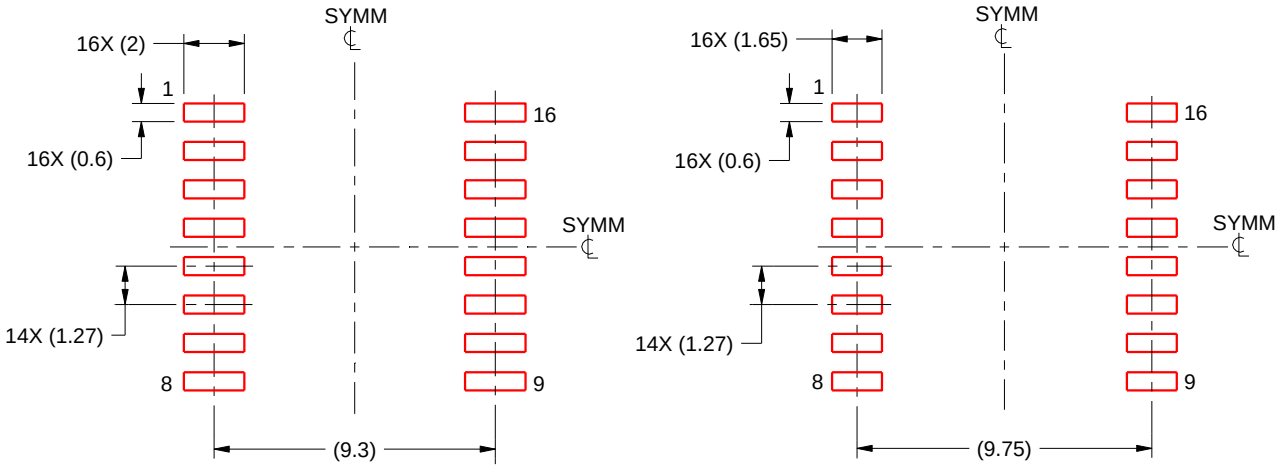
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4223098/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4223098/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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