ESD762 24V, 2-Channel, ESD Protection With 2.5A of 8/20µs Surge Protection

1 Features

- Robust surge protection:
  - IEC 61000-4-5 (8/20µs): 2.5A
- IEC 61000-4-2 level 4 ESD protection:
  - ±18kV contact discharge
  - ±18kV air-gap discharge
- 24V working voltage
- Bidirectional ESD protection
- 2-channel device provides complete ESD and surge protection with single component
- Low clamping voltage protects downstream components
- I/O capacitance = 1.7pF (typical)

2 Applications

- USB power delivery (USB-PD):
  - VBUS protection
  - IO protection (withstand short to VBUS)
- Industrial control networks:
  - Smart distribution system (SDS)
  - DeviceNet IEC 62026-3
  - CANopen – CiA 301/302-2 and EN 50325-4
  - 4/20mA circuits
  - PLC surge protection
  - ADC surge protection

3 Description

ESD762 is a bidirectional ESD protection diode for USB power delivery (USB-PD) and industrial interfaces. ESD762 is rated to dissipate contact ESD that meets or exceeds the maximum level specified in the IEC 61000-4-2 level 4 standard (±18kV contact and ±18kV airgap). The low dynamic resistance and low clamping voltage enables system level protection against transient events. This protection is key because industrial systems require a high level of robustness and reliability.

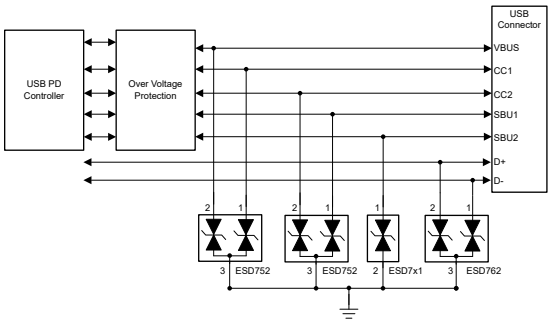
These devices feature a low IO capacitance per channel and a pin-out to suit two IO lines from damage caused by electrostatic discharge (ESD) and other transients. The I_{PP} = 2.5A (8/20µs surge waveform) capability of the ESD762 makes it suitable for protecting USB VBUS against transient surge events as well as industrial I/O lines. Additionally, the 1.7pF line capacitance of the ESD762 is suitable for protecting the slower speed signals for USB power delivery and IO signals for industrial applications.

ESD762 is offered in SOT-23 and DFN1110 packages for easy flow through routing.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE (2)
ESD762	DBZ (SOT-23, 3)	2.92mm × 2.37mm
	DXA (DFN1110, 3)	1.1mm x 1.0mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



USB Power Delivery Typical Application

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4 Pin Configuration and Functions

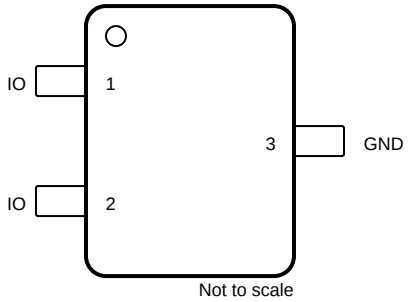


Figure 4-1. DBZ Package, 3-Pin SOT-23 (Top View)

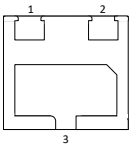


Figure 4-2. DXA Package, 3-Pin DFN1110-3 (Bottom View)

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
IO	1, 2	I/O	ESD protected IO
GND	3	G	Connect to ground.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		MIN	MAX	UNIT
Ppp	IEC 61000-4-5 Power (t_p – 8/20 µs) at 25°C		90	W
I_{pp}	IEC 61000-4-5 current (t_p – 8/20 µs) at 25°C		2.5	A
T_A	Operating free-air temperature	-55	150	°C
T_J	Junction temperature	-55	150	°C
T_{stg}	Storage temperature	-65	155	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings—JEDEC Specification

PARAMETER		TEST CONDITION	VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	± 2500	V
		Charged device model (CDM), per JEDEC specification JS-002 (2)	± 1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufactuuring with a standard ESD control proccess.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufactuuring with a standard ESD control proccess.

5.3 ESD Ratings—IEC Specification

over TA = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITION	VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 Contact Discharge, all pins	±18000	V
		IEC 61000-4-2 Air Discharge, all pins	±18000	V

5.4 Recommended Operating Conditions

PARAMETER		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	-24		24	V
T_A	Operating free-air temperature	-55		150	°C

5.5 Thermal Information

THERMAL METRIC(1)		ESD762		UNIT
		DBZ (SOT-23)	DXA (DFN1110)	
		3 PINS	3 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	325.3	318.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	178.8	174.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	165.5	164.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	52.4	26.0	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	164.4	163.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.6 Electrical Characteristics

over T_A = 25°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	PACKAGE	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage			–24		24	V
V_{BRF}	Forward breakdown voltage(2)	I_{IO} = 10 mA, IO to GND		25.5		35.5	V
V_{BRR}	Reverse breakdown voltage(2)	I_{IO} = –10 mA, IO to GND		–35.5		–25.5	V
V_{CLAMP}	Clamping voltage(3)	I_{PP} = 2.5 A, t_p = 8/20 µs, from IO to GND			36		V
	Clamping voltage(4)	I_{PP} = 16 A, TLP, IO to GND or GND to IO	SOT-23		38		V
			DFN1110-3		42		V
I_{LEAK}	Leakage current	V_{IO} = ±24 V, IO to GND		-50	5	50	nA
R_{DYN}	Dynamic resistance(4)	IO to GND and GND to IO	SOT-23		0.57		Ω
			DFN1110-3		0.68		Ω
C_L	Line capacitance(5)	V_{IO} = 0 V, f = 1 MHz, V_{pp} = 30 mV			1.7	2.8	pF

(1) Measurements made on each IO channel.
(2) V_{BRF} and V_{BRR} are defined as the voltage when +/- 10 mA is applied in the positive or negative direction respectively, before the device latches into the snapback state.
(3) Device stressed with 8/20 µs exponential decay waveform according to IEC 61000-4-5.
(4) Non-repetitive current pulse, Transmission Line Pulse (TLP); square pulse; ANSI / ESD STM5.5.1-2008
(5) Measured from IO to GND on each channel.

5.7 Typical Characteristics – ESD762 (DBZ)

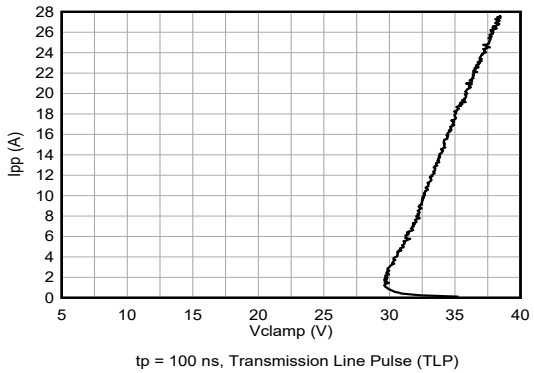


Figure 5-1. Positive TLP Curve

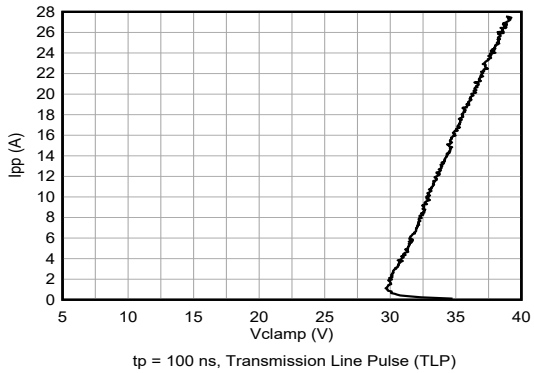


Figure 5-2. Negative TLP Curve

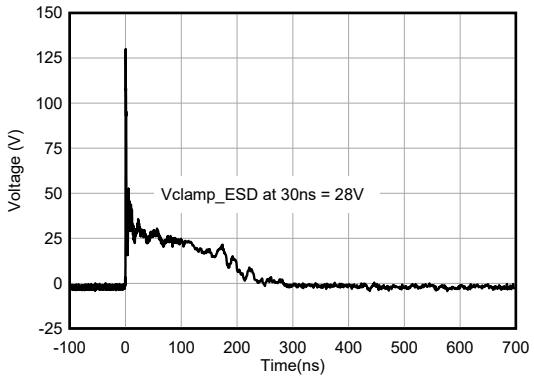


Figure 5-3. +8-kV Clamped IEC Waveform

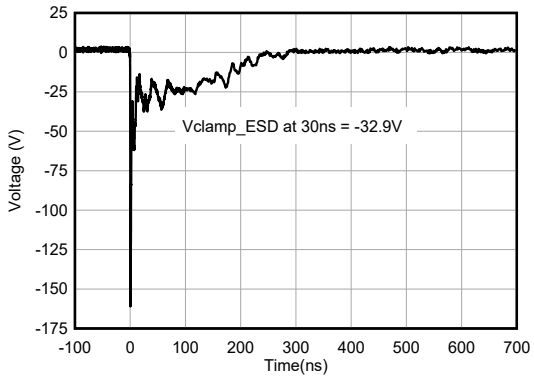


Figure 5-4. −8-kV Clamped IEC Waveform

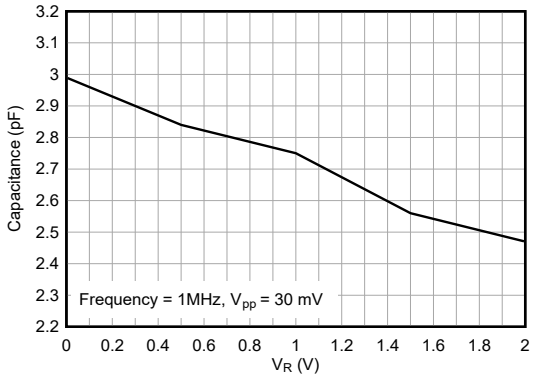


Figure 5-5. Capacitance vs. Bias Voltage

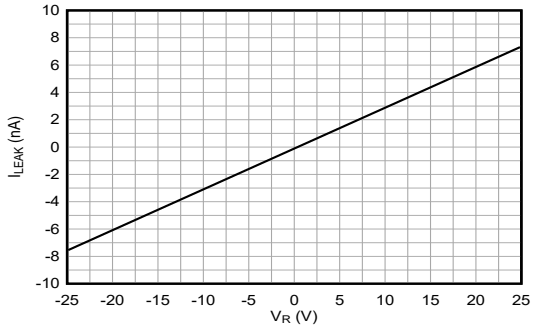


Figure 5-6. Leakage Current vs. Bias Voltage Across Temperature

5.7 Typical Characteristics – ESD762 (DBZ) (continued)

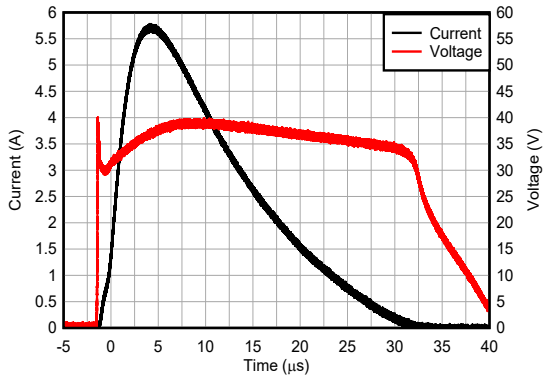


Figure 5-7. 8/20 µs Surge Response at 5.7A

5.8 Typical Characteristics – ESD762 (DXA)

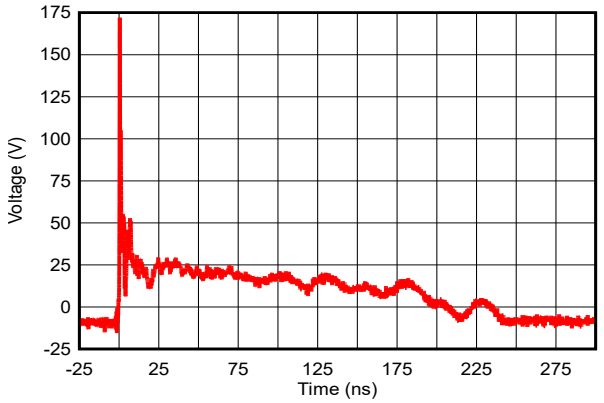


Figure 5-8. +8kV Clamped IEC Waveform

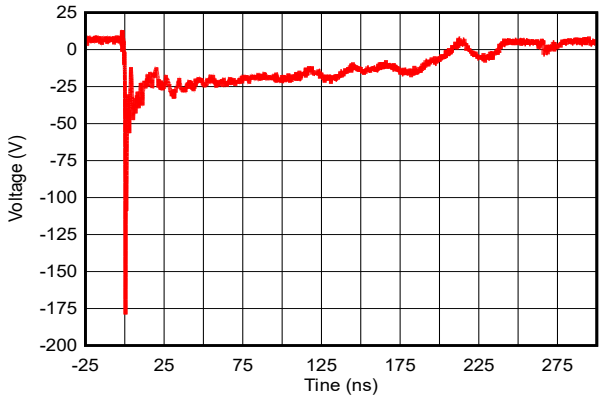


Figure 5-9. −8kV Clamped IEC Waveform

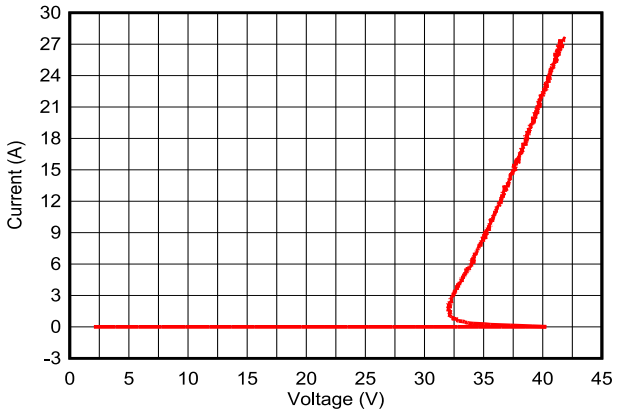


Figure 5-10. Positive TLP Curve

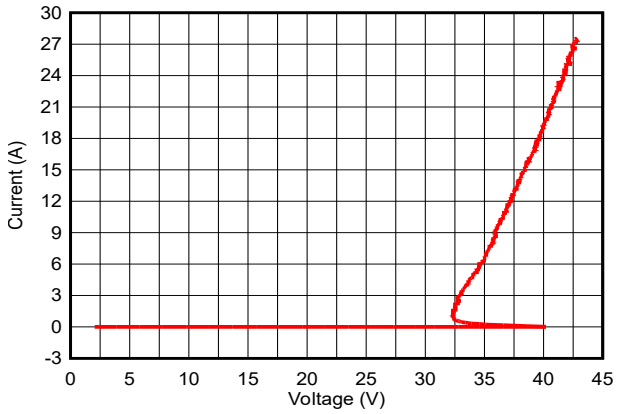


Figure 5-11. Negative TLP Curve

5.8 Typical Characteristics – ESD762 (DXA) (continued)

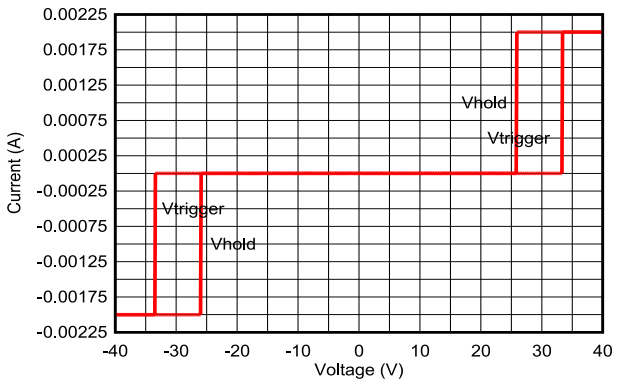


Figure 5-12. DC-IV Characteristics

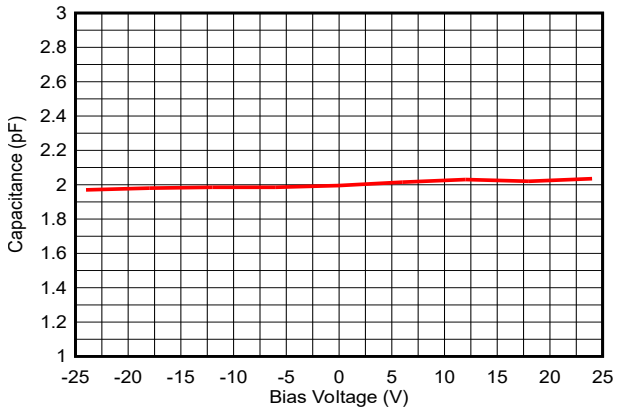


Figure 5-13. Capacitance vs. Bias Voltage

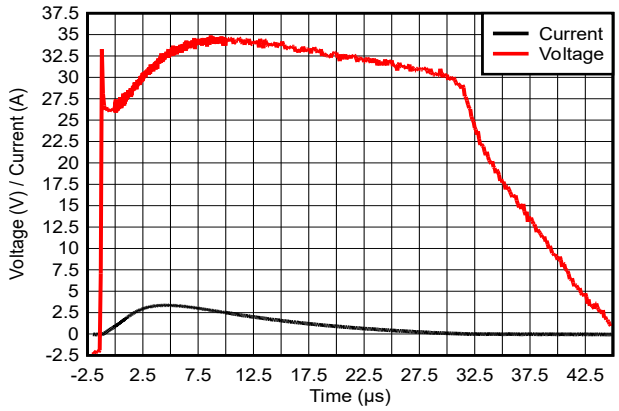


Figure 5-14. 8/20µs Surge Response

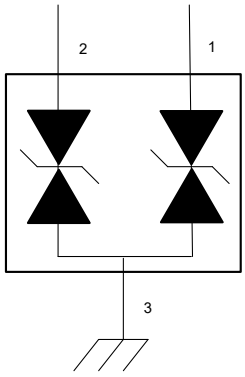
6 Detailed Description

6.1 Overview

ESD762 is a dual-channel ESD TVS diode in a SOT-23 leaded package and a DFN1110 leadless package. This product offers IEC 61000-4-2 ±18kV contact & air-gap ESD protection respectively, and has a clamp circuit with a back-to-back TVS diode for bidirectional signal support.

A typical application of this product is the ESD protection for USB-PD slower speed signals (CC1, CC2, SBU1, SBU2, D+, and D-). The I_{PP} = 2.5A (8/20µs surge waveform) capability of the ESD762 makes it suitable for protecting VBUS. ESD762 is also a good fit for protecting industrial IOs requiring 2.5A or less of surge current protection. The 1.7pF line capacitance of this ESD protection diode is suitable for USB-PD slower speed signals and industrial IO applications.

6.2 Functional Block Diagram



6.3 Feature Description

ESD762 is a bidirectional TVS diodes with a high ESD protection level. This device protects the circuit from ESD strikes up to ±18kV contact and ±18kV air-gap as specified in the IEC 61000-4-2 standard. The ESD762 can also handle up to 2.5A of surge current (IEC 61000-4-5 8/20 µs). The I/O capacitance of 1.7pF (typical) are suitable for USB power delivery slower speed signals and industrial applications. This clamping device has a small dynamic resistance, which makes the clamping voltage low when the device is actively protecting other circuits.

For example, the ESD762 clamping voltage is only 36V when the device is taking 2.5A transient current. The breakdown is bidirectional so these protection devices are a good fit for applications requiring postive and negative polarity protection. Low leakage allows these diodes to conserve power when working below the V_{RWM}. The temperature range of −55°C to +150°C makes this ESD device work at extensive temperatures in most environments. The leaded SOT-23 package is good for applications requiring automatic optical inspection (AOI).

6.3.1 Temperature Range

These devices are qualified to operate from –55°C to +150°C.

6.3.2 IEC 61000-4-5 Surge Protection

The IO pins can withstand surge events up to 2.5A (8/20µs waveform) for the ESD762. An ESD-surge clamp diverts this current to ground.

6.3.3 IO Capacitance

The capacitance between the I/O pins is 1.7pF for the ESD762. These capacitances are designed for USB power delivery slower speed signals and industrial applications.

6.3.4 Dynamic Resistance

The IO pins feature an ESD clamp that has a low R_{DYN} of 0.57Ω for the SOT-23 package, and 0.68Ω for the DFN1110-3 package, which prevents system damage during ESD events.

6.3.5 DC Breakdown Voltage

The DC breakdown voltage between the IO pins is a minimum of ± 25.5V. This protects sensitive equipment is protected from surges above the reverse standoff voltage of ± 24V.

6.3.6 Ultra Low Leakage Current

The IO pins feature an ultra-low leakage current of 50nA (maximum) with a bias of ± 24V.

6.3.7 Clamping Voltage

The IO pins feature an ESD clamp that is capable of clamping the voltage to 36V (I_{PP} = 2.5A for 8/20µs surge waveform), 38V (I_{PP} = 16A for TLP, SOT-23 package), and 42V (I_{PP} = 16A for TLP, DFN1110-3 package).

6.3.8 Industry Standard Leaded Packages

These devices feature industry standard SOT-23 (DBZ) and DFN1110-3 packages for automatic optical inspection (AOI).

6.4 Device Functional Modes

The ESD762 are dual channel passive clamp devices that have low leakage during normal operation when the voltage between IO and GND is below V_{RWM}, and activate when the voltage between IO and GND goes above V_{BR}. During IEC 61000-4-2 ESD events, transient voltages as high as ±18kV can be clamped on either channel. When the voltages on the protected lines fall below the V_{HOLD}, the device reverts back to the low leakage passive state.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

ESD762 is a dual channel TVS diode which is used to provide a path to ground for dissipating ESD events on USB-PD or industrial IO signal lines. As the current from the ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage (V_{CLAMP}) to a safe level for the protected IC.

7.2 Typical Application

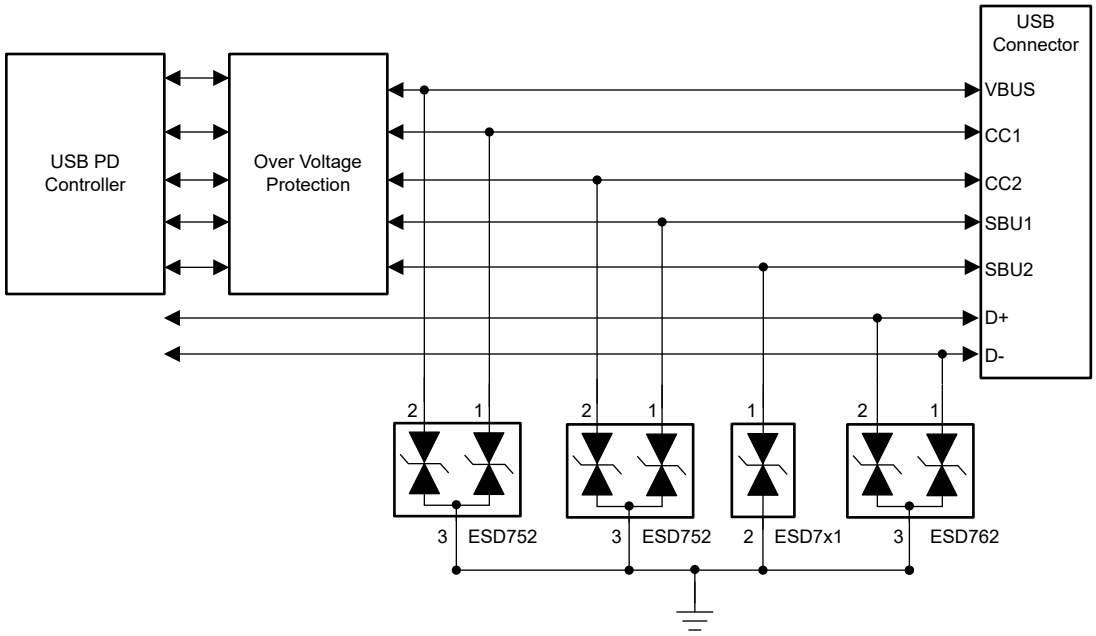


Figure 7-1. USB Power Delivery Typical Application

7.2.1 Design Requirements

For this design example, the ESD762 are used to provide ESD protection on a USB-PD connector. Table 7-1 lists the known design parameters for this application.

Table 7-1. Design Parameters for the USB Power Delivery Typical Application

Design Parameter	Value
Diode configuration	Bidirectional
VBUS Voltage	+ 20V
V_{IO} signal range	+ 3.3V
V_{RWM}	± 24V
Short to VBUS event on V_{IO}	± 20V
Data rate	Up to 480Mbps

7.2.2 Detailed Design Procedure

The ESD762 has a V_{RWM} of ± 24V to prevent the diode from being damaged during a short event that can occur when one of the USB-PD slower speed lines (CC1, CC2, SBU1, SBU2, D+, and D-) is shorted to VBUS. The bidirectional characteristic protects both positive and negative polarity. The low 1.7pF capacitance of the ESD762 device enables data rates up to 480Mbps, which allows the designer to meet the requirements for the D+ and D- signals. The ESD762 has an I_{PP} = 2.5A (8/20µs) surge current capability making it suitable for protecting the VBUS power rail.

7.2.3 Application Curves

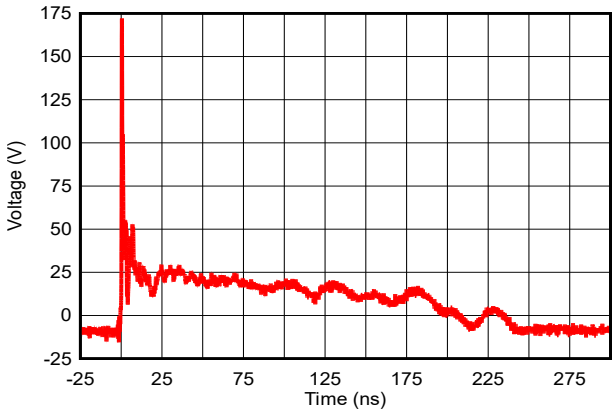


Figure 7-2. +8kV Clamped IEC Waveform

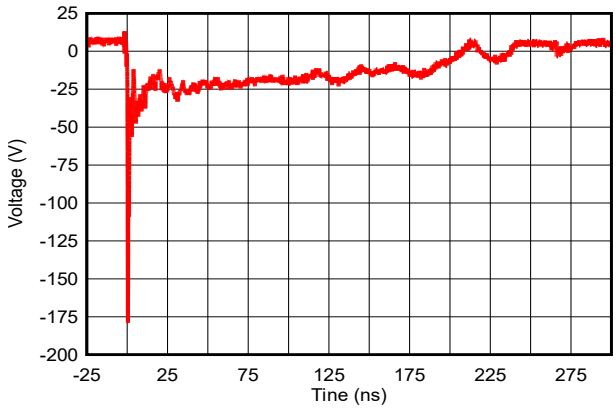


Figure 7-3. −8kV Clamped IEC Waveform

8 Power Supply Recommendations

These are passive TVS diode-based ESD protection devices; therefore, there is no requirement to power it. Ensure that the maximum voltage specifications for each pin are not violated.

9 Layout

9.1 Layout Guidelines

- The optimum placement of the device is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.
- If pin 3 is connected to ground, use a thick and short trace for this return path.

9.2 Layout Example

This is a typical example of a dual channel IO routing.

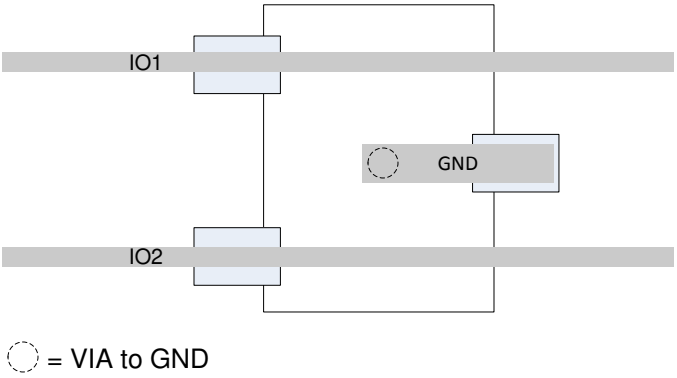


Figure 9-1. Routing with DBZ Package

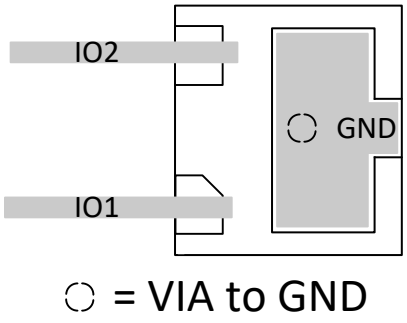


Figure 9-2. Routing with DXA Package

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *ESD Layout Guide* user's guide
- Texas Instruments, *ESD and Surge Protection for USB Interfaces* application note
- Texas Instruments, *ESD Protection Diodes EVM* user's guide
- Texas Instruments, *Generic ESD Evaluation Module* user's guide
- Texas Instruments, *Reading and Understanding an ESD Protection* data sheet

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from December 1, 2025 to April 29, 2026 (from Revision C (December 2025) to Revision D (April 2026))	**Page**
• Removed ESD752 specifications from the data sheet	1
• Added DFN1110-3 package to device package options	1

Changes from Revision B (November 2022) to Revision C (December 2025)	Page
• Removed ESD752 specifications from the data sheet	1
• Added DFN1110-3 package to device package options	1

Changes from Revision A (August 2022) to Revision B (November 2022)	Page
• Added ESD762 Specifications to the data sheet	1

Changes from Revision * (May 2022) to Revision A (August 2022)	Page
• Changed the status of the data sheet from: *Advanced Information* to: *Production Data*	1

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ESD762DBZR	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	2RK8
ESD762DBZR.B	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	2RK8
ESD762DXAR	Active	Production	USON (DXA) | 3	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-55 to 150	1X3

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

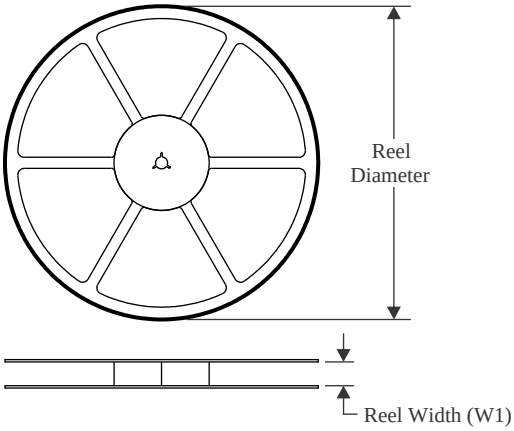
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

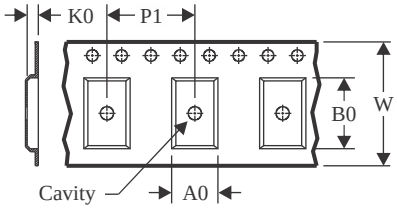
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

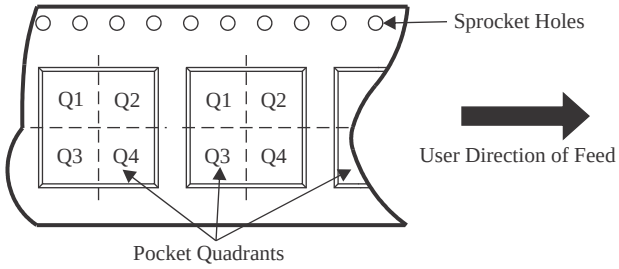


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

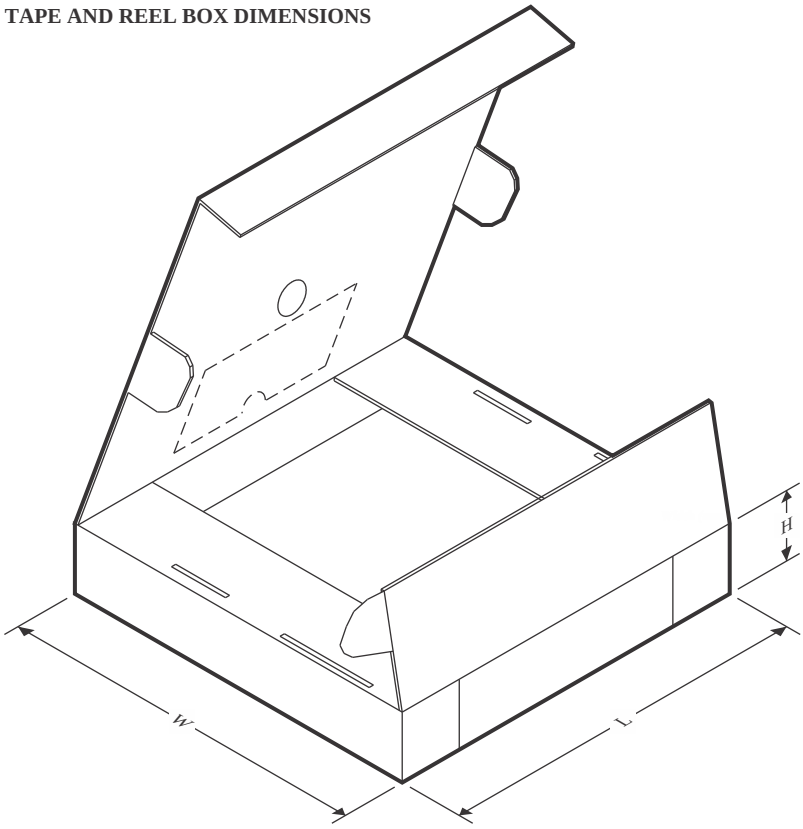
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ESD762DBZR	SOT-23	DBZ	3	3000	180.0	8.4	2.9	3.35	1.35	4.0	8.0	Q3
ESD762DXAR	USON	DXA	3	3000	180.0	8.4	1.2	1.3	0.65	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

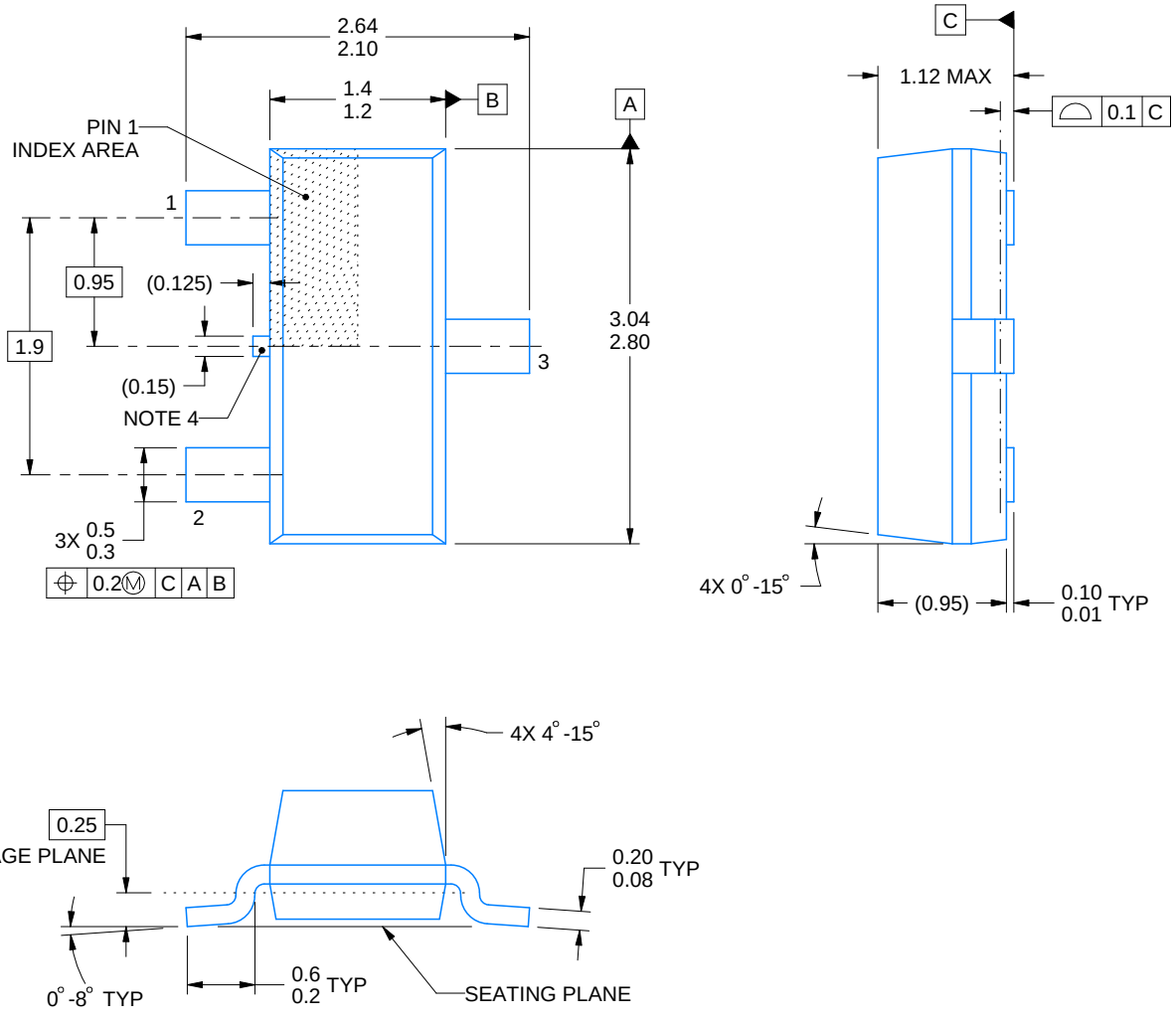
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ESD762DBZR	SOT-23	DBZ	3	3000	210.0	185.0	35.0
ESD762DXAR	USON	DXA	3	3000	210.0	185.0	35.0

PACKAGE OUTLINE

DBZ0003A

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



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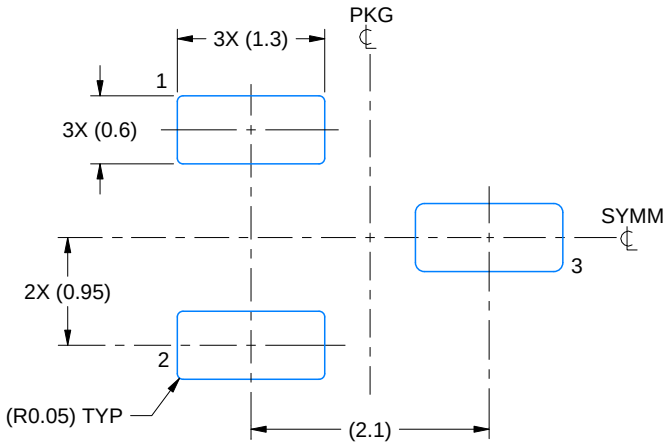
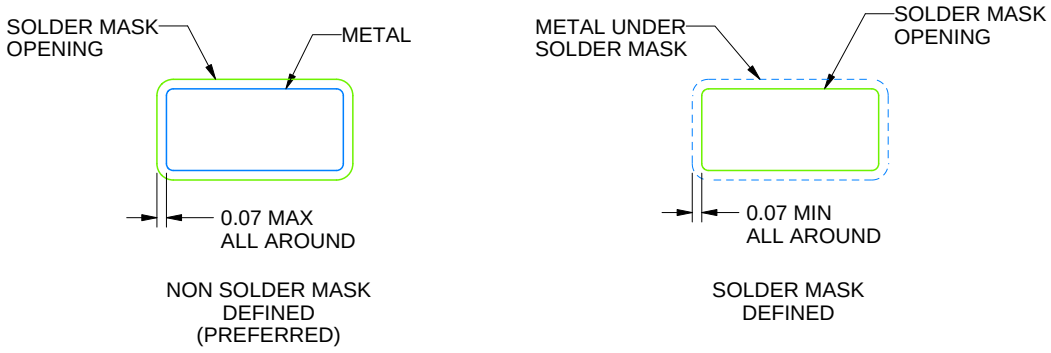
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-236, except minimum foot length.
4. Support pin may differ or may not be present.
5. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS

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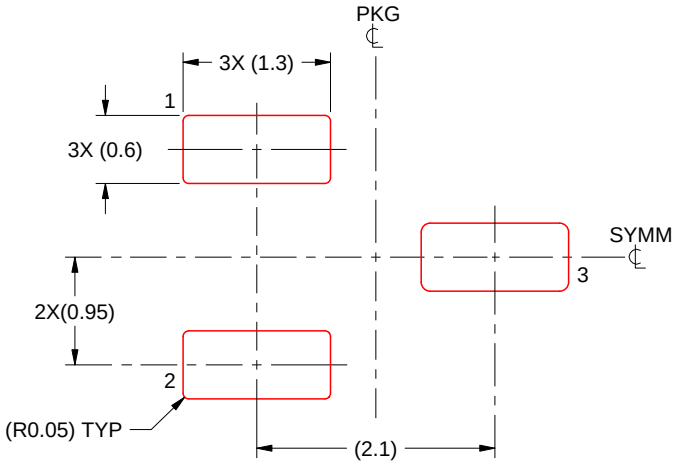
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

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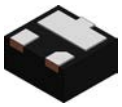
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

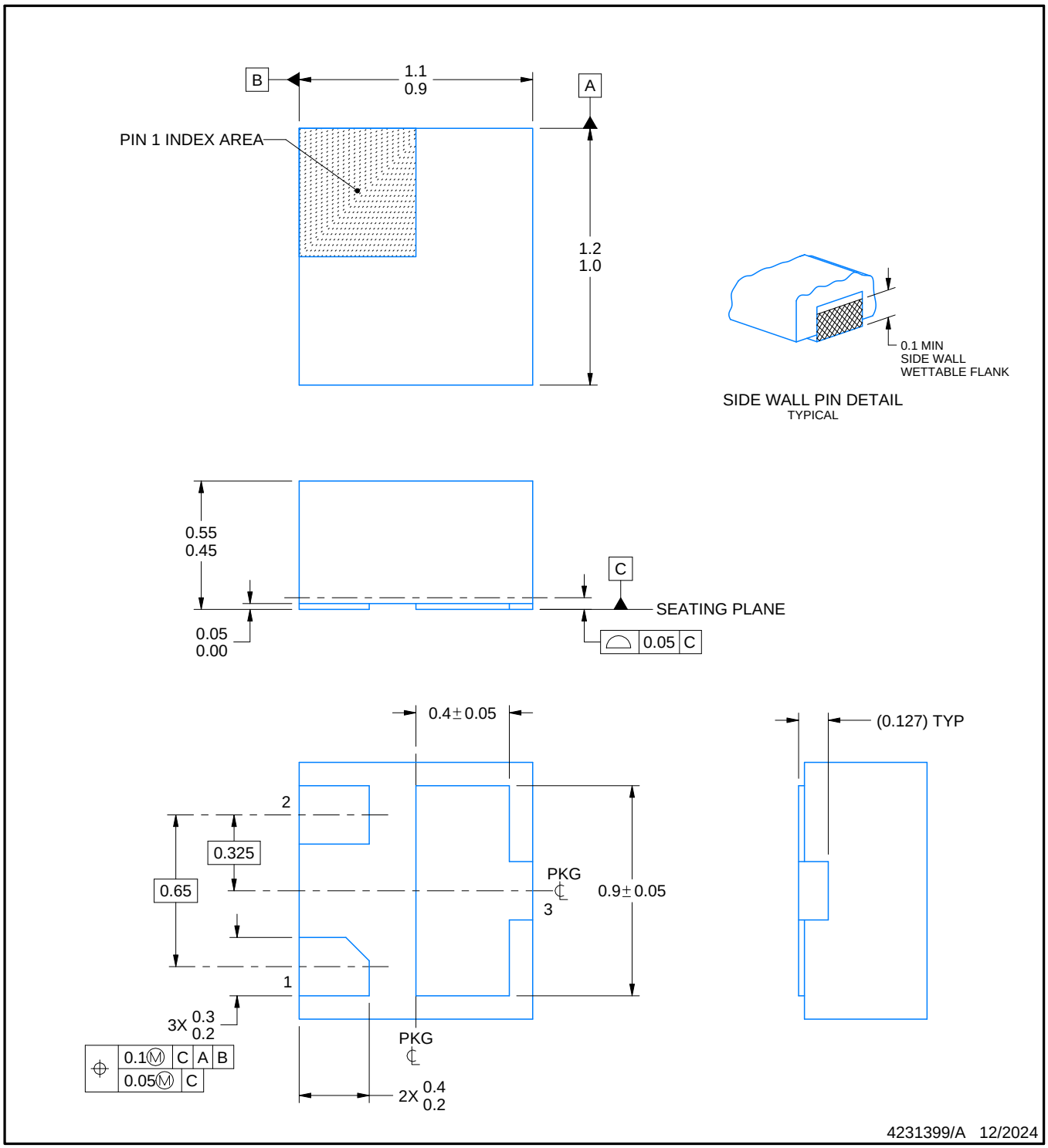
DXA0003A



PACKAGE OUTLINE

USON - 0.55 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

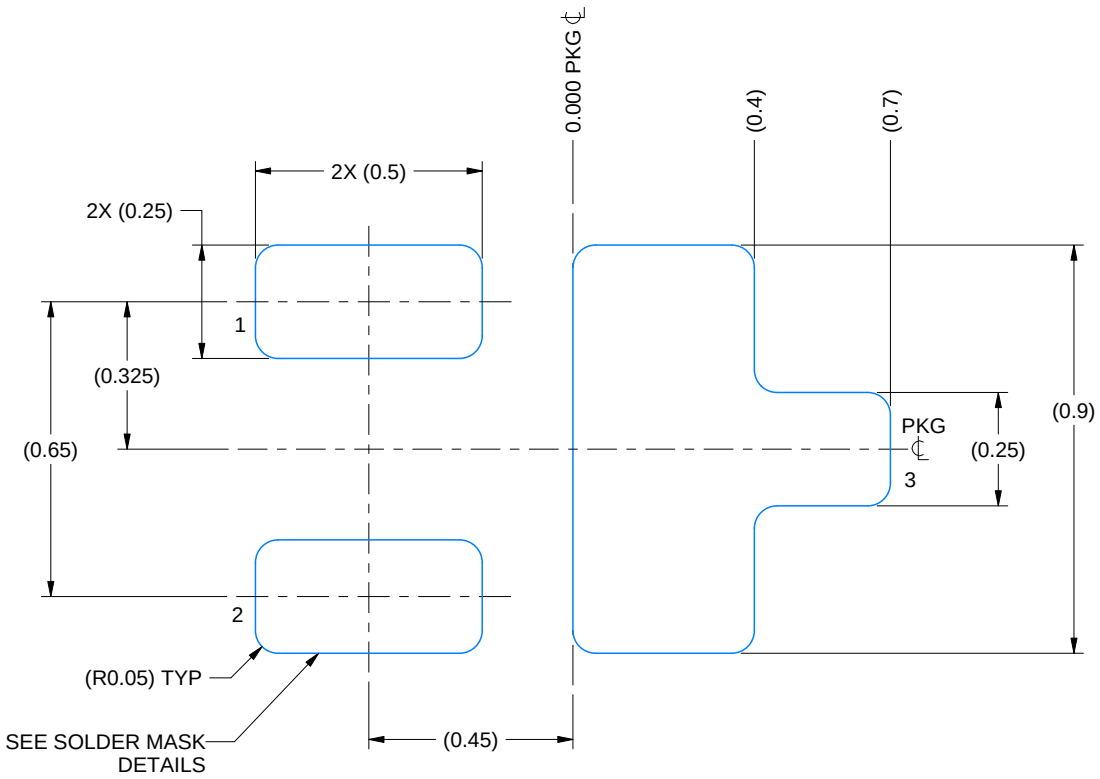
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

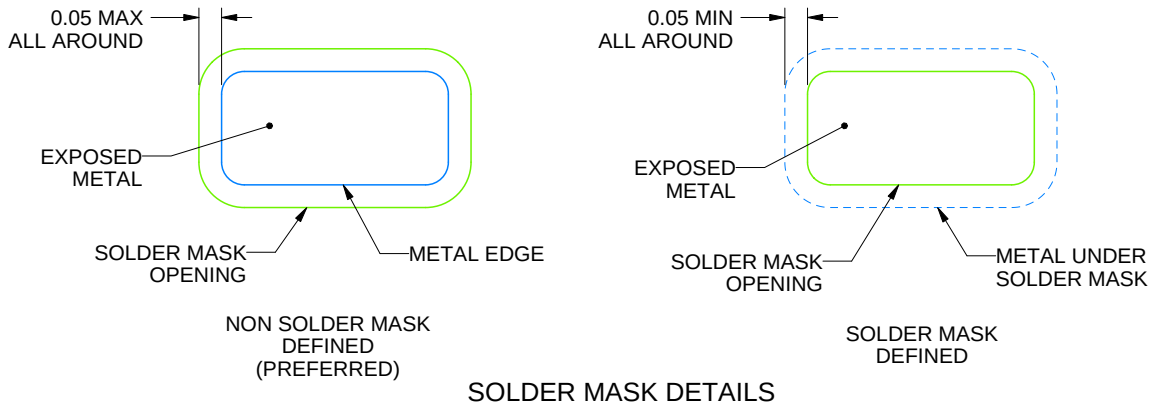
DXA0003A

USON - 0.55 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 60X



SOLDER MASK DETAILS

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NOTES: (continued)

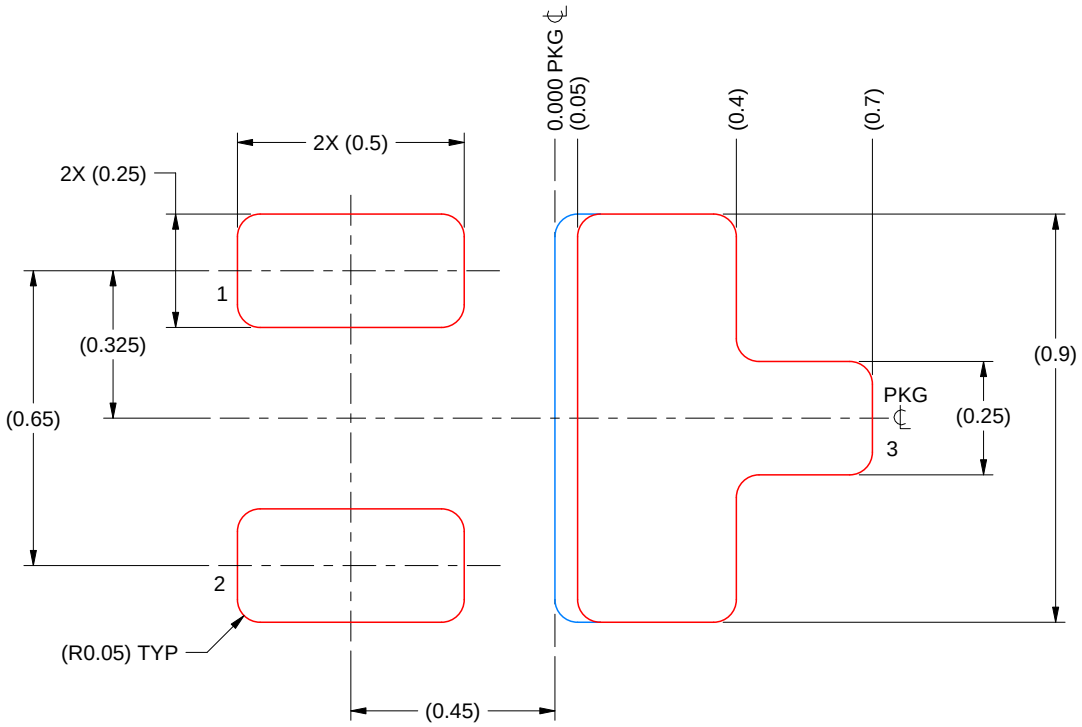
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DXA0003A

USON - 0.55 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 60X

EXPOSED PAD 3
90% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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